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Express Mail mailing number:	Date of deposit: 5/22/2008
File reference no.: S-0039 PCT	International application no. (if known):
Customer Number ¹ : 38139	Earliest priority date claimed (Day/Month/Year): 5/25/2007
Title of the invention: Fully Connected Generalized Multi-Link Multi-Stage Networks	

¹ Customer Number will allow access to the application in Private PAIR but cannot be used to establish or change the correspondence address. **This is a new International Application****SCREENING DISCLOSURE INFORMATION:**

In order to assist in screening the accompanying international application for purposes of determining whether a license for foreign transmittal should and could be granted and for other purposes, the following information is supplied. (check as boxes as apply):

- The invention disclose was **not** made in the United States of America.
- There is no prior U.S. application relating to this invention.
- The following prior U.S. application(s) contain subject matter which is related to the invention disclosed in the attached international application. (NOTE: priority to these applications may or may not be claimed on the Request (form PCT/RO/101) and this listing does **not** constitute a claim for priority.)

application no.	60/940, 389	filed on	5/25/2007
application no.	60/940, 392	filed on	5/25/2007

- The present international application contains additional subject matter not found in the prior U.S. application(s) identified above. The additional subject matter is found on pages 207-211 and **DOES NOT ALTER** **MIGHT BE CONSIDERED TO ALTER** the general nature of the invention in a manner which would require the U.S. application to have been made available for inspection by the appropriate defense agencies under 35 U.S.C. 181 and 37 C.F.R. 5.15.

Itemized list of contents

Sheets of Request form: 3	Check no.:
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The person signing this form is:	<input checked="" type="checkbox"/> Applicant	Venkat Konda
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This collection of information is required by 37 CFR 1.10 and 1.412. The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 15 minutes to complete, including gathering information, preparing, and submitting the completed form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.

SEND TO: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Filer:	Venkar Konda
Attorney Docket Number:	S-0039PCT

International Application for filing in the US receiving office Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Transmittal fee	1601	1	300	300
PCT Search Fee- no prior US appl filed	1602	1	1800	1800
Intl Filing Fee (1st-30 Pgs.) PCT Easy	1701	1	1173	1173
Suppl. Intl Filing Fee (each page > 30)	1703	320	14	4480

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Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
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Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				7753

Electronic Acknowledgement Receipt

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Title of Invention:	FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
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1	Specification	S-0039PCT.pdf	1016396	no	222
			f551548becc5fade4aff2672e1b6fdeda4a6df2		
Warnings:					
Information:					
2	Drawings-only black and white line drawings	S-0039PCT-FIGs.pdf	901693	no	125
			bf3afa7239e79ff7683413abb131dcb12de87c5		
Warnings:					
Information:					
3	RO/101 - Request form for new IA - Conventional	S-0039PCT-RO-101.pdf	271086	no	3
			5c747bf9e60067017073b92c4f6d2a145cc27c74		
Warnings:					
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4	PCT-Transmittal Letter	S-0039PCT-PTO-1382.pdf	105350	no	1
			42a5e375c3c54725e29049bad033d3a75aabe99e		
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5	Fee payment - International Application	S-0039PCT-Fee.pdf	70340	no	1
			ade90ee7e5473f0066ffcf3deb25fd6fd44260b		
Warnings:					
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6	Fee Worksheet (PTO-06)	fee-info.pdf	8557	no	2
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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS

Venkat Konda

5 CROSS REFERENCE TO RELATED APPLICATIONS

This application is Continuation In Part PCT Application to and incorporates by reference in its entirety the U.S. Provisional Patent Application Serial No. 60/940, 389 entitled "FULLY CONNECTED GENERALIZED REARRANGEABLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda
10 assigned to the same assignee as the current application, filed May 25, 2007.

This application is Continuation In Part PCT Application to and incorporates by reference in its entirety the U.S. Provisional Patent Application Serial No. 60/940, 392 entitled "FULLY CONNECTED GENERALIZED STRICTLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same
15 assignee as the current application, filed concurrently.

This application is Continuation In Part PCT Application to and incorporates by reference in its entirety the U.S. Provisional Patent Application Serial No. 60/940, 391 entitled "FULLY CONNECTED GENERALIZED FOLDED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application,
20 filed concurrently.

This application is related to and incorporates by reference in its entirety the PCT Application Serial No. PCT/US08/56064 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed March 6, 2008, the U.S. Provisional Patent
25 Application Serial No. 60/905,526 entitled "LARGE SCALE CROSSPOINT REDUCTION WITH NONBLOCKING UNICAST & MULTICAST IN ARBITRARILY LARGE MULTI-STAGE NETWORKS" by Venkat Konda assigned to

the same assignee as the current application, filed March 6, 2007, and the U.S. Provisional Patent Application Serial No. 60/940, 383 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

5 This application is related to and incorporates by reference in its entirety the PCT Application Docket No. S-0038PCT entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed concurrently, the U.S. Provisional Patent Application Serial No. 60/940, 387 entitled "FULLY CONNECTED GENERALIZED
10 BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007, and the U.S. Provisional Patent Application Serial No. 60/940, 390 entitled "FULLY CONNECTED GENERALIZED MULTI-LINK BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

15 This application is related to and incorporates by reference in its entirety the PCT Application Docket No. S-0045PCT entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed concurrently, and the U.S. Provisional Patent Application Serial No. 60/940, 394 entitled "VLSI LAYOUTS OF FULLY
20 CONNECTED GENERALIZED NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007..

 This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application Serial No. 60/984, 724 entitled "VLSI LAYOUTS OF FULLY CONNECTED NETWORKS WITH LOCALITY EXPLOITATION" by Venkat
25 Konda assigned to the same assignee as the current application, filed November 2, 2007.

 This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application Serial No. 61/018, 494 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED AND PYRAMID NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed January 1, 2008.

BACKGROUND OF INVENTION

Clos switching network, Benes switching network, and Cantor switching network are a network of switches configured as a multi-stage network so that fewer switching points are necessary to implement connections between its inlet links (also called "inputs") and outlet links (also called "outputs") than would be required by a single stage (e.g. crossbar) switch having the same number of inputs and outputs. Clos and Benes networks are very popularly used in digital crossconnects, switch fabrics and parallel computer systems. However Clos and Benes networks may block some of the connection requests.

There are generally three types of nonblocking networks: strictly nonblocking; wide sense nonblocking; and rearrangeably nonblocking (See V.E. Benes, "Mathematical Theory of Connecting Networks and Telephone Traffic" Academic Press, 1965 that is incorporated by reference, as background). In a rearrangeably nonblocking network, a connection path is guaranteed as a result of the network's ability to rearrange prior connections as new incoming calls are received. In strictly nonblocking network, for any connection request from an inlet link to some set of outlet links, it is always possible to provide a connection path through the network to satisfy the request without disturbing other existing connections, and if more than one such path is available, any path can be selected without being concerned about realization of future potential connection requests. In wide-sense nonblocking networks, it is also always possible to provide a connection path through the network to satisfy the request without disturbing other existing connections, but in this case the path used to satisfy the connection request must be carefully selected so as to maintain the nonblocking connecting capability for future potential connection requests.

Butterfly Networks, Banyan Networks, Batcher-Banyan Networks, Baseline Networks, Delta Networks, Omega Networks and Flip networks have been widely studied particularly for self routing packet switching applications. Also Benes Networks with radix of two have been widely studied and it is known that Benes Networks of radix two are shown to be built with back to back baseline networks which are rearrangeably nonblocking for unicast connections.

U.S. Patent 5,451,936 entitled “Non-blocking Broadcast Network” granted to Yang et al. is incorporated by reference herein as background of the invention. This patent describes a number of well known nonblocking multi-stage switching network designs in the background section at column 1, line 22 to column 3, 59. An article by Y. Yang, and G.M., Masson entitled, “Non-blocking Broadcast Switching Networks” IEEE Transactions on Computers, Vol. 40, No. 9, September 1991 that is incorporated by reference as background indicates that if the number of switches in the middle stage, m , of a three-stage network satisfies the relation $m \geq \min((n-1)(x+r^{1/x}))$ where $1 \leq x \leq \min(n-1, r)$, the resulting network is nonblocking for multicast assignments. In the relation, r is the number of switches in the input stage, and n is the number of inlet links in each input switch.

U.S. Patent 6,885,669 entitled “Rearrangeably Nonblocking Multicast Multi-stage Networks” by Konda showed that three-stage Clos network is rearrangeably nonblocking for arbitrary fan-out multicast connections when $m \geq 2 \times n$. And U.S. Patent 6,868,084 entitled “Strictly Nonblocking Multicast Multi-stage Networks” by Konda showed that three-stage Clos network is strictly nonblocking for arbitrary fan-out multicast connections when $m \geq 3 \times n - 1$.

In general multi-stage networks for stages of more than three and radix of more than two are not well studied. An article by Charles Clos entitled “A Study of Non-Blocking Switching Networks” The Bell Systems Technical Journal, Volume XXXII, Jan. 1953, No.1, pp. 406-424 showed a way of constructing large multi-stage networks by recursive substitution with a crosspoint complexity of $d^2 \times N \times (\log_d N)^{2.58}$ for strictly nonblocking unicast network. Similarly U.S. Patent 6,885,669 entitled “Rearrangeably Nonblocking Multicast Multi-stage Networks” by Konda showed a way of constructing large multi-stage networks by recursive substitution for rearrangeably nonblocking multicast network. An article by D. G. Cantor entitled “On Non-Blocking Switching Networks” 1: pp. 367-377, 1972 by John Wiley and Sons, Inc., showed a way of constructing large multi-stage networks with a crosspoint complexity of $d^2 \times N \times (\log_d N)^2$ for strictly nonblocking unicast, (by using $\log_d N$ number of Benes Networks for $d = 2$) and without counting the crosspoints in multiplexers and

demultiplexers. Jonathan Turner studied the cascaded Benes Networks with radices larger than two, for nonblocking multicast with 10 times the crosspoint complexity of that of nonblocking unicast for a network of size $N=256$.

5 The crosspoint complexity of all these networks is prohibitively large to implement the interconnect for multicast connections particularly in field programmable gate array (FPGA) devices, programmable logic devices (PLDs), field programmable interconnect Chips (FPICs), digital crossconnects, switch fabrics and parallel computer systems.

10 SUMMARY OF INVENTION

A generalized multi-link multi-stage network comprising $(2 \times \log_d N) - 1$ stages is operated in strictly nonblocking manner for unicast includes an input stage having $\frac{N}{d}$ switches with each of them having d inlet links and $2 \times d$ outgoing links connecting to second stage switches, an output stage having $\frac{N}{d}$ switches with each of them having d outlet links and $2 \times d$ incoming links connecting from switches in the penultimate stage. The network also has $(2 \times \log_d N) - 3$ middle stages with each middle stage having $\frac{N}{d}$ switches, and each switch in the middle stage has $2 \times d$ incoming links connecting from the switches in its immediate preceding stage, and $2 \times d$ outgoing links connecting to the switches in its immediate succeeding stage. Also the same generalized multi-link multi-stage network is operated in rearrangeably nonblocking manner for arbitrary fan-out multicast and each multicast connection is set up by use of at most two outgoing links from the input stage switch.

A generalized multi-link multi-stage network comprising $(2 \times \log_d N) - 1$ stages is operated in strictly nonblocking manner for multicast includes an input stage having $\frac{N}{d}$ switches with each of them having d inlet links and $3 \times d$ outgoing links connecting to

second stage switches, an output stage having $\frac{N}{d}$ switches with each of them having d outlet links and $3 \times d$ incoming links connecting from switches in the penultimate stage. The network also has $(2 \times \log_d N) - 3$ middle stages with each middle stage having $\frac{N}{d}$ switches, and each switch in the middle stage has $3 \times d$ incoming links connecting from
 5 the switches in its immediate preceding stage, and $3 \times d$ outgoing links connecting to the switches in its immediate succeeding stage.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1A is a diagram 100A of an exemplary symmetrical multi-link multi-stage
 10 network $V_{mlink}(N, d, s)$ having inverse Benes connection topology of five stages with $N = 8$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1B is a diagram 100B of an exemplary symmetrical multi-link multi-stage
 15 network $V_{mlink}(N, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with $N = 8$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1C is a diagram 100C of an exemplary symmetrical multi-link multi-stage
 20 network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with $N = 8$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1D is a diagram 100D of an exemplary symmetrical multi-link multi-stage
 25 network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with $N = 8$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably

nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1E is a diagram 100E of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with $N = 8$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1F is a diagram 100F of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having Baseline connection topology of five stages with $N = 8$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1G is a diagram 100G of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with $N = 8$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1H is a diagram 100H of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with $N = 8$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1I is a diagram 100I of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five stages with $N = 8$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1J is a diagram 100J of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with $N = 8$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1K is a diagram 100K of a general symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ with $(2 \times \log_d N) - 1$ stages with $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

10 FIG. 1A1 is a diagram 100A1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having inverse Benes connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

15 FIG. 1B1 is a diagram 100B1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

20 FIG. 1C1 is a diagram 100C1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

25 FIG. 1D1 is a diagram 100D1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking network

for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1E1 is a diagram 100E1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1F1 is a diagram 100F1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having Baseline connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1G1 is a diagram 100G1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1H1 is a diagram 100H1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1I1 is a diagram 100I1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 2$,

strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1J1 is a diagram 100J1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with
 5 $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1K1 is a diagram 100K1 of a general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2 \times \log_d N) - 1$ stages with $N_1 = p * N_2$ and $s = 2$,
 10 strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1A2 is a diagram 100A2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having inverse Benes connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking
 15 network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1B2 is a diagram 100B2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking
 20 network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1C2 is a diagram 100C2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking
 25 network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1D2 is a diagram 100D2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out
5 multicast connections, in accordance with the invention.

FIG. 1E2 is a diagram 100E2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking network for unicast connections
10 and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1F2 is a diagram 100F2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having Baseline connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out
15 multicast connections, in accordance with the invention.

FIG. 1G2 is a diagram 100G2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking
20 network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1H2 is a diagram 100H2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking network
25 for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1I2 is a diagram 100I2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1J2 is a diagram 100J2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1K2 is a diagram 100K2 of a general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2 \times \log_d N) - 1$ stages with $N_2 = p * N_1$ and $s = 2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2A is a diagram 200A of an exemplary symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N, d, s)$ having inverse Benes connection topology of five stages with $N = 8$, $d = 2$ and $s = 2$ with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2B is a diagram 200B of a general symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N, d, 2)$ with $(2 \times \log_d N) - 1$ stages strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections in accordance with the invention.

FIG. 2C is a diagram 200C of an exemplary asymmetrical folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, 2)$ having inverse Benes connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, and $d = 2$ with exemplary multicast

connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2D is a diagram 200D of a general asymmetrical folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, 2)$ with $N_2 = p * N_1$ and with $(2 \times \log_d N) - 1$ stages strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections in accordance with the invention.

FIG. 2E is a diagram 200E of an exemplary asymmetrical folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, 2)$ having inverse Benes connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, and $d = 2$ with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2F is a diagram 200F of a general asymmetrical folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, 2)$ with $N_1 = p * N_2$ and with $(2 \times \log_d N) - 1$ stages strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections in accordance with the invention.

FIG. 3A is a diagram 300A of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having inverse Benes connection topology of five stages with $N = 8$, $d = 2$ and $s = 3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3B is a diagram 300B of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with $N = 8$, $d = 2$ and $s = 3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3C is a diagram 300C of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with $N =$

8, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3D is a diagram 300D of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with $N =$
 5 8, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3E is a diagram 300E of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with $N = 8$, $d = 2$ and $s=3$, strictly
 10 nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3F is a diagram 300F of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having Baseline connection topology of five stages with $N = 8$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in
 15 accordance with the invention.

FIG. 3G is a diagram 300G of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with $N = 8$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3H is a diagram 300H of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with $N =$
 20 8, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3I is a diagram 300I of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ (having a connection topology built using back-to-back Banyan
 25 Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly

networks) of five stages with $N = 8$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3J is a diagram 300J of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with $N =$
 5 8 , $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3K is a diagram 300K of a general symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ with $(2 \times \log_d N) - 1$ stages with $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

10 FIG. 3A1 is a diagram 300A1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having inverse Benes connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

15 FIG. 3B1 is a diagram 300B1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections.

20 FIG. 3C1 is a diagram 300C1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

25 FIG. 3D1 is a diagram 300D1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3E1 is a diagram 300E1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out
5 multicast connections, in accordance with the invention.

FIG. 3F1 is a diagram 300F1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having Baseline connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

10 FIG. 3G1 is a diagram 300G1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

15 FIG. 3H1 is a diagram 300H1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

20 FIG. 3I1 is a diagram 300I1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

25 FIG. 3J1 is a diagram 300J1 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3K1 is a diagram 300K1 of a general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2 \times \log_d N) - 1$ stages with $N_1 = p * N_2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

5 FIG. 3A2 is a diagram 300A2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having inverse Benes connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

10 FIG. 3B2 is a diagram 300B2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

15 FIG. 3C2 is a diagram 300C2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

20 FIG. 3D2 is a diagram 300D2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

25 FIG. 3E2 is a diagram 300E2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3F2 is a diagram 300F2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having Baseline connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

5 FIG. 3G2 is a diagram 300G2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

10 FIG. 3H2 is a diagram 300H2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

15 FIG. 3I2 is a diagram 300I2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

20 FIG. 3J2 is a diagram 300J2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

25 FIG. 3K2 is a diagram 300K2 of a general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2 \times \log_d N) - 1$ stages with $N_2 = p * N_1$ and $s=3$, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4A is a diagram 400A of an exemplary symmetrical folded multi-stage network $V_{fold}(N, d, s)$ having inverse Benes connection topology of five stages with $N = 8$, $d = 2$ and $s=2$ with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4A1 is a diagram 400A1 of an exemplary symmetrical folded multi-stage network $V_{fold}(N, d, 2)$ having Omega connection topology of five stages with $N = 8$, $d = 2$ and $s=2$ with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4A2 is a diagram 400A2 of an exemplary symmetrical folded multi-stage network $V_{fold}(N, d, 2)$ having nearest neighbor connection topology of five stages with $N = 8$, $d = 2$ and $s=2$ with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4B is a diagram 400B of a general symmetrical folded multi-stage network $V_{fold}(N, d, 2)$ with $(2 \times \log_d N) - 1$ stages strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections in accordance with the invention.

FIG. 4C is a diagram 400C of an exemplary asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 2)$ having inverse Benes connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, and $d = 2$ with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4C1 is a diagram 400C1 of an exemplary asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 2)$ having Omega connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, and $d = 2$ with exemplary multicast connections, strictly

nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4C2 is a diagram 400C2 of an exemplary asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 2)$ having nearest neighbor connection topology of five stages with $N_1 = 8$, $N_2 = p^* N_1 = 24$ where $p = 3$, and $d = 2$ with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4D is a diagram 400D of a general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 2)$ with $N_2 = p^* N_1$ and with $(2 \times \log_d N) - 1$ stages strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections in accordance with the invention.

FIG. 4E is a diagram 400E of an exemplary asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 2)$ having inverse Benes connection topology of five stages with $N_2 = 8$, $N_1 = p^* N_2 = 24$, where $p = 3$, and $d = 2$ with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4E1 is a diagram 400E1 of an exemplary asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 2)$ having Omega connection topology of five stages with $N_2 = 8$, $N_1 = p^* N_2 = 24$, where $p = 3$, and $d = 2$ with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4E2 is a diagram 400E2 of an exemplary asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 2)$ having nearest neighbor connection topology of five stages with $N_2 = 8$, $N_1 = p^* N_2 = 24$, where $p = 3$, and $d = 2$ with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably

nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4F is a diagram 400F of a general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 2)$ with $N_1 = p * N_2$ and with $(2 \times \log_d N) - 1$ stages strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections in accordance with the invention.

FIG. 5A is a diagram 500A of an exemplary symmetrical folded multi-stage network $V_{fold}(N, d, s)$ having inverse Benes connection topology of five stages with $N = 8$, $d = 2$ and $s = 1$ with exemplary unicast connections rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. 5B is a diagram 500B of a general symmetrical folded multi-stage network $V_{fold}(N, d, 1)$ with $(2 \times \log_d N) - 1$ stages rearrangeably nonblocking network for unicast connections in accordance with the invention.

FIG. 5C is a diagram 500C of an exemplary asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 1)$ having inverse Benes connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, and $d = 2$ with exemplary unicast connections rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. 5D is a diagram 500D of a general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 1)$ with $N_2 = p * N_1$ and with $(2 \times \log_d N) - 1$ stages rearrangeably nonblocking network for unicast connections in accordance with the invention.

FIG. 5E is a diagram 500E of an exemplary asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 1)$ having inverse Benes connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, and $d = 2$ with exemplary unicast connections rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. 5F is a diagram 500F of a general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 1)$ with $N_1 = p * N_2$ and with $(2 \times \log_d N) - 1$ stages rearrangeably nonblocking network for unicast connections in accordance with the invention.

5 FIG. 6A is a diagram 600A of an exemplary symmetrical multi-stage network $V(N, d, s)$ having inverse Benes connection topology of five stages with $N = 8$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

10 FIG. 6B is a diagram 600B of an exemplary symmetrical multi-stage network $V(N, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with $N = 8$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections.

15 FIG. 6C is a diagram 600C of an exemplary symmetrical multi-stage network $V(N, d, s)$ having an exemplary connection topology of five stages with $N = 8$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. 6D is a diagram 600D of an exemplary symmetrical multi-stage network $V(N, d, s)$ having an exemplary connection topology of five stages with $N = 8$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

20 FIG. 6E is a diagram 600E of an exemplary symmetrical multi-stage network $V(N, d, s)$ (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with $N = 8$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections.

25 FIG. 6F is a diagram 600F of an exemplary symmetrical multi-stage network $V(N, d, s)$ having Baseline connection topology of five stages with $N = 8$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections.

FIG. 6G is a diagram 600G of an exemplary symmetrical multi-stage network $V(N, d, s)$ having an exemplary connection topology of five stages with $N = 8$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

5 FIG. 6H is a diagram 600H of an exemplary symmetrical multi-stage network $V(N, d, s)$ having an exemplary connection topology of five stages with $N = 8$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

10 FIG. 6I is a diagram 600I of an exemplary symmetrical multi-stage network $V(N, d, s)$ (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five stages with $N = 8$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections.

15 FIG. 6J is a diagram 600J of an exemplary symmetrical multi-stage network $V(N, d, s)$ having an exemplary connection topology of five stages with $N = 8$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections.

FIG. 6K is a diagram 600K of a general symmetrical multi-stage network $V(N, d, s)$ with $(2 \times \log_d N) - 1$ stages with $s = 1$, rearrangeably nonblocking network for unicast connections in accordance with the invention.

20 FIG. 6A1 is a diagram 600A1 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having inverse Benes connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

25 FIG. 6B1 is a diagram 600B1 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections.

FIG. 6C1 is a diagram 600C1 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

5 FIG. 6D1 is a diagram 600D1 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

10 FIG. 6E1 is a diagram 600E1 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections.

15 FIG. 6F1 is a diagram 600F1 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having Baseline connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections.

20 FIG. 6G1 is a diagram 600G1 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. 6H1 is a diagram 600H1 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

25 FIG. 6I1 is a diagram 600I1 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five

stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections.

FIG. 6J1 is a diagram 600J1 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1 = 8$, $N_2 = p * N_1 = 24$ where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections.

FIG. 6K1 is a diagram 600K1 of a general asymmetrical multi-stage network $V(N_1, N_2, d, s)$ with $(2 \times \log_d N) - 1$ stages with $N_1 = p * N_2$ and $s = 1$, rearrangeably nonblocking network for unicast connections in accordance with the invention.

10 FIG. 6A2 is a diagram 600A2 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having inverse Benes connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

15 FIG. 6B2 is a diagram 600B2 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections.

20 FIG. 6C2 is a diagram 600C2 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

25 FIG. 6D2 is a diagram 600D2 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. 6E2 is a diagram 600E2 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections.

5 FIG. 6F2 is a diagram 600F2 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having Baseline connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections.

10 FIG. 6G2 is a diagram 600G2 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

15 FIG. 6H2 is a diagram 600H2 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

20 FIG. 6I2 is a diagram 600I2 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections.

25 FIG. 6J2 is a diagram 600J2 of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2 = 8$, $N_1 = p * N_2 = 24$, where $p = 3$, $d = 2$ and $s = 1$, rearrangeably nonblocking network for unicast connections.

FIG. 6K2 is a diagram 600K2 of a general asymmetrical multi-stage network $V(N_1, N_2, d, s)$ with $(2 \times \log_d N) - 1$ stages with $N_2 = p^* N_1$ and $s = 1$, rearrangeably nonblocking network for unicast connections in accordance with the invention.

FIG. 7A is high-level flowchart of a scheduling method according to the invention, used to set up the multicast connections in all the networks disclosed in this invention.

FIG. 8A1 is a diagram 800A1 of an exemplary prior art implementation of a two by two switch; FIG. 8A2 is a diagram 800A2 for programmable integrated circuit prior art implementation of the diagram 800A1 of FIG. 8A1; FIG. 8A3 is a diagram 800A3 for one-time programmable integrated circuit prior art implementation of the diagram 800A1 of FIG. 8A1; FIG. 8A4 is a diagram 800A4 for integrated circuit placement and route implementation of the diagram 800A1 of FIG. 8A1.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is concerned with the design and operation of large scale crosspoint reduction using arbitrarily large multi-link multi-stage switching networks for broadcast, unicast and multicast connections. Particularly multi-link multi-stage networks with stages more than three and radices greater than or equal to two offer large scale crosspoint reduction when configured with optimal links as disclosed in this invention.

When a transmitting device simultaneously sends information to more than one receiving device, the one-to-many connection required between the transmitting device and the receiving devices is called a multicast connection. A set of multicast connections is referred to as a multicast assignment. When a transmitting device sends information to one receiving device, the one-to-one connection required between the transmitting device and the receiving device is called unicast connection. When a transmitting device simultaneously sends information to all the available receiving devices, the one-to-all connection required between the transmitting device and the receiving devices is called a broadcast connection.

In general, a multicast connection is meant to be one-to-many connection, which includes unicast and broadcast connections. A multicast assignment in a switching network is nonblocking if any of the available inlet links can always be connected to any of the available outlet links.

5 In certain multi-link multi-stage networks, folded multi-link multi-stage networks, and folded multi-stage networks of the type described herein, any connection request of arbitrary fan-out, i.e. from an inlet link to an outlet link or to a set of outlet links of the network, can be satisfied without blocking if necessary by rearranging some of the previous connection requests. In certain other multi-link multi-stage networks of the type
10 described herein, any connection request of arbitrary fan-out, i.e. from an inlet link to an outlet link or to a set of outlet links of the network, can be satisfied without blocking with never needing to rearrange any of the previous connection requests.

In certain multi-link multi-stage networks, folded multi-link multi-stage networks, and folded multi-stage networks of the type described herein, any connection request of
15 unicast from an inlet link to an outlet link of the network, can be satisfied without blocking if necessary by rearranging some of the previous connection requests. In certain other multi-link multi-stage networks of the type described herein, any connection request of unicast from an inlet link to an outlet link of the network, can be satisfied without blocking with never needing to rearrange any of the previous connection requests.

20 Nonblocking configurations for other types of networks with numerous connection topologies and scheduling methods are disclosed as follows:

1) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-stage networks $V(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the PCT Application
25 Serial No. PCT/US08/56064 that is incorporated by reference above.

2) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in U.S.

Provisional Patent Application Serial No. 60/940, 387 that is incorporated by reference above.

3) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in U.S. Provisional Patent Application Serial No. 60/940, 390 that is incorporated by reference above.

4) VLSI layouts of generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, and generalized hypercube networks $V_{cube}(N_1, N_2, d, s)$ for $s = 1, 2, 3$ or any number in general, are described in detail in U.S. Provisional Patent Application Serial No. 60/940, 394 that is incorporated by reference above.

5) VLSI layouts of numerous types of multi-stage networks with locality exploitation are described in U.S. Provisional Patent Application Serial No. 60/984, 724 that is incorporated by reference above.

6) VLSI layouts of numerous types of multistage pyramid networks are described in U.S. Provisional Patent Application Serial No. 61/018, 494 that is incorporated by reference above.

RNB MULTI-LINK MULTI-STAGE EMBODIMENTS:

Symmetric RNB Embodiments:

Referring to FIG. 1A, in one embodiment, an exemplary symmetrical multi-link multi-stage network 100A with five stages of twenty switches for satisfying

communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by four switches IS1-IS4 and output stage 120 consists of four, four by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, four by four switches MS(1,1) - MS(1,4), middle stage 140 consists of four, four by four switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by four switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N}{d}$, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by $\frac{N}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the notation $2d * d$. Likewise, the size of each switch in any of the middle stages can be denoted as $2d * 2d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL1-IL8), d represents the inlet links of each input switch

or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL1-IL8 as there are outlet links OL1-OL8, in a symmetrical network they are the same.

5 Each of the $\frac{N}{d}$ input switches IS1 – IS4 are connected to exactly $2 \times d$ switches in middle stage 130 through $2 \times d$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and also to middle switch MS(1,2) through the links ML(1,3) and ML(1,4)).

Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are
 10 connected from exactly d input switches through $2 \times d$ links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,7) and ML(1,8) are connected to the middle switch MS(1,1) from input switch IS2) and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected from
 15 middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,3) and ML(2,4) are connected from middle switch MS(1,1) to middle switch MS(2,3)).

Similarly each of the $\frac{N}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage
 140 are connected from exactly d switches in middle stage 130 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected to the middle switch MS(2,1) from
 20 middle switch MS(1,1), and the links ML(2,11) and ML(2,12) are connected to the middle switch MS(2,1) from middle switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,3) and ML(3,4) are connected from middle switch MS(2,1) to middle switch
 25 MS(3,3)).

Similarly each of the $\frac{N}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,11) and ML(3,12) are connected to the middle switch MS(3,1) from middle switch MS(2,3)) and also are connected to exactly d output switches in output stage 120 through $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected to output switch OS1 from Middle switch MS(3,1), and the links ML(4,3) and ML(4,4) are connected to output switch OS2 from middle switch MS(3,1)).

Each of the $\frac{N}{d}$ output switches OS1 – OS4 are connected from exactly $2 \times d$ switches in middle stage 150 through $2 \times d$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1) and ML(4,2), and output switch OS1 is also connected from middle switch MS(3,2) through the links ML(4,7) and ML(4,8)).

Finally the connection topology of the network 100A shown in FIG. 1A is known to be back to back inverse Benes connection topology.

Referring to FIG. 1B, in another embodiment of network $V_{mlink}(N, d, s)$, an exemplary symmetrical multi-link multi-stage network 100B with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by four switches IS1-IS4 and output stage 120 consists of four, four by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, four by four switches MS(1,1) - MS(1,4), middle stage 140 consists of four, four by four switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by four switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be
 5 operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output
 10 switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N}{d}$, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by $\frac{N}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the
 15 notation $2d * d$. Likewise, the size of each switch in any of the middle stages can be denoted as $2d * 2d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The symmetric multi-link multi-stage network of FIG. 1B is also the network of the type $V_{mlink}(N, d, s)$, where N represents the total number of inlet links of all input
 20 switches (for example the links IL1-IL8), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL1-IL8 as there are outlet links OL1-OL8, in a symmetrical network they are the same.

25 Each of the $\frac{N}{d}$ input switches IS1 – IS4 are connected to exactly $2 \times d$ switches in middle stage 130 through $2 \times d$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and also to middle switch MS(1,2) through the links ML(1,3) and ML(1,4)).

Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through $2 \times d$ links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,9) and ML(1,10) are connected to the middle switch MS(1,1) from
 5 input switch IS3) and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,3) and ML(2,4) are connected from middle switch MS(1,1) to middle switch MS(2,2)).

Similarly each of the $\frac{N}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage
 10 140 are connected from exactly d switches in middle stage 130 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,9) and ML(2,10) are connected to the middle switch MS(2,1) from middle switch MS(1,3)) and also are connected to exactly d
 15 switches in middle stage 150 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,3) and ML(3,4) are connected from middle switch MS(2,1) to middle switch MS(3,2)).

Similarly each of the $\frac{N}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage
 20 150 are connected from exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,9) and ML(3,10) are connected to the middle switch MS(3,1) from middle switch MS(2,3)) and also are connected to exactly d output
 25 switches in output stage 120 through $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected to output switch OS1 from Middle switch MS(3,1), and the links ML(4,3) and ML(4,4) are connected to output switch OS2 from middle switch MS(3,1)).

Each of the $\frac{N}{d}$ output switches OS1 – OS4 are connected from exactly $2 \times d$ switches in middle stage 150 through $2 \times d$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1) and ML(4,2), and output switch OS1 is also connected from middle switch MS(3,3) through the links
 5 ML(4,9) and ML(4,10)).

Finally the connection topology of the network 100B shown in FIG. 1B is known to be back to back Omega connection topology.

Referring to FIG. 1C, in another embodiment of network $V_{mlink}(N, d, s)$, an exemplary symmetrical multi-link multi-stage network 100C with five stages of twenty
 10 switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by four switches IS1-IS4 and output stage 120 consists of four, four by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of
 15 four, four by four switches MS(1,1) - MS(1,4), middle stage 140 consists of four, four by four switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by four switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the
 20 switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle
 25 stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and

of output stage 120 can be denoted in general with the variable $\frac{N}{d}$, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by $\frac{N}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the notation $2d * d$. Likewise, the size of each switch in any of the middle stages can be denoted as $2d * 2d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The symmetric multi-link multi-stage network of FIG. 1C is also the network of the type $V_{mlink}(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL1-IL8), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL1-IL8 as there are outlet links OL1-OL8, in a symmetrical network they are the same.

Each of the $\frac{N}{d}$ input switches IS1 – IS4 are connected to exactly $2 \times d$ switches in middle stage 130 through $2 \times d$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and also to middle switch MS(1,2) through the links ML(1,3) and ML(1,4)).

Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through $2 \times d$ links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,15) and ML(1,16) are connected to the middle switch MS(1,1) from input switch IS4) and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,3) and ML(2,4) are connected from middle switch MS(1,1) to middle switch MS(2,2)).

Similarly each of the $\frac{N}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,15) and ML(2,16) are connected to the middle switch MS(2,1) from middle switch MS(1,4)) and also are connected to exactly d switches in middle stage 150 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,3) and ML(3,4) are connected from middle switch MS(2,1) to middle switch MS(3,2)).

10 Similarly each of the $\frac{N}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,15) and ML(3,16) are connected to the middle switch MS(3,1) from middle switch MS(2,4)) and also are connected to exactly d output switches in output stage 120 through $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected to output switch OS1 from middle switch MS(3,1), and the links ML(4,3) and ML(4,4) are connected to output switch OS2 from middle switch MS(3,1)).

Each of the $\frac{N}{d}$ output switches OS1 – OS4 are connected from exactly $2 \times d$ switches in middle stage 150 through $2 \times d$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1) and ML(4,2), and output switch OS1 is also connected from middle switch MS(3,4) through the links ML(4,15) and ML(4,16)).

25 Finally the connection topology of the network 100C shown in FIG. 1C is hereinafter called nearest neighbor connection topology.

Similar to network 100A of FIG. 1A, 100B of FIG. 1B, and 100C of FIG. 1C, referring to FIG. 1D, FIG. 1E, FIG. 1F, FIG. 1G, FIG. 1H, FIG. 1I and FIG. 1J with

exemplary symmetrical multi-link multi-stage networks 100D, 100E, 100F, 100G, 100H, 100I, and 100J respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by four switches IS1-IS4 and output stage 120 consists of four, four by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, four by four switches MS(1,1) - MS(1,4), middle stage 140 consists of four, four by four switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by four switches MS(3,1) - MS(3,4).

Such networks can also be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

The networks 100D, 100E, 100F, 100G, 100H, 100I and 100J of FIG. 1D, FIG. 1E, FIG. 1F, FIG. 1G, FIG. 1H, FIG. 1I, and FIG. 1J are also embodiments of symmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL1-IL8), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL1-IL8 as there are outlet links OL1-OL8, in a symmetrical network they are the same.

Just like networks of 100A, 100B and 100C, for all the networks 100D, 100E, 100F, 100G, 100H, 100I and 100J of FIG. 1D, FIG. 1E, FIG. 1F, FIG. 1G, FIG. 1H, FIG.

1I, and FIG. 1J, each of the $\frac{N}{d}$ input switches IS1 – IS4 are connected to exactly $2 \times d$ switches in middle stage 130 through $2 \times d$ links.

Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through $2 \times d$ links and also are connected to
 5 exactly d switches in middle stage 140 through $2 \times d$ links.

Similarly each of the $\frac{N}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through $2 \times d$ links and also are connected to exactly d switches in middle stage 150 through $2 \times d$ links.

Similarly each of the $\frac{N}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage
 10 150 are connected from exactly d switches in middle stage 140 through $2 \times d$ links and also are connected to exactly d output switches in output stage 120 through $2 \times d$ links.

Each of the $\frac{N}{d}$ output switches OS1 – OS4 are connected from exactly $2 \times d$ switches in middle stage 150 through $2 \times d$ links.

In all the ten embodiments of FIG. 1A to FIG. 1J the connection topology is
 15 different. That is the way the links ML(1,1) - ML(1,16), ML(2,1) - ML(2,16), ML(3,1) - ML(3,16), and ML(4,1) - ML(4,16) are connected between the respective stages is different. Even though only ten embodiments are illustrated, in general, the network $V_{mlink}(N, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{mlink}(N, d, s)$ may be back to back Benes networks,
 20 Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{mlink}(N, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{mlink}(N, d, s)$ can be built. The

ten embodiments of FIG. 1A to FIG. 1J are only three examples of network

$$V_{mlink}(N, d, s).$$

In all the ten embodiments of FIG. 1A to FIG. 1J, each of the links ML(1,1) – ML(1,16), ML(2,1) – ML(2,16), ML(3,1) – ML(3,16) and ML(4,1) – ML(4,16) are
 5 either available for use by a new connection or not available if currently used by an existing connection. The input switches IS1-IS4 are also referred to as the network input ports. The input stage 110 is often referred to as the first stage. The output switches OS1-OS4 are also referred to as the network output ports. The output stage 120 is often referred to as the last stage. The middle stage switches MS(1,1) – MS(1,4), MS(2,1) –
 10 MS(2,4), and MS(3,1) – MS(3,4) are referred to as middle switches or middle ports.

In the example illustrated in FIG. 1A (or in FIG1B to FIG. 1J), a fan-out of four is possible to satisfy a multicast connection request if input switch is IS2, but only two switches in middle stage 130 will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS1, again only a fan-out
 15 of two is used. The specific middle switches that are chosen in middle stage 130 when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network 100A (or 100B to 100J), to be operated in rearrangeably nonblocking manner in accordance with the
 20 invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage 130 is used to satisfy the request. Moreover,
 25 although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage 130, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the rearrangeably nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and
 30 the output stage switches to satisfy the connection request.

Generalized Symmetric RNB Embodiments:

Network 100K of FIG. 1K is an example of general symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ with $(2 \times \log_d N) - 1$ stages. The general symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s \geq 2$ according to the current invention. Also the general symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ can be operated in strictly nonblocking manner for unicast if $s \geq 2$ according to the current invention. (And in the example of FIG. 1K, $s = 2$). The general symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ with $(2 \times \log_d N) - 1$ stages has d inlet links for each of $\frac{N}{d}$ input switches IS1-IS(N/d) (for example the links IL1-IL(d) to the input switch IS1) and $2 \times d$ outgoing links for each of $\frac{N}{d}$ input switches IS1-IS(N/d) (for example the links ML(1,1) - ML(1,2d) to the input switch IS1). There are d outlet links for each of $\frac{N}{d}$ output switches OS1-OS(N/d) (for example the links OL1-OL(d) to the output switch OS1) and $2 \times d$ incoming links for each of $\frac{N}{d}$ output switches OS1-OS(N/d) (for example ML(2x Log_d N - 2,1) - ML(2x Log_d N - 2, 2x d) to the output switch OS1).

Each of the $\frac{N}{d}$ input switches IS1 - IS(N/d) are connected to exactly d switches in middle stage 130 through $2 \times d$ links.

Each of the $\frac{N}{d}$ middle switches MS(1,1) - MS(1,N/d) in the middle stage 130 are connected from exactly d input switches through $2 \times d$ links and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links.

Similarly each of the $\frac{N}{d}$ middle switches MS(Log_d N - 1,1) - MS(Log_d N - 1, $\frac{N}{d}$) in the middle stage 130 + 10 * (Log_d N - 2) are connected from exactly d switches in

middle stage $130 + 10 * (\text{Log}_d N - 3)$ through $2 \times d$ links and also are connected to exactly d switches in middle stage $130 + 10 * (\text{Log}_d N - 1)$ through $2 \times d$ links.

Similarly each of the $\frac{N}{d}$ middle switches $MS(2 \times \text{Log}_d N - 3, 1) -$

$MS(2 \times \text{Log}_d N - 3, \frac{N}{d})$ in the middle stage $130 + 10 * (2 * \text{Log}_d N - 4)$ are connected from
 5 exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N - 5)$ through $2 \times d$ links and also are connected to exactly d output switches in output stage 120 through $2 \times d$ links.

Each of the $\frac{N}{d}$ output switches OS1 – OS(N/d) are connected from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N - 4)$ through $2 \times d$ links.

As described before, again the connection topology of a general $V_{mlink}(N, d, s)$
 10 may be any one of the connection topologies. For example the connection topology of the network $V_{mlink}(N, d, s)$ may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection
 15 topology of the general $V_{mlink}(N, d, s)$ network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network $V_{mlink}(N, d, s)$ can be built. The embodiments of FIG. 1A to FIG. 1J are ten examples of network $V_{mlink}(N, d, s)$.

The general symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ can be
 20 operated in rearrangeably nonblocking manner for multicast when $s \geq 2$ according to the current invention. Also the general symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ can be operated in strictly nonblocking manner for unicast if $s \geq 2$ according to the current invention.

Every switch in the multi-link multi-stage networks discussed herein has multicast capability. In a $V_{mlink}(N, d, s)$ network, if a network inlet link is to be connected to more

than one outlet link on the same output switch, then it is only necessary for the corresponding input switch to have one path to that output switch. This follows because that path can be multicast within the output switch to as many outlet links as necessary. Multicast assignments can therefore be described in terms of connections between input switches and output switches. An existing connection or a new connection from an input switch to r' output switches is said to have fan-out r' . If all multicast assignments of a first type, wherein any inlet link of an input switch is to be connected in an output switch to at most one outlet link are realizable, then multicast assignments of a second type, wherein any inlet link of each input switch is to be connected to more than one outlet link in the same output switch, can also be realized. For this reason, the following discussion is limited to general multicast connections of the first type (with fan-out r' , $1 \leq r' \leq \frac{N}{d}$) although the same discussion is applicable to the second type.

To characterize a multicast assignment, for each inlet link $i \in \left\{1, 2, \dots, \frac{N}{d}\right\}$, let $I_i = O$, where $O \subset \left\{1, 2, \dots, \frac{N}{d}\right\}$, denote the subset of output switches to which inlet link i is to be connected in the multicast assignment. For example, the network of Fig. 1C shows an exemplary five-stage network, namely $V_{mlink}(8, 2, 2)$, with the following multicast assignment $I_1 = \{2, 4\}$ and all other $I_j = \phi$ for $j = [2-8]$. It should be noted that the connection I_1 fans out in the first stage switch IS1 into middle switches MS(1,1) and MS(1,2) in middle stage 130, and fans out in middle switches MS(1,1) and MS(1,2) only once into middle switches MS(2,1) and MS(2,3) respectively in middle stage 140.

The connection I_1 also fans out in middle switches MS(2,1) and MS(2,3) only once into middle switches MS(3,2) and MS(3,4) respectively in middle stage 150. The connection I_1 also fans out in middle switches MS(3,2) and MS(3,4) only once into output switches OS2 and OS4 in output stage 120. Finally the connection I_1 fans out once in the output stage switch OS2 into outlet link OL3 and in the output stage switch OS4 twice into the outlet links OL7 and OL8. In accordance with the invention, each

connection can fan out in the input stage switch into at most two middle stage switches in middle stage 130.

Asymmetric RNB ($N_2 > N_1$) Embodiments:

Referring to FIG. 1A1, in one embodiment, an exemplary asymmetrical multi-link
 5 multi-stage network 100A1 with five stages of twenty switches for satisfying
 communication requests, such as setting up a telephone call or a data call, or a connection
 between configurable logic blocks, between an input stage 110 and output stage 120 via
 middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by
 four switches IS1-IS4 and output stage 120 consists of four, eight by six switches OS1-
 10 OS4. And all the middle stages namely middle stage 130 consists of four, four by four
 switches MS(1,1) - MS(1,4), middle stage 140 consists of four, four by four switches
 MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by eight switches MS(3,1)
 - MS(3,4).

Such a network can be operated in strictly non-blocking manner for unicast
 15 connections, because the switches in the input stage 110 are of size two by four, the
 switches in output stage 120 are of size four by two, and there are four switches in each
 of middle stage 130, middle stage 140 and middle stage 150. Such a network can be
 operated in rearrangeably non-blocking manner for multicast connections, because the
 switches in the input stage 110 are of size two by four, the switches in output stage 120
 20 are of size eight by six, and there are four switches in each of middle stage 130, middle
 stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output
 switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and
 of output stage 120 can be denoted in general with the variable $\frac{N_1}{d}$, where N_1 is the total
 25 number of inlet links or and N_2 is the total number of outlet links and $N_2 > N_1$ and
 $N_2 = p * N_1$ where $p > 1$. The number of middle switches in each middle stage is
 denoted by $\frac{N_1}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the

notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the notation $(d + d_2) * d_2$, where $d_2 = N_2 \times \frac{d}{N_1} = p \times d$. The size of each switch in any of the middle stages excepting the last middle stage can be denoted as $2d * 2d$. The size of each switch in the last middle stage can be denoted as $2d * (d + d_2)$. A switch as used

5 herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example the links

10 OL1-OL24), d represents the inlet links of each input switch where $N_2 > N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the $\frac{N_1}{d}$ input switches IS1 – IS4 are connected to exactly d switches in middle stage 130 through $2 \times d$ links (for example input switch IS1 is connected to

15 middle switch MS(1,1) through the links ML(1,1), ML(1,2), and also to middle switch MS(1,2) through the links ML(1,3) and ML(1,4)).

Each of the $\frac{N_1}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through $2 \times d$ links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1,

20 and the links ML(1,7) and ML(1,8) are connected to the middle switch MS(1,1) from input switch IS2) and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,3) and ML(2,4) are connected from middle switch MS(1,1) to middle switch MS(2,3)).

Similarly each of the $\frac{N_1}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,11) and ML(2,12) are connected to the middle switch MS(2,1) from middle switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,3) and ML(3,4) are connected from middle switch MS(2,1) to middle switch MS(3,3)).

10 Similarly each of the $\frac{N_1}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,11) and ML(3,12) are connected to the middle switch MS(3,1) from middle switch MS(2,3)) and also are connected to exactly $\frac{d + d_2}{2}$ output switches in output stage 120 through $d + d_2$ links (for example the links ML(4,1) and ML(4,2) are connected to output switch OS1 from Middle switch MS(3,1); the links ML(4,3) and ML(4,4) are connected to output switch OS2 from middle switch MS(3,1); the links ML(4,5) and ML(4,6) are connected to output switch OS3 from Middle switch MS(3,1); and the links ML(4,7) and ML(4,8) are connected to output switch OS4 from middle switch MS(3,1)).

Each of the $\frac{N_1}{d}$ output switches OS1 – OS4 are connected from exactly $\frac{d + d_2}{2}$ switches in middle stage 150 through $d + d_2$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1) and ML(4,2); output switch OS1 is also connected from middle switch MS(3,2) through the links ML(4,9) and ML(4,10); output switch OS1 is connected from middle switch MS(3,3) through the links ML(4,17) and ML(4,18); and output switch OS1 is also connected from middle switch MS(3,4) through the links ML(4,25) and ML(4,26)).

Finally the connection topology of the network 100A1 shown in FIG. 1A1 is known to be back to back inverse Benes connection topology.

Referring to FIG. 1B1, in one embodiment, an exemplary asymmetrical multi-link multi-stage network 100B1 with five stages of twenty switches for satisfying
 5 communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by four switches IS1-IS4 and output stage 120 consists of four, eight by six switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, four by four
 10 switches MS(1,1) - MS(1,4), middle stage 140 consists of four, four by four switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by eight switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the
 15 switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size eight by six, and there are four switches in each of middle stage 130, middle
 20 stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_1}{d}$, where N_1 is the total
 number of inlet links or and N_2 is the total number of outlet links and $N_2 > N_1$ and
 25 $N_2 = p * N_1$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_1}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the

notation $(d + d_2) * d_2$, where $d_2 = N_2 \times \frac{d}{N_1} = p \times d$. The size of each switch in any of the middle stages excepting the last middle stage can be denoted as $2d * 2d$. The size of each switch in the last middle stage can be denoted as $2d * (d + d_2)$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may

5 be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL24), d represents the inlet links of each input switch where $N_2 > N_1$, and s is

10 the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the $\frac{N_1}{d}$ input switches IS1 – IS4 are connected to exactly $2 \times d$ switches in middle stage 130 through $2 \times d$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and also to middle switch

15 MS(1,2) through the links ML(1,3) and ML(1,4)).

Each of the $\frac{N_1}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through $2 \times d$ links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,9) and ML(1,10) are connected to the middle switch MS(1,1) from

20 input switch IS3) and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,3) and ML(2,4) are connected from middle switch MS(1,1) to middle switch MS(2,2)).

Similarly each of the $\frac{N_1}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage

25 140 are connected from exactly d switches in middle stage 130 through $2 \times d$ links (for

example the links ML(2,1) and ML(2,2) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,9) and ML(2,10) are connected to the middle switch MS(2,1) from middle switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,3) and ML(3,4) are connected from middle switch MS(2,1) to middle switch MS(3,2)).

Similarly each of the $\frac{N_1}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,9) and ML(3,10) are connected to the middle switch MS(3,1) from middle switch MS(2,3)) and also are connected to exactly $\frac{d + d_2}{2}$ output switches in output stage 120 through $d + d_2$ links (for example the links ML(4,1) and ML(4,2) are connected to output switch OS1 from middle switch MS(3,1); the links ML(4,3) and ML(4,4) are connected to output switch OS2 from middle switch MS(3,1); the links ML(4,5) and ML(4,6) are connected to output switch OS3 from Middle switch MS(3,1); and the links ML(4,7) and ML(4,8) are connected to output switch OS4 from middle switch MS(3,1)).

Each of the $\frac{N_1}{d}$ output switches OS1 – OS4 are connected from exactly $\frac{d + d_2}{2}$ switches in middle stage 150 through $d + d_2$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1) and ML(4,2); output switch OS1 is also connected from middle switch MS(3,2) through the links ML(4,9) and ML(4,10); output switch OS1 is connected from middle switch MS(3,3) through the links ML(4,17) and ML(4,18); and output switch OS1 is also connected from middle switch MS(3,4) through the links ML(4,25) and ML(4,26)).

Finally the connection topology of the network 100B1 shown in FIG. 1B1 is known to be back to back Omega connection topology.

Referring to FIG. 1C1, in one embodiment, an exemplary asymmetrical multi-link multi-stage network 100C1 with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by four switches IS1-IS4 and output stage 120 consists of four, eight by six switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, four by four switches MS(1,1) - MS(1,4), middle stage 140 consists of four, four by four switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by eight switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size eight by six, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_1}{d}$, where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_2 > N_1$ and $N_2 = p * N_1$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_1}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the notation $(d + d_2) * d_2$, where $d_2 = N_2 \times \frac{d}{N_1} = p \times d$. The size of each switch in any of the middle stages excepting the last middle stage can be denoted as $2d * 2d$. The size of

each switch in the last middle stage can be denoted as $2d * (d + d_2)$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents

5 the total number of inlet links of all input switches (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL24), d represents the inlet links of each input switch where $N_2 > N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

10 Each of the $\frac{N_1}{d}$ input switches IS1 – IS4 are connected to exactly $2 \times d$ switches in middle stage 130 through $2 \times d$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and also to middle switch MS(1,2) through the links ML(1,3) and ML(1,4)).

Each of the $\frac{N_1}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are

15 connected from exactly d input switches through $2 \times d$ links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,15) and ML(1,16) are connected to the middle switch MS(1,1) from input switch IS4) and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected from

20 middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,3) and ML(2,4) are connected from middle switch MS(1,1) to middle switch MS(2,2)).

Similarly each of the $\frac{N_1}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage

140 are connected from exactly d switches in middle stage 130 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected to the middle switch MS(2,1) from

25 middle switch MS(1,1), and the links ML(2,15) and ML(2,16) are connected to the middle switch MS(2,1) from middle switch MS(1,4)) and also are connected to exactly d

switches in middle stage 150 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,3) and ML(3,4) are connected from middle switch MS(2,1) to middle switch MS(3,2)).

- 5 Similarly each of the $\frac{N_1}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,15) and ML(3,16) are connected to the middle switch MS(3,1) from middle switch MS(2,4)) and also are connected to exactly
- 10 $\frac{d + d_2}{2}$ output switches in output stage 120 through $d + d_2$ links (for example the links ML(4,1) and ML(4,2) are connected to output switch OS1 from middle switch MS(3,1); the links ML(4,3) and ML(4,4) are connected to output switch OS2 from middle switch MS(3,1); the links ML(4,5) and ML(4,6) are connected to output switch OS3 from Middle switch MS(3,1); and the links ML(4,7) and ML(4,8) are connected to output
- 15 switch OS4 from middle switch MS(3,1)).

- Each of the $\frac{N_1}{d}$ output switches OS1 – OS4 are connected from exactly $\frac{d + d_2}{2}$ switches in middle stage 150 through $d + d_2$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1) and ML(4,2); output switch OS1 is also connected from middle switch MS(3,2) through the links ML(4,9) and
- 20 ML(4,10); output switch OS1 is connected from middle switch MS(3,3) through the links ML(4,17) and ML(4,18); and output switch OS1 is also connected from middle switch MS(3,4) through the links ML(4,25) and ML(4,26)).

Finally the connection topology of the network 100C1 shown in FIG. 1C1 is hereinafter called nearest neighbor connection topology.

- 25 Similar to network 100A1 of FIG. 1A1, 100B1 of FIG. 1B1, and 100C1 of FIG. 1C1, referring to FIG. 1D1, FIG. 1E1, FIG. 1F1, FIG. 1G1, FIG. 1H1, FIG. 1I1 and FIG.

1J1 with exemplary asymmetrical multi-link multi-stage networks 100D1, 100E1, 100F1, 100G1, 100H1, 100I1, and 100J1 respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by four switches IS1-IS4 and output stage 120 consists of four, four by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, four by four switches MS(1,1) - MS(1,4), middle stage 140 consists of four, four by four switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by four switches MS(3,1) - MS(3,4).

Such networks can also be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

The networks 100D1, 100E1, 100F1, 100G1, 100H1, 100I1 and 100J1 of FIG. 1D1, FIG. 1E1, FIG. 1F1, FIG. 1G1, FIG. 1H1, FIG. 1I1, and FIG. 1J1 are also embodiments of asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL24), d represents the inlet links of each input switch where $N_2 > N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Just like networks of 100A1, 100B1 and 100C1, for all the networks 100D1, 100E1, 100F1, 100G1, 100H1, 100I1 and 100J1 of FIG. 1D1, FIG. 1E1, FIG. 1F1, FIG.

1G1, FIG. 1H1, FIG. 1I1, and FIG. 1J1, each of the $\frac{N_1}{d}$ input switches IS1 – IS4 are connected to exactly d switches in middle stage 130 through $2 \times d$ links.

Each of the $\frac{N_1}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through $2 \times d$ links and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links.

Similarly each of the $\frac{N_1}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through $2 \times d$ links and also are connected to exactly d switches in middle stage 150 through $2 \times d$ links.

Similarly each of the $\frac{N_1}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $2 \times d$ links and also are connected to exactly $\frac{d + d_2}{2}$ output switches in output stage 120 through $d + d_2$ links.

Each of the $\frac{N_1}{d}$ output switches OS1 – OS4 are connected from exactly $\frac{d + d_2}{2}$ switches in middle stage 150 through $d + d_2$ links.

In all the ten embodiments of FIG. 1A1 to FIG. 1J1 the connection topology is different. That is the way the links ML(1,1) - ML(1,16), ML(2,1) - ML(2,16), ML(3,1) - ML(3,16), and ML(4,1) - ML(4,16) are connected between the respective stages is different. Even though only ten embodiments are illustrated, in general, the network $V_{mlink}(N_1, N_2, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{mlink}(N_1, N_2, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{mlink}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link all the output links should be

reachable. Based on this property numerous embodiments of the network

$V_{mlink}(N_1, N_2, d, s)$ can be built. The ten embodiments of FIG. 1A1 to FIG. 1J1 are only three examples of network $V_{mlink}(N_1, N_2, d, s)$.

In all the ten embodiments of FIG. 1A1 to FIG. 1J1, each of the links ML(1,1) –
 5 ML(1,16), ML(2,1) – ML(2,16), ML(3,1) – ML(3,16) and ML(4,1) – ML(4,16) are
 either available for use by a new connection or not available if currently used by an
 existing connection. The input switches IS1-IS4 are also referred to as the network input
 ports. The input stage 110 is often referred to as the first stage. The output switches
 OS1-OS4 are also referred to as the network output ports. The output stage 120 is often
 10 referred to as the last stage. The middle stage switches MS(1,1) – MS(1,4), MS(2,1) –
 MS(2,4), and MS(3,1) – MS(3,4) are referred to as middle switches or middle ports.

In the example illustrated in FIG. 1A1 (or in FIG. 1B1 to FIG. 1J1), a fan-out of
 four is possible to satisfy a multicast connection request if input switch is IS2, but only
 two switches in middle stage 130 will be used. Similarly, although a fan-out of three is
 15 possible for a multicast connection request if the input switch is IS1, again only a fan-out
 of two is used. The specific middle switches that are chosen in middle stage 130 when
 selecting a fan-out of two is irrelevant so long as at most two middle switches are selected
 to ensure that the connection request is satisfied. In essence, limiting the fan-out from
 input switch to no more than two middle switches permits the network 100A1 (or 100B1
 20 to 100J1), to be operated in rearrangeably nonblocking manner in accordance with the
 invention.

The connection request of the type described above can be unicast connection
 request, a multicast connection request or a broadcast connection request, depending on
 the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single
 25 middle stage switch in middle stage 130 is used to satisfy the request. Moreover,
 although in the above-described embodiment a limit of two has been placed on the fan-
 out into the middle stage switches in middle stage 130, the limit can be greater depending
 on the number of middle stage switches in a network (while maintaining the
 rearrangeably nonblocking nature of operation of the network for multicast connections).

However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Asymmetric RNB ($N_2 > N_1$) Embodiments:

Network 100K1 of FIG. 1K1 is an example of general asymmetrical multi-link
 5 multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2 \times \log_d N_1) - 1$ stages where $N_2 > N_1$ and
 $N_2 = p * N_1$ where $p > 1$. In network 100K1 of FIG. 1K1, $N_1 = N$ and $N_2 = p * N$. The
 general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated
 in rearrangeably nonblocking manner for multicast when $s \geq 2$ according to the current
 invention. Also the general asymmetrical multi-link multi-stage network
 10 $V_{mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if
 $s \geq 2$ according to the current invention. (And in the example of FIG. 1K1, $s = 2$). The
 general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with
 $(2 \times \log_d N_1) - 1$ stages has d inlet links for each of $\frac{N_1}{d}$ input switches IS1-IS(N_1/d) (for
 example the links IL1-IL(d) to the input switch IS1) and $2 \times d$ outgoing links for each of
 15 $\frac{N_1}{d}$ input switches IS1-IS(N_1/d) (for example the links ML(1,1) - ML(1,2d) to the input
 switch IS1). There are d_2 (where $d_2 = N_2 \times \frac{d}{N_1} = p \times d$) outlet links for each of $\frac{N_1}{d}$
 output switches OS1-OS(N_1/d) (for example the links OL1-OL($p*d$) to the output switch
 OS1) and $d + d_2$ ($= d + p \times d$) incoming links for each of $\frac{N_1}{d}$ output switches OS1-
 OS(N_1/d) (for example $ML(2 \times \log_d N_1 - 2, 1) - ML(2 \times \log_d N_1 - 2, d + d_2)$ to the output
 20 switch OS1).

Each of the $\frac{N_1}{d}$ input switches IS1 – IS(N_1/d) are connected to exactly $2 \times d$
 switches in middle stage 130 through $2 \times d$ links.

Each of the $\frac{N_1}{d}$ middle switches $MS(1,1) - MS(1,N_1/d)$ in the middle stage 130 are connected from exactly d input switches through $2 \times d$ links and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links.

Similarly each of the $\frac{N_1}{d}$ middle switches $MS(\log_d N_1 - 1, 1) -$

- 5 $MS(\log_d N_1 - 1, \frac{N_1}{d})$ in the middle stage $130 + 10 * (\log_d N_1 - 2)$ are connected from exactly d switches in middle stage $130 + 10 * (\log_d N_1 - 3)$ through $2 \times d$ links and also are connected to exactly d switches in middle stage $130 + 10 * (\log_d N_1 - 1)$ through $2 \times d$ links.

Similarly each of the $\frac{N_1}{d}$ middle switches $MS(2 * \log_d N_1 - 3, 1) -$

- 10 $MS(2 * \log_d N_1 - 3, \frac{N_1}{d})$ in the middle stage $130 + 10 * (2 * \log_d N_1 - 4)$ are connected from exactly d switches in middle stage $130 + 10 * (2 * \log_d N_1 - 5)$ through $2 \times d$ links and also are connected to exactly $\frac{d + d_2}{2}$ output switches in output stage 120 through $d + d_2$ links.

Each of the $\frac{N_1}{d}$ output switches $OS1 - OS(N_1/d)$ are connected from exactly

- 15 $\frac{d + d_2}{2}$ switches in middle stage $130 + 10 * (2 * \log_d N_1 - 4)$ through $d + d_2$ links.

- As described before, again the connection topology of a general $V_{mink}(N_1, N_2, d, s)$ may be any one of the connection topologies. For example the connection topology of the network $V_{mink}(N_1, N_2, d, s)$ may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta
20 Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general $V_{mink}(N_1, N_2, d, s)$ network is,

when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network $V_{mlink}(N_1, N_2, d, s)$ can be built. The embodiments of FIG. 1A1 to FIG. 1J1 are ten examples of network $V_{mlink}(N_1, N_2, d, s)$ for $s = 2$ and $N_2 > N_1$.

5 The general symmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s = 2$ according to the current invention. Also the general symmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if $s = 2$ according to the current invention.

10 For example, the network of Fig. 1C1 shows an exemplary five-stage network, namely $V_{mlink}(8, 24, 2, 2)$, with the following multicast assignment $I_1 = \{1, 4\}$ and all other $I_j = \phi$ for $j = [2-8]$. It should be noted that the connection I_1 fans out in the first stage switch IS1 into middle switches MS(1,1) and MS(1,2) in middle stage 130, and fans out in middle switches MS(1,1) and MS(1,2) only once into middle switches MS(2,1) and
15 MS(2,3) respectively in middle stage 140.

The connection I_1 also fans out in middle switches MS(2,1) and MS(2,3) only once into middle switches MS(3,1) and MS(3,4) respectively in middle stage 150. The connection I_1 also fans out in middle switches MS(3,1) and MS(3,4) only once into output switches OS1 and OS4 in output stage 120. Finally the connection I_1 fans out
20 once in the output stage switch OS1 into outlet link OL2 and in the output stage switch OS4 twice into the outlet links OL20 and OL23. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage 130.

Asymmetric RNB ($N_1 > N_2$) Embodiments:

25 Referring to FIG. 1A2, in one embodiment, an exemplary asymmetrical multi-link multi-stage network 100A2 with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection

between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, six by eight switches IS1-IS4 and output stage 120 consists of four, four by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, eight by four
 5 switches MS(1,1) - MS(1,4), middle stage 140 consists of four, four by four switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by four switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size six by eight, the
 10 switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size six by eight, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle
 15 stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_2}{d}$, where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1 > N_2$ and
 20 $N_1 = p * N_2$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_2}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d_1 * (d + d_1)$ and each output switch OS1-OS4 can be denoted in general with the notation $(2 * d * d)$, where $d_1 = N_1 * \frac{d}{N_2} = p * d$. The size of each switch in any of the middle stages excepting the first middle stage can be denoted as $2d * 2d$. The
 25 size of each switch in the first middle stage can be denoted as $(d + d_1) * 2d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-

stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL24), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL8), d represents the inlet links of each input switch where $N_1 > N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the $\frac{N_2}{d}$ input switches IS1 – IS4 are connected to exactly $\frac{d + d_1}{2}$ switches in middle stage 130 through $d + d_1$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2); input switch IS1 is connected to middle switch MS(1,2) through the links ML(1,3) and ML(1,4); input switch IS1 is connected to middle switch MS(1,3) through the links ML(1,5), ML(1,6); and input switch IS1 is also connected to middle switch MS(1,4) through the links ML(1,7) and ML(1,8)).

Each of the $\frac{N_2}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly $\frac{d + d_1}{2}$ input switches through $d + d_1$ links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1; the links ML(1,9) and ML(1,10) are connected to the middle switch MS(1,1) from input switch IS2; the links ML(1,17) and ML(1,18) are connected to the middle switch MS(1,1) from input switch IS3; and the links ML(1,25) and ML(1,26) are connected to the middle switch MS(1,1) from input switch IS4) and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,3) and ML(2,4) are connected from middle switch MS(1,1) to middle switch MS(2,3)).

Similarly each of the $\frac{N_2}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through $2 \times d$ links (for

example the links ML(2,1) and ML(2,2) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,11) and ML(2,12) are connected to the middle switch MS(2,1) from middle switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,3) and ML(3,4) are connected from middle switch MS(2,1) to middle switch MS(3,3)).

Similarly each of the $\frac{N_2}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,11) and ML(3,12) are connected to the middle switch MS(3,1) from middle switch MS(2,3)) and also are connected to exactly d output switches in output stage 120 through $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected to output switch OS1 from middle switch MS(3,1); and the links ML(4,3) and ML(4,4) are connected to output switch OS2 from middle switch MS(3,1)).

Each of the $\frac{N_2}{d}$ output switches OS1 – OS4 are connected from exactly d switches in middle stage 150 through $2 \times d$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1) and ML(4,2); and output switch OS1 is also connected from middle switch MS(3,2) through the links ML(4,7) and ML(4,8)).

Finally the connection topology of the network 100A2 shown in FIG. 1A2 is known to be back to back inverse Benes connection topology.

Referring to FIG. 1B2, in one embodiment, an exemplary asymmetrical multi-link multi-stage network 100B2 with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via

middle stages 130, 140, and 150 is shown where input stage 110 consists of four, six by eight switches IS1-IS4 and output stage 120 consists of four, four by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, eight by four switches MS(1,1) - MS(1,4), middle stage 140 consists of four, four by four switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by four switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size six by eight, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size six by eight, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_2}{d}$, where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1 > N_2$ and $N_1 = p * N_2$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_2}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d_1 * (d + d_1)$ and each output switch OS1-OS4 can be denoted in general with the notation $(2 \times d * d)$, where $d_1 = N_1 \times \frac{d}{N_2} = p \times d$. The size of each switch in any of the middle stages excepting the first middle stage can be denoted as $2d * 2d$. The size of each switch in the first middle stage can be denoted as $(d + d_1) * 2d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1

represents the total number of inlet links of all input switches (for example the links IL1-IL24), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL8), d represents the inlet links of each input switch where $N_1 > N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the $\frac{N_2}{d}$ input switches IS1 – IS4 are connected to exactly $\frac{d + d_1}{2}$ switches in middle stage 130 through $d + d_1$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2); input switch IS1 is connected to middle switch MS(1,2) through the links ML(1,3) and ML(1,4); input switch IS1 is connected to middle switch MS(1,3) through the links ML(1,5), ML(1,6); and input switch IS1 is also connected to middle switch MS(1,4) through the links ML(1,7) and ML(1,8)).

Each of the $\frac{N_2}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly $\frac{d + d_1}{2}$ input switches through $d + d_1$ links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1; the links ML(1,9) and ML(1,10) are connected to the middle switch MS(1,1) from input switch IS2; the links ML(1,17) and ML(1,18) are connected to the middle switch MS(1,1) from input switch IS3; and the links ML(1,25) and ML(1,26) are connected to the middle switch MS(1,1) from input switch IS4) and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,3) and ML(2,4) are connected from middle switch MS(1,1) to middle switch MS(2,2)).

Similarly each of the $\frac{N_2}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected to the middle switch MS(2,1) from

middle switch MS(1,1), and the links ML(2,9) and ML(2,10) are connected to the middle switch MS(2,1) from middle switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,3) and ML(3,4) are connected from middle switch MS(2,1) to middle switch MS(3,2)).

Similarly each of the $\frac{N_2}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,9) and ML(3,10) are connected to the middle switch MS(3,1) from middle switch MS(2,3)) and also are connected to exactly d output switches in output stage 120 through $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected to output switch OS1 from middle switch MS(3,1); and the links ML(4,3) and ML(4,4) are connected to output switch OS2 from middle switch MS(3,1)).

Each of the $\frac{N_2}{d}$ output switches OS1 – OS4 are connected from exactly d switches in middle stage 150 through $2 \times d$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1) and ML(4,2); and output switch OS1 is also connected from middle switch MS(3,3) through the links ML(4,9) and ML(4,10)).

Finally the connection topology of the network 100B2 shown in FIG. 1B2 is known to be back to back Omega connection topology.

Referring to FIG. 1C2, in one embodiment, an exemplary asymmetrical multi-link multi-stage network 100C2 with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, six by eight switches IS1-IS4 and output stage 120 consists of four, four by two switches OS1-

OS4. And all the middle stages namely middle stage 130 consists of four, eight by four switches MS(1,1) - MS(1,4), middle stage 140 consists of four, four by four switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by four switches MS(3,1) - MS(3,4).

- 5 Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size six by eight, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the
- 10 switches in the input stage 110 are of size six by eight, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

- In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and
- 15 of output stage 120 can be denoted in general with the variable $\frac{N_2}{d}$, where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1 > N_2$ and $N_1 = p * N_2$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_2}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d_1 * (d + d_1)$ and each output switch OS1-OS4 can be denoted in general
- 20 with the notation $(2 \times d * d)$, where $d_1 = N_1 \times \frac{d}{N_2} = p \times d$. The size of each switch in any of the middle stages excepting the first middle stage can be denoted as $2d * 2d$. The size of each switch in the first middle stage can be denoted as $(d + d_1) * 2d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-
- 25 stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL24), N_2 represents the total number of outlet links of all output switches (for example

the links OL1-OL8), d represents the inlet links of each input switch where $N_1 > N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the $\frac{N_2}{d}$ input switches IS1 – IS4 are connected to exactly $\frac{d + d_1}{2}$

5 switches in middle stage 130 through $d + d_1$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2); input switch IS1 is connected to middle switch MS(1,2) through the links ML(1,3) and ML(1,4); input switch IS1 is connected to middle switch MS(1,3) through the links ML(1,5), ML(1,6); and input switch IS1 is also connected to middle switch MS(1,4) through the links
10 ML(1,7) and ML(1,8)).

Each of the $\frac{N_2}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are

connected from exactly $\frac{d + d_1}{2}$ input switches through $d + d_1$ links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1; the links ML(1,9) and ML(1,10) are connected to the middle switch MS(1,1)
15 from input switch IS2; the links ML(1,17) and ML(1,18) are connected to the middle switch MS(1,1) from input switch IS3; and the links ML(1,25) and ML(1,26) are connected to the middle switch MS(1,1) from input switch IS4) and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch
20 MS(2,1), and the links ML(2,3) and ML(2,4) are connected from middle switch MS(1,1) to middle switch MS(2,2)).

Similarly each of the $\frac{N_2}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage

140 are connected from exactly d switches in middle stage 130 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected to the middle switch MS(2,1) from
25 middle switch MS(1,1), and the links ML(2,15) and ML(2,16) are connected to the middle switch MS(2,1) from middle switch MS(1,4)) and also are connected to exactly d

switches in middle stage 150 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,3) and ML(3,4) are connected from middle switch MS(2,1) to middle switch MS(3,2)).

5 Similarly each of the $\frac{N_2}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,15) and ML(3,16) are connected to the middle switch MS(3,1) from middle switch MS(2,4)) and also are connected to exactly d
 10 output switches in output stage 120 through $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected to output switch OS1 from middle switch MS(3,1); and the links ML(4,3) and ML(4,4) are connected to output switch OS2 from middle switch MS(3,1)).

Each of the $\frac{N_2}{d}$ output switches OS1 – OS4 are connected from exactly d
 15 switches in middle stage 150 through $2 \times d$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1) and ML(4,2); and output switch OS1 is also connected from middle switch MS(3,4) through the links ML(4,15) and ML(4,16)).

20 Finally the connection topology of the network 100C2 shown in FIG. 1C2 is hereinafter called nearest neighbor connection topology.

Similar to network 100A2 of FIG. 1A2, 100B2 of FIG. 1B2, and 100C2 of FIG. 1C2, referring to FIG. 1D2, FIG. 1E2, FIG. 1F2, FIG. 1G2, FIG. 1H2, FIG. 1I2 and FIG. 1J2 with exemplary asymmetrical multi-link multi-stage networks 100D2, 100E2, 100F2, 100G2, 100H2, 100I2, and 100J2 respectively with five stages of twenty switches for
 25 satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of

four, six by eight switches IS1-IS4 and output stage 120 consists of four, four by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, eight by four switches MS(1,1) - MS(1,4), middle stage 140 consists of four, four by four switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by four switches
 5 MS(3,1) - MS(3,4).

Such networks can also be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be
 10 operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size six by eight, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

The networks 100D2, 100E2, 100F2, 100G2, 100H2, 100I2 and 100J2 of
 15 FIG. 1D2, FIG. 1E2, FIG. 1F2, FIG. 1G2, FIG. 1H2, FIG. 1I2, and FIG. 1J2 are also embodiments of asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL24), d represents the inlet
 20 links of each input switch where $N_1 > N_2$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Just like networks of 100A2, 100B2 and 100C2, for all the networks 100D2, 100E2, 100F2, 100G2, 100H2, 100I2 and 100J2 of FIG. 1D2, FIG. 1E2, FIG. 1F2, FIG. 1G2, FIG. 1H2, FIG. 1I2, and FIG. 1J2, each of the $\frac{N_2}{d}$ input switches IS1 – IS4 are
 25 connected to exactly $\frac{d + d_2}{2}$ switches in middle stage 130 through $d + d_2$ links.

Each of the $\frac{N_2}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly $\frac{d+d_2}{2}$ input switches through $d+d_2$ links and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links.

5 Similarly each of the $\frac{N_2}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through $2 \times d$ links and also are connected to exactly d switches in middle stage 150 through $2 \times d$ links.

Similarly each of the $\frac{N_2}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $2 \times d$ links and also are connected to exactly d output switches in output stage 120 through $2 \times d$ links.

10 Each of the $\frac{N_2}{d}$ output switches OS1 – OS4 are connected from exactly d switches in middle stage 150 through $2 \times d$ links.

In all the ten embodiments of FIG. 1A2 to FIG. 1J2 the connection topology is different. That is the way the links ML(1,1) - ML(1,16), ML(2,1) - ML(2,16), ML(3,1) - ML(3,16), and ML(4,1) - ML(4,16) are connected between the respective stages is
 15 different. Even though only ten embodiments are illustrated, in general, the network $V_{mlink}(N_1, N_2, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{mlink}(N_1, N_2, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{mlink}(N_1, N_2, d, s)$ network
 20 is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{mlink}(N_1, N_2, d, s)$ can be built. The ten embodiments of FIG. 1A2 to FIG. 1J2 are only three examples of network $V_{mlink}(N_1, N_2, d, s)$.

In all the ten embodiments of FIG. 1A2 to FIG. 1J2, each of the links ML(1,1) – ML(1,16), ML(2,1) – ML(2,16), ML(3,1) – ML(3,16) and ML(4,1) – ML(4,16) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS1-IS4 are also referred to as the network input
5 ports. The input stage 110 is often referred to as the first stage. The output switches OS1-OS4 are also referred to as the network output ports. The output stage 120 is often referred to as the last stage. The middle stage switches MS(1,1) – MS(1,4), MS(2,1) – MS(2,4), and MS(3,1) – MS(3,4) are referred to as middle switches or middle ports.

In the example illustrated in FIG. 1A2 (or in FIG. 1B2 to FIG. 1J2), a fan-out of
10 four is possible to satisfy a multicast connection request if input switch is IS2, but only two switches in middle stage 130 will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS1, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage 130 when
15 selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network 100A2 (or 100B2 to 100J2), to be operated in rearrangeably nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection
20 request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage 130 is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage 130, the limit can be greater depending
25 on the number of middle stage switches in a network (while maintaining the rearrangeably nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Asymmetric RNB ($N_2 > N_1$) Embodiments:

Network 1001K2 of FIG. 1K2 is an example of general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2 \times \log_d N_2) - 1$ stages where $N_1 > N_2$ and $N_1 = p * N_2$ where $p > 1$. In network 100K2 of FIG. 1K2, $N_2 = N$ and $N_1 = p * N$. The

5 general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s \geq 2$ according to the current invention. Also the general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if $s \geq 2$ according to the current invention. (And in the example of FIG. 1K2, $s = 2$). The

10 general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2 \times \log_d N_2) - 1$ stages has d_1 (where $d_1 = N_1 \times \frac{d}{N_2} = p \times d$ inlet links for each of $\frac{N_2}{d}$ input switches IS1-IS(N_2/d) (for example the links IL1-IL($p*d$) to the input switch IS1) and $d + d_1 (= d + p \times d)$ outgoing links for each of $\frac{N_2}{d}$ input switches IS1-IS(N_2/d) (for example the links ML(1,1) - ML(1,($d+p*d$)) to the input switch IS1). There are d outlet

15 links for each of $\frac{N_2}{d}$ output switches OS1-OS(N_2/d) (for example the links OL1-OL(d) to the output switch OS1) and $2 \times d$ incoming links for each of $\frac{N_2}{d}$ output switches OS1-OS(N_2/d) (for example $ML(2 \times \log_d N_2 - 2, 1) - ML(2 \times \log_d N_2 - 2, 2 \times d)$ to the output switch OS1).

Each of the $\frac{N_2}{d}$ input switches IS1 - IS(N_2/d) are connected to exactly $\frac{d + d_1}{2}$

20 switches in middle stage 130 through $d + d_1$ links.

Each of the $\frac{N_2}{d}$ middle switches MS(1,1) - MS(1, N_2/d) in the middle stage 130 are connected from exactly d input switches through $2 \times d$ links and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links.

Similarly each of the $\frac{N_2}{d}$ middle switches $MS(\text{Log}_d N_2 - 1, 1)$ -
 $MS(\text{Log}_d N_2 - 1, \frac{N_2}{d})$ in the middle stage $130 + 10 * (\text{Log}_d N_2 - 2)$ are connected from
 exactly d switches in middle stage $130 + 10 * (\text{Log}_d N_2 - 3)$ through $2 \times d$ links and also
 are connected to exactly d switches in middle stage $130 + 10 * (\text{Log}_d N_2 - 1)$ through
 5 $2 \times d$ links.

Similarly each of the $\frac{N_2}{d}$ middle switches $MS(2 * \text{Log}_d N_2 - 3, 1)$ -
 $MS(2 * \text{Log}_d N_2 - 3, \frac{N_2}{d})$ in the middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 4)$ are connected
 from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 5)$ through $2 \times d$ links
 and also are connected to exactly d output switches in output stage 120 through $2 \times d$
 10 links.

Each of the $\frac{N_2}{d}$ output switches OS1 – OS(N_2/d) are connected from exactly d
 switches in middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 4)$ through $2 \times d$ links.

As described before, again the connection topology of a general
 $V_{mlink}(N_1, N_2, d, s)$ may be any one of the connection topologies. For example the
 15 connection topology of the network $V_{mlink}(N_1, N_2, d, s)$ may be back to back inverse
 Benes networks, back to back Omega networks, back to back Benes networks, Delta
 Networks and many more combinations. The applicant notes that the fundamental
 property of a valid connection topology of the general $V_{mlink}(N_1, N_2, d, s)$ network is,
 when no connections are setup from any input link if any output link should be reachable.
 20 Based on this property numerous embodiments of the network $V_{mlink}(N_1, N_2, d, s)$ can be
 built. The embodiments of FIG. 1A2 to FIG. 1J2 are ten examples of network
 $V_{mlink}(N_1, N_2, d, s)$ for $s = 2$ and $N_2 > N_1$.

The general symmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s \geq 2$ according to the current invention. Also the general symmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if

5 $s \geq 2$ according to the current invention.

For example, the network of Fig. 1C2 shows an exemplary five-stage network, namely $V_{mlink}(8, 24, 2, 2)$, with the following multicast assignment $I_1 = \{1, 4\}$ and all other $I_j = \phi$ for $j = [2-8]$. It should be noted that the connection I_1 fans out in the first stage switch IS1 into middle switches MS(1,1) and MS(1,4) in middle stage 130, and fans out

10 in middle switches MS(1,1) and MS(1,4) only once into middle switches MS(2,1) and MS(2,4) respectively in middle stage 140.

The connection I_1 also fans out in middle switches MS(2,1) and MS(2,4) only once into middle switches MS(3,1) and MS(3,4) respectively in middle stage 150. The connection I_1 also fans out in middle switches MS(3,1) and MS(3,4) only once into

15 output switches OS1 and OS4 in output stage 120. Finally the connection I_1 fans out once in the output stage switch OS1 into outlet link OL1 and in the output stage switch OS4 twice into the outlet links OL7 and OL8. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage 130.

20 **Symmetric Folded RNB Embodiments:**

The folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ disclosed, in the current invention, is topologically exactly the same as the multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$, disclosed in the current invention so far, excepting that in the illustrations folded network $V_{fold-mlink}(N_1, N_2, d, s)$ is shown as it is folded at middle

25 stage $130 + 10 * (\text{Log}_d N_2 - 2)$. This is true for all the embodiments presented in the current invention.

Referring to FIG. 2A, in one embodiment, an exemplary symmetrical folded multi-link multi-stage network 200A with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by four switches IS1-IS4 and output stage 120 consists of four, four by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, four by four switches MS(1,1) - MS(1,4), middle stage 140 consists of four, four by four switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by four switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N}{d}$, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by $\frac{N}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the notation $2d * d$. Likewise, the size of each switch in any of the middle stages can be denoted as $2d * 2d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric folded multi-link multi-stage network can be represented with the

notation $V_{fold-link}(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL1-IL8), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not
 5 necessary that there be the same number of inlet links IL1-IL8 as there are outlet links OL1-OL8, in a symmetrical network they are the same.

Each of the $\frac{N}{d}$ input switches IS1 – IS4 are connected to exactly $2 \times d$ switches in middle stage 130 through $2 \times d$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and also to middle switch
 10 MS(1,2) through the links ML(1,3) and ML(1,4)).

Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through $2 \times d$ links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,7) and ML(1,8) are connected to the middle switch MS(1,1) from
 15 input switch IS2) and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,3) and ML(2,4) are connected from middle switch MS(1,1) to middle switch MS(2,3)).

Similarly each of the $\frac{N}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage
 20 140 are connected from exactly d switches in middle stage 130 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,11) and ML(2,12) are connected to the middle switch MS(2,1) from middle switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through $2 \times d$ links (for example the links ML(3,1) and
 25 ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,3) and ML(3,4) are connected from middle switch MS(2,1) to middle switch MS(3,3)).

Similarly each of the $\frac{N}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,11) and ML(3,12) are connected to the middle switch MS(3,1) from middle switch MS(2,3)) and also are connected to exactly d output switches in output stage 120 through $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected to output switch OS1 from Middle switch MS(3,1), and the links ML(4,3) and ML(4,4) are connected to output switch OS2 from middle switch MS(3,1)).

Each of the $\frac{N}{d}$ output switches OS1 – OS4 are connected from exactly $2 \times d$ switches in middle stage 150 through $2 \times d$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1) and ML(4,2), and output switch OS1 is also connected from middle switch MS(3,2) through the links ML(4,7) and ML(4,8)).

Finally the connection topology of the network 200A shown in FIG. 2A is known to be back to back inverse Benes connection topology.

In other embodiments the connection topology may be different from the network 200A of FIG. 2A. That is the way the links ML(1,1) - ML(1,16), ML(2,1) - ML(2,16), ML(3,1) - ML(3,16), and ML(4,1) - ML(4,16) are connected between the respective stages is different. Even though only one embodiment is illustrated, in general, the network $V_{fold-link}(N, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{fold-link}(N, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{fold-link}(N, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network

$V_{fold-link}(N, d, s)$ can be built. The embodiment of FIG. 2A is only one example of network $V_{fold-link}(N, d, s)$.

In the embodiment of FIG. 2A each of the links ML(1,1) – ML(1,16), ML(2,1) – ML(2,16), ML(3,1) – ML(3,16) and ML(4,1) – ML(4,16) are either available for use by
 5 a new connection or not available if currently used by an existing connection. The input switches IS1-IS4 are also referred to as the network input ports. The input stage 110 is often referred to as the first stage. The output switches OS1-OS4 are also referred to as the network output ports. The output stage 120 is often referred to as the last stage. The middle stage switches MS(1,1) – MS(1,4) and MS(2,1) – MS(2,4) are referred to as
 10 middle switches or middle ports. The middle stage 130 is also referred to as root stage and middle stage switches MS(2,1) – MS(2,4) are referred to as root stage switches.

In the example illustrated in FIG. 2A, a fan-out of four is possible to satisfy a multicast connection request if input switch is IS2, but only two switches in middle stage 130 will be used. Similarly, although a fan-out of three is possible for a multicast
 15 connection request if the input switch is IS1, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage 130 when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network 200A, to be operated in
 20 rearrangeably nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage 130 is used to satisfy the request. Moreover,
 25 although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage 130, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the rearrangeably nonblocking nature of operation of the network for multicast connections).

However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Symmetric Folded RNB Embodiments:

Network 200B of FIG. 2B is an example of general symmetrical folded multi-link
 5 multi-stage network $V_{fold-link}(N, d, s)$ with $(2 \times \log_d N) - 1$ stages. The general
 symmetrical folded multi-link multi-stage network $V_{fold-link}(N, d, s)$ can be operated in
 rearrangeably nonblocking manner for multicast when $s \geq 2$ according to the current
 invention. Also the general symmetrical folded multi-link multi-stage network
 $V_{fold-link}(N, d, s)$ can be operated in strictly nonblocking manner for unicast if
 10 $s \geq 2$ according to the current invention. (And in the example of FIG. 2B, $s = 2$). The
 general symmetrical folded multi-link multi-stage network $V_{fold-link}(N, d, s)$ with
 $(2 \times \log_d N) - 1$ stages has d inlet links for each of $\frac{N}{d}$ input switches IS1-IS(N/d) (for
 example the links IL1-IL(d) to the input switch IS1) and $2 \times d$ outgoing links for each of
 $\frac{N}{d}$ input switches IS1-IS(N/d) (for example the links ML(1,1) - ML(1,2d) to the input
 15 switch IS1). There are d outlet links for each of $\frac{N}{d}$ output switches OS1-OS(N/d) (for
 example the links OL1-OL(d) to the output switch OS1) and $2 \times d$ incoming links for
 each of $\frac{N}{d}$ output switches OS1-OS(N/d) (for example $ML(2 \times \log_d N - 2, 1) -$
 $ML(2 \times \log_d N - 2, 2 \times d)$ to the output switch OS1).

Each of the $\frac{N}{d}$ input switches IS1 - IS(N/d) are connected to exactly d switches
 20 in middle stage 130 through $2 \times d$ links.

Each of the $\frac{N}{d}$ middle switches MS(1,1) - MS(1,N/d) in the middle stage 130 are
 connected from exactly d input switches through $2 \times d$ links and also are connected to
 exactly d switches in middle stage 140 through $2 \times d$ links.

Similarly each of the $\frac{N}{d}$ middle switches $MS(\text{Log}_d N - 1, 1) - MS(\text{Log}_d N - 1, \frac{N}{d})$

in the middle stage $130 + 10 * (\text{Log}_d N - 2)$ are connected from exactly d switches in middle stage $130 + 10 * (\text{Log}_d N - 3)$ through $2 \times d$ links and also are connected to exactly d switches in middle stage $130 + 10 * (\text{Log}_d N - 1)$ through $2 \times d$ links.

5 Similarly each of the $\frac{N}{d}$ middle switches $MS(2 * \text{Log}_d N - 3, 1) -$

$MS(2 * \text{Log}_d N - 3, \frac{N}{d})$ in the middle stage $130 + 10 * (2 * \text{Log}_d N - 4)$ are connected from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N - 5)$ through $2 \times d$ links and also are connected to exactly d output switches in output stage 120 through $2 \times d$ links.

Each of the $\frac{N}{d}$ output switches OS1 – OS(N/d) are connected from exactly d

10 switches in middle stage $130 + 10 * (2 * \text{Log}_d N - 4)$ through $2 \times d$ links.

As described before, again the connection topology of a general $V_{\text{fold-link}}(N, d, s)$ may be any one of the connection topologies. For example the connection topology of the network $V_{\text{fold-link}}(N, d, s)$ may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more
 15 combinations. The applicant notes that the fundamental property of a valid connection topology of the general $V_{\text{fold-link}}(N, d, s)$ network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network $V_{\text{fold-link}}(N, d, s)$ can be built. The embodiment of FIG. 1A is one example of network $V_{\text{fold-link}}(N, d, s)$.

20 The general symmetrical folded multi-link multi-stage network $V_{\text{fold-link}}(N, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s \geq 2$ according to the current invention. Also the general symmetrical folded multi-link multi-

stage network $V_{fold-link}(N, d, s)$ can be operated in strictly nonblocking manner for unicast if $s \geq 2$ according to the current invention.

Every switch in the folded multi-link multi-stage networks discussed herein has multicast capability. In a $V_{fold-link}(N, d, s)$ network, if a network inlet link is to be
 5 connected to more than one outlet link on the same output switch, then it is only necessary for the corresponding input switch to have one path to that output switch. This follows because that path can be multicast within the output switch to as many outlet links as necessary. Multicast assignments can therefore be described in terms of connections between input switches and output switches. An existing connection or a
 10 new connection from an input switch to r' output switches is said to have fan-out r' . If all multicast assignments of a first type, wherein any inlet link of an input switch is to be connected in an output switch to at most one outlet link are realizable, then multicast assignments of a second type, wherein any inlet link of each input switch is to be connected to more than one outlet link in the same output switch, can also be realized.
 15 For this reason, the following discussion is limited to general multicast connections of the first type (with fan-out r' , $1 \leq r' \leq \frac{N}{d}$) although the same discussion is applicable to the second type.

To characterize a multicast assignment, for each inlet link $i \in \left\{1, 2, \dots, \frac{N}{d}\right\}$, let
 $I_i = O$, where $O \subset \left\{1, 2, \dots, \frac{N}{d}\right\}$, denote the subset of output switches to which inlet link i
 20 is to be connected in the multicast assignment. For example, the network of Fig. 1C shows an exemplary five-stage network, namely $V_{mlink}(8, 2, 2)$, with the following multicast assignment $I_1 = \{2, 4\}$ and all other $I_j = \phi$ for $j = [2-8]$. It should be noted that the connection I_1 fans out in the first stage switch IS1 into middle switches MS(1,1) and MS(1,2) in middle stage 130, and fans out in middle switches MS(1,1) and MS(1,2) only
 25 once into middle switches MS(2,1) and MS(2,3) respectively in middle stage 140.

The connection I_1 also fans out in middle switches MS(2,1) and MS(2,3) only once into middle switches MS(3,2) and MS(3,4) respectively in middle stage 150. The connection I_1 also fans out in middle switches MS(3,2) and MS(3,4) only once into output switches OS2 and OS4 in output stage 120. Finally the connection I_1 fans out
 5 once in the output stage switch OS2 into outlet link OL3 and in the output stage switch OS4 twice into the outlet links OL7 and OL8. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage 130.

Asymmetric Folded RNB ($N_2 > N_1$) Embodiments:

10 Referring to FIG. 2C, in one embodiment, an exemplary asymmetrical folded multi-link multi-stage network 200C with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by
 15 four switches IS1-IS4 and output stage 120 consists of four, eight by six switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, four by four switches MS(1,1) - MS(1,4), middle stage 140 consists of four, four by four switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by eight switches MS(3,1) - MS(3,4).

20 Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the
 25 switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size eight by six, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and

of output stage 120 can be denoted in general with the variable $\frac{N_1}{d}$, where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_2 > N_1$ and $N_2 = p * N_1$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_1}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the notation $(d + d_2) * d_2$, where $d_2 = N_2 \times \frac{d}{N_1} = p \times d$. The size of each switch in any of the middle stages excepting the last middle stage can be denoted as $2d * 2d$. The size of each switch in the last middle stage can be denoted as $2d * (d + d_2)$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric folded multi-link multi-stage network can be represented with the notation $V_{fold-link}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL24), d represents the inlet links of each input switch where $N_2 > N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the $\frac{N_1}{d}$ input switches IS1 – IS4 are connected to exactly d switches in middle stage 130 through $2 \times d$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and also to middle switch MS(1,2) through the links ML(1,3) and ML(1,4)).

Each of the $\frac{N_1}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through $2 \times d$ links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,7) and ML(1,8) are connected to the middle switch MS(1,1) from input switch IS2) and also are connected to exactly d switches in middle stage 140

through $2 \times d$ links (for example the links $ML(2,1)$ and $ML(2,2)$ are connected from middle switch $MS(1,1)$ to middle switch $MS(2,1)$, and the links $ML(2,3)$ and $ML(2,4)$ are connected from middle switch $MS(1,1)$ to middle switch $MS(2,3)$).

Similarly each of the $\frac{N_1}{d}$ middle switches $MS(2,1) - MS(2,4)$ in the middle stage

- 5 140 are connected from exactly d switches in middle stage 130 through $2 \times d$ links (for example the links $ML(2,1)$ and $ML(2,2)$ are connected to the middle switch $MS(2,1)$ from middle switch $MS(1,1)$, and the links $ML(2,11)$ and $ML(2,12)$ are connected to the middle switch $MS(2,1)$ from middle switch $MS(1,3)$) and also are connected to exactly d switches in middle stage 150 through $2 \times d$ links (for example the links $ML(3,1)$ and
- 10 $ML(3,2)$ are connected from middle switch $MS(2,1)$ to middle switch $MS(3,1)$, and the links $ML(3,3)$ and $ML(3,4)$ are connected from middle switch $MS(2,1)$ to middle switch $MS(3,3)$).

Similarly each of the $\frac{N_1}{d}$ middle switches $MS(3,1) - MS(3,4)$ in the middle stage

- 150 are connected from exactly d switches in middle stage 140 through $2 \times d$ links (for
- 15 example the links $ML(3,1)$ and $ML(3,2)$ are connected to the middle switch $MS(3,1)$ from middle switch $MS(2,1)$, and the links $ML(3,11)$ and $ML(3,12)$ are connected to the middle switch $MS(3,1)$ from middle switch $MS(2,3)$) and also are connected to exactly $\frac{d + d_2}{2}$ output switches in output stage 120 through $d + d_2$ links (for example the links
- 20 $ML(4,1)$ and $ML(4,2)$ are connected to output switch OS1 from Middle switch $MS(3,1)$; the links $ML(4,3)$ and $ML(4,4)$ are connected to output switch OS2 from middle switch $MS(3,1)$; the links $ML(4,5)$ and $ML(4,6)$ are connected to output switch OS3 from Middle switch $MS(3,1)$; and the links $ML(4,7)$ and $ML(4,8)$ are connected to output switch OS4 from middle switch $MS(3,1)$).

Each of the $\frac{N_1}{d}$ output switches OS1 – OS4 are connected from exactly $\frac{d + d_2}{2}$

- 25 switches in middle stage 150 through $d + d_2$ links (for example output switch OS1 is connected from middle switch $MS(3,1)$ through the links $ML(4,1)$ and $ML(4,2)$; output

switch OS1 is also connected from middle switch MS(3,2) through the links ML(4,9) and ML(4,10); output switch OS1 is connected from middle switch MS(3,3) through the links ML(4,17) and ML(4,18); and output switch OS1 is also connected from middle switch MS(3,4) through the links ML(4,25) and ML(4,26)).

- 5 Finally the connection topology of the network 200C shown in FIG. 2C is known to be back to back inverse Benes connection topology.

In other embodiments the connection topology may be different from the network 200C of FIG. 2C. That is the way the links ML(1,1) - ML(1,16), ML(2,1) - ML(2,16), ML(3,1) - ML(3,16), and ML(4,1) - ML(4,16) are connected between the respective
 10 stages is different. Even though only one embodiment is illustrated, in general, the network $V_{fold-link}(N, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{fold-link}(N, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{fold-link}(N, d, s)$
 15 network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{fold-link}(N, d, s)$ can be built. The embodiment of FIG. 2C is only one example of network $V_{fold-link}(N, d, s)$.

In the embodiment of FIG. 2C each of the links ML(1,1) – ML(1,16), ML(2,1) – ML(2,16), ML(3,1) – ML(3,16) and ML(4,1) – ML(4,16) are either available for use by
 20 a new connection or not available if currently used by an existing connection. The input switches IS1-IS4 are also referred to as the network input ports. The input stage 110 is often referred to as the first stage. The output switches OS1-OS4 are also referred to as the network output ports. The output stage 120 is often referred to as the last stage. The
 25 middle stage switches MS(1,1) – MS(1,4) and MS(2,1) – MS(2,4) are referred to as middle switches or middle ports. The middle stage 130 is also referred to as root stage and middle stage switches MS(2,1) – MS(2,4) are referred to as root stage switches.

In the example illustrated in FIG. 2C, a fan-out of four is possible to satisfy a multicast connection request if input switch is IS2, but only two switches in middle stage 130 will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS1, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage 130 when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network 200C, to be operated in rearrangeably nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage 130 is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage 130, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the rearrangeably nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

20 **Generalized Asymmetric Folded RNB ($N_2 > N_1$) Embodiments:**

Network 200D of FIG. 2D is an example of general asymmetrical folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ with $(2 \times \log_d N_1) - 1$ stages where $N_2 > N_1$ and $N_2 = p * N_1$ where $p > 1$. In network 200D of FIG. 2D, $N_1 = N$ and $N_2 = p * N$. The general asymmetrical folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s \geq 2$ according to the current invention. Also the general asymmetrical folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if $s \geq 2$ according to the current invention. (And in the example of FIG. 2D, $s = 2$). The general asymmetrical folded multi-link multi-stage

- network $V_{fold-link}(N_1, N_2, d, s)$ with $(2 \times \log_d N_1) - 1$ stages has d inlet links for each of $\frac{N_1}{d}$ input switches IS1-IS(N_1/d) (for example the links IL1-IL(d) to the input switch IS1) and $2 \times d$ outgoing links for each of $\frac{N_1}{d}$ input switches IS1-IS(N_1/d) (for example the links ML(1,1) - ML(1,2d) to the input switch IS1). There are d_2 (where
- 5 $d_2 = N_2 \times \frac{d}{N_1} = p \times d$) outlet links for each of $\frac{N_1}{d}$ output switches OS1-OS(N_1/d) (for example the links OL1-OL($p \times d$) to the output switch OS1) and $d + d_2 (= d + p \times d)$ incoming links for each of $\frac{N_1}{d}$ output switches OS1-OS(N_1/d) (for example ML($2 \times \log_d N_1 - 2, 1$) - ML($2 \times \log_d N_1 - 2, d + d_2$) to the output switch OS1).

- Each of the $\frac{N_1}{d}$ input switches IS1 - IS(N_1/d) are connected to exactly $2 \times d$
- 10 switches in middle stage 130 through $2 \times d$ links.

Each of the $\frac{N_1}{d}$ middle switches MS(1,1) - MS(1, N_1/d) in the middle stage 130 are connected from exactly d input switches through $2 \times d$ links and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links.

- Similarly each of the $\frac{N_1}{d}$ middle switches MS($\log_d N_1 - 1, 1$) -
- 15 MS($\log_d N_1 - 1, \frac{N_1}{d}$) in the middle stage $130 + 10 * (\log_d N_1 - 2)$ are connected from exactly d switches in middle stage $130 + 10 * (\log_d N_1 - 3)$ through $2 \times d$ links and also are connected to exactly d switches in middle stage $130 + 10 * (\log_d N_1 - 1)$ through $2 \times d$ links.

Similarly each of the $\frac{N_1}{d}$ middle switches $MS(2 \times \text{Log}_d N_1 - 3, 1) - MS(2 \times \text{Log}_d N_1 - 3, \frac{N_1}{d})$ in the middle stage $130 + 10 * (2 * \text{Log}_d N_1 - 4)$ are connected from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N_1 - 5)$ through $2 \times d$ links and also are connected to exactly $\frac{d + d_2}{2}$ output switches in output stage 120 through

5 $d + d_2$ links.

Each of the $\frac{N_1}{d}$ output switches OS1 – OS(N_1/d) are connected from exactly $\frac{d + d_2}{2}$ switches in middle stage $130 + 10 * (2 * \text{Log}_d N_1 - 4)$ through $d + d_2$ links.

As described before, again the connection topology of a general $V_{fold-link}(N_1, N_2, d, s)$ may be any one of the connection topologies. For example the

10 connection topology of the network $V_{fold-link}(N_1, N_2, d, s)$ may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general $V_{fold-link}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link if any output link should be reachable.

15 Based on this property numerous embodiments of the network $V_{fold-link}(N_1, N_2, d, s)$ can be built. The embodiment of FIG. 1C is one example of network $V_{fold-link}(N_1, N_2, d, s)$ for $s = 2$ and $N_2 > N_1$.

The general symmetrical folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for

20 multicast when $s \geq 2$ according to the current invention. Also the general symmetrical folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if $s \geq 2$ according to the current invention.

For example, the network of Fig. 2C shows an exemplary five-stage network, namely $V_{fold-link}(8,24,2,2)$, with the following multicast assignment $I_1 = \{1,4\}$ and all other $I_j = \phi$ for $j = [2-8]$. It should be noted that the connection I_1 fans out in the first stage switch IS1 into middle switches MS(1,1) and MS(1,2) in middle stage 130, and fans
 5 out in middle switches MS(1,1) and MS(1,2) only once into middle switches MS(2,1) and MS(2,3) respectively in middle stage 140.

The connection I_1 also fans out in middle switches MS(2,1) and MS(2,3) only once into middle switches MS(3,1) and MS(3,4) respectively in middle stage 150. The connection I_1 also fans out in middle switches MS(3,1) and MS(3,4) only once into
 10 output switches OS1 and OS4 in output stage 120. Finally the connection I_1 fans out once in the output stage switch OS1 into outlet link OL2 and in the output stage switch OS4 twice into the outlet links OL20 and OL23. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage 130.

15 **Asymmetric Folded RNB ($N_1 > N_2$) Embodiments:**

Referring to FIG. 2E, in one embodiment, an exemplary asymmetrical folded multi-link multi-stage network 200E with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via
 20 middle stages 130, 140, and 150 is shown where input stage 110 consists of four, six by eight switches IS1-IS4 and output stage 120 consists of four, four by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, eight by four switches MS(1,1) - MS(1,4), middle stage 140 consists of four, four by four switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by four switches MS(3,1)
 25 - MS(3,4).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size six by eight, the switches in output stage 120 are of size four by two, and there are four switches in each

of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size six by eight, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle
 5 stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_2}{d}$, where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1 > N_2$ and
 10 $N_1 = p * N_2$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_2}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d_1 * (d + d_1)$ and each output switch OS1-OS4 can be denoted in general with the notation $(2 * d * d)$, where $d_1 = N_1 * \frac{d}{N_2} = p * d$. The size of each switch in any of the middle stages excepting the first middle stage can be denoted as $2d * 2d$. The
 15 size of each switch in the first middle stage can be denoted as $(d + d_1) * 2d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric folded multi-link multi-stage network can be represented with the notation $V_{fold-link}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links
 20 IL1-IL24), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL8), d represents the inlet links of each input switch where $N_1 > N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the $\frac{N_2}{d}$ input switches IS1 – IS4 are connected to exactly $\frac{d + d_1}{2}$
 25 switches in middle stage 130 through $d + d_1$ links (for example input switch IS1 is

connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2); input switch IS1 is connected to middle switch MS(1,2) through the links ML(1,3) and ML(1,4); input switch IS1 is connected to middle switch MS(1,3) through the links ML(1,5), ML(1,6); and input switch IS1 is also connected to middle switch MS(1,4) through the links
 5 ML(1,7) and ML(1,8)).

Each of the $\frac{N_2}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly $\frac{d+d_1}{2}$ input switches through $d+d_1$ links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1; the links ML(1,9) and ML(1,10) are connected to the middle switch MS(1,1) from input switch IS2; the links ML(1,17) and ML(1,18) are connected to the middle switch MS(1,1) from input switch IS3; and the links ML(1,25) and ML(1,26) are connected to the middle switch MS(1,1) from input switch IS4) and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch
 10 MS(2,1), and the links ML(2,3) and ML(2,4) are connected from middle switch MS(1,1) to middle switch MS(2,3)).

Similarly each of the $\frac{N_2}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,11) and ML(2,12) are connected to the middle switch MS(2,1) from middle switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,3) and ML(3,4) are connected from middle switch MS(2,1) to middle switch
 20 MS(3,3)).

Similarly each of the $\frac{N_2}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,11) and ML(3,12) are connected to the middle switch MS(3,1) from middle switch MS(2,3)) and also are connected to exactly d output switches in output stage 120 through $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected to output switch OS1 from middle switch MS(3,1); and the links ML(4,3) and ML(4,4) are connected to output switch OS2 from middle switch MS(3,1)).

Each of the $\frac{N_2}{d}$ output switches OS1 – OS4 are connected from exactly d switches in middle stage 150 through $2 \times d$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1) and ML(4,2); and output switch OS1 is also connected from middle switch MS(3,2) through the links ML(4,7) and ML(4,8)).

Finally the connection topology of the network 200E shown in FIG. 2E is known to be back to back inverse Benes connection topology.

In other embodiments the connection topology may be different from the network 200E of FIG. 2E. That is the way the links ML(1,1) - ML(1,16), ML(2,1) - ML(2,16), ML(3,1) - ML(3,16), and ML(4,1) - ML(4,16) are connected between the respective stages is different. Even though only one embodiment is illustrated, in general, the network $V_{fold-link}(N, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{fold-link}(N, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{fold-link}(N, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network

$V_{fold-link}(N, d, s)$ can be built. The embodiment of FIG. 2E is only one example of network $V_{fold-link}(N, d, s)$.

In the embodiment of FIG. 2E each of the links ML(1,1) – ML(1,16), ML(2,1) – ML(2,16), ML(3,1) – ML(3,16) and ML(4,1) – ML(4,16) are either available for use by
 5 a new connection or not available if currently used by an existing connection. The input switches IS1-IS4 are also referred to as the network input ports. The input stage 110 is often referred to as the first stage. The output switches OS1-OS4 are also referred to as the network output ports. The output stage 120 is often referred to as the last stage. The middle stage switches MS(1,1) – MS(1,4) and MS(2,1) – MS(2,4) are referred to as
 10 middle switches or middle ports. The middle stage 130 is also referred to as root stage and middle stage switches MS(2,1) – MS(2,4) are referred to as root stage switches.

In the example illustrated in FIG. 2E, a fan-out of four is possible to satisfy a multicast connection request if input switch is IS2, but only two switches in middle stage 130 will be used. Similarly, although a fan-out of three is possible for a multicast
 15 connection request if the input switch is IS1, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage 130 when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network 200E, to be operated in rearrangeably
 20 nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch is used to satisfy the request. Moreover, although in the above-
 25 described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage 130, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the rearrangeably nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may

be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Asymmetric Folded RNB ($N_2 > N_1$) Embodiments:

Network 200F of FIG. 2F is an example of general asymmetrical folded multi-link
 5 multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ with $(2 \times \log_d N_2) - 1$ stages where $N_1 > N_2$
 and $N_1 = p * N_2$ where $p > 1$. In network 200F of FIG. 2F, $N_2 = N$ and $N_1 = p * N$. The
 general asymmetrical folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ can
 be operated in rearrangeably nonblocking manner for multicast when $s \geq 2$ according to
 the current invention. Also the general asymmetrical folded multi-link multi-stage
 10 network $V_{fold-link}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for
 unicast if $s \geq 2$ according to the current invention. (And in the example of FIG. 2F,
 $s = 2$). The general asymmetrical folded multi-link multi-stage network

$V_{fold-link}(N_1, N_2, d, s)$ with $(2 \times \log_d N_2) - 1$ stages has d_1 (where $d_1 = N_1 \times \frac{d}{N_2} = p \times d$

inlet links for each of $\frac{N_2}{d}$ input switches IS1-IS(N_2/d) (for example the links IL1-

15 IL($p*d$) to the input switch IS1) and $d + d_1$ ($= d + p \times d$) outgoing links for each of $\frac{N_2}{d}$
 input switches IS1-IS(N_2/d) (for example the links ML(1,1) - ML(1,($d+p*d$)) to the input
 switch IS1). There are d outlet links for each of $\frac{N_2}{d}$ output switches OS1-OS(N_2/d) (for
 example the links OL1-OL(d) to the output switch OS1) and $2 \times d$ incoming links for
 each of $\frac{N_2}{d}$ output switches OS1-OS(N_2/d) (for example ML($2 \times \log_d N_2 - 2, 1$) -
 20 ML($2 \times \log_d N_2 - 2, 2 \times d$) to the output switch OS1).

Each of the $\frac{N_2}{d}$ input switches IS1 - IS(N_2/d) are connected to exactly $\frac{d + d_1}{2}$

switches in middle stage 130 through $d + d_1$ links.

Each of the $\frac{N_2}{d}$ middle switches $MS(1,1) - MS(1,N_2/d)$ in the middle stage 130 are connected from exactly d input switches through $2 \times d$ links and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links.

Similarly each of the $\frac{N_2}{d}$ middle switches $MS(\text{Log}_d N_2 - 1, 1) -$

- 5 $MS(\text{Log}_d N_2 - 1, \frac{N_2}{d})$ in the middle stage $130 + 10 * (\text{Log}_d N_2 - 2)$ are connected from exactly d switches in middle stage $130 + 10 * (\text{Log}_d N_2 - 3)$ through $2 \times d$ links and also are connected to exactly d switches in middle stage $130 + 10 * (\text{Log}_d N_2 - 1)$ through $2 \times d$ links.

Similarly each of the $\frac{N_2}{d}$ middle switches $MS(2 * \text{Log}_d N_2 - 3, 1) -$

- 10 $MS(2 * \text{Log}_d N_2 - 3, \frac{N_2}{d})$ in the middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 4)$ are connected from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 5)$ through $2 \times d$ links and also are connected to exactly d output switches in output stage 120 through $2 \times d$ links.

Each of the $\frac{N_2}{d}$ output switches $OS1 - OS(N_2/d)$ are connected from exactly d

- 15 switches in middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 4)$ through $2 \times d$ links.

As described before, again the connection topology of a general

- $V_{\text{fold-link}}(N_1, N_2, d, s)$ may be any one of the connection topologies. For example the connection topology of the network $V_{\text{fold-link}}(N_1, N_2, d, s)$ may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta
- 20 Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general $V_{\text{fold-link}}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link if any output link should be reachable.

Based on this property numerous embodiments of the network $V_{fold-link}(N_1, N_2, d, s)$ can be built. The embodiment of FIG. 2F is one example of network $V_{fold-link}(N_1, N_2, d, s)$ for $s = 2$ and $N_2 > N_1$.

- The general symmetrical folded multi-link multi-stage network
- 5 $V_{fold-link}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s \geq 2$ according to the current invention. Also the general symmetrical folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if $s \geq 2$ according to the current invention.

- For example, the network of Fig. 2E shows an exemplary five-stage network,
- 10 namely $V_{fold-link}(8, 24, 2, 2)$, with the following multicast assignment $I_1 = \{1, 4\}$ and all other $I_j = \phi$ for $j = [2-8]$. It should be noted that the connection I_1 fans out in the first stage switch IS1 into middle switches MS(1,1) and MS(1,4) in middle stage 130, and fans out in middle switches MS(1,1) and MS(1,4) only once into middle switches MS(2,1) and MS(2,4) respectively in middle stage 140.

- 15 The connection I_1 also fans out in middle switches MS(2,1) and MS(2,4) only once into middle switches MS(3,1) and MS(3,4) respectively in middle stage 150. The connection I_1 also fans out in middle switches MS(3,1) and MS(3,4) only once into output switches OS1 and OS4 in output stage 120. Finally the connection I_1 fans out once in the output stage switch OS1 into outlet link OL1 and in the output stage switch
- 20 OS4 twice into the outlet links OL7 and OL8. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage 130.

SNB MULTI-LINK MULTI-STAGE EMBODIMENTS:

Symmetric SNB Embodiments:

- 25 Referring to FIG. 3A, in one embodiment, an exemplary symmetrical multi-link multi-stage network 300A with five stages of twenty switches for satisfying

communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by six switches IS1-IS4 and output stage 120 consists of four, six by two switches OS1-OS4.

5 And all the middle stages namely middle stage 130 consists of four, six by six switches MS(1,1) - MS(1,4), middle stage 140 consists of four, six by six switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, six by six switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by six, the

10 switches in output stage 120 are of size six by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N}{d}$, where N is the total

15 number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by $\frac{N}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 3d$ and each output switch OS1-OS4 can be denoted in general with the notation $3d * d$. Likewise, the size of each switch in any of the middle stages can be denoted as $3d * 3d$. A switch as used herein can be either a crossbar switch, or a network

20 of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL1-IL8), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each

25 input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL1-IL8 as there are outlet links OL1-OL8, in a symmetrical network they are the same.

Each of the $\frac{N}{d}$ input switches IS1 – IS4 are connected to exactly $3 \times d$ switches

in middle stage 130 through $3 \times d$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and ML(1,3); and also to middle switch MS(1,2) through the links ML(1,4), ML(1,5), and ML(1,6)).

- 5 Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through $3 \times d$ links (for example the links ML(1,1), ML(1,2), and ML(1,3) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,10), ML(1,11), and ML(1,12) are connected to the middle switch MS(1,1) from input switch IS2) and also are connected to exactly d switches in
- 10 middle stage 140 through $3 \times d$ links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,4), ML(2,5), and ML(2,6) are connected from middle switch MS(1,1) to middle switch MS(2,3)).

- Similarly each of the $\frac{N}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage
- 15 140 are connected from exactly d switches in middle stage 130 through $3 \times d$ links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,16), ML(2,17), and ML(2,18) are connected to the middle switch MS(2,1) from middle switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through $3 \times d$ links (for example the
- 20 links ML(3,1), ML(3,2), and ML(3,3) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,4), ML(3,5), and ML(3,6) are connected from middle switch MS(2,1) to middle switch MS(3,3)).

- Similarly each of the $\frac{N}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage
- 150 are connected from exactly d switches in middle stage 140 through $3 \times d$ links (for
- 25 example the links ML(3,1), ML(3,2), and ML(3,3) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,16), ML(3,17), and ML(3,18)

are connected to the middle switch MS(3,1) from middle switch MS(2,3)) and also are connected to exactly d output switches in output stage 120 through $3 \times d$ links (for example the links ML(4,1), ML(4,2), and ML(4,3) are connected to output switch OS1 from Middle switch MS(3,1), and the links ML(4,10), ML(4,11), and ML(4,12) are
 5 connected to output switch OS2 from middle switch MS(3,1)).

Each of the $\frac{N}{d}$ output switches OS1 – OS4 are connected from exactly $3 \times d$ switches in middle stage 150 through $3 \times d$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1), ML(4,2), and ML(4,3), and output switch OS1 is also connected from middle switch MS(3,2) through
 10 the links ML(4,10), ML(4,11) and ML(4,12)).

Finally the connection topology of the network 300A shown in FIG. 3A is known to be back to back inverse Benes connection topology.

Referring to FIG. 3B, in another embodiment of network $V_{mlink}(N, d, s)$, an exemplary symmetrical multi-link multi-stage network 300B with five stages of twenty
 15 switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by six switches IS1-IS4 and output stage 120 consists of four, six by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of
 20 four, six by six switches MS(1,1) - MS(1,4), middle stage 140 consists of four, six by six switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, six by six switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by six, the
 25 switches in output stage 120 are of size six by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and

of output stage 120 can be denoted in general with the variable $\frac{N}{d}$, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by $\frac{N}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 3d$ and each output switch OS1-OS4 can be denoted in general with the notation $3d * d$. Likewise, the size of each switch in any of the middle stages can be denoted as $3d * 3d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The symmetric multi-link multi-stage network of FIG. 3B is also the network of the type $V_{mlink}(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL1-IL8), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL1-IL8 as there are outlet links OL1-OL8, in a symmetrical network they are the same.

Each of the $\frac{N}{d}$ input switches IS1 – IS4 are connected to exactly $3 \times d$ switches in middle stage 130 through $3 \times d$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and ML(1,3); and also to middle switch MS(1,2) through the links ML(1,4), ML(1,5), and ML(1,6)).

Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through $3 \times d$ links (for example the links ML(1,1), ML(1,2), and ML(1,3) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,13), ML(1,14), and ML(1,15) are connected to the middle switch MS(1,1) from input switch IS3) and also are connected to exactly d switches in middle stage 140 through $3 \times d$ links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected from middle switch MS(1,1) to middle switch MS(2,1); and the links ML(2,4), ML(2,5), and ML(2,6) are connected from middle switch MS(1,1) to middle switch MS(2,2)).

Similarly each of the $\frac{N}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through $3 \times d$ links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,13), ML(2,14), and ML(2,15) are connected to the middle switch MS(2,1) from middle switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through $3 \times d$ links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,4), ML(3,5) and ML(3,6) are connected from middle switch MS(2,1) to middle switch MS(3,2)).

10 Similarly each of the $\frac{N}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $3 \times d$ links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,13), ML(3,14), and ML(3,15) are connected to the middle switch MS(3,1) from middle switch MS(2,3)) and also are connected to exactly d output switches in output stage 120 through $3 \times d$ links (for example the links ML(4,1), ML(4,2), and ML(4,3) are connected to output switch OS1 from Middle switch MS(3,1), and the links ML(4,4), ML(4,5), and ML(4,6) are connected to output switch OS2 from middle switch MS(3,1)).

Each of the $\frac{N}{d}$ output switches OS1 – OS4 are connected from exactly $3 \times d$ switches in middle stage 150 through $3 \times d$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1), ML(4,2), and ML(4,3), and output switch OS1 is also connected from middle switch MS(3,3) through the links ML(4,13), ML(4,14), and ML(4,15)).

Finally the connection topology of the network 300B shown in FIG. 3B is known to be back to back Omega connection topology.

Referring to FIG. 3C, in another embodiment of network $V_{mlink}(N, d, s)$, an exemplary symmetrical multi-link multi-stage network 300C with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by six switches IS1-IS4 and output stage 120 consists of four, six by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, six by six switches MS(1,1) - MS(1,4), middle stage 140 consists of four, six by six switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, six by six switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by six, the switches in output stage 120 are of size six by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N}{d}$, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by $\frac{N}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 3d$ and each output switch OS1-OS4 can be denoted in general with the notation $3d * d$. Likewise, the size of each switch in any of the middle stages can be denoted as $3d * 3d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The symmetric multi-link multi-stage network of FIG. 3C is also the network of the type $V_{mlink}(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL1-IL8), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there

be the same number of inlet links IL1-IL8 as there are outlet links OL1-OL8, in a symmetrical network they are the same.

Each of the $\frac{N}{d}$ input switches IS1 – IS4 are connected to exactly $3 \times d$ switches in middle stage 130 through $3 \times d$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and ML(1,3); and also to middle switch MS(1,2) through the links ML(1,4), ML(1,5), and ML(1,6)).

Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through $3 \times d$ links (for example the links ML(1,1), ML(1,2), and ML(1,3) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,22), ML(1,23), and ML(1,24) are connected to the middle switch MS(1,1) from input switch IS4) and also are connected to exactly d switches in middle stage 140 through $3 \times d$ links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,4), ML(2,5), and ML(2,6) are connected from middle switch MS(1,1) to middle switch MS(2,2)).

Similarly each of the $\frac{N}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through $3 \times d$ links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,22), ML(2,23), and ML(2,24) are connected to the middle switch MS(2,1) from middle switch MS(1,4)) and also are connected to exactly d switches in middle stage 150 through $3 \times d$ links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,4), ML(3,5), and ML(3,6) are connected from middle switch MS(2,1) to middle switch MS(3,2)).

Similarly each of the $\frac{N}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $3 \times d$ links (for

example the links ML(3,1), ML(3,2), and ML(3,3) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,22), ML(3,23), and ML(3,24) are connected to the middle switch MS(3,1) from middle switch MS(2,4) and also are connected to exactly d output switches in output stage 120 through $3 \times d$ links (for
 5 example the links ML(4,1), ML(4,2), and ML(4,3) are connected to output switch OS1 from middle switch MS(3,1), and the links ML(4,4), ML(4,5), and ML(4,6) are connected to output switch OS2 from middle switch MS(3,1)).

Each of the $\frac{N}{d}$ output switches OS1 – OS4 are connected from exactly $3 \times d$ switches in middle stage 150 through $3 \times d$ links (for example output switch OS1 is
 10 connected from middle switch MS(3,1) through the links ML(4,1), ML(4,2), and ML(4,3), and output switch OS1 is also connected from middle switch MS(3,4) through the links ML(4,22), ML(4,23), and ML(4,24)).

Finally the connection topology of the network 300C shown in FIG. 3C is hereinafter called nearest neighbor connection topology.

15 Similar to network 300A of FIG. 3A, 300B of FIG. 3B, and 300C of FIG. 3C, referring to FIG. 3D, FIG. 3E, FIG. 3F, FIG. 3G, FIG. 3H, FIG. 3I and FIG. 3J with exemplary symmetrical multi-link multi-stage networks 300D, 300E, 300F, 300G, 300H, 300I, and 300J respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection
 20 between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by six switches IS1-IS4 and output stage 120 consists of four, six by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, six by six switches MS(1,1) - MS(1,4), middle stage 140 consists of four, six by six switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, six by six switches MS(3,1) - MS(3,4).
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Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by six, the

switches in output stage 120 are of size six by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

The networks 300D, 300E, 300F, 300G, 300H, 300I and 300J of FIG. 3D, FIG. 3E, FIG. 3F, FIG. 3G, FIG. 3H, FIG. 3I, and FIG. 3J are also embodiments of symmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL1-IL8), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL1-IL8 as there are outlet links OL1-OL8, in a symmetrical network they are the same.

Just like networks of 300A, 300B and 300C, for all the networks 300D, 300E, 300F, 300G, 300H, 300I and 300J of FIG. 3D, FIG. 3E, FIG. 3F, FIG. 3G, FIG. 3H, FIG. 3I, and FIG. 3J, each of the $\frac{N}{d}$ input switches IS1 – IS4 are connected to exactly $3 \times d$ switches in middle stage 130 through $3 \times d$ links.

Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through $3 \times d$ links and also are connected to exactly d switches in middle stage 140 through $3 \times d$ links.

Similarly each of the $\frac{N}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through $3 \times d$ links and also are connected to exactly d switches in middle stage 150 through $3 \times d$ links.

Similarly each of the $\frac{N}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $3 \times d$ links and also are connected to exactly d output switches in output stage 120 through $3 \times d$ links.

Each of the $\frac{N}{d}$ output switches OS1 – OS4 are connected from exactly $3 \times d$ switches in middle stage 150 through $3 \times d$ links.

In all the ten embodiments of FIG. 3A to FIG. 3J the connection topology is different. That is the way the links ML(1,1) - ML(1,24), ML(2,1) - ML(2,24), ML(3,1) - ML(3,24), and ML(4,1) - ML(4,24) are connected between the respective stages is different. Even though only ten embodiments are illustrated, in general, the network $V_{mlink}(N, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{mlink}(N, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{mlink}(N, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{mlink}(N, d, s)$ can be built. The ten embodiments of FIG. 3A to FIG. 3J are only three examples of network $V_{mlink}(N, d, s)$.

In all the ten embodiments of FIG. 3A to FIG. 3J, each of the links ML(1,1) – ML(1,24), ML(2,1) – ML(2,24), ML(3,1) – ML(3,24) and ML(4,1) – ML(4,24) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS1-IS4 are also referred to as the network input ports. The input stage 110 is often referred to as the first stage. The output switches OS1-OS4 are also referred to as the network output ports. The output stage 120 is often referred to as the last stage. The middle stage switches MS(1,1) – MS(1,4), MS(2,1) – MS(2,4), and MS(3,1) – MS(3,4) are referred to as middle switches or middle ports.

In the example illustrated in FIG. 3A (or in FIG1B to FIG. 3J), a fan-out of four is possible to satisfy a multicast connection request if input switch is IS2, but only two switches in middle stage 130 will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS1, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage 130 when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected

to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network 300A (or 300B to 300J), to be operated in strictly nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection
 5 request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage 130 is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage 130, the limit can be greater depending
 10 on the number of middle stage switches in a network (while maintaining the strictly nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Symmetric SNB Embodiments:

15 Network 300K of FIG. 3K is an example of general symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ with $(2 \times \log_d N) - 1$ stages. The general symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ can be operated in strictly nonblocking manner for multicast when $s \geq 3$ according to the current invention (and in the example of FIG. 3K, $s = 3$). The general symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ with
 20 $(2 \times \log_d N) - 1$ stages has d inlet links for each of $\frac{N}{d}$ input switches IS1-IS(N/d) (for example the links IL1-IL(d) to the input switch IS1) and $3 \times d$ outgoing links for each of $\frac{N}{d}$ input switches IS1-IS(N/d) (for example the links ML(1,1) - ML(1,3d) to the input switch IS1). There are d outlet links for each of $\frac{N}{d}$ output switches OS1-OS(N/d) (for example the links OL1-OL(d) to the output switch OS1) and $3 \times d$ incoming links for
 25 each of $\frac{N}{d}$ output switches OS1-OS(N/d) (for example $ML(2 \times \log_d N - 2, 1) - ML(2 \times \log_d N - 2, 3 \times d)$ to the output switch OS1).

Each of the $\frac{N}{d}$ input switches IS1 – IS(N/d) are connected to exactly d switches in middle stage 130 through $3 \times d$ links.

Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,N/d) in the middle stage 130 are connected from exactly d input switches through $3 \times d$ links and also are connected to exactly d switches in middle stage 140 through $3 \times d$ links.

Similarly each of the $\frac{N}{d}$ middle switches $MS(\text{Log}_d N - 1, 1) - MS(\text{Log}_d N - 1, \frac{N}{d})$ in the middle stage $130 + 10 * (\text{Log}_d N - 2)$ are connected from exactly d switches in middle stage $130 + 10 * (\text{Log}_d N - 3)$ through $3 \times d$ links and also are connected to exactly d switches in middle stage $130 + 10 * (\text{Log}_d N - 1)$ through $3 \times d$ links.

10 Similarly each of the $\frac{N}{d}$ middle switches $MS(2 * \text{Log}_d N - 3, 1) - MS(2 * \text{Log}_d N - 3, \frac{N}{d})$ in the middle stage $130 + 10 * (2 * \text{Log}_d N - 4)$ are connected from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N - 5)$ through $3 \times d$ links and also are connected to exactly d output switches in output stage 120 through $3 \times d$ links.

Each of the $\frac{N}{d}$ output switches OS1 – OS(N/d) are connected from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N - 4)$ through $3 \times d$ links.

As described before, again the connection topology of a general $V_{mlink}(N, d, s)$ may be any one of the connection topologies. For example the connection topology of the network $V_{mlink}(N, d, s)$ may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general $V_{mlink}(N, d, s)$ network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous

embodiments of the network $V_{mlink}(N, d, s)$ can be built. The embodiments of FIG. 3A to FIG. 3J are ten examples of network $V_{mlink}(N, d, s)$.

The general symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ can be operated in strictly nonblocking manner for multicast when $s \geq 3$ according to the current invention.

Every switch in the multi-link multi-stage networks discussed herein has multicast capability. In a $V_{mlink}(N, d, s)$ network, if a network inlet link is to be connected to more than one outlet link on the same output switch, then it is only necessary for the corresponding input switch to have one path to that output switch. This follows because that path can be multicast within the output switch to as many outlet links as necessary. Multicast assignments can therefore be described in terms of connections between input switches and output switches. An existing connection or a new connection from an input switch to r' output switches is said to have fan-out r' . If all multicast assignments of a first type, wherein any inlet link of an input switch is to be connected in an output switch to at most one outlet link are realizable, then multicast assignments of a second type, wherein any inlet link of each input switch is to be connected to more than one outlet link in the same output switch, can also be realized. For this reason, the following discussion is limited to general multicast connections of the first type (with fan-out r' , $1 \leq r' \leq \frac{N}{d}$) although the same discussion is applicable to the second type.

To characterize a multicast assignment, for each inlet link $i \in \left\{1, 2, \dots, \frac{N}{d}\right\}$, let $I_i = O$, where $O \subset \left\{1, 2, \dots, \frac{N}{d}\right\}$, denote the subset of output switches to which inlet link i is to be connected in the multicast assignment. For example, the network of Fig. 3C shows an exemplary five-stage network, namely $V_{mlink}(8, 2, 3)$, with the following multicast assignment $I_1 = \{1, 4\}$ and all other $I_j = \phi$ for $j = [2-8]$. It should be noted that the connection I_1 fans out in the first stage switch IS1 into middle switches MS(1,1) and

MS(1,2) in middle stage 130, and fans out in middle switches MS(1,1) and MS(1,2) only once into middle switches MS(2,1) and MS(2,3) respectively in middle stage 140.

The connection I_1 also fans out in middle switches MS(2,1) and MS(2,3) only once into middle switches MS(3,1) and MS(3,4) respectively in middle stage 150. The connection I_1 also fans out in middle switches MS(3,1) and MS(3,4) only once into output switches OS1 and OS4 in output stage 120. Finally the connection I_1 fans out once in the output stage switch OS1 into outlet link OL1 and in the output stage switch OS4 twice into the outlet links OL7 and OL8. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage 130.

Asymmetric SNB ($N_2 > N_1$) Embodiments:

Referring to FIG. 3A1, in one embodiment, an exemplary asymmetrical multi-link multi-stage network 300A1 with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by six switches IS1-IS4 and output stage 120 consists of four, eight by six switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, six by six switches MS(1,1) - MS(1,4), middle stage 140 consists of four, six by six switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by eight switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by six, the switches in output stage 120 are of size eight by six, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and

of output stage 120 can be denoted in general with the variable $\frac{N_1}{d}$, where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_2 > N_1$ and $N_2 = p * N_1$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_1}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 3d$ and each output switch OS1-OS4 can be denoted in general with the notation $(2d + d_2) * d_2$, where $d_2 = N_2 \times \frac{d}{N_1} = p \times d$. The size of each switch in any of the middle stages excepting the last middle stage can be denoted as $3d * 3d$. The size of each switch in the last middle stage can be denoted as $3d * (2d + d_2)$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL24), d represents the inlet links of each input switch where $N_2 > N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the $\frac{N_1}{d}$ input switches IS1 – IS4 are connected to exactly d switches in middle stage 130 through $3 \times d$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and ML(1,3); and also to middle switch MS(1,2) through the links ML(1,4), ML(1,5), and ML(1,6)).

Each of the $\frac{N_1}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through $3 \times d$ links (for example the links ML(1,1), ML(1,2), and ML(1,3) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,13), ML(1,14), and ML(1,15) are connected to the middle switch MS(1,1) from input switch IS3) and also are connected to exactly d switches in

Each of the $\frac{N_1}{d}$ output switches OS1 – OS4 are connected from exactly $\frac{2d + d_2}{3}$ switches in middle stage 150 through $2d + d_2$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1), ML(4,2), and ML(4,3); output switch OS1 is also connected from middle switch MS(3,2) through the links ML(4,16), ML(4,17), and ML(4,18); output switch OS1 is connected from middle switch MS(3,3) through the links ML(4,28), ML(4,29), and ML(4,30); and output switch OS1 is also connected from middle switch MS(3,4) through the links ML(4,43), ML(4,44), and ML(4,45)).

Finally the connection topology of the network 300A1 shown in FIG. 3A1 is known to be back to back inverse Benes connection topology.

Referring to FIG. 3B1, in one embodiment, an exemplary asymmetrical multi-link multi-stage network 300B1 with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by six switches IS1-IS4 and output stage 120 consists of four, eight by six switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, six by six switches MS(1,1) - MS(1,4), middle stage 140 consists of four, six by six switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by eight switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by six, the switches in output stage 120 are of size eight by six, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_1}{d}$, where N_1 is the total

number of inlet links or and N_2 is the total number of outlet links and $N_2 > N_1$ and $N_2 = p * N_1$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_1}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 3d$ and each output switch OS1-OS4 can be denoted in general with the

5 notation $(2d + d_2) * d_2$, where $d_2 = N_2 \times \frac{d}{N_1} = p \times d$. The size of each switch in any of the middle stages excepting the last middle stage can be denoted as $3d * 3d$. The size of each switch in the last middle stage can be denoted as $2d * (2d + d_2)$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage

10 network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL24), d represents the inlet links of each input switch where $N_2 > N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each

15 input switch.

Each of the $\frac{N_1}{d}$ input switches IS1 – IS4 are connected to exactly $3 \times d$ switches

in middle stage 130 through $3 \times d$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and ML(1,3); and also to middle switch MS(1,2) through the links ML(1,4), ML(1,5), and ML(1,6)).

20 Each of the $\frac{N_1}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through $3 \times d$ links (for example the links ML(1,1), ML(1,2), and ML(1,3) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,13), ML(1,14), and ML(1,15) are connected to the middle switch MS(1,1) from input switch IS3) and also are connected to exactly d switches in

25 middle stage 140 through $3 \times d$ links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected from middle switch MS(1,1) to middle switch MS(2,1); and the

links ML(2,4), ML(2,5), and ML(2,6) are connected from middle switch MS(1,1) to middle switch MS(2,2)).

Similarly each of the $\frac{N_1}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through $3 \times d$ links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,13), ML(2,14), and ML(2,15) are connected to the middle switch MS(2,1) from middle switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through $3 \times d$ links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,4), ML(3,5) and ML(3,6) are connected from middle switch MS(2,1) to middle switch MS(3,2)).

Similarly each of the $\frac{N_1}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $3 \times d$ links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,13), ML(3,14), and ML(3,15) are connected to the middle switch MS(3,1) from middle switch MS(2,3)) and also are connected to exactly $\frac{2d + d_2}{3}$ output switches in output stage 120 through $2d + d_2$ links (For example the links ML(4,1), ML(4,2), and ML(4,3) are connected to output switch OS1 from Middle switch MS(3,1); the links ML(4,4), ML(4,5), and ML(4,6) are connected to output switch OS2 from middle switch MS(3,1); the links ML(4,7), ML(4,8), and ML(4,9) are connected to output switch OS3 from Middle switch MS(3,1); the links ML(4,10), ML(4,11), and ML(4,12) are connected to output switch OS2 from middle switch MS(3,1)).

Each of the $\frac{N_1}{d}$ output switches OS1 – OS4 are connected from exactly $\frac{2d + d_2}{3}$ switches in middle stage 150 through $2d + d_2$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1), ML(4,2), and

ML(4,3); output switch OS1 is also connected from middle switch MS(3,2) through the links ML(4,16), ML(4,17), and ML(4,18); output switch OS1 is connected from middle switch MS(3,3) through the links ML(4,28), ML(4,29), and ML(4,30); and output switch OS1 is also connected from middle switch MS(3,4) through the links ML(4,43),
 5 ML(4,44), and ML(4,45)).

Finally the connection topology of the network 300B1 shown in FIG. 3B1 is known to be back to back Omega connection topology.

Referring to FIG. 3C1, in one embodiment, an exemplary asymmetrical multi-link multi-stage network 300C1 with five stages of twenty switches for satisfying
 10 communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by six switches IS1-IS4 and output stage 120 consists of four, eight by six switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, six by six
 15 switches MS(1,1) - MS(1,4), middle stage 140 consists of four, six by six switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, four by eight switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by six, the
 20 switches in output stage 120 are of size eight by six, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_1}{d}$, where N_1 is the total
 25 number of inlet links or and N_2 is the total number of outlet links and $N_2 > N_1$ and $N_2 = p * N_1$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_1}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the

notation $d * 3d$ and each output switch OS1-OS4 can be denoted in general with the notation $(2d + d_2) * d_2$, where $d_2 = N_2 \times \frac{d}{N_1} = p \times d$. The size of each switch in any of the middle stages excepting the last middle stage can be denoted as $3d * 3d$. The size of each switch in the last middle stage can be denoted as $2d * (2d + d_2)$. A switch as used

5 herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example the links

10 OL1-OL24), d represents the inlet links of each input switch where $N_2 > N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the $\frac{N_1}{d}$ input switches IS1 – IS4 are connected to exactly $3 \times d$ switches in middle stage 130 through $3 \times d$ links (for example input switch IS1 is connected to

15 middle switch MS(1,1) through the links ML(1,1), ML(1,2), and ML(1,3); and also to middle switch MS(1,2) through the links ML(1,4), ML(1,5), and ML(1,6)).

Each of the $\frac{N_1}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through $3 \times d$ links (for example the links ML(1,1), ML(1,2), and ML(1,3) are connected to the middle switch MS(1,1) from input

20 switch IS1, and the links ML(1,22), ML(1,23), and ML(1,24) are connected to the middle switch MS(1,1) from input switch IS4)) and also are connected to exactly d switches in middle stage 140 through $3 \times d$ links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,4), ML(2,5), and ML(2,6) are connected from middle switch MS(1,1) to

25 middle switch MS(2,2)).

Similarly each of the $\frac{N_1}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through $3 \times d$ links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,22), ML(2,23), and ML(2,24) are connected to the middle switch MS(2,1) from middle switch MS(1,4)) and also are connected to exactly d switches in middle stage 150 through $3 \times d$ links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,4), ML(3,5), and ML(3,6) are connected from middle switch MS(2,1) to middle switch MS(3,2)).

10 Similarly each of the $\frac{N_1}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $3 \times d$ links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,22), ML(3,23), and ML(3,24) are connected to the middle switch MS(3,1) from middle switch MS(2,4)) and also are connected to exactly $\frac{2d + d_2}{3}$ output switches in output stage 120 through $2d + d_2$ links (For example the links ML(4,1), ML(4,2), and ML(4,3) are connected to output switch OS1 from Middle switch MS(3,1); the links ML(4,4), ML(4,5), and ML(4,6) are connected to output switch OS2 from middle switch MS(3,1); the links ML(4,7), ML(4,8), and ML(4,9) are connected to output switch OS3 from Middle switch MS(3,1); the links ML(4,10), ML(4,11), and ML(4,12) are connected to output switch OS2 from middle switch MS(3,1)).

Each of the $\frac{N_1}{d}$ output switches OS1 – OS4 are connected from exactly $\frac{2d + d_2}{3}$ switches in middle stage 150 through $2d + d_2$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1), ML(4,2), and ML(4,3); output switch OS1 is also connected from middle switch MS(3,2) through the links ML(4,16), ML(4,17), and ML(4,18); output switch OS1 is connected from middle switch MS(3,3) through the links ML(4,28), ML(4,29), and ML(4,30); and output switch

OS1 is also connected from middle switch MS(3,4) through the links ML(4,43), ML(4,44), and ML(4,45)).

Finally the connection topology of the network 300C1 shown in FIG. 3C1 is hereinafter called nearest neighbor connection topology.

5 Similar to network 300A1 of FIG. 3A1, 300B1 of FIG. 3B1, and 300C1 of FIG. 3C1, referring to FIG. 3D1, FIG. 3E1, FIG. 3F1, FIG. 3G1, FIG. 3H1, FIG. 3I1 and FIG. 3J1 with exemplary asymmetrical multi-link multi-stage networks 300D1, 300E1, 300F1, 300G1, 300H1, 300I1, and 300J1 respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a
10 connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by six switches IS1-IS4 and output stage 120 consists of four, six by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, six by six switches MS(1,1) - MS(1,4), middle stage 140 consists of four, six by six
15 switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, six by six switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by six, the switches in output stage 120 are of size six by two, and there are four switches in each of
20 middle stage 130, middle stage 140 and middle stage 150.

The networks 300D1, 300E1, 300F1, 300G1, 300H1, 300I1 and 300J1 of FIG. 3D1, FIG. 3E1, FIG. 3F1, FIG. 3G1, FIG. 3H1, FIG. 3I1, and FIG. 3J1 are also embodiments of asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all
25 input switches (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL24), d represents the inlet links of each input switch where $N_2 > N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Just like networks of 300A1, 300B1 and 300C1, for all the networks 300D1, 300E1, 300F1, 300G1, 300H1, 300I1 and 300J1 of FIG. 3D1, FIG. 3E1, FIG. 3F1, FIG. 3G1, FIG. 3H1, FIG. 3I1, and FIG. 3J1, each of the $\frac{N_1}{d}$ input switches IS1 – IS4 are connected to exactly d switches in middle stage 130 through $3 \times d$ links.

- 5 Each of the $\frac{N_1}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through $3 \times d$ links and also are connected to exactly d switches in middle stage 140 through $3 \times d$ links.

- 10 Similarly each of the $\frac{N_1}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through $3 \times d$ links and also are connected to exactly d switches in middle stage 150 through $3 \times d$ links.

Similarly each of the $\frac{N_1}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $3 \times d$ links and also are connected to exactly $\frac{2d + d_2}{3}$ output switches in output stage 120 through $2d + d_2$ links.

- 15 Each of the $\frac{N_1}{d}$ output switches OS1 – OS4 are connected from exactly $\frac{2d + d_2}{3}$ switches in middle stage 150 through $2d + d_2$ links.

- 20 In all the ten embodiments of FIG. 3A1 to FIG. 3J1 the connection topology is different. That is the way the links ML(1,1) - ML(1,24), ML(2,1) - ML(2,24), ML(3,1) - ML(3,24), and ML(4,1) - ML(4,48) are connected between the respective stages is different. Even though only ten embodiments are illustrated, in general, the network $V_{mlink}(N_1, N_2, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{mlink}(N_1, N_2, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the

fundamental property of a valid connection topology of the $V_{mlink}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{mlink}(N_1, N_2, d, s)$ can be built. The ten embodiments of FIG. 3A1 to FIG. 3J1 are only
 5 three examples of network $V_{mlink}(N_1, N_2, d, s)$.

In all the ten embodiments of FIG. 3A1 to FIG. 3J1, each of the links ML(1,1) – ML(1,24), ML(2,1) – ML(2,24), ML(3,1) – ML(3,24) and ML(4,1) – ML(4,48) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS1-IS4 are also referred to as the network input
 10 ports. The input stage 110 is often referred to as the first stage. The output switches OS1-OS4 are also referred to as the network output ports. The output stage 120 is often referred to as the last stage. The middle stage switches MS(1,1) – MS(1,4), MS(2,1) – MS(2,4), and MS(3,1) – MS(3,4) are referred to as middle switches or middle ports.

In the example illustrated in FIG. 3A1 (or in FIG. 3B1 to FIG. 3J1), a fan-out of
 15 four is possible to satisfy a multicast connection request if input switch is IS2, but only two switches in middle stage 130 will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS1, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage 130 when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected
 20 to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network 300A1 (or 300B1 to 300J1), to be operated in strictly nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on
 25 the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage 130 is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage 130, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the strictly

nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Asymmetric SNB ($N_2 > N_1$) Embodiments:

5 Network 300K1 of FIG. 3K1 is an example of general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2 \times \log_d N_1) - 1$ stages where $N_2 > N_1$ and $N_2 = p * N_1$ where $p > 1$. In network 300K1 of FIG. 3K1, $N_1 = N$ and $N_2 = p * N$. The general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for multicast when $s \geq 3$ according to the current
 10 invention (and in the example of FIG. 3K1, $s = 3$). The general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2 \times \log_d N_1) - 1$ stages has d inlet links for each of $\frac{N_1}{d}$ input switches IS1-IS(N_1/d) (for example the links IL1-IL(d) to the input switch IS1) and $3 \times d$ outgoing links for each of $\frac{N_1}{d}$ input switches IS1-IS(N_1/d) (for example the links ML(1,1) - ML(1,3d) to the input switch IS1). There are d_2 (where
 15 $d_2 = N_2 \times \frac{d}{N_1} = p \times d$) outlet links for each of $\frac{N_1}{d}$ output switches OS1-OS(N_1/d) (for example the links OL1-OL($p \times d$) to the output switch OS1) and $2d + d_2$ ($= 2d + p \times d$) incoming links for each of $\frac{N_1}{d}$ output switches OS1-OS(N_1/d) (for example $ML(2 \times \log_d N_1 - 2, 1) - ML(2 \times \log_d N_1 - 2, 2d + d_2)$ to the output switch OS1).

Each of the $\frac{N_1}{d}$ input switches IS1 - IS(N_1/d) are connected to exactly $3 \times d$
 20 switches in middle stage 130 through $3 \times d$ links.

Each of the $\frac{N_1}{d}$ middle switches $MS(1,1) - MS(1,N_1/d)$ in the middle stage 130 are connected from exactly d input switches through $3 \times d$ links and also are connected to exactly d switches in middle stage 140 through $3 \times d$ links.

Similarly each of the $\frac{N_1}{d}$ middle switches $MS(\text{Log}_d N_1 - 1, 1) -$

- 5 $MS(\text{Log}_d N_1 - 1, \frac{N_1}{d})$ in the middle stage $130 + 10 * (\text{Log}_d N_1 - 2)$ are connected from exactly d switches in middle stage $130 + 10 * (\text{Log}_d N_1 - 3)$ through $3 \times d$ links and also are connected to exactly d switches in middle stage $130 + 10 * (\text{Log}_d N_1 - 1)$ through $3 \times d$ links.

Similarly each of the $\frac{N_1}{d}$ middle switches $MS(2 \times \text{Log}_d N_1 - 3, 1) -$

- 10 $MS(2 \times \text{Log}_d N_1 - 3, \frac{N_1}{d})$ in the middle stage $130 + 10 * (2 * \text{Log}_d N_1 - 4)$ are connected from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N_1 - 5)$ through $3 \times d$ links and also are connected to exactly $\frac{2d + d_2}{3}$ output switches in output stage 120 through $2d + d_2$ links.

Each of the $\frac{N_1}{d}$ output switches $OS1 - OS(N_1/d)$ are connected from exactly

- 15 $\frac{2d + d_2}{3}$ switches in middle stage $130 + 10 * (2 * \text{Log}_d N_1 - 4)$ through $2d + d_2$ links.

- As described before, again the connection topology of a general $V_{mlink}(N_1, N_2, d, s)$ may be any one of the connection topologies. For example the connection topology of the network $V_{mlink}(N_1, N_2, d, s)$ may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta
20 Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general $V_{mlink}(N_1, N_2, d, s)$ network is,

when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network $V_{mlink}(N_1, N_2, d, s)$ can be built. The embodiments of FIG. 3A1 to FIG. 3J1 are ten examples of network $V_{mlink}(N_1, N_2, d, s)$ for $s = 3$ and $N_2 > N_1$.

- 5 The general symmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for multicast when $s \geq 3$ according to the current invention.

For example, the network of FIG. 3C1 shows an exemplary five-stage network, namely $V_{mlink}(8, 24, 2, 3)$, with the following multicast assignment $I_1 = \{1, 4\}$ and all other
 10 $I_j = \phi$ for $j = [2-8]$. It should be noted that the connection I_1 fans out in the first stage switch IS1 into middle switches MS(1,1) and MS(1,2) in middle stage 130, and fans out in middle switches MS(1,1) and MS(1,2) only once into middle switches MS(2,1) and MS(2,3) respectively in middle stage 140.

The connection I_1 also fans out in middle switches MS(2,1) and MS(2,3) only
 15 once into middle switches MS(3,1) and MS(3,4) respectively in middle stage 150. The connection I_1 also fans out in middle switches MS(3,1) and MS(3,4) only once into output switches OS1 and OS4 in output stage 120. Finally the connection I_1 fans out once in the output stage switch OS1 into outlet link OL2 and in the output stage switch OS4 twice into the outlet links OL19 and OL21. In accordance with the invention, each
 20 connection can fan out in the input stage switch into at most two middle stage switches in middle stage 130.

Asymmetric SNB ($N_1 > N_2$) Embodiments:

Referring to FIG. 3A2, in one embodiment, an exemplary asymmetrical multi-link multi-stage network 300A2 with five stages of twenty switches for satisfying
 25 communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, six by

eight switches IS1-IS4 and output stage 120 consists of four, six by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, eight by four switches MS(1,1) - MS(1,4), middle stage 140 consists of four, six by six switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, six by six switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage 110 are of size six by eight, the switches in output stage 120 are of size six by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_2}{d}$, where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1 > N_2$ and $N_1 = p * N_2$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_2}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d_1 * (2d + d_1)$ and each output switch OS1-OS4 can be denoted in general with the notation $3d * d$, where $d_1 = N_1 * \frac{d}{N_2} = p * d$. The size of each switch in any of the middle stages excepting the first middle stage can be denoted as $3d * 3d$. The size of each switch in the first middle stage can be denoted as $(2d + d_1) * 3d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL24), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL8), d represents the inlet links of each input switch where $N_1 > N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the $\frac{N_2}{d}$ input switches IS1 – IS4 are connected to exactly $\frac{2d + d_1}{3}$

switches in middle stage 130 through $2d + d_1$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and ML(1,3); input switch IS1 is also connected to middle switch MS(1,2) through the links ML(1,4), ML(1,5), and ML(1,6); input switch IS1 is connected to middle switch MS(1,3) through the links ML(1,7), ML(1,8), and ML(1,9); and input switch IS1 is also connected to middle switch MS(1,4) through the links ML(1,10), ML(1,11), and ML(1,12)).

Each of the $\frac{N_2}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are

connected from exactly $\frac{2d + d_1}{3}$ input switches through $2d + d_1$ links (for example

middle switch MS(1,1) is connected from input switch IS1 through the links ML(1,1), ML(1,2), and ML(1,3); middle switch MS(1,1) is connected from input switch IS2 through the links ML(1,16), ML(1,17), and ML(1,18); middle switch MS(1,1) is connected from input switch IS3 through the links ML(1,28), ML(1,29), and ML(1,30); and middle switch MS(1,1) is connected from input switch IS4 through the links ML(1,43), ML(1,44), and ML(1,45)) and also are connected to exactly d switches in middle stage 140 through $3 \times d$ links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,4), ML(2,5), and ML(2,6) are connected from middle switch MS(1,1) to middle switch MS(2,3)).

Similarly each of the $\frac{N_2}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage

140 are connected from exactly d switches in middle stage 130 through $3 \times d$ links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,16), ML(2,17), and ML(2,18) are connected to the middle switch MS(2,1) from middle switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through $3 \times d$ links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected from middle switch MS(2,1) to

middle switch MS(3,1), and the links ML(3,4), ML(3,5), and ML(3,6) are connected from middle switch MS(2,1) to middle switch MS(3,3)).

Similarly each of the $\frac{N_2}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $3 \times d$ links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,16), ML(3,17), and ML(3,18) are connected to the middle switch MS(3,1) from middle switch MS(2,3)) and also are connected to exactly d output switches in output stage 120 through $3 \times d$ links (for example the links ML(4,1), ML(4,2), and ML(4,3) are connected to output switch OS1 from Middle switch MS(3,1), and the links ML(4,10), ML(4,11), and ML(4,12) are connected to output switch OS2 from middle switch MS(3,1)).

Each of the $\frac{N_2}{d}$ output switches OS1 – OS4 are connected from exactly d switches in middle stage 150 through $3 \times d$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1), ML(4,2), and ML(4,3), and output switch OS1 is also connected from middle switch MS(3,2) through the links ML(4,10), ML(4,11) and ML(4,12)).

Finally the connection topology of the network 300A2 shown in FIG. 3A2 is known to be back to back inverse Benes connection topology.

Referring to FIG. 3B2, in one embodiment, an exemplary asymmetrical multi-link multi-stage network 300B2 with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, six by eight switches IS1-IS4 and output stage 120 consists of four, six by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, eight by four switches MS(1,1) - MS(1,4), middle stage 140 consists of four, six by six switches

MS(2,1) - MS(2,4), and middle stage 150 consists of four, six by six switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage 110 are of size six by eight, the
 5 switches in output stage 120 are of size six by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and
 10 of output stage 120 can be denoted in general with the variable $\frac{N_2}{d}$, where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1 > N_2$ and $N_1 = p * N_2$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_2}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d_1 * (2d + d_1)$ and each output switch OS1-OS4 can be denoted in general
 15 with the notation $3d * d$, where $d_1 = N_1 \times \frac{d}{N_2} = p \times d$. The size of each switch in any of the middle stages excepting the first middle stage can be denoted as $3d * 3d$. The size of each switch in the first middle stage can be denoted as $(2d + d_1) * 3d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents
 20 the total number of inlet links of all input switches (for example the links IL1-IL24), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL8), d represents the inlet links of each input switch where $N_1 > N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the $\frac{N_2}{d}$ input switches IS1 – IS4 are connected to exactly $\frac{2d + d_1}{3}$

switches in middle stage 130 through $2d + d_1$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and ML(1,3); input switch IS1 is also connected to middle switch MS(1,2) through the links ML(1,4), ML(1,5), and ML(1,6); input switch IS1 is connected to middle switch MS(1,3) through the links ML(1,7), ML(1,8), and ML(1,9); and input switch IS1 is also connected to middle switch MS(1,4) through the links ML(1,10), ML(1,11), and ML(1,12)).

Each of the $\frac{N_2}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are

connected from exactly $\frac{2d + d_1}{3}$ input switches through $2d + d_1$ links (for example

middle switch MS(1,1) is connected from input switch IS1 through the links ML(1,1), ML(1,2), and ML(1,3); middle switch MS(1,1) is connected from input switch IS2 through the links ML(1,16), ML(1,17), and ML(1,18); middle switch MS(1,1) is connected from input switch IS3 through the links ML(1,28), ML(1,29), and ML(1,30); and middle switch MS(1,1) is connected from input switch IS4 through the links ML(1,43), ML(1,44), and ML(1,45)) and also are connected to exactly d switches in middle stage 140 through $2 \times d$ links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected from middle switch MS(1,1) to middle switch MS(2,1); and the links ML(2,4), ML(2,5), and ML(2,6) are connected from middle switch MS(1,1) to middle switch MS(2,2)).

Similarly each of the $\frac{N_2}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage

140 are connected from exactly d switches in middle stage 130 through $3 \times d$ links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,13), ML(2,14), and ML(2,15) are connected to the middle switch MS(2,1) from middle switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through $3 \times d$ links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected from middle switch MS(2,1) to

middle switch MS(3,1), and the links ML(3,4), ML(3,5) and ML(3,6) are connected from middle switch MS(2,1) to middle switch MS(3,2)).

Similarly each of the $\frac{N_2}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $3 \times d$ links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,13), ML(3,14), and ML(3,15) are connected to the middle switch MS(3,1) from middle switch MS(2,3)) and also are connected to exactly d output switches in output stage 120 through $3 \times d$ links (for example the links ML(4,1), ML(4,2), and ML(4,3) are connected to output switch OS1 from Middle switch MS(3,1), and the links ML(4,4), ML(4,5), and ML(4,6) are connected to output switch OS2 from middle switch MS(3,1)).

Each of the $\frac{N_2}{d}$ output switches OS1 – OS4 are connected from exactly d switches in middle stage 150 through $3 \times d$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1), ML(4,2), and ML(4,3), and output switch OS1 is also connected from middle switch MS(3,3) through the links ML(4,13), ML(4,14), and ML(4,15)).

Finally the connection topology of the network 300B2 shown in FIG. 3B2 is known to be back to back Omega connection topology.

Referring to FIG. 3C2, in one embodiment, an exemplary asymmetrical multi-link multi-stage network 300C2 with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, six by eight switches IS1-IS4 and output stage 120 consists of four, six by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, eight by four switches MS(1,1) - MS(1,4), middle stage 140 consists of four, six by six switches

MS(2,1) - MS(2,4), and middle stage 150 consists of four, six by six switches MS(3,1) - MS(3,4).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage 110 are of size six by eight, the
 5 switches in output stage 120 are of size six by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and
 of output stage 120 can be denoted in general with the variable $\frac{N_2}{d}$, where N_1 is the
 10 total number of inlet links or and N_2 is the total number of outlet links and $N_1 > N_2$ and $N_1 = p * N_2$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_2}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d_1 * (2d + d_1)$ and each output switch OS1-OS4 can be denoted in general
 with the notation $3d * d$, where $d_1 = N_1 \times \frac{d}{N_2} = p \times d$. The size of each switch in any of
 15 the middle stages excepting the first middle stage can be denoted as $3d * 3d$. The size of each switch in the first middle stage can be denoted as $(2d + d_1) * 3d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents
 20 the total number of inlet links of all input switches (for example the links IL1-IL24), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL8), d represents the inlet links of each input switch where $N_1 > N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the $\frac{N_2}{d}$ input switches IS1 – IS4 are connected to exactly $\frac{2d + d_1}{3}$ switches in middle stage 130 through $2d + d_1$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and ML(1,3); input switch IS1 is also connected to middle switch MS(1,2) through the links ML(1,4), ML(1,5), and ML(1,6); input switch IS1 is connected to middle switch MS(1,3) through the links ML(1,7), ML(1,8), and ML(1,9); and input switch IS1 is also connected to middle switch MS(1,4) through the links ML(1,10), ML(1,11), and ML(1,12)).

Each of the $\frac{N_2}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly $\frac{2d + d_1}{3}$ input switches through $2d + d_1$ links (for example middle switch MS(1,1) is connected from input switch IS1 through the links ML(1,1), ML(1,2), and ML(1,3); middle switch MS(1,1) is connected from input switch IS2 through the links ML(1,16), ML(1,17), and ML(1,18); middle switch MS(1,1) is connected from input switch IS3 through the links ML(1,28), ML(1,29), and ML(1,30); and middle switch MS(1,1) is connected from input switch IS4 through the links ML(1,43), ML(1,44), and ML(1,45)) and also are connected to exactly d switches in middle stage 140 through $3 \times d$ links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,4), ML(2,5), and ML(2,6) are connected from middle switch MS(1,1) to middle switch MS(2,2)).

Similarly each of the $\frac{N_2}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through $3 \times d$ links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,22), ML(2,23), and ML(2,24) are connected to the middle switch MS(2,1) from middle switch MS(1,4)) and also are connected to exactly d switches in middle stage 150 through $3 \times d$ links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected from middle switch MS(2,1) to

middle switch MS(3,1), and the links ML(3,4), ML(3,5), and ML(3,6) are connected from middle switch MS(2,1) to middle switch MS(3,2)).

Similarly each of the $\frac{N_2}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $3 \times d$ links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,22), ML(3,23), and ML(3,24) are connected to the middle switch MS(3,1) from middle switch MS(2,4)) and also are connected to exactly d output switches in output stage 120 through $3 \times d$ links (for example the links ML(4,1), ML(4,2), and ML(4,3) are connected to output switch OS1 from middle switch MS(3,1), and the links ML(4,4), ML(4,5), and ML(4,6) are connected to output switch OS2 from middle switch MS(3,1)).

Each of the $\frac{N_2}{d}$ output switches OS1 – OS4 are connected from exactly d switches in middle stage 150 through $3 \times d$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1), ML(4,2), and ML(4,3), and output switch OS1 is also connected from middle switch MS(3,4) through the links ML(4,22), ML(4,23), and ML(4,24)).

Finally the connection topology of the network 300C2 shown in FIG. 3C2 is hereinafter called nearest neighbor connection topology.

Similar to network 300A2 of FIG. 3A2, 300B2 of FIG. 3B2, and 300C2 of FIG. 3C2, referring to FIG. 3D2, FIG. 3E2, FIG. 3F2, FIG. 3G2, FIG. 3H2, FIG. 3I2 and FIG. 3J2 with exemplary asymmetrical multi-link multi-stage networks 300D2, 300E2, 300F2, 300G2, 300H2, 300I2, and 300J2 respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, six by eight switches IS1-IS4 and output stage 120 consists of four, six by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four,

eight by four switches MS(1,1) - MS(1,4), middle stage 140 consists of four, six by six switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, six by six switches MS(3,1) - MS(3,4).

5 Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage 110 are of size six by eight, the switches in output stage 120 are of size six by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

10 The networks 300D2, 300E2, 300F2, 300G2, 300H2, 300I2 and 300J2 of FIG. 3D2, FIG. 3E2, FIG. 3F2, FIG. 3G2, FIG. 3H2, FIG. 3I2, and FIG. 3J2 are also embodiments of asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL24), d represents the inlet links of each input switch where $N_1 > N_2$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Just like networks of 300A2, 300B2 and 300C2, for all the networks 300D2, 300E2, 300F2, 300G2, 300H2, 300I2 and 300J2 of FIG. 3D2, FIG. 3E2, FIG. 3F2, FIG. 3G2, FIG. 3H2, FIG. 3I2, and FIG. 3J2, each of the $\frac{N_2}{d}$ input switches IS1 - IS4 are connected to exactly $\frac{2d + d_1}{3}$ switches in middle stage 130 through $2d + d_2$ links.

20 Each of the $\frac{N_2}{d}$ middle switches MS(1,1) - MS(1,4) in the middle stage 130 are connected from exactly $\frac{2d + d_1}{3}$ input switches through $2d + d_2$ links and also are connected to exactly d switches in middle stage 140 through $3 \times d$ links.

Similarly each of the $\frac{N_2}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through $3 \times d$ links and also are connected to exactly d switches in middle stage 150 through $3 \times d$ links.

5 Similarly each of the $\frac{N_2}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through $3 \times d$ links and also are connected to exactly d output switches in output stage 120 through $3 \times d$ links.

Each of the $\frac{N_2}{d}$ output switches OS1 – OS4 are connected from exactly d switches in middle stage 150 through $3 \times d$ links.

In all the ten embodiments of FIG. 3A2 to FIG. 3J2 the connection topology is
 10 different. That is the way the links ML(1,1) - ML(1,48), ML(2,1) - ML(2,24), ML(3,1) - ML(3,24), and ML(4,1) - ML(4,24) are connected between the respective stages is different. Even though only ten embodiments are illustrated, in general, the network $V_{mlink}(N_1, N_2, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{mlink}(N_1, N_2, d, s)$ may be back to back Benes
 15 networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{mlink}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{mlink}(N_1, N_2, d, s)$ can be built. The ten embodiments of FIG. 3A2 to FIG. 3J2 are only
 20 three examples of network $V_{mlink}(N_1, N_2, d, s)$.

In all the ten embodiments of FIG. 3A2 to FIG. 3J2, each of the links ML(1,1) – ML(1,48), ML(2,1) – ML(2,24), ML(3,1) – ML(3,24) and ML(4,1) – ML(4,24) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS1-IS4 are also referred to as the network input
 25 ports. The input stage 110 is often referred to as the first stage. The output switches

OS1-OS4 are also referred to as the network output ports. The output stage 120 is often referred to as the last stage. The middle stage switches MS(1,1) – MS(1,4), MS(2,1) – MS(2,4), and MS(3,1) – MS(3,4) are referred to as middle switches or middle ports.

In the example illustrated in FIG. 3A2 (or in FIG. 3B2 to FIG. 3J2), a fan-out of four is possible to satisfy a multicast connection request if input switch is IS2, but only two switches in middle stage 130 will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS1, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage 130 when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network 300A2 (or 300B2 to 300J2), to be operated in strictly nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage 130 is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage 130, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the strictly nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Asymmetric SNB ($N_2 > N_1$) Embodiments:

Network 3001K2 of FIG. 3K2 is an example of general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2 \times \log_d N_2) - 1$ stages where $N_1 > N_2$ and $N_1 = p * N_2$ where $p > 1$. In network 300K2 of FIG. 3K2, $N_2 = N$ and $N_1 = p * N$. The general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for multicast when $s = 3$ according to the current invention (and in the example of FIG. 3K2, $s = 3$). The general asymmetrical multi-link

multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2 \times \log_d N_2) - 1$ stages has d_1 (where $d_1 = N_1 \times \frac{d}{N_2} = p \times d$) inlet links for each of $\frac{N_2}{d}$ input switches IS1-IS(N_2/d) (for example the links IL1-IL($p \times d$) to the input switch IS1) and $2d + d_1 (= 2d + p \times d)$ outgoing links for each of $\frac{N_2}{d}$ input switches IS1-IS(N_2/d) (for example the links ML(1,1) - ML(1,($d+p \times d$)) to the input switch IS1). There are d outlet links for each of $\frac{N_2}{d}$ output switches OS1-OS(N_2/d) (for example the links OL1-OL(d) to the output switch OS1) and $2 \times d$ incoming links for each of $\frac{N_2}{d}$ output switches OS1-OS(N_2/d) (for example ML($2 \times \log_d N_2 - 2, 1$) - ML($2 \times \log_d N_2 - 2, 3 \times d$) to the output switch OS1).

10 Each of the $\frac{N_2}{d}$ input switches IS1 - IS(N_2/d) are connected to exactly $\frac{2d + d_1}{3}$ switches in middle stage 130 through $2d + d_2$ links.

Each of the $\frac{N_2}{d}$ middle switches MS(1,1) - MS(1, N_2/d) in the middle stage 130 are connected from exactly d input switches through $3 \times d$ links and also are connected to exactly d switches in middle stage 140 through $3 \times d$ links.

15 Similarly each of the $\frac{N_2}{d}$ middle switches MS($\log_d N_2 - 1, 1$) - MS($\log_d N_2 - 1, \frac{N_2}{d}$) in the middle stage $130 + 10 * (\log_d N_2 - 2)$ are connected from exactly d switches in middle stage $130 + 10 * (\log_d N_2 - 3)$ through $3 \times d$ links and also are connected to exactly d switches in middle stage $130 + 10 * (\log_d N_2 - 1)$ through $3 \times d$ links.

Similarly each of the $\frac{N_2}{d}$ middle switches $MS(2 \times \text{Log}_d N_2 - 3, 1)$ -
 $MS(2 \times \text{Log}_d N_2 - 3, \frac{N_2}{d})$ in the middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 4)$ are connected
 from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 5)$ through $3 \times d$ links
 and also are connected to exactly d output switches in output stage 120 through $3 \times d$
 5 links.

Each of the $\frac{N_2}{d}$ output switches OS1 – OS(N_2/d) are connected from exactly d
 switches in middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 4)$ through $2 \times d$ links.

As described before, again the connection topology of a general
 $V_{mlink}(N_1, N_2, d, s)$ may be any one of the connection topologies. For example the
 10 connection topology of the network $V_{mlink}(N_1, N_2, d, s)$ may be back to back inverse
 Benes networks, back to back Omega networks, back to back Benes networks, Delta
 Networks and many more combinations. The applicant notes that the fundamental
 property of a valid connection topology of the general $V_{mlink}(N_1, N_2, d, s)$ network is,
 when no connections are setup from any input link if any output link should be reachable.
 15 Based on this property numerous embodiments of the network $V_{mlink}(N_1, N_2, d, s)$ can be
 built. The embodiments of FIG. 3A2 to FIG. 3J2 are ten examples of network
 $V_{mlink}(N_1, N_2, d, s)$ for $s = 3$ and $N_2 > N_1$.

The general symmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can
 be operated in strictly nonblocking manner for multicast when $s \geq 3$ according to the
 20 current invention.

For example, the network of Fig. 3C2 shows an exemplary five-stage network,
 namely $V_{mlink}(8, 24, 2, 3)$, with the following multicast assignment $I_1 = \{1, 4\}$ and all other
 $I_j = \phi$ for $j = [2-8]$. It should be noted that the connection I_1 fans out in the first stage
 switch IS1 into middle switches MS(1,1) and MS(1,4) in middle stage 130, and fans out

in middle switches MS(1,1) and MS(1,4) only once into middle switches MS(2,1) and MS(2,4) respectively in middle stage 140.

The connection I_1 also fans out in middle switches MS(2,1) and MS(2,4) only once into middle switches MS(3,1) and MS(3,4) respectively in middle stage 150. The connection I_1 also fans out in middle switches MS(3,1) and MS(3,4) only once into output switches OS1 and OS4 in output stage 120. Finally the connection I_1 fans out once in the output stage switch OS1 into outlet link OL1 and in the output stage switch OS4 twice into the outlet links OL7 and OL8. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage 130.

Folded Strictly Nonblocking multi-link multi-stage Networks:

The folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, s)$, disclosed in the current invention, is topologically exactly the same as the multi-stage network $V_{link}(N_1, N_2, d, s)$, disclosed in U.S. Provisional Patent Application Docket No. M-0037US that is incorporated by reference above, excepting that in the illustrations folded network $V_{fold-link}(N_1, N_2, d, s)$ is shown as it is folded at middle stage $130 + 10 * (\text{Log}_d N_2 - 2)$.

The general symmetrical folded multi-link multi-stage network $V_{fold-link}(N, d, s)$ can also be operated in strictly nonblocking manner for multicast when $s \geq 3$ according to the current invention. Similarly the general asymmetrical folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ can also be operated in strictly nonblocking manner for multicast when $s \geq 3$ according to the current invention.

25

FOLDED MULTI-STAGE NETWORK EMBODIMENTS:

Symmetric folded RNB Embodiments:

Referring to FIG. 4A, in one embodiment, an exemplary symmetrical folded multi-stage network 400A with five stages of thirty two switches for satisfying

5 communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by four switches IS1-IS4 and output stage 120 consists of four, four by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of eight, two by two

10 switches MS(1,1) - MS(1,8), middle stage 140 consists of eight, two by two switches MS(2,1) - MS(2,8), and middle stage 150 consists of eight, two by two switches MS(3,1) - MS(3,8).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the

15 switches in output stage 120 are of size four by two, and there are eight switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are eight switches in each of middle stage 130, middle

20 stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N}{d}$, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage

25 is denoted by $2 \times \frac{N}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the notation $2d * d$. Likewise, the size of each switch in any of the middle stages can be denoted as $d * d$. A switch as used herein can be either a crossbar switch, or a network

of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric folded multi-stage network can be represented with the notation $V_{fold}(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL1-IL8), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL1-IL8 as there are outlet links OL1-OL8, in a symmetrical network they are the same.

Each of the $\frac{N}{d}$ input switches IS1 – IS4 are connected to exactly $2 \times d$ switches in middle stage 130 through $2 \times d$ links (for example input switch IS1 is connected to middle switches MS(1,1), MS(1,2), MS(1,5) and MS(1,6) through the links ML(1,1), ML(1,2), ML(1,3) and ML(1,4) respectively).

Each of the $2 \times \frac{N}{d}$ middle switches MS(1,1) – MS(1,8) in the middle stage 130 are connected from exactly d input switches through d links (for example the links ML(1,1) and ML(1,5) are connected to the middle switch MS(1,1) from input switch IS1 and IS2 respectively) and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,3) respectively).

Similarly each of the $2 \times \frac{N}{d}$ middle switches MS(2,1) – MS(2,8) in the middle stage 140 are connected from exactly d switches in middle stage 130 through d links (for example the links ML(2,1) and ML(2,6) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,3) respectively) and also are connected to exactly d switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and MS(3,3) respectively).

Similarly each of the $2 \times \frac{N}{d}$ middle switches MS(3,1) – MS(3,8) in the middle stage 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,6) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,3) respectively) and also are connected to
 5 exactly d output switches in output stage 120 through d links (for example the links ML(4,1) and ML(4,2) are connected to output switches OS1 and OS2 respectively from middle switches MS(3,1)).

Each of the $\frac{N}{d}$ output switches OS1 – OS4 are connected from exactly $2 \times d$ switches in middle stage 150 through $2 \times d$ links (for example output switch OS1 is
 10 connected from middle switches MS(3,1), MS(3,2), MS(3,5) and MS(3,6) through the links ML(4,1), ML(4,3), ML(4,9) and ML(4,11) respectively).

Finally the connection topology of the network 400A shown in FIG. 4A is known to be back to back inverse Benes connection topology.

Referring to FIG. 4A1, in another embodiment of network $V_{fold}(N, d, s)$, an
 15 exemplary symmetrical folded multi-stage network 400A1 with five stages of thirty two switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by four switches IS1-IS4 and output stage 120 consists of four, four
 20 by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of eight, two by two switches MS(1,1) - MS(1,8), middle stage 140 consists of eight, two by two switches MS(2,1) - MS(2,8), and middle stage 150 consists of eight, two by two switches MS(3,1) - MS(3,8).

Such a network can be operated in strictly non-blocking manner for unicast
 25 connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are eight switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be

operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are eight switches in each of middle stage 130, middle stage 140 and middle stage 150.

- 5 In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N}{d}$, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by $2 \times \frac{N}{d}$. The size of each input switch IS1-IS4 can be denoted in general
- 10 with the notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the notation $2d * d$. Likewise, the size of each switch in any of the middle stages can be denoted as $d * d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The symmetric folded multi-stage network of FIG. 4A1 is also the network of the type
- 15 $V_{fold}(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL1-IL8), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL1-IL8 as there are outlet links OL1-OL8, in a
- 20 symmetrical network they are the same.

Each of the $\frac{N}{d}$ input switches IS1 – IS4 are connected to exactly $2 \times d$ switches in middle stage 130 through $2 \times d$ links (for example input switch IS1 is connected to middle switches MS(1,1), MS(1,2), MS(1,5) and MS(1,6) through the links ML(1,1), ML(1,2), ML(1,3) and ML(1,4) respectively).

- 25 Each of the $2 \times \frac{N}{d}$ middle switches MS(1,1) – MS(1,8) in the middle stage 130 are connected from exactly d input switches through d links (for example the links

ML(1,1) and ML(1,9) are connected to the middle switch MS(1,1) from input switch IS1 and IS3 respectively) and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,2) respectively).

5 Similarly each of the $2 \times \frac{N}{d}$ middle switches MS(2,1) – MS(2,8) in the middle stage 140 are connected from exactly d switches in middle stage 130 through d links (for example the links ML(2,1) and ML(2,5) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,3) respectively) and also are connected to exactly d switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and MS(3,2) respectively).

 Similarly each of the $2 \times \frac{N}{d}$ middle switches MS(3,1) – MS(3,8) in the middle stage 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,5) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,3) respectively) and also are connected to exactly d output switches in output stage 120 through d links (for example the links ML(4,1) and ML(4,2) are connected to output switches OS1 and OS2 respectively from middle switches MS(3,1)).

 Each of the $\frac{N}{d}$ output switches OS1 – OS4 are connected from exactly $2 \times d$ switches in middle stage 150 through $2 \times d$ links (for example output switch OS1 is connected from middle switches MS(3,1), MS(3,3), MS(3,5) and MS(3,7) through the links ML(4,1), ML(4,5), ML(4,9) and ML(4,13) respectively).

 Finally the connection topology of the network 400A1 shown in FIG. 4A1 is known to be back to back Omega connection topology.

25 Referring to FIG. 4A2, in another embodiment of network $V_{fold}(N, d, s)$, an exemplary symmetrical folded multi-stage network 400A2 with five stages of thirty two

switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by four switches IS1-IS4 and output stage 120 consists of four, four by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of eight, two by two switches MS(1,1) - MS(1,8), middle stage 140 consists of eight, two by two switches MS(2,1) - MS(2,8), and middle stage 150 consists of eight, two by two switches MS(3,1) - MS(3,8).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are eight switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are eight switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N}{d}$, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by $2 \times \frac{N}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the notation $2d * d$. Likewise, the size of each switch in any of the middle stages can be denoted as $d * d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The symmetric folded multi-stage network of FIG. 4A2 is also the network of the type $V_{fold}(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL1-IL8), d represents the inlet links of each input switch or outlet

links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL1-IL8 as there are outlet links OL1-OL8, in a symmetrical network they are the same.

- 5 Each of the $\frac{N}{d}$ input switches IS1 – IS4 are connected to exactly $2 \times d$ switches in middle stage 130 through $2 \times d$ links (for example input switch IS1 is connected to middle switches MS(1,1), MS(1,2), MS(1,5) and MS(1,6) through the links ML(1,1), ML(1,2), ML(1,3) and ML(1,4) respectively).

- 10 Each of the $2 \times \frac{N}{d}$ middle switches MS(1,1) – MS(1,8) in the middle stage 130 are connected from exactly d input switches through d links (for example the links ML(1,1) and ML(1,14) are connected to the middle switch MS(1,1) from input switch IS1 and IS4 respectively) and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,2) respectively).

- 15 Similarly each of the $2 \times \frac{N}{d}$ middle switches MS(2,1) – MS(2,8) in the middle stage 140 are connected from exactly d switches in middle stage 130 through d links (for example the links ML(2,1) and ML(2,8) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,4) respectively) and also are connected to exactly d switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and MS(3,2) respectively).
- 20

- 25 Similarly each of the $2 \times \frac{N}{d}$ middle switches MS(3,1) – MS(3,8) in the middle stage 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,8) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,4) respectively) and also are connected to exactly d output switches in output stage 120 through d links (for example the links

ML(4,1) and ML(4,2) are connected to output switches OS1 and OS2 respectively from middle switches MS(3,1)).

Each of the $\frac{N}{d}$ output switches OS1 – OS4 are connected from exactly $2 \times d$ switches in middle stage 150 through $2 \times d$ links (for example output switch OS1 is
 5 connected from middle switches MS(3,1), MS(3,4), MS(3,5) and MS(3,8) through the links ML(4,1), ML(4,2), ML(4,3) and ML(4,4) respectively).

Finally the connection topology of the network 400A2 shown in FIG. 4A2 is hereinafter called nearest neighbor connection topology.

In the three embodiments of FIG. 4A, FIG. 4A1 and FIG. 4A2 the connection
 10 topology is different. That is the way the links ML(1,1) - ML(1,16), ML(2,1) - ML(2,16), ML(3,1) - ML(3,16), and ML(4,1) - ML(4,16) are connected between the respective stages is different. Even though only three embodiments are illustrated, in general, the network $V_{fold}(N, d, s)$ can comprise any arbitrary type of connection topology. For
 15 example the connection topology of the network $V_{fold}(N, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{fold}(N, d, s)$ network is, when no connections are setup from any input link all the output links should be
 20 reachable. Based on this property numerous embodiments of the network $V_{fold}(N, d, s)$ can be built. The embodiments of FIG. 4A, FIG. 4A1, and FIG. 4A2 are only three examples of network $V_{fold}(N, d, s)$.

In the three embodiments of FIG. 4A, FIG. 4A1 and FIG. 4A2, each of the links ML(1,1) – ML(1,16), ML(2,1) – ML(2,16), ML(3,1) – ML(3,16) and ML(4,1) –
 ML(4,16) are either available for use by a new connection or not available if currently
 25 used by an existing connection. The input switches IS1-IS4 are also referred to as the network input ports. The input stage 110 is often referred to as the first stage. The output switches OS1-OS4 are also referred to as the network output ports. The output stage 120 is often referred to as the last stage. The middle stage switches MS(1,1) – MS(1,8),

MS(2,1) – MS(2,8), and MS(3,1) – MS(3,8) are referred to as middle switches or middle ports.

In the example illustrated in FIG. 4A (or in FIG1A1, or in FIG. 4A2), a fan-out of four is possible to satisfy a multicast connection request if input switch is IS2, but only two switches in middle stage 130 will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS1, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage 130 when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network 400A (or 400A1, or 400A2), to be operated in rearrangeably nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage 130 is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage 130, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the rearrangeably nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Symmetric folded RNB Embodiments:

Network 400B of FIG. 4B is an example of general symmetrical folded multi-stage network $V_{fold}(N, d, s)$ with $(2 \times \log_d N) - 1$ stages. The general symmetrical folded multi-stage network $V_{fold}(N, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s \geq 2$ according to the current invention. Also the general symmetrical folded multi-stage network $V_{fold}(N, d, s)$ can be operated in strictly

nonblocking manner for unicast if $s \geq 2$ according to the current invention. (And in the example of FIG. 4B, $s = 2$). The general symmetrical folded multi-stage network

$V_{fold}(N, d, s)$ with $(2 \times \log_d N) - 1$ stages has d inlet links for each of $\frac{N}{d}$ input switches

IS1-IS(N/d) (for example the links IL1-IL(d) to the input switch IS1) and $2 \times d$ outgoing
 5 links for each of $\frac{N}{d}$ input switches IS1-IS(N/d) (for example the links ML(1,1) -

ML(1,2d) to the input switch IS1). There are d outlet links for each of $\frac{N}{d}$ output

switches OS1-OS(N/d) (for example the links OL1-OL(d) to the output switch OS1) and

$2 \times d$ incoming links for each of $\frac{N}{d}$ output switches OS1-OS(N/d) (for

example $ML(2 \times \log_d N - 2, 1) - ML(2 \times \log_d N - 2, 2 \times d)$ to the output switch OS1).

10 Each of the $\frac{N}{d}$ input switches IS1 - IS(N/d) are connected to exactly $2 \times d$

switches in middle stage 130 through $2 \times d$ links (for example input switch IS1 is

connected to middle switches MS(1,1) - MS(1,d) through the links ML(1,1) - ML(1,d)

and to middle switches MS(1,N/d+1) - MS(1,{N/d}+d) through the links ML(1,d+1) -

ML(1,2d) respectively.

15 Each of the $2 \times \frac{N}{d}$ middle switches MS(1,1) - MS(1,2N/d) in the middle stage

130 are connected from exactly d input switches through d links and also are connected
 to exactly d switches in middle stage 140 through d links.

Similarly each of the $2 \times \frac{N}{d}$ middle switches $MS(\log_d N - 1, 1) -$

$MS(\log_d N - 1, 2 \times \frac{N}{d})$ in the middle stage $130 + 10 * (\log_d N - 2)$ are connected from

20 exactly d switches in middle stage $130 + 10 * (\log_d N - 3)$ through d links and also are
 connected to exactly d switches in middle stage $130 + 10 * (\log_d N - 1)$ through d links.

Similarly each of the $2 \times \frac{N}{d}$ middle switches $MS(2 \times \log_d N - 3, 1)$ -

$MS(2 \times \log_d N - 3, 2 \times \frac{N}{d})$ in the middle stage $130 + 10 * (2 * \log_d N - 4)$ are connected from exactly d switches in middle stage $130 + 10 * (2 * \log_d N - 5)$ through d links and also are connected to exactly d output switches in output stage 120 through d links.

- 5 Each of the $\frac{N}{d}$ output switches OS1 – OS(N/d) are connected from exactly $2 \times d$ switches in middle stage $130 + 10 * (2 * \log_d N - 4)$ through $2 \times d$ links.

As described before, again the connection topology of a general $V_{fold}(N, d, s)$ may be any one of the connection topologies. For example the connection topology of the network $V_{fold}(N, d, s)$ may be back to back inverse Benes networks, back to back Omega
 10 networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general $V_{fold}(N, d, s)$ network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network $V_{fold}(N, d, s)$ can be built. The embodiments of FIG. 4A, FIG. 4A1, and
 15 FIG. 4A2 are three examples of network $V_{fold}(N, d, s)$.

The general symmetrical folded multi-stage network $V_{fold}(N, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s \geq 2$ according to the current invention. Also the general symmetrical folded multi-stage network $V_{fold}(N, d, s)$ can be operated in strictly nonblocking manner for unicast if $s \geq 2$ according to the
 20 current invention.

Every switch in the folded multi-stage networks discussed herein has multicast capability. In a $V_{fold}(N, d, s)$ network, if a network inlet link is to be connected to more than one outlet link on the same output switch, then it is only necessary for the corresponding input switch to have one path to that output switch. This follows because

that path can be multicast within the output switch to as many outlet links as necessary. Multicast assignments can therefore be described in terms of connections between input switches and output switches. An existing connection or a new connection from an input switch to r' output switches is said to have fan-out r' . If all multicast assignments of a first type, wherein any inlet link of an input switch is to be connected in an output switch to at most one outlet link are realizable, then multicast assignments of a second type, wherein any inlet link of each input switch is to be connected to more than one outlet link in the same output switch, can also be realized. For this reason, the following discussion is limited to general multicast connections of the first type (with fan-out r' , $1 \leq r' \leq \frac{N}{d}$) although the same discussion is applicable to the second type.

To characterize a multicast assignment, for each inlet link $i \in \left\{1, 2, \dots, \frac{N}{d}\right\}$, let

$I_i = O$, where $O \subset \left\{1, 2, \dots, \frac{N}{d}\right\}$, denote the subset of output switches to which inlet link i

is to be connected in the multicast assignment. For example, the network of FIG. 4A shows an exemplary five-stage network, namely $V_{fold}(8, 2, 2)$, with the following multicast assignment $I_1 = \{2, 3\}$ and all other $I_j = \emptyset$ for $j = [2-8]$. It should be noted that the connection I_1 fans out in the first stage switch IS1 into middle switches MS(1,1) and MS(1,5) in middle stage 130, and fans out in middle switches MS(1,1) and MS(1,5) only once into middle switches MS(2,1) and MS(2,5) respectively in middle stage 140.

The connection I_1 also fans out in middle switches MS(2,1) and MS(2,5) only once into middle switches MS(3,1) and MS(3,7) respectively in middle stage 150. The connection I_1 also fans out in middle switches MS(3,1) and MS(3,7) only once into output switches OS2 and OS3 in output stage 120. Finally the connection I_1 fans out once in the output stage switch OS2 into outlet link OL3 and in the output stage switch OS3 twice into the outlet links OL5 and OL6. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage 130.

Asymmetric folded RNB ($N_2 > N_1$) Embodiments:

Referring to FIG. 4C, in one embodiment, an exemplary asymmetrical folded multi-stage network 400C with five stages of thirty two switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection
 5 between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by four switches IS1-IS4 and output stage 120 consists of four, eight by six switches OS1-OS4. And all the middle stages namely middle stage 130 consists of eight, two by two switches MS(1,1) - MS(1,8), middle stage 140 consists of eight, two by two switches
 10 MS(2,1) - MS(2,8), and middle stage 150 consists of eight, two by four switches MS(3,1) - MS(3,8).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size eight by six, and there are eight switches in each
 15 of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size eight by six, and there are eight switches of size two by two in each of middle stage 130 and middle stage 140, and eight switches of size two by four in middle stage
 20 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_1}{d}$, where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_2 > N_1$ and
 25 $N_2 = p * N_1$ where $p > 1$. The number of middle switches in each middle stage is denoted by $2 * \frac{N_1}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the

notation $(d + d_2) * d$, where $d_2 = N_2 \times \frac{d}{N_1} = p \times d$. The size of each switch in any of the middle stages excepting the last middle stage can be denoted as $d * d$. The size of each switch in the last middle stage can be denoted as $d * \frac{(d + d_2)}{2}$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric folded multi-stage network can be represented with the notation $V_{fold}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL24), d represents the inlet links of each input switch where $N_2 > N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the $\frac{N_1}{d}$ input switches IS1 – IS4 are connected to exactly $2 \times d$ switches in middle stage 130 through $2 \times d$ links (for example input switch IS1 is connected to middle switches MS(1,1), MS(1,2), MS(1,5) and MS(1,6) through the links ML(1,1), ML(1,2), ML(1,3) and ML(1,4) respectively).

Each of the $2 \times \frac{N_1}{d}$ middle switches MS(1,1) – MS(1,8) in the middle stage 130 are connected from exactly d input switches through d links (for example the links ML(1,1) and ML(1,5) are connected to the middle switch MS(1,1) from input switch IS1 and IS2 respectively) and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,3) respectively).

Similarly each of the $2 \times \frac{N_1}{d}$ middle switches MS(2,1) – MS(2,8) in the middle stage 140 are connected from exactly d switches in middle stage 130 through d links (for example the links ML(2,1) and ML(2,6) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,3) respectively) and also are connected to

exactly d switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and MS(3,3) respectively).

Similarly each of the $2 \times \frac{N_1}{d}$ middle switches MS(3,1) – MS(3,8) in the middle
 5 stage 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,6) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,3) respectively) and also are connected to exactly $\frac{d + d_2}{2}$ output switches in output stage 120 through $\frac{d + d_2}{2}$ links (for example the links ML(4,1), ML(4,2), ML(4,3) and ML(4,4) are connected to output switches OS1,
 10 OS2, OS3, and OS4 respectively from middle switches MS(3,1)).

Each of the $\frac{N_1}{d}$ output switches OS1 – OS4 are connected from exactly $d + d_2$ switches in middle stage 150 through $d + d_2$ links (for example output switch OS1 is connected from middle switches MS(3,1), MS(3,2), MS(3,3), MS(3,4), MS(3,5), MS(3,6), MS(3,7), and MS(3,8) through the links ML(4,1), ML(4,5), ML(4,9), ML(4,13),
 15 ML(4,17), ML(4,21), ML(4,25) and ML(4,29) respectively).

Finally the connection topology of the network 400C shown in FIG. 4C is known to be back to back inverse Benes connection topology.

Referring to FIG. 4C1, in another embodiment of network $V_{fold}(N_1, N_2, d, s)$, an exemplary asymmetrical folded multi-stage network 400C1 with five stages of thirty two
 20 switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by four switches IS1-IS4 and output stage 120 consists of four, eight by six switches OS1-OS4. And all the middle stages namely middle stage 130 consists of
 25 eight, two by two switches MS(1,1) - MS(1,8), middle stage 140 consists of eight, two by

two switches MS(2,1) - MS(2,8), and middle stage 150 consists of eight, two by four switches MS(3,1) - MS(3,8).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size eight by six, and there are eight switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size eight by six, and there are eight switches of size two by two in each of middle stage 130 and middle stage 140, and eight switches of size two by four in middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_1}{d}$, where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_2 > N_1$ and $N_2 = p * N_1$ where $p > 1$. The number of middle switches in each middle stage is denoted by $2 * \frac{N_1}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the notation $(d + d_2) * d$, where $d_2 = N_2 * \frac{d}{N_1} = p * d$. The size of each switch in any of the middle stages excepting the last middle stage can be denoted as $d * d$. The size of each switch in the last middle stage can be denoted as $d * \frac{(d + d_2)}{2}$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The asymmetric folded multi-stage network of FIG. 4C1 is also the network of the type $V_{fold}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example

the links OL1-OL24), d represents the inlet links of each input switch where $N_2 > N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the $\frac{N_1}{d}$ input switches IS1 – IS4 are connected to exactly $2 \times d$ switches
 5 in middle stage 130 through $2 \times d$ links (for example input switch IS1 is connected to middle switches MS(1,1), MS(1,2), MS(1,5) and MS(1,6) through the links ML(1,1), ML(1,2), ML(1,3) and ML(1,4) respectively).

Each of the $2 \times \frac{N_1}{d}$ middle switches MS(1,1) – MS(1,8) in the middle stage 130
 10 are connected from exactly d input switches through d links (for example the links ML(1,1) and ML(1,9) are connected to the middle switch MS(1,1) from input switch IS1 and IS3 respectively) and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,2) respectively).

Similarly each of the $2 \times \frac{N_1}{d}$ middle switches MS(2,1) – MS(2,8) in the middle
 15 stage 140 are connected from exactly d switches in middle stage 130 through d links (for example the links ML(2,1) and ML(2,5) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,3) respectively) and also are connected to exactly d switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and
 20 MS(3,2) respectively).

Similarly each of the $2 \times \frac{N_1}{d}$ middle switches MS(3,1) – MS(3,8) in the middle
 stage 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,5) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,3) respectively) and also are connected to
 25 exactly $\frac{d + d_2}{2}$ output switches in output stage 120 through $\frac{d + d_2}{2}$ links (for example

the links ML(4,1), ML(4,2), ML(4,3) and ML(4,4) are connected to output switches OS1, OS2, OS3, and OS4 respectively from middle switches MS(3,1)).

Each of the $\frac{N_1}{d}$ output switches OS1 – OS4 are connected from exactly $d + d_2$ switches in middle stage 150 through $d + d_2$ links (for example output switch OS1 is
 5 connected from middle switches MS(3,1), MS(3,2), MS(3,3), MS(3,4), MS(3,5), MS(3,6), MS(3,7), and MS(3,8) through the links ML(4,1), ML(4,5), ML(4,9), ML(4,13), ML(4,17), ML(4,21), ML(4,25) and ML(4,29) respectively).

Finally the connection topology of the network 400C1 shown in FIG. 4C1 is known to be back to back Omega connection topology.

10 Referring to FIG. 4C2, in another embodiment of network $V_{fold}(N_1, N_2, d, s)$, an exemplary asymmetrical folded multi-stage network 400C2 with five stages of thirty two switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110
 15 consists of four, two by four switches IS1-IS4 and output stage 120 consists of four, eight by six switches OS1-OS4. And all the middle stages namely middle stage 130 consists of eight, two by two switches MS(1,1) - MS(1,8), middle stage 140 consists of eight, two by two switches MS(2,1) - MS(2,8), and middle stage 150 consists of eight, two by four switches MS(3,1) - MS(3,8).

20 Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size eight by six, and there are eight switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the
 25 switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size eight by six, and there are eight switches of size two by two in each of middle stage 130 and middle stage 140, and eight switches of size two by four in middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_1}{d}$, where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_2 > N_1$ and

5 $N_2 = p * N_1$ where $p > 1$. The number of middle switches in each middle stage is denoted by $2 * \frac{N_1}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the notation $(d + d_2) * d$, where $d_2 = N_2 * \frac{d}{N_1} = p * d$. The size of each switch in any of the middle stages excepting the last middle stage can be denoted as $d * d$. The size of

10 each switch in the last middle stage can be denoted as $d * \frac{(d + d_2)}{2}$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The asymmetric folded multi-stage network of FIG. 4C2 is also the network of the type $V_{fold}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL24), d represents the inlet links of each input switch where $N_2 > N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the $\frac{N_1}{d}$ input switches IS1 – IS4 are connected to exactly $2 * d$ switches

20 in middle stage 130 through $2 * d$ links (for example input switch IS1 is connected to middle switches MS(1,1), MS(1,2), MS(1,5) and MS(1,6) through the links ML(1,1), ML(1,2), ML(1,3) and ML(1,4) respectively).

Each of the $2 * \frac{N_1}{d}$ middle switches MS(1,1) – MS(1,8) in the middle stage 130 are connected from exactly d input switches through d links (for example the links

ML(1,1) and ML(1,14) are connected to the middle switch MS(1,1) from input switch IS1 and IS4 respectively) and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,2) respectively).

- 5 Similarly each of the $2 \times \frac{N_1}{d}$ middle switches MS(2,1) – MS(2,8) in the middle stage 140 are connected from exactly d switches in middle stage 130 through d links (for example the links ML(2,1) and ML(2,8) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,4) respectively) and also are connected to exactly d switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and MS(3,2) respectively).
- 10

- Similarly each of the $2 \times \frac{N_1}{d}$ middle switches MS(3,1) – MS(3,8) in the middle stage 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,8) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,4) respectively) and also are connected to exactly $\frac{d + d_2}{2}$ output switches in output stage 120 through $\frac{d + d_2}{2}$ links (for example the links ML(4,1), ML(4,2), ML(4,3) and ML(4,4) are connected to output switches OS1, OS2, OS3, and OS4 respectively from middle switches MS(3,1)).
- 15

- Each of the $\frac{N_1}{d}$ output switches OS1 – OS4 are connected from exactly $d + d_2$ switches in middle stage 150 through $d + d_2$ links (for example output switch OS1 is connected from middle switches MS(3,1), MS(3,2), MS(3,3), MS(3,4), MS(3,5), MS(3,6), MS(3,7), and MS(3,8) through the links ML(4,1), ML(4,5), ML(4,9), ML(4,13), ML(4,17), ML(4,21), ML(4,25) and ML(4,29) respectively).
- 20

- Finally the connection topology of the network 400C2 shown in FIG. 4C2 is hereinafter called nearest neighbor connection topology.
- 25

In the three embodiments of FIG. 4C, FIG. 4C1 and FIG. 4C2 the connection topology is different. That is the way the links ML(1,1) - ML(1,16), ML(2,1) - ML(2,16), ML(3,1) - ML(3,16), and ML(4,1) - ML(4,16) are connected between the respective stages is different. Even though only three embodiments are illustrated, in general, the network $V_{fold}(N_1, N_2, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{fold}(N_1, N_2, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{fold}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{fold}(N_1, N_2, d, s)$ can be built. The embodiments of FIG. 4C, FIG. 4C1, and FIG. 4C2 are only three examples of network $V_{fold}(N_1, N_2, d, s)$.

In the three embodiments of FIG. 4C, FIG. 4C1 and FIG. 4C2, each of the links ML(1,1) – ML(1,32), ML(2,1) – ML(2,16), ML(3,1) – ML(3,16) and ML(4,1) – ML(4,16) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS1-IS4 are also referred to as the network input ports. The input stage 110 is often referred to as the first stage. The output switches OS1-OS4 are also referred to as the network output ports. The output stage 120 is often referred to as the last stage. The middle stage switches MS(1,1) – MS(1,8), MS(2,1) – MS(2,8), and MS(3,1) – MS(3,8) are referred to as middle switches or middle ports.

In the example illustrated in FIG. 4C (or in FIG1C1, or in FIG. 4C2), a fan-out of four is possible to satisfy a multicast connection request if input switch is IS2, but only two switches in middle stage 130 will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS1, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage 130 when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network 400C (or 400C1,

or 400C2), to be operated in rearrangeably nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage 130 is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage 130, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the rearrangeably nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Asymmetric folded RNB ($N_2 > N_1$) Embodiments:

Network 400D of FIG. 4D is an example of general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ with $(2 \times \log_d N_1) - 1$ stages where $N_2 > N_1$ and $N_2 = p * N_1$ where $p > 1$. In network 400D of FIG. 4D, $N_1 = N$ and $N_2 = p * N$. The general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s \geq 2$ according to the current invention. Also the general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if $s \geq 2$ according to the current invention. (And in the example of FIG. 4D, $s = 2$). The general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ with $(2 \times \log_d N_1) - 1$ stages has d inlet links for each of $\frac{N_1}{d}$ input switches IS1-IS(N_1/d) (for example the links IL1-IL(d) to the input switch IS1) and $2 \times d$ outgoing links for each of $\frac{N_1}{d}$ input switches IS1-IS(N_1/d) (for example the links ML(1,1) - ML(1,2d) to the input switch IS1). There are d_2 (where $d_2 = N_2 \times \frac{d}{N_1} = p \times d$) outlet links for each of $\frac{N_1}{d}$ output switches OS1-OS(N_1/d) (for

example the links OL1-OL($p \times d$) to the output switch OS1) and $d + d_2$ ($= d + p \times d$)

incoming links for each of $\frac{N_1}{d}$ output switches OS1-OS(N_1/d) (for

example $ML(2 \times \text{Log}_d N_1 - 2, 1)$ - $ML(2 \times \text{Log}_d N_1 - 2, d + d_2)$ to the output switch OS1).

Each of the $\frac{N_1}{d}$ input switches IS1 – IS(N_1/d) are connected to exactly $2 \times d$

- 5 switches in middle stage 130 through $2 \times d$ links (for example in one embodiment the input switch IS1 is connected to middle switches MS(1,1) - MS(1,d) through the links ML(1,1) - ML(1,d) and to middle switches MS(1, $N_1/d+1$) – MS(1, $\{N_1/d\}+d$) through the links ML(1,d+1) – ML(1,2d) respectively.

Each of the $2 \times \frac{N_1}{d}$ middle switches MS(1,1) – MS(1,2 N_1/d) in the middle stage

- 10 130 are connected from exactly d input switches through d links and also are connected to exactly d switches in middle stage 140 through d links.

Similarly each of the $2 \times \frac{N_1}{d}$ middle switches $MS(\text{Log}_d N_1 - 1, 1)$ -

$MS(\text{Log}_d N_1 - 1, 2 \times \frac{N_1}{d})$ in the middle stage $130 + 10 * (\text{Log}_d N_1 - 2)$ are connected from

- 15 exactly d switches in middle stage $130 + 10 * (\text{Log}_d N_1 - 3)$ through d links and also are connected to exactly d switches in middle stage $130 + 10 * (\text{Log}_d N_1 - 1)$ through d links.

Similarly each of the $2 \times \frac{N_1}{d}$ middle switches $MS(2 \times \text{Log}_d N_1 - 3, 1)$ -

$MS(2 \times \text{Log}_d N_1 - 3, 2 \times \frac{N_1}{d})$ in the middle stage $130 + 10 * (2 * \text{Log}_d N_1 - 4)$ are

- 20 connected from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N_1 - 5)$ through d links and also are connected to exactly d output switches in output stage 120 through d links.

Each of the $\frac{N_1}{d}$ output switches OS1 – OS(N_1/d) are connected from exactly $d + d_2$ switches in middle stage $130 + 10 * (2 * \text{Log}_d N_1 - 4)$ through $d + d_2$ links.

As described before, again the connection topology of a general $V_{fold}(N_1, N_2, d, s)$ may be any one of the connection topologies. For example the connection topology of the network $V_{fold}(N_1, N_2, d, s)$ may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general $V_{fold}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network $V_{fold}(N_1, N_2, d, s)$ can be built. The embodiments of FIG. 4C, FIG. 4C1, and FIG. 4C2 are three examples of network $V_{fold}(N_1, N_2, d, s)$ for $s = 2$ and $N_2 > N_1$.

The general symmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s \geq 2$ according to the current invention. Also the general symmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if $s \geq 2$ according to the current invention.

For example, the network of FIG. 4C shows an exemplary five-stage network, namely $V_{fold}(8, 24, 2, 2)$, with the following multicast assignment $I_1 = \{2, 3\}$ and all other $I_j = \phi$ for $j = [2-8]$. It should be noted that the connection I_1 fans out in the first stage switch IS1 into middle switches MS(1,1) and MS(1,5) in middle stage 130, and fans out in middle switches MS(1,1) and MS(1,5) only once into middle switches MS(2,1) and MS(2,5) respectively in middle stage 140.

The connection I_1 also fans out in middle switches MS(2,1) and MS(2,5) only once into middle switches MS(3,1) and MS(3,7) respectively in middle stage 150. The connection I_1 also fans out in middle switches MS(3,1) and MS(3,7) only once into

output switches OS2 and OS3 in output stage 120. Finally the connection I_1 fans out once in the output stage switch OS2 into outlet link OL7 and in the output stage switch OS3 twice into the outlet links OL13 and OL16. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage 130.

Asymmetric folded RNB ($N_1 > N_2$) Embodiments:

Referring to FIG. 4E, in one embodiment, an exemplary asymmetrical folded multi-stage network 400E with five stages of thirty two switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, six by eight switches IS1-IS4 and output stage 120 consists of four, four by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of eight, four by two switches MS(1,1) - MS(1,8), middle stage 140 consists of eight, two by two switches MS(2,1) - MS(2,8), and middle stage 150 consists of eight, two by two switches MS(3,1) - MS(3,8).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size six by eight, the switches in output stage 120 are of size four by two, and there are eight switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size six by eight, the switches in output stage 120 are of size four by two, and there are eight switches of size four by two in middle stage 130, and eight switches of size two by two in middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_2}{d}$, where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1 > N_2$ and

$N_1 = p * N_2$ where $p > 1$. The number of middle switches in each middle stage is denoted by $2 \times \frac{N_2}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * (d + d_1)$ and each output switch OS1-OS4 can be denoted in general with the notation $(2 \times d * d)$, where $d_1 = N_1 \times \frac{d}{N_2} = p \times d$. The size of each switch in any of the middle stages excepting the first middle stage can be denoted as $d * d$. The size of each switch in the first middle stage can be denoted as $\frac{(d + d_1)}{2} * d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric folded multi-stage network can be represented with the notation $V_{fold}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL24), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL8), d represents the inlet links of each input switch where $N_1 > N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

15 Each of the $\frac{N_2}{d}$ input switches IS1 – IS4 are connected to exactly $d + d_1$ switches in middle stage 130 through $d + d_1$ links (for example input switch IS1 is connected to middle switches MS(1,1), MS(1,2), MS(1,3), MS(1,4), MS(1,5), MS(1,6), MS(1,7), and MS(1,8) through the links ML(1,1), ML(1,2), ML(1,3), ML(1,4), ML(1,5), ML(1,6), ML(1,7), and ML(1,8) respectively).

20 Each of the $2 \times \frac{N_2}{d}$ middle switches MS(1,1) – MS(1,8) in the middle stage 130 are connected from exactly $\frac{(d + d_1)}{2}$ input switches through $\frac{(d + d_1)}{2}$ links (for example the links ML(1,1), ML(1,9), ML(1,17) and ML(1,25) are connected to the middle switch MS(1,1) from input switch IS1, IS2, IS3, and IS4 respectively) and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1)

and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,3) respectively).

5 Similarly each of the $2 \times \frac{N_2}{d}$ middle switches MS(2,1) – MS(2,8) in the middle stage 140 are connected from exactly d switches in middle stage 130 through d links (for example the links ML(2,1) and ML(2,6) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,3) respectively) and also are connected to exactly d switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and MS(3,3) respectively).

10 Similarly each of the $2 \times \frac{N_2}{d}$ middle switches MS(3,1) – MS(3,8) in the middle stage 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,6) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,3) respectively) and also are connected to exactly d output switches in output stage 120 through d links (for example the links
15 ML(4,1) and ML(4,2) are connected to output switches OS1 and OS2 respectively from middle switches MS(3,1)).

Each of the $\frac{N_2}{d}$ output switches OS1 – OS4 are connected from exactly $2 \times d$ switches in middle stage 150 through $2 \times d$ links (for example output switch OS1 is connected from middle switches MS(3,1), MS(3,2), MS(3,5), and MS(3,6) through the
20 links ML(4,1), ML(4,3), ML(4,9), and ML(4,11) respectively).

Finally the connection topology of the network 400E shown in FIG. 4E is known to be back to back inverse Benes connection topology.

Referring to FIG. 4E1, in another embodiment of network $V_{fold}(N_1, N_2, d, s)$, an exemplary asymmetrical folded multi-stage network 400E1 with five stages of thirty two
25 switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110

and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, six by eight switches IS1-IS4 and output stage 120 consists of four, four by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of eight, four by two switches MS(1,1) - MS(1,8), middle stage 140 consists of eight, two by two switches MS(2,1) - MS(2,8), and middle stage 150 consists of eight, two by two switches MS(3,1) - MS(3,8).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size six by eight, the switches in output stage 120 are of size four by two, and there are eight switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size six by eight, the switches in output stage 120 are of size four by two, and there are eight switches of size four by two in middle stage 130, and eight switches of size two by two in middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_2}{d}$, where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1 > N_2$ and $N_1 = p * N_2$ where $p > 1$. The number of middle switches in each middle stage is denoted by $2 \times \frac{N_2}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * (d + d_1)$ and each output switch OS1-OS4 can be denoted in general with the notation $(2 \times d * d)$, where $d_1 = N_1 \times \frac{d}{N_2} = p \times d$. The size of each switch in any of the middle stages excepting the first middle stage can be denoted as $d * d$. The size of each switch in the first middle stage can be denoted as $\frac{(d + d_1)}{2} * d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The asymmetric folded multi-stage

network of FIG. 4E1 is also the network of the type $V_{fold}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL24), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL8), d represents the inlet links of each input switch where $N_1 > N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the $\frac{N_2}{d}$ input switches IS1 – IS4 are connected to exactly $d + d_1$ switches in middle stage 130 through $d + d_1$ links (for example input switch IS1 is connected to middle switches MS(1,1), MS(1,2), MS(1,3), MS(1,4), MS(1,5), MS(1,6), MS(1,7), and MS(1,8) through the links ML(1,1), ML(1,2), ML(1,3), ML(1,4), ML(1,5), ML(1,6), ML(1,7), and ML(1,8) respectively).

Each of the $2 \times \frac{N_2}{d}$ middle switches MS(1,1) – MS(1,8) in the middle stage 130 are connected from exactly $\frac{(d + d_1)}{2}$ input switches through $\frac{(d + d_1)}{2}$ links (for example the links ML(1,1), ML(1,9), ML(1,17) and ML(1,25) are connected to the middle switch MS(1,1) from input switch IS1, IS2, IS3, and IS4 respectively) and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,2) respectively).

Similarly each of the $2 \times \frac{N_2}{d}$ middle switches MS(2,1) – MS(2,8) in the middle stage 140 are connected from exactly d switches in middle stage 130 through d links (for example the links ML(2,1) and ML(2,5) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,3) respectively) and also are connected to exactly d switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and MS(3,2) respectively).

Similarly each of the $2 \times \frac{N_2}{d}$ middle switches MS(3,1) – MS(3,8) in the middle stage 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,5) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,3) respectively) and also are connected to
 5 exactly d output switches in output stage 120 through d links (for example the links ML(4,1) and ML(4,2) are connected to output switches OS1 and OS2 respectively from middle switches MS(3,1)).

Each of the $\frac{N_2}{d}$ output switches OS1 – OS4 are connected from exactly $2 \times d$ switches in middle stage 150 through $2 \times d$ links (for example output switch OS1 is
 10 connected from middle switches MS(3,1), MS(3,3), MS(3,5), and MS(3,7) through the links ML(4,1), ML(4,5), ML(4,9), and ML(4,13) respectively).

Finally the connection topology of the network 400E1 shown in FIG. 4E1 is known to be back to back Omega connection topology.

Referring to FIG. 4E2, in another embodiment of network $V_{fold}(N_1, N_2, d, s)$, an
 15 exemplary asymmetrical folded multi-stage network 400E2 with five stages of thirty two switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, six by eight switches IS1-IS4 and output stage 120 consists of four, four
 20 by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of eight, four by two switches MS(1,1) - MS(1,8), middle stage 140 consists of eight, two by two switches MS(2,1) - MS(2,8), and middle stage 150 consists of eight, two by two switches MS(3,1) - MS(3,8).

Such a network can be operated in strictly non-blocking manner for unicast
 25 connections, because the switches in the input stage 110 are of size six by eight, the switches in output stage 120 are of size four by two, and there are eight switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be

operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size six by eight, the switches in output stage 120 are of size four by two, and there are eight switches of size four by two in middle stage 130, and eight switches of size two by two in middle stage 140 and middle stage 150.

- 5 In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_2}{d}$, where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1 > N_2$ and $N_1 = p * N_2$ where $p > 1$. The number of middle switches in each middle stage is
- 10 denoted by $2 \times \frac{N_2}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * (d + d_1)$ and each output switch OS1-OS4 can be denoted in general with the notation $(2 \times d * d)$, where $d_1 = N_1 \times \frac{d}{N_2} = p \times d$. The size of each switch in any of the middle stages excepting the first middle stage can be denoted as $d * d$. The size of each switch in the first middle stage can be denoted as $\frac{(d + d_1)}{2} * d$. A switch as used
- 15 herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The asymmetric folded multi-stage network of FIG. 4E1 is also the network of the type $V_{fold}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL24), N_2 represents the total number of outlet links of all output switches (for example
- 20 the links OL1-OL8), d represents the inlet links of each input switch where $N_1 > N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

- Each of the $\frac{N_2}{d}$ input switches IS1 – IS4 are connected to exactly $d + d_1$ switches in middle stage 130 through $d + d_1$ links (for example input switch IS1 is
- 25 connected to middle switches MS(1,1), MS(1,2), MS(1,3), MS(1,4), MS(1,5), MS(1,6),

MS(1,7), and MS(1,8) through the links ML(1,1), ML(1,2), ML(1,3), ML(1,4), ML(1,5), ML(1,6), ML(1,7), and ML(1,8) respectively).

Each of the $2 \times \frac{N_2}{d}$ middle switches MS(1,1) – MS(1,8) in the middle stage 130 are connected from exactly $\frac{(d+d_1)}{2}$ input switches through $\frac{(d+d_1)}{2}$ links (for example the links ML(1,1), ML(1,9), ML(1,17) and ML(1,25) are connected to the middle switch MS(1,1) from input switch IS1, IS2, IS3, and IS4 respectively) and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,2) respectively).

10 Similarly each of the $2 \times \frac{N_2}{d}$ middle switches MS(2,1) – MS(2,8) in the middle stage 140 are connected from exactly d switches in middle stage 130 through d links (for example the links ML(2,1) and ML(2,8) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,4) respectively) and also are connected to exactly d switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and MS(3,2) respectively).

20 Similarly each of the $2 \times \frac{N_2}{d}$ middle switches MS(3,1) – MS(3,8) in the middle stage 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,8) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,4) respectively) and also are connected to exactly d output switches in output stage 120 through d links (for example the links ML(4,1) and ML(4,2) are connected to output switches OS1 and OS2 respectively from middle switches MS(3,1)).

25 Each of the $\frac{N_2}{d}$ output switches OS1 – OS4 are connected from exactly $2 \times d$ switches in middle stage 150 through $2 \times d$ links (for example output switch OS1 is

connected from middle switches MS(3,1), MS(3,4), MS(3,5), and MS(3,8) through the links ML(4,1), ML(4,8), ML(4,9), and ML(4,16) respectively).

Finally the connection topology of the network 400E2 shown in FIG. 4E2 is hereinafter called nearest neighbor connection topology.

5 In the three embodiments of FIG. 4E, FIG. 4E1 and FIG. 4E2 the connection topology is different. That is the way the links ML(1,1) - ML(1,32), ML(2,1) - ML(2,16), ML(3,1) - ML(3,16), and ML(4,1) - ML(4,16) are connected between the respective stages is different. Even though only three embodiments are illustrated, in general, the network $V_{fold}(N_1, N_2, d, s)$ can comprise any arbitrary type of connection topology. For
 10 example the connection topology of the network $V_{fold}(N_1, N_2, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{fold}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network
 15 $V_{fold}(N_1, N_2, d, s)$ can be built. The embodiments of FIG. 4E, FIG. 4E1, and FIG. 4E2 are only three examples of network $V_{fold}(N_1, N_2, d, s)$.

 In the three embodiments of FIG. 4E, FIG. 4E1 and FIG. 4E2, each of the links ML(1,1) – ML(1,32), ML(2,1) – ML(2,16), ML(3,1) – ML(3,16) and ML(4,1) – ML(4,16) are either available for use by a new connection or not available if currently
 20 used by an existing connection. The input switches IS1-IS4 are also referred to as the network input ports. The input stage 110 is often referred to as the first stage. The output switches OS1-OS4 are also referred to as the network output ports. The output stage 120 is often referred to as the last stage. The middle stage switches MS(1,1) – MS(1,8), MS(2,1) – MS(2,8), and MS(3,1) – MS(3,8) are referred to as middle switches or middle
 25 ports.

 In the example illustrated in FIG. 4E (or in FIG1E1, or in FIG. 4E2), a fan-out of four is possible to satisfy a multicast connection request if input switch is IS2, but only two switches in middle stage 130 will be used. Similarly, although a fan-out of three is

possible for a multicast connection request if the input switch is IS1, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage 130 when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from
 5 input switch to no more than two middle switches permits the network 400E (or 400E1, or 400E2), to be operated in rearrangeably nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on
 10 the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage 130 is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage 130, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the
 15 rearrangeably nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Asymmetric folded RNB ($N_1 > N_2$) Embodiments:

Network 400F of FIG. 4F is an example of general asymmetrical folded multi-
 20 stage network $V_{fold}(N_1, N_2, d, s)$ with $(2 \times \log_d N_2) - 1$ stages where $N_1 > N_2$ and $N_1 = p * N_2$ where $p > 1$. In network 400D of FIG. 4F, $N_2 = N$ and $N_1 = p * N$. The general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s \geq 2$ according to the current invention. Also the general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$
 25 can be operated in strictly nonblocking manner for unicast if $s \geq 2$ according to the current invention. (And in the example of FIG. 4F, $s = 2$). The general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ with $(2 \times \log_d N_2) - 1$ stages has d_1
 (where $d_1 = N_1 \times \frac{d}{N_2} = p \times d$ inlet links for each of $\frac{N_2}{d}$ input switches IS1-IS(N_2/d) (for

example the links $IL1-IL(p*d)$ to the input switch IS1) and $d + d_1 (= d + p*d)$ outgoing links for each of $\frac{N_2}{d}$ input switches IS1-IS(N_2/d) (for example the links $ML(1,1) - ML(1,(d+p*d))$ to the input switch IS1). There are d outlet links for each of $\frac{N_2}{d}$ output switches OS1-OS(N_2/d) (for example the links $OL1-OL(d)$ to the output switch OS1) and

5 $2*d$ incoming links for each of $\frac{N_2}{d}$ output switches OS1-OS(N_2/d) (for example $ML(2*Log_d N_2 - 2,1) - ML(2*Log_d N_2 - 2,2*d)$ to the output switch OS1).

Each of the $\frac{N_2}{d}$ input switches IS1 – IS(N_2/d) are connected to exactly $d + d_1$ switches in middle stage 130 through $d + d_1$ links (for example in one embodiment the input switch IS1 is connected to middle switches $MS(1,1) - MS(1, (d+d_1)/2)$ through the

10 links $ML(1,1) - ML(1,(d+d_1)/2)$ and to middle switches $MS(1,N_1/d+1) - MS(1, \{N_1/d\}+(d+d_1)/2)$ through the links $ML(1, ((d+d_1)/2)+1) - ML(1, (d+d_1))$ respectively.

Each of the $2*\frac{N_2}{d}$ middle switches $MS(1,1) - MS(1,2*N_2/d)$ in the middle stage 130 are connected from exactly d input switches through d links and also are connected to exactly d switches in middle stage 140 through d links.

15 Similarly each of the $2*\frac{N_2}{d}$ middle switches $MS(Log_d N_2 - 1,1) - MS(Log_d N_2 - 1,2*\frac{N_2}{d})$ in the middle stage $130 + 10*(Log_d N_2 - 2)$ are connected from exactly d switches in middle stage $130 + 10*(Log_d N_2 - 3)$ through d links and also are connected to exactly d switches in middle stage $130 + 10*(Log_d N_2 - 1)$ through d links.

Similarly each of the $2 \times \frac{N_2}{d}$ middle switches $MS(2 \times \text{Log}_d N_2 - 3, 1) - MS(2 \times \text{Log}_d N_2 - 3, 2 \times \frac{N_2}{d})$ in the middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 4)$ are connected from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 5)$ through d links and also are connected to exactly d output switches in output stage 120 through d links.

Each of the $\frac{N_2}{d}$ output switches OS1 – OS(N_2/d) are connected from exactly $2 \times d$ switches in middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 4)$ through $2 \times d$ links.

As described before, again the connection topology of a general $V_{fold}(N_1, N_2, d, s)$ may be any one of the connection topologies. For example the connection topology of the network $V_{fold}(N_1, N_2, d, s)$ may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general $V_{fold}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network $V_{fold}(N_1, N_2, d, s)$ can be built. The embodiments of FIG. 4E, FIG. 4E1, and FIG. 4E2 are three examples of network $V_{fold}(N_1, N_2, d, s)$ for $s = 2$ and $N_1 > N_2$.

The general symmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s \geq 2$ according to the current invention. Also the general symmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if $s \geq 2$ according to the current invention.

For example, the network of FIG. 4E shows an exemplary five-stage network, namely $V_{fold}(24, 8, 2, 2)$, with the following multicast assignment $I_1 = \{2, 3\}$ and all other

$I_j = \phi$ for $j = [2-8]$. It should be noted that the connection I_1 fans out in the first stage switch IS1 into middle switches MS(1,1) and MS(1,5) in middle stage 130, and fans out in middle switches MS(1,1) and MS(1,5) only once into middle switches MS(2,1) and MS(2,5) respectively in middle stage 140.

- 5 The connection I_1 also fans out in middle switches MS(2,1) and MS(2,5) only once into middle switches MS(3,1) and MS(3,7) respectively in middle stage 150. The connection I_1 also fans out in middle switches MS(3,1) and MS(3,7) only once into output switches OS2 and OS3 in output stage 120. Finally the connection I_1 fans out once in the output stage switch OS2 into outlet link OL3 and in the output stage switch
- 10 OS3 twice into the outlet links OL5 and OL6. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage 130.

SNB Embodiments:

- The folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ disclosed, in the current
- 15 invention, is topologically exactly the same as the multi-stage network $V_{fold}(N_1, N_2, d, s)$, disclosed in U.S. Provisional Patent Application Docket No. M-0037US that is incorporated by reference above, excepting that in the illustrations folded network $V_{fold}(N_1, N_2, d, s)$ is shown as it is folded at middle stage $130 + 10 * (\text{Log}_d N_2 - 2)$.

- The general symmetrical folded multi-stage network $V_{fold}(N, d, s)$ can also be
- 20 operated in strictly nonblocking manner for multicast when $s \geq 3$ according to the current invention. Similarly the general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can also be operated in strictly nonblocking manner for multicast when $s \geq 3$ according to the current invention.

Symmetric folded RNB Unicast Embodiments:

- 25 Referring to FIG. 5A, an exemplary symmetrical folded multi-stage network 500A respectively with five stages of twenty switches for satisfying communication

requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by two switches IS1-IS4 and output stage 120 consists of four, two by two switches OS1-OS4.

5 And all the middle stages namely middle stage 130 consists of four, two by two switches MS(1,1) - MS(1,4), middle stage 140 consists of four, two by two switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, two by two switches MS(3,1) - MS(3,4).

Such a network can be operated in rearrangeably nonblocking manner for unicast connections, because the switches in the input stage 110 are of size two by two, the

10 switches in output stage 120 are of size two by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

The connection topology of the network 500A shown in FIG. 5A is known to be back to back inverse Benes connection topology. In other embodiments the connection topology is different. That is the way the links ML(1,1) - ML(1,8), ML(2,1) - ML(2,8),

15 ML(3,1) - ML(3,8), and ML(4,1) - ML(4,8) are connected between the respective stages is different.

Even though only one embodiment is illustrated, in general, the network $V_{fold}(N, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{fold}(N, d, s)$ may be back to back Benes networks,

20 Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{fold}(N, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{fold}(N, d, s)$ can be built. The embodiment of FIG. 5A is only one example of network $V_{fold}(N, d, s)$.

25 The network 500A of FIG. 5A is also rearrangeably nonblocking for unicast according to the current invention. In one embodiment of these networks each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the

variable $\frac{N}{d}$, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by $\frac{N}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * d$ and each output switch OS1-OS4 can be denoted in general with the notation $d * d$. Likewise, the size of each switch in any of the middle stages can be denoted as $d * d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric folded multi-stage network can be represented with the notation $V_{fold}(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL1-IL8), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL1-IL8 as there are outlet links OL1-OL8, in a symmetrical network they are the same.

In network 500A of FIG. 5A, each of the $\frac{N}{d}$ input switches IS1 – IS4 are connected to exactly d switches in middle stage 130 through d links (for example input switch IS1 is connected to middle switches MS(1,1) and MS(1,2) through the links ML(1,1) and ML(1,2) respectively).

Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through d links (for example the links ML(1,1) and ML(1,4) are connected to the middle switch MS(1,1) from input switch IS1 and IS2 respectively) and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,3) respectively).

Similarly each of the $\frac{N}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through d links (for

example the links ML(2,1) and ML(2,6) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,3) respectively) and also are connected to exactly d switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and
 5 MS(3,3) respectively).

Similarly each of the $\frac{N}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,6) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,3) respectively) and also are connected to exactly d
 10 output switches in output stage 120 through d links (for example the links ML(4,1) and ML(4,2) are connected to output switches OS1 and OS2 respectively from middle switch MS(3,1)).

Each of the $\frac{N}{d}$ output switches OS1 – OS4 are connected from exactly d switches in middle stage 150 through d links (for example output switch OS1 is
 15 connected from middle switches MS(3,1) and MS(3,2) through the links ML(4,1) and ML(4,4) respectively).

Generalized Symmetric folded RNB Unicast Embodiments:

Network 500B of FIG. 5B is an example of general symmetrical folded multi-stage network $V_{fold}(N, d, s)$ with $(2 \times \log_d N) - 1$ stages. The general symmetrical folded
 20 multi-stage network $V_{fold}(N, d, s)$ can be operated in rearrangeably nonblocking manner for unicast when $s \geq 1$ according to the current invention (and in the example of FIG. 5B, $s = 1$). The general symmetrical folded multi-stage network $V_{fold}(N, d, s)$ with
 $(2 \times \log_d N) - 1$ stages has d inlet links for each of $\frac{N}{d}$ input switches IS1-IS(N/d) (for
 example the links IL1-IL(d) to the input switch IS1) and d outgoing links for each of $\frac{N}{d}$
 25 input switches IS1-IS(N/d) (for example the links ML(1,1) - ML(1,d) to the input switch

IS1). There are d outlet links for each of $\frac{N}{d}$ output switches OS1-OS(N/d) (for example OL1-OL(d) to the output switch OS1) and d incoming links for each of $\frac{N}{d}$ output switches OS1-OS(N/d) (for example $ML(2 \times \log_d N - 2, 1) - ML(2 \times \log_d N - 2, d)$ to the output switch OS1).

- 5 Each of the $\frac{N}{d}$ input switches IS1 – IS(N/d) are connected to exactly d switches in middle stage 130 through d links.

Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,N/d) in the middle stage 130 are connected from exactly d input switches through d links and also are connected to exactly d switches in middle stage 140 through d links.

- 10 Similarly each of the $\frac{N}{d}$ middle switches $MS(\log_d N - 1, 1) - MS(\log_d N - 1, \frac{N}{d})$ in the middle stage $130 + 10 * (\log_d N - 2)$ are connected from exactly d switches in middle stage $130 + 10 * (\log_d N - 3)$ through d links and also are connected to exactly d switches in middle stage $130 + 10 * (\log_d N - 1)$ through d links.

Similarly each of the $\frac{N}{d}$ middle switches $MS(2 \times \log_d N - 3, 1) -$

- 15 $MS(2 \times \log_d N - 3, \frac{N}{d})$ in the middle stage $130 + 10 * (2 * \log_d N - 4)$ are connected from exactly d switches in middle stage $130 + 10 * (2 * \log_d N - 5)$ through d links and also are connected to exactly d output switches in output stage 120 through d links.

Each of the $\frac{N}{d}$ output switches OS1 – OS(N/d) are connected from exactly d switches in middle stage $130 + 10 * (2 * \log_d N - 4)$ through d links.

The general symmetrical folded multi-stage network $V_{fold}(N, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s = 1$ according to the current invention.

Asymmetric folded RNB ($N_2 > N_1$) Unicast Embodiments:

5 Referring to FIG. 5C, an exemplary symmetrical folded multi-stage network 500C respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by two switches IS1-IS4
10 and output stage 120 consists of four, six by six switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, two by two switches MS(1,1) - MS(1,4), middle stage 140 consists of four, two by two switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, two by six switches MS(3,1) - MS(3,4).

Such networks can be operated in rearrangeably nonblocking manner for unicast
15 connections, because the switches in the input stage 110 are of size two by two, the switches in output stage 120 are of size six by six, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

The connection topology of the network 500C shown in FIG. 5C is known to be back to back inverse Benes connection topology. The connection topology of the
20 networks 500C is different in the other embodiments. That is the way the links ML(1,1) - ML(1,8), ML(2,1) - ML(2,8), ML(3,1) - ML(3,8), and ML(4,1) - ML(4,8) are connected between the respective stages is different.

Even though only one embodiment is illustrated, in general, the network
 $V_{fold}(N_1, N_2, d, s)$ can comprise any arbitrary type of connection topology. For example
25 the connection topology of the network $V_{fold}(N_1, N_2, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{fold}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link all the output links should be

reachable. Based on this property numerous embodiments of the network $V_{fold}(N_1, N_2, d, s)$ can be built. The embodiment of FIG. 5C is only one example of network $V_{fold}(N_1, N_2, d, s)$.

The networks 500C of FIG. 5C is also rearrangeably nonblocking for unicast according to the current invention. In one embodiment of these networks each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_1}{d}$, where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_2 > N_1$ and $N_2 = p * N_1$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_1}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * d$ and each output switch OS1-OS4 can be denoted in general with the notation $d_2 * d_2$, where $d_2 = N_2 * \frac{d}{N_1} = p * d$. The size of each switch in any of the middle stages excepting the last middle stage can be denoted as $d * d$. The size of each switch in the last middle stage can be denoted as $d * d_2$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric folded multi-stage network can be represented with the notation $V_{fold}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL24), d represents the inlet links of each input switch where $N_2 > N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

In network 500C of FIG. 5C, each of the $\frac{N_1}{d}$ input switches IS1 – IS4 are connected to exactly d switches in middle stage 130 through d links (for example input

switch IS1 is connected to middle switches MS(1,1) and MS(1,2) through the links ML(1,1) and ML(1,2) respectively).

Each of the $\frac{N_1}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through d links (for example the links ML(1,1) and ML(1,4) are connected to the middle switch MS(1,1) from input switch IS1 and IS2 respectively) and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,3) respectively).

Similarly each of the $\frac{N_1}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through d links (for example the links ML(2,1) and ML(2,6) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,3) respectively) and also are connected to exactly d switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and MS(3,3) respectively).

Similarly each of the $\frac{N_1}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,6) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,3) respectively) and also are connected to exactly d output switches in output stage 120 through d_2 links (for example the links ML(4,1) and ML(4,2) are connected to output switches OS1 from middle switch MS(3,1); the links ML(4,3) and ML(4,4) are connected to output switches OS2 from middle switch MS(3,1); the link ML(4,5) is connected to output switches OS3 from middle switch MS(3,1); and the link ML(4,6) is connected to output switches OS4 from middle switch MS(3,1)).

Each of the $\frac{N_1}{d}$ output switches OS1 – OS4 are connected from exactly d switches in middle stage 150 through d_2 links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1) and ML(4,2); output switch OS1 is connected from middle switch MS(3,2) through the links ML(4,7) and ML(4,8); output switch OS1 is connected from middle switch MS(3,3) through the link ML(4,13); and output switch OS1 is connected from middle switch MS(3,4) through the links ML(4,19)).

Generalized Asymmetric folded RNB ($N_2 > N_1$) Unicast Embodiments:

10 Network 500D of FIG. 5D is an example of general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ with $(2 \times \log_d N) - 1$ stages where $N_2 > N_1$ and $N_2 = p * N_1$ where $p > 1$. In network 500D of FIG. 5D, $N_1 = N$ and $N_2 = p * N$. The general symmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for unicast when $s \geq 1$ according to the current
 15 invention (and in the example of FIG. 5D, $s = 1$). The general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ with $(2 \times \log_d N) - 1$ stages has d inlet links for each of $\frac{N_1}{d}$ input switches IS1-IS(N_1/d) (for example the links IL1-IL(d) to the input switch IS1) and d outgoing links for each of $\frac{N_1}{d}$ input switches IS1-IS(N_1/d) (for example the links ML(1,1) - ML(1, d) to the input switch IS1). There are d_2 (where $d_2 = N_2 \times \frac{d}{N_1} = p \times d$)
 20 outlet links for each of $\frac{N_1}{d}$ output switches OS1-OS(N_1/d) (for example the links OL1-OL($p*d$) to the output switch OS1) and d_2 ($= p \times d$) incoming links for each of $\frac{N_1}{d}$ output switches OS1-OS(N_1/d) (for example $ML(2 \times \log_d N_1 - 2, 1)$ - $ML(2 \times \log_d N_1 - 2, d_2)$ to the output switch OS1).

Each of the $\frac{N_1}{d}$ input switches IS1 – IS(N_1/d) are connected to exactly d switches in middle stage 130 through d links.

Each of the $\frac{N_1}{d}$ middle switches MS(1,1) – MS(1, N_1/d) in the middle stage 130 are connected from exactly d input switches through d links and also are connected to exactly d switches in middle stage 140 through d links.

Similarly each of the $\frac{N_1}{d}$ middle switches $MS(\text{Log}_d N_1 - 1, 1)$ - $MS(\text{Log}_d N_1 - 1, \frac{N_1}{d})$ in the middle stage $130 + 10 * (\text{Log}_d N_1 - 2)$ are connected from exactly d switches in middle stage $130 + 10 * (\text{Log}_d N_1 - 3)$ through d links and also are connected to exactly d switches in middle stage $130 + 10 * (\text{Log}_d N_1 - 1)$ through d links.

Similarly each of the $\frac{N_1}{d}$ middle switches $MS(2 * \text{Log}_d N_1 - 3, 1)$ - $MS(2 * \text{Log}_d N_1 - 3, \frac{N_1}{d})$ in the middle stage $130 + 10 * (2 * \text{Log}_d N_1 - 4)$ are connected from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N_1 - 5)$ through d links and also are connected to exactly d output switches in output stage 120 through d_2 links.

Each of the $\frac{N_1}{d}$ output switches OS1 – OS(N_1/d) are connected from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N - 4)$ through d_2 links.

The general symmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s \geq 1$ according to the current invention.

20

Asymmetric folded RNB ($N_1 > N_2$) Unicast Embodiments:

Referring to FIG. 5E, an exemplary symmetrical folded multi-stage network 500E with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks,

5 between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, six by six switches IS1-IS4 and output stage 120 consists of four, two by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, six by two switches MS(1,1) - MS(1,4), middle stage 140 consists of four, two by two switches MS(2,1) - MS(2,4), and middle stage 150

10 consists of four, two by two switches MS(3,1) - MS(3,4).

Such a network can be operated in rearrangeably nonblocking manner for unicast connections, because the switches in the input stage 110 are of size six by six, the switches in output stage 120 are of size two by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

15 The connection topology of the network 500E shown in FIG. 5E is known to be back to back inverse Benes connection topology. The connection topology of the networks 500E is different in the other embodiments. That is the way the links ML(1,1) - ML(1,8), ML(2,1) - ML(2,8), ML(3,1) - ML(3,8), and ML(4,1) - ML(4,8) are connected between the respective stages is different.

20 Even though only one embodiment is illustrated, in general, the network $V_{fold}(N_1, N_2, d, s)$, comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{fold}(N_1, N_2, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{fold}(N_1, N_2, d, s)$ network is,

25 when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{fold}(N_1, N_2, d, s)$ can be built. The embodiment of FIG. 5E is only one example of network $V_{fold}(N_1, N_2, d, s)$.

The network 500E is rearrangeably nonblocking for unicast according to the current invention. In one embodiment of these networks each of the input switches IS1- IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_2}{d}$, where

5 N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1 > N_2$ and $N_1 = p * N_2$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_2}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d_1 * d_1$ and each output switch OS1-OS4 can be denoted in general with the notation $(d * d)$, where $d_1 = N_1 \times \frac{d}{N_2} = p \times d$. The size of each switch in any of the

10 middle stages excepting the first middle stage can be denoted as $d * d$. The size of each switch in the first middle stage can be denoted as $d_1 * d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric folded multi-stage network can be represented with the notation $V_{fold}(N_1, N_2, d, s)$, where N_1 represents the total number of

15 inlet links of all input switches (for example the links IL1-IL24), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL8), d represents the inlet links of each output switch where $N_1 > N_2$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

In network 500E of FIG. 5E, each of the $\frac{N_2}{d}$ input switches IS1 – IS4 are

20 connected to exactly d switches in middle stage 130 through d_1 links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1) and ML(1,2); input switch IS1 is connected to middle switch MS(1,2) through the links ML(1,3) and ML(1,4); input switch IS1 is connected to middle switch MS(1,3) through the link ML(1,5); and input switch IS1 is connected to middle switch MS(1,4) through

25 the links ML(1,6)).

Each of the $\frac{N_2}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d_1 input switches through d links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1; the links ML(1,7) and ML(1,8) are connected to the middle switch MS(1,1) from input switch IS2; the link ML(1,13) is connected to the middle switch MS(1,1) from input switch IS3; and the link ML(1,19) is connected to the middle switch MS(1,1) from input switch IS4), and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,3) respectively).

10 Similarly each of the $\frac{N_1}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through d links (for example the links ML(2,1) and ML(2,6) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,3) respectively) and also are connected to exactly d switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and MS(3,3) respectively).

20 Similarly each of the $\frac{N_1}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,6) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,3) respectively) and also are connected to exactly d output switches in output stage 120 through d_2 links (for example the links ML(4,1) and ML(4,2) are connected to output switches OS1 and OS2 respectively from middle switch MS(3,1)).

25 Each of the $\frac{N_1}{d}$ output switches OS1 – OS4 are connected from exactly d switches in middle stage 150 through d_2 links (for example output switch OS1 is

connected from middle switches MS(3,1) and MS(3,2) through the links ML(4,1) and ML(4,4) respectively).

Generalized Asymmetric folded RNB ($N_1 > N_2$) Unicast Embodiments:

Network 500F of FIG. 5F is an example of general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ with $(2 \times \log_d N) - 1$ stages where $N_1 > N_2$ and $N_1 = p * N_2$ where $p > 1$. In network 500F of FIG. 5F, $N_2 = N$ and $N_1 = p * N$. The general symmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for unicast when $s = 1$ according to the current invention (and in the example of FIG. 5F, $s = 1$). The general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ with $(2 \times \log_d N) - 1$ stages has d_1 (where $d_1 = N_1 \times \frac{d}{N_2} = p \times d$ inlet links for each of $\frac{N_2}{d}$ input switches IS1-IS(N_2/d) (for example the links IL1-IL($p*d$) to the input switch IS1) and $d_1 (= p \times d)$ outgoing links for each of $\frac{N_2}{d}$ input switches IS1-IS(N_2/d) (for example the links ML(1,1) - ML(1,($d+p*d$)) to the input switch IS1). There are d outlet links for each of $\frac{N_2}{d}$ output switches OS1-OS(N_2/d) (for example the links OL1-OL(d) to the output switch OS1) and d incoming links for each of $\frac{N_2}{d}$ output switches OS1-OS(N_2/d) (for example ML($2 \times \log_d N_2 - 2, 1$) - ML($2 \times \log_d N_2 - 2, d$) to the output switch OS1).

Each of the $\frac{N_2}{d}$ input switches IS1 - IS(N_2/d) are connected to exactly d switches in middle stage 130 through d_1 links.

Each of the $\frac{N_2}{d}$ middle switches MS(1,1) - MS(1, N_2/d) in the middle stage 130 are connected from exactly d input switches through d_1 links and also are connected to exactly d switches in middle stage 140 through d links.

Similarly each of the $\frac{N_2}{d}$ middle switches $MS(\text{Log}_d N_2 - 1, 1)$ -
 $MS(\text{Log}_d N_2 - 1, \frac{N_2}{d})$ in the middle stage $130 + 10 * (\text{Log}_d N_2 - 2)$ are connected from
 exactly d switches in middle stage $130 + 10 * (\text{Log}_d N_2 - 3)$ through d links and also are
 connected to exactly d switches in middle stage $130 + 10 * (\text{Log}_d N_2 - 1)$ through d
 5 links.

Similarly each of the $\frac{N_2}{d}$ middle switches $MS(2 * \text{Log}_d N_2 - 3, 1)$ -
 $MS(2 * \text{Log}_d N_2 - 3, \frac{N_2}{d})$ in the middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 4)$ are connected
 from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 5)$ through d links
 and also are connected to exactly d output switches in output stage 120 through d links.
 10 Each of the $\frac{N_2}{d}$ output switches OS1 – OS(N_2/d) are connected from exactly d
 switches in middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 4)$ through d links.

The general symmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be
 operated in rearrangeably nonblocking manner for unicast when $s \geq 1$ according to the
 current invention.

15 **Symmetric RNB Unicast Embodiments:**

Referring to FIG. 6A, FIG. 6B, FIG. 6C, FIG. 6D, FIG. 6E, FIG. 6F, FIG. 6G,
 FIG. 600H, FIG. 600I and FIG. 6J with exemplary symmetrical multi-stage networks
 600A, 600B, 600C, 600D, 600E, 600F, 600G, 600H, 600I, and 600J respectively with
 five stages of twenty switches for satisfying communication requests, such as setting up a
 20 telephone call or a data call, or a connection between configurable logic blocks, between
 an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown
 where input stage 110 consists of four, two by two switches IS1-IS4 and output stage 120
 consists of four, two by two switches OS1-OS4. And all the middle stages namely middle

stage 130 consists of four, two by two switches MS(1,1) - MS(1,4), middle stage 140 consists of four, two by two switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, two by two switches MS(3,1) - MS(3,4).

Such networks can be operated in rearrangeably nonblocking manner for unicast
 5 connections, because the switches in the input stage 110 are of size two by two, the switches in output stage 120 are of size two by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In all the ten embodiments of FIG. 6A to FIG. 6J the connection topology is different. That is the way the links ML(1,1) - ML(1,8), ML(2,1) - ML(2,8), ML(3,1) -
 10 ML(3,8), and ML(4,1) - ML(4,8) are connected between the respective stages is different. For example, the connection topology of the network 600A shown in FIG. 6A is known to be back to back inverse Benes connection topology; the connection topology of the network 600B shown in FIG. 6B is known to be back to back Omega connection topology; and the connection topology of the network 600C shown in FIG. 6C is
 15 hereinafter called nearest neighbor connection topology.

Even though only ten embodiments are illustrated, in general, the network $V(N, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V(N, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental
 20 property of a valid connection topology of the $V(N, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V(N, d, s)$ can be built. The ten embodiments of FIG. 6A to FIG. 6J are only three examples of network $V(N, d, s)$.

The networks 600A - 600J of FIG. 6A - FIG. 6J are also rearrangeably
 25 nonblocking for unicast according to the current invention. In one embodiment of these networks each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N}{d}$, where N is the total number of inlet links or

outlet links. The number of middle switches in each middle stage is denoted by $\frac{N}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * d$ and each output switch OS1-OS4 can be denoted in general with the notation $d * d$. Likewise, the size of each switch in any of the middle stages can be denoted as $d * d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric multi-stage network can be represented with the notation $V(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL1-IL8), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL1-IL8 as there are outlet links OL1-OL8, in a symmetrical network they are the same.

In network 600A of FIG. 6A, each of the $\frac{N}{d}$ input switches IS1 – IS4 are connected to exactly d switches in middle stage 130 through d links (for example input switch IS1 is connected to middle switches MS(1,1) and MS(1,2) through the links ML(1,1) and ML(1,2) respectively).

Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through d links (for example the links ML(1,1) and ML(1,4) are connected to the middle switch MS(1,1) from input switch IS1 and IS2 respectively) and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,3) respectively).

Similarly each of the $\frac{N}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through d links (for example the links ML(2,1) and ML(2,6) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,3) respectively) and also are connected to exactly d

switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and MS(3,3) respectively).

- Similarly each of the $\frac{N}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage
- 5 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,6) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,3) respectively) and also are connected to exactly d output switches in output stage 120 through d links (for example the links ML(4,1) and ML(4,2) are connected to output switches OS1 and OS2 respectively from middle switch
- 10 MS(3,1)).

Each of the $\frac{N}{d}$ output switches OS1 – OS4 are connected from exactly d switches in middle stage 150 through d links (for example output switch OS1 is connected from middle switches MS(3,1) and MS(3,2) through the links ML(4,1) and ML(4,4) respectively).

15 **Generalized Symmetric RNB Unicast Embodiments:**

- Network 600K of FIG. 6K is an example of general symmetrical multi-stage network $V(N, d, s)$ with $(2 \times \log_d N) - 1$ stages. The general symmetrical multi-stage network $V(N, d, s)$ can be operated in rearrangeably nonblocking manner for unicast when $s \geq 1$ according to the current invention (and in the example of FIG. 6K, $s = 1$).
- 20 The general symmetrical multi-stage network $V(N, d, s)$ with $(2 \times \log_d N) - 1$ stages has d inlet links for each of $\frac{N}{d}$ input switches IS1-IS(N/d) (for example the links IL1-IL(d) to the input switch IS1) and d outgoing links for each of $\frac{N}{d}$ input switches IS1-IS(N/d) (for example the links ML(1,1) - ML(1,d) to the input switch IS1). There are d outlet links for each of $\frac{N}{d}$ output switches OS1-OS(N/d) (for example OL1-OL(d) to the output

switch OS1) and d incoming links for each of $\frac{N}{d}$ output switches OS1-OS(N/d) (for example $ML(2 \times \text{Log}_d N - 2, 1) - ML(2 \times \text{Log}_d N - 2, d)$ to the output switch OS1).

Each of the $\frac{N}{d}$ input switches IS1 – IS(N/d) are connected to exactly d switches in middle stage 130 through d links.

- 5 Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,N/d) in the middle stage 130 are connected from exactly d input switches through d links and also are connected to exactly d switches in middle stage 140 through d links.

- Similarly each of the $\frac{N}{d}$ middle switches $MS(\text{Log}_d N - 1, 1) - MS(\text{Log}_d N - 1, \frac{N}{d})$ in the middle stage $130 + 10 * (\text{Log}_d N - 2)$ are connected from exactly d switches in
 10 middle stage $130 + 10 * (\text{Log}_d N - 3)$ through d links and also are connected to exactly d switches in middle stage $130 + 10 * (\text{Log}_d N - 1)$ through d links.

- Similarly each of the $\frac{N}{d}$ middle switches $MS(2 \times \text{Log}_d N - 3, 1) -$
 $MS(2 \times \text{Log}_d N - 3, \frac{N}{d})$ in the middle stage $130 + 10 * (2 * \text{Log}_d N - 4)$ are connected from
 exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N - 5)$ through d links and also
 15 are connected to exactly d output switches in output stage 120 through d links.

Each of the $\frac{N}{d}$ output switches OS1 – OS(N/d) are connected from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N - 4)$ through d links.

- The general symmetrical multi-stage network $V(N, d, s)$ can be operated in rearrangeably nonblocking manner for unicast when $s \geq 1$ according to the current
 20 invention.

Asymmetric RNB ($N_2 > N_1$) Unicast Embodiments:

Referring to FIG. 6A1, FIG. 6B1, FIG. 6C1, FIG. 6D1, FIG. 6E1, FIG. 6F1, FIG. 6G1, FIG. 600H1, FIG. 600I1 and FIG. 6J1 with exemplary symmetrical multi-stage networks 600A1, 600B1, 600C1, 600D1, 600E1, 600F1, 600G1, 600H1, 600I1, and 600J1 respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by two switches IS1-IS4 and output stage 120 consists of four, six by six switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, two by two switches MS(1,1) - MS(1,4), middle stage 140 consists of four, two by two switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, two by six switches MS(3,1) - MS(3,4).

Such networks can be operated in rearrangeably nonblocking manner for unicast connections, because the switches in the input stage 110 are of size two by two, the switches in output stage 120 are of size six by six, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In all the ten embodiments of FIG. 6A1 to FIG. 6J1 the connection topology is different. That is the way the links ML(1,1) - ML(1,8), ML(2,1) - ML(2,8), ML(3,1) - ML(3,8), and ML(4,1) - ML(4,8) are connected between the respective stages is different. For example, the connection topology of the network 600A1 shown in FIG. 6A1 is known to be back to back inverse Benes connection topology; the connection topology of the network 600B1 shown in FIG. 6B1 is known to be back to back Omega connection topology; and the connection topology of the network 600C1 shown in FIG. 6C1 is hereinafter called nearest neighbor connection topology.

Even though only ten embodiments are illustrated, in general, the network $V(N_1, N_2, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V(N_1, N_2, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V(N_1, N_2, d, s)$ network is, when no

connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V(N_1, N_2, d, s)$ can be built. The ten embodiments of FIG. 6A1 to FIG. 6J1 are only three examples of network $V(N_1, N_2, d, s)$.

- 5 The networks 600A1 - 600J1 of FIG. 6A1 - FIG. 6J1 are also rearrangeably nonblocking for unicast according to the current invention. In one embodiment of these networks each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_1}{d}$, where N_1 is the total number of inlet links or
- 10 and N_2 is the total number of outlet links and $N_2 > N_1$ and $N_2 = p * N_1$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_1}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * d$ and each output switch OS1-OS4 can be denoted in general with the notation $d_2 * d_2$, where
- $$d_2 = N_2 \times \frac{d}{N_1} = p \times d .$$
- 15 The size of each switch in any of the middle stages excepting the last middle stage can be denoted as $d * d$. The size of each switch in the last middle stage can be denoted as $d * d_2$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-stage network can be represented with the notation $V(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches
- 20 (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL24), d represents the inlet links of each input switch where $N_2 > N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

- In network 600A1 of FIG. 6A1, each of the $\frac{N_1}{d}$ input switches IS1 – IS4 are
- 25 connected to exactly d switches in middle stage 130 through d links (for example input

switch IS1 is connected to middle switches MS(1,1) and MS(1,2) through the links ML(1,1) and ML(1,2) respectively).

Each of the $\frac{N_1}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d input switches through d links (for example the links ML(1,1) and ML(1,4) are connected to the middle switch MS(1,1) from input switch IS1 and IS2 respectively) and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,3) respectively).

Similarly each of the $\frac{N_1}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through d links (for example the links ML(2,1) and ML(2,6) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,3) respectively) and also are connected to exactly d switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and MS(3,3) respectively).

Similarly each of the $\frac{N_1}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,6) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,3) respectively) and also are connected to exactly d output switches in output stage 120 through d_2 links (for example the links ML(4,1) and ML(4,2) are connected to output switches OS1 from middle switch MS(3,1); the links ML(4,3) and ML(4,4) are connected to output switches OS2 from middle switch MS(3,1); the link ML(4,5) is connected to output switches OS3 from middle switch MS(3,1); and the link ML(4,6) is connected to output switches OS4 from middle switch MS(3,1)).

Each of the $\frac{N_1}{d}$ output switches OS1 – OS4 are connected from exactly d switches in middle stage 150 through d_2 links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1) and ML(4,2); output switch OS1 is connected from middle switch MS(3,2) through the links ML(4,7) and ML(4,8); output switch OS1 is connected from middle switch MS(3,3) through the link ML(4,13); and output switch OS1 is connected from middle switch MS(3,4) through the links ML(4,19)).

Generalized Asymmetric RNB ($N_2 > N_1$) Unicast Embodiments:

Network 600K1 of FIG. 6K1 is an example of general asymmetrical multi-stage network $V(N_1, N_2, d, s)$ with $(2 \times \log_d N) - 1$ stages where $N_2 > N_1$ and $N_2 = p * N_1$ where $p > 1$. In network 400K1 of FIG. 4K1, $N_1 = N$ and $N_2 = p * N$. The general symmetrical multi-stage network $V(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for unicast when $s \geq 1$ according to the current invention (and in the example of FIG. 6K1, $s = 1$). The general asymmetrical multi-stage network $V(N_1, N_2, d, s)$ with $(2 \times \log_d N) - 1$ stages has d inlet links for each of $\frac{N_1}{d}$ input switches IS1-IS(N_1/d) (for example the links IL1-IL(d) to the input switch IS1) and d outgoing links for each of $\frac{N_1}{d}$ input switches IS1-IS(N_1/d) (for example the links ML(1,1) - ML(1, d) to the input switch IS1). There are d_2 (where $d_2 = N_2 \times \frac{d}{N_1} = p \times d$) outlet links for each of $\frac{N_1}{d}$ output switches OS1-OS(N_1/d) (for example the links OL1-OL($p \times d$) to the output switch OS1) and d_2 ($= p \times d$) incoming links for each of $\frac{N_1}{d}$ output switches OS1-OS(N_1/d) (for example $ML(2 \times \log_d N_1 - 2, 1)$ - $ML(2 \times \log_d N_1 - 2, d_2)$ to the output switch OS1).

Each of the $\frac{N_1}{d}$ input switches IS1 – IS(N_1/d) are connected to exactly d switches in middle stage 130 through d links.

Each of the $\frac{N_1}{d}$ middle switches MS(1,1) – MS(1, N_1/d) in the middle stage 130 are connected from exactly d input switches through d links and also are connected to exactly d switches in middle stage 140 through d links.

Similarly each of the $\frac{N_1}{d}$ middle switches $MS(\text{Log}_d N_1 - 1, 1)$ - $MS(\text{Log}_d N_1 - 1, \frac{N_1}{d})$ in the middle stage $130 + 10 * (\text{Log}_d N_1 - 2)$ are connected from exactly d switches in middle stage $130 + 10 * (\text{Log}_d N_1 - 3)$ through d links and also are connected to exactly d switches in middle stage $130 + 10 * (\text{Log}_d N_1 - 1)$ through d links.

Similarly each of the $\frac{N_1}{d}$ middle switches $MS(2 * \text{Log}_d N_1 - 3, 1)$ - $MS(2 * \text{Log}_d N_1 - 3, \frac{N_1}{d})$ in the middle stage $130 + 10 * (2 * \text{Log}_d N_1 - 4)$ are connected from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N_1 - 5)$ through d links and also are connected to exactly d output switches in output stage 120 through d_2 links.

Each of the $\frac{N_1}{d}$ output switches OS1 – OS(N_1/d) are connected from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N - 4)$ through d_2 links.

The general symmetrical multi-stage network $V(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s = 1$ according to the current invention.

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Asymmetric RNB ($N_1 > N_2$) Unicast Embodiments:

Referring to FIG. 6A2, FIG. 6B2, FIG. 6C2, FIG. 6D2, FIG. 6E2, FIG. 6F2, FIG. 6G2, FIG. 600H2, FIG. 600I2 and FIG. 6J2 with exemplary symmetrical multi-stage networks 600A2, 600B2, 600C2, 600D2, 600E2, 600F2, 600G2, 600H2, 600I2, and 600J2 respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, six by six switches IS1-IS4 and output stage 120 consists of four, two by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, six by two switches MS(1,1) - MS(1,4), middle stage 140 consists of four, two by two switches MS(2,1) - MS(2,4), and middle stage 150 consists of four, two by two switches MS(3,1) - MS(3,4).

Such networks can be operated in rearrangeably nonblocking manner for unicast connections, because the switches in the input stage 110 are of size six by six, the switches in output stage 120 are of size two by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In all the ten embodiments of FIG. 6A2 to FIG. 6J2 the connection topology is different. That is the way the links ML(1,1) - ML(1,8), ML(2,1) - ML(2,8), ML(3,1) - ML(3,8), and ML(4,1) - ML(4,8) are connected between the respective stages is different. For example, the connection topology of the network 600A2 shown in FIG. 6A2 is known to be back to back inverse Benes connection topology; the connection topology of the network 600B2 shown in FIG. 6B2 is known to be back to back Omega connection topology; and the connection topology of the network 600C2 shown in FIG. 6C2 is hereinafter called nearest neighbor connection topology.

Even though only ten embodiments are illustrated, in general, the network $V(N_1, N_2, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V(N_1, N_2, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V(N_1, N_2, d, s)$ network is, when no

connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V(N_1, N_2, d, s)$ can be built. The ten embodiments of FIG. 6A2 to FIG. 6J2 are only three examples of network $V(N_1, N_2, d, s)$.

- 5 The networks 600A2 - 600J2 of FIG. 6A2 - FIG. 6J2 are also rearrangeably nonblocking for unicast according to the current invention. In one embodiment of these networks each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N_2}{d}$, where N_1 is the total number of inlet links or
- 10 and N_2 is the total number of outlet links and $N_1 > N_2$ and $N_1 = p * N_2$ where $p > 1$. The number of middle switches in each middle stage is denoted by $\frac{N_2}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d_1 * d_1$ and each output switch OS1-OS4 can be denoted in general with the notation $(d * d)$, where
- $$d_1 = N_1 \times \frac{d}{N_2} = p \times d.$$
- 15 The size of each switch in any of the middle stages excepting the first middle stage can be denoted as $d * d$. The size of each switch in the first middle stage can be denoted as $d_1 * d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-stage network can be represented with the notation $V(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches
- 20 (for example the links IL1-IL24), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL8), d represents the inlet links of each output switch where $N_1 > N_2$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

- In network 600A2 of FIG. 6A2, each of the $\frac{N_2}{d}$ input switches IS1 - IS4 are
- 25 connected to exactly d switches in middle stage 130 through d_1 links (for example input

switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1) and ML(1,2); input switch IS1 is connected to middle switch MS(1,2) through the links ML(1,3) and ML(1,4); input switch IS1 is connected to middle switch MS(1,3) through the link ML(1,5); and input switch IS1 is connected to middle switch MS(1,4) through the links ML(1,6)).

Each of the $\frac{N_2}{d}$ middle switches MS(1,1) – MS(1,4) in the middle stage 130 are connected from exactly d_1 input switches through d links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1; the links ML(1,7) and ML(1,8) are connected to the middle switch MS(1,1) from input switch IS2; the link ML(1,13) is connected to the middle switch MS(1,1) from input switch IS3; and the link ML(1,19) is connected to the middle switch MS(1,1) from input switch IS4), and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,3) respectively).

Similarly each of the $\frac{N_1}{d}$ middle switches MS(2,1) – MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through d links (for example the links ML(2,1) and ML(2,6) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,3) respectively) and also are connected to exactly d switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and MS(3,3) respectively).

Similarly each of the $\frac{N_1}{d}$ middle switches MS(3,1) – MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,6) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,3) respectively) and also are connected to exactly d output switches in output stage 120 through d_2 links (for example the links ML(4,1) and

ML(4,2) are connected to output switches OS1 and OS2 respectively from middle switch MS(3,1)).

Each of the $\frac{N_1}{d}$ output switches OS1 – OS4 are connected from exactly d switches in middle stage 150 through d_2 links (for example output switch OS1 is
 5 connected from middle switches MS(3,1) and MS(3,2) through the links ML(4,1) and ML(4,4) respectively).

Generalized Asymmetric RNB ($N_1 > N_2$) Unicast Embodiments:

Network 600K2 of FIG. 6K2 is an example of general asymmetrical multi-stage network $V(N_1, N_2, d, s)$ with $(2 \times \log_d N) - 1$ stages where $N_1 > N_2$ and $N_1 = p * N_2$
 10 where $p > 1$. In network 400K2 of FIG. 4K2, $N_2 = N$ and $N_1 = p * N$.. The general symmetrical multi-stage network $V(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for unicast when $s \geq 1$ according to the current invention (and in the example of FIG. 6K2, $s = 1$). The general asymmetrical multi-stage network

$V(N_1, N_2, d, s)$ with $(2 \times \log_d N) - 1$ stages has d_1 (where $d_1 = N_1 \times \frac{d}{N_2} = p \times d$ inlet
 15 links for each of $\frac{N_2}{d}$ input switches IS1-IS(N_2/d) (for example the links IL1-IL($p*d$) to

the input switch IS1) and $d_1 (= p \times d)$ outgoing links for each of $\frac{N_2}{d}$ input switches IS1-IS(N_2/d) (for example the links ML(1,1) - ML(1,($d+p*d$)) to the input switch IS1).

There are d outlet links for each of $\frac{N_2}{d}$ output switches OS1-OS(N_2/d) (for example the links OL1-OL(d) to the output switch OS1) and d incoming links for each of $\frac{N_2}{d}$ output
 20 switches OS1-OS(N_2/d) (for example $ML(2 \times \text{Log}_d N_2 - 2, 1) - ML(2 \times \text{Log}_d N_2 - 2, d)$ to the output switch OS1).

Each of the $\frac{N_2}{d}$ input switches IS1 – IS(N_2/d) are connected to exactly d switches in middle stage 130 through d_1 links.

Each of the $\frac{N_2}{d}$ middle switches MS(1,1) – MS(1, N_2/d) in the middle stage 130 are connected from exactly d input switches through d_1 links and also are connected to exactly d switches in middle stage 140 through d links.

Similarly each of the $\frac{N_2}{d}$ middle switches $MS(\text{Log}_d N_2 - 1, 1)$ - $MS(\text{Log}_d N_2 - 1, \frac{N_2}{d})$ in the middle stage $130 + 10 * (\text{Log}_d N_2 - 2)$ are connected from exactly d switches in middle stage $130 + 10 * (\text{Log}_d N_2 - 3)$ through d links and also are connected to exactly d switches in middle stage $130 + 10 * (\text{Log}_d N_2 - 1)$ through d links.

Similarly each of the $\frac{N_2}{d}$ middle switches $MS(2 * \text{Log}_d N_2 - 3, 1)$ - $MS(2 * \text{Log}_d N_2 - 3, \frac{N_2}{d})$ in the middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 4)$ are connected from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 5)$ through d links and also are connected to exactly d output switches in output stage 120 through d links.

Each of the $\frac{N_2}{d}$ output switches OS1 – OS(N_2/d) are connected from exactly d switches in middle stage $130 + 10 * (2 * \text{Log}_d N_2 - 4)$ through d links.

The general symmetrical multi-stage network $V(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for unicast when $s \geq 1$ according to the current invention.

Scheduling Method Embodiments:

FIG. 7A shows a high-level flowchart of a scheduling method 1000, in one embodiment executed to setup multicast and unicast connections in network 100A of FIG. 1A (or any of the networks $V_{mlink}(N_1, N_2, d, s)$ and the networks $V(N_1, N_2, d, s)$ disclosed in this invention). According to this embodiment, a multicast connection request is received in act 1010. Then the control goes to act 1020.

In act 1020, based on the inlet link and input switch of the multicast connection received in act 1010, from each available outgoing middle link of the input switch of the multicast connection, by traveling forward from middle stage 130 to middle stage $130+10*(\text{Log}_d N - 2)$, the lists of all reachable middle switches in each middle stage are derived recursively. That is, first, by following each available outgoing middle link of the input switch all the reachable middle switches in middle stage 130 are derived. Next, starting from the selected middle switches in middle stage 130 traveling through all of their available outgoing middle links to middle stage 140 all the available middle switches in middle stage 140 are derived. This process is repeated recursively until all the reachable middle switches, starting from the outgoing middle link of input switch, in middle stage $130+10*(\text{Log}_d N - 2)$ are derived. This process is repeated for each available outgoing middle link from the input switch of the multicast connection and separate reachable lists are derived in each middle stage from middle stage 130 to middle stage $130+10*(\text{Log}_d N - 2)$ for all the available outgoing middle links from the input switch. Then the control goes to act 1030.

In act 1030, based on the destinations of the multicast connection received in act 1010, from the output switch of each destination, by traveling backward from output stage 120 to middle stage $130+10*(\text{Log}_d N - 2)$, the lists of all middle switches in each middle stage from which each destination output switch (and hence the destination outlet links) is reachable, are derived recursively. That is, first, by following each available incoming middle link of the output switch of each destination link of the multicast connection, all the middle switches in middle stage $130+10*(2*\text{Log}_d N - 4)$ from which the output switch is reachable, are derived. Next, starting from the selected middle

switches in middle stage $130+10*(2*Log_dN-4)$ traveling backward through all of their available incoming middle links from middle stage $130+10*(2*Log_dN-5)$ all the available middle switches in middle stage $130+10*(2*Log_dN-5)$ from which the output switch is reachable, are derived. This process is repeated recursively until all the middle switches in middle stage $130+10*(Log_dN-2)$ from which the output switch is reachable, are derived. This process is repeated for each output switch of each destination link of the multicast connection and separate lists in each middle stage from middle stage $130+10*(2*Log_dN-4)$ to middle stage $130+10*(Log_dN-2)$ for all the output switches of each destination link of the connection are derived. Then the control goes to act 1040.

In act 1040, using the lists generated in acts 1020 and 1030, particularly list of middle switches derived in middle stage $130+10*(Log_dN-2)$ corresponding to each outgoing link of the input switch of the multicast connection, and the list of middle switches derived in middle stage $130+10*(Log_dN-2)$ corresponding to each output switch of the destination links, the list of all the reachable destination links from each outgoing link of the input switch are derived. Specifically if a middle switch in middle stage $130+10*(Log_dN-2)$ is reachable from an outgoing link of the input switch, say “x”, and also from the same middle switch in middle stage $130+10*(Log_dN-2)$ if the output switch of a destination link, say “y”, is reachable then using the outgoing link of the input switch x, destination link y is reachable. Accordingly, the list of all the reachable destination links from each outgoing link of the input switch is derived. The control then goes to act 1050.

In act 1050, among all the outgoing links of the input switch, it is checked if all the destinations are reachable using only one outgoing link of the input switch. If one outgoing link is available through which all the destinations of the multicast connection are reachable (i.e., act 1050 results in “yes”), the control goes to act 1070. And in act 1070, the multicast connection is setup by traversing from the selected only one outgoing middle link of the input switch in act 1050, to all the destinations. Then the control transfers to act 1090.

If act 1050 results “no”, that is one outgoing link is not available through which all the destinations of the multicast connection are reachable, then the control goes to act 1060. In act 1060, it is checked if all destination links of the multicast connection are reachable using two outgoing middle links from the input switch. According to the
 5 current invention, it is always possible to find at most two outgoing middle links from the input switch through which all the destinations of a multicast connection are reachable. So act 1060 always results in “yes”, and then the control transfers to act 1080. In act 1080, the multicast connection is setup by traversing from the selected only two outgoing middle links of the input switch in act 1060, to all the destinations. Then the control
 10 transfers to act 1090.

In act 1090, all the middle links between any two stages of the network used to setup the connection in either act 1070 or act 1080 are marked unavailable so that these middle links will be made unavailable to other multicast connections. The control then returns to act 1010, so that acts 1010, 1020, 1030, 1040, 1050, 1060, 1070, 1080, and
 15 1090 are executed in a loop, for each connection request until the connections are set up.

In the example illustrated in FIG. 1A, four outgoing middle links are available to satisfy a multicast connection request if input switch is IS2, but only at most two outgoing middle links of the input switch will be used in accordance with this method. Similarly, although three outgoing middle links is available for a multicast connection
 20 request if the input switch is IS1, again only at most two outgoing middle links is used. The specific outgoing middle links of the input switch that are chosen when selecting two outgoing middle links of the input switch is irrelevant to the method of FIG. 7A so long as at most two outgoing middle links of the input switch are selected to ensure that the connection request is satisfied, i.e. the destination switches identified by the connection
 25 request can be reached from the outgoing middle links of the input switch that are selected. In essence, limiting the outgoing middle links of the input switch to no more than two permits the network $V_{mlink}(N_1, N_2, d, s)$ and the network $V(N_1, N_2, d, s)$ to be operated in nonblocking manner in accordance with the invention.

According to the current invention, using the method 1040 of FIG. 7A, the network $V_{m\text{link}}(N_1, N_2, d, s)$ and the networks $V(N_1, N_2, d, s)$ are operated in rearrangeably nonblocking for unicast connections when $s \geq 1$, are operated in strictly nonblocking for unicast connections when $s \geq 2$, and are operated in rearrangeably
 5 nonblocking for multicast connections when $s \geq 2$.

The connection request of the type described above in reference to method 1000 of FIG. 7A can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, only one outgoing middle link of the input switch is used to satisfy the request.
 10 Moreover, in method 1000 described above in reference to FIG. 7A any number of middle links may be used between any two stages excepting between the input stage and middle stage 130, and also any arbitrary fan-out may be used within each output stage switch, to satisfy the connection request.

As noted above method 1000 of FIG. 7A can be used to setup multicast
 15 connections, unicast connections, or broadcast connection of all the networks $V_{m\text{link}}(N, d, s)$, $V_{m\text{link}}(N_1, N_2, d, s)$, $V(N, d, s)$ and $V(N_1, N_2, d, s)$ disclosed in this invention.

Applications Embodiments:

20 All the embodiments disclosed in the current invention are useful in many varieties of applications. FIG. 8A1 illustrates the diagram of 800A1 which is a typical two by two switch with two inlet links namely IL1 and IL2, and two outlet links namely OL1 and OL2. The two by two switch also implements four crosspoints namely CP(1,1), CP(1,2), CP(2,1) and CP(2,2) as illustrated in FIG. 8A1. For example the diagram of
 25 800A1 may the implementation of middle switch MS(1,1) of the diagram 400A of FIG. 4A where inlet link IL1 of diagram 800A1 corresponds to middle link ML(1,1) of diagram 400A, inlet link IL2 of diagram 800A1 corresponds to middle link ML(1,5) of diagram 400A, outlet link OL1 of diagram 800A1 corresponds to middle link ML(2,1) of

diagram 400A, outlet link OL2 of diagram 800A1 corresponds to middle link ML(2,2) of diagram 400A.

1) Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in
5 programmable integrated circuit applications. FIG. 8A2 illustrates the detailed diagram
800A2 for the implementation of the diagram 800A1 in programmable integrated circuit
embodiments. Each crosspoint is implemented by a transistor coupled between the
corresponding inlet link and outlet link, and a programmable cell in programmable
integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by
10 transistor C(1,1) coupled between inlet link IL1 and outlet link OL1, and programmable
cell P(1,1); crosspoint CP(1,2) is implemented by transistor C(1,2) coupled between inlet
link IL1 and outlet link OL2, and programmable cell P(1,2); crosspoint CP(2,1) is
implemented by transistor C(2,1) coupled between inlet link IL2 and outlet link OL1, and
programmable cell P(2,1); and crosspoint CP(2,2) is implemented by transistor C(2,2)
15 coupled between inlet link IL2 and outlet link OL2, and programmable cell P(2,2).

If the programmable cell is programmed ON, the corresponding transistor couples
the corresponding inlet link and outlet link. If the programmable cell is programmed
OFF, the corresponding inlet link and outlet link are not connected. For example if the
programmable cell P(1,1) is programmed ON, the corresponding transistor C(1,1) couples
20 the corresponding inlet link IL1 and outlet link OL1. If the programmable cell P(1,1) is
programmed OFF, the corresponding inlet link IL1 and outlet link OL1 are not
connected. In volatile programmable integrated circuit embodiments the programmable
cell may be an SRAM (Static Random Address Memory) cell. In non-volatile
programmable integrated circuit embodiments the programmable cell may be a Flash
25 memory cell. Also the programmable integrated circuit embodiments may implement
field programmable logic arrays (FPGA) devices, or programmable Logic devices (PLD),
or Application Specific Integrated Circuits (ASIC) embedded with programmable logic
circuits or 3D-FPGAs.

2) One-time Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in one-time programmable integrated circuit applications. FIG. 8A3 illustrates the detailed diagram 800A3 for the implementation of the diagram 800A1 in one-time programmable
5 integrated circuit embodiments. Each crosspoint is implemented by a via coupled between the corresponding inlet link and outlet link in one-time programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by via V(1,1) coupled between inlet link IL1 and outlet link OL1; crosspoint CP(1,2) is implemented by via V(1,2) coupled between inlet link IL1 and outlet link OL2; crosspoint CP(2,1) is
10 implemented by via V(2,1) coupled between inlet link IL2 and outlet link OL1; and crosspoint CP(2,2) is implemented by via V(2,2) coupled between inlet link IL2 and outlet link OL2.

If the via is programmed ON, the corresponding inlet link and outlet link are permanently connected which is denoted by thick circle at the intersection of inlet link
15 and outlet link. If the via is programmed OFF, the corresponding inlet link and outlet link are not connected which is denoted by the absence of thick circle at the intersection of inlet link and outlet link. For example in the diagram 800A3 the via V(1,1) is programmed ON, and the corresponding inlet link IL1 and outlet link OL1 are connected as denoted by thick circle at the intersection of inlet link IL1 and outlet link OL1; the via
20 V(2,2) is programmed ON, and the corresponding inlet link IL2 and outlet link OL2 are connected as denoted by thick circle at the intersection of inlet link IL2 and outlet link OL2; the via V(1,2) is programmed OFF, and the corresponding inlet link IL1 and outlet link OL2 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL1 and outlet link OL2; the via V(2,1) is programmed OFF, and the
25 corresponding inlet link IL2 and outlet link OL1 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL2 and outlet link OL1. One-time programmable integrated circuit embodiments may be anti-fuse based programmable integrated circuit devices or mask programmable structured ASIC devices.

3) Integrated Circuit Placement and Route Embodiments:

All the embodiments disclosed in the current invention are useful in Integrated Circuit Placement and Route applications, for example in ASIC backend Placement and Route tools. FIG. 8A4 illustrates the detailed diagram 800A4 for the implementation of the diagram 800A1 in Integrated Circuit Placement and Route embodiments. In an
 5 integrated circuit since the connections are known a-priori, the switch and crosspoints are actually virtual. However the concept of virtual switch and virtual crosspoint using the embodiments disclosed in the current invention reduces the number of required wires, wire length needed to connect the inputs and outputs of different netlists and the time
 10 required by the tool for placement and route of netlists in the integrated circuit.

Each virtual crosspoint is used to either to hardwire or provide no connectivity between the corresponding inlet link and outlet link. Specifically crosspoint CP(1,1) is implemented by direct connect point DCP(1,1) to hardwire (i.e., to permanently connect) inlet link IL1 and outlet link OL1 which is denoted by the thick circle at the intersection
 15 of inlet link IL1 and outlet link OL1; crosspoint CP(2,2) is implemented by direct connect point DCP(2,2) to hardwire inlet link IL2 and outlet link OL2 which is denoted by the thick circle at the intersection of inlet link IL2 and outlet link OL2. The diagram 800A4 does not show direct connect point DCP(1,2) and direct connect point DCP(1,3) since they are not needed and in the hardware implementation they are eliminated.
 20 Alternatively inlet link IL1 needs to be connected to outlet link OL1 and inlet link IL1 does not need to be connected to outlet link OL2. Also inlet link IL2 needs to be connected to outlet link OL2 and inlet link IL2 does not need to be connected to outlet link OL1. Furthermore in the example of the diagram 800A4, there is no need to drive the signal of inlet link IL1 horizontally beyond outlet link OL1 and hence the inlet link IL1 is
 25 not even extended horizontally until the outlet link OL2. Also the absence of direct connect point DCP(2,1) illustrates there is no need to connect inlet link IL2 and outlet link OL1.

In summary in integrated circuit placement and route tools, the concept of virtual switches and virtual cross points is used during the implementation of the placement &
 30 routing algorithmically in software, however during the hardware implementation cross

points in the cross state are implemented as hardwired connections between the corresponding inlet link and outlet link, and in the bar state are implemented as no connection between inlet link and outlet link.

3) More Application Embodiments:

5 All the embodiments disclosed in the current invention are also useful in the design of SoC interconnects, Field programmable interconnect chips, parallel computer systems and in time-space-time switches.

 Numerous modifications and adaptations of the embodiments, implementations, and examples described herein will be apparent to the skilled artisan in view of the
10 disclosure.

CLAIMS

What is claimed is:

1. A network having a plurality of multicast connections, said network comprising:
 - N_1 inlet links and N_2 outlet links, and
 - 5 when $N_2 > N_1$ and $N_2 = p * N_1$ where $p > 1$ then $N_1 = N$, $d_1 = d$, and

$$d_2 = N_2 \times \frac{d}{N_1} = p \times d$$
; and
 - an input stage comprising $\frac{N_1}{d}$ input switches, and each input switch comprising d inlet links and each said input switch further comprising $x \times d$ outgoing links connecting to switches in a second stage where $x > 0$; and
 - 10 an output stage comprising $\frac{N_1}{d}$ output switches, and each output switch comprising d_2 outlet links and each said output switch further comprising $x \times \frac{(d + d_2)}{2}$ incoming links connecting from switches in the penultimate stage; and
 - a plurality of y middle stages comprising $\frac{N}{d}$ middle switches in each of said y middle stages wherein said second stage and said penultimate stage are one of said
 - 15 middle stages where $y > 3$, and
 - each middle switch in all said middle stages excepting said penultimate stage comprising $x \times d$ incoming links (hereinafter "incoming middle links") connecting from switches in its immediate preceding stage, and each middle switch further comprising $x \times d$ outgoing links (hereinafter "outgoing middle links") connecting to
 - 20 switches in its immediate succeeding stage; and
 - each middle switch in said penultimate stage comprising $x \times d$ incoming links connecting from switches in its immediate preceding stage, and each middle switch further comprising $x \times \frac{(d + d_2)}{2}$ outgoing links connecting to switches in its immediate succeeding stage i.e., said output stage; or

when $N_1 > N_2$ and $N_1 = p * N_2$ where $p > 1$ then $N_2 = N$, $d_2 = d$ and

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d \text{ and}$$

an input stage comprising $\frac{N_2}{d}$ input switches, and each input switch comprising

d_1 inlet links and each input switch further comprising $x \times \frac{(d + d_1)}{2}$ outgoing links

5 connecting to switches in a second stage where $x > 0$; and

an output stage comprising $\frac{N_2}{d}$ output switches, and each output switch

comprising d outlet links and each output switch further comprising $x \times d$ incoming links connecting from switches in the penultimate stage; and

a plurality of y middle stages comprising $\frac{N}{d}$ middle switches in each of said y

10 middle stages wherein said second stage and said penultimate stage are one of said middle stages where $y > 3$, and

each middle switch in said second stage comprising $x \times \frac{(d + d_1)}{2}$ incoming links

connecting from switches in its immediate preceding stage i.e., said input stage, and each middle switch further comprising $x \times d$ outgoing links connecting to switches in its

15 immediate succeeding stage; and

each middle switch in all said middle stages excepting said second stage comprising $x \times d$ incoming links (hereinafter “incoming middle links”) connecting from switches in its immediate preceding stage, and each middle switch further comprising $x \times d$ outgoing links (hereinafter “outgoing middle links”) connecting to

20 switches in its immediate succeeding stage; and

wherein each multicast connection from an inlet link passes through at most two outgoing links in input switch, and said multicast connection further passes through a plurality of outgoing links in a plurality switches in each said middle stage and in said output stage.

2. The network of claim 1, wherein all said incoming middle links and outgoing middle links are connected in any arbitrary topology such that when no connections are setup in said network, a connection from any said inlet link to any said outlet link can be setup.
- 5 3. The network of claim 2, wherein $y \geq (2 \times \log_d N_1) - 3$ when $N_2 > N_1$, and $y \geq (2 \times \log_d N_2) - 3$ when $N_1 > N_2$.
4. The network of claim 3, wherein $x \geq 1$, wherein said each multicast connection comprises only one destination link, and
said each multicast connection from an inlet link passes through only one
10 outgoing link in input switch, and said multicast connection further passes through only one outgoing link in one of the switches in each said middle stage and in said output stage, and
further is always capable of setting up said multicast connection by changing the path, defined by passage of an existing multicast connection, thereby to change only one
15 outgoing link of the input switch used by said existing multicast connection, and said network is hereinafter "rearrangeably nonblocking network for unicast".
5. The network of claim 3, wherein $x \geq 2$, wherein said each multicast connection comprises only one destination link, and
said each multicast connection from an inlet link passes through only one
20 outgoing link in input switch, and said multicast connection further passes through only one outgoing link in one of the switches in each said middle stage and in said output stage, and
further is always capable of setting up said multicast connection by never
changing path of an existing multicast connection, wherein said each multicast
25 connection comprises only one destination link and the network is hereinafter "strictly nonblocking network for unicast".
6. The network of claim 3, wherein $x \geq 2$,

further is always capable of setting up said multicast connection by changing the path, defined by passage of an existing multicast connection, thereby to change one or two outgoing links of the input switch used by said existing multicast connection, and said network is hereinafter “rearrangeably nonblocking network”.

- 5 7. The network of claim 3, wherein $x \geq 3$,
further is always capable of setting up said multicast connection by never changing path of an existing multicast connection, and the network is hereinafter “strictly nonblocking network”.
8. The network of claim 1, further comprising a controller coupled to each of said
10 input, output and middle stages to set up said multicast connection.
9. The network of claim 1, wherein said N_1 inlet links and N_2 outlet links are the same number of links, i.e., $N_1 = N_2 = N$, and $d_1 = d_2 = d$.
10. The network of claim 1, wherein said each input switch, said each output switch and said each middle switch is either fully populated or partially populated.
- 15 11. The network of claim 1,
wherein each of said input switches, or each of said output switches, or each of said middle switches further recursively comprise one or more networks.
12. A method for setting up one or more multicast connections in a network having
 N_1 inlet links and N_2 outlet links, and
20 when $N_2 > N_1$ and $N_2 = p * N_1$ where $p > 1$ then $N_1 = N$, $d_1 = d$, and
$$d_2 = N_2 \times \frac{d}{N_1} = p \times d$$
; and having
an input stage having $\frac{N_1}{d}$ input switches, and each input switch having d inlet links and each input switch further having $x \times d$ outgoing links connected to switches in a second stage where $x > 0$; and

- an output stage having $\frac{N_1}{d}$ output switches, and each output switch having d_2 outlet links and each output switch further having $x \times \frac{(d + d_2)}{2}$ incoming links connected from switches in the penultimate stage; and
- a plurality of y middle stages having $\frac{N}{d}$ middle switches in each of said y middle stages wherein said second stage and said penultimate stage being one of said middle stages where $y > 3$, and
- each middle switch in all said middle stages excepting said penultimate stage having $x \times d$ incoming links connected from switches in its immediate preceding stage, and each middle switch further having $x \times d$ outgoing links connected to switches in its immediate succeeding stage; and
- each middle switch in said penultimate stage having $x \times d$ incoming links connected from switches in its immediate preceding stage, and each middle switch further having $x \times \frac{(d + d_2)}{2}$ outgoing links connected to switches in its immediate succeeding stage; or
- when $N_1 > N_2$ and $N_1 = p * N_2$ where $p > 1$ then $N_2 = N$, $d_2 = d$ and $d_1 = N_1 \times \frac{d}{N_2} = p \times d$; and having
- an input stage having $\frac{N_2}{d}$ input switches, and each input switch having d_1 inlet links and each input switch further having $x \times \frac{(d + d_1)}{2}$ outgoing links connected to switches in a second stage where $x > 0$; and
- an output stage having $\frac{N_2}{d}$ output switches, and each output switch having d outlet links and each output switch further having $x \times d$ incoming links connected from switches in the penultimate stage; and

a plurality of y middle stages having $\frac{N}{d}$ middle switches in each of said y middle stages wherein said second stage and said penultimate stage being one of said middle stages where $y > 3$, and

each middle switch in said second stage having $x \times \frac{(d + d_1)}{2}$ incoming links

- 5 connected from switches in its immediate preceding stage, and each middle switch further having $x \times d$ outgoing links connected to switches in its immediate succeeding stage; and each middle switch in all said middle stages excepting said second stage having $x \times d$ incoming links connected from switches in its immediate preceding stage, and each middle switch further having $x \times d$ outgoing links connected to switches in its immediate
- 10 succeeding stage; and said method comprising:

receiving a multicast connection at said input stage;

fanning out said multicast connection through at most two outgoing links in input switch and a plurality of outgoing links in a plurality of middle switches in each said middle stage to set up said multicast connection to a plurality of output switches among

- 15 said $\frac{N_2}{d}$ output switches, wherein said plurality of output switches are specified as destinations of said multicast connection, wherein said at most two outgoing links in input switch and said plurality of outgoing links in said plurality of middle switches in each said middle stage are available.

13. A method of claim 12 wherein said act of fanning out is performed without
- 20 changing any existing connection to pass through another set of plurality of middle switches in each said middle stage.

14. A method of claim 12 wherein said act of fanning out is performed recursively.

15. A method of claim 12 wherein a connection exists through said network and passes through a plurality of middle switches in each said middle stage and said method
- 25 further comprises:

if necessary, changing said connection to pass through another set of plurality of middle switches in each said middle stage, act hereinafter "rearranging connection".

16. A method of claim 12 wherein said acts of fanning out and rearranging are performed recursively.

5 17. A method for setting up one or more multicast connections in a network having N_1 inlet links and N_2 outlet links, and

when $N_2 > N_1$ and $N_2 = p * N_1$ where $p > 1$ then $N_1 = N$, $d_1 = d$, and

$d_2 = N_2 \times \frac{d}{N_1} = p \times d$; and having

an input stage having $\frac{N_1}{d}$ input switches, and each input switch having d inlet

10 links and each input switch further having $x \times d$ outgoing links connected to switches in a second stage where $x > 0$; and

an output stage having $\frac{N_1}{d}$ output switches, and each output switch having d_2

outlet links and each output switch further having $x \times \frac{(d + d_2)}{2}$ incoming links connected

from switches in the penultimate stage; and

15 a plurality of y middle stages having $\frac{N}{d}$ middle switches in each of said y

middle stages wherein said second stage and said penultimate stage being one of said middle stages where $y > 3$, and

each middle switch in all said middle stages excepting said penultimate stage having $x \times d$ incoming links connected from switches in its immediate preceding stage,

20 and each middle switch further having $x \times d$ outgoing links connected to switches in its immediate succeeding stage; and

each middle switch in said penultimate stage having $x \times d$ incoming links connected from switches in its immediate preceding stage, and each middle switch further

having $x \times \frac{(d + d_2)}{2}$ outgoing links connected to switches in its immediate succeeding stage; or

when $N_1 > N_2$ and $N_1 = p * N_2$ where $p > 1$ then $N_2 = N$, $d_2 = d$ and

$d_1 = N_1 \times \frac{d}{N_2} = p \times d$; and having

5 an input stage having $\frac{N_2}{d}$ input switches, and each input switch having d_1 inlet

links and each input switch further having $x \times \frac{(d + d_1)}{2}$ outgoing links connected to

switches in a second stage where $x > 0$; and

an output stage having $\frac{N_2}{d}$ output switches, and each output switch having

10 d outlet links and each output switch further having $x \times d$ incoming links connected from switches in the penultimate stage; and

a plurality of y middle stages having $\frac{N}{d}$ middle switches in each of said y

middle stages wherein said second stage and said penultimate stage being one of said middle stages where $y > 3$, and

each middle switch in said second stage having $x \times \frac{(d + d_1)}{2}$ incoming links

15 connected from switches in its immediate preceding stage, and each middle switch further having $x \times d$ outgoing links connected to switches in its immediate succeeding stage; and

each middle switch in all said middle stages excepting said second stage having $x \times d$ incoming links connected from switches in its immediate preceding stage, and each middle switch further having $x \times d$ outgoing links connected to switches in its immediate

20 succeeding stage; and said method comprising:

checking if a first outgoing link in input switch and a first plurality of outgoing links in plurality of middle switches in each said middle stage are available to at least a first subset of destination output switches of said multicast connection; and

checking if a second outgoing link in input switch and second plurality of outgoing links in plurality of middle switches in each said middle stage are available to a second subset of destination output switches of said multicast connection.

5 wherein each destination output switch of said multicast connection is one of said first subset of destination output switches and said second subset of destination output switches.

18. The method of claim 17 further comprising:

10 prior to said checkings, checking if all the destination output switches of said multicast connection are available through said first outgoing link in input switch and said first plurality of outgoing links in plurality of middle switches in each said middle stage

19. The method of claim 17 further comprising:

15 repeating said checkings of available second outgoing link in input switch and second plurality of outgoing links in plurality of middle switches in each said middle stage to a second subset of destination output switches of said multicast connection to each outgoing link in input switch other than said first and said second outgoing links in input switch.

20 wherein each destination output switch of said multicast connection is one of said first subset of destination output switches and said second subset of destination output switches.

20. The method of claim 17 further comprising:

25 repeating said checkings of available first outgoing link in input switch and first plurality of outgoing links in plurality of middle switches in each said middle stage to a first subset of destination output switches of said multicast connection to each outgoing link in input switch other than said first outgoing link in input switch.

21. The method of claim 17 further comprising:

setting up each of said multicast connection from its said input switch to its said output switches through not more than two outgoing links, selected by said checkings, by

fanning out said multicast connection in its said input switch into not more than said two outgoing links.

22. The method of claim 17 wherein any of said acts of checking and setting up are performed recursively.

5

FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS**Venkat Konda****ABSTRACT OF DISCLOSURE**

A generalized multi-link multi-stage network comprising $(2 \times \log_d N) - 1$ stages is operated in strictly nonblocking manner for unicast includes an input stage having $\frac{N}{d}$ switches with each of them having d inlet links and $2 \times d$ outgoing links connecting to second stage switches, an output stage having $\frac{N}{d}$ switches with each of them having d outlet links and $2 \times d$ incoming links connecting from switches in the penultimate stage. The network also has $(2 \times \log_d N) - 3$ middle stages with each middle stage having $\frac{N}{d}$ switches, and each switch in the middle stage has $2 \times d$ incoming links connecting from the switches in its immediate preceding stage, and $2 \times d$ outgoing links connecting to the switches in its immediate succeeding stage. Also the same generalized multi-link multi-stage network is operated in rearrangeably nonblocking manner for arbitrary fan-out multicast and each multicast connection is set up by use of at most two outgoing links from the input stage switch.

A generalized multi-link multi-stage network comprising $(2 \times \log_d N) - 1$ stages is operated in strictly nonblocking manner for multicast includes an input stage having $\frac{N}{d}$ switches with each of them having d inlet links and $3 \times d$ outgoing links connecting to second stage switches, an output stage having $\frac{N}{d}$ switches with each of them having d outlet links and $3 \times d$ incoming links connecting from switches in the penultimate stage. The network also has $(2 \times \log_d N) - 3$ middle stages with each middle stage having $\frac{N}{d}$ switches, and each switch in the middle stage has $3 \times d$ incoming links connecting from the switches in its immediate preceding stage, and $3 \times d$ outgoing links connecting to the switches in its immediate succeeding stage.

PCT

REQUEST

The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty.

For receiving Office use only

International Application No.	PCT/US08/64604
International Filing Date	22-05-2008
Name of receiving Office and "PCT International Application"	RO/US
Applicant's or agent's file reference (if desired) (12 characters maximum)	S-0039 PCT

Box No. I TITLE OF INVENTION	
FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS	
Box No. II APPLICANT <input checked="" type="checkbox"/> This person is also inventor	
Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)	Telephone No.
Venkat Konda 6278, Grand Oak Way San Jose, CA 95135	408-472-3273
	Facsimile No.
	408-238-2478
	Applicant's registration No. with the Office
State (that is, country) of nationality: USA	State (that is, country) of residence: USA
This person is applicant for the purposes of:	<input checked="" type="checkbox"/> all designated States <input type="checkbox"/> all designated States except the United States of America <input type="checkbox"/> the United States of America only <input type="checkbox"/> the States indicated in the Supplemental Box
Box No. III FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)	
<input type="checkbox"/> Further applicants and/or (further) inventors are indicated on a continuation sheet.	
Box No. IV AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE	
The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as:	<input type="checkbox"/> agent <input type="checkbox"/> common representative
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Venkat Konda 6278, Grand Oak Way San Jose, CA 95135	408-472-3273
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	408-238-2478
	Agent's registration No. with the Office
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Box No. VI PRIORITY CLAIM				
The priority of the following earlier application(s) is hereby claimed:				
	Filing date of earlier application <i>(day/month/year)</i>	Number of earlier application	Where earlier application is:	
			national application: country or Member of WTO	regional application: regional Office
item (1)	25/5/2007	60/940, 389	US	USPTO
item (2)	25/5/2007	60/940, 391	US	USPTO
item (3)	25/5/2007	60/940, 392	US	USPTO
<input type="checkbox"/> Further priority claims are indicated in the Supplemental Box.				
<p>Transmit certified copy: the receiving Office is requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) <i>(only if the earlier application was filed with the Office which for the purposes of this international application is the receiving Office)</i> identified above as:</p> <p style="text-align: center;"><input type="checkbox"/> all items <input type="checkbox"/> item (1) <input type="checkbox"/> item (2) <input type="checkbox"/> item (3) <input type="checkbox"/> other, see Supplemental Box</p>				
<p>Restore the right of priority: the receiving Office is requested to restore the right of priority for the earlier application(s) identified above or in the Supplemental Box as item(s) (_____). <i>(See also the Notes to Box No. VI: further information must be provided to support a request to restore the right of priority.)</i></p>				
<p>Incorporation by reference: where an element of the international application referred to in Article 11(1)(iii)(d) or (e) or a part of the description, claims or drawings referred to in Rule 20.5(a) is not otherwise contained in this international application but is completely contained in an earlier application whose priority is claimed on the date on which one or more elements referred to in Article 11(1)(iii) were first received by the receiving Office, that element or part is, subject to confirmation under Rule 20.6, incorporated by reference in this international application for the purposes of Rule 20.6.</p>				
Box No. VII INTERNATIONAL SEARCHING AUTHORITY				
<p>Choice of International Searching Authority (ISA) <i>(if two or more International Searching Authorities are competent to carry out the international search, indicate the Authority chosen; the two-letter code may be used):</i></p> <p>ISA / US</p>				
<p>Request to use results of earlier search; reference to that search <i>(if an earlier search has been carried out by or requested from the International Searching Authority):</i></p> <p>Date <i>(day/month/year)</i> Number Country <i>(or regional Office)</i></p>				
Box No. VIII DECLARATIONS				
<p>The following declarations are contained in Boxes Nos. VIII (i) to (v) <i>(mark the applicable check-boxes below and indicate in the right column the number of each type of declaration):</i></p>				Number of declarations
<input type="checkbox"/>	Box No. VIII (i)	Declaration as to the identity of the inventor	:	
<input type="checkbox"/>	Box No. VIII (ii)	Declaration as to the applicant's entitlement, as at the international filing date, to apply for and be granted a patent	:	
<input type="checkbox"/>	Box No. VIII (iii)	Declaration as to the applicant's entitlement, as at the international filing date, to claim the priority of the earlier application	:	
<input type="checkbox"/>	Box No. VIII (iv)	Declaration of inventorship (only for the purposes of the designation of the United States of America)	:	
<input type="checkbox"/>	Box No. VIII (v)	Declaration as to non-prejudicial disclosures or exceptions to lack of novelty	:	

Box No. IX CHECK LIST; LANGUAGE OF FILING		
<p>This international application contains:</p> <p>(a) on paper, the following number of sheets:</p> <p>request (including declaration and supplemental sheets) 3</p> <p>description (excluding sequence listing and/or tables related thereto) 211</p> <p>claims 10</p> <p>abstract 1</p> <p>drawings 125 [347]</p> <p>Sub-total number of sheets 350 [347]</p> <p>sequence listing</p> <p>tables related thereto</p> <p><i>(for both, actual number of sheets if filed on paper, whether or not also filed in electronic form; see (c) below)</i></p> <p>Total number of sheets 350 [347]</p> <p>(b) <input type="checkbox"/> only in electronic form (Section 801(a)(i))</p> <p>(i) <input type="checkbox"/> sequence listing</p> <p>(ii) <input type="checkbox"/> tables related thereto</p> <p>(c) <input type="checkbox"/> also in electronic form (Section 801(a)(ii))</p> <p>(i) <input type="checkbox"/> sequence listing</p> <p>(ii) <input type="checkbox"/> tables related thereto</p> <p>Type and number of carriers (diskette, CD-ROM, CD-R or other) on which are contained the</p> <p><input type="checkbox"/> sequence listing:</p> <p><input type="checkbox"/> tables related thereto:</p> <p><i>(additional copies to be indicated under items 9(ii) and/or 10(ii), in right column)</i></p>	<p>This international application is accompanied by the following item(s) <i>(mark the applicable check-boxes below and indicate in right column the number of each item)</i>:</p> <p>1. <input checked="" type="checkbox"/> fee calculation sheet</p> <p>2. <input type="checkbox"/> original separate power of attorney</p> <p>3. <input type="checkbox"/> original general power of attorney</p> <p>4. <input type="checkbox"/> copy of general power of attorney; reference number, if any:</p> <p>5. <input type="checkbox"/> statement explaining lack of signature</p> <p>6. <input type="checkbox"/> priority document(s) identified in Box No. VI as item(s):</p> <p>7. <input type="checkbox"/> translation of international application into <i>(language)</i>:</p> <p>8. <input type="checkbox"/> separate indications concerning deposited microorganism or other biological material</p> <p>9. <input type="checkbox"/> sequence listing in electronic form <i>(indicate type and number of carriers)</i></p> <p>(i) <input type="checkbox"/> copy submitted for the purposes of international search under Rule 13ter only (and not as part of the international application)</p> <p>(ii) <input type="checkbox"/> <i>(only where check-box (b)(i) or (c)(i) is marked in left column)</i> additional copies including, where applicable, the copy for the purposes of international search under Rule 13ter</p> <p>(iii) <input type="checkbox"/> together with relevant statement as to the identity of the copy or copies with the sequence listing mentioned in left column</p> <p>10. <input type="checkbox"/> tables in electronic form related to sequence listing <i>(indicate type and number of carriers)</i></p> <p>(i) <input type="checkbox"/> copy submitted for the purposes of international search under Section 802(b-quater) only (and not as part of the international application)</p> <p>(ii) <input type="checkbox"/> <i>(only where check-box (b)(ii) or (c)(ii) is marked in left column)</i> additional copies including, where applicable, the copy for the purposes of international search under Section 802(b-quater)</p> <p>(iii) <input type="checkbox"/> together with relevant statement as to the identity of the copy or copies with the tables mentioned in left column</p> <p>11. <input type="checkbox"/> other <i>(specify)</i>:</p>	<p>Number of items</p>
<p>Figure of the drawings which should accompany the abstract: FIG. 1A</p>	<p>Language of filing of the international application: English</p>	
<p>Box No. X SIGNATURE OF APPLICANT, AGENT OR COMMON REPRESENTATIVE <i>Next to each signature, indicate the name of the person signing and the capacity in which the person signs (if such capacity is not obvious from reading the request).</i></p>		
<p>/Venkat Konda/ applicant</p> <p>VENKAT KONDA</p>		
<p>----- For receiving Office use only -----</p>		
<p>1. Date of actual receipt of the purported international application: 22-05-2008</p>	<p>2. Drawings:</p> <p><input type="checkbox"/> received:</p> <p><input type="checkbox"/> not received:</p>	
<p>3. Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application:</p>	<p>6. <input type="checkbox"/> Transmittal of search copy delayed until search fee is paid</p>	
<p>4. Date of timely receipt of the required corrections under PCT Article 11(2):</p>	<p>5. International Searching Authority (if two or more are competent): ISA / US</p>	
<p>----- For International Bureau use only -----</p>		
<p>Date of receipt of the record copy by the International Bureau:</p>		

This sheet is not part of and does not count as a sheet of the international application.

PCT

FEE CALCULATION SHEET Annex to the Request

For receiving Office use only

International Application No. **PCT/US08/64604**

Date stamp of the receiving Office **22-05-2008**

Applicant's or agent's file reference **S-0039 PCT**

Applicant

CALCULATION OF PRESCRIBED FEES

1. TRANSMITTAL FEE **\$300.00** [T]

2. SEARCH FEE **\$1800.00** [S]

International search to be carried out by _____
(If two or more International Searching Authorities are competent to carry out the international search, indicate the name of the Authority which is chosen to carry out the international search.)

3. INTERNATIONAL FILING FEE

Where items (b) and/or (c) of Box No. IX apply, enter **Sub-total number of sheets** } _____
Where items (b) and (c) of Box No. IX do not apply, enter **Total number of sheets** }

[i1] first 30 sheets **\$1194.00** [i1]

[i2] **320** x **13** = **\$4160.00** [i2]
number of sheets in excess of 30 fee per sheet

[i3] additional component (only if a sequence listing and/or tables related thereto are filed in electronic form under Section 801(a)(i), or both in that form and on paper, under Section 801(a)(ii):
400 x _____ = _____ [i3]
fee per sheet

Add amounts entered at i1, i2 and i3 and enter total at I [I]

(Applicants from certain States are entitled to a reduction of 75% of the international filing fee. Where the applicant is (or all applicants are) so entitled, the total to be entered at I is 25% of the international filing fee.)

4. FEE FOR PRIORITY DOCUMENT (if applicable) [P]

5. TOTAL FEES PAYABLE **\$7454.00**
Add amounts entered at T, S, I and P, and enter total in the TOTAL box **TOTAL**

MODE OF PAYMENT (Not all modes of payment may be available at all receiving Offices)

- authorization to charge deposit account (see below)
- postal money order
- cash
- coupons
- cheque
- bank draft
- revenue stamps
- other (specify): **Credit Card**

AUTHORIZATION TO CHARGE (OR CREDIT) DEPOSIT ACCOUNT

(This mode of payment may not be available at all receiving Offices)

- Authorization to charge the total fees indicated above.
- (This check-box may be marked only if the conditions for deposit accounts of the receiving Office so permit) Authorization to charge any deficiency or credit any overpayment in the total fees indicated above.
- Authorization to charge the fee for priority document.

Receiving Office: RO/ _____

Deposit Account No.: _____

Date: _____

Name: _____

Signature: _____

FIG. 1A

100A

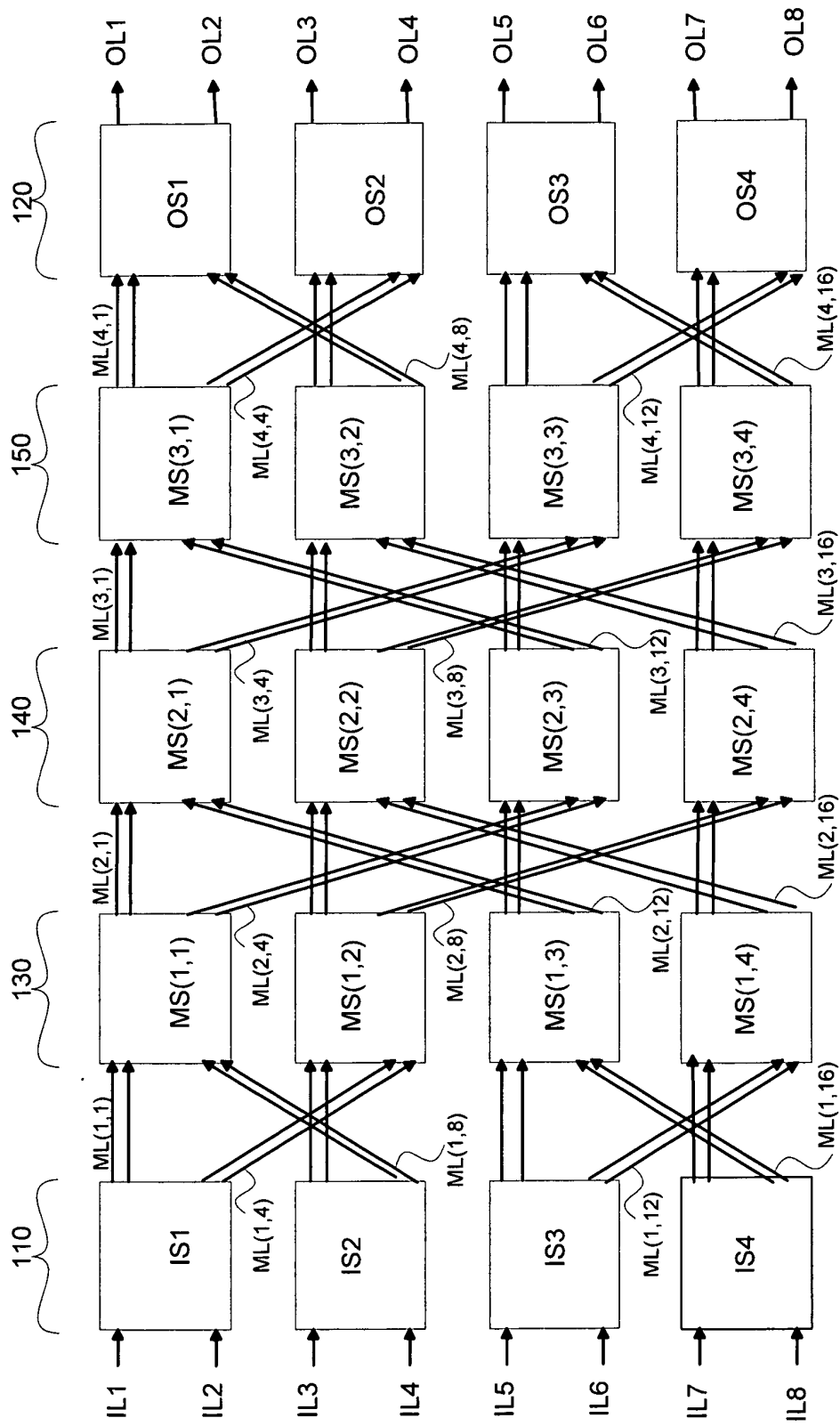


FIG. 1B

100B

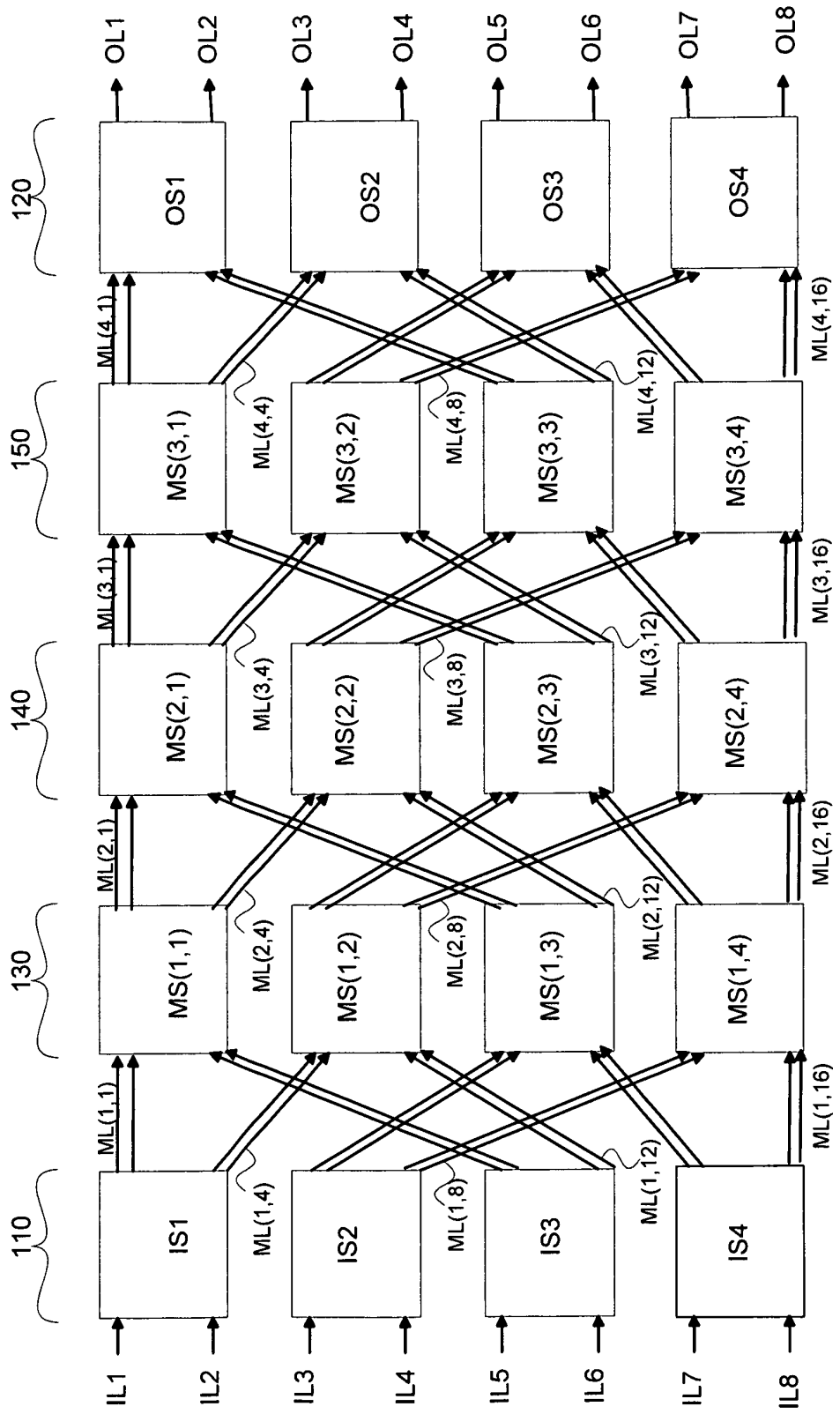


FIG. 1C

100C

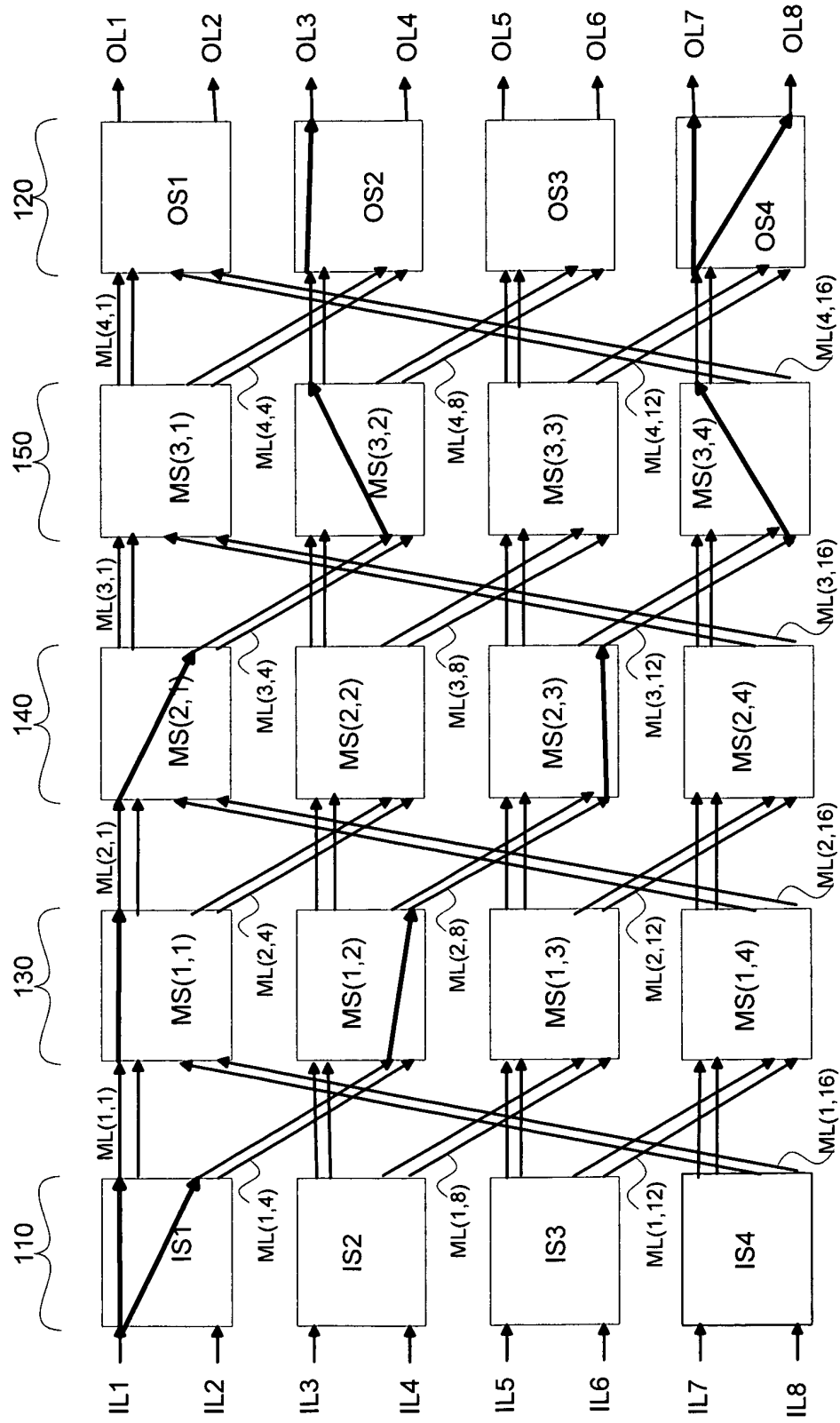


FIG. 1D

100D

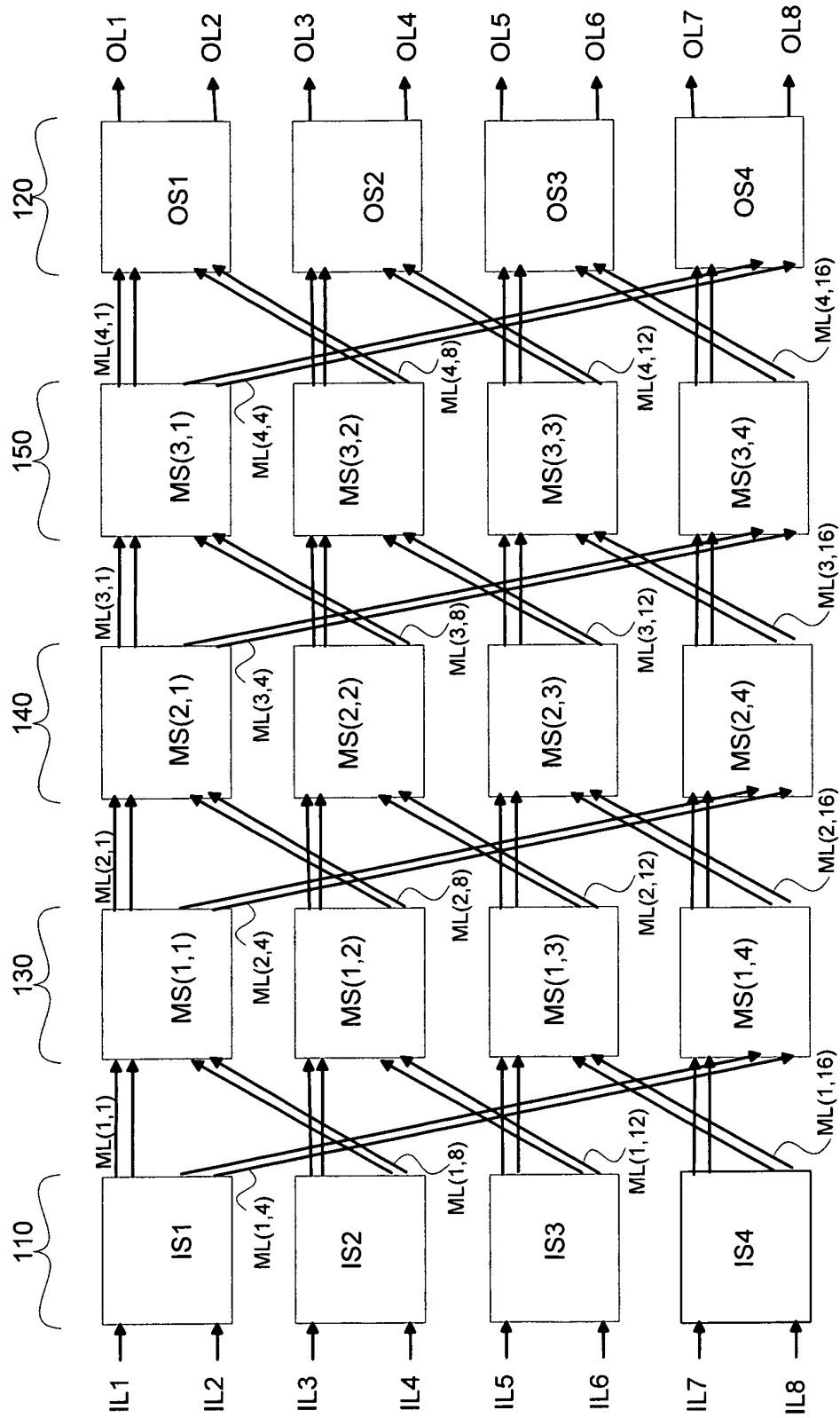


FIG. 1E

100E

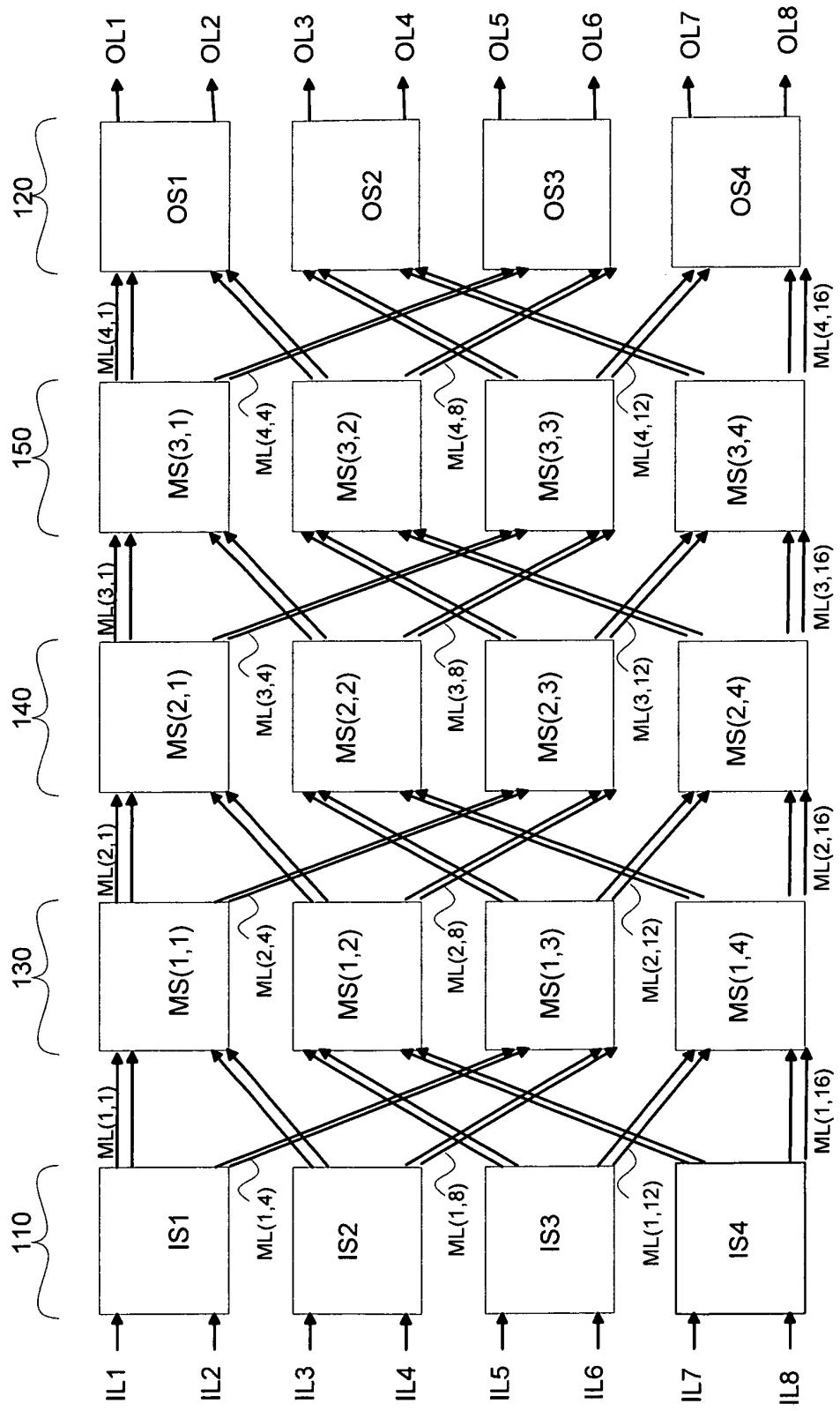


FIG. 1F

100F

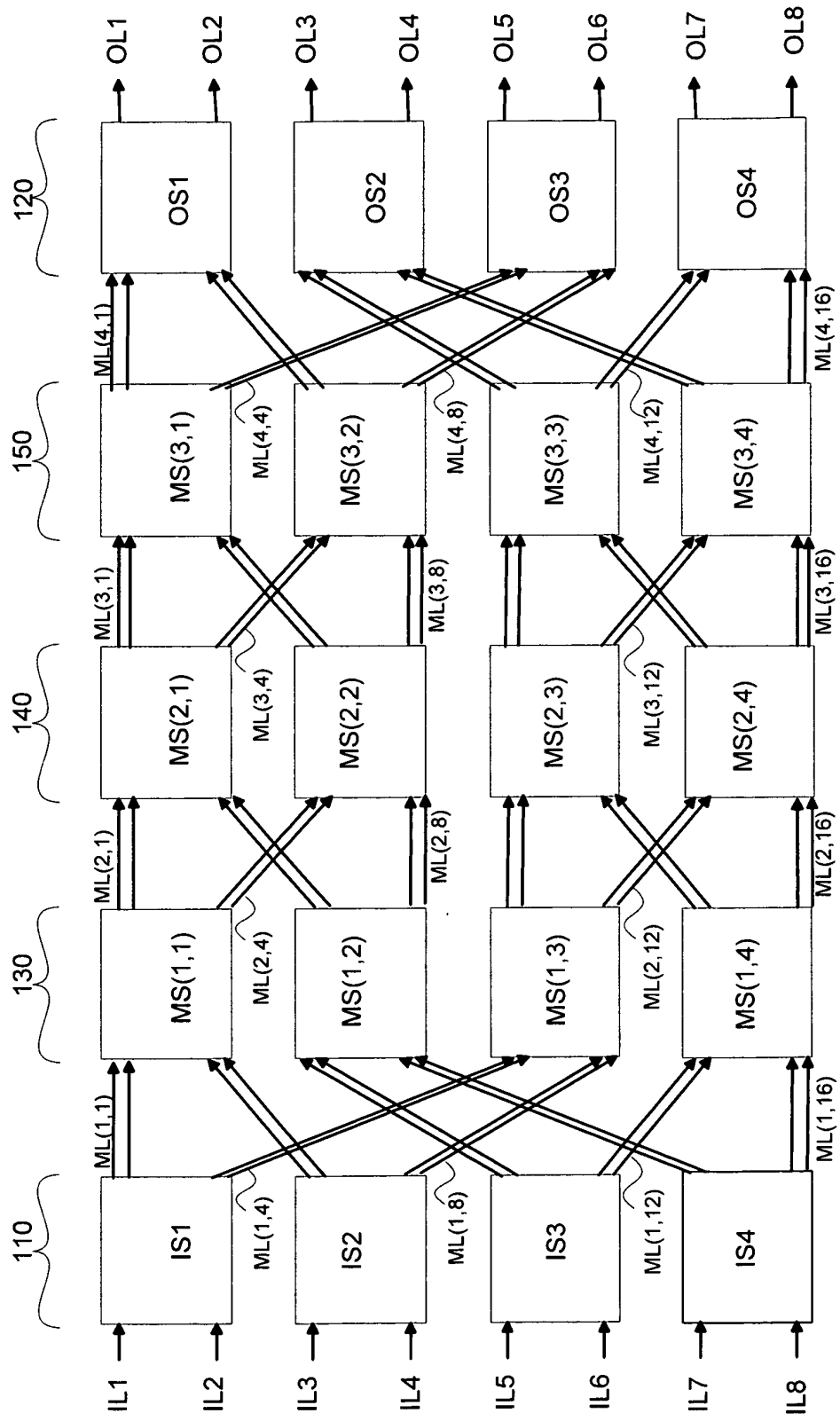


FIG. 1G

100G

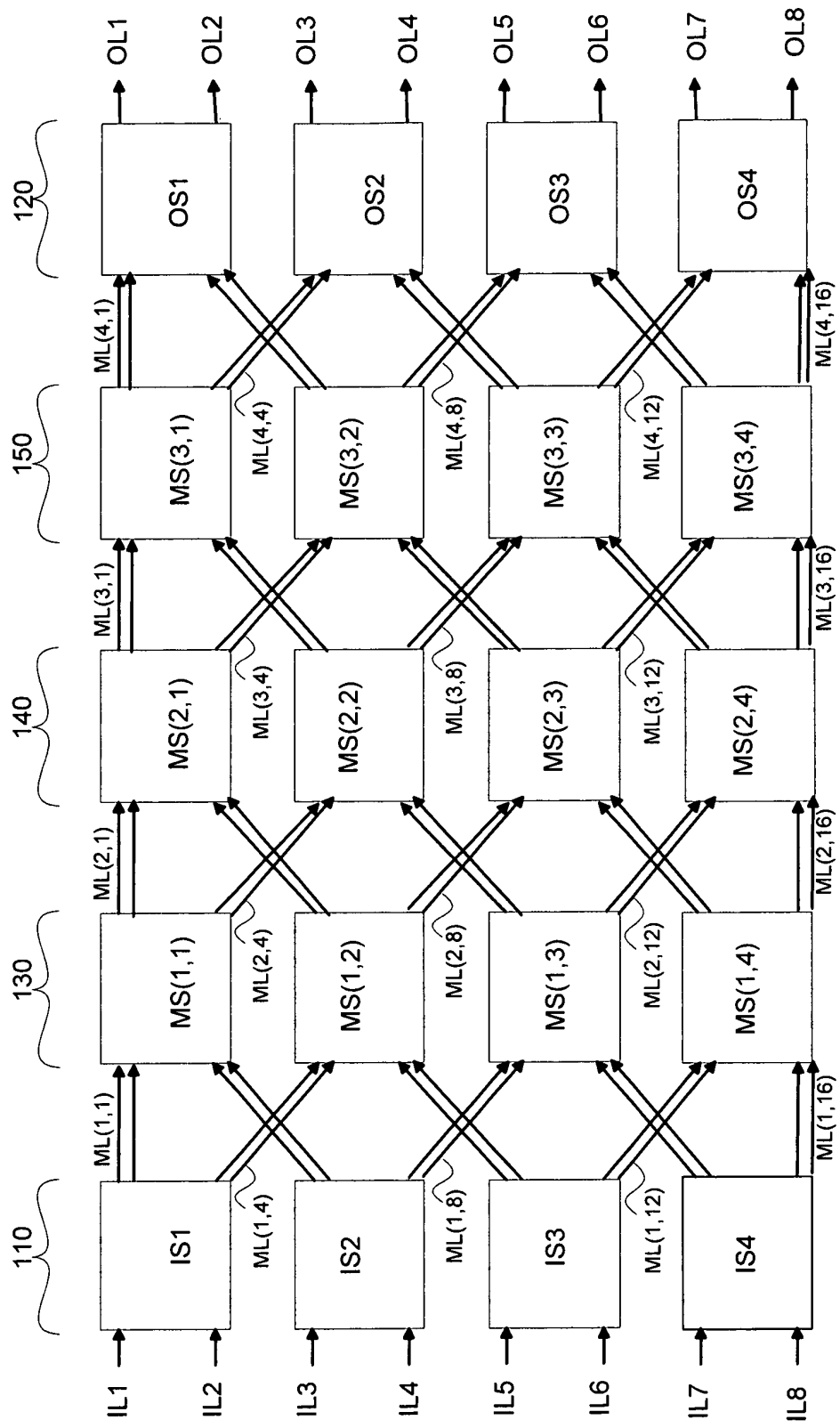


FIG. 1H

100H

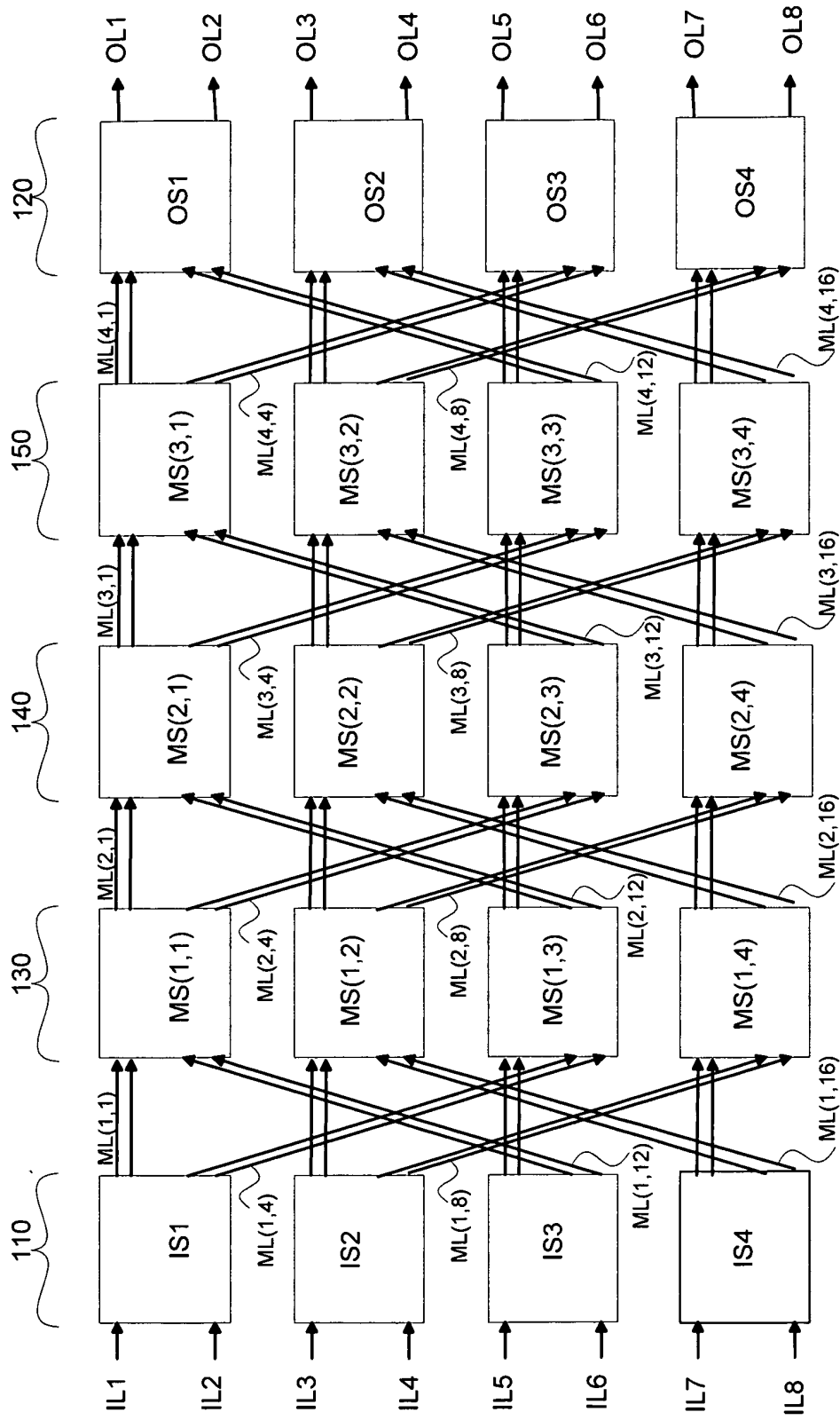


FIG. 11

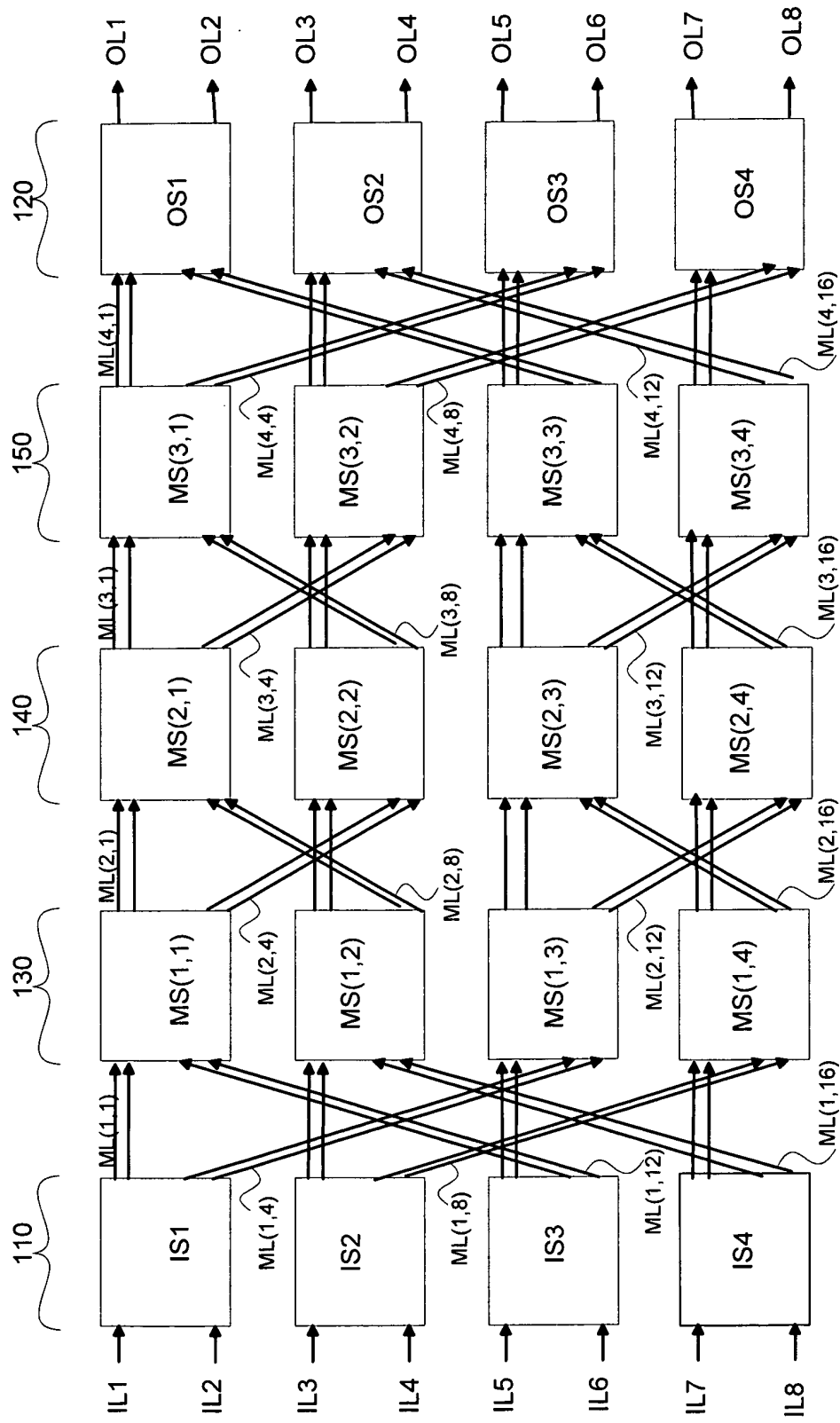
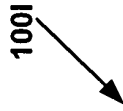


FIG. 1J

100J

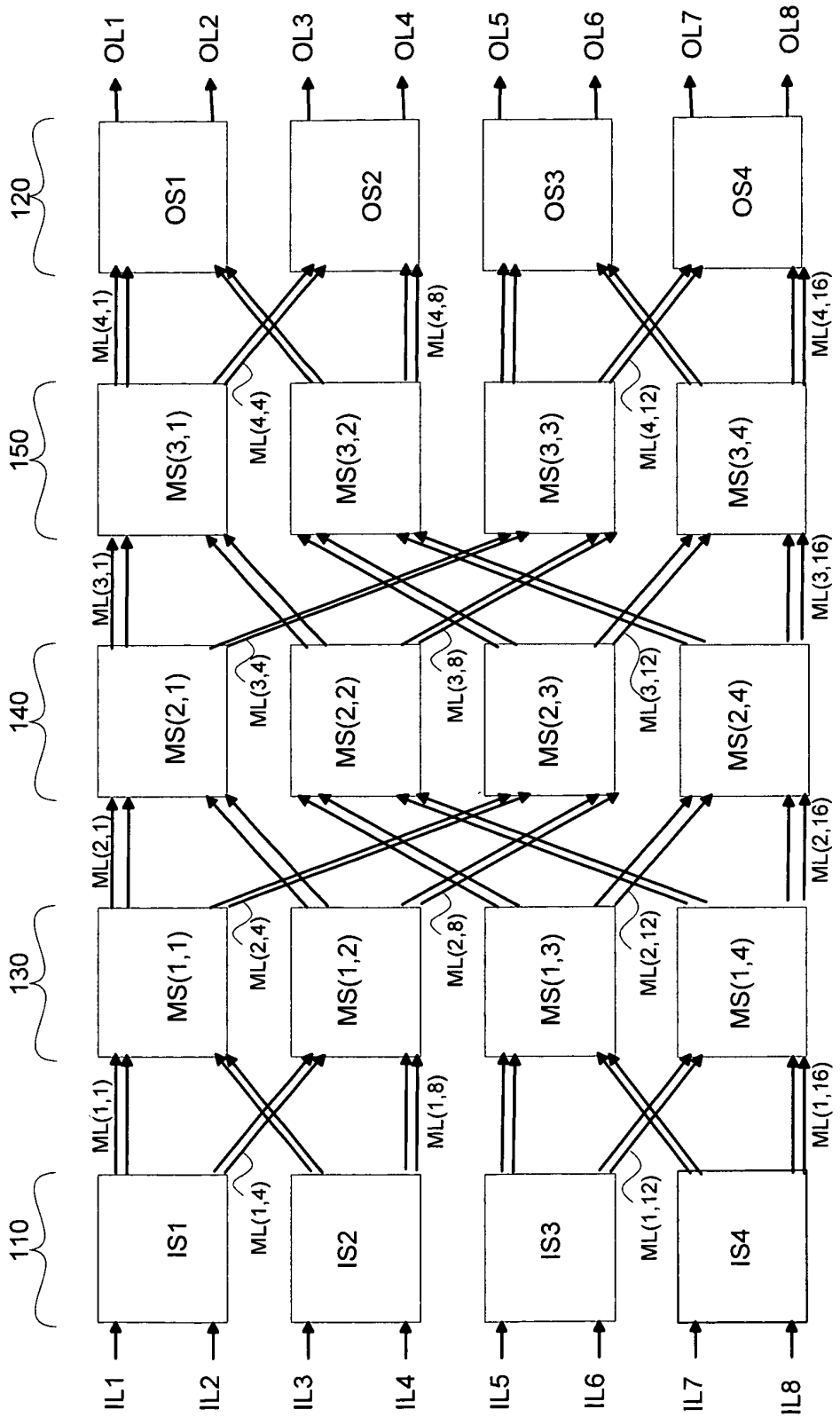


FIG. 1K

100K

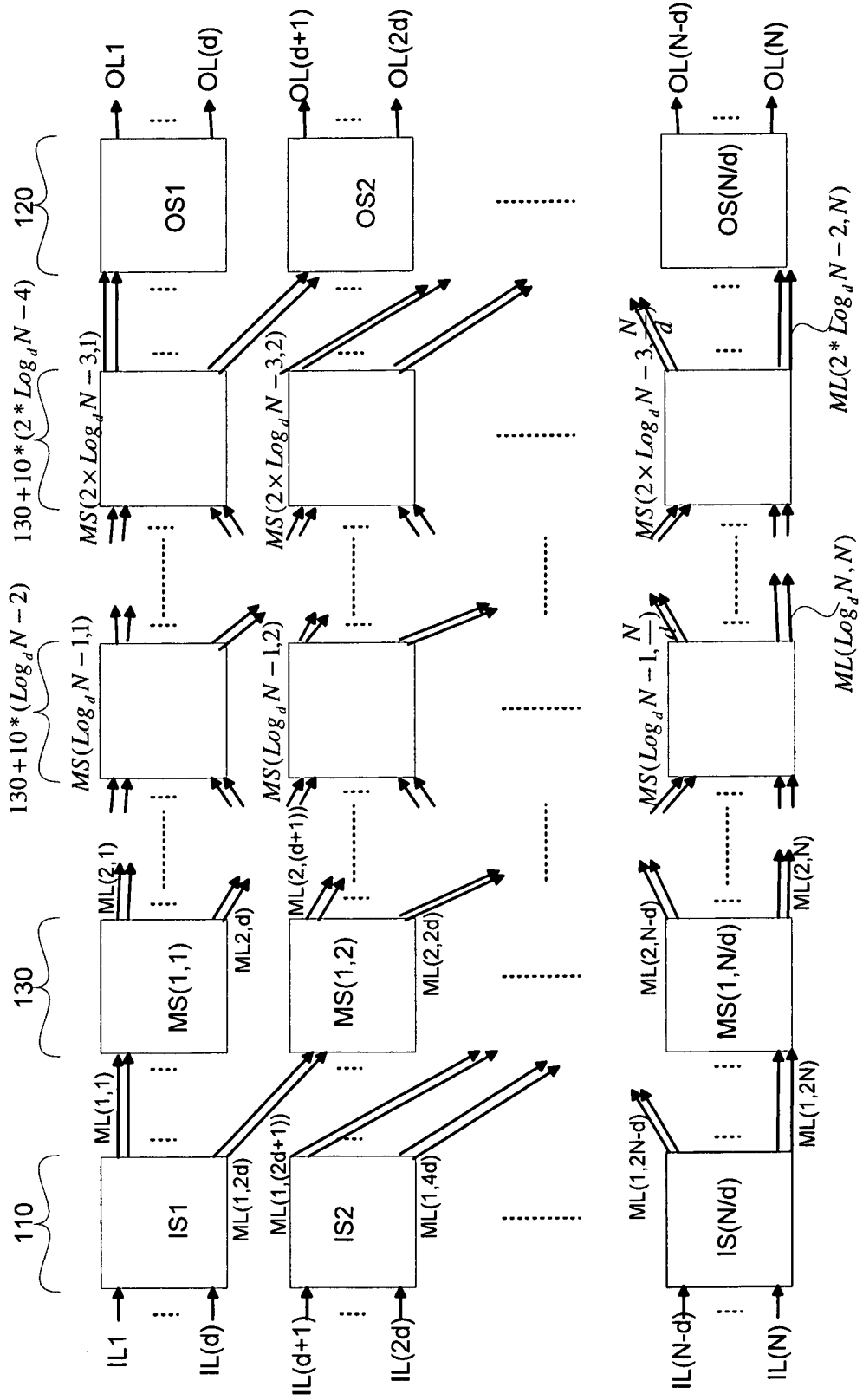


FIG. 1A1

100A1

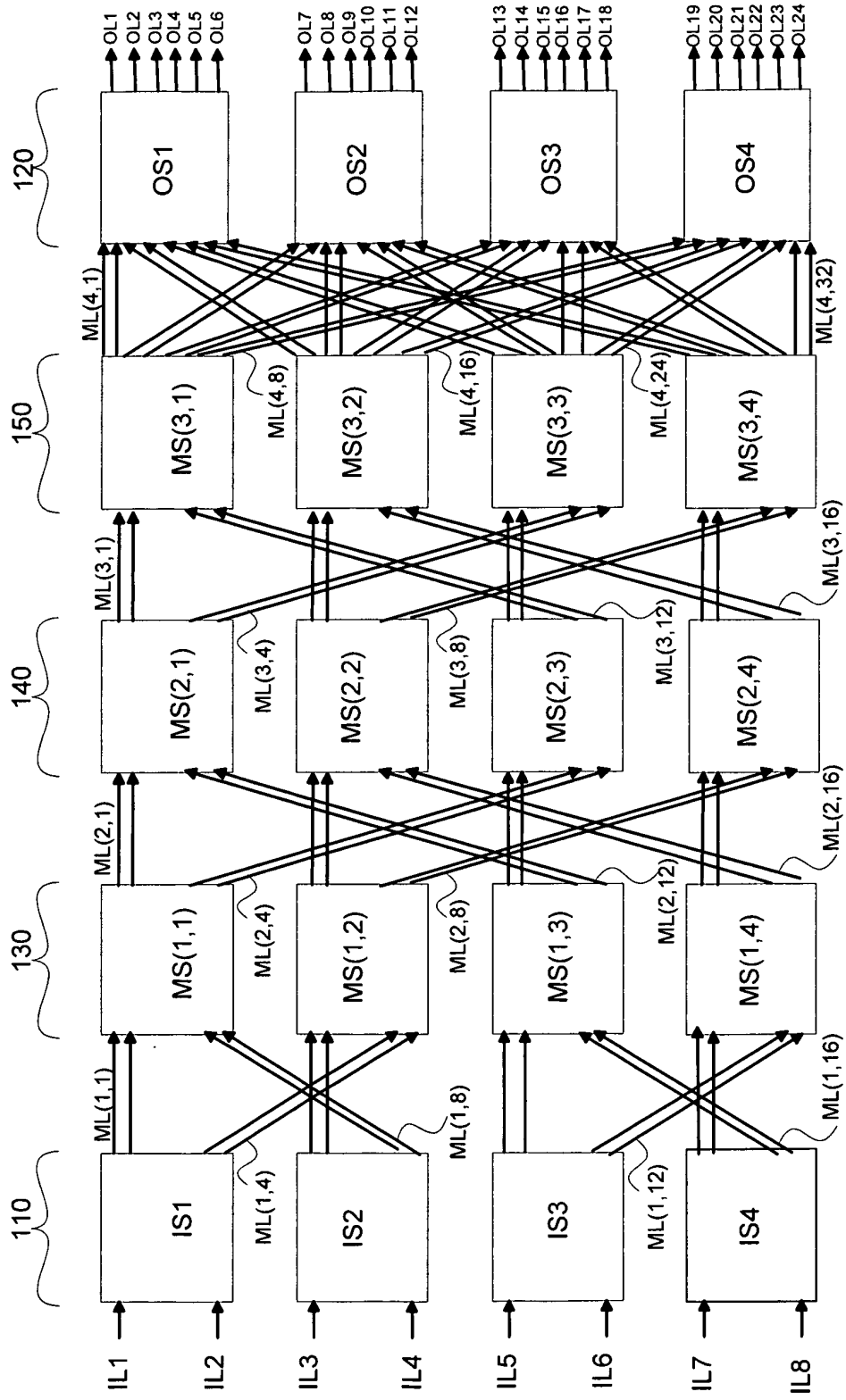


FIG. 1B1

100B1

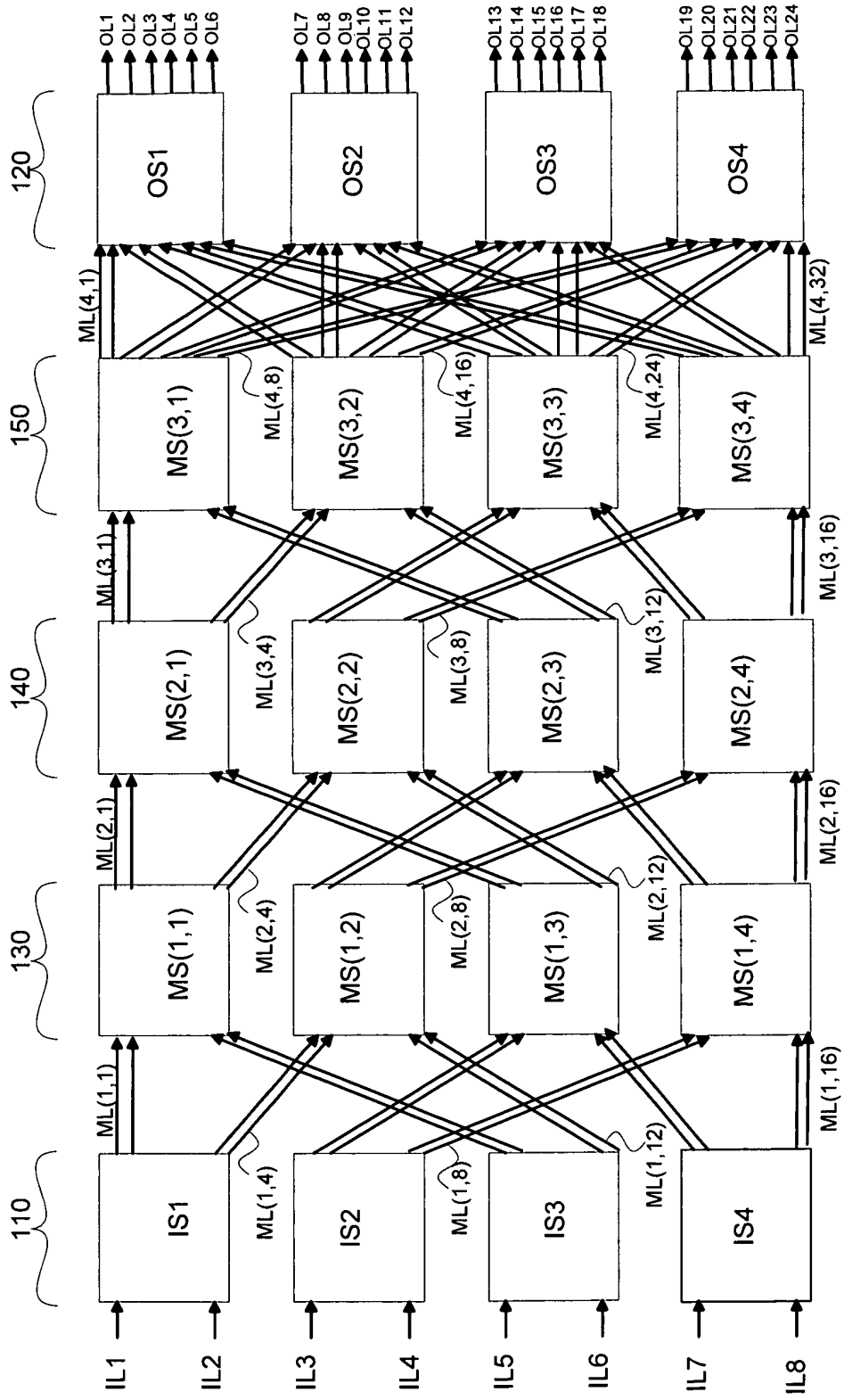


FIG. 1C1

100C1

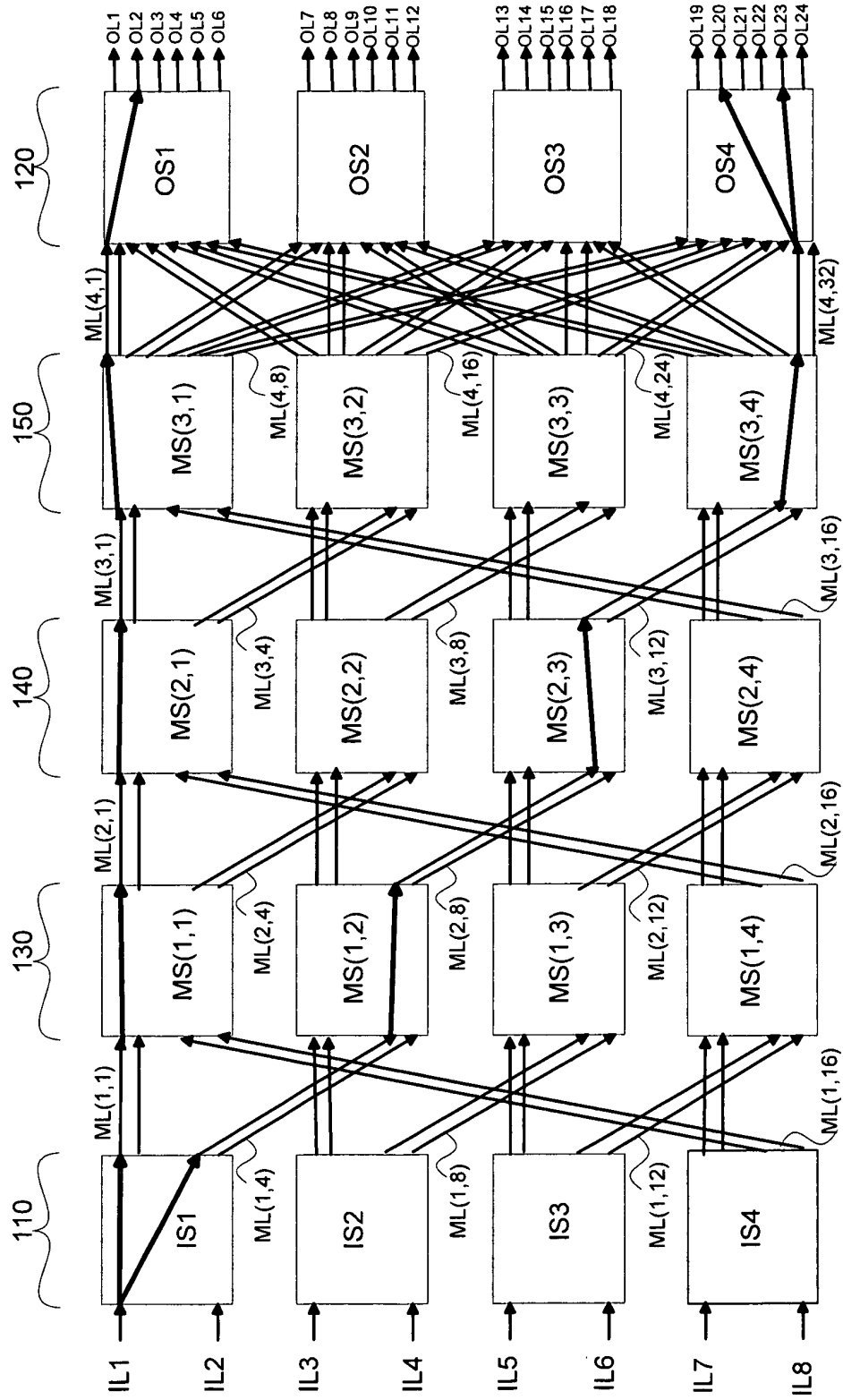


FIG. 1D1

100D1

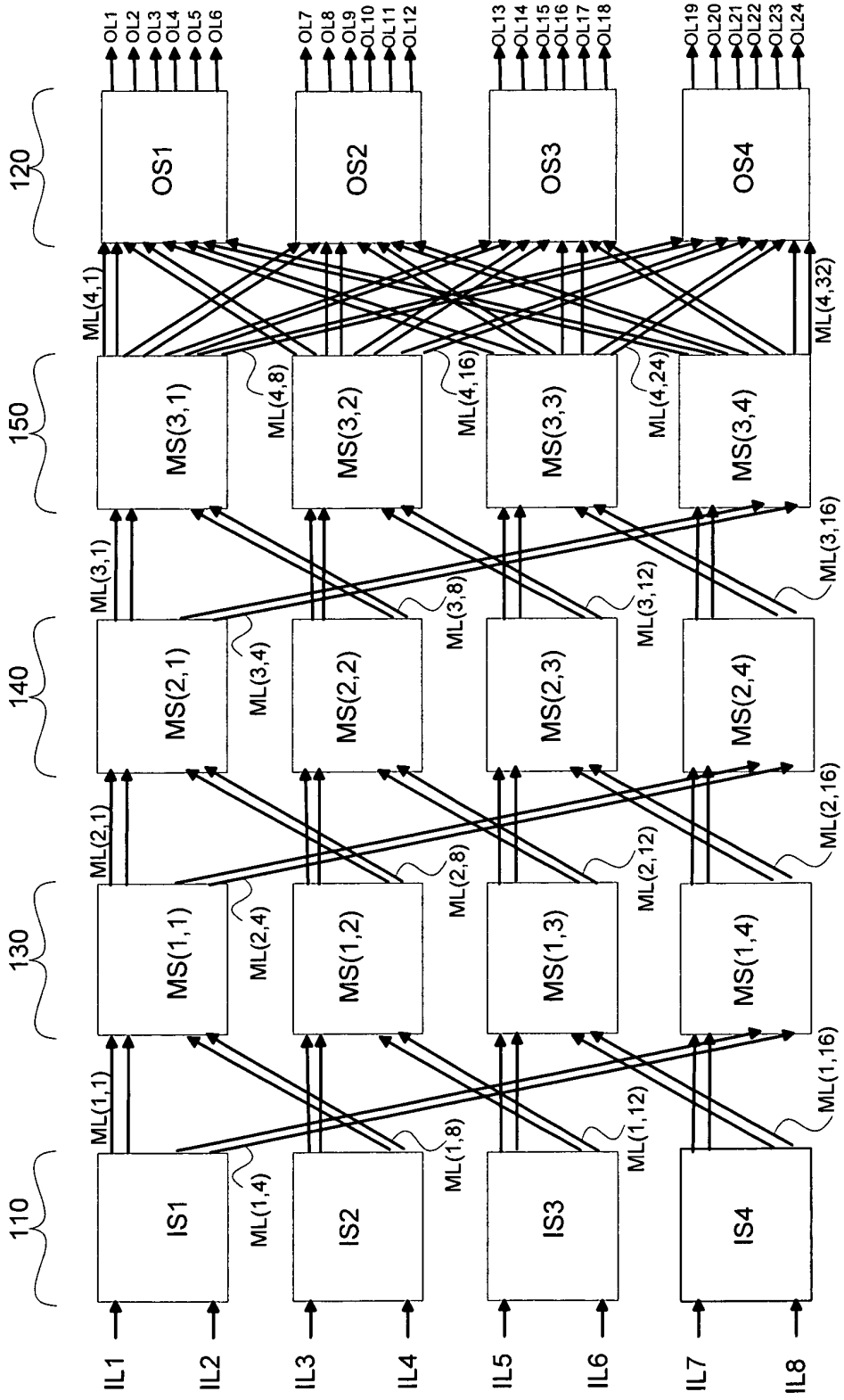


FIG. 1E1

100E1

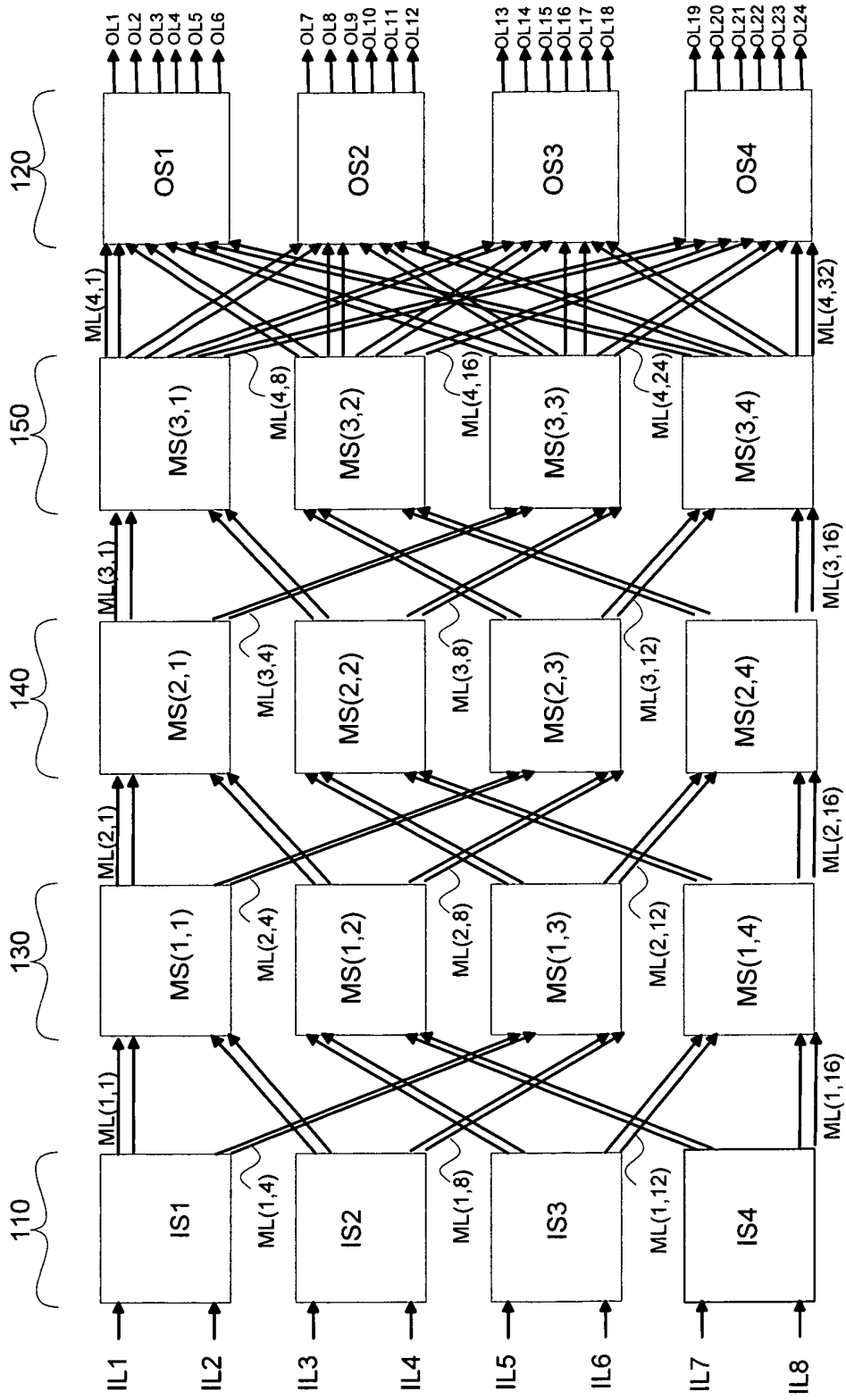


FIG. 1F1

100F1

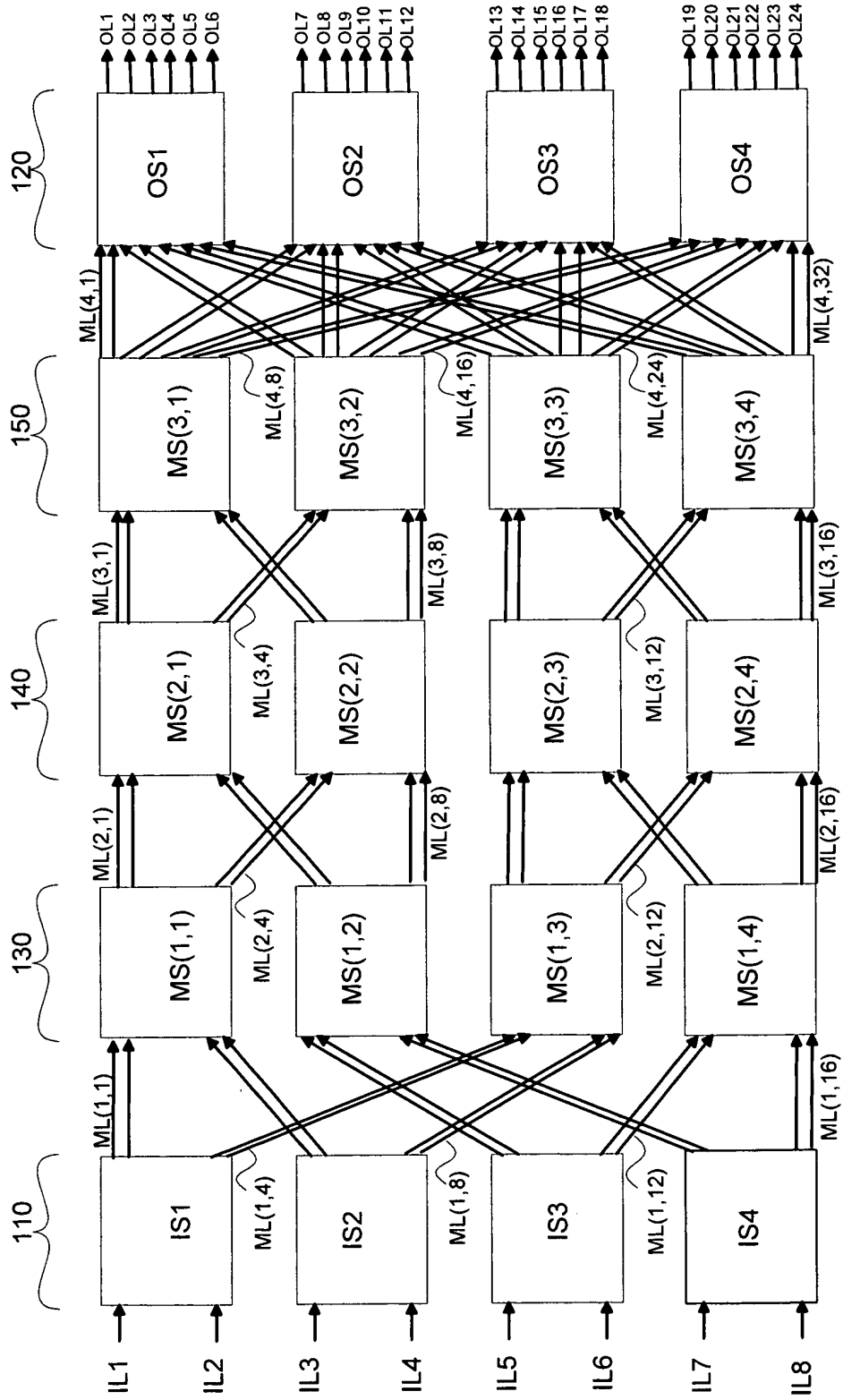


FIG. 1G1

100G1

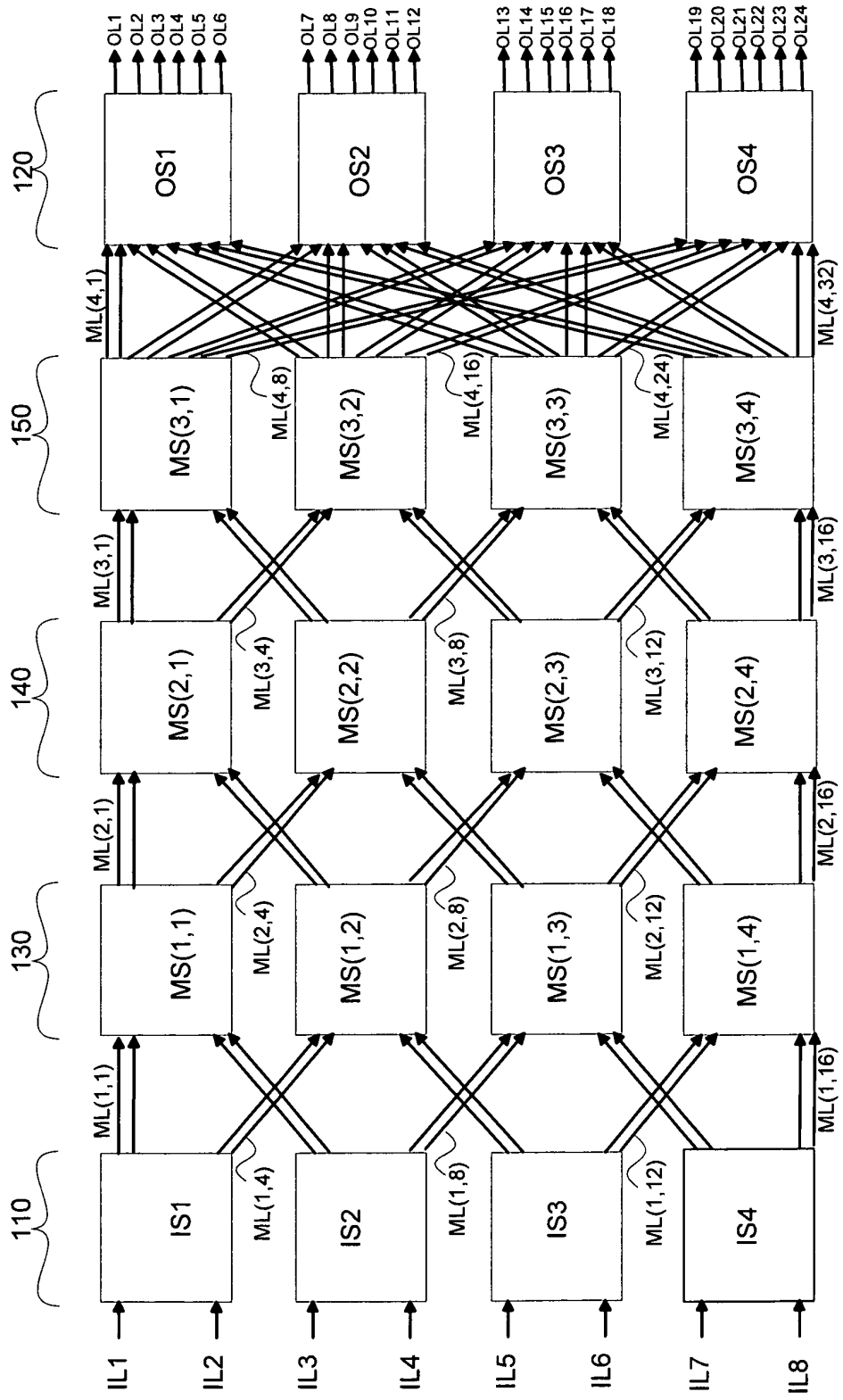


FIG. 1H1

100H1

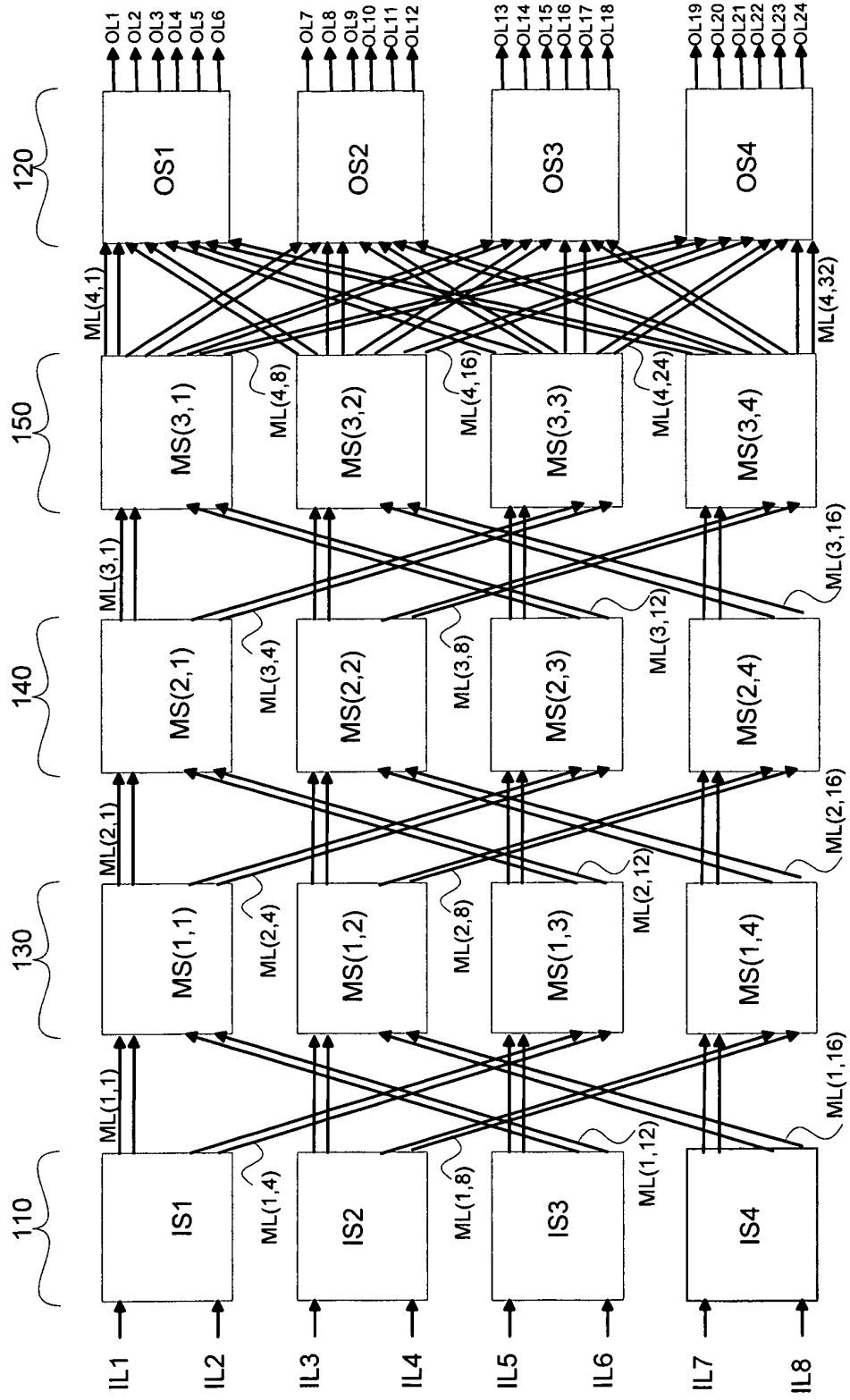


FIG. 111

10011

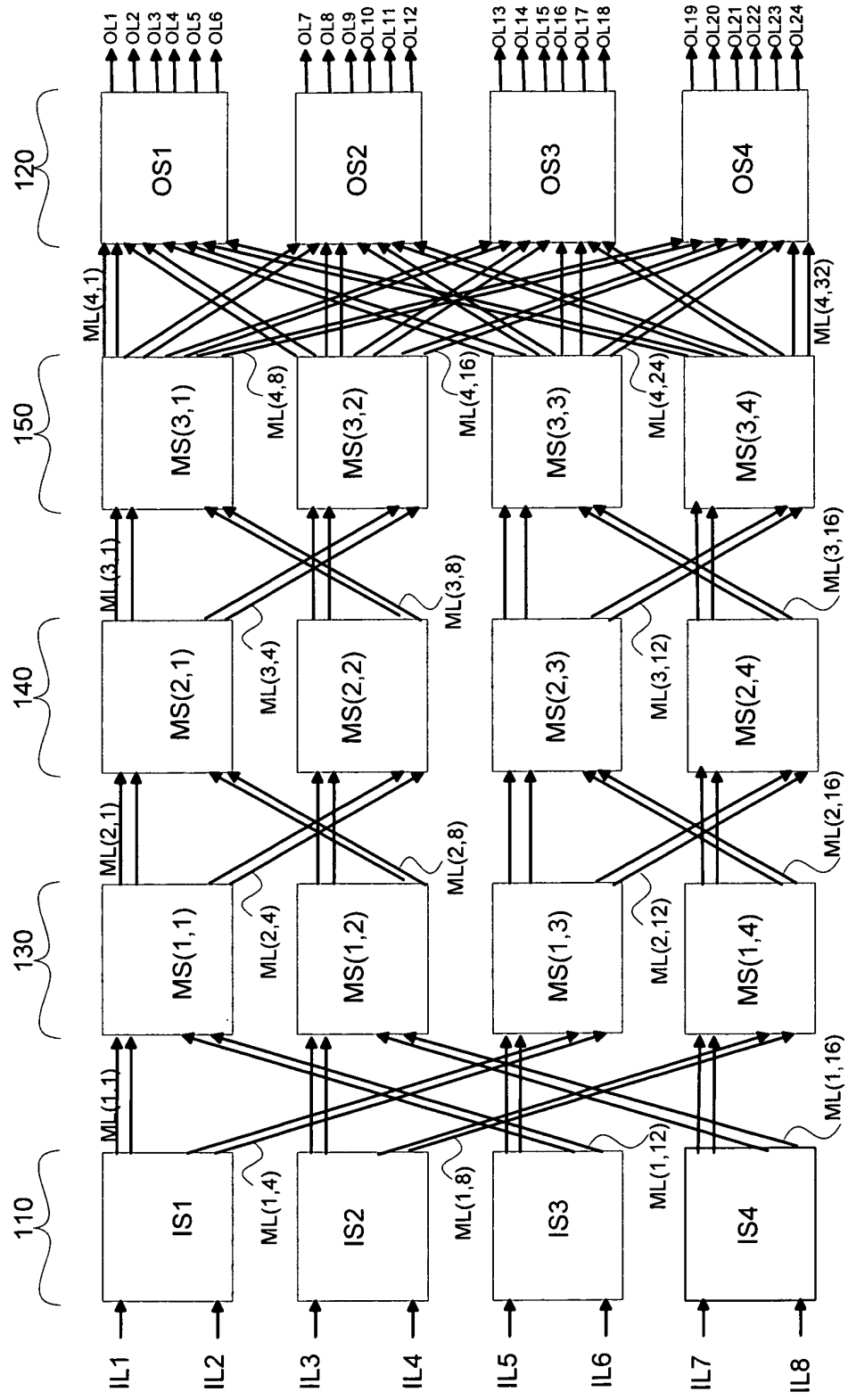
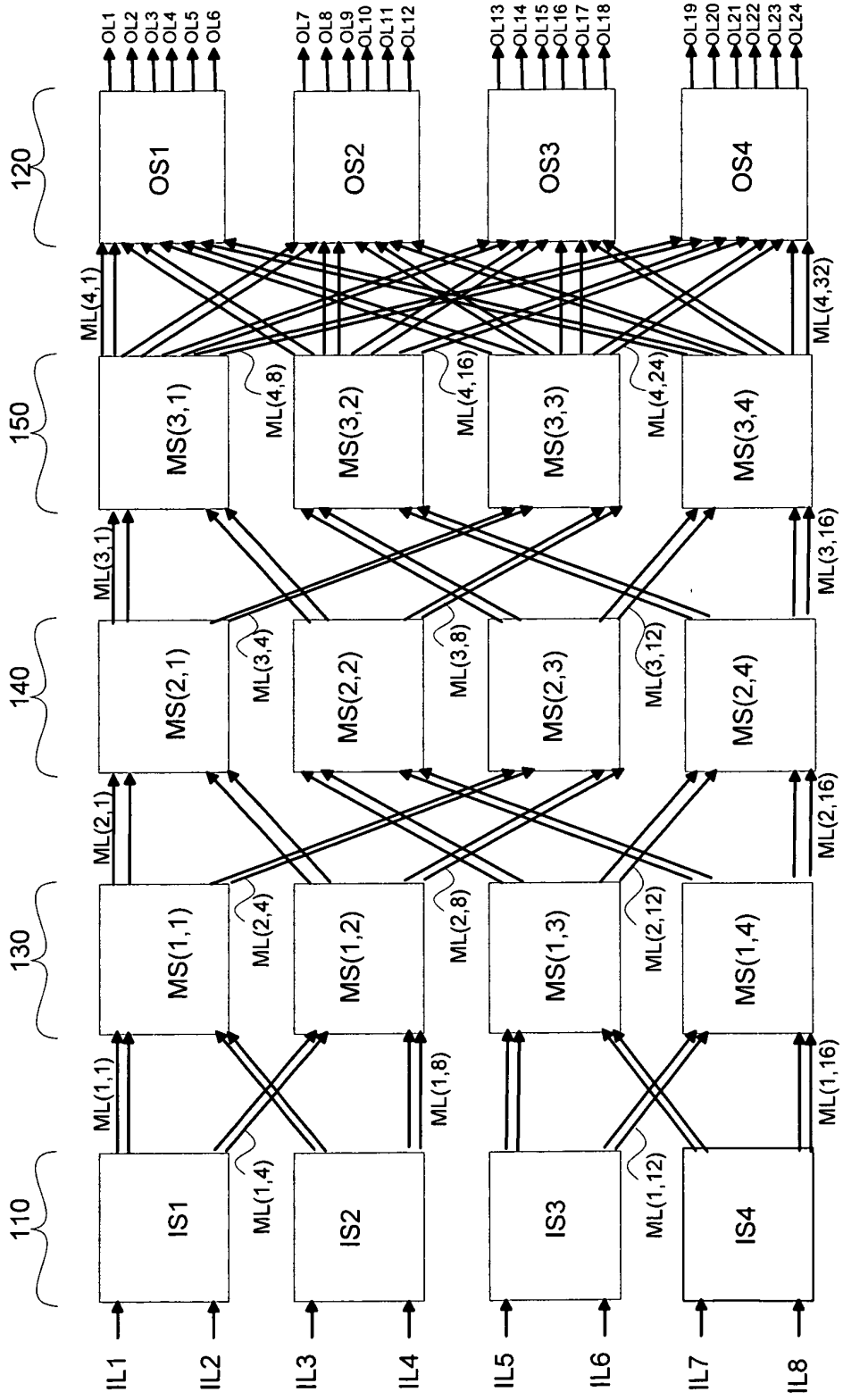


FIG. 1J1

100J1



Page 22 of 125
FIG. 1K1

100K1

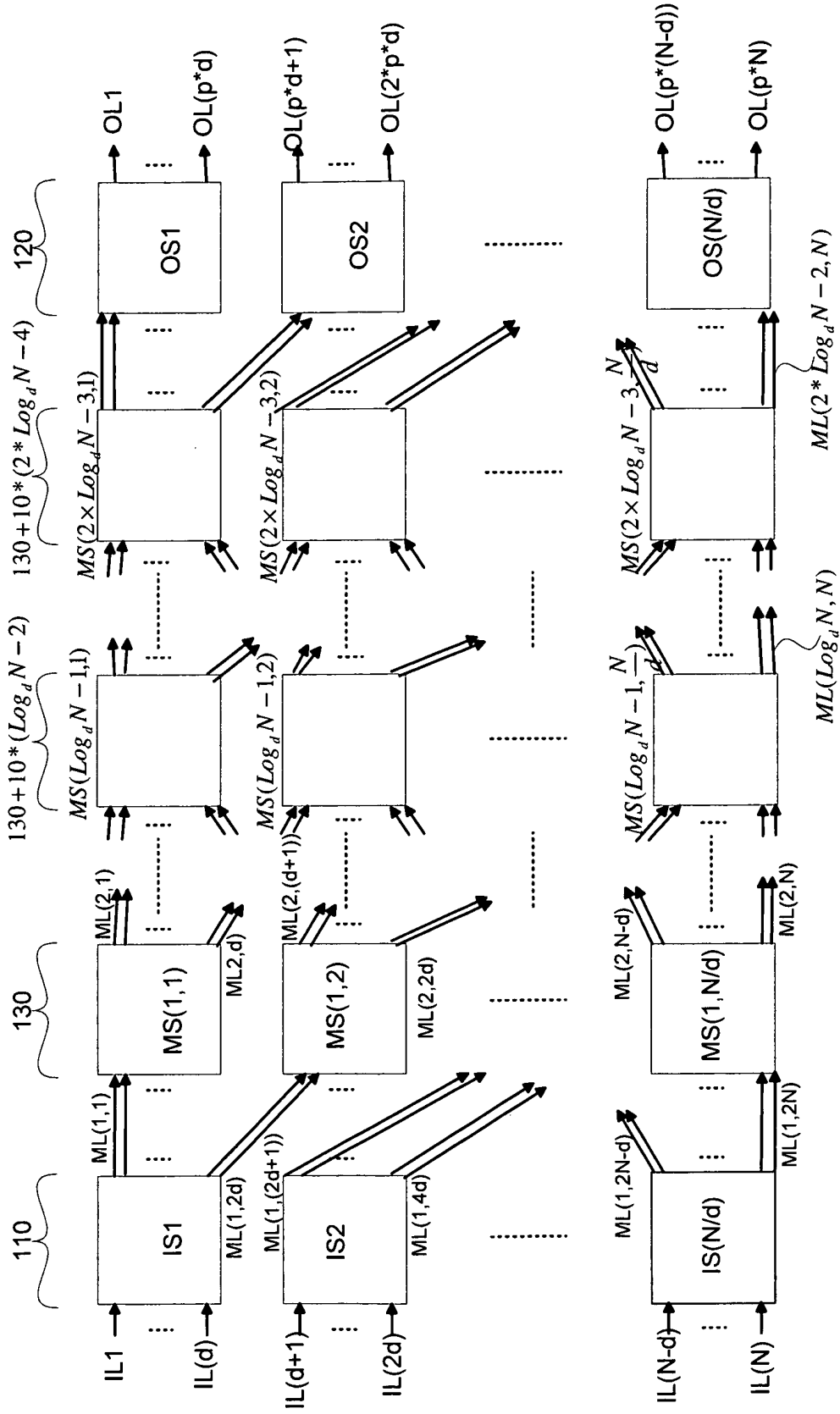


FIG. 1A2

100A2

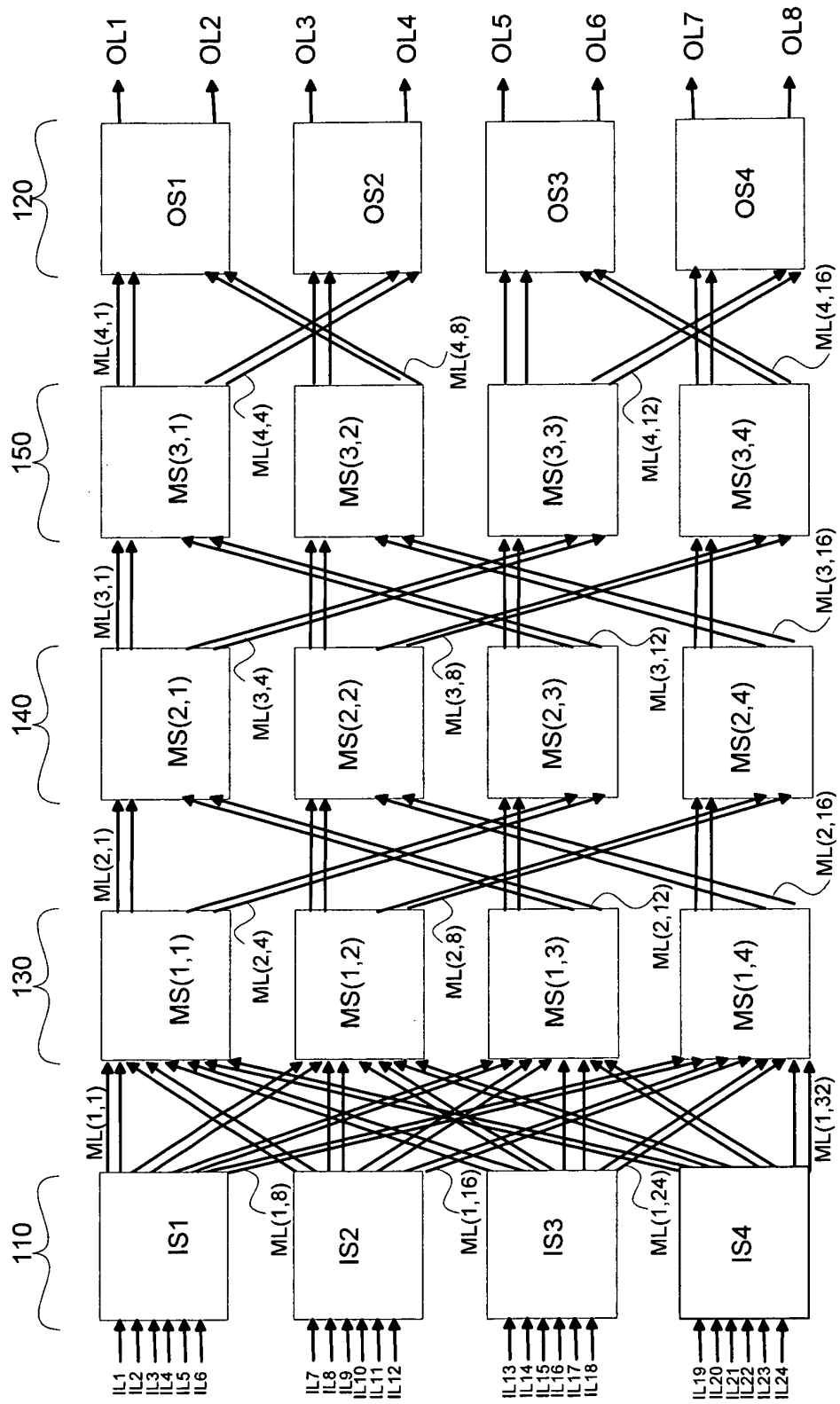


FIG. 1B2

100B2

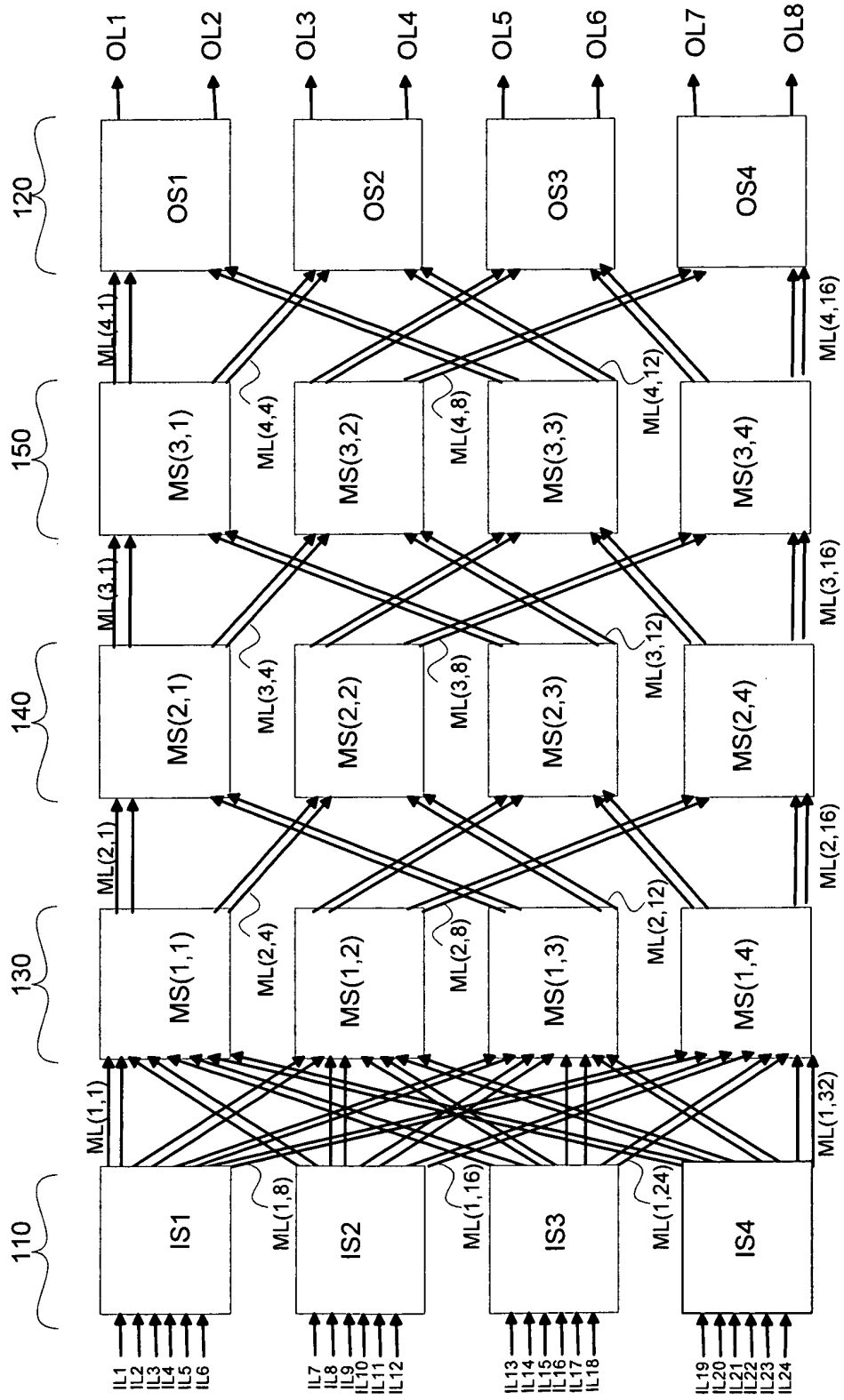


FIG. 1C2

100C2

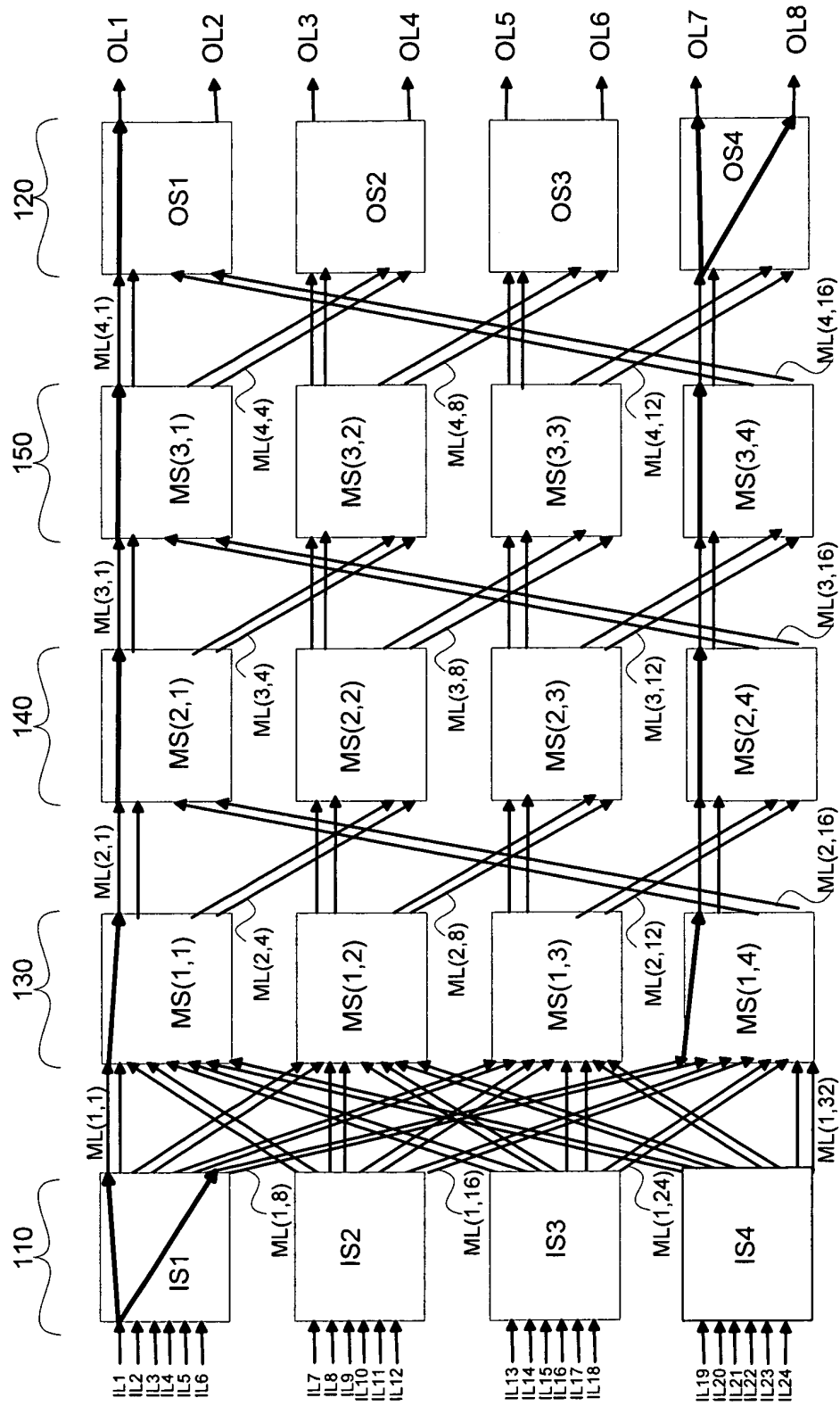


FIG. 1D2

100D2

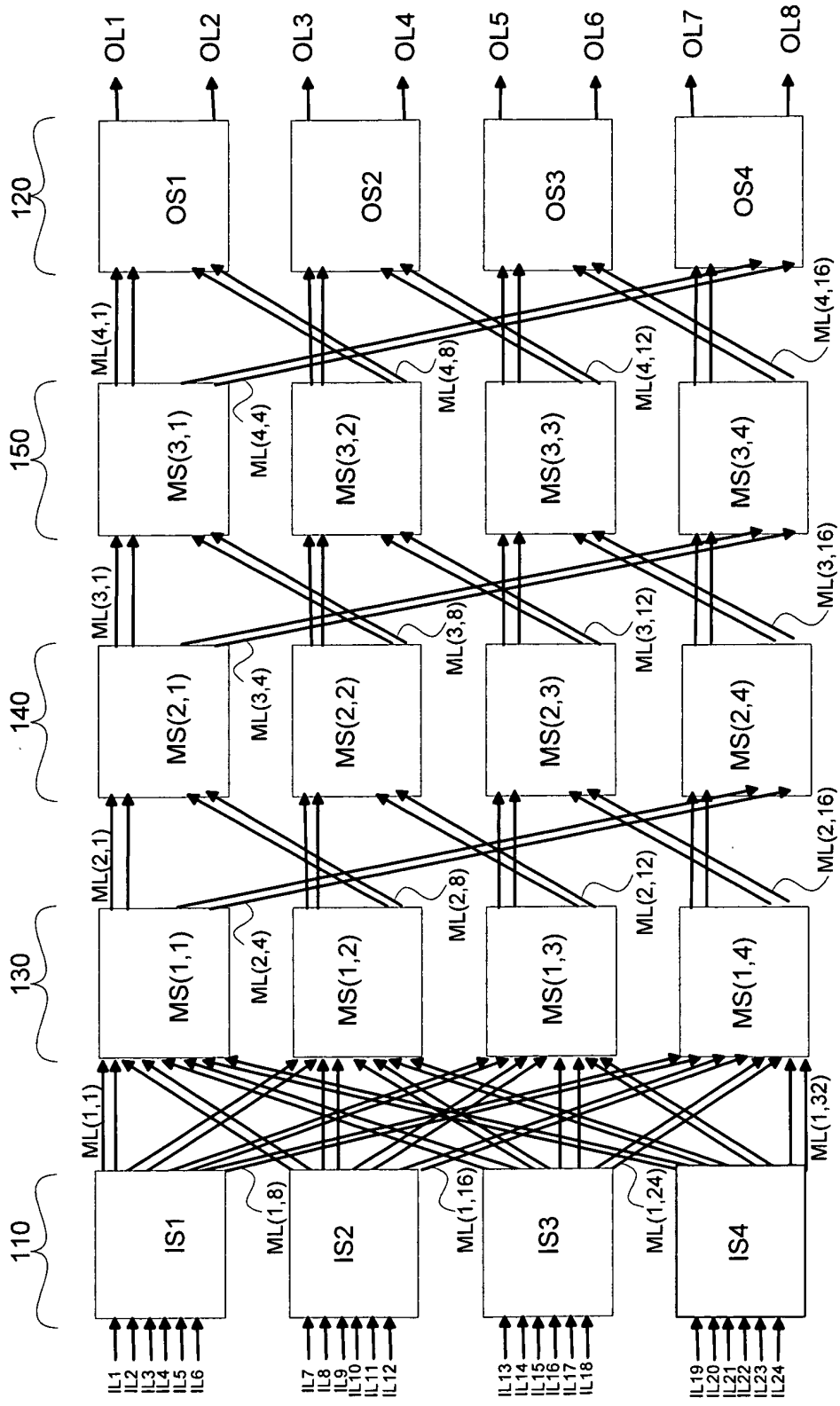


FIG. 1E2

100E2

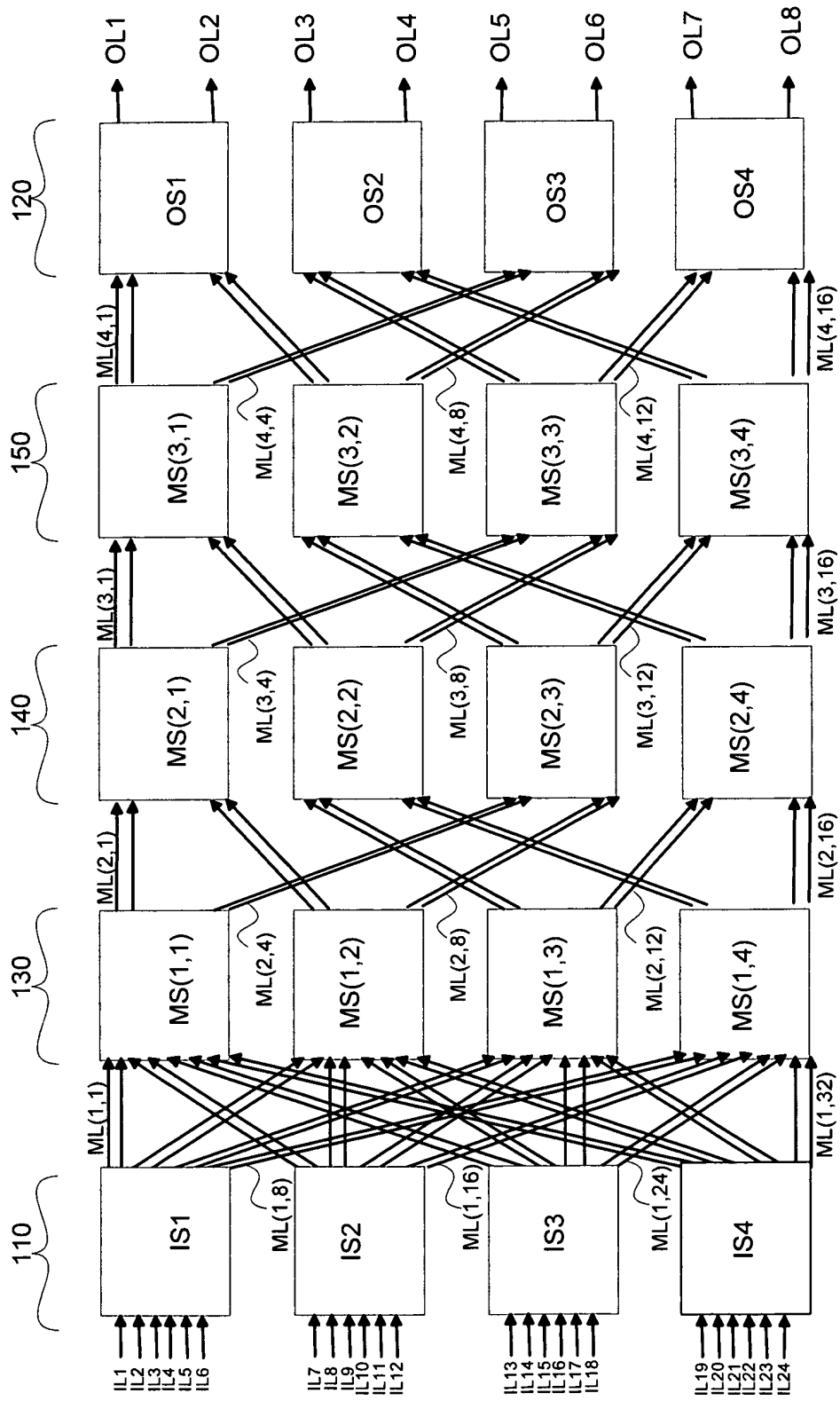


FIG. 1F2

100F2

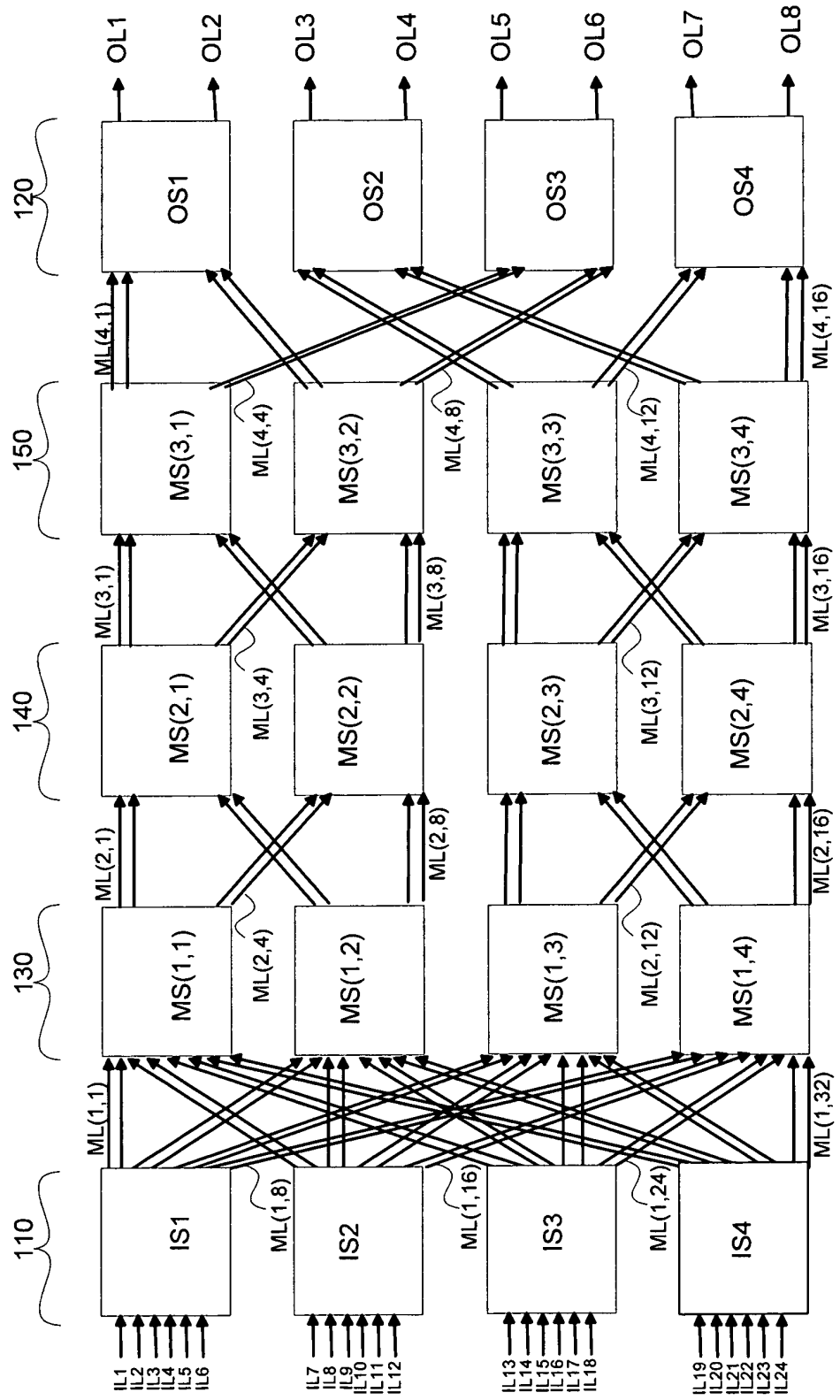


FIG. 1G2

100G2

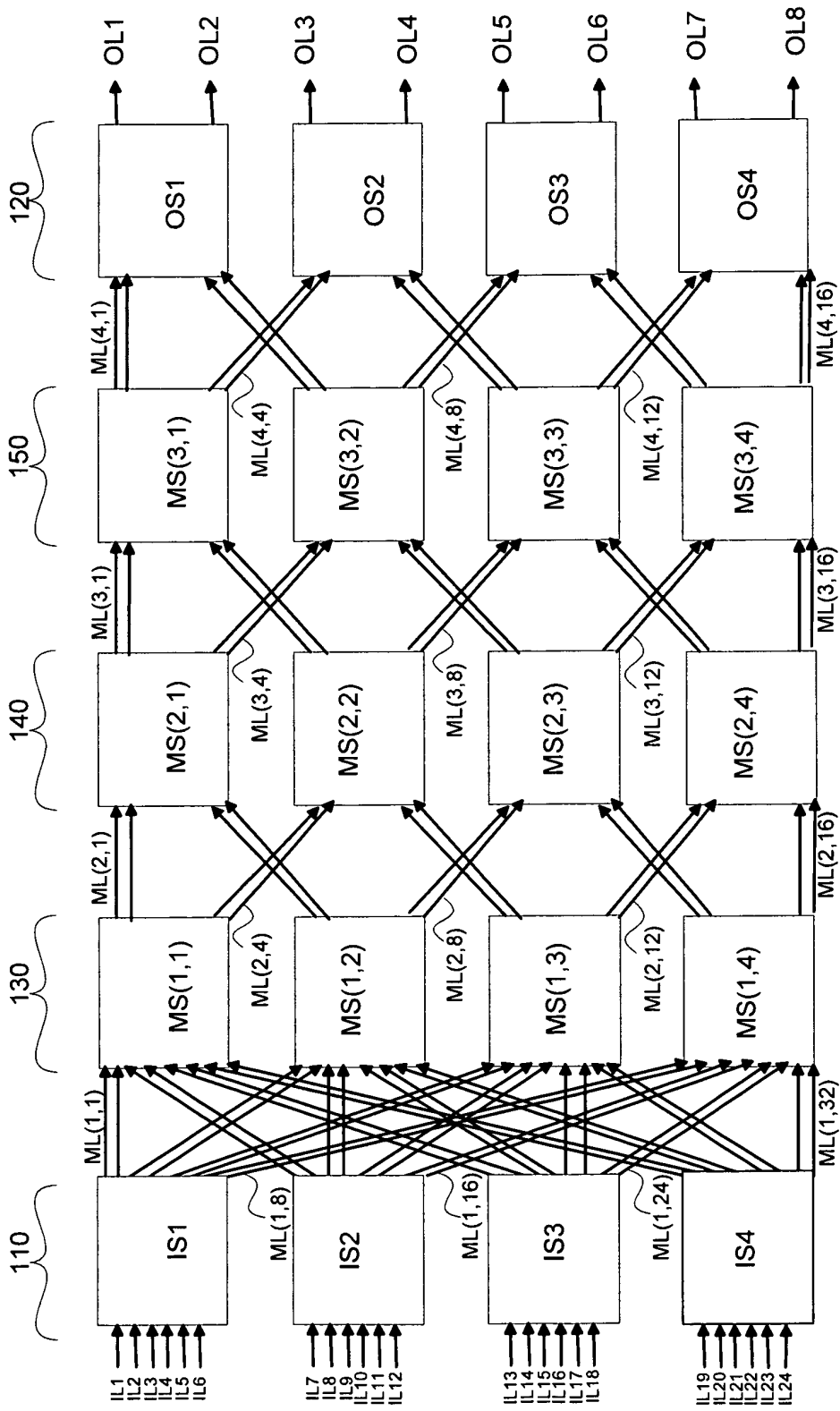


FIG. 1H2

100H2

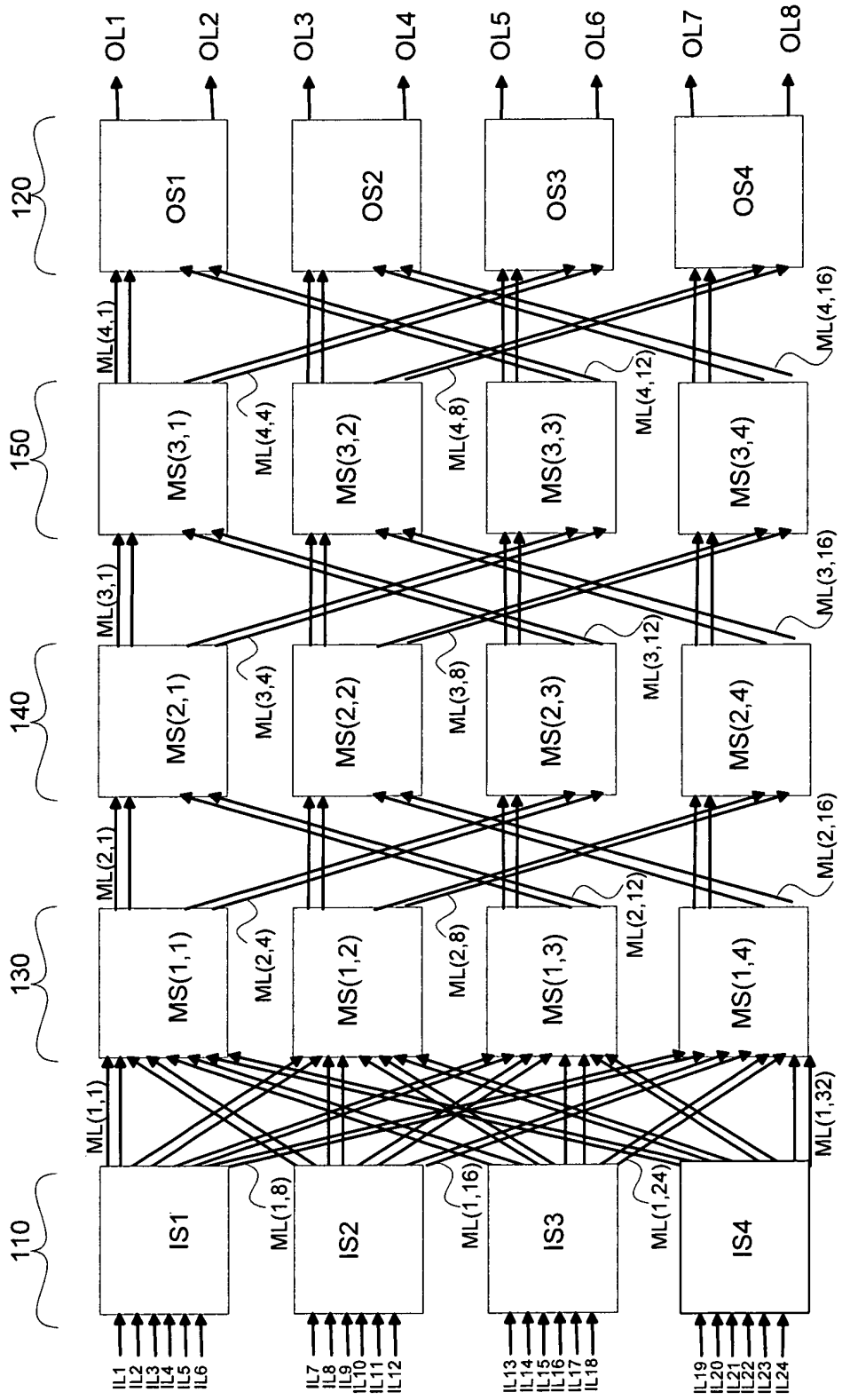


FIG. 112

10012

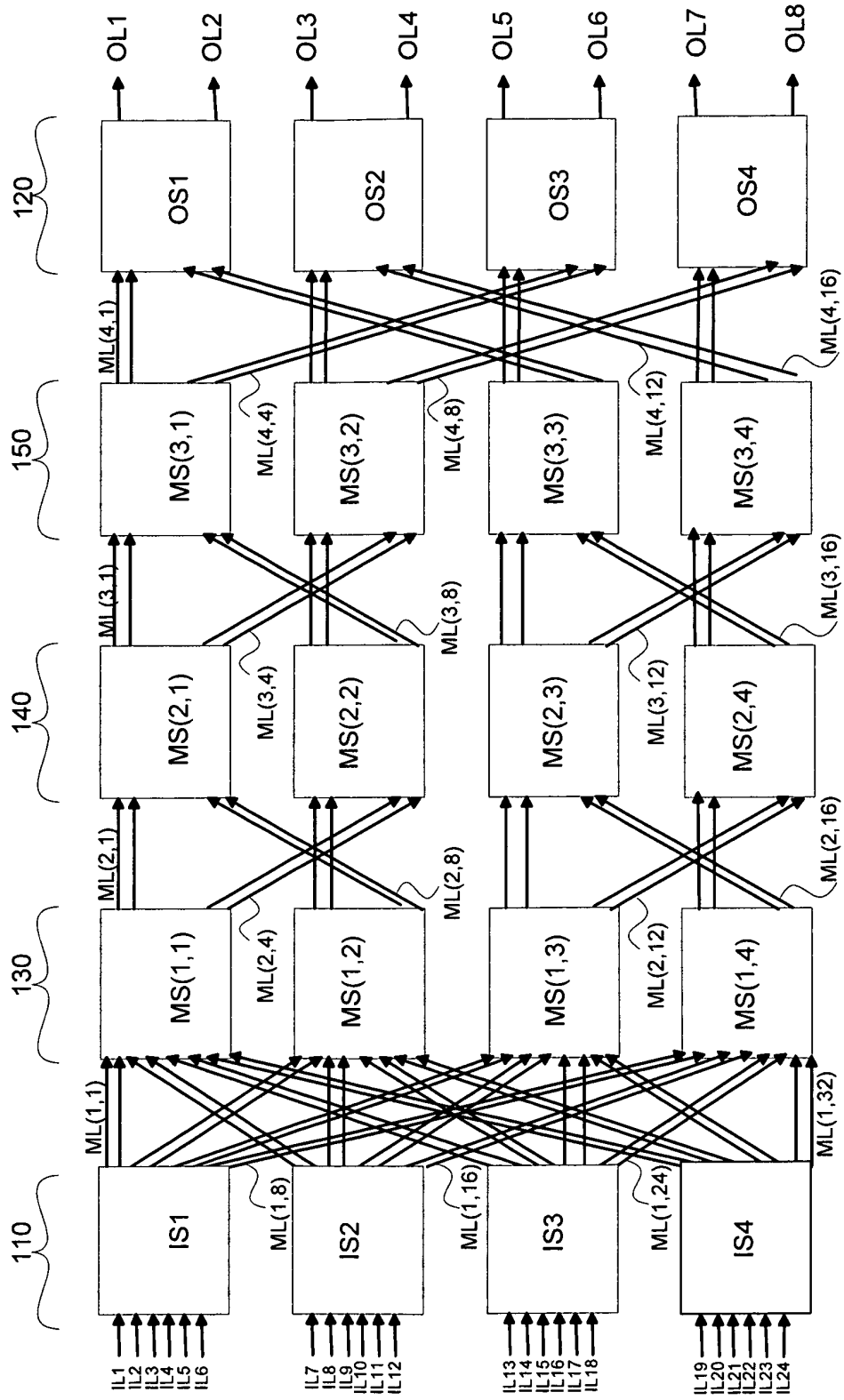


FIG. 1J2

100J2

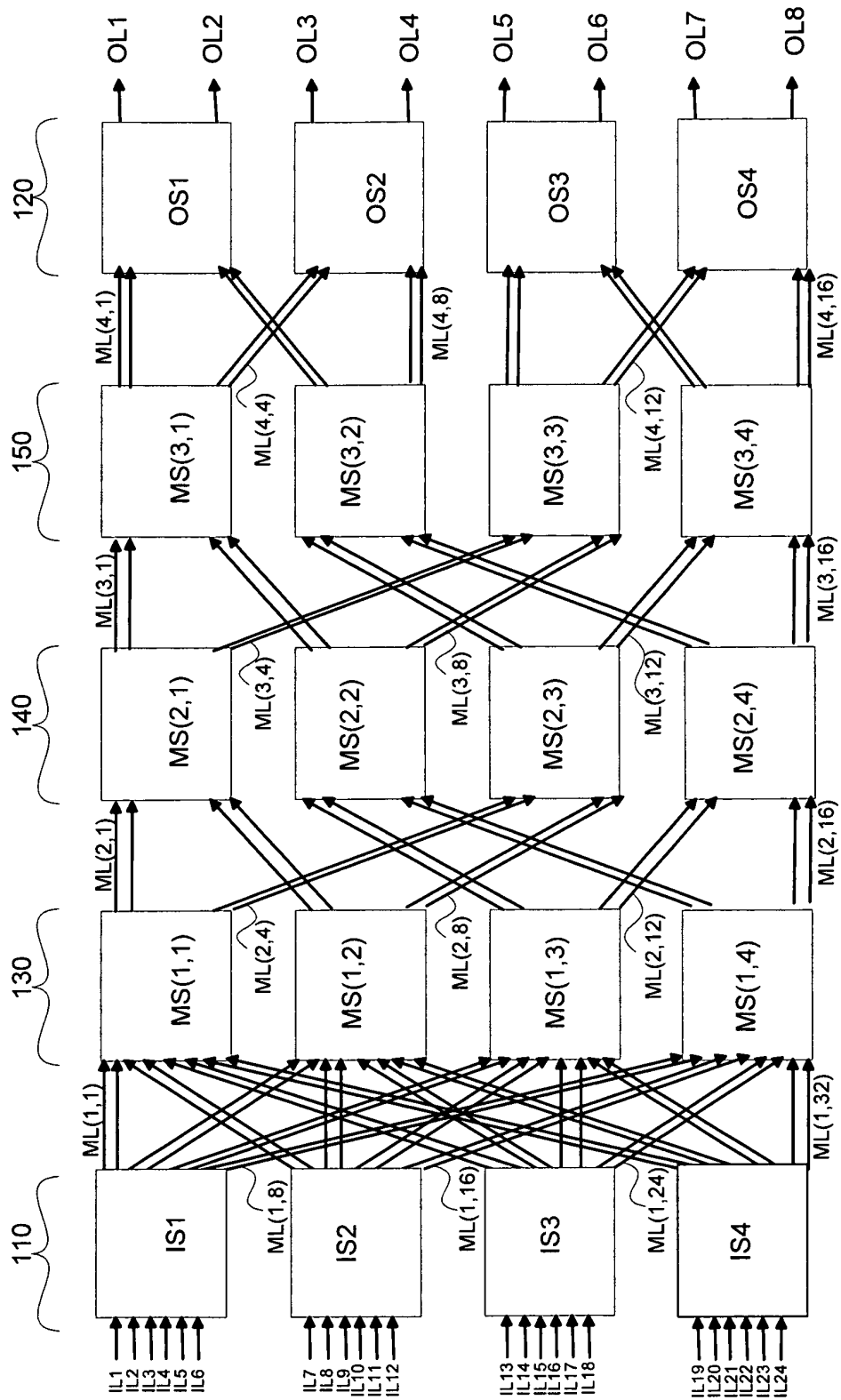


FIG. 1K2

100K2

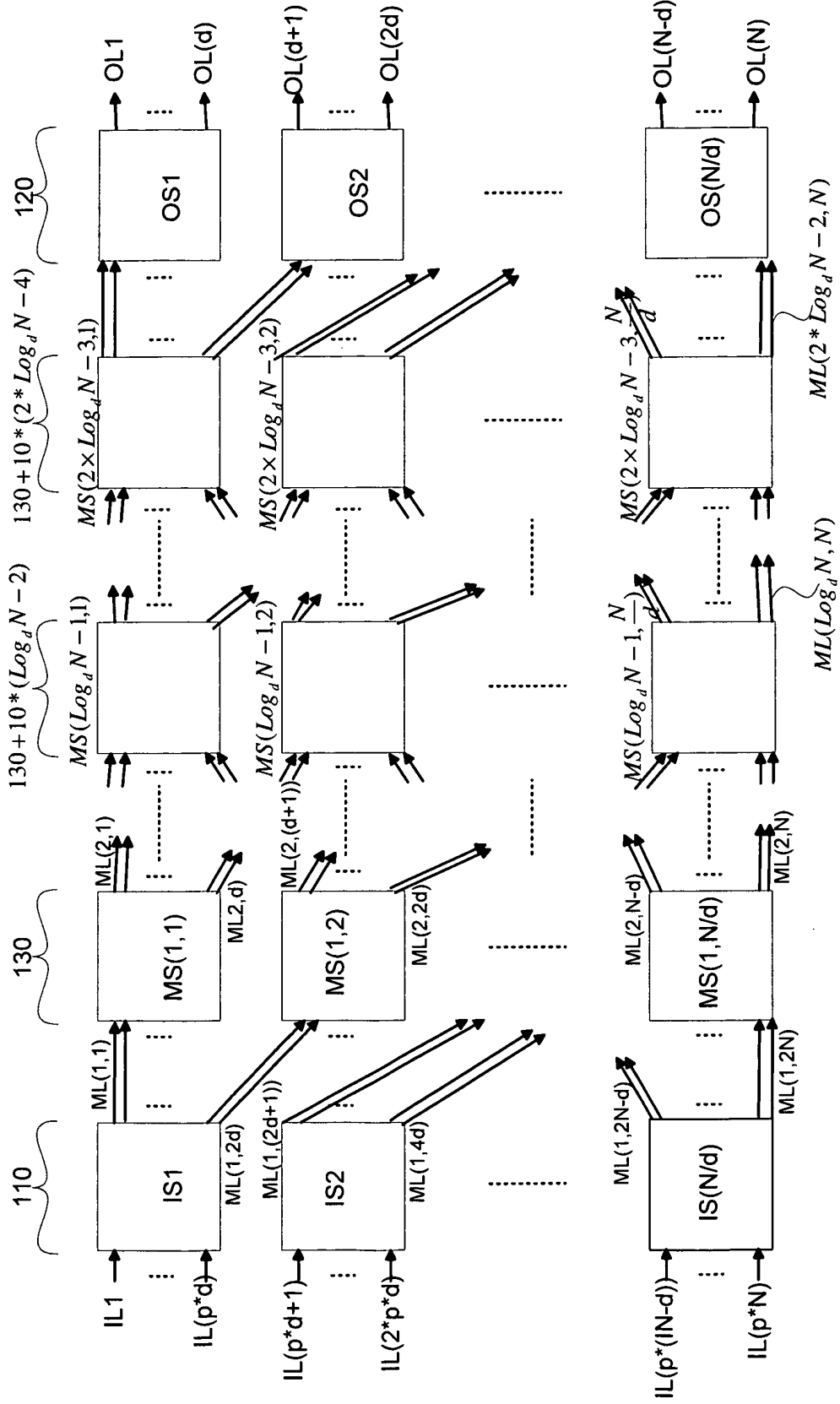


FIG. 2A

200A

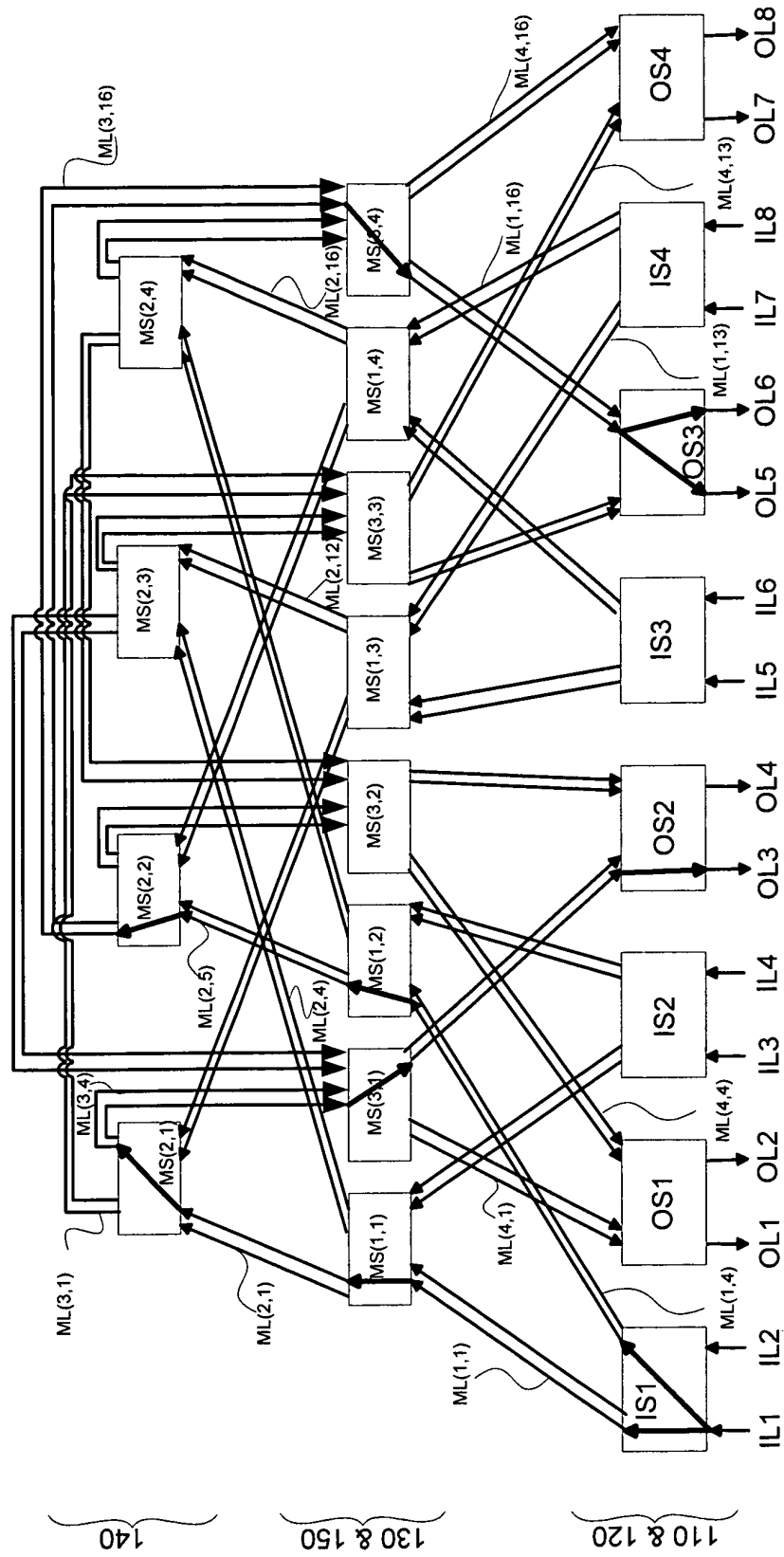


FIG. 2C

200C

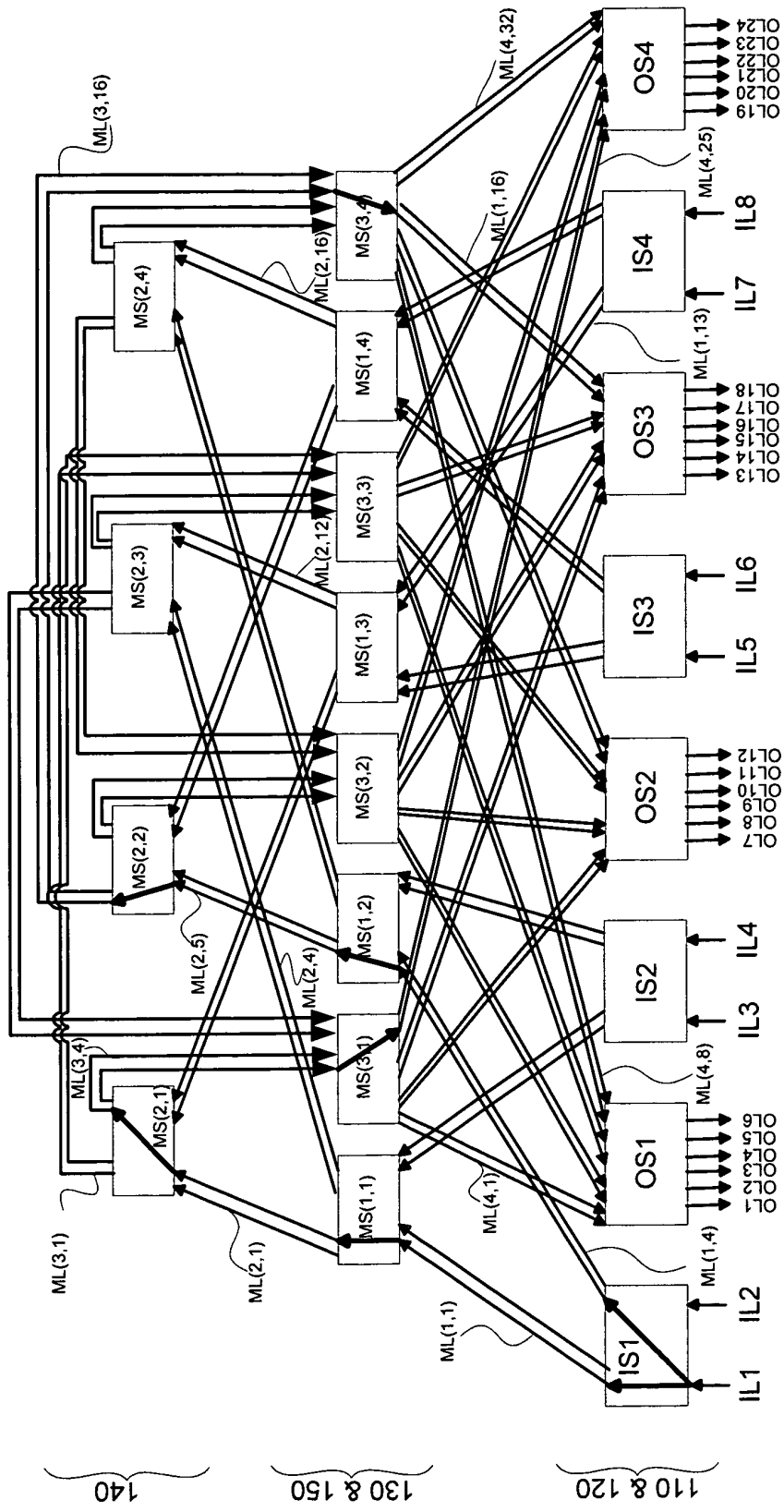


FIG. 2E

200E

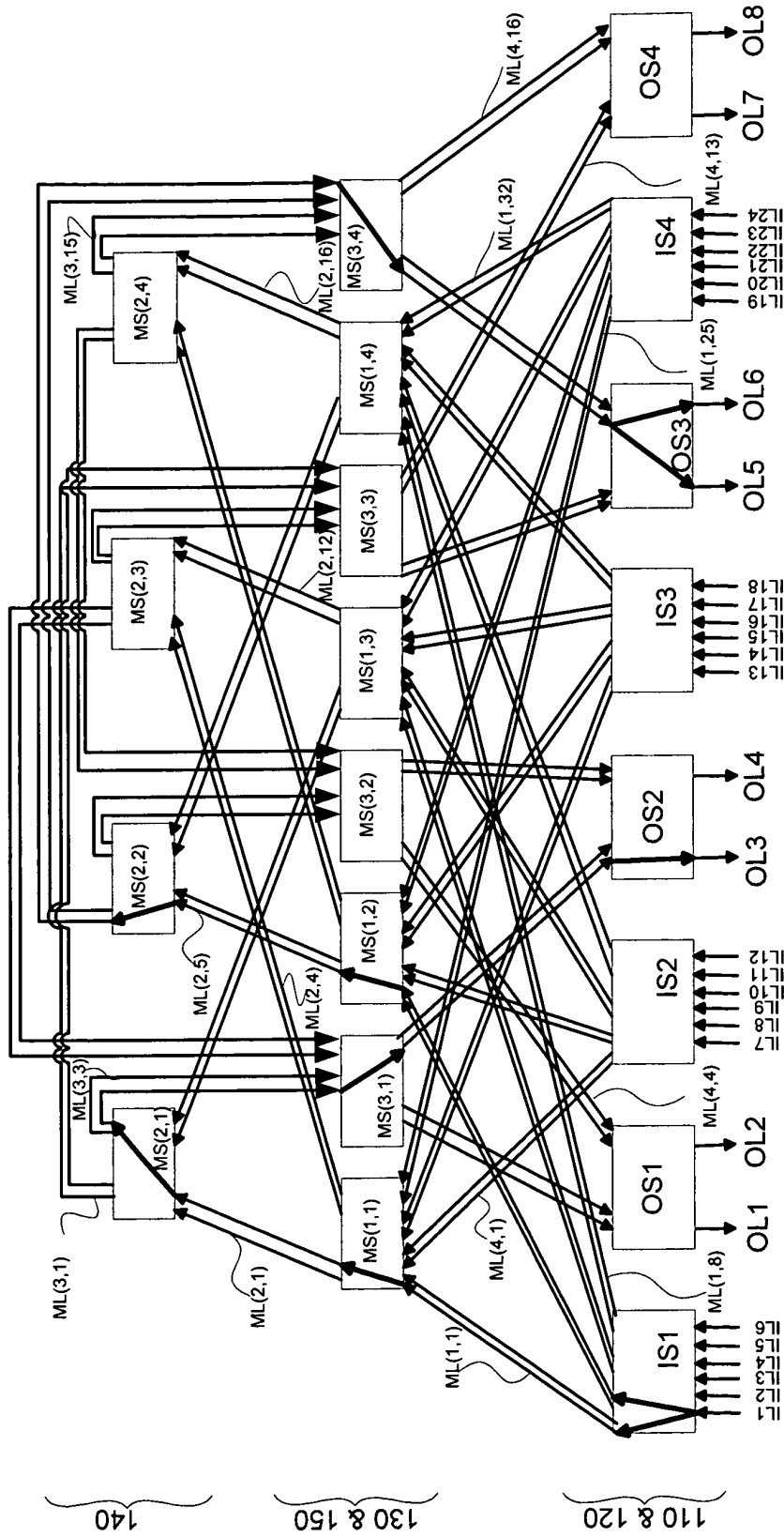


FIG. 3A

300A

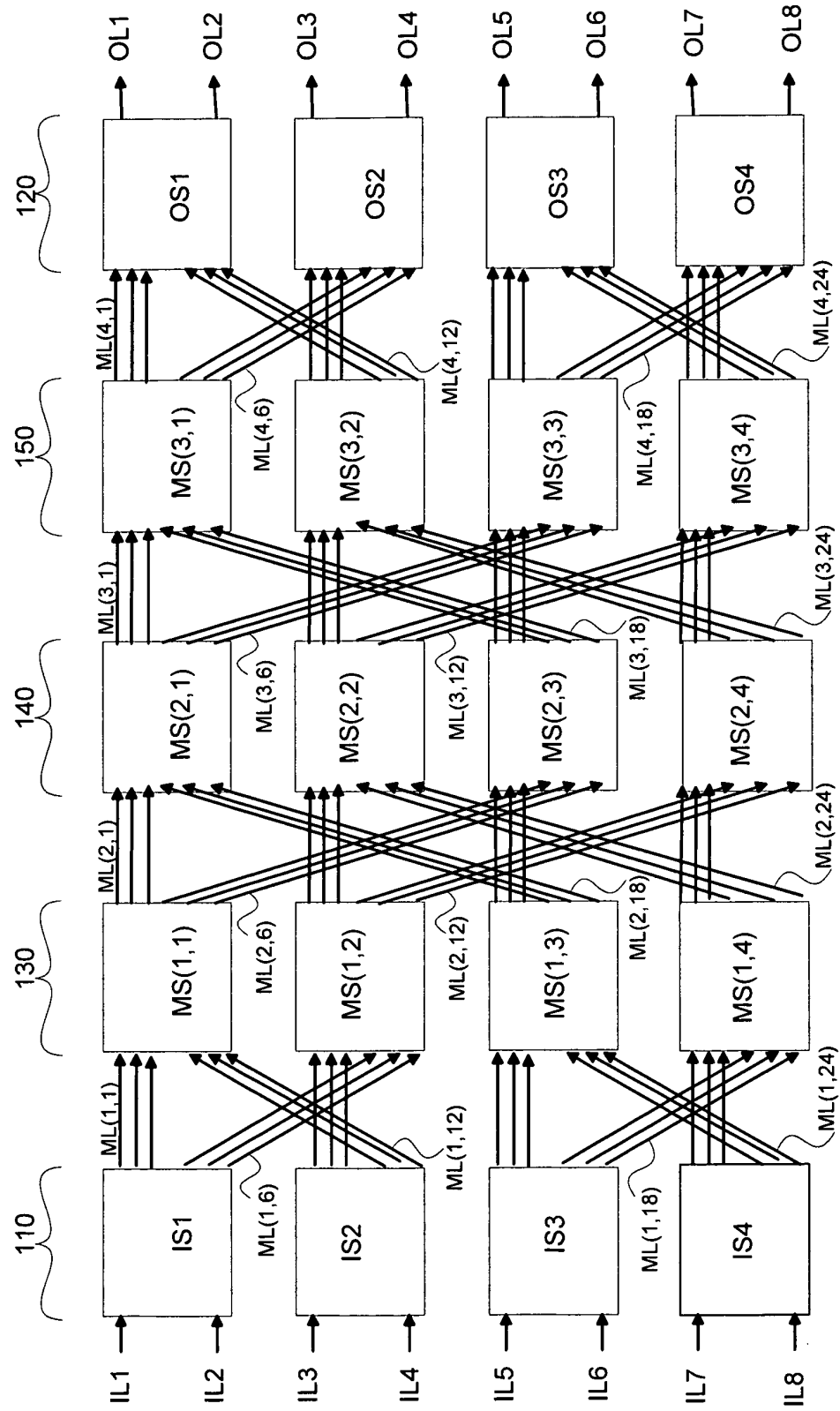


FIG. 3B

300B

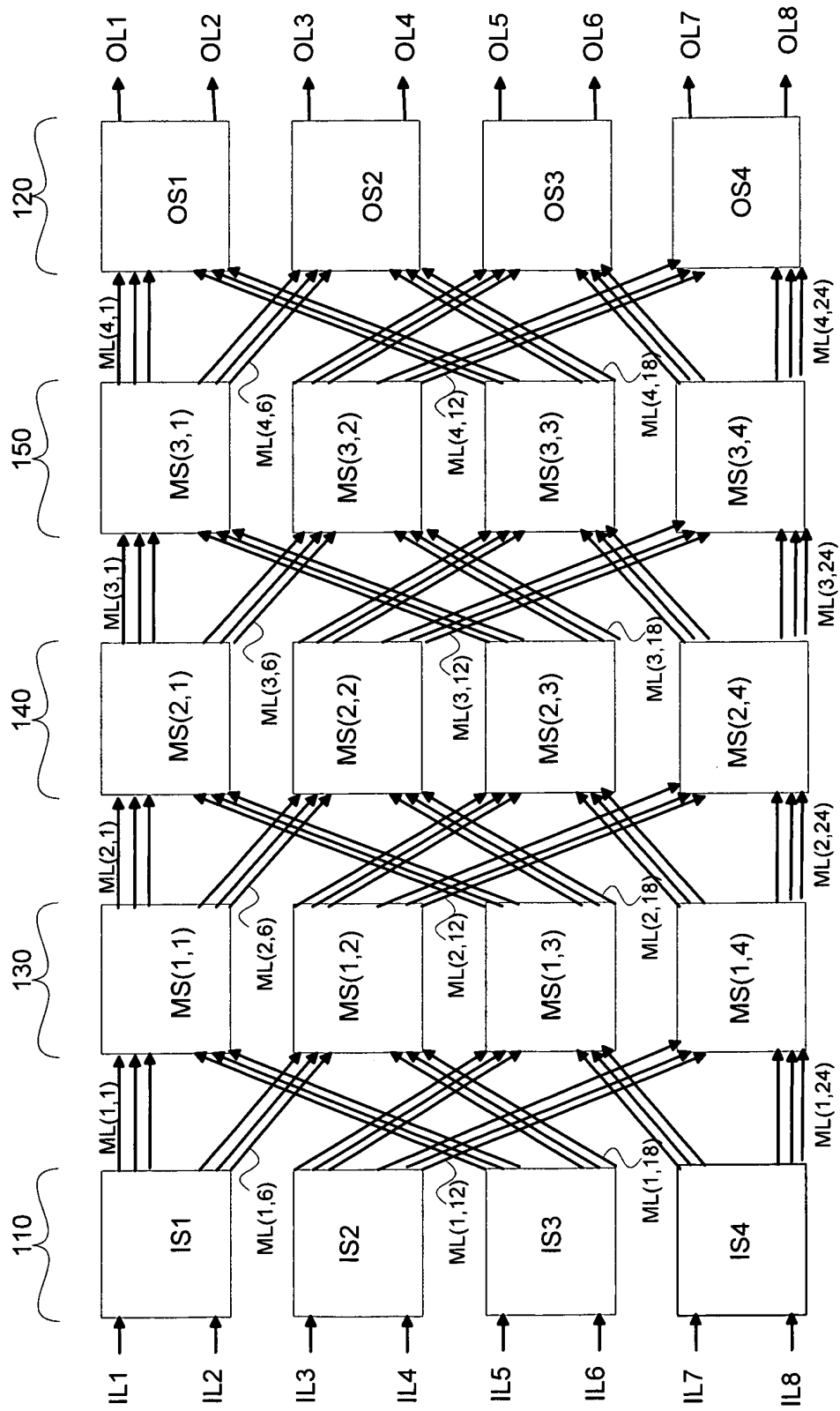


FIG. 3C

300C

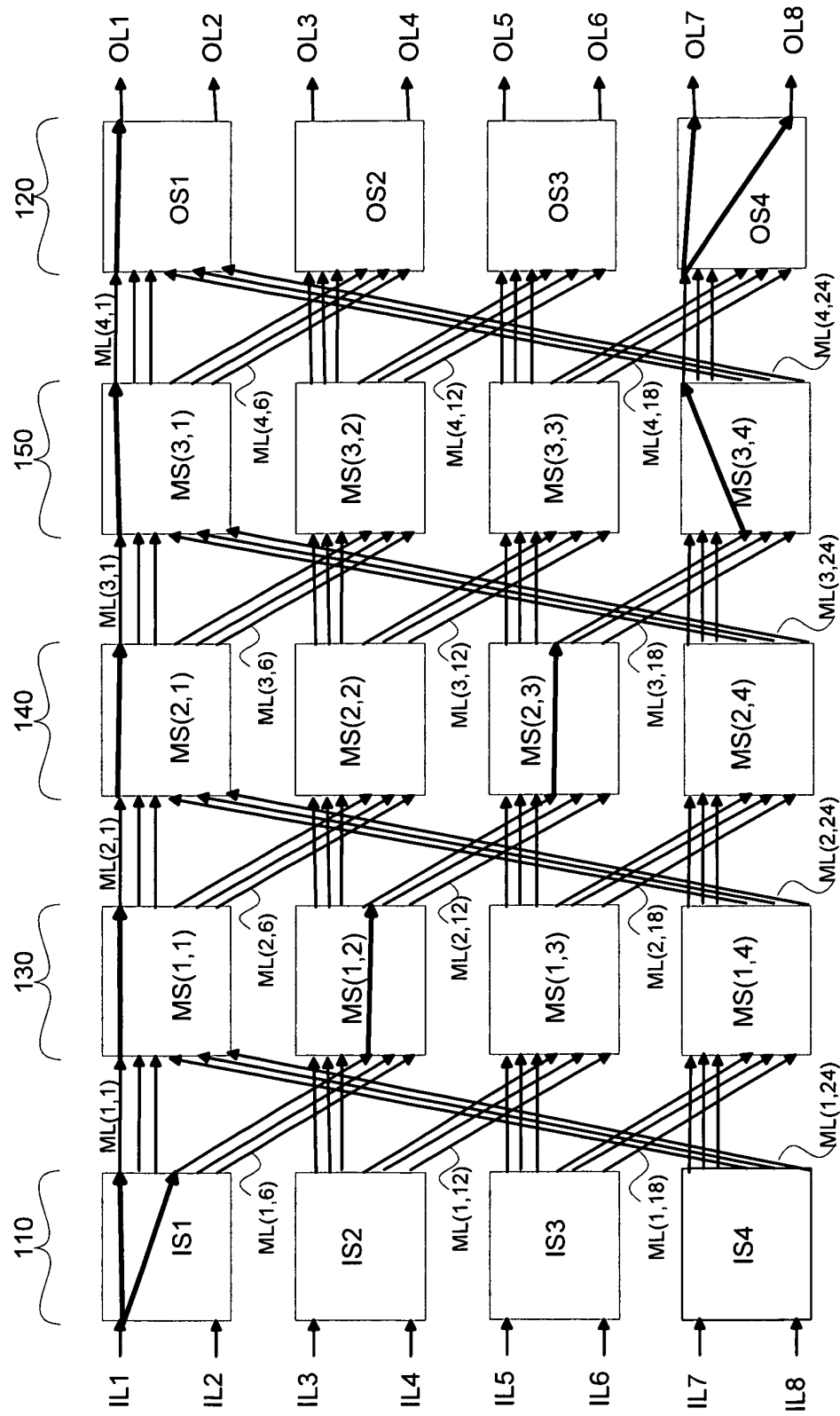


FIG. 3D

300D

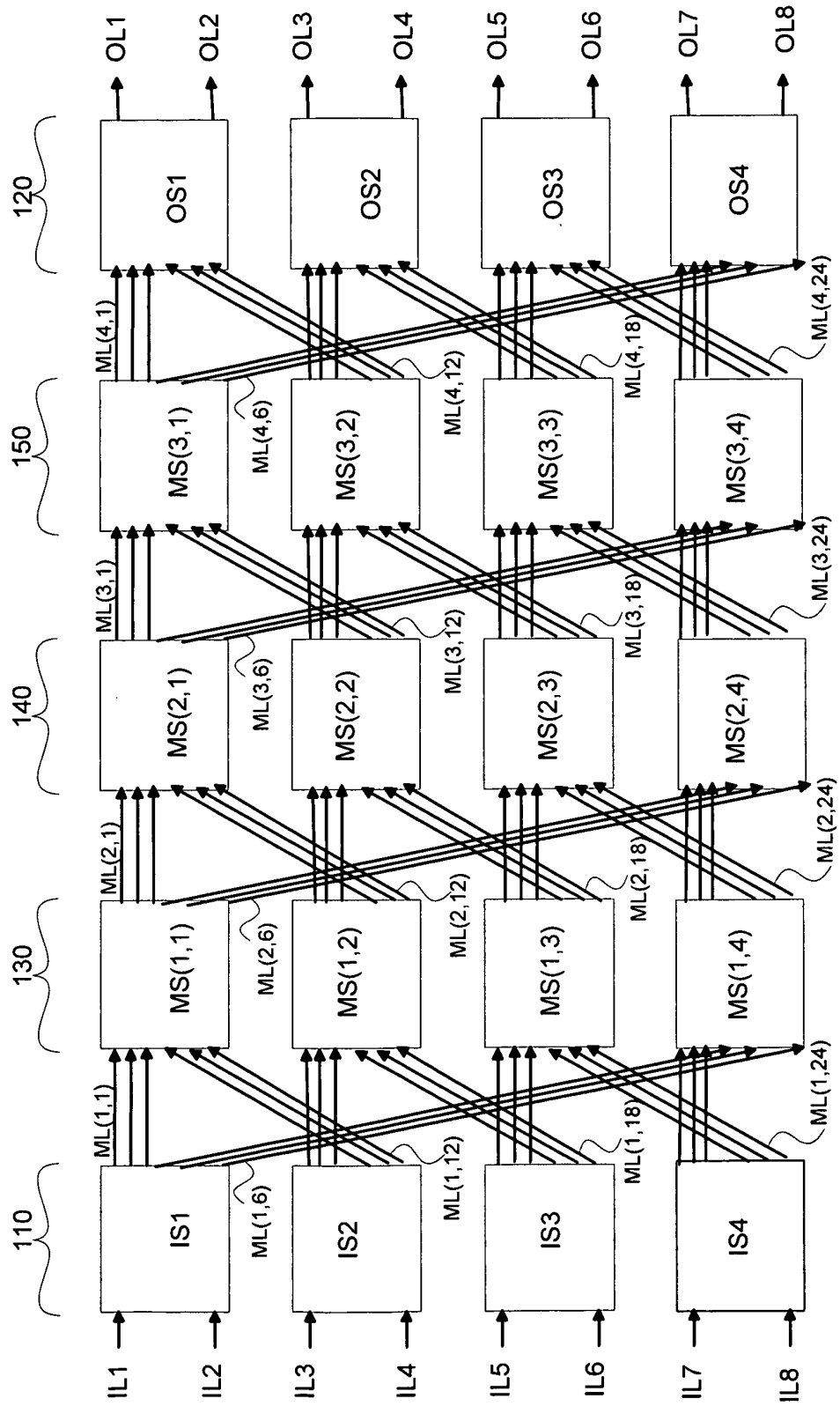


FIG. 3F

300F

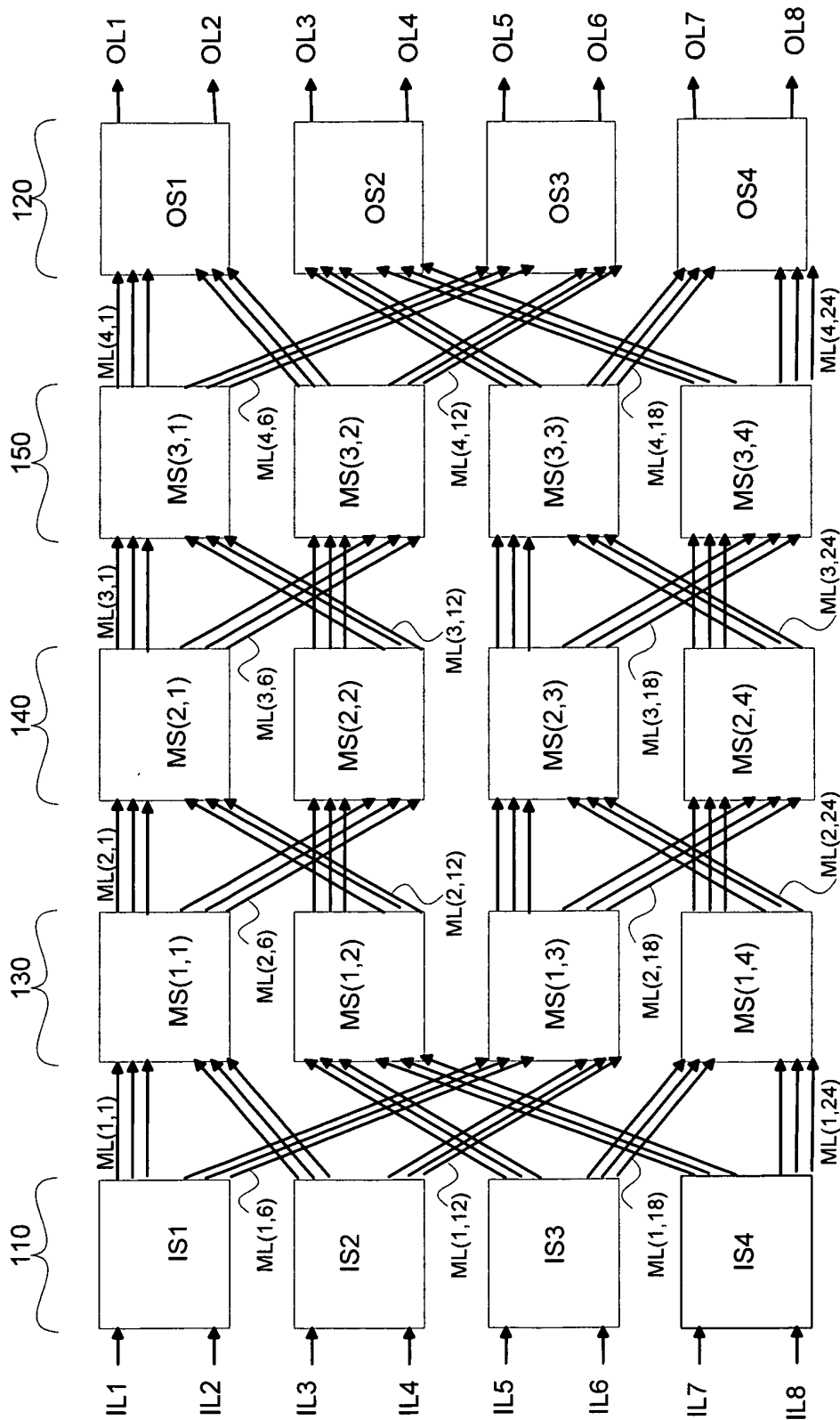


FIG. 3G

300G

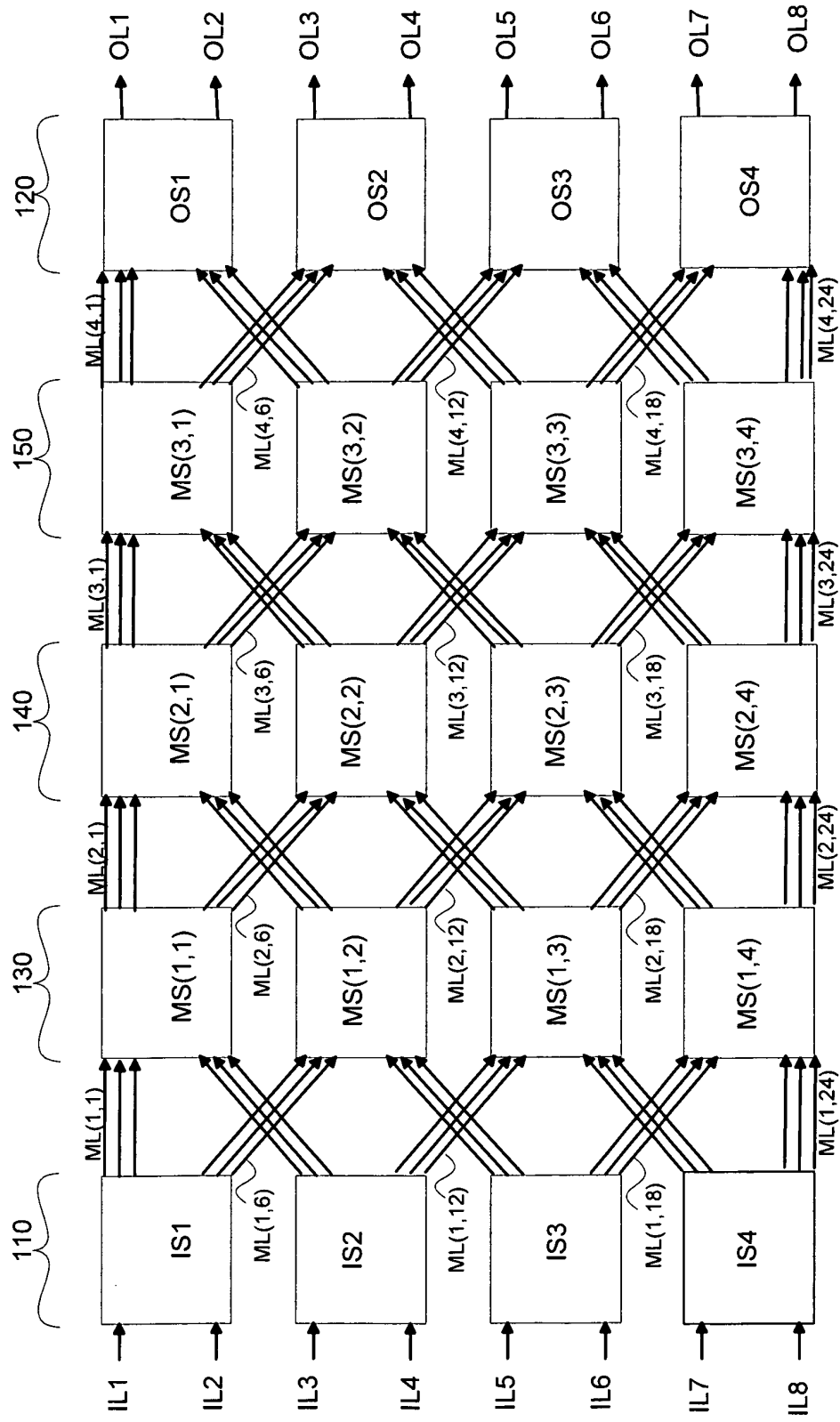


FIG. 3H

300H

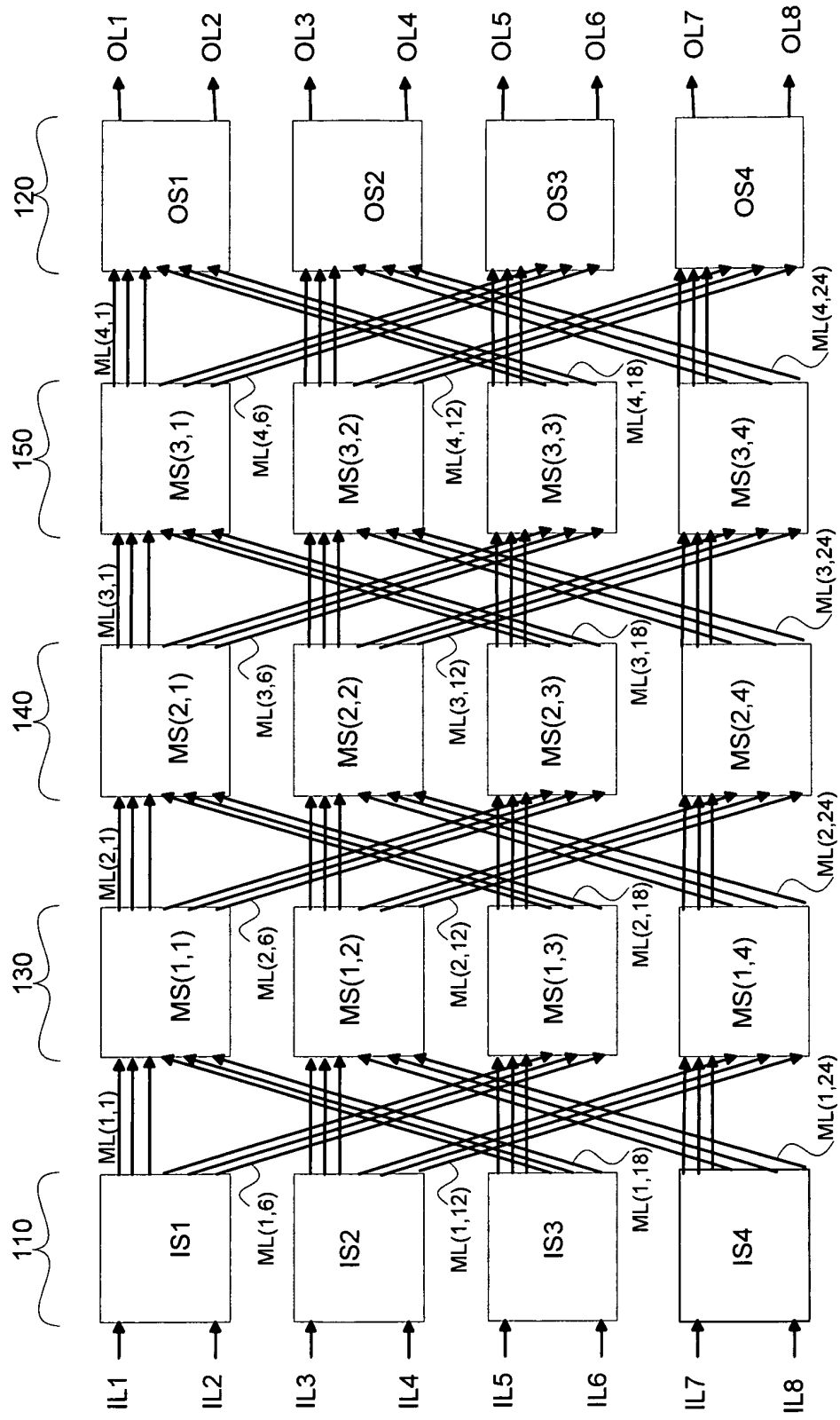


FIG. 31

300I

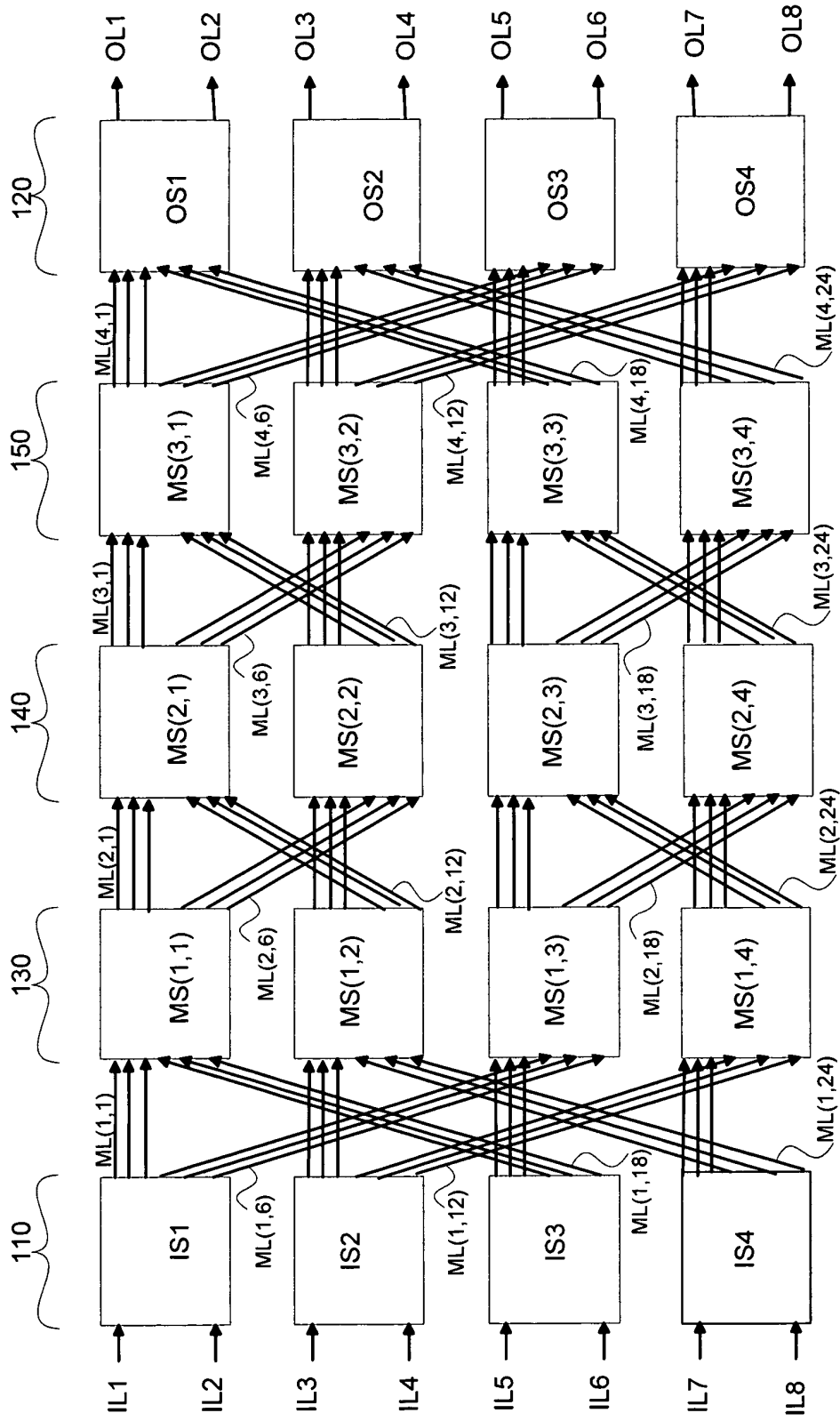


FIG. 3J

300J

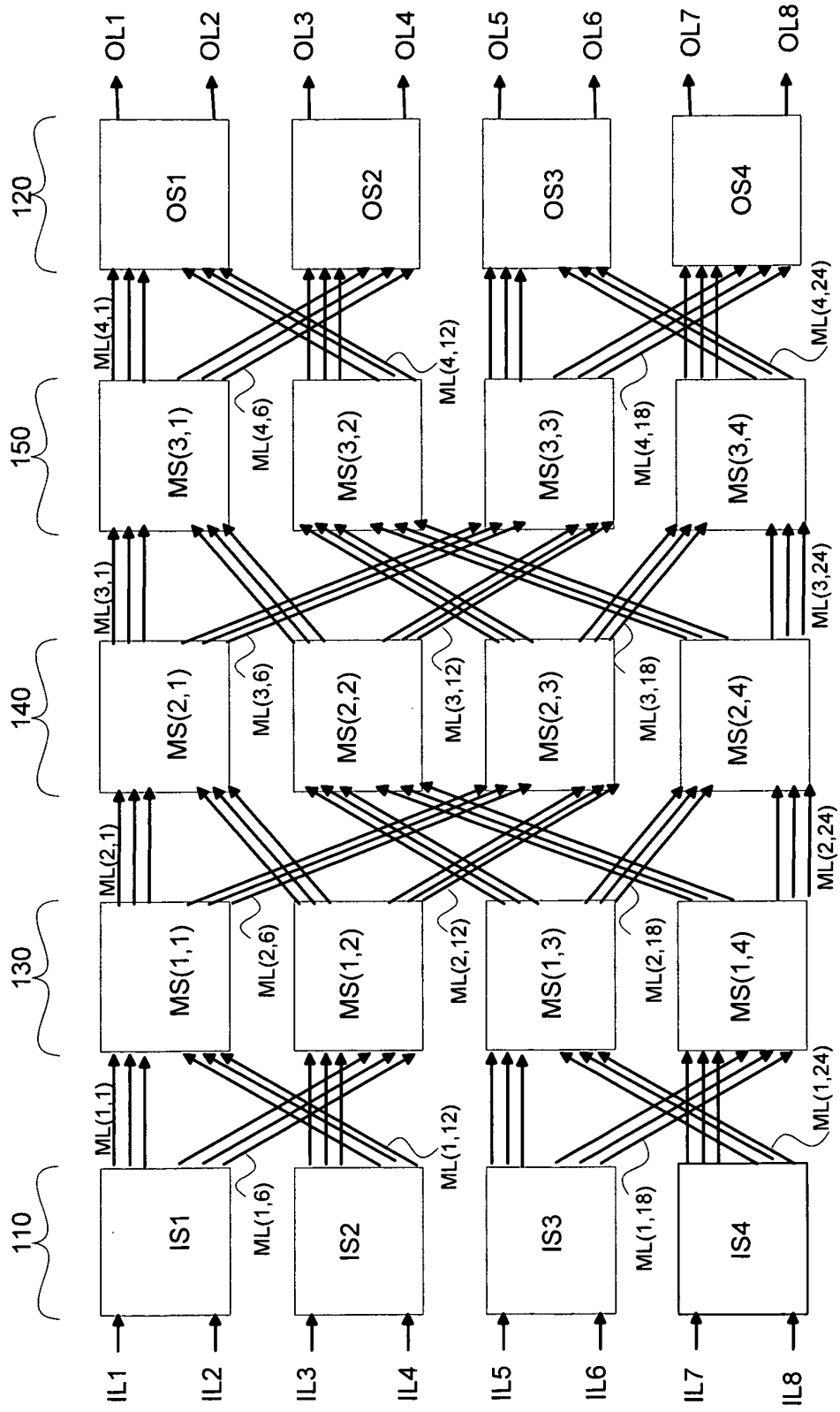


FIG. 3K

300K

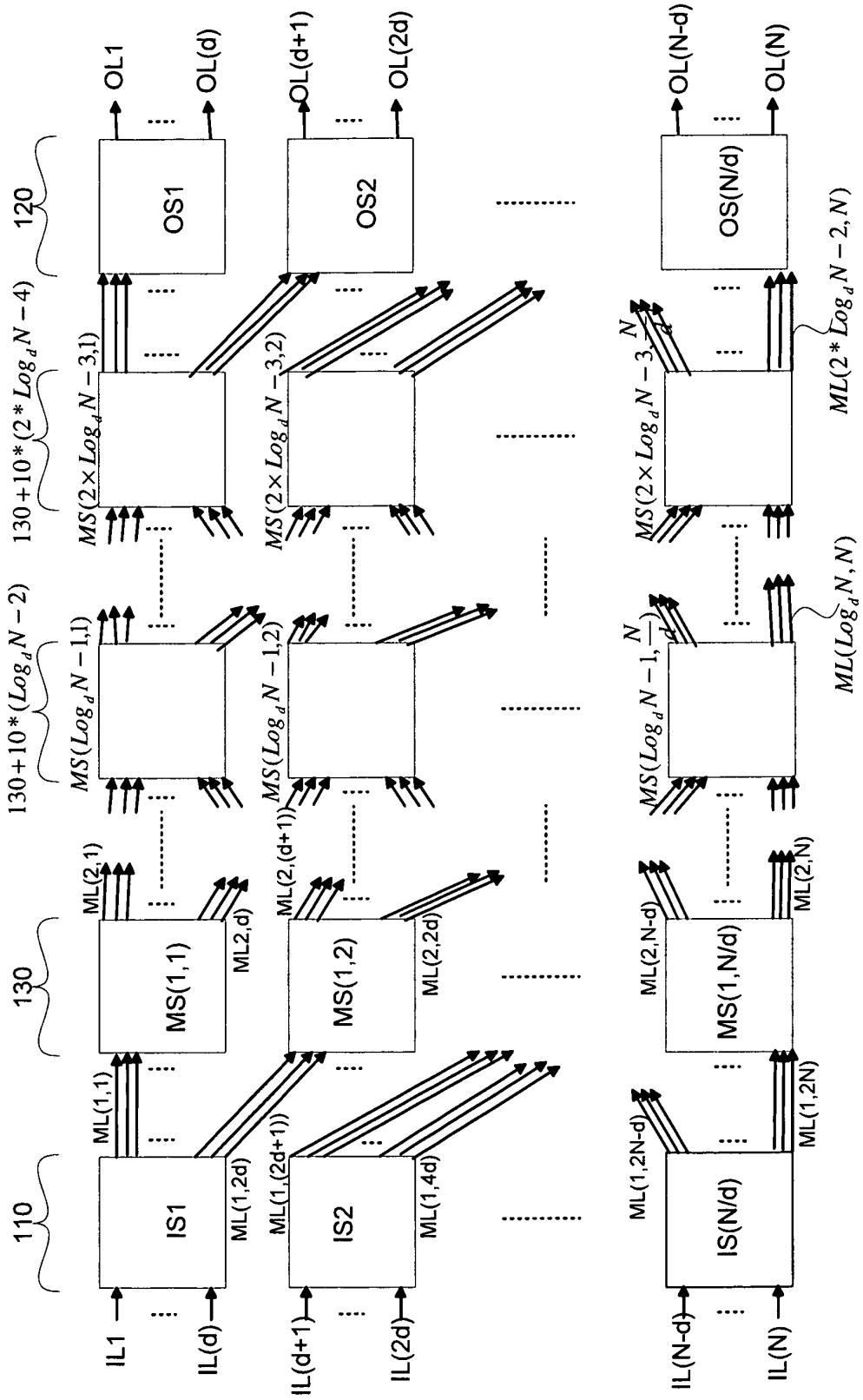


FIG. 3A1

300A1

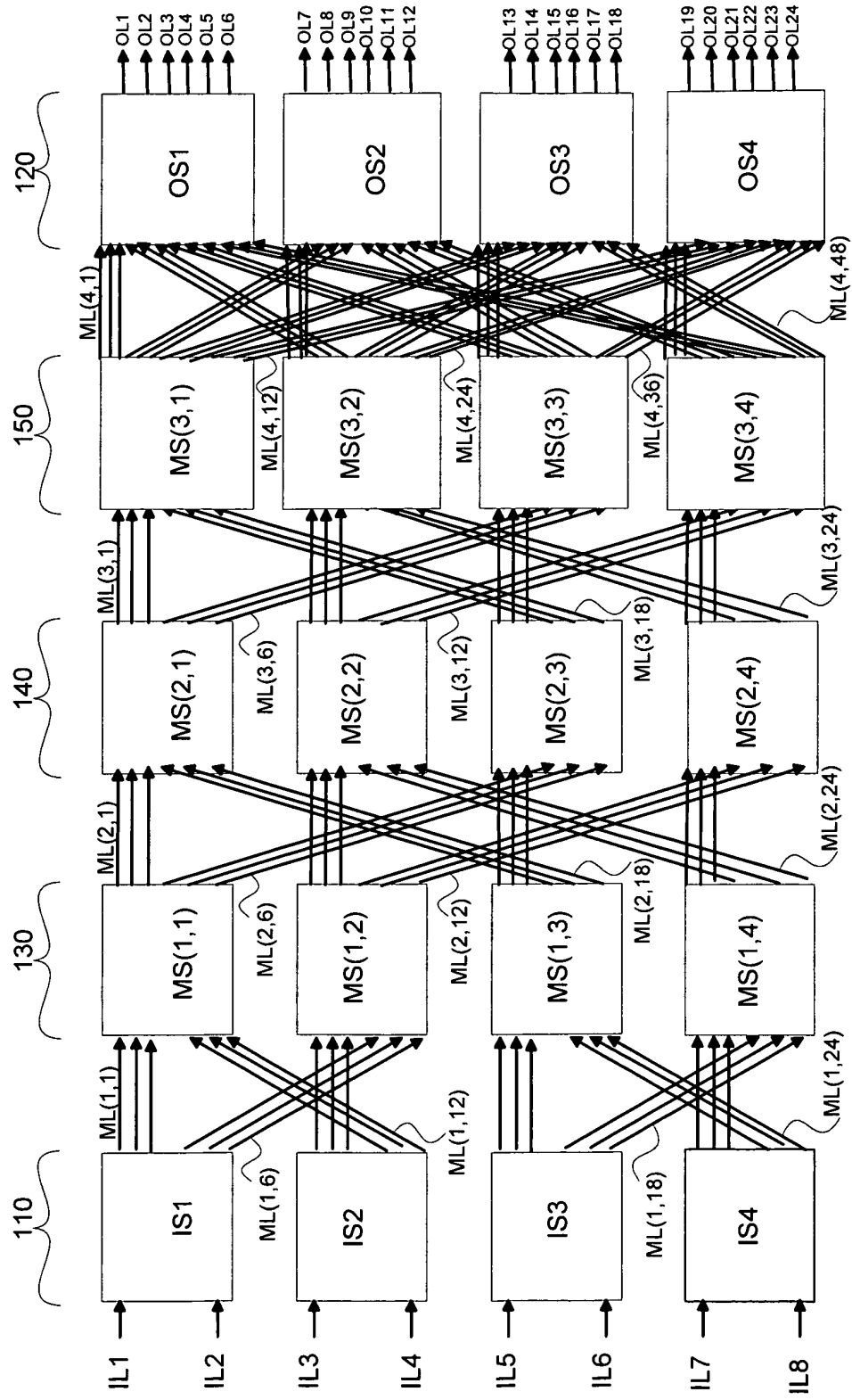


FIG. 3B1

300B1

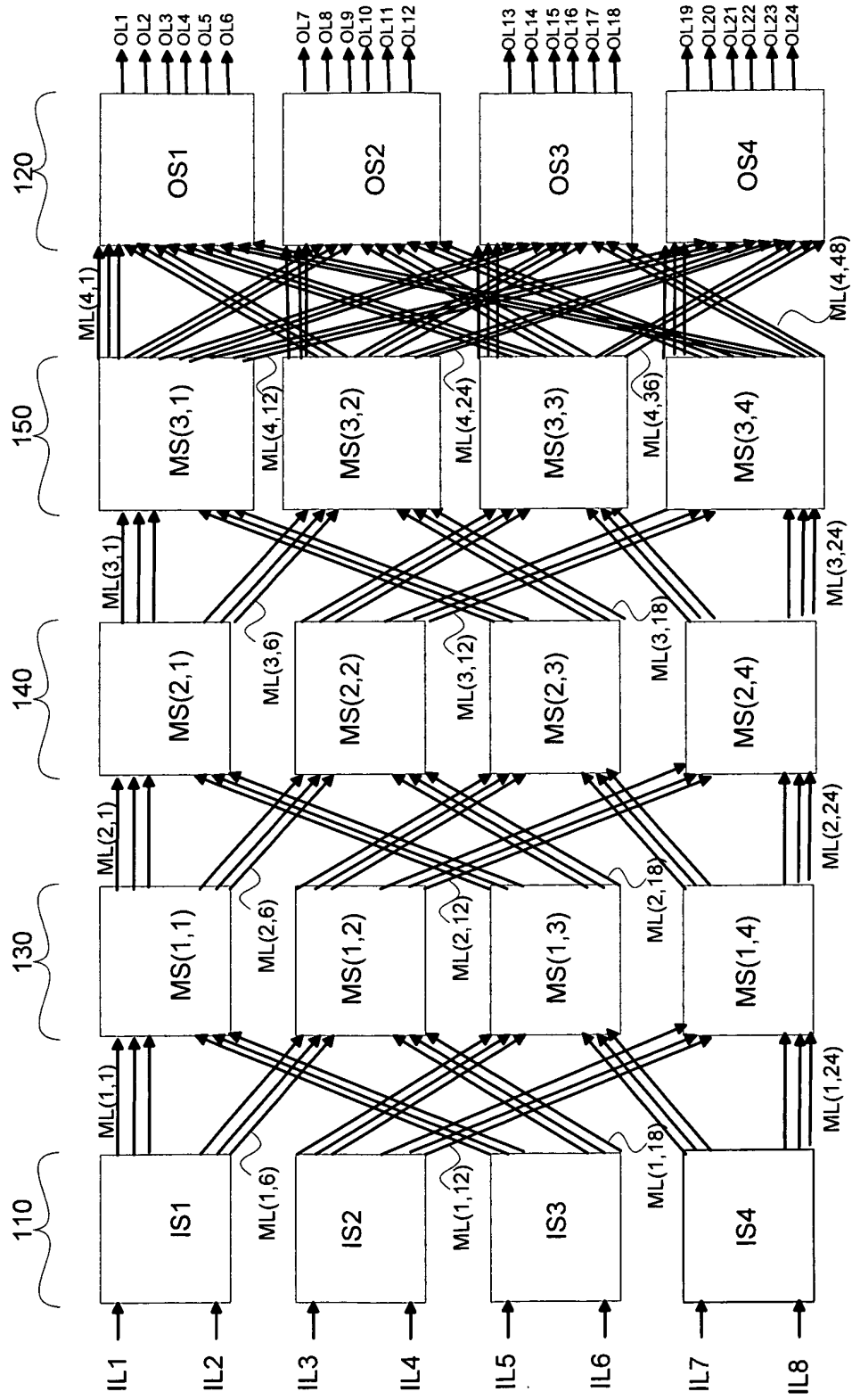


FIG. 3C1

300C1

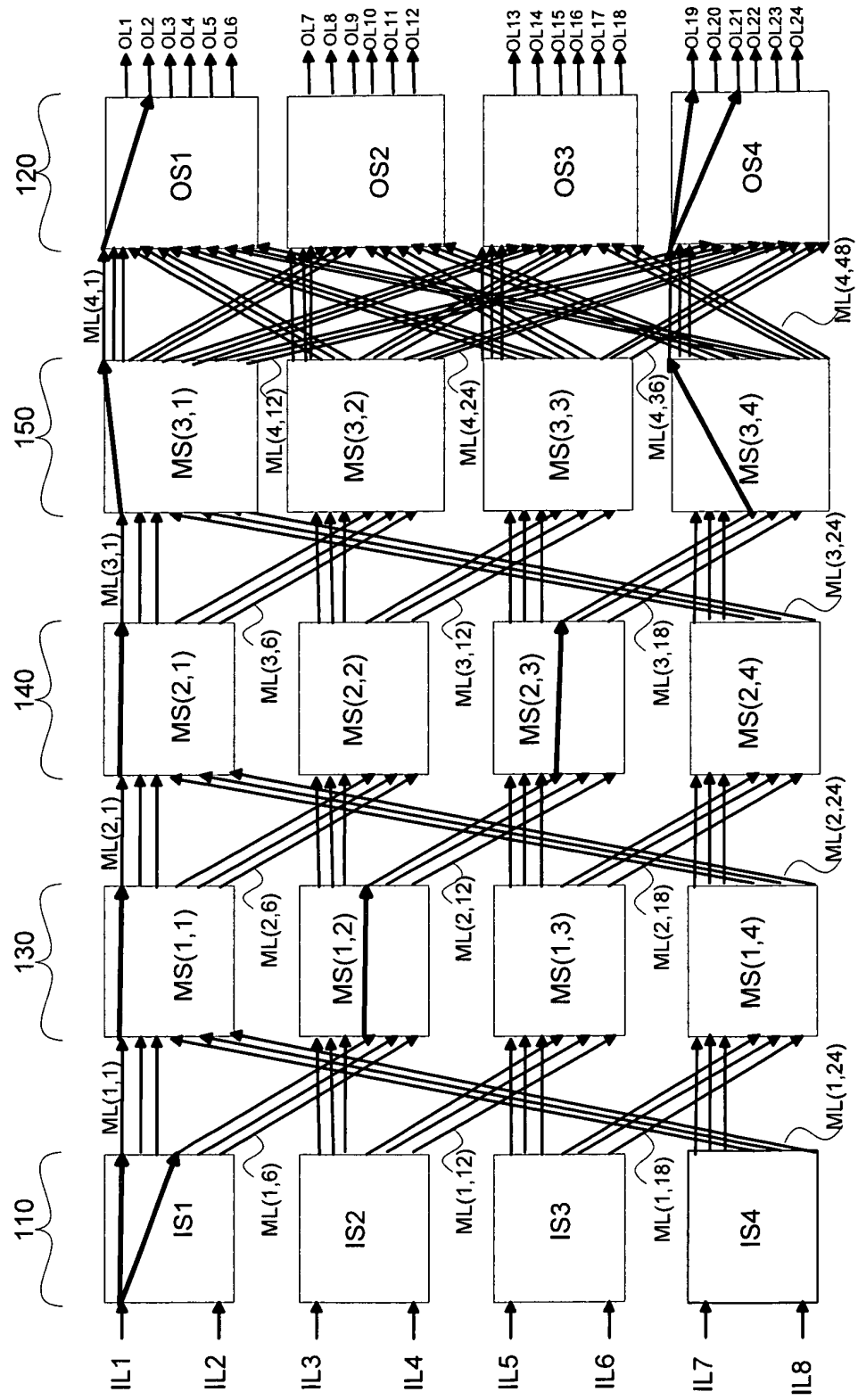


FIG. 3D1

300D1

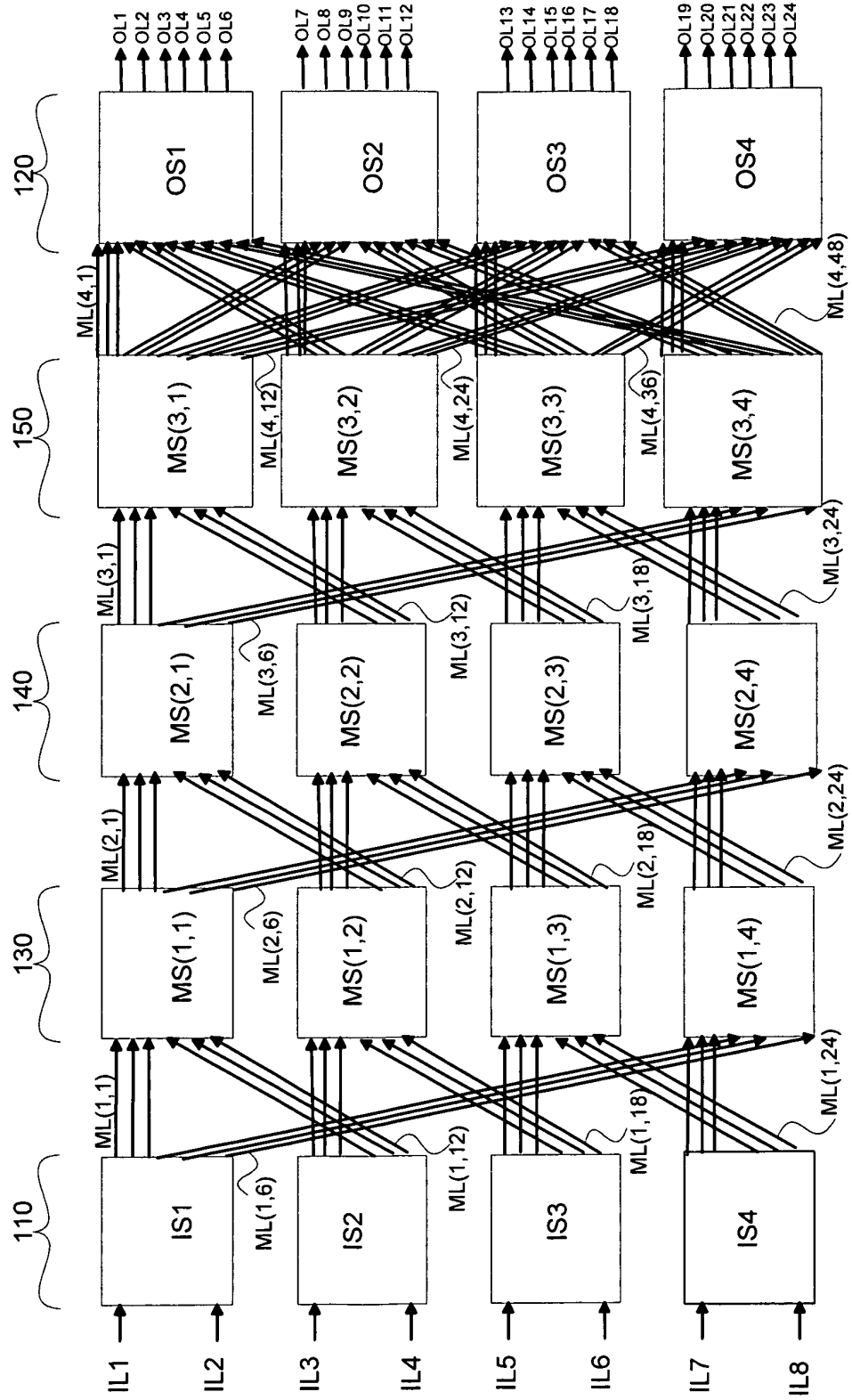
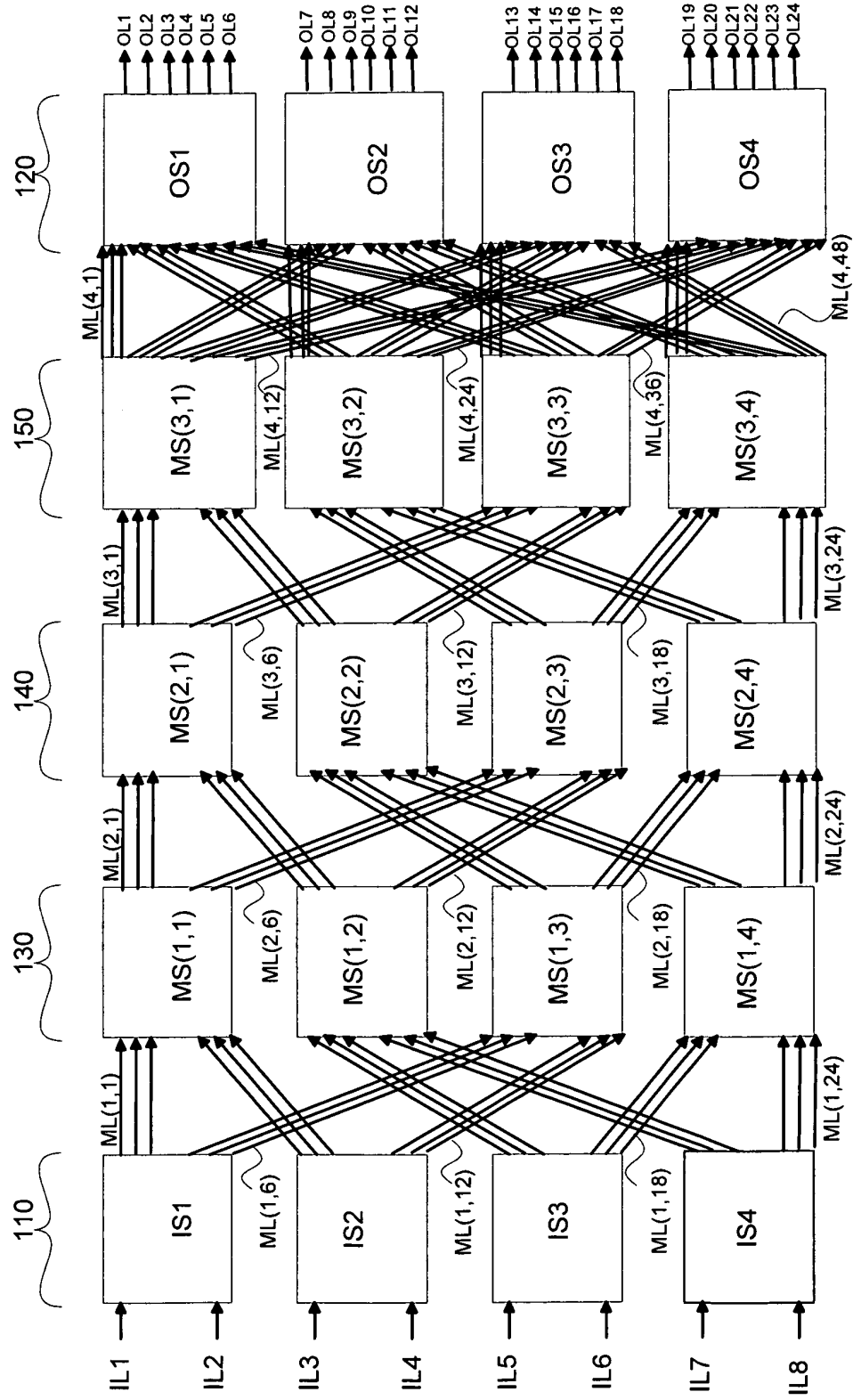


FIG. 3E1

300E1



300F1

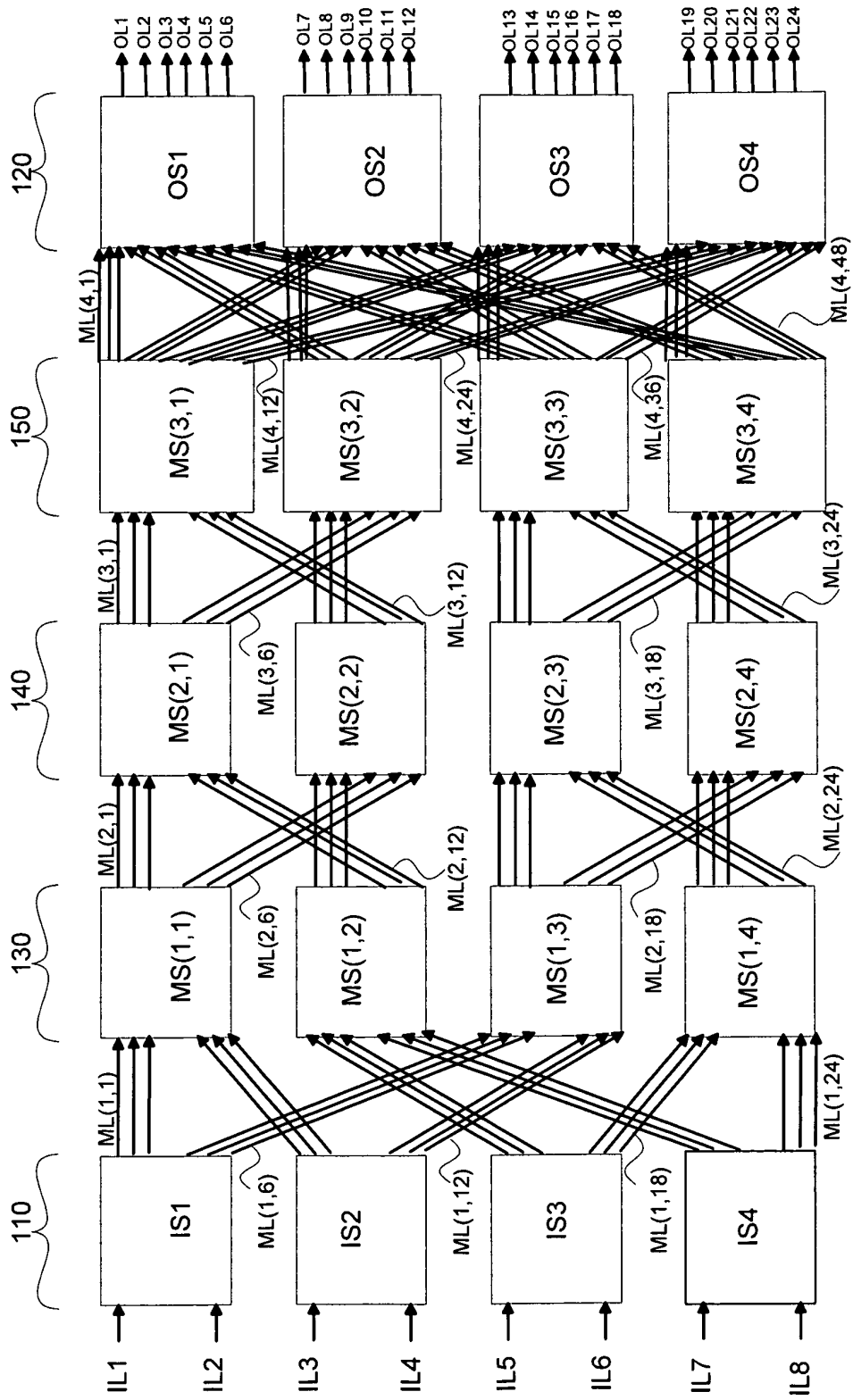


FIG. 3G1

300G1

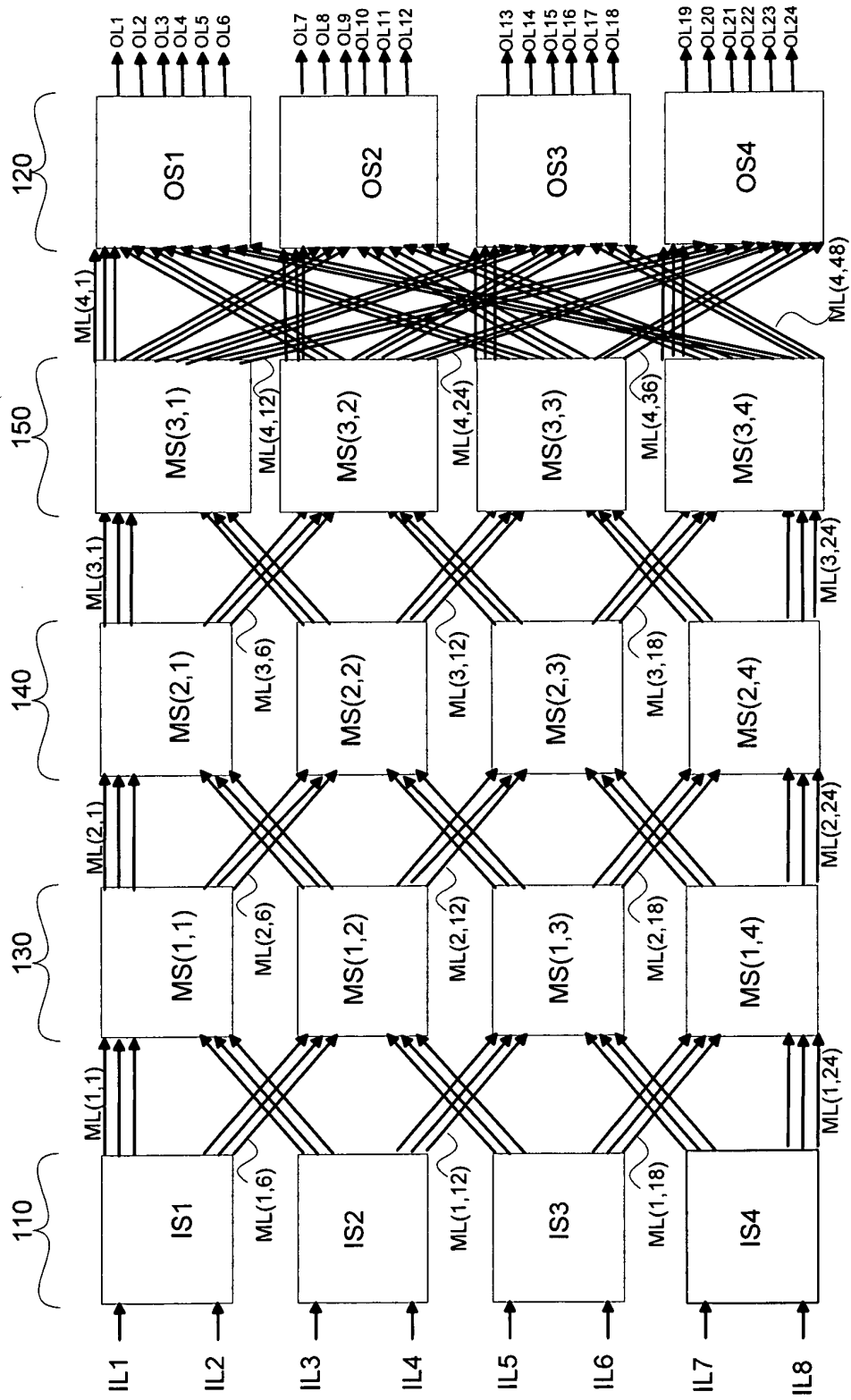


FIG. 3H1

300H1

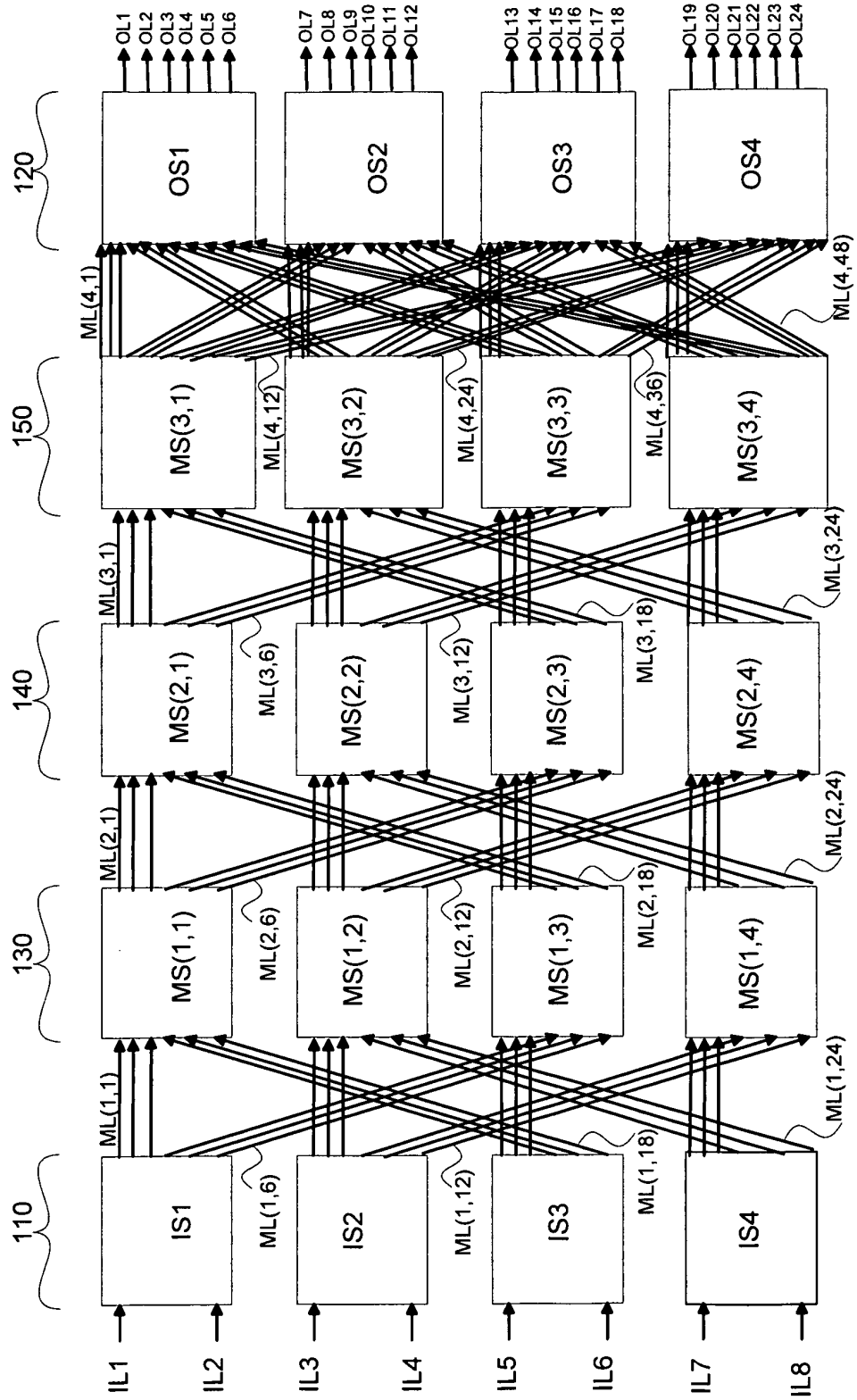


FIG. 311

30011

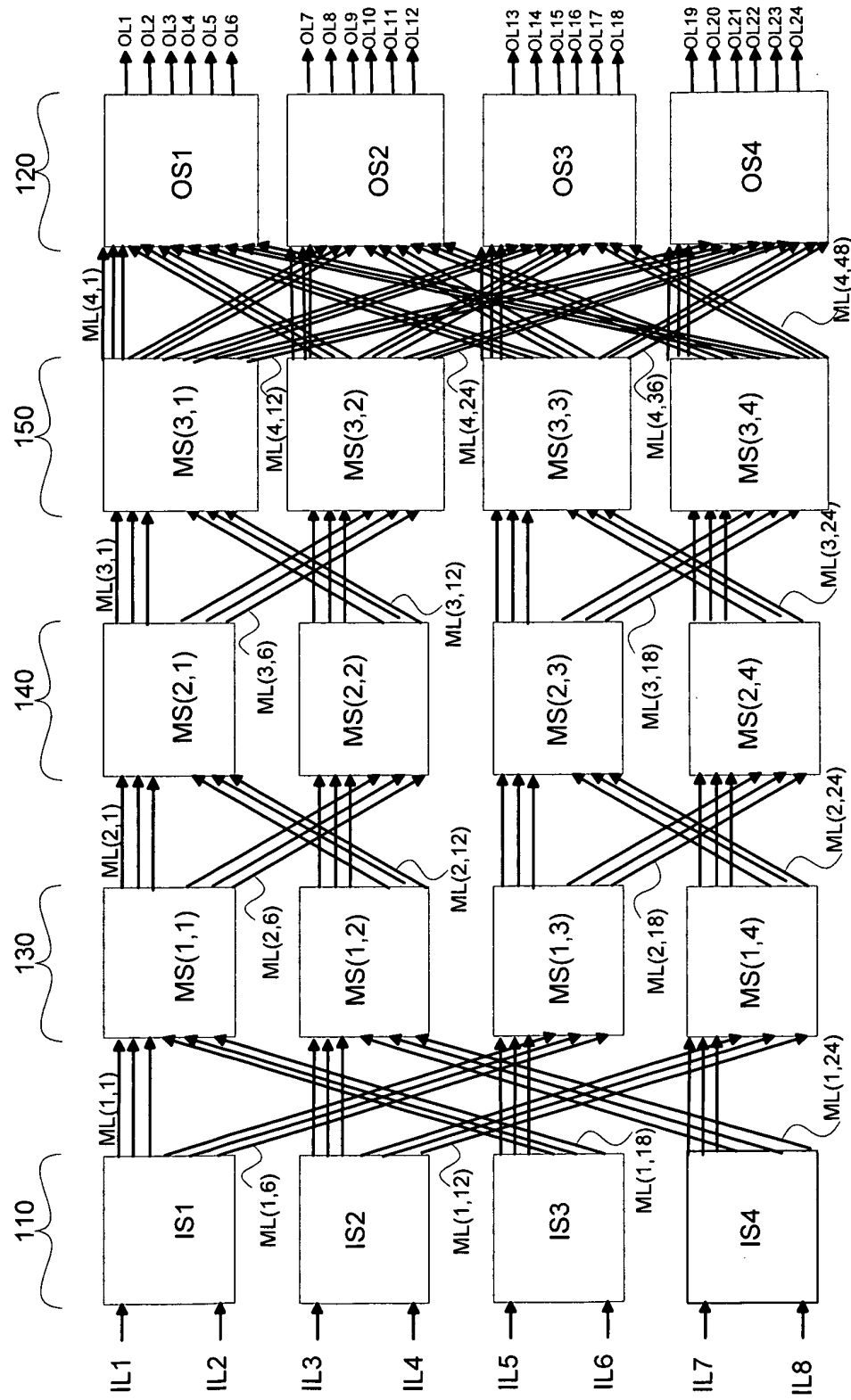


FIG. 3J1

300,J1

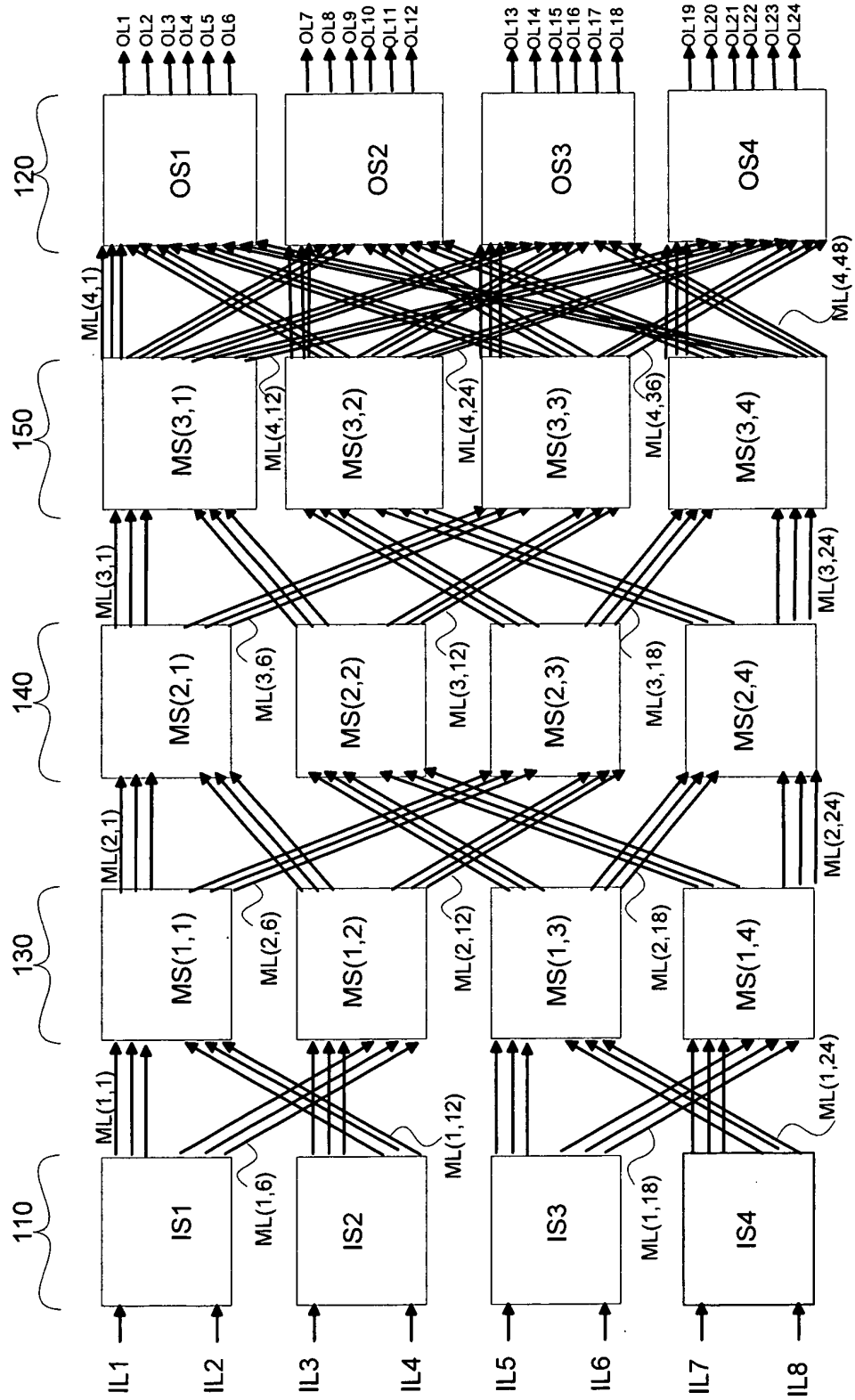


FIG. 3K1

300K1

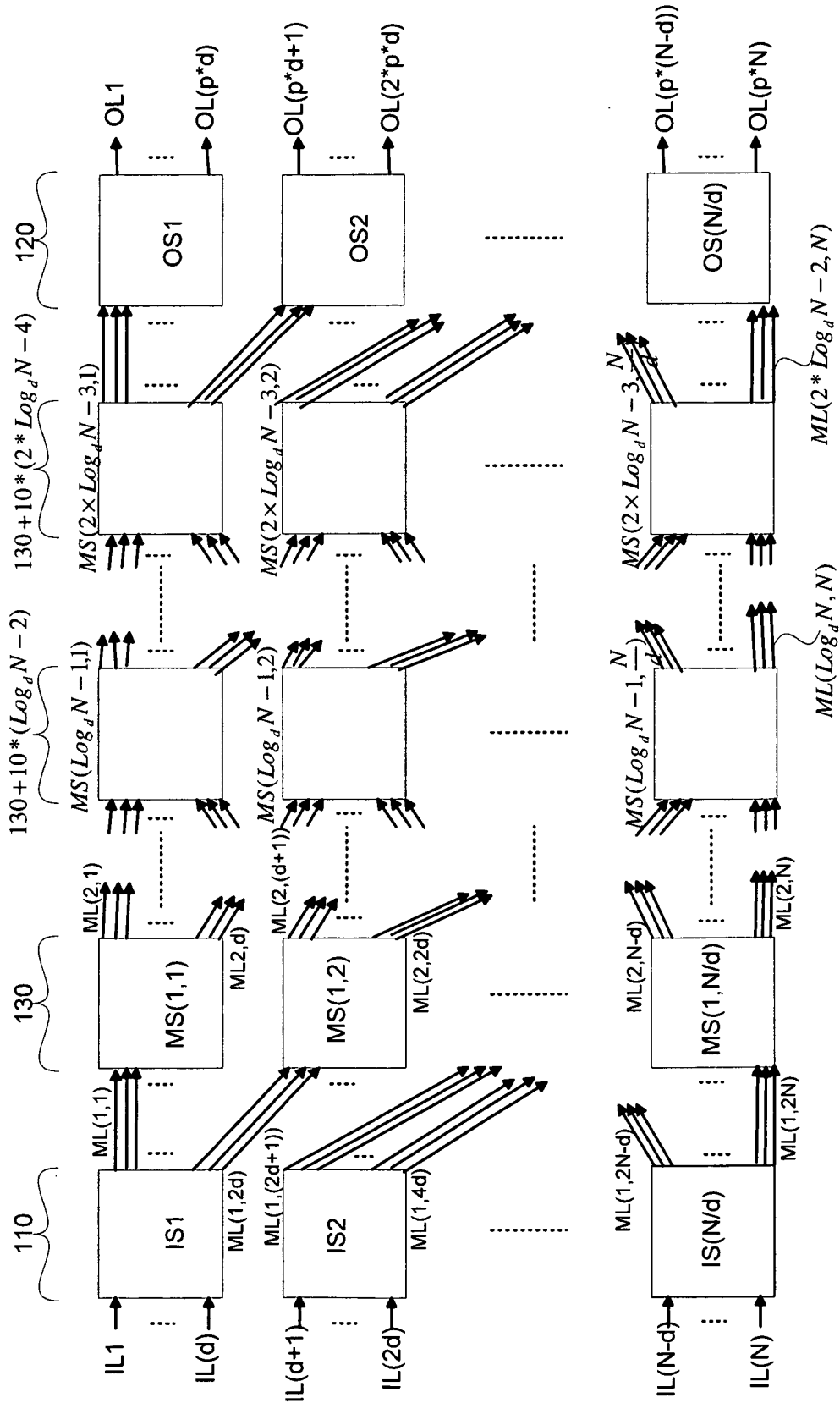


FIG. 3A2

300A2

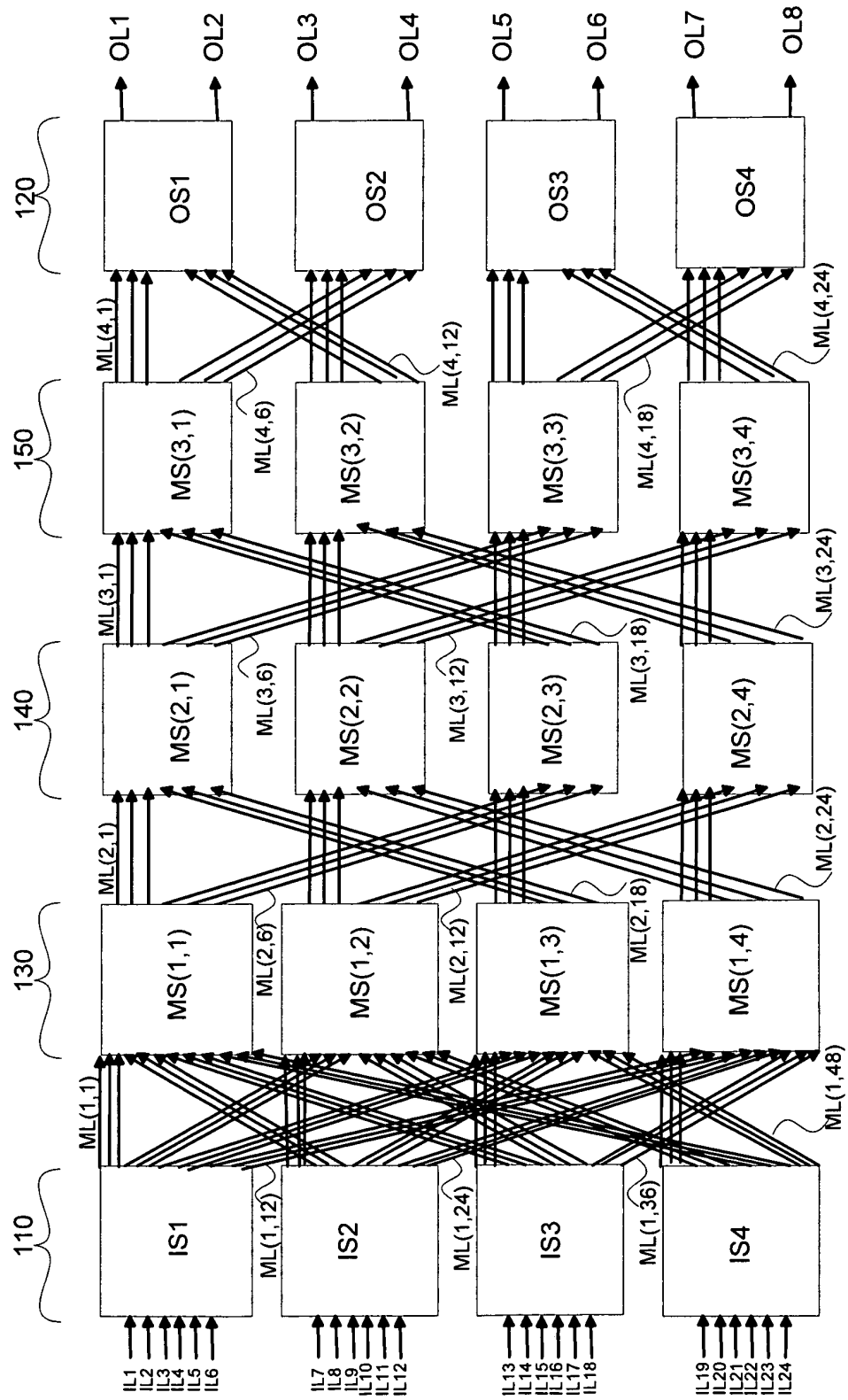


FIG. 3B2

300B2

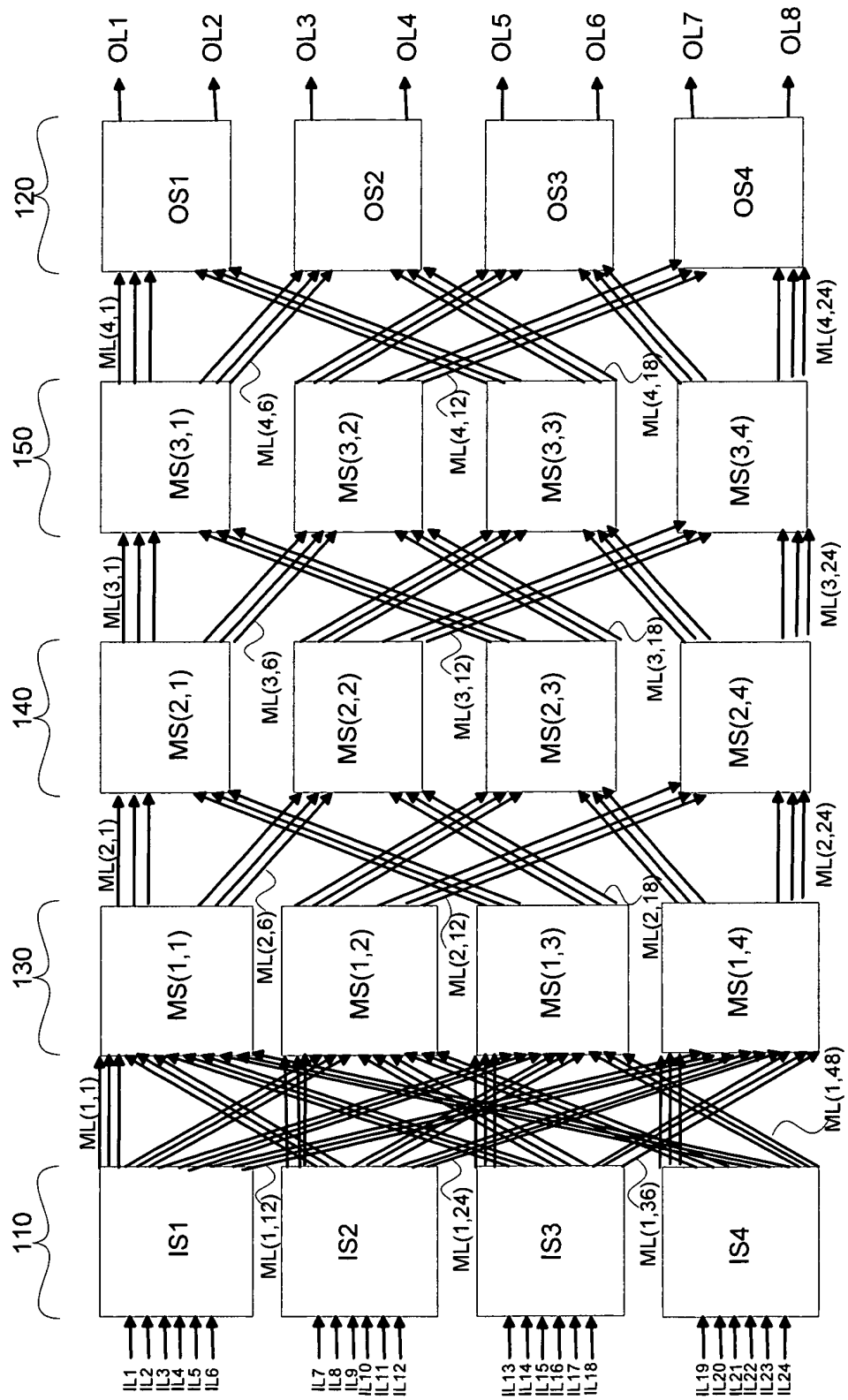


FIG. 3C2

300C2

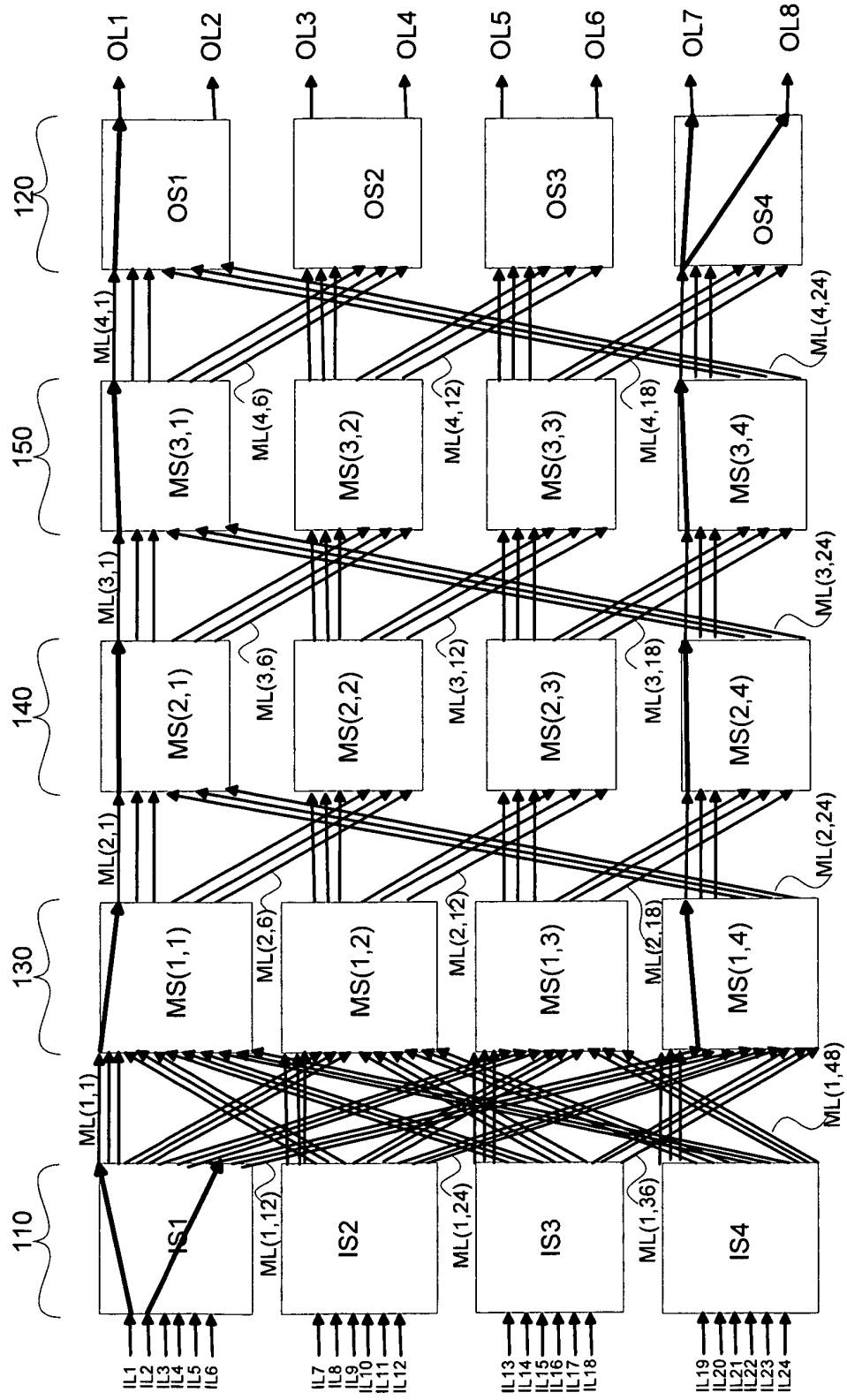


FIG. 3D2

300D2

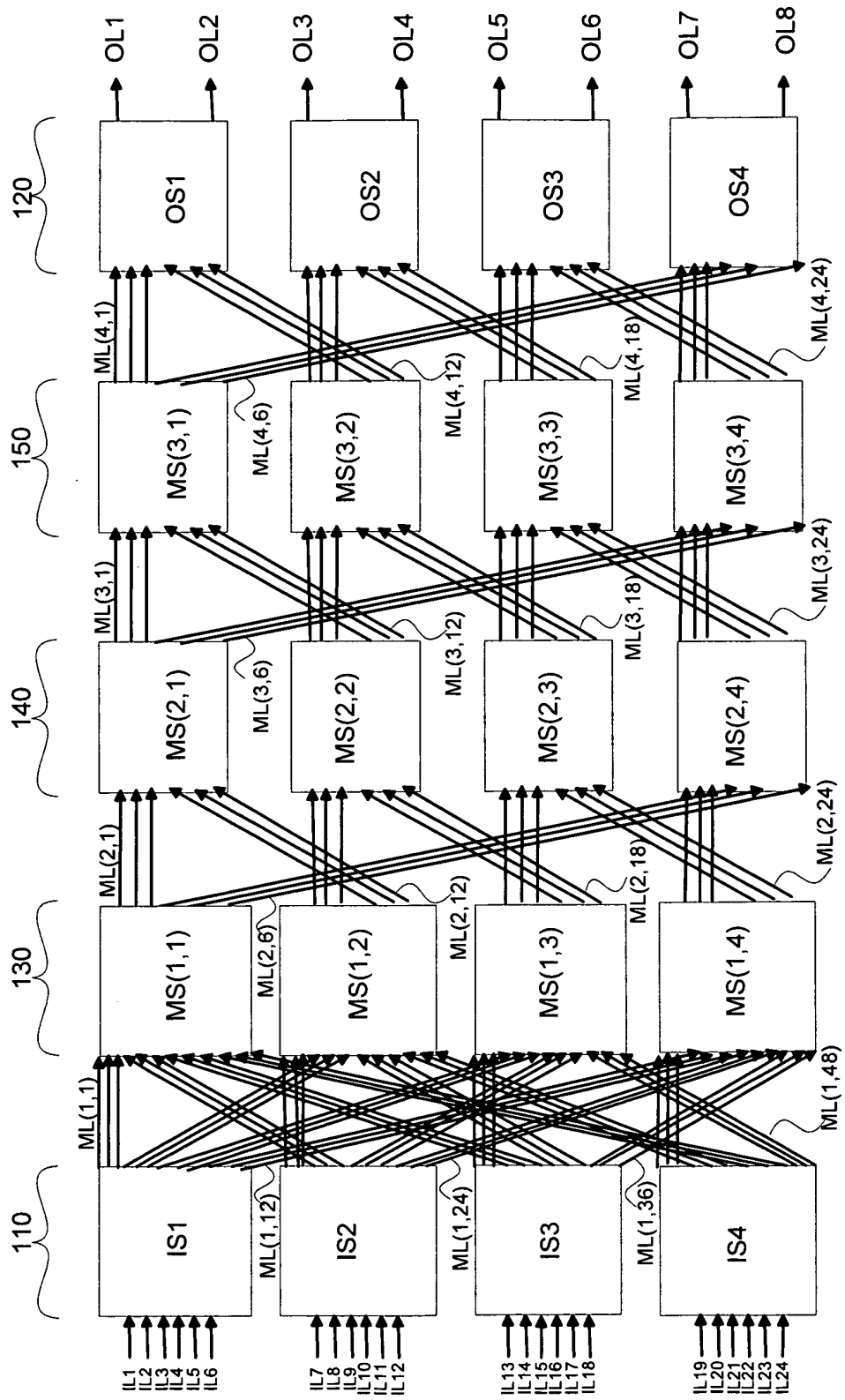


FIG. 3E2

300E2

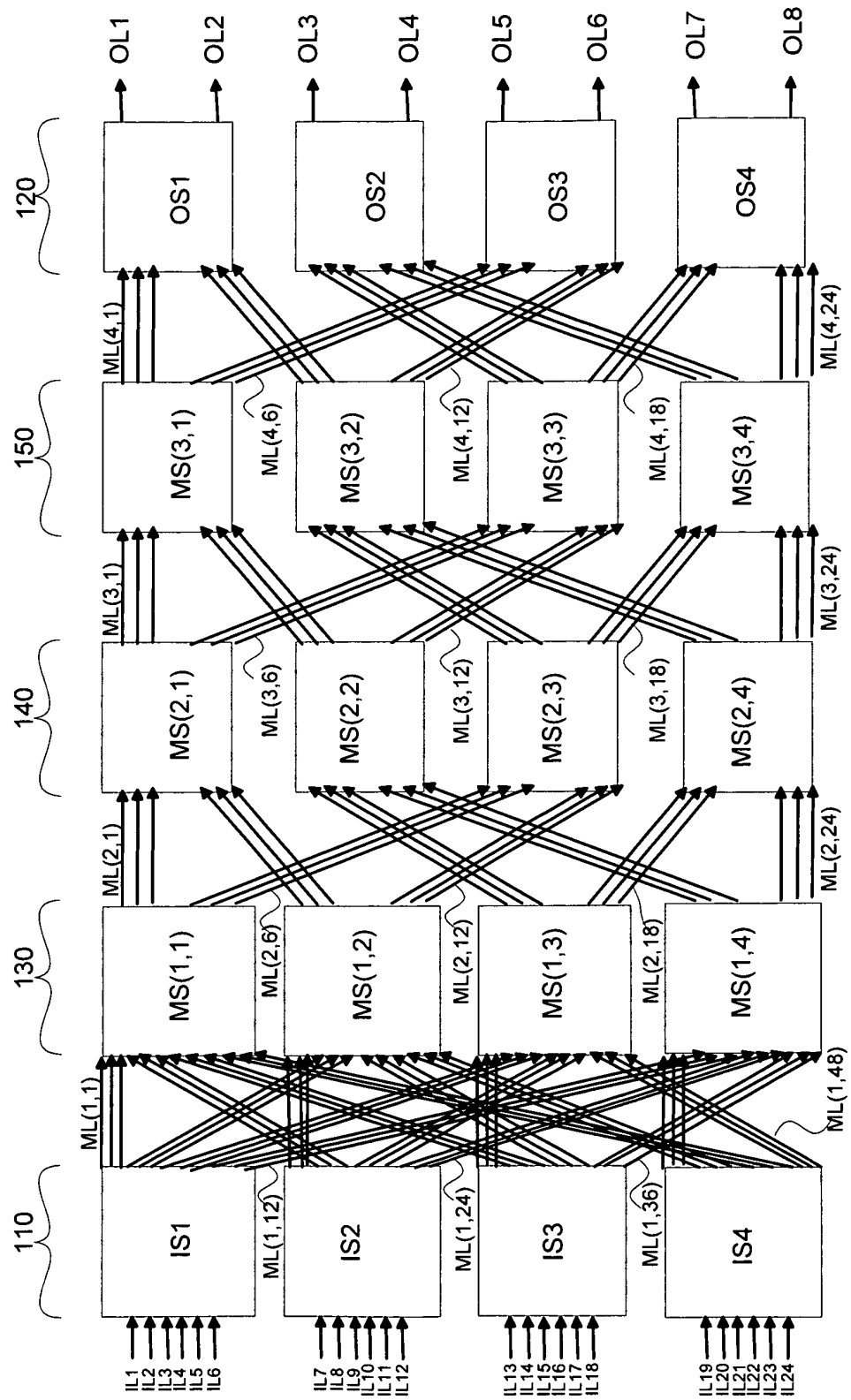


FIG. 3F2

300F2

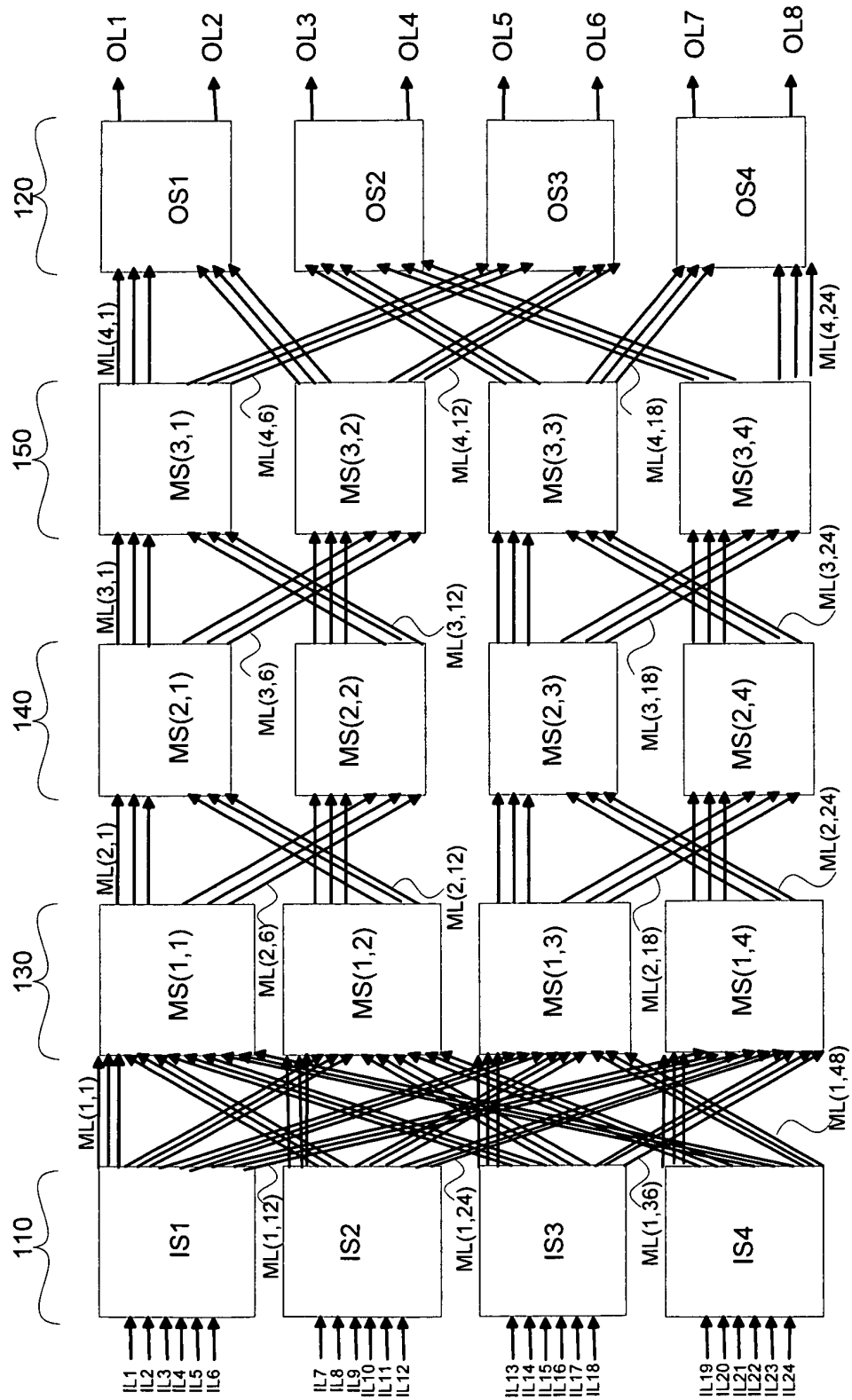


FIG. 3G2

300G2

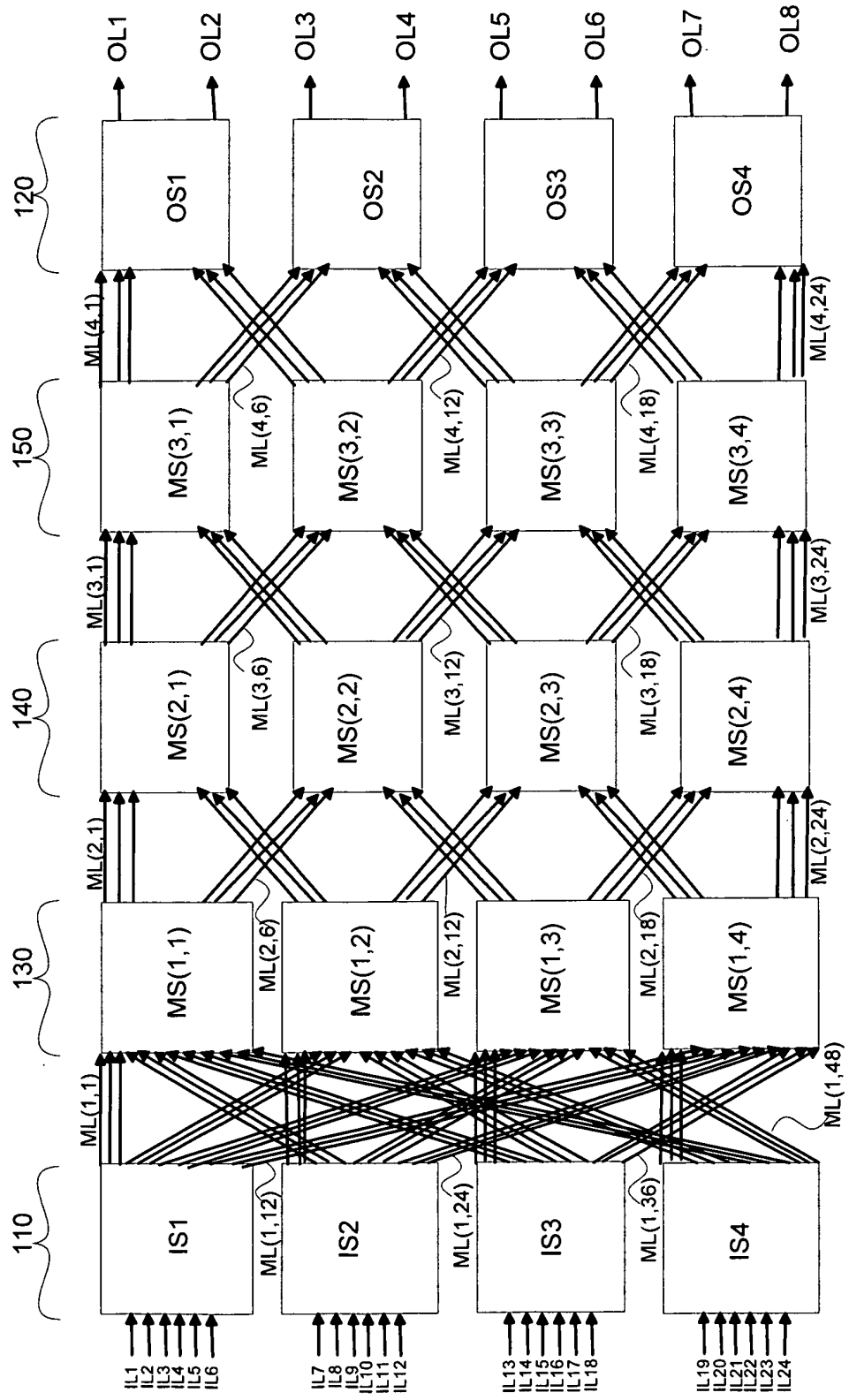


FIG. 3H2

300H2

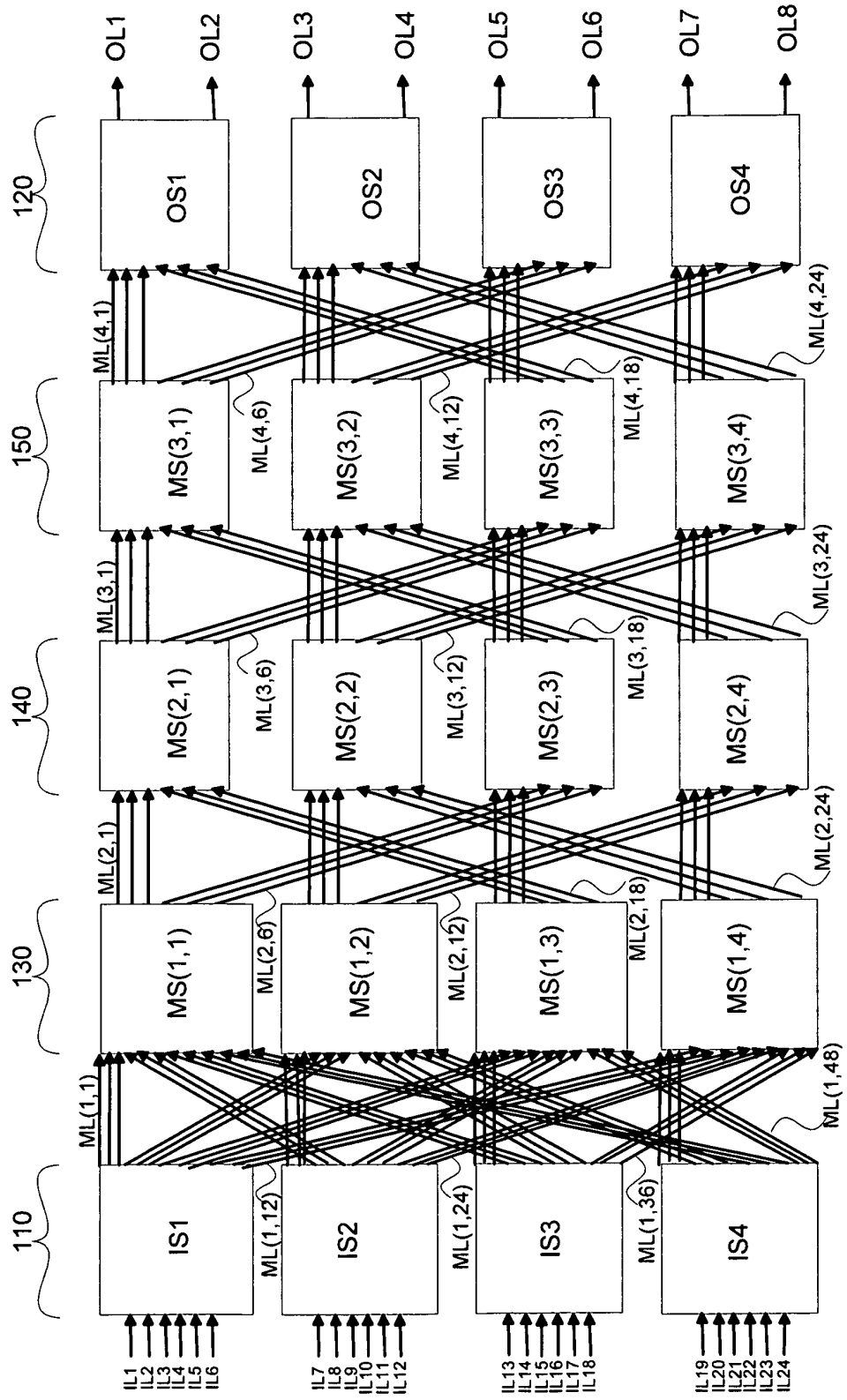


FIG. 312

30012

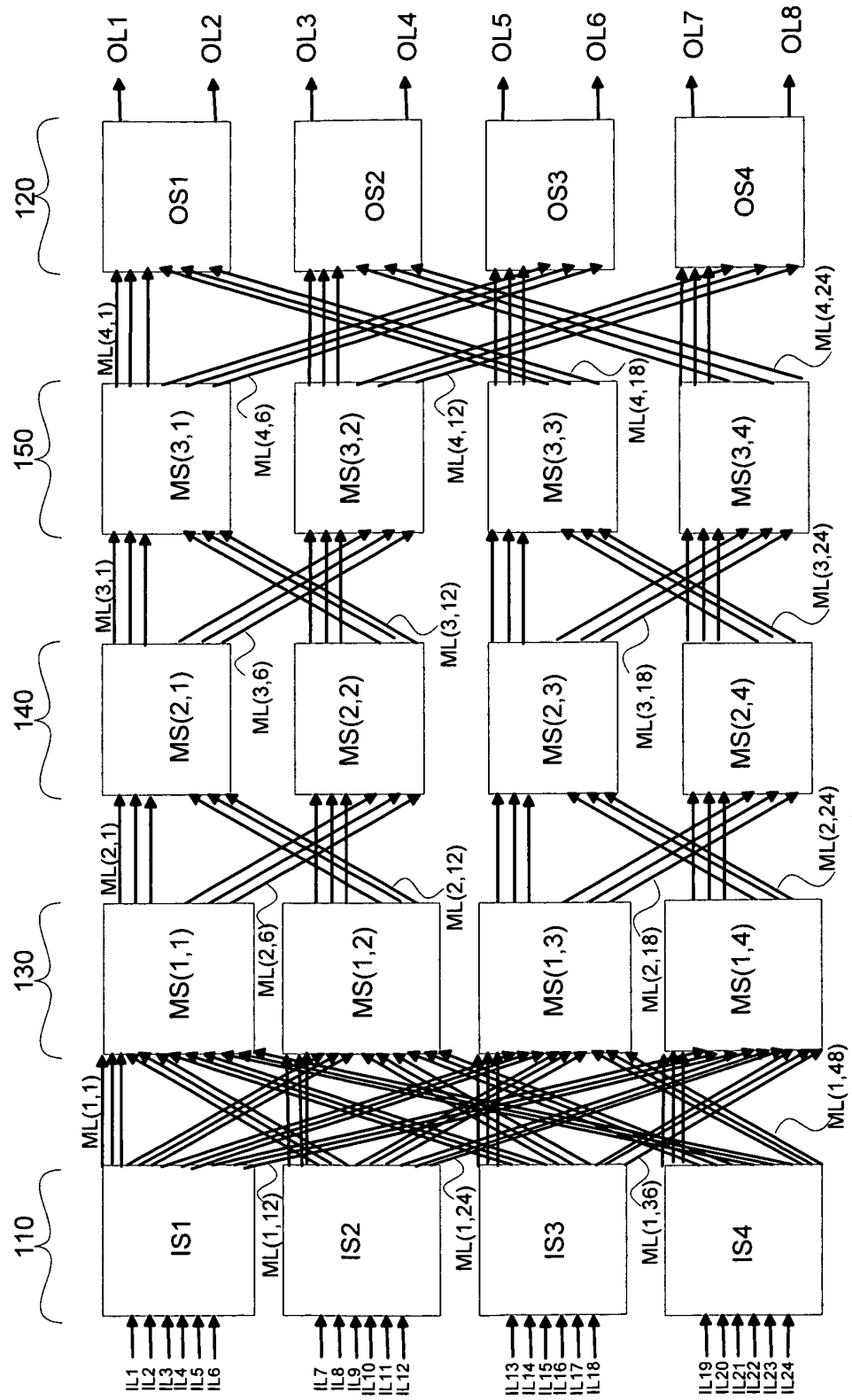


FIG. 3J2

300J2

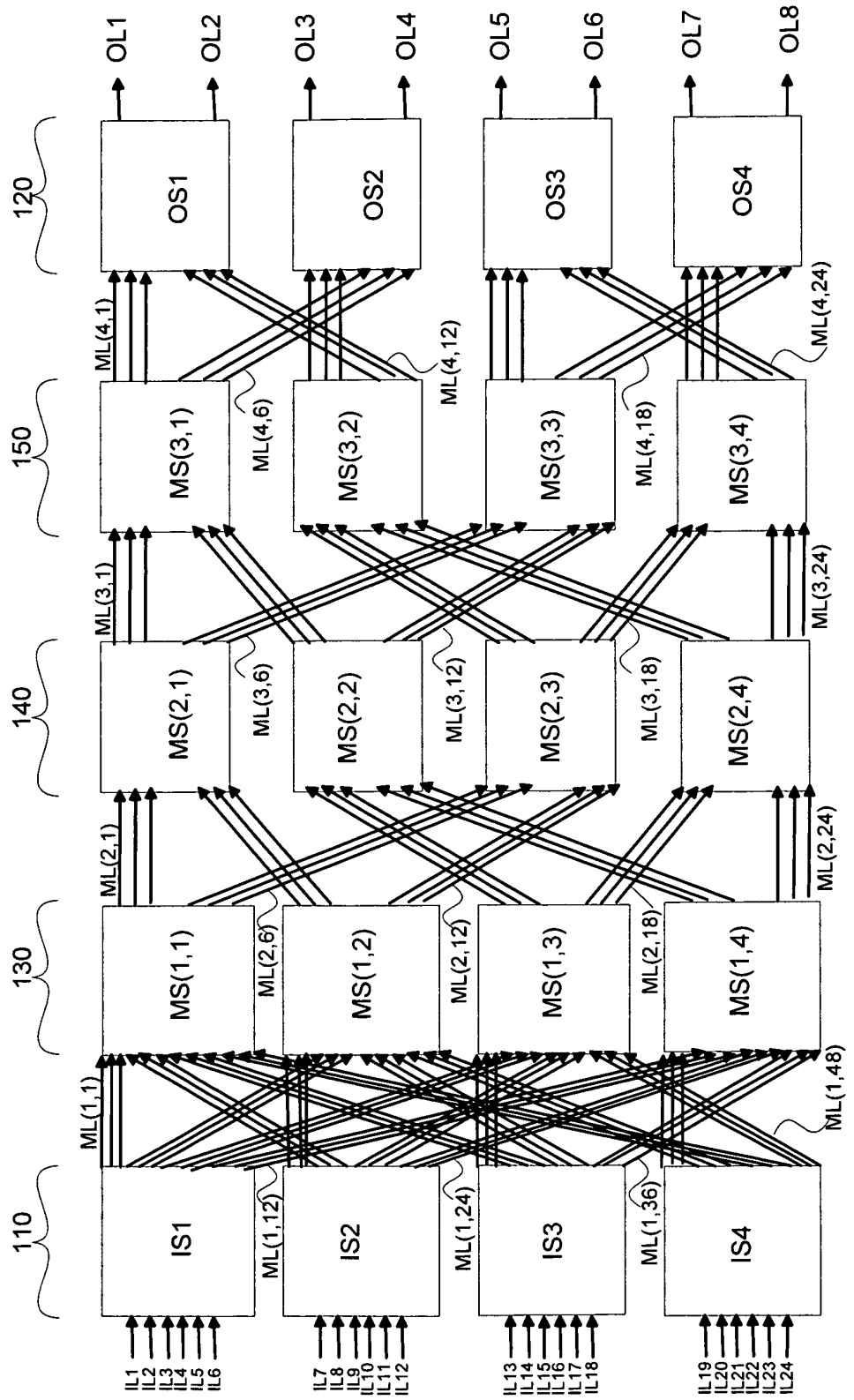


FIG. 3K2

300K2

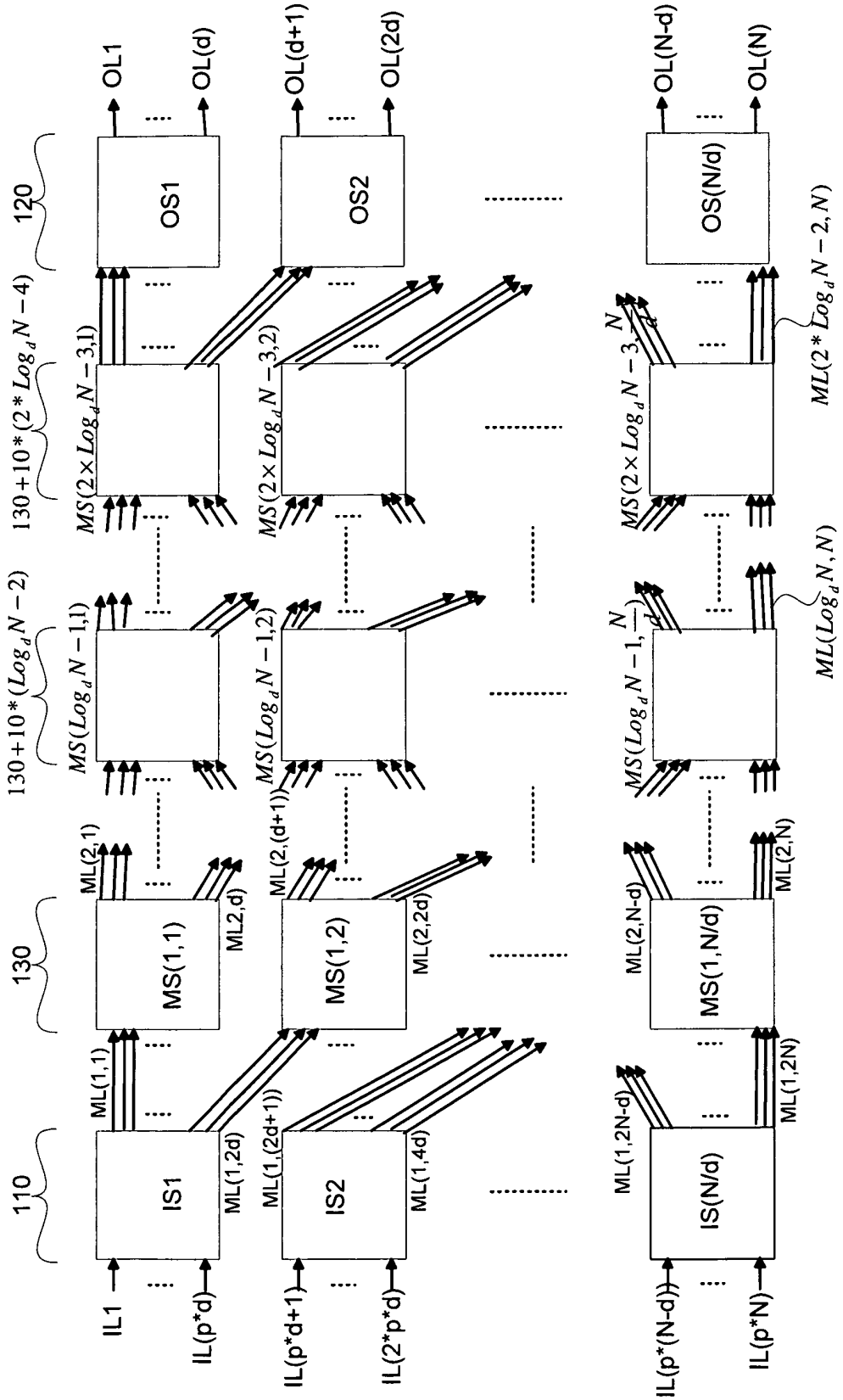


FIG. 4A

400A

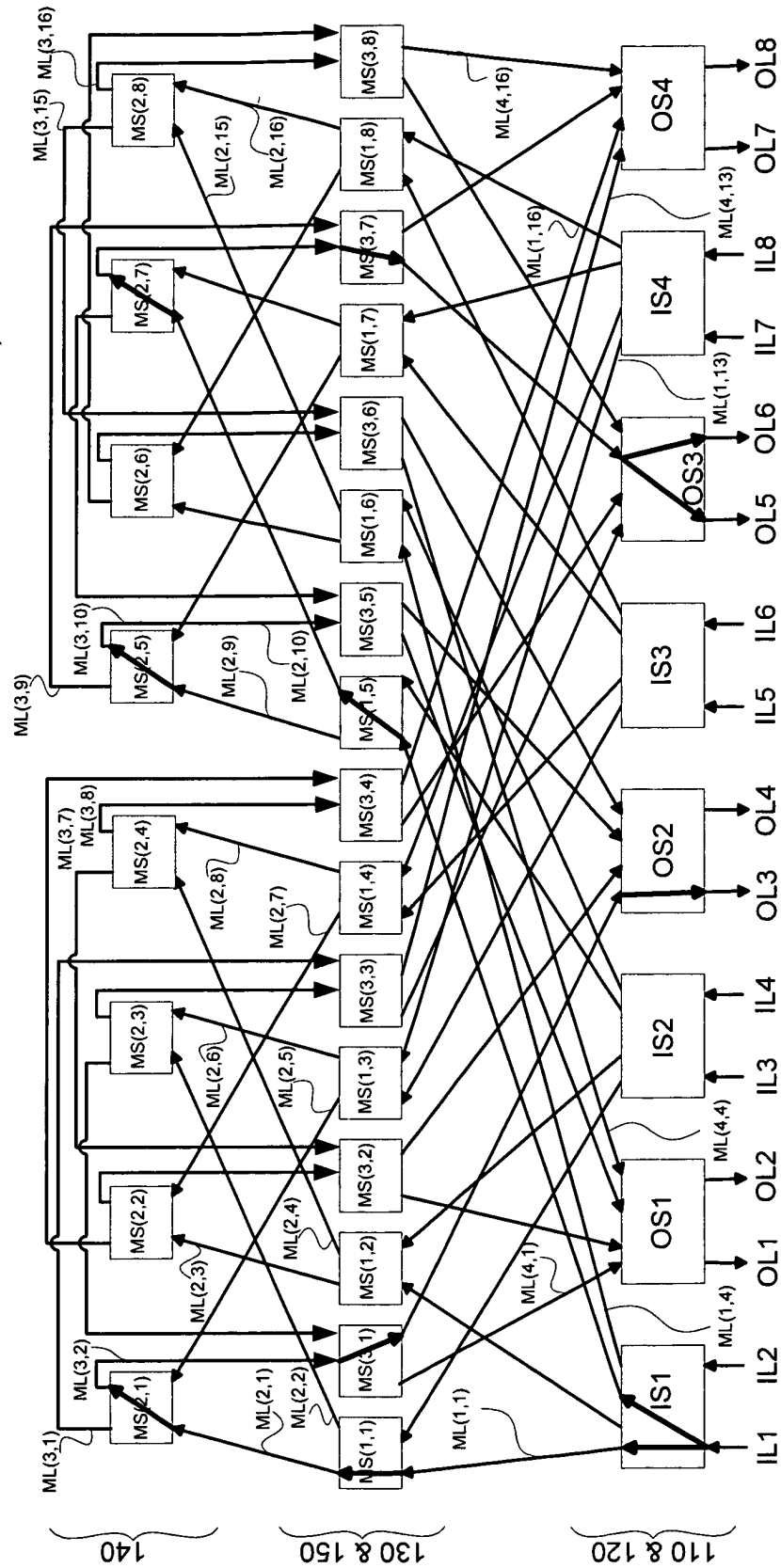


FIG. 4A1

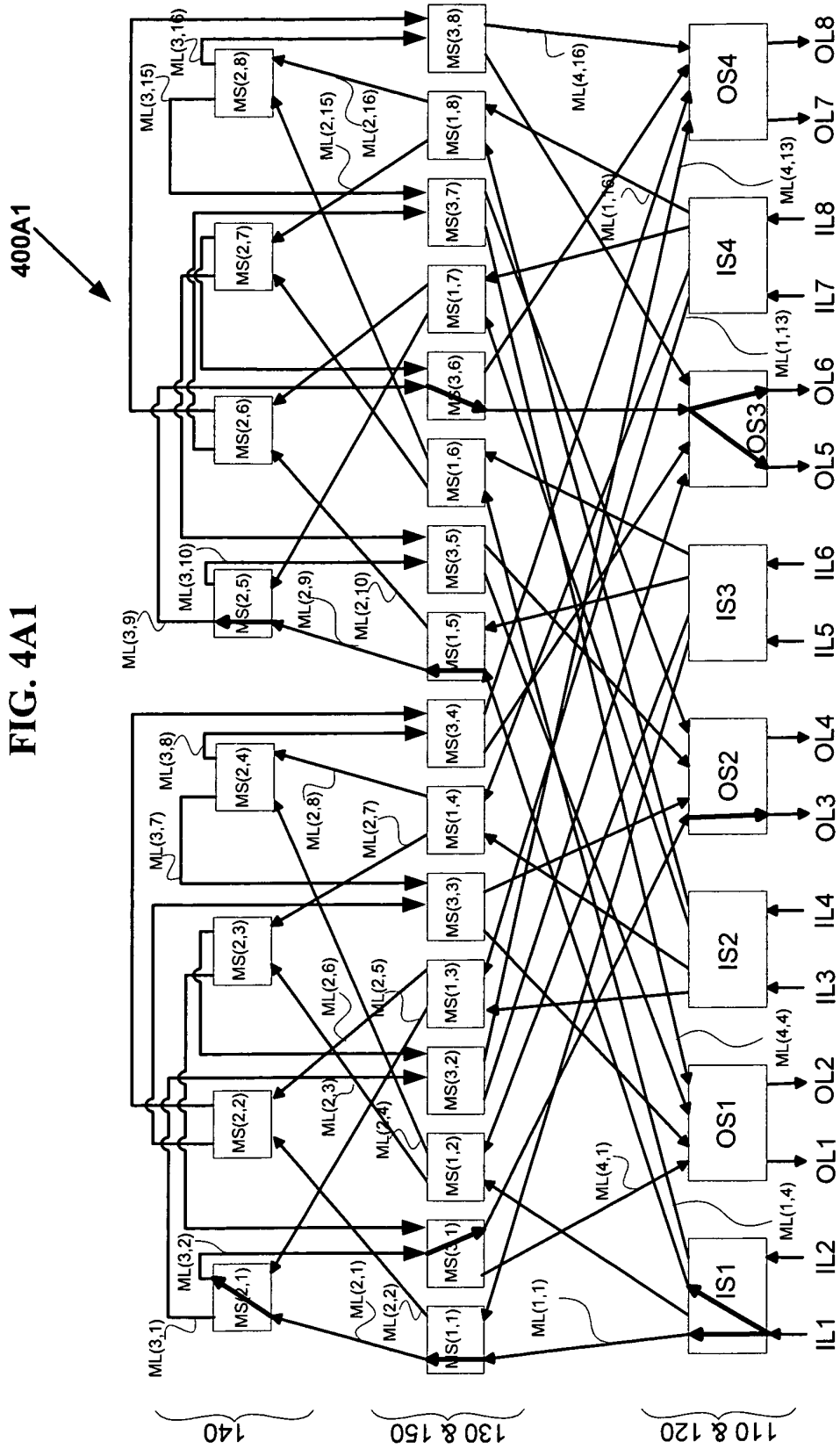


FIG. 4A2

400A2

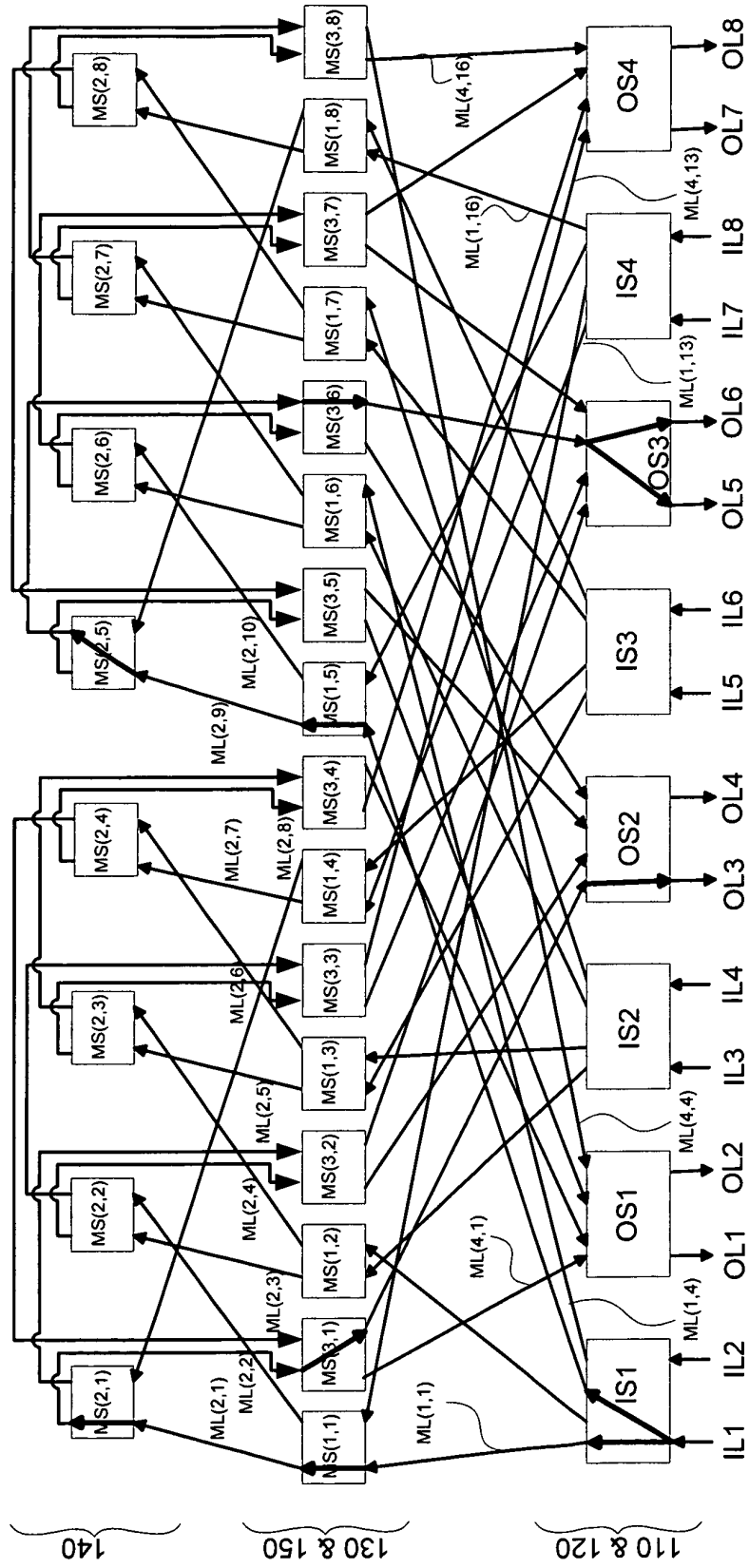
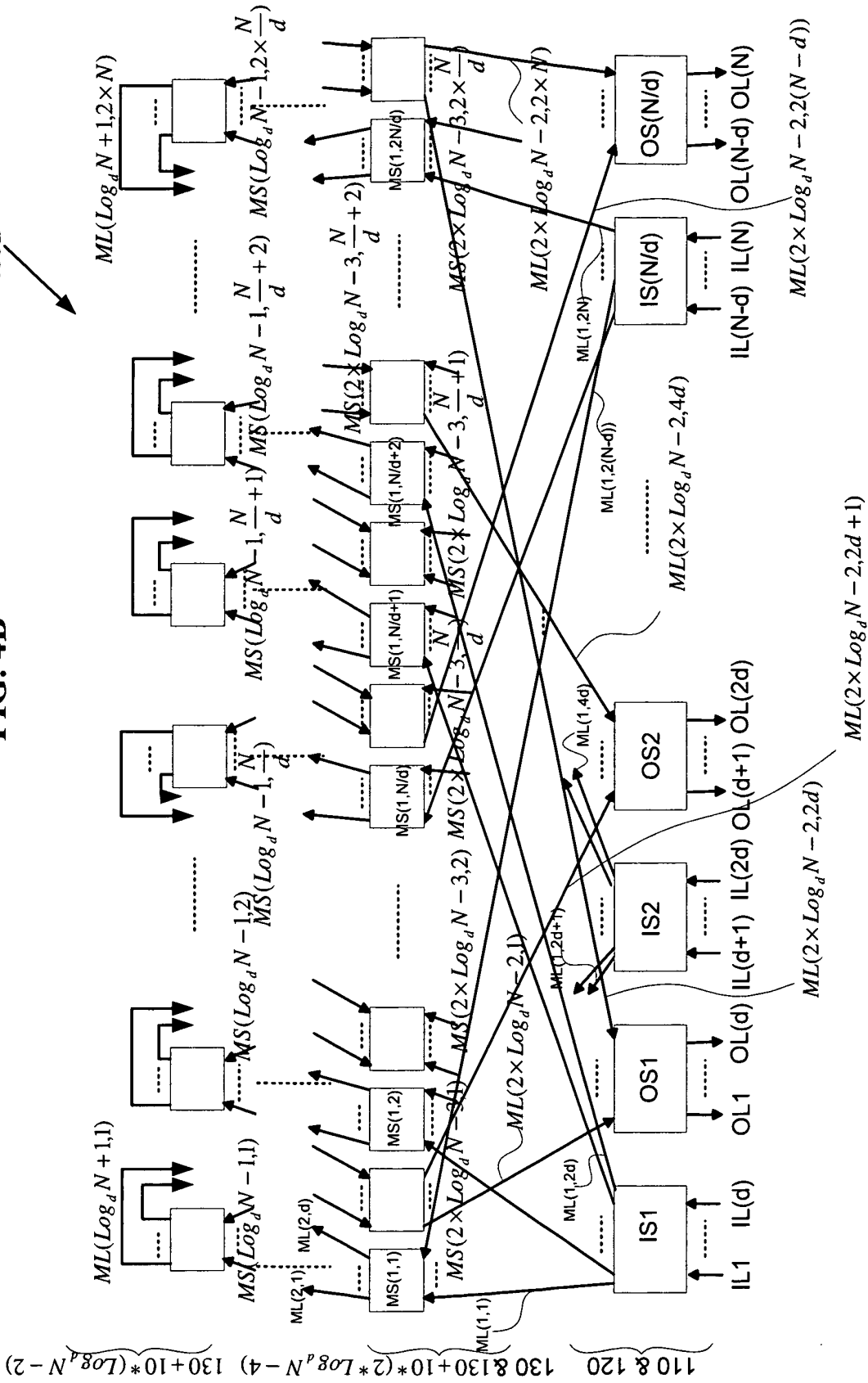


FIG. 4B

400B



110 & 120 130 & 130 + 10 * (2 * Log_d N - 4) 130 + 10 * (Log_d N - 2)

FIG. 4C

400C

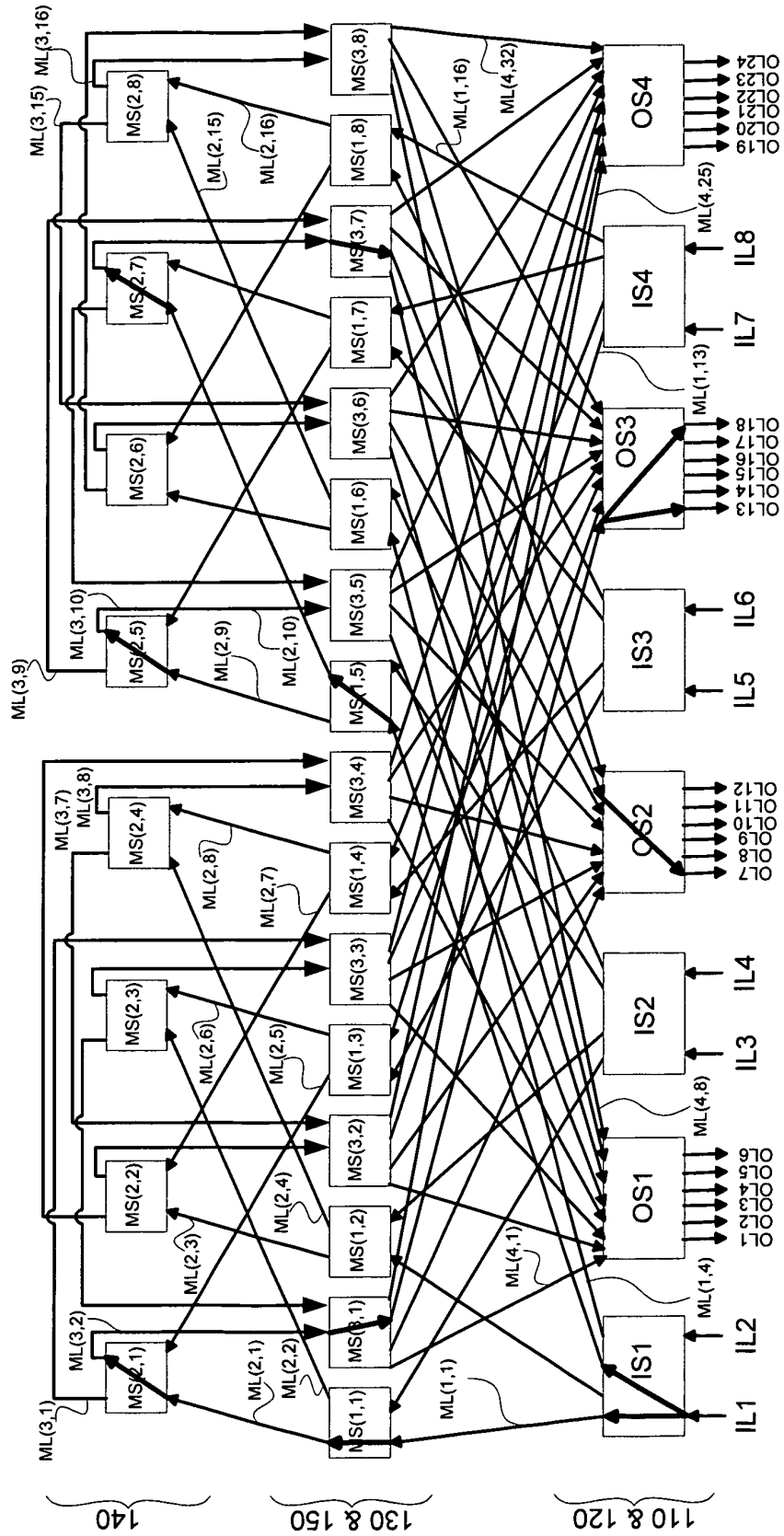


FIG. 4C1

400C1

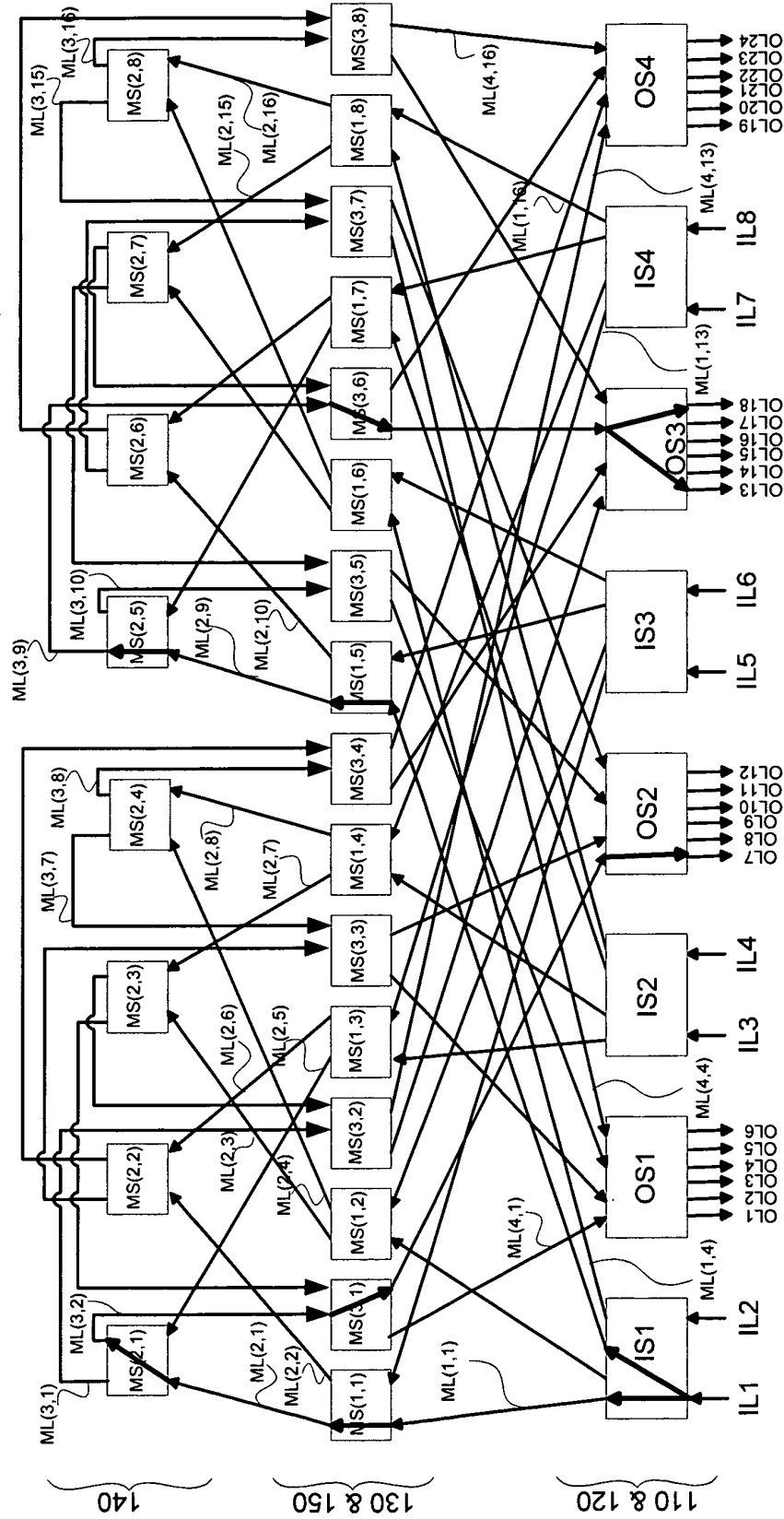


FIG. 4C2

400C2

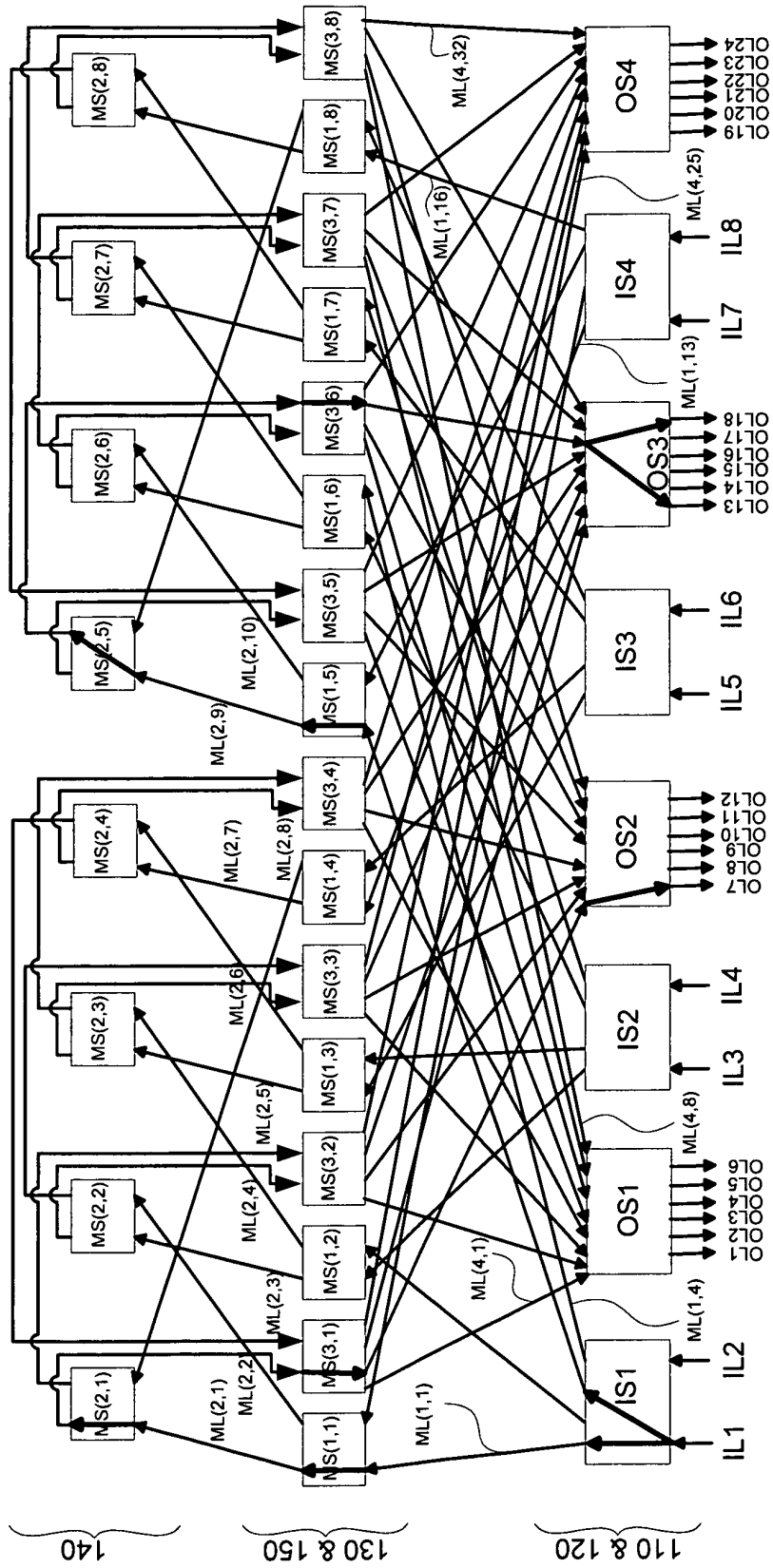


FIG. 4E

400E

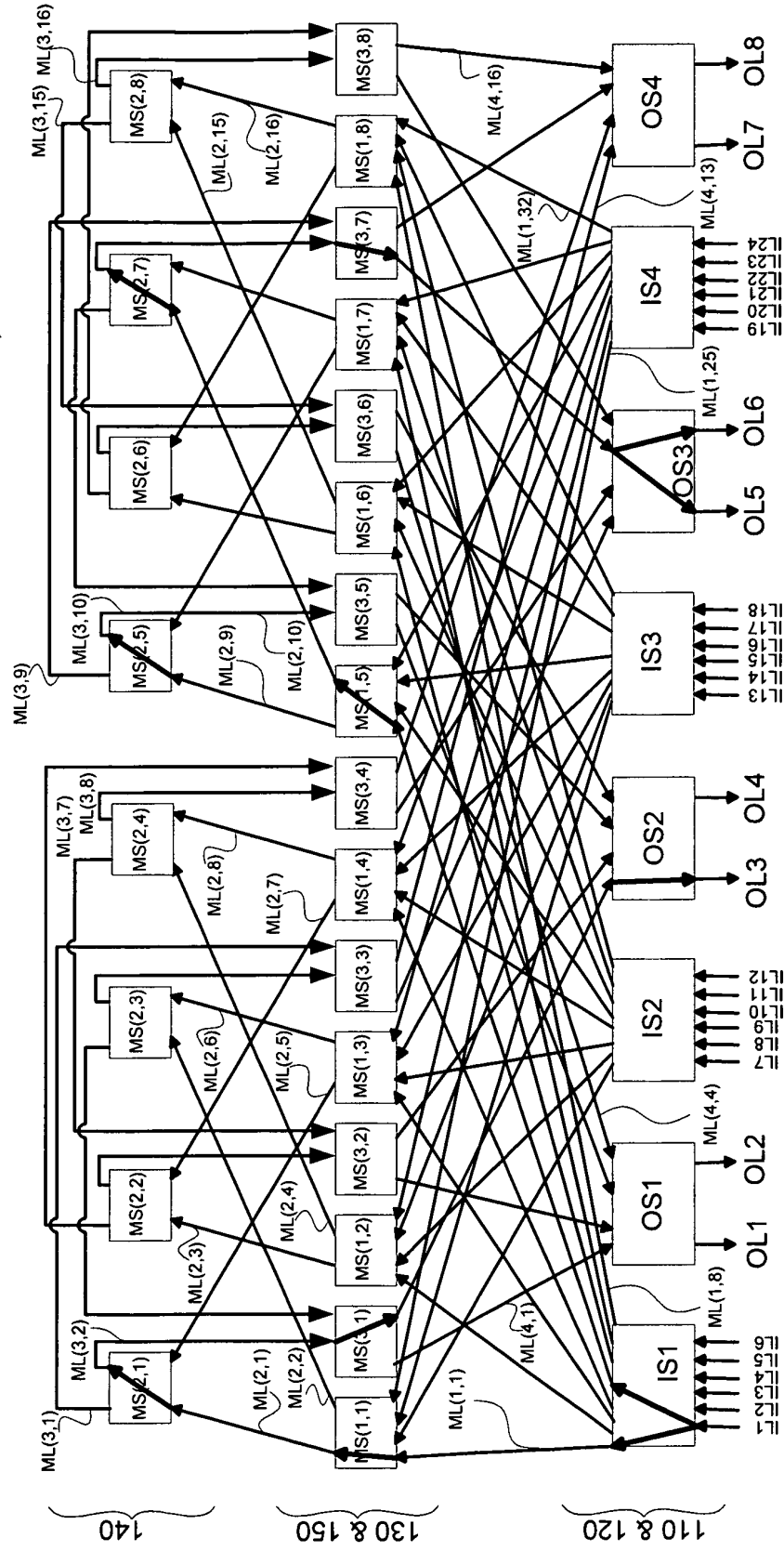


FIG. 4E1
 400E1

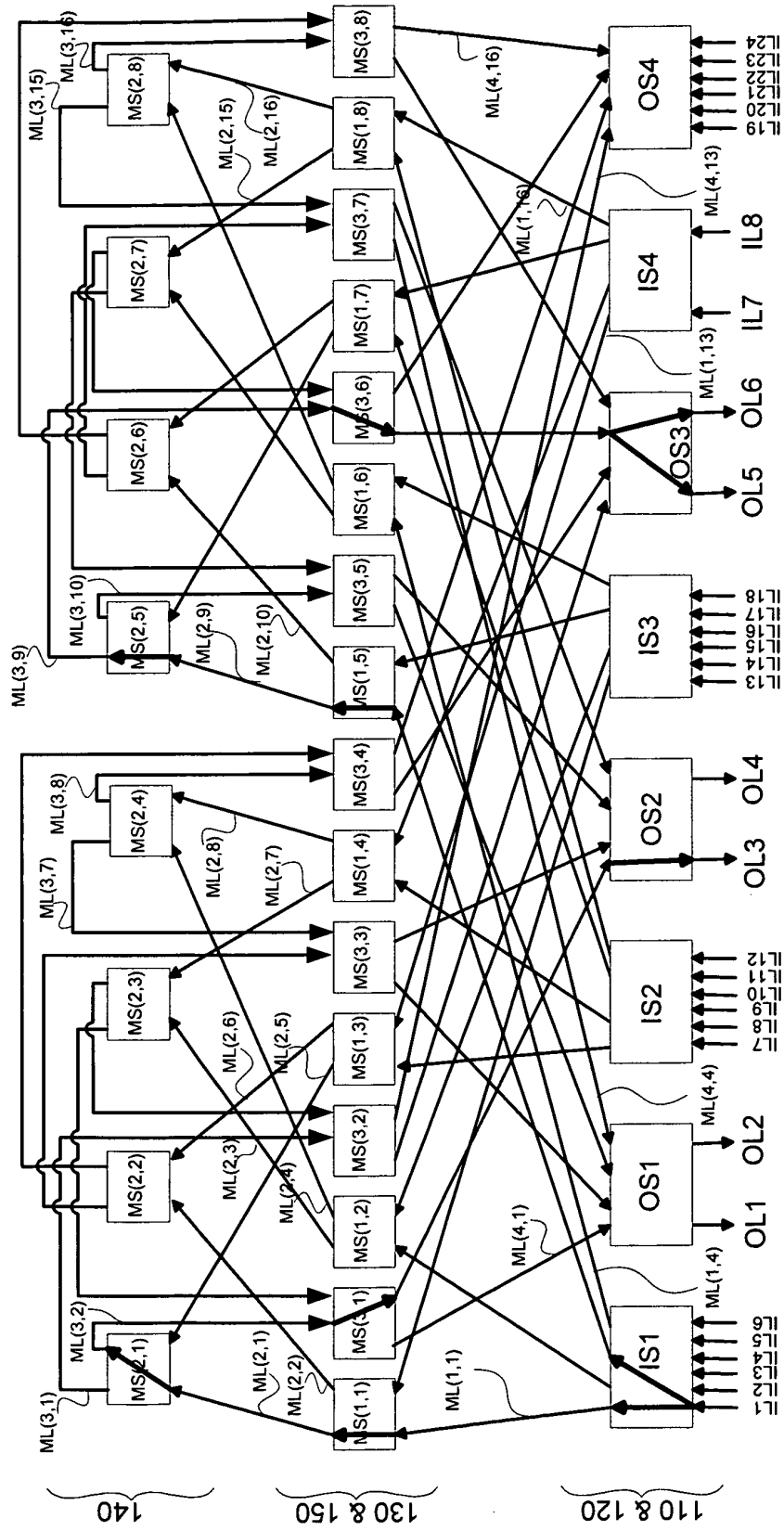


FIG. 4E2

400E2

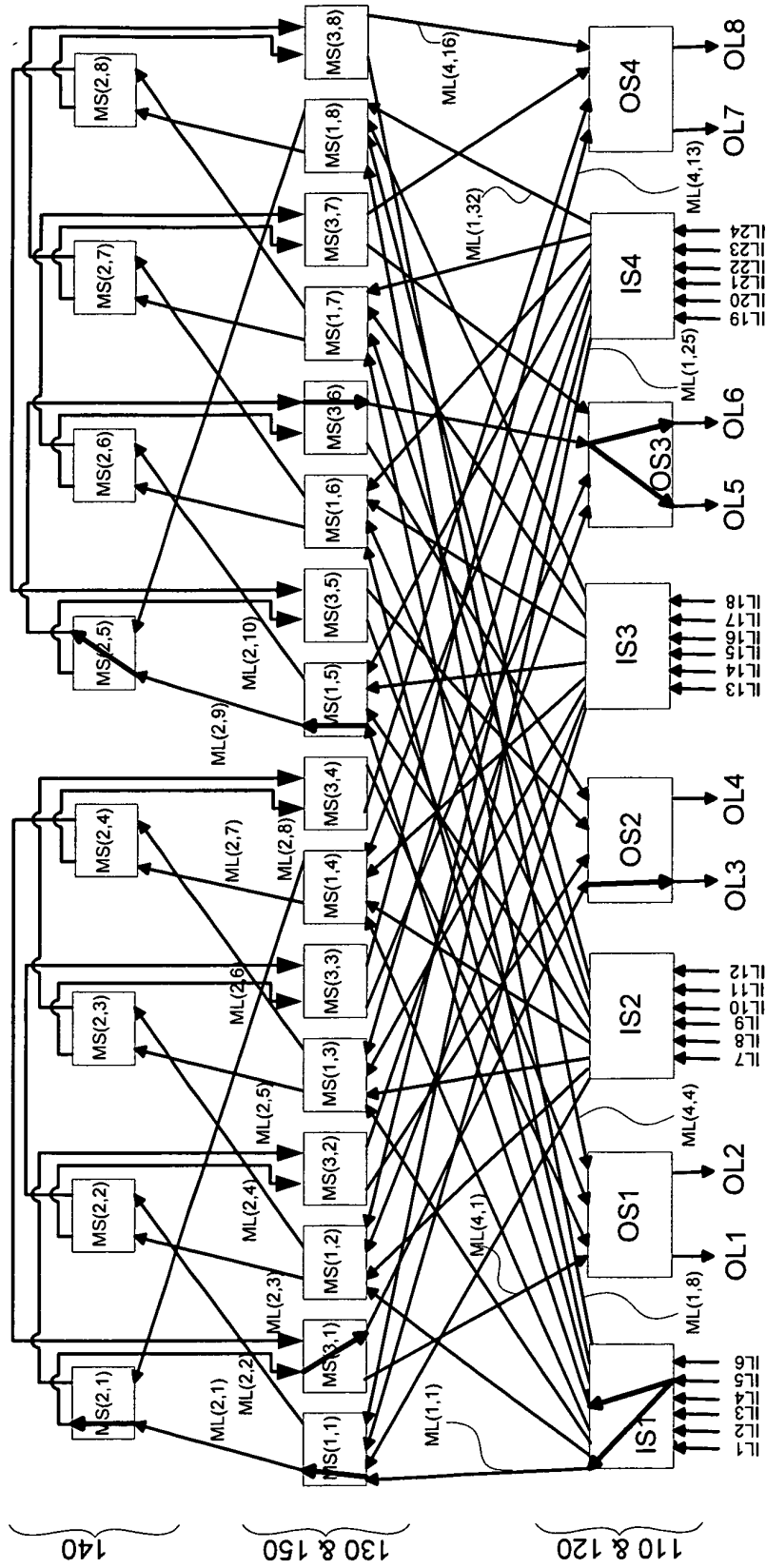


FIG. 4F

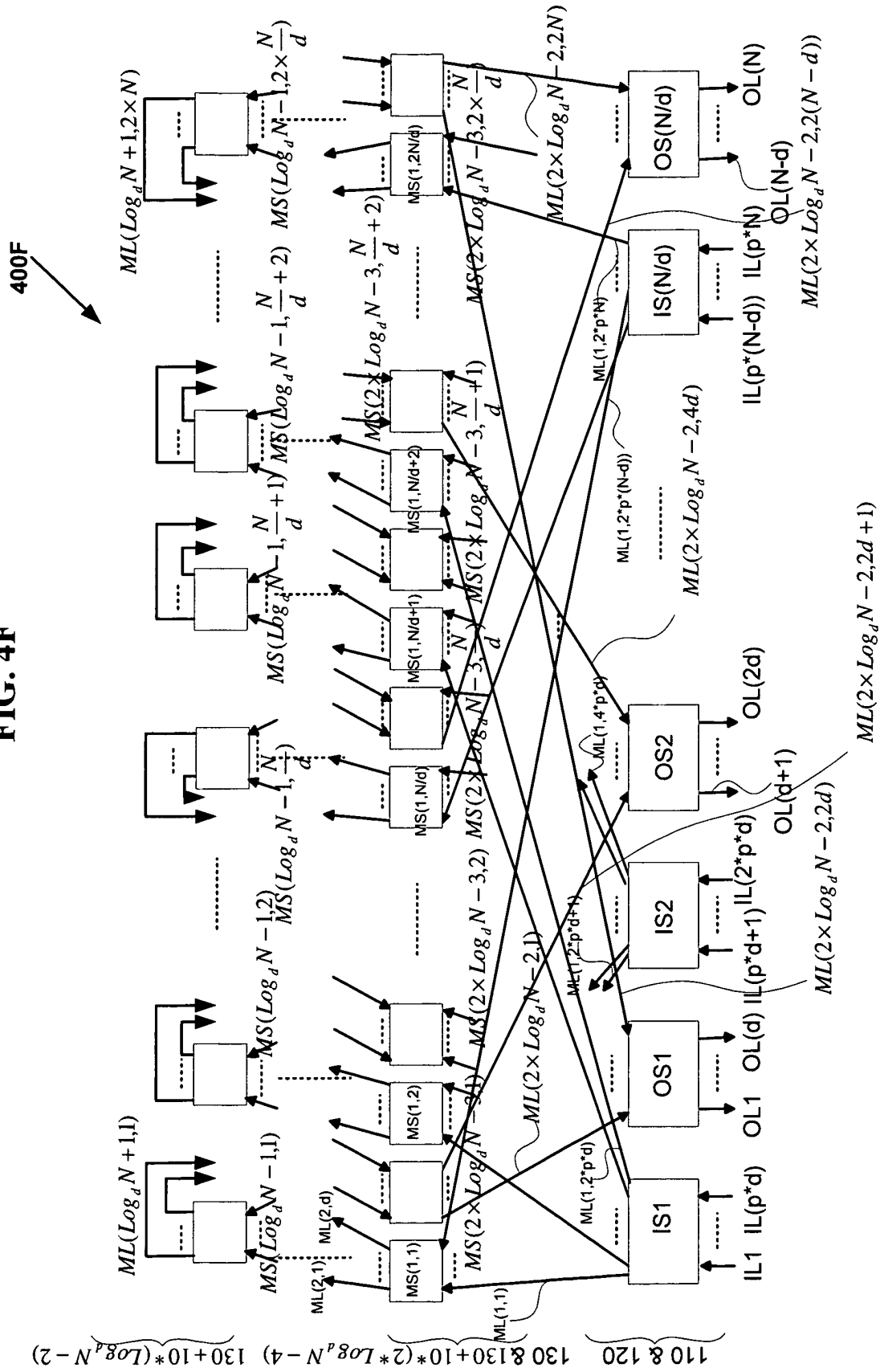


FIG. 5A

500A

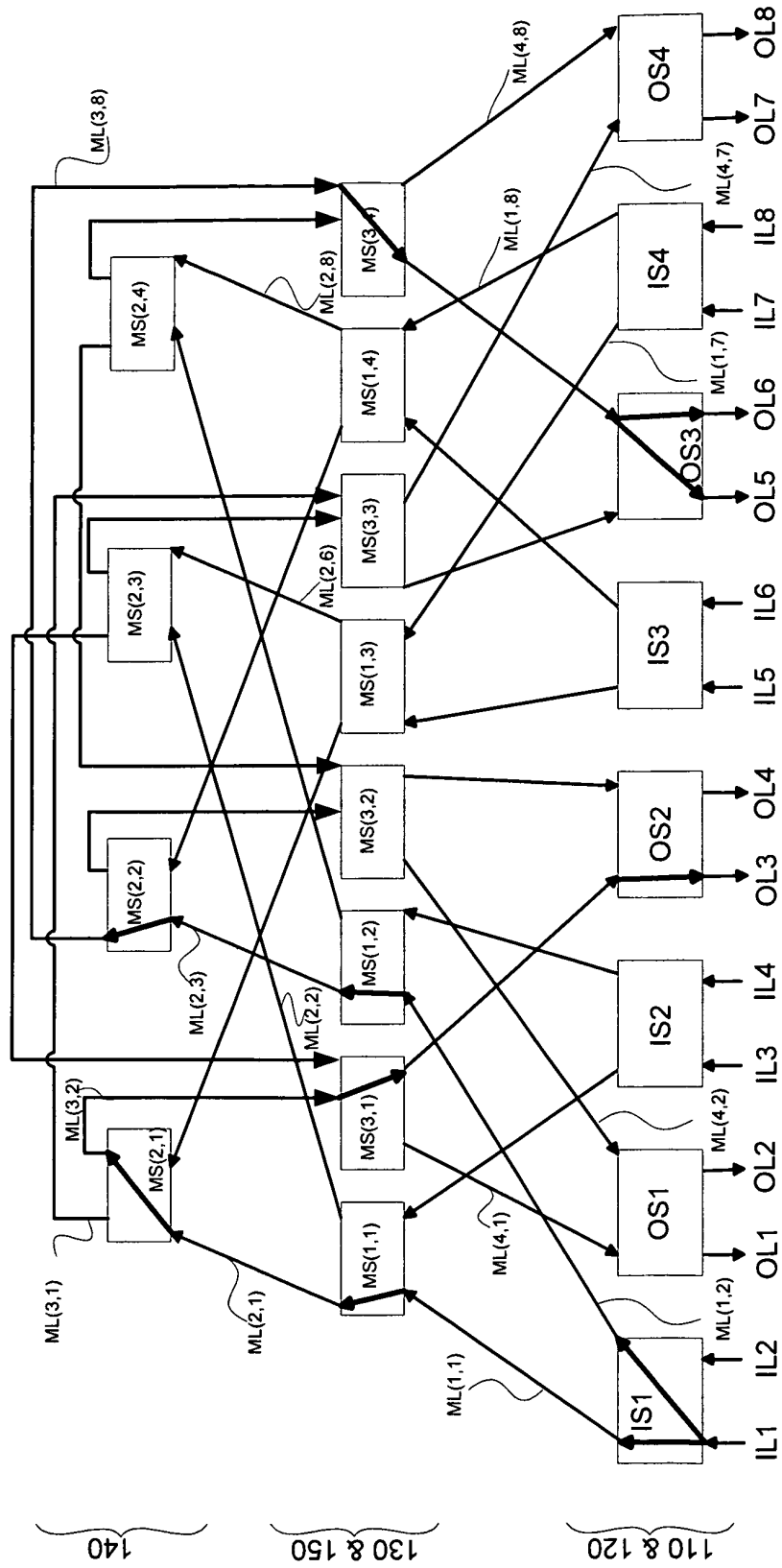


FIG. 5B

500B

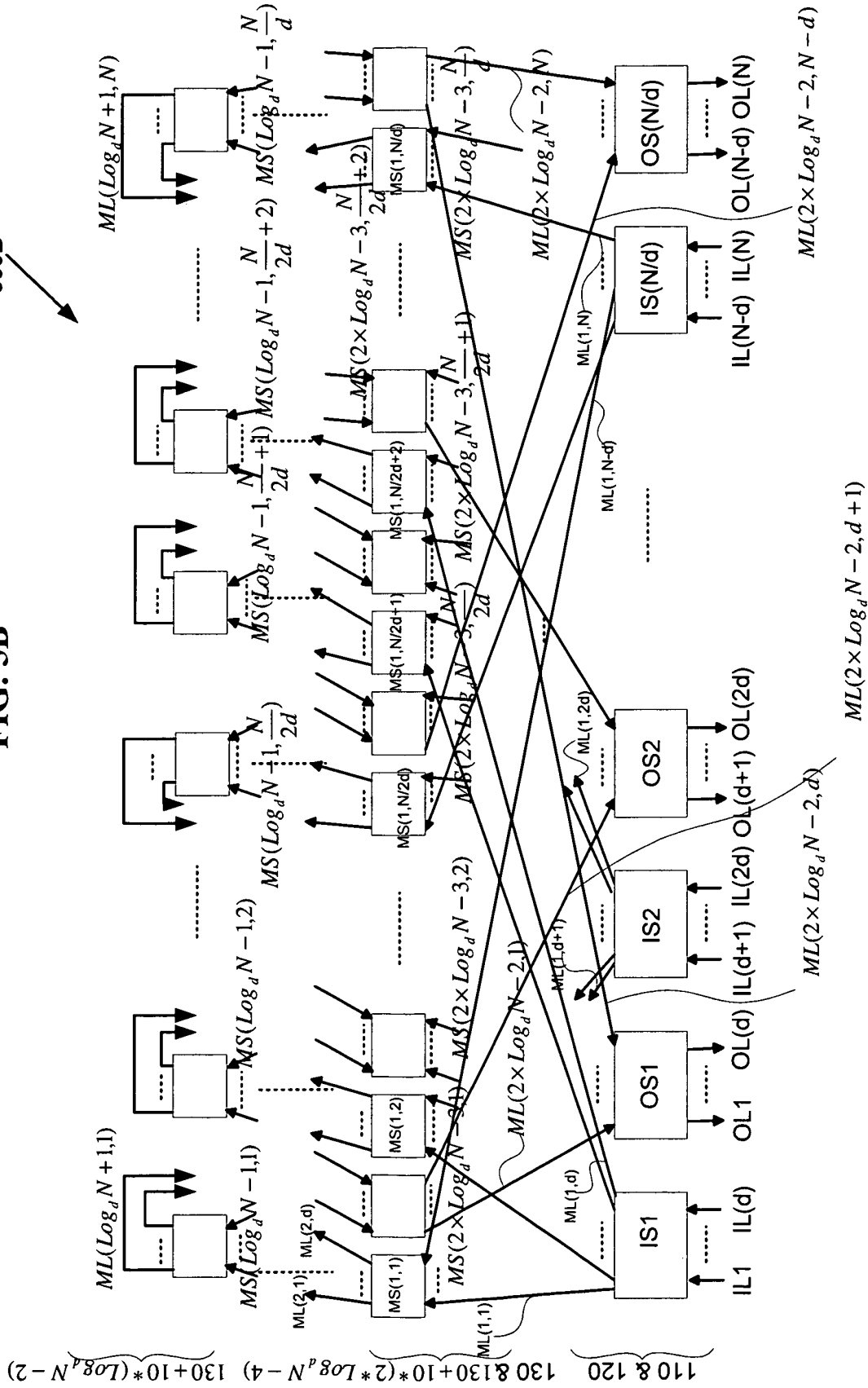


FIG. 5C

500C

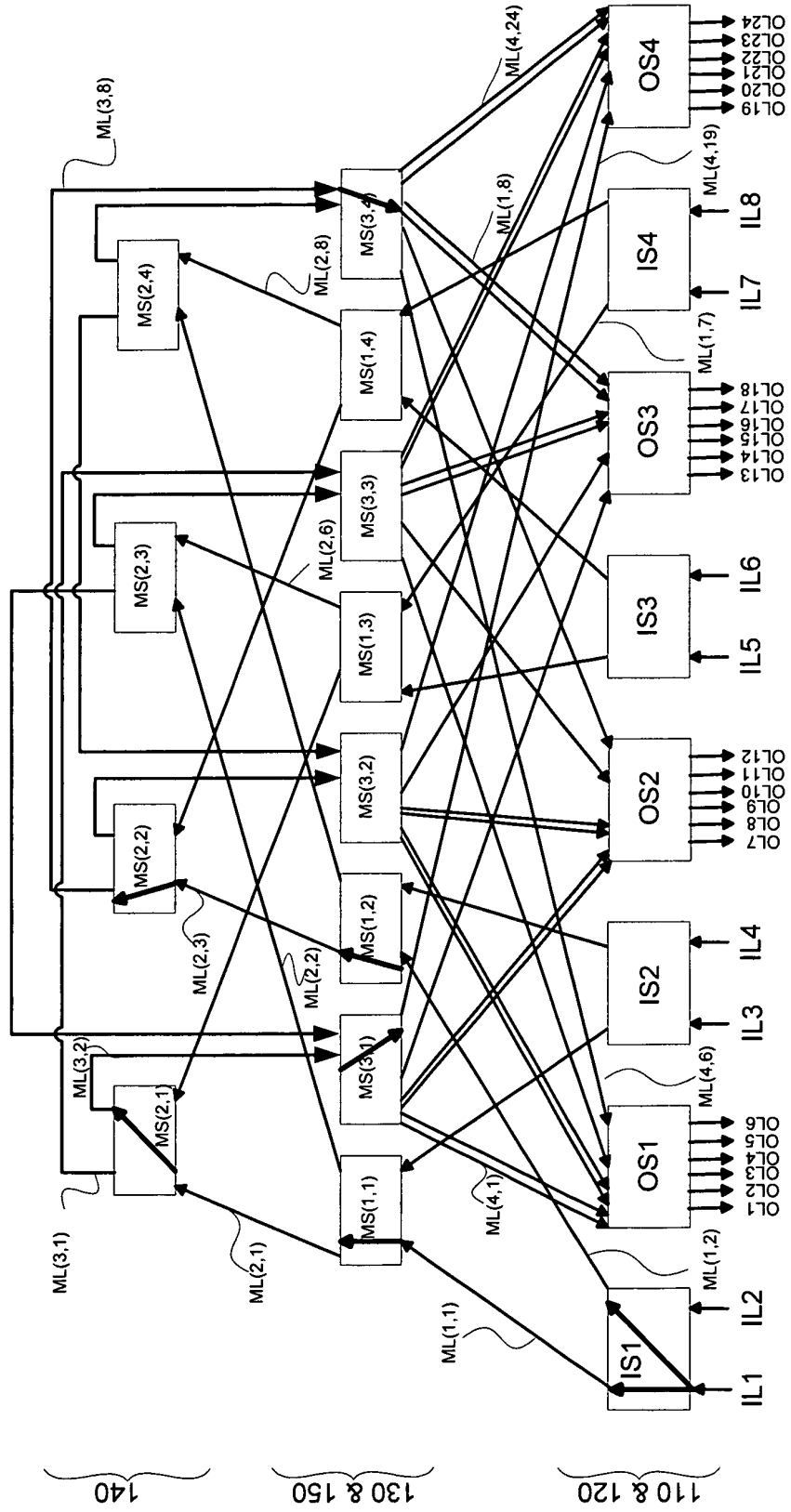


FIG. 5E

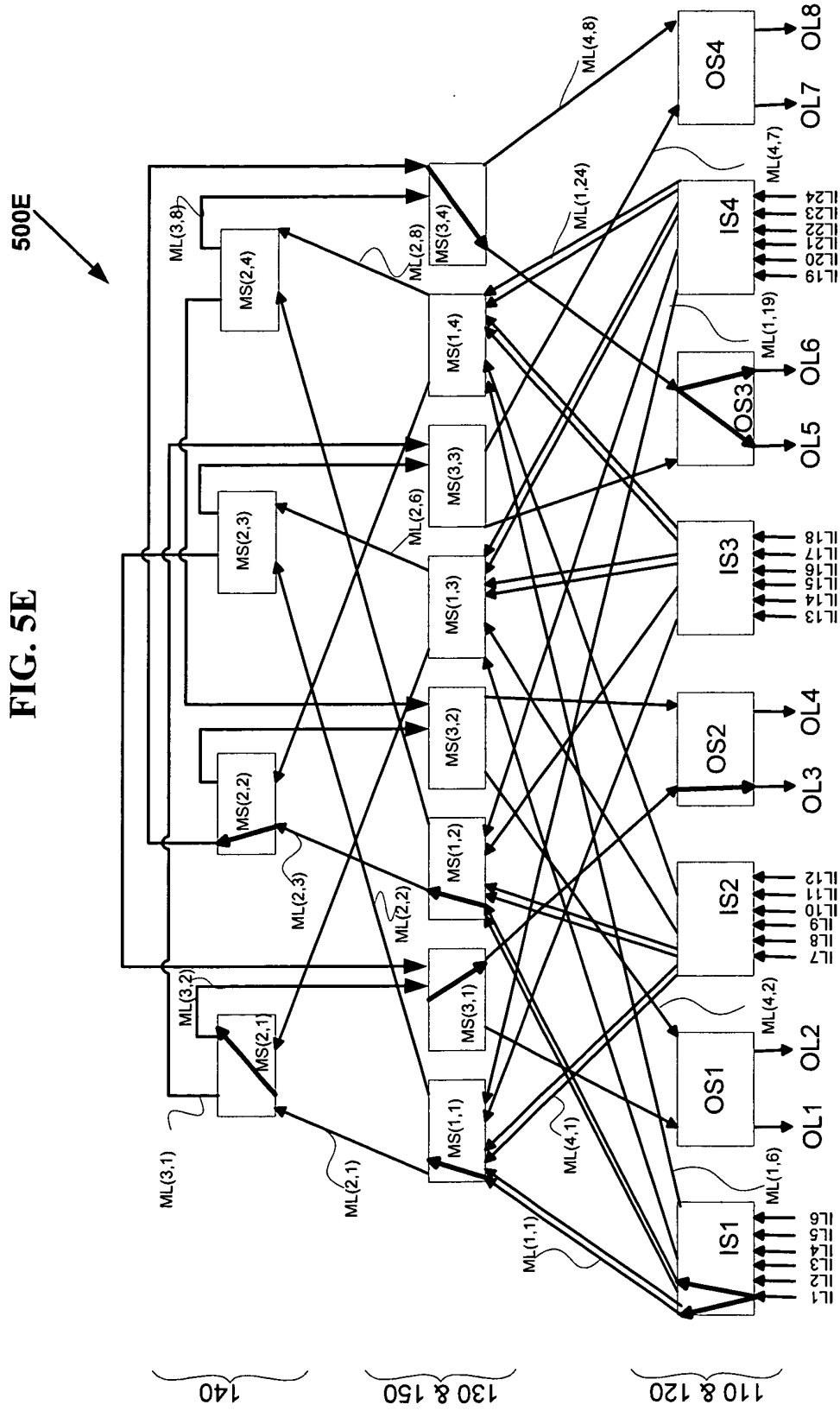


FIG. 5F

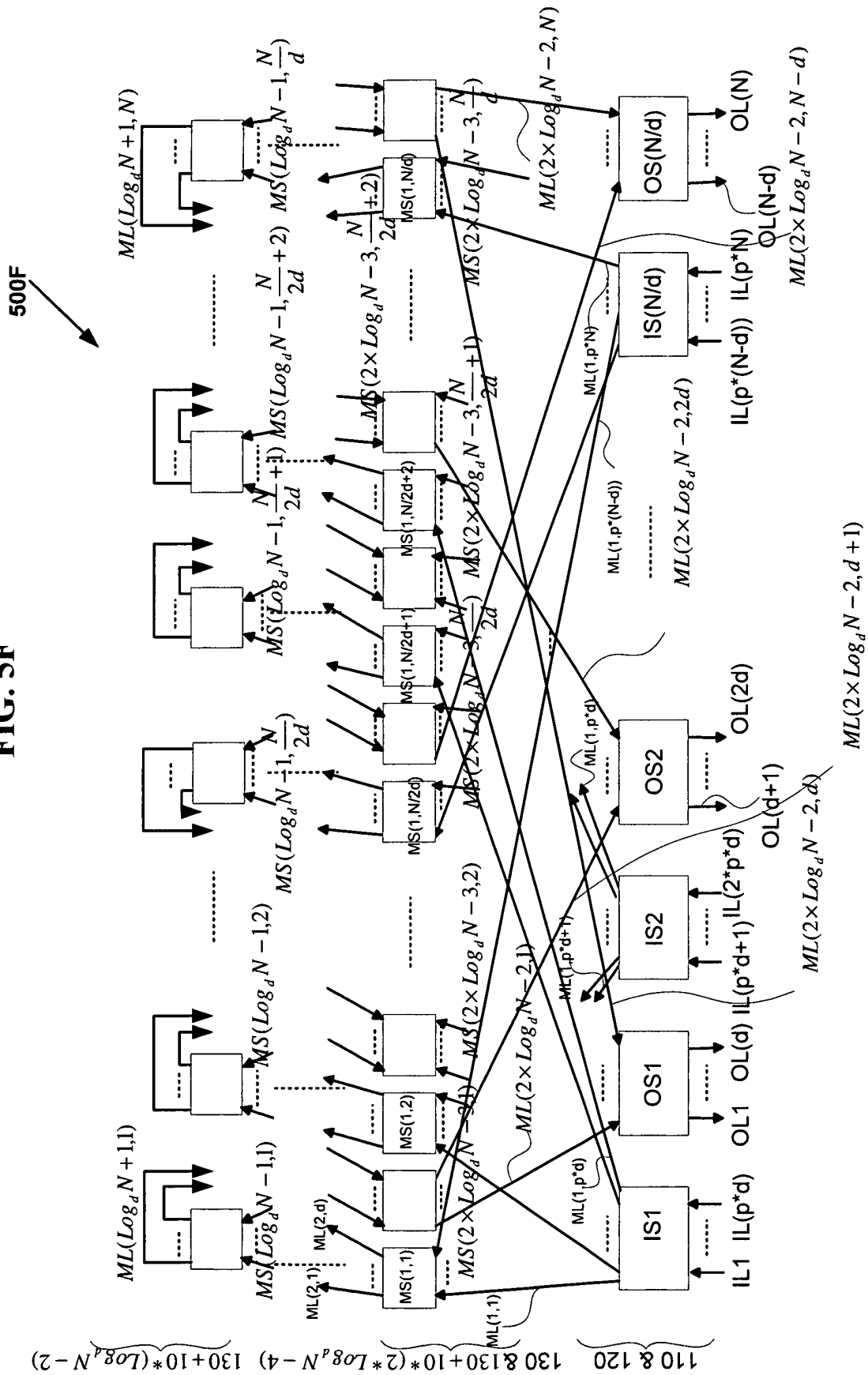


FIG. 6A

600A

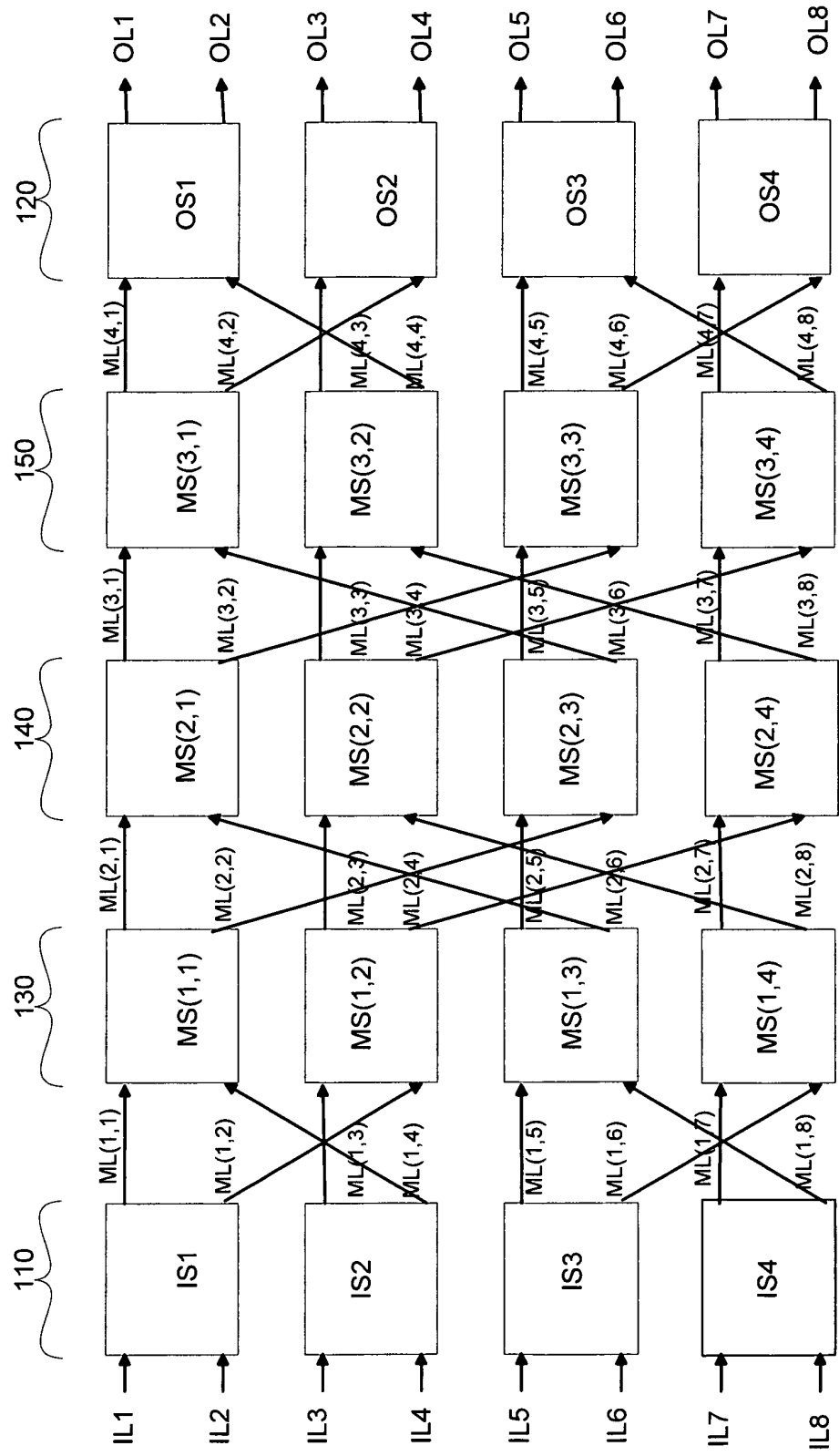


FIG. 6B

600B

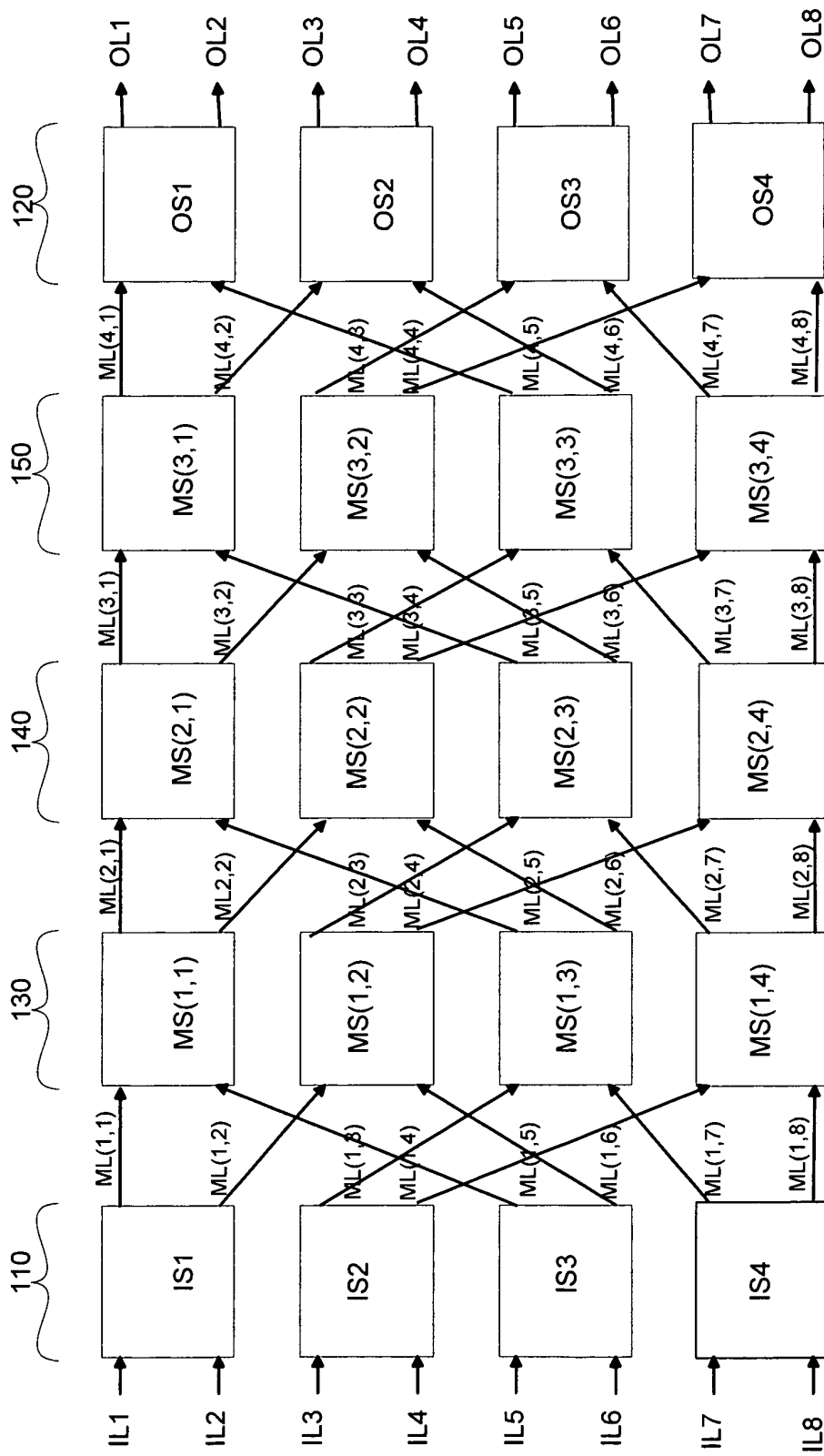


FIG. 6C

600C

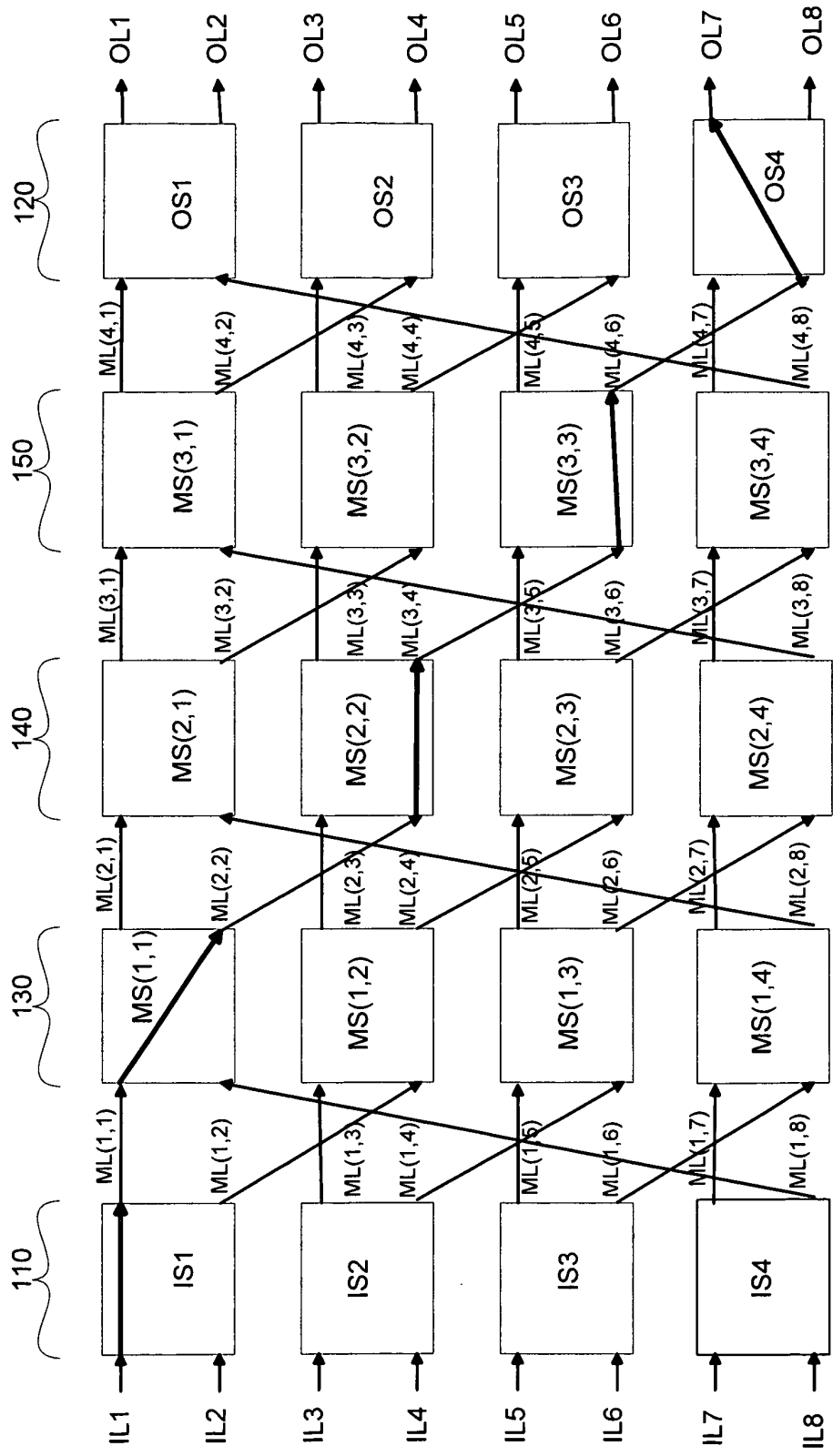


FIG. 6D

600D

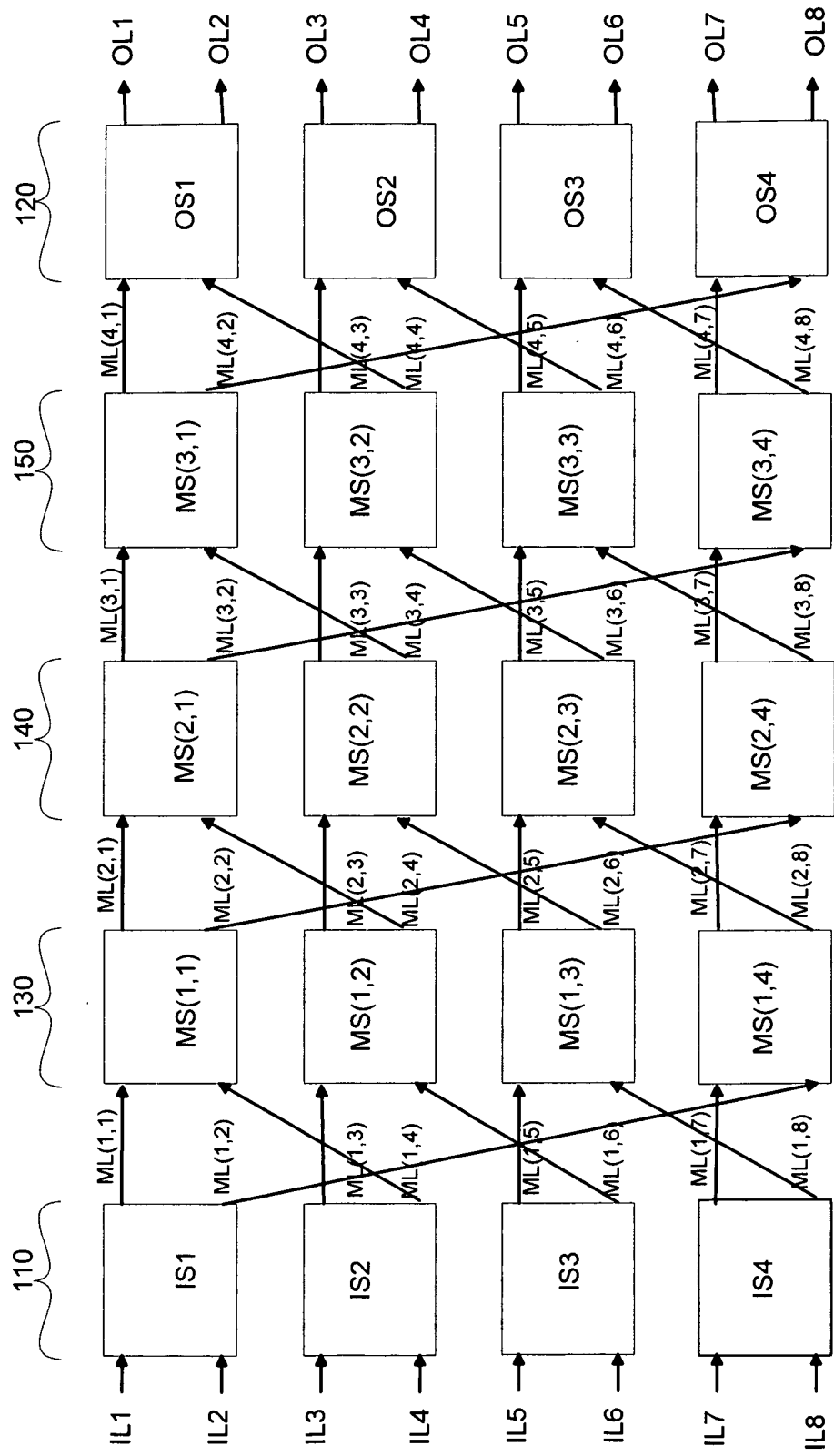


FIG. 6E

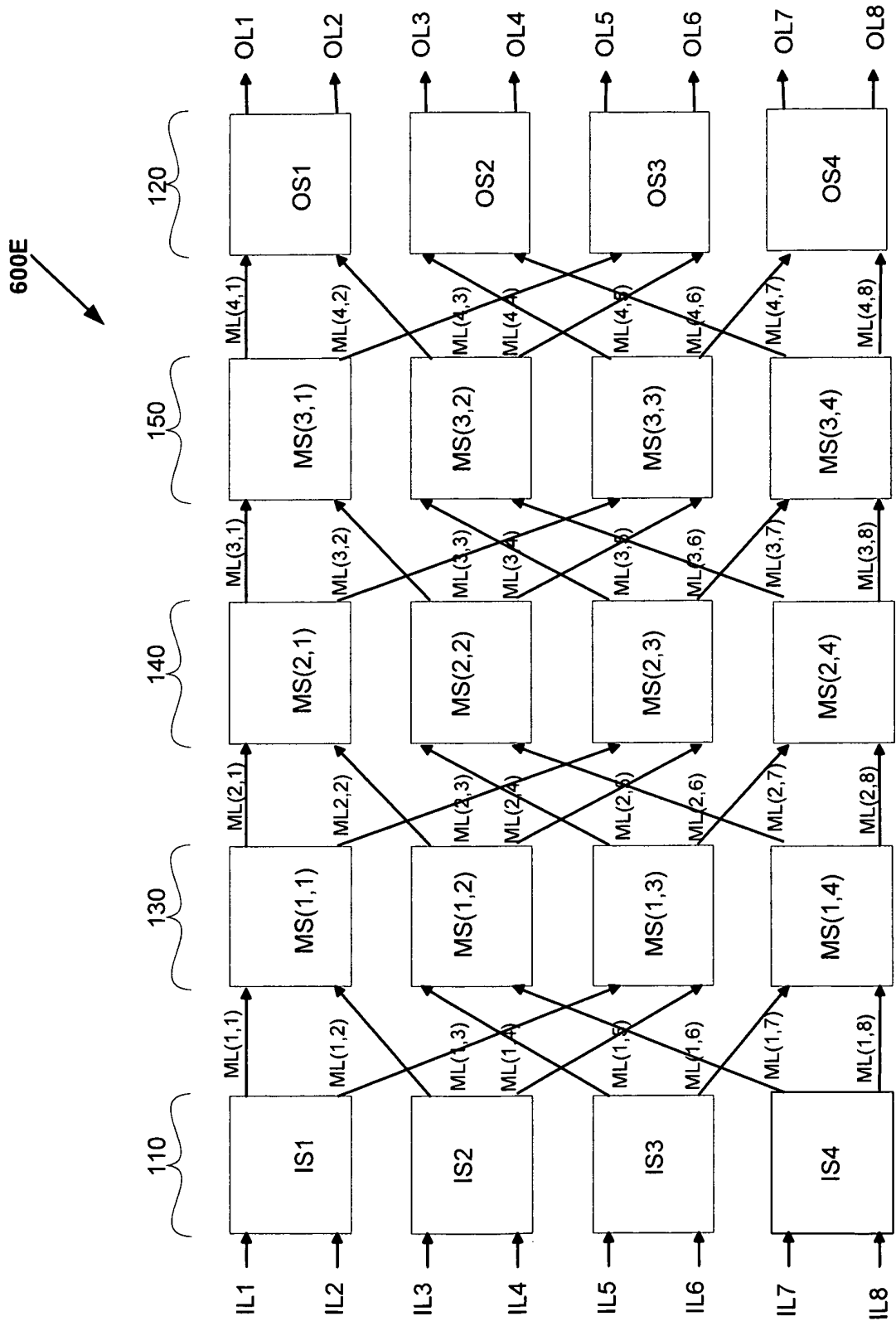


FIG. 6F

600F

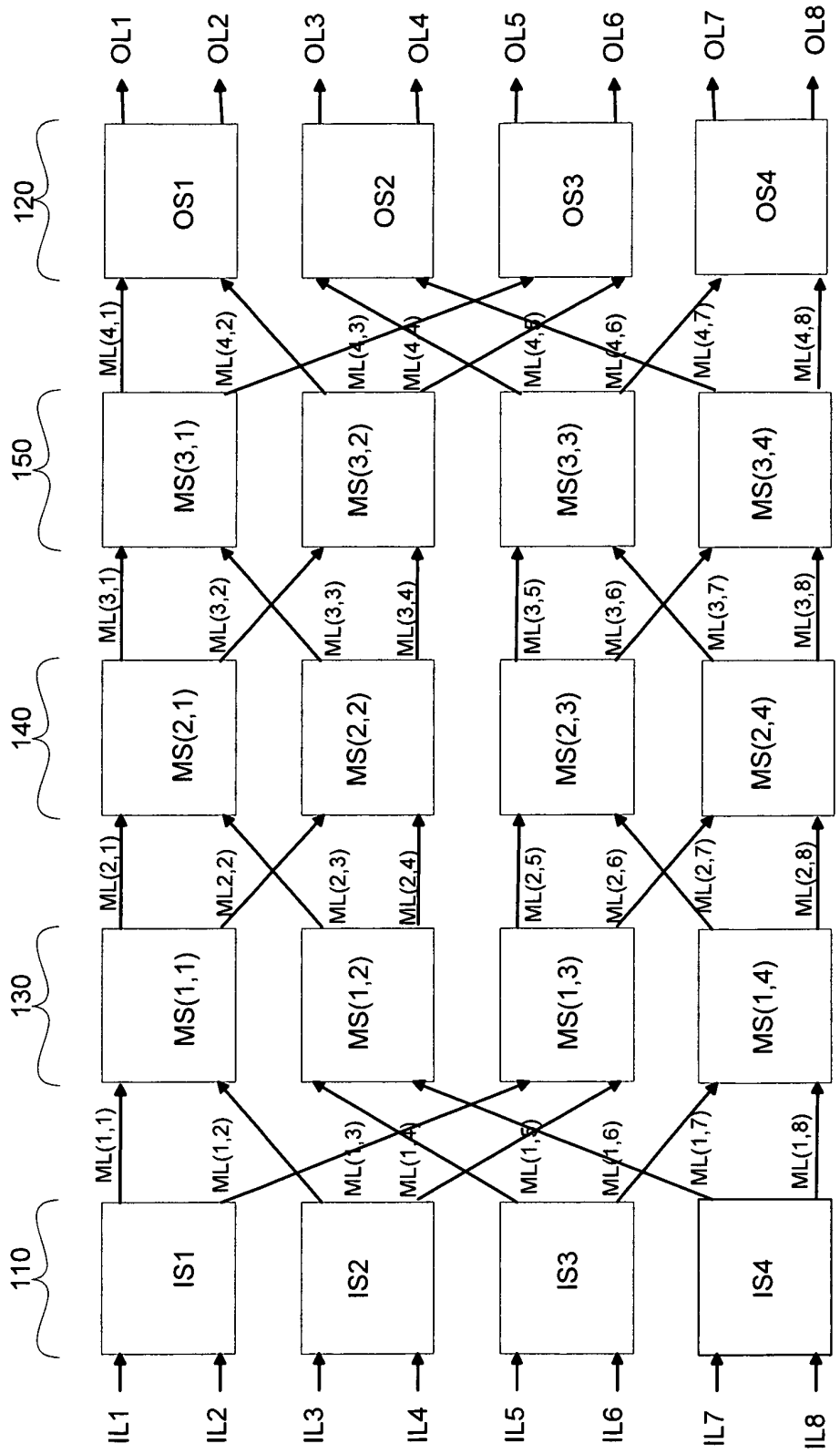


FIG. 6G

600G

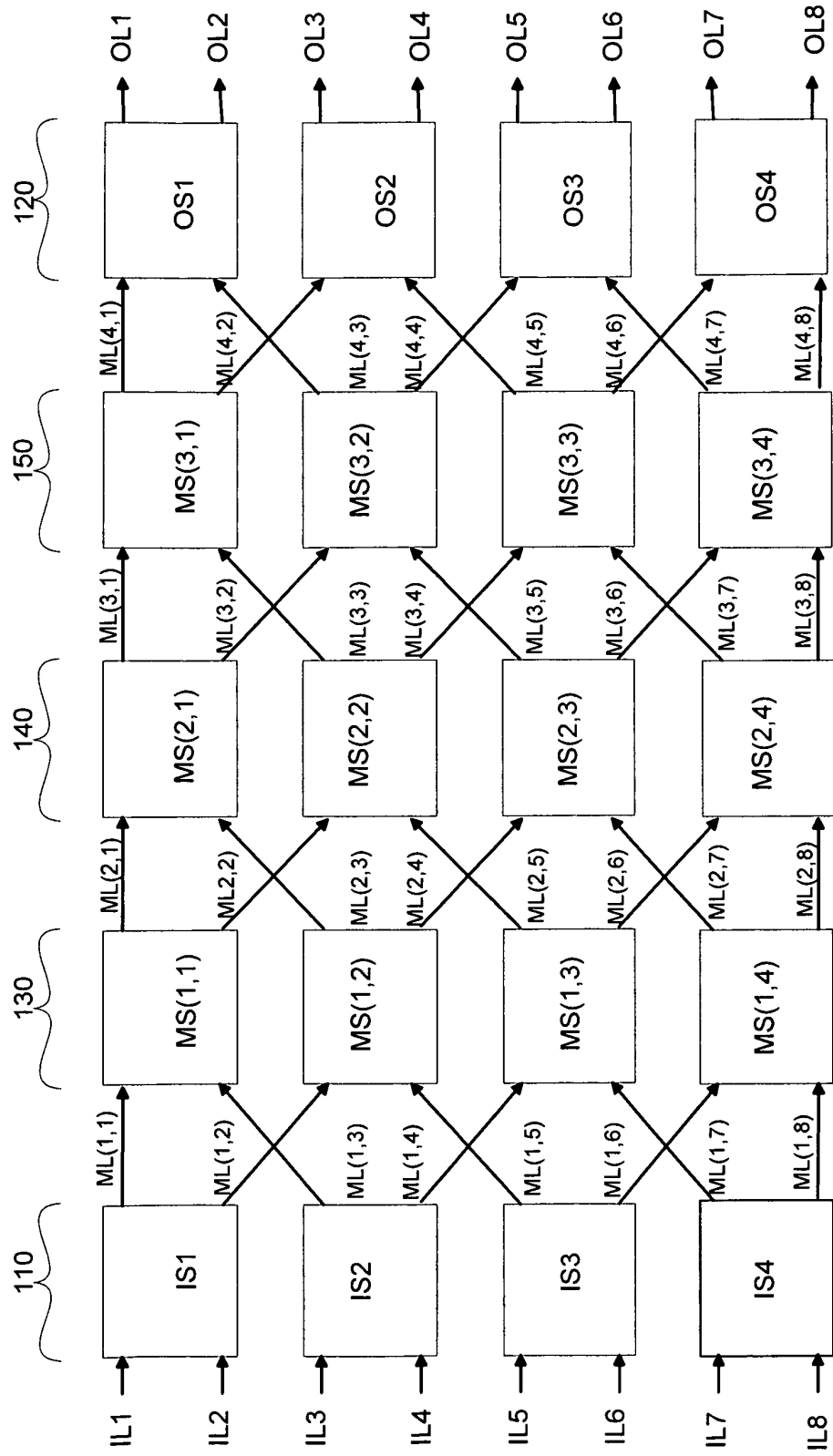


FIG. 6H

600H

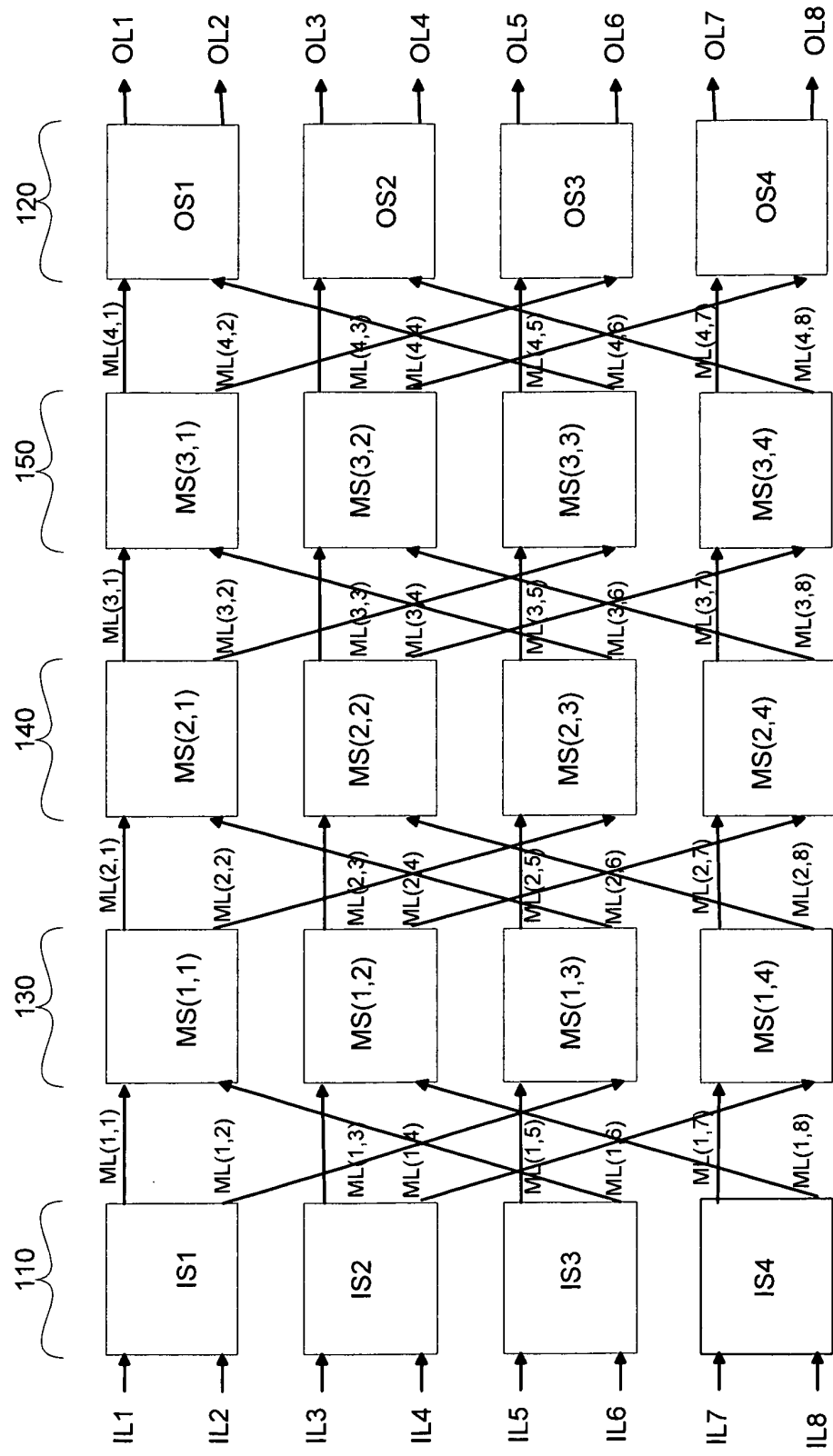


FIG. 6I

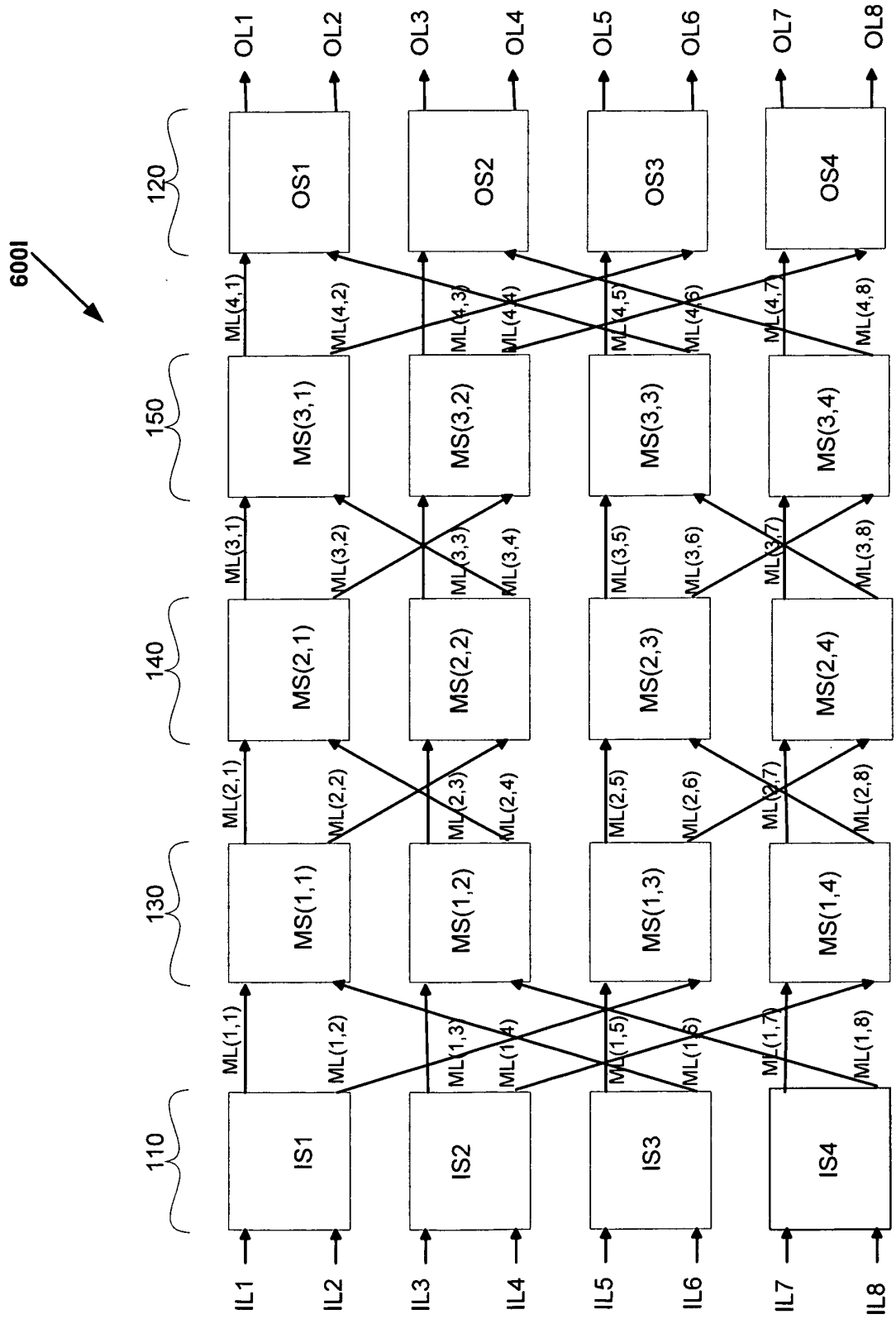


FIG. 6J

600J

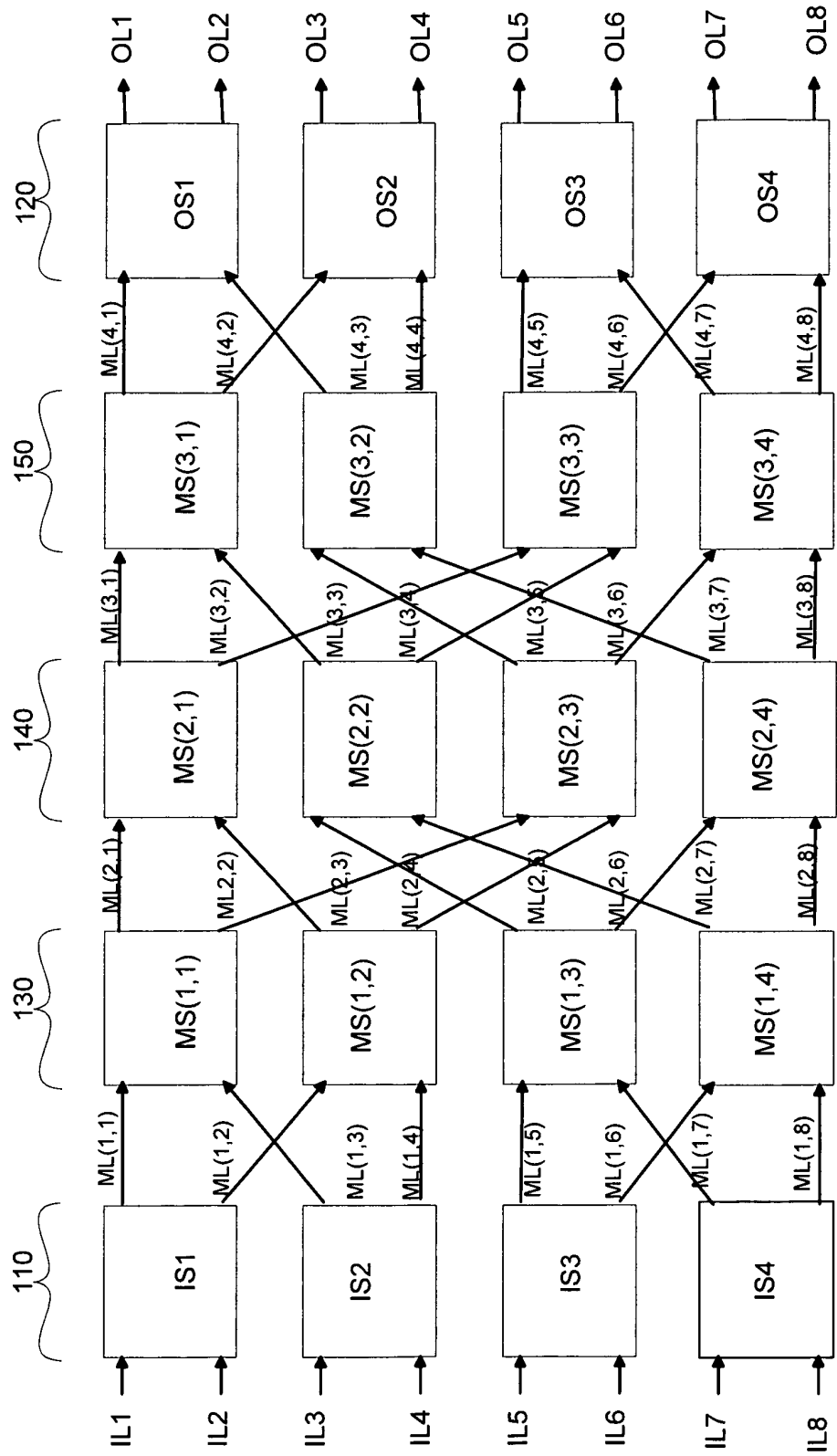


FIG. 6K

600K

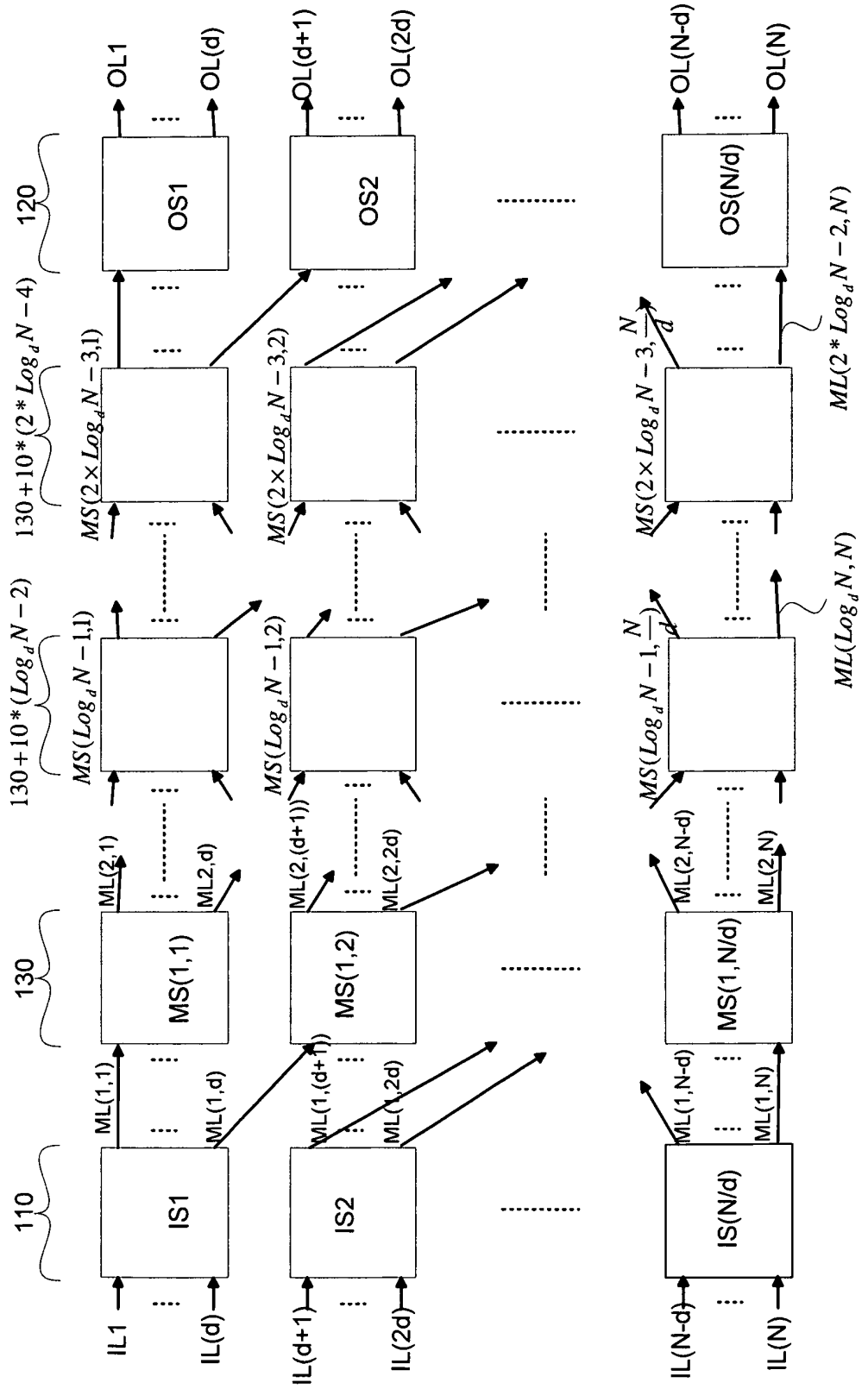


FIG. 6A1

600A1

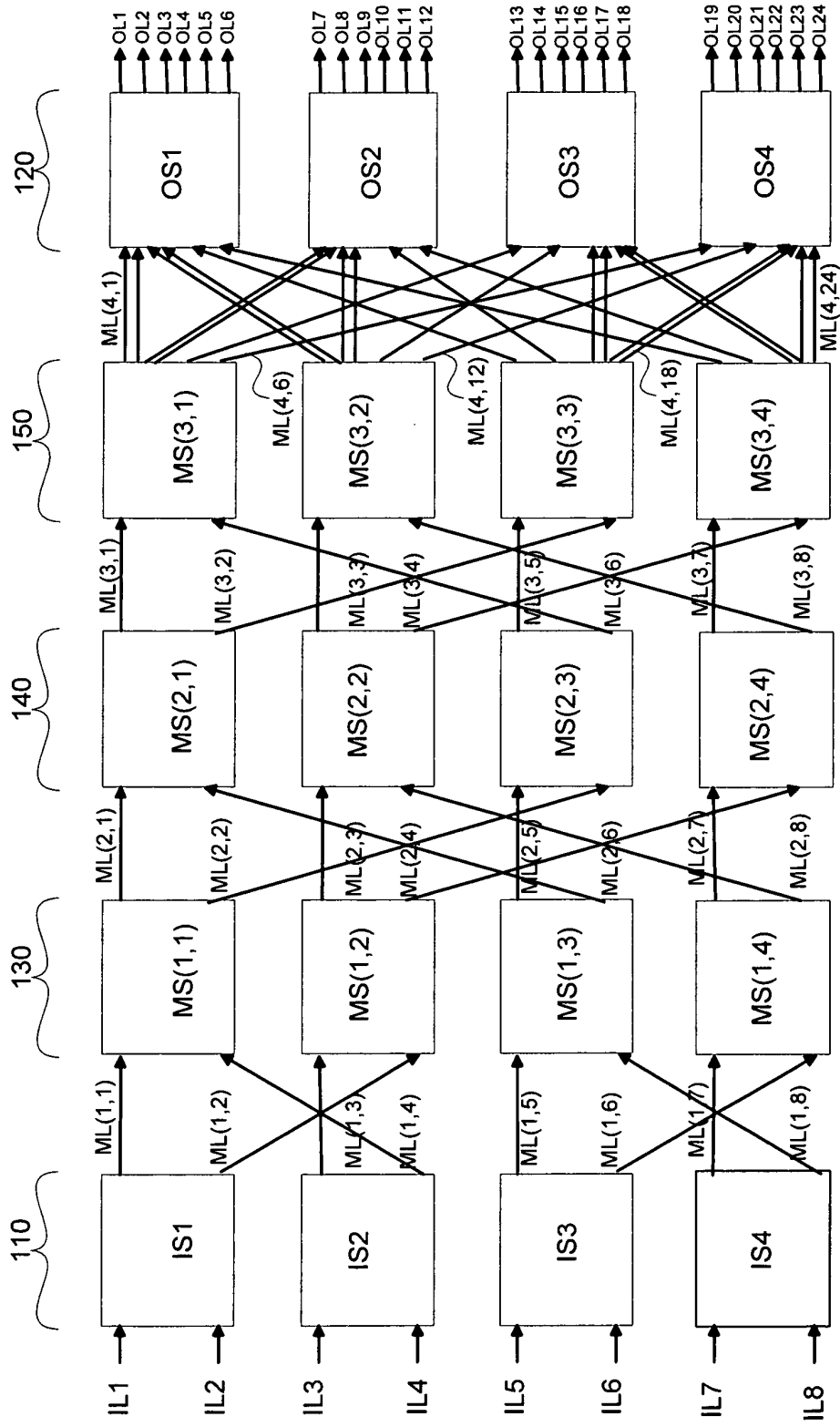


FIG. 6B1

600B1

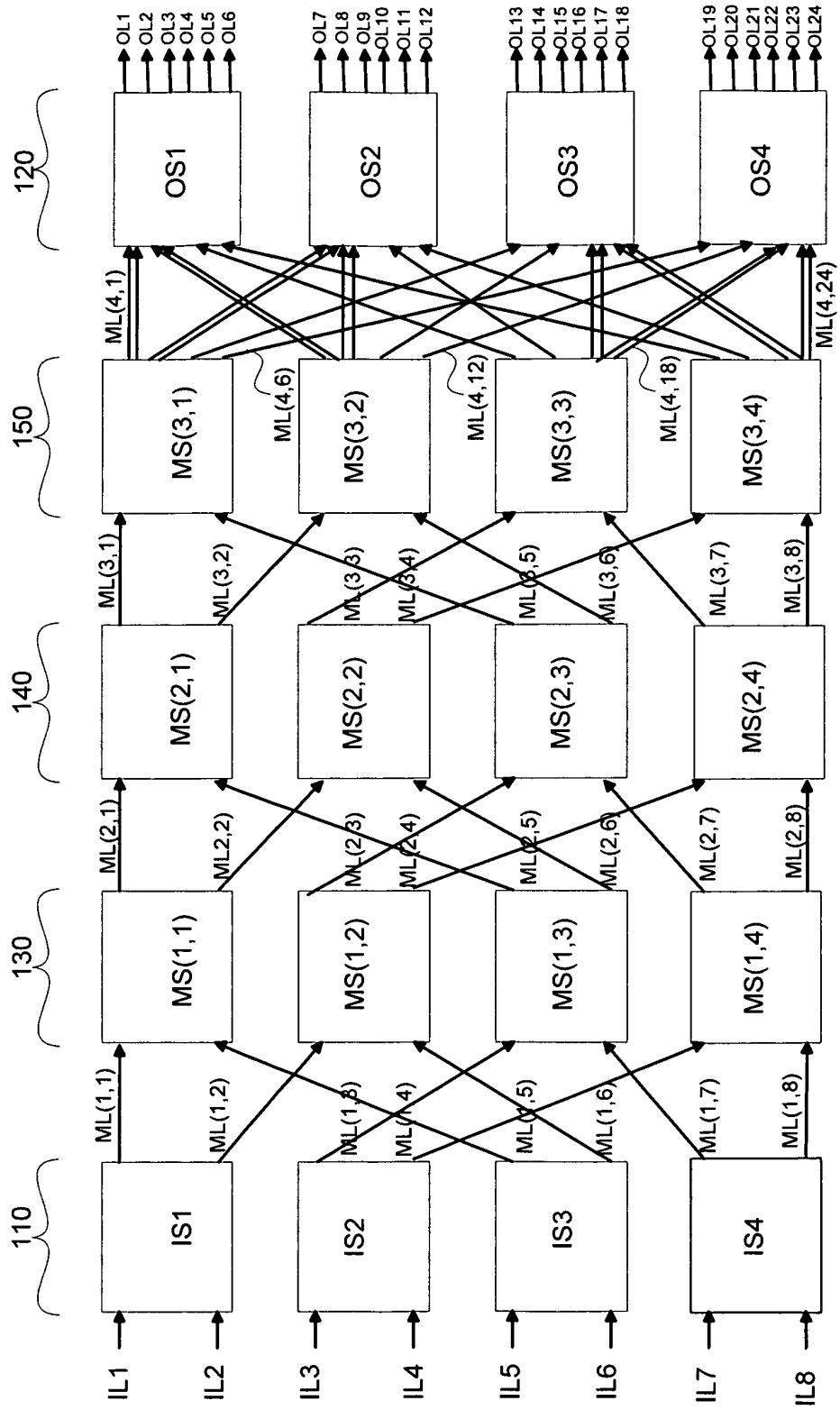


FIG. 6C1

600C1

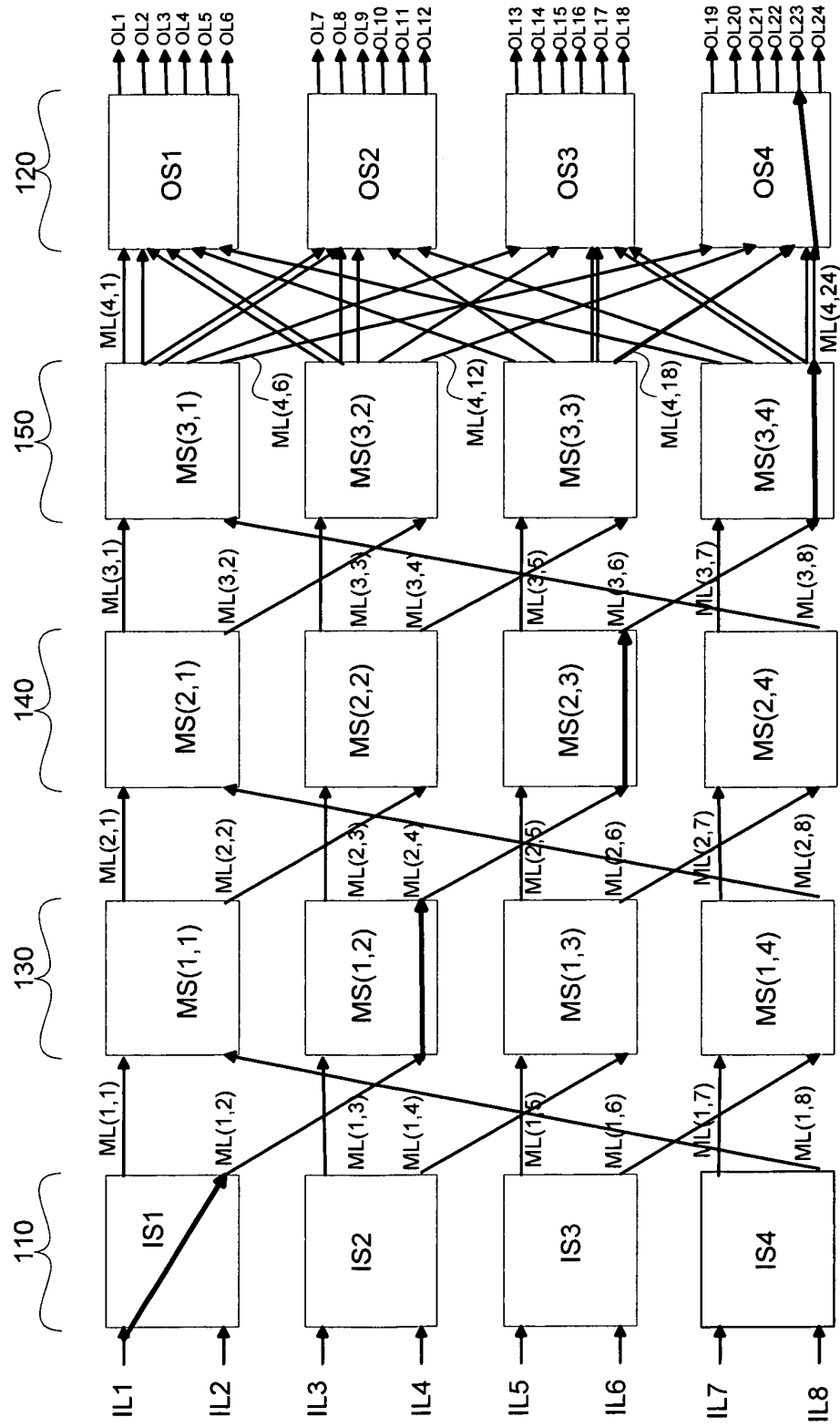


FIG. 6D1

600D1

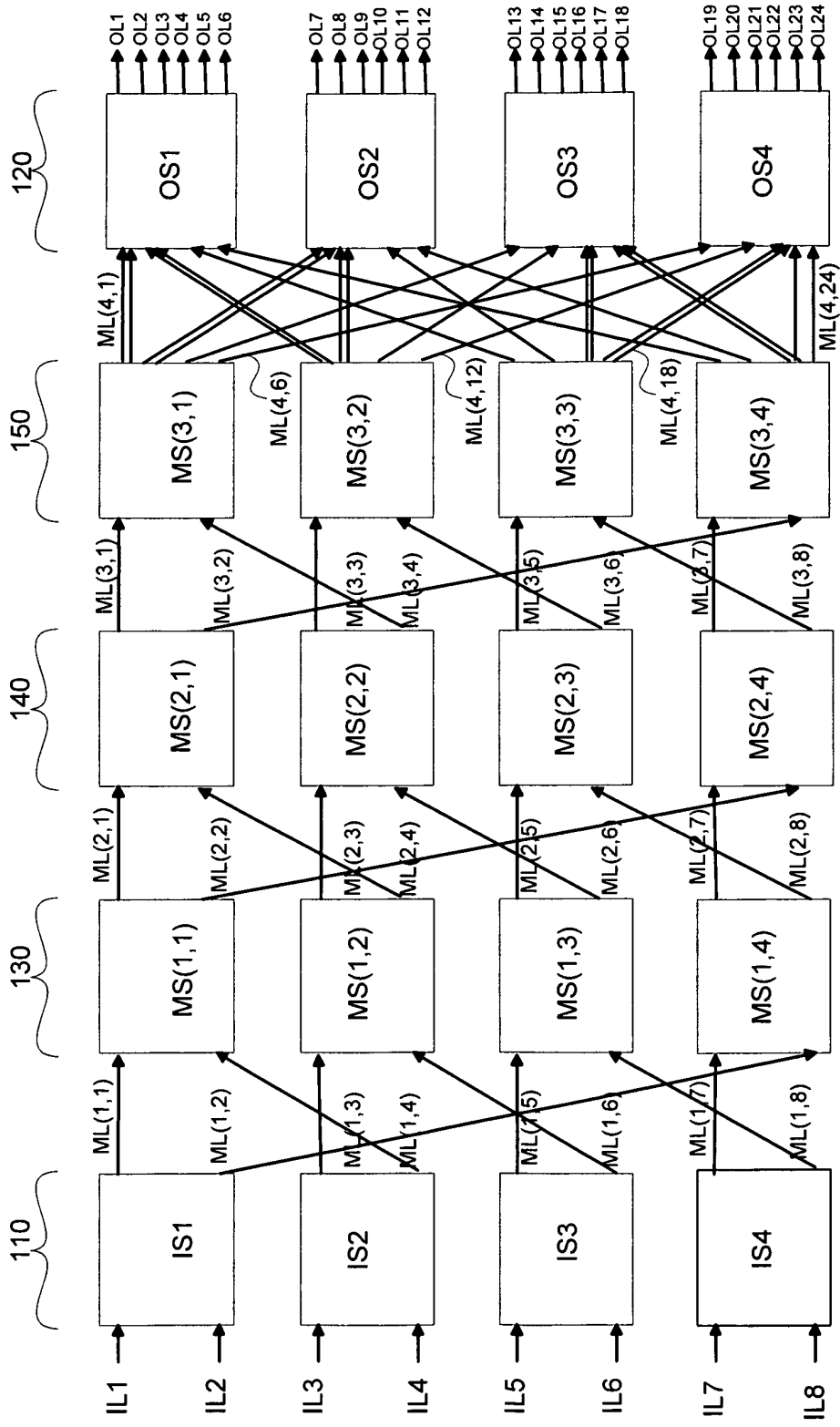


FIG. 6E1

600E1

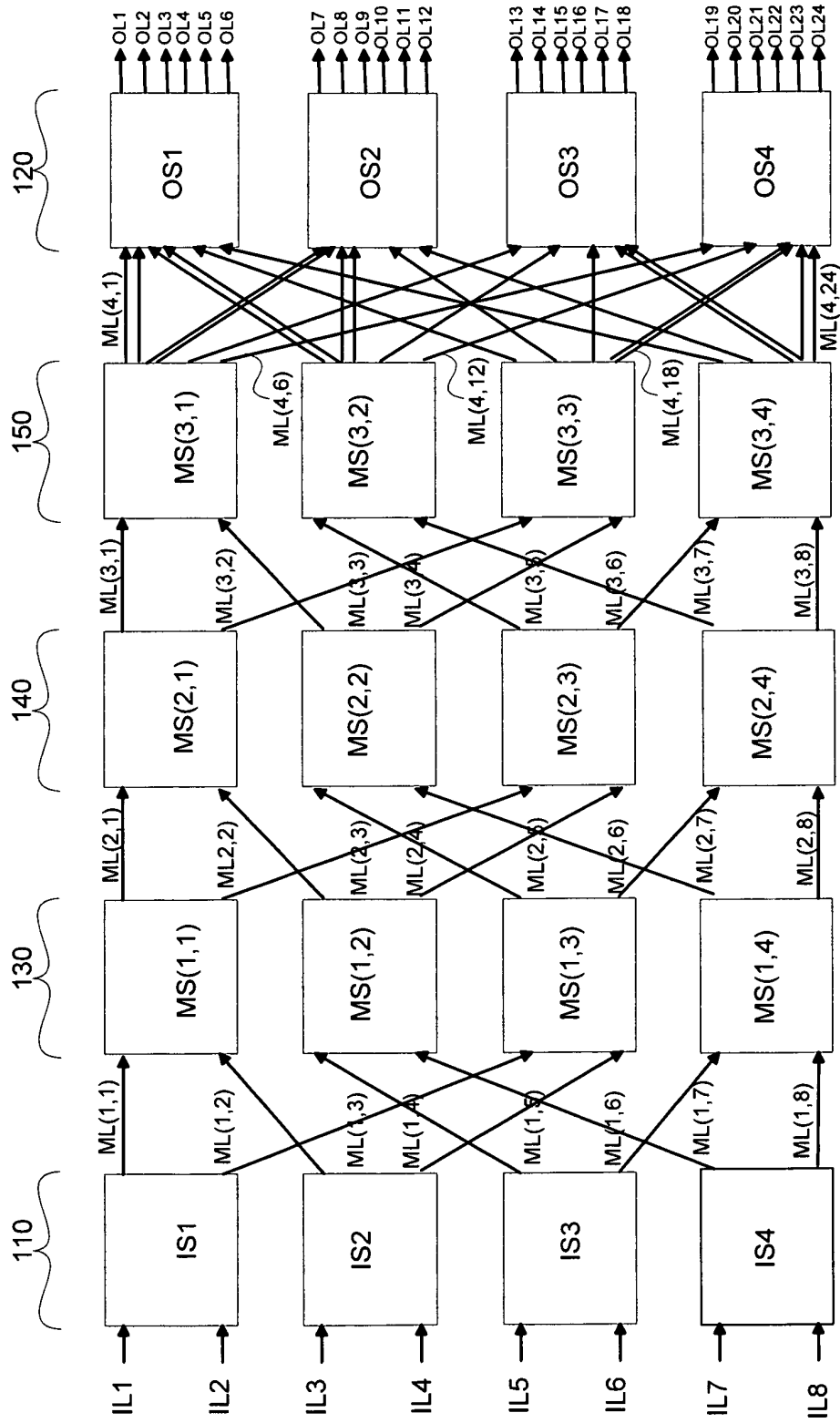


FIG. 6F1

600F1

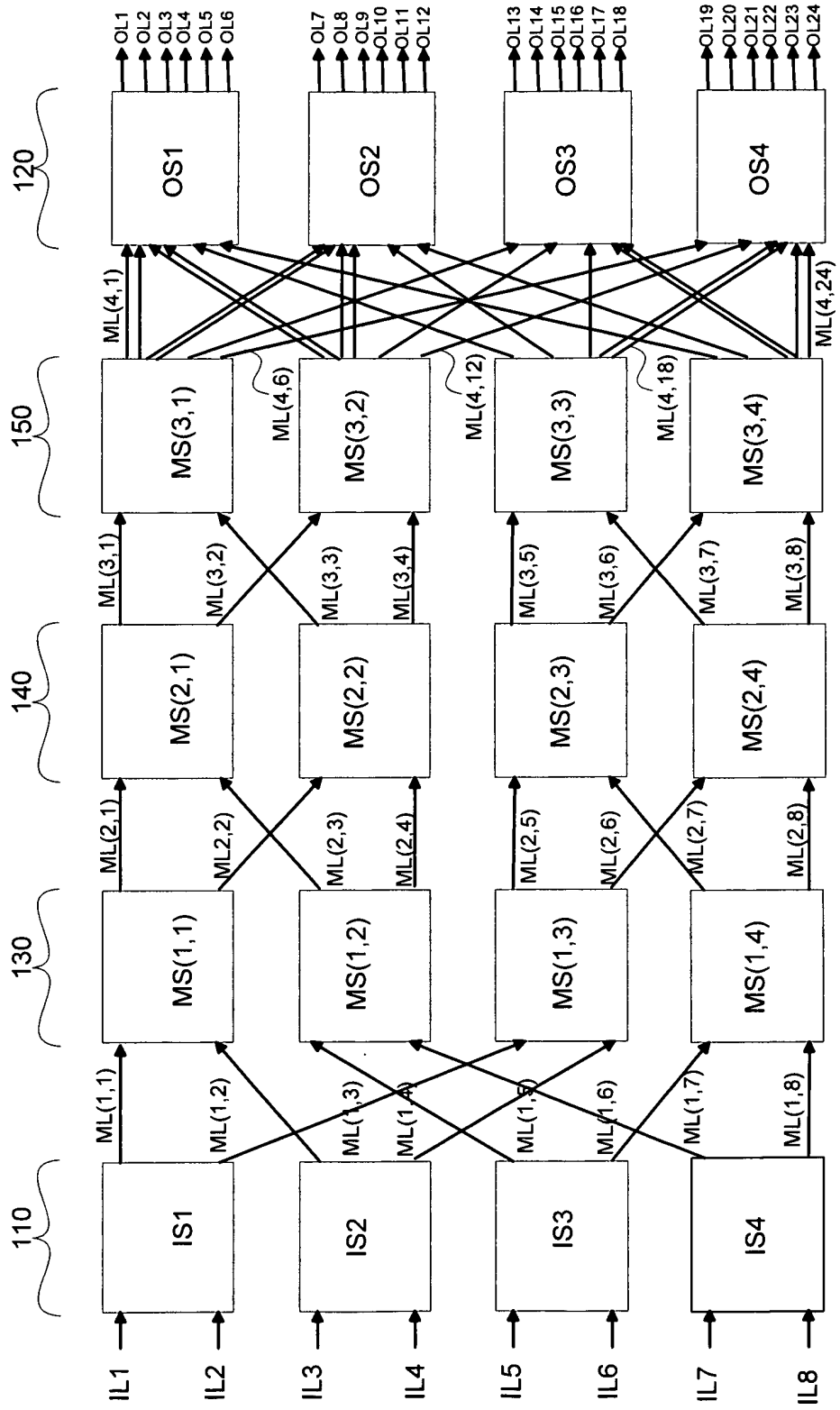


FIG. 6G1

600G1

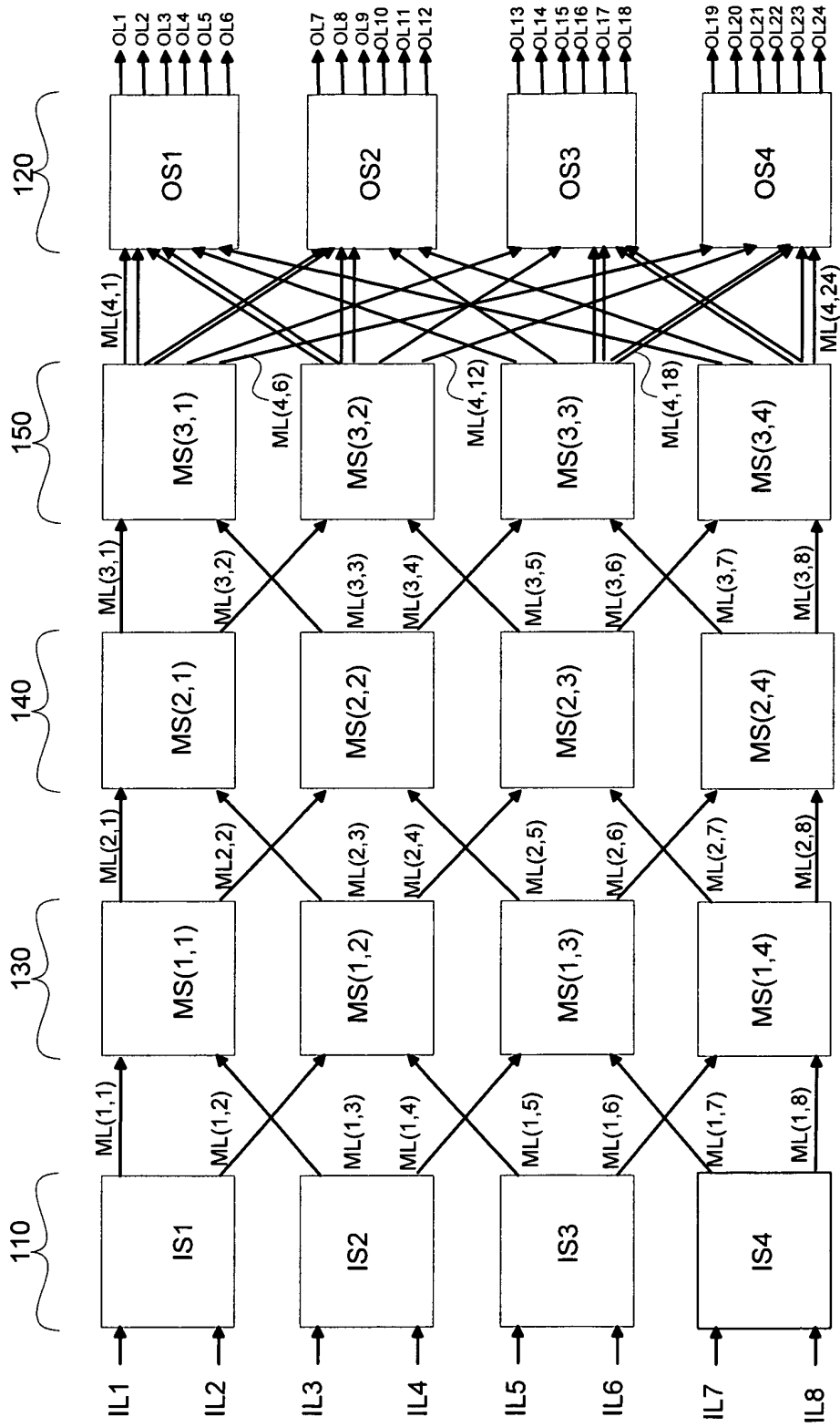


FIG. 6H1

600H1

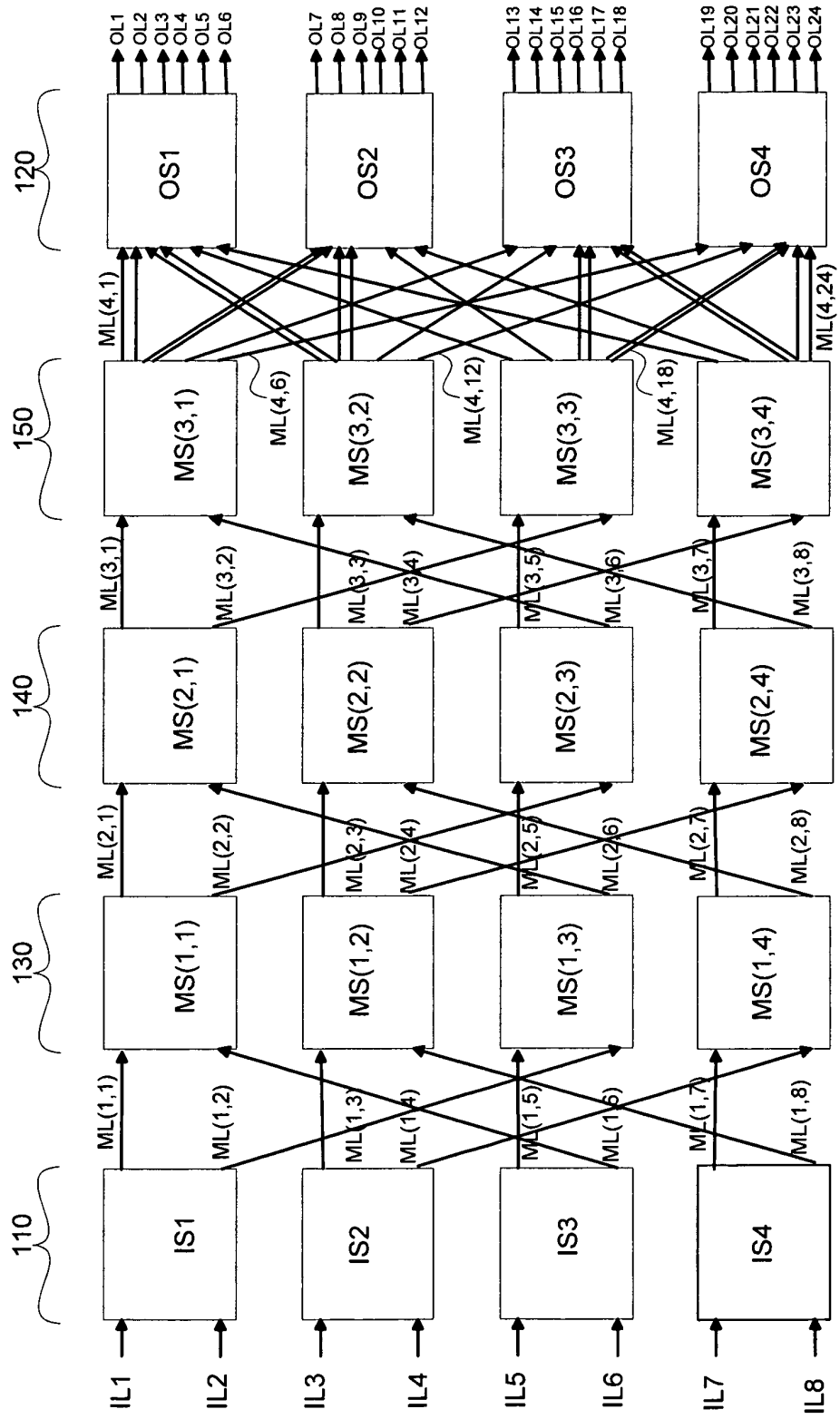


FIG. 6II

60011

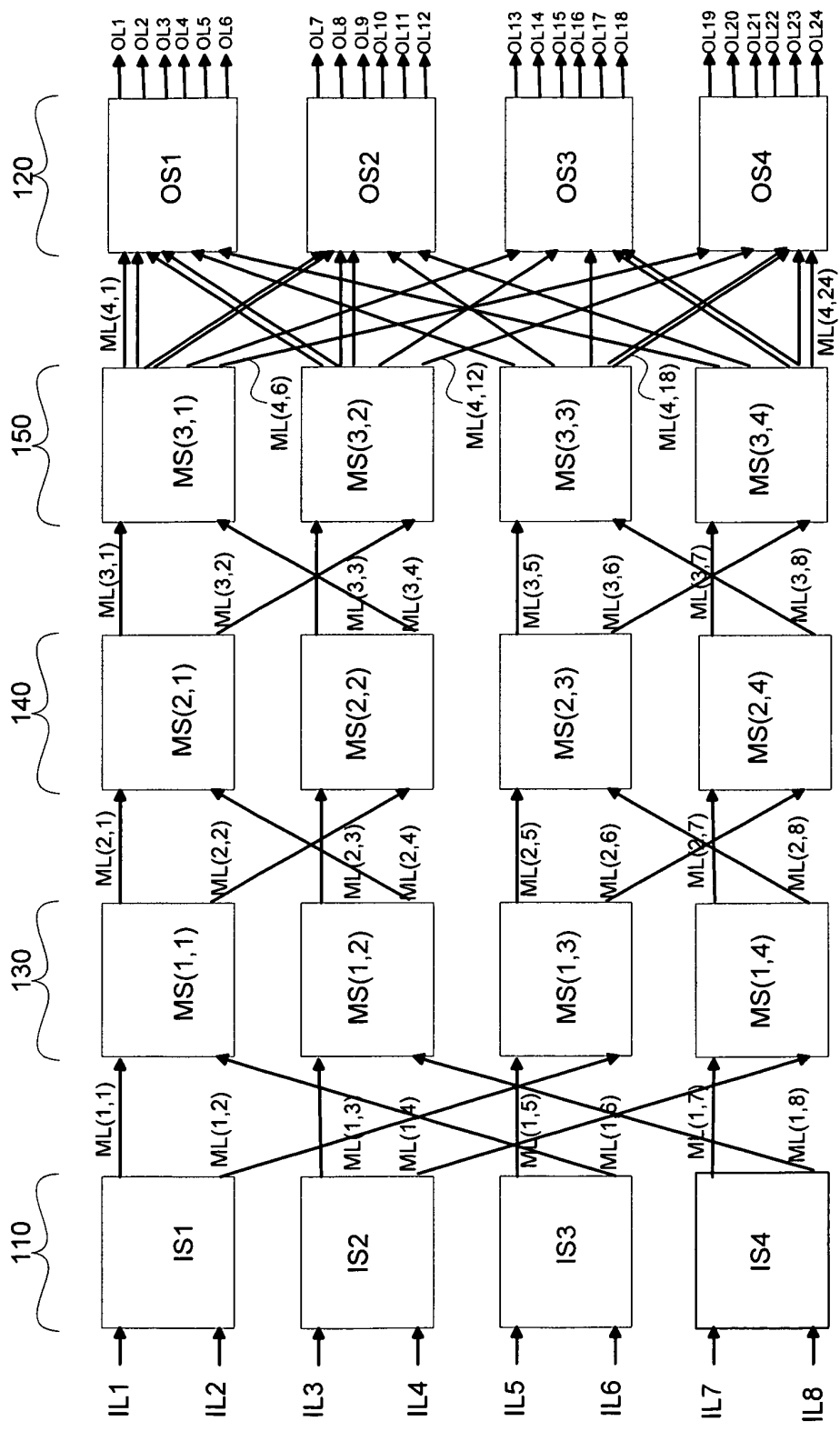


FIG. 6J1

600J1

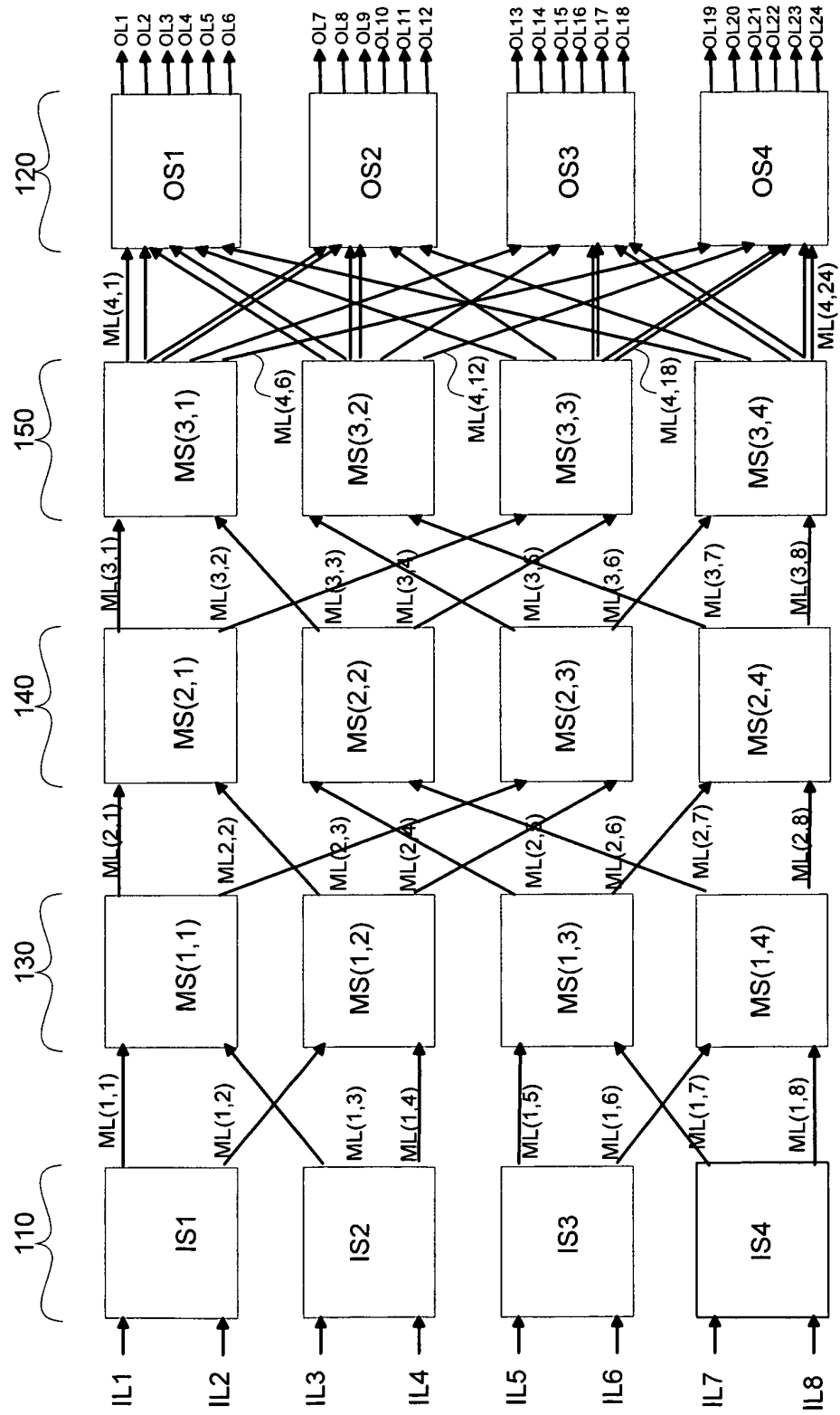


FIG. 6K1

600K1

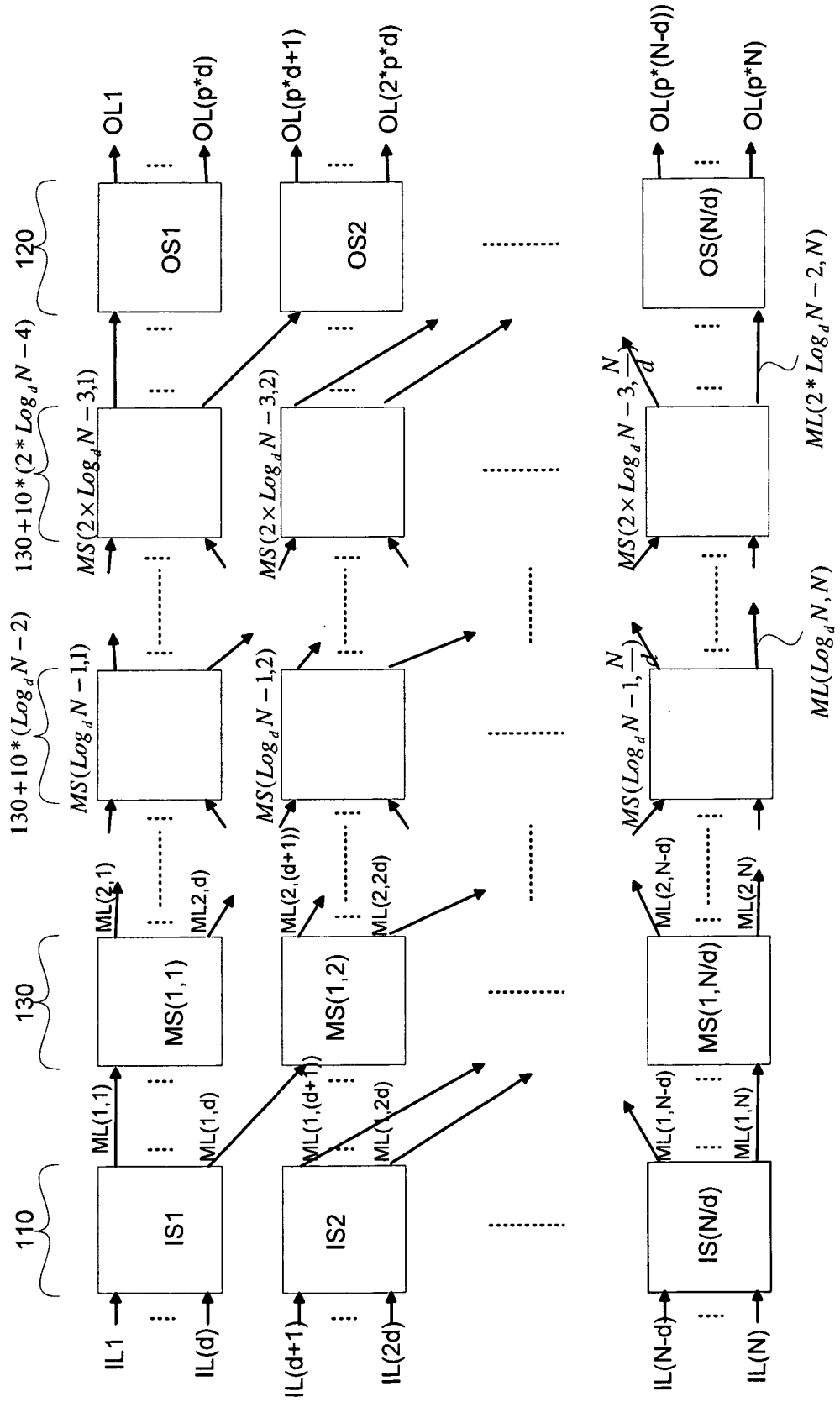


FIG. 6A2

600A2

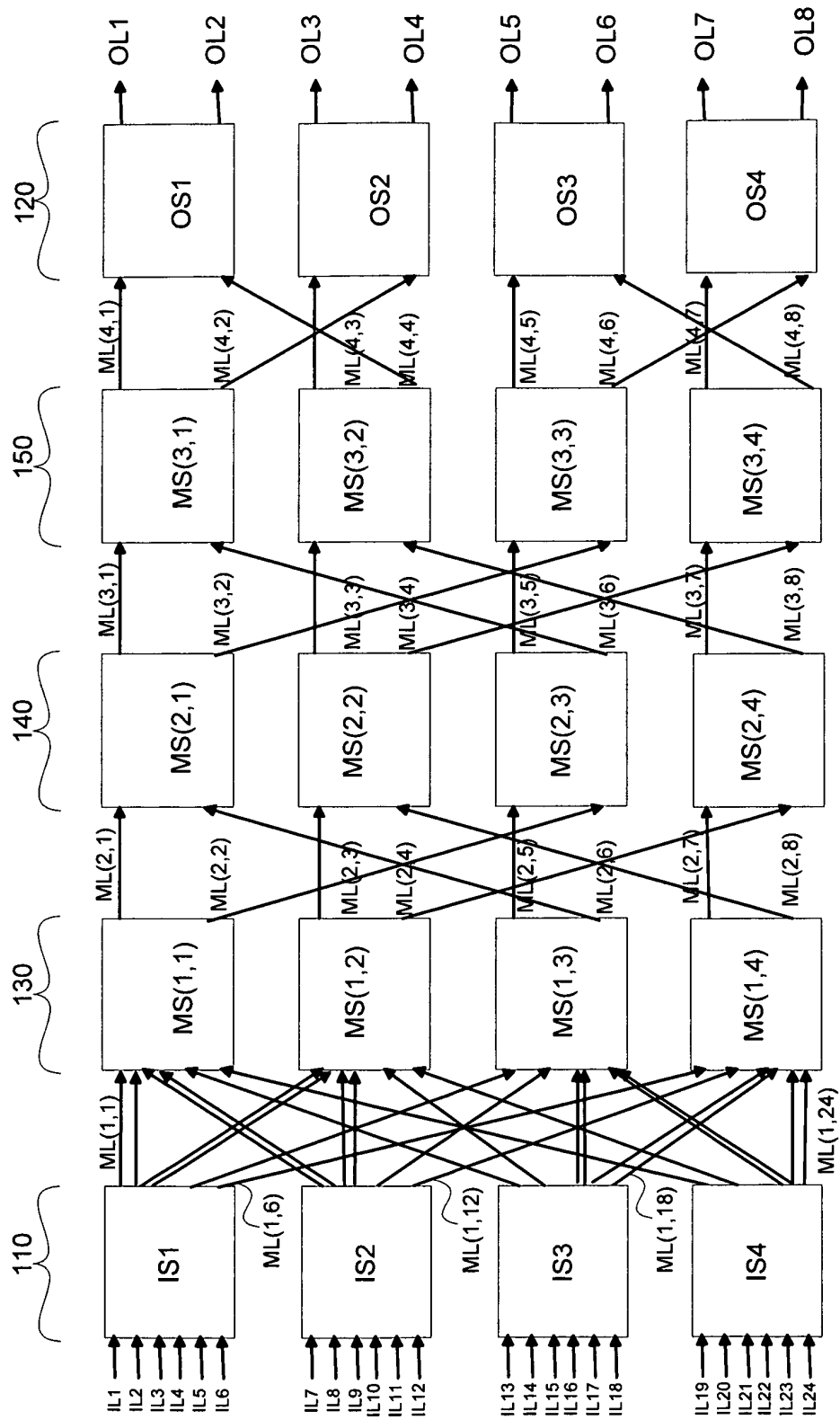


FIG. 6B2

600B2

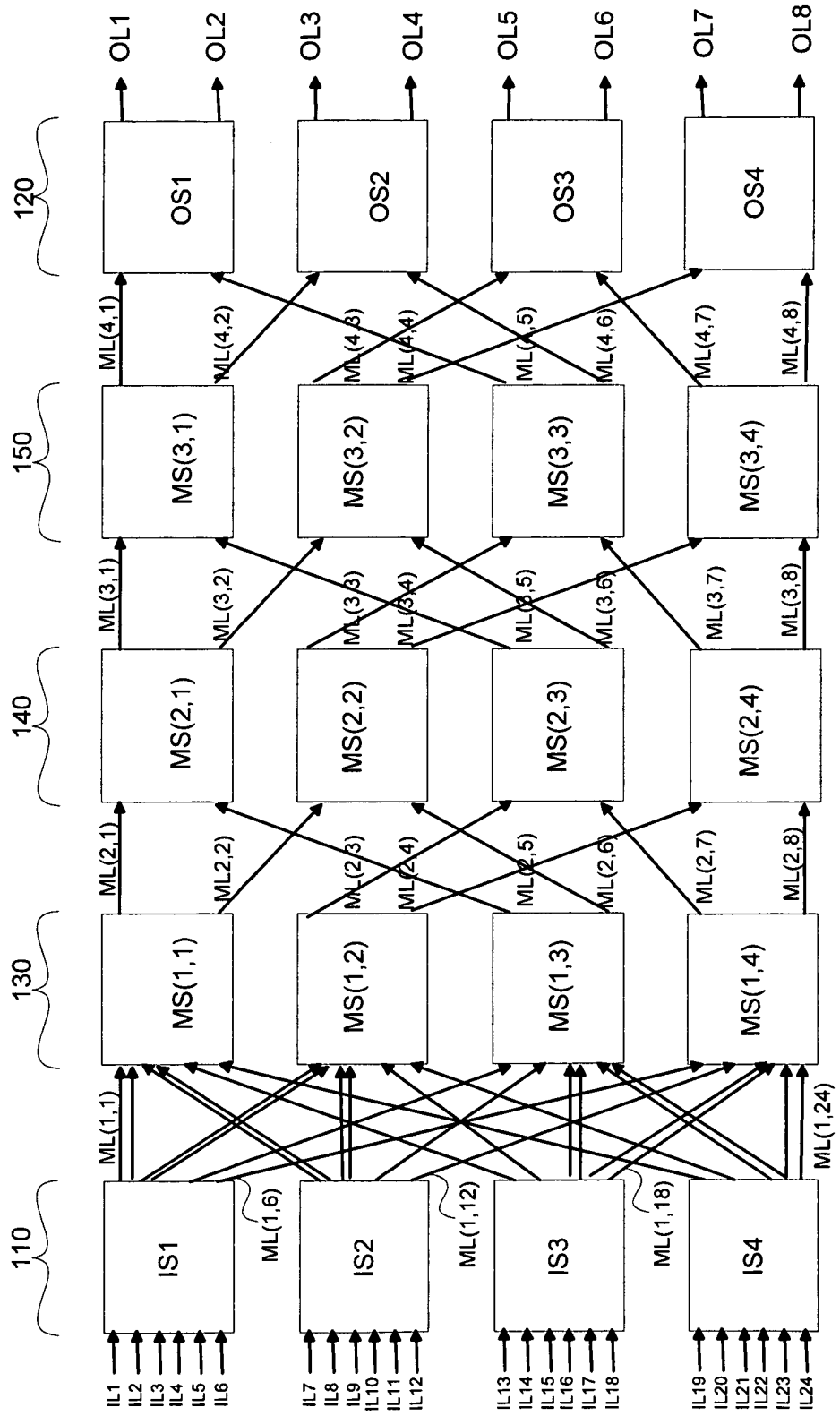


FIG. 6C2

600C2

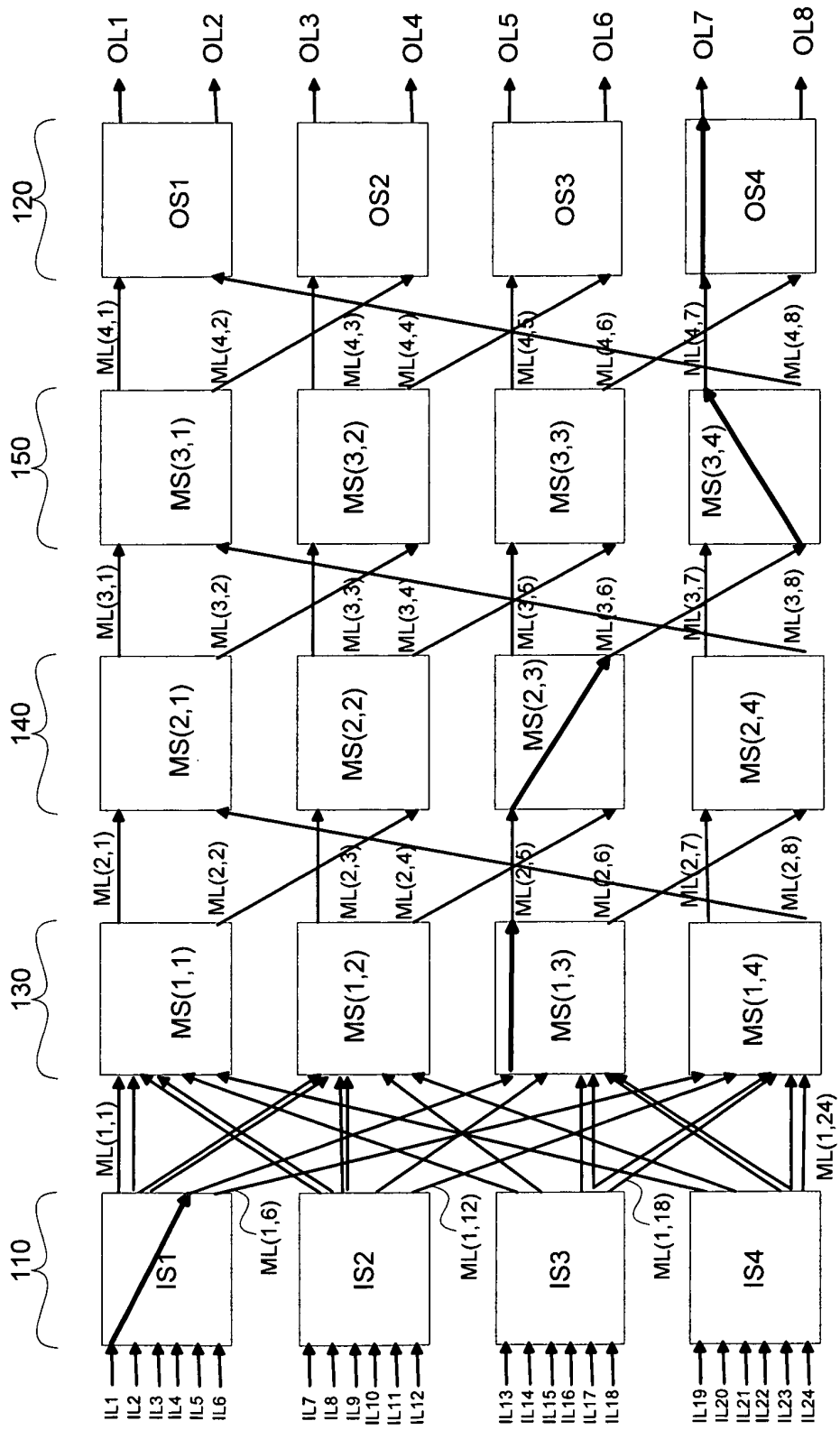


FIG. 6D2

600D2

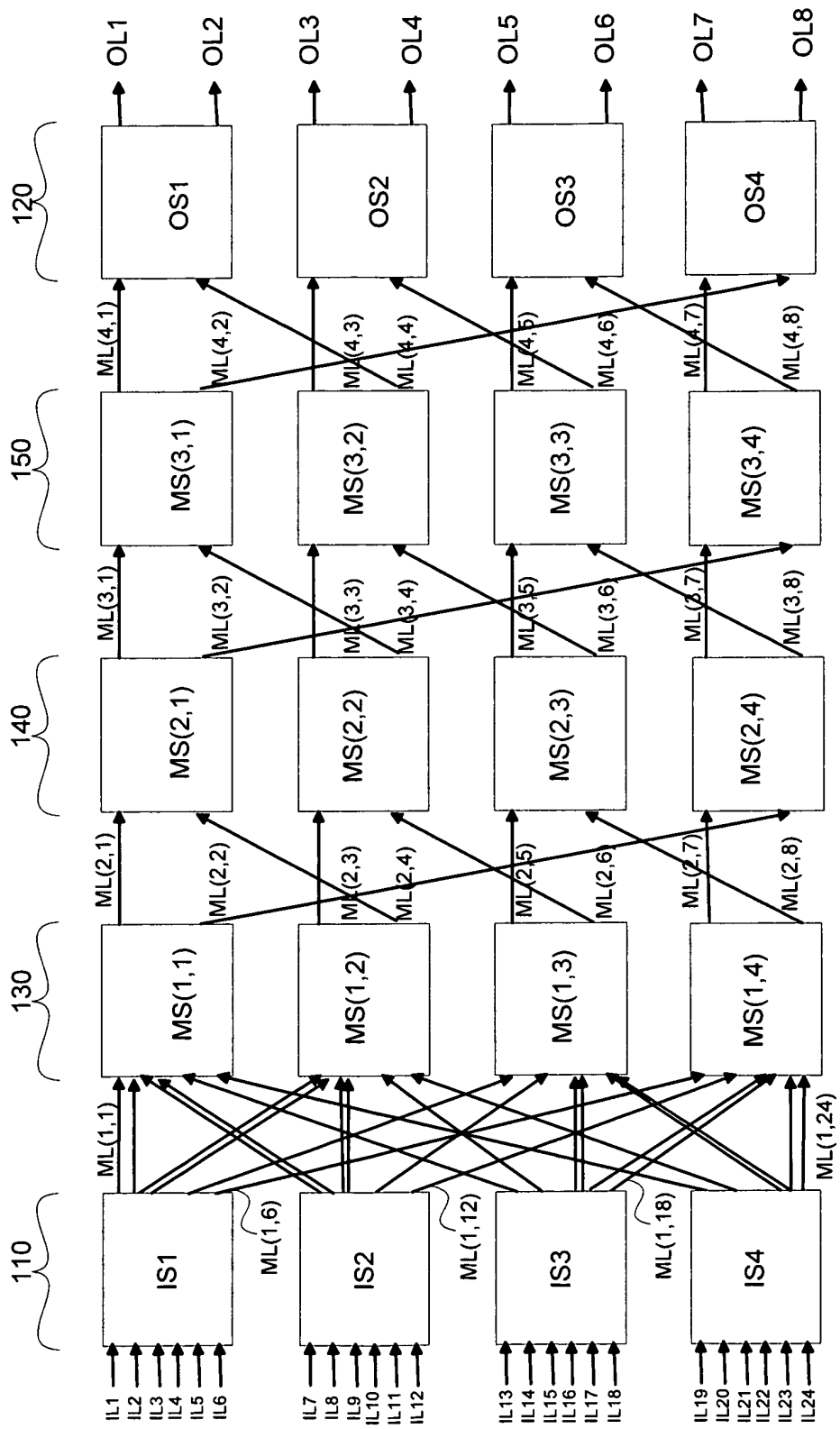


FIG. 6E2

600E2

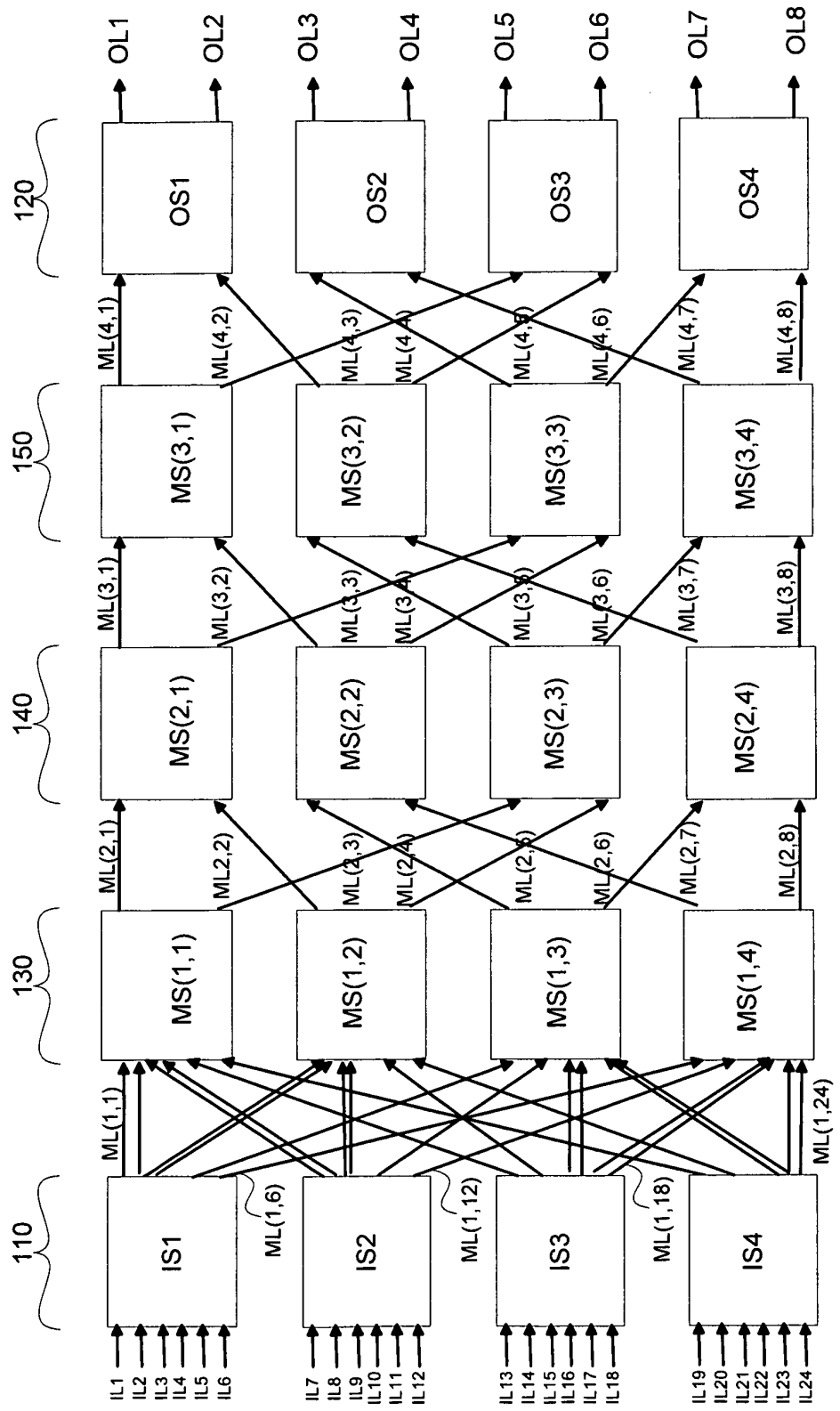


FIG. 6F2

600F2

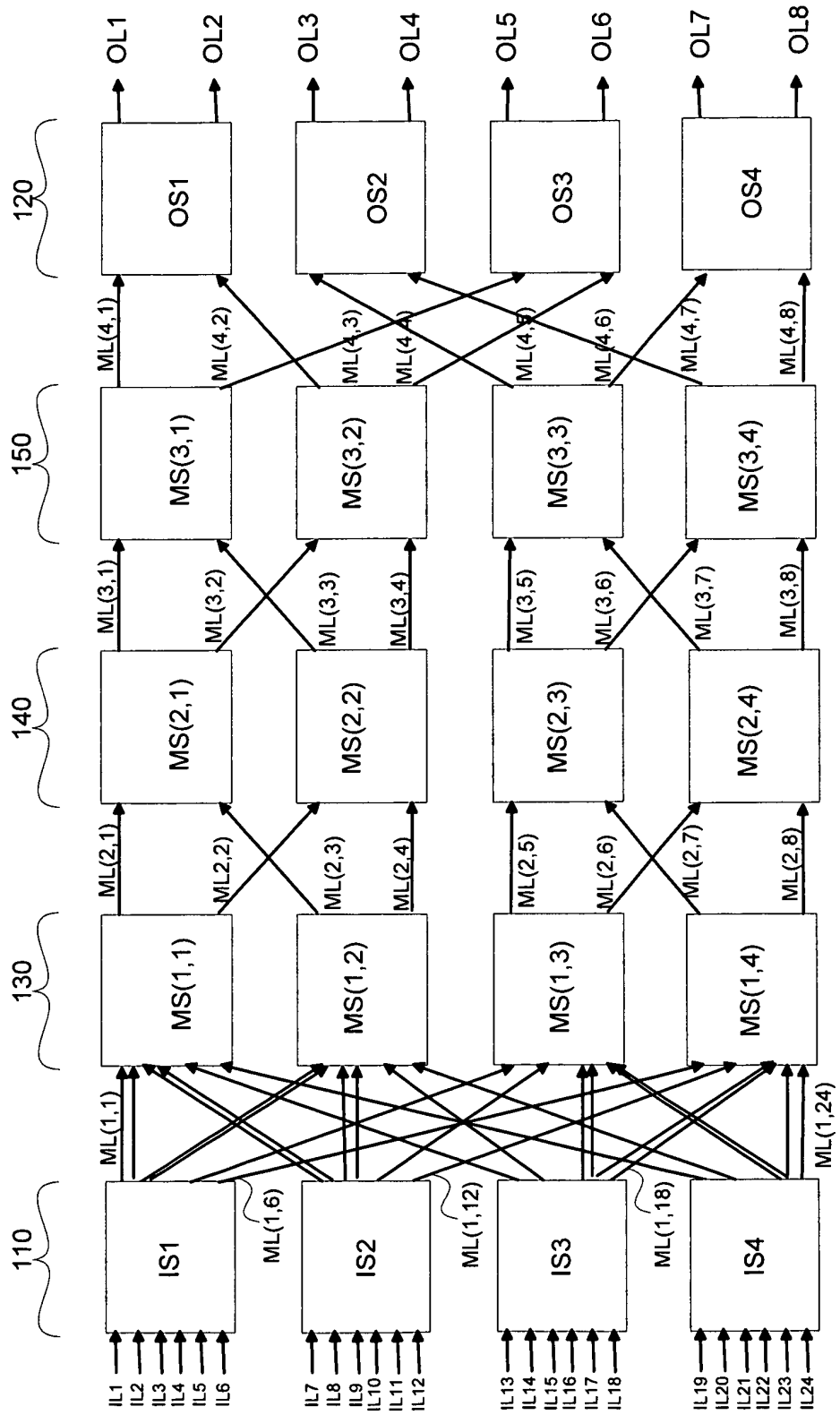


FIG. 6G2

600G2

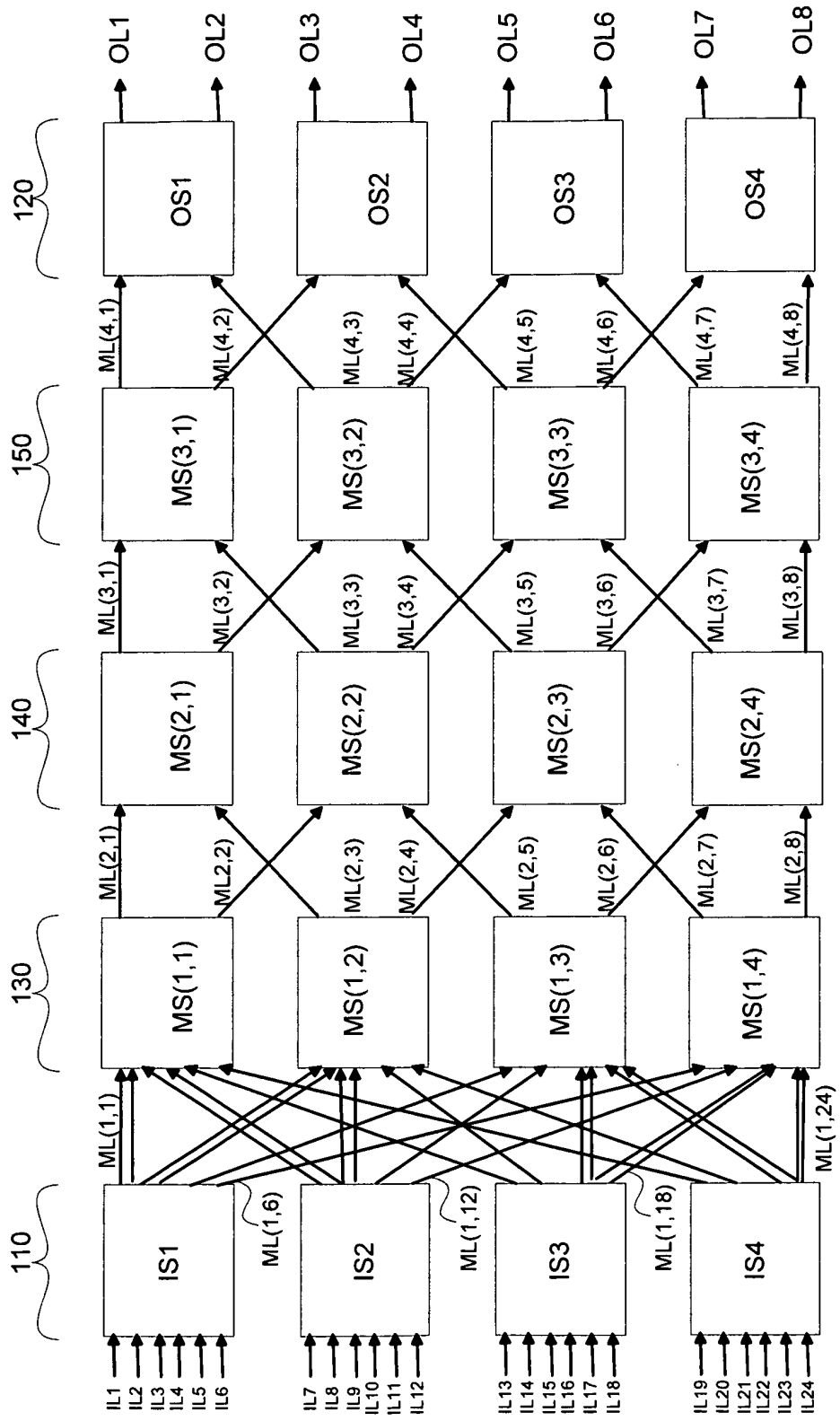


FIG. 6H2

600H2

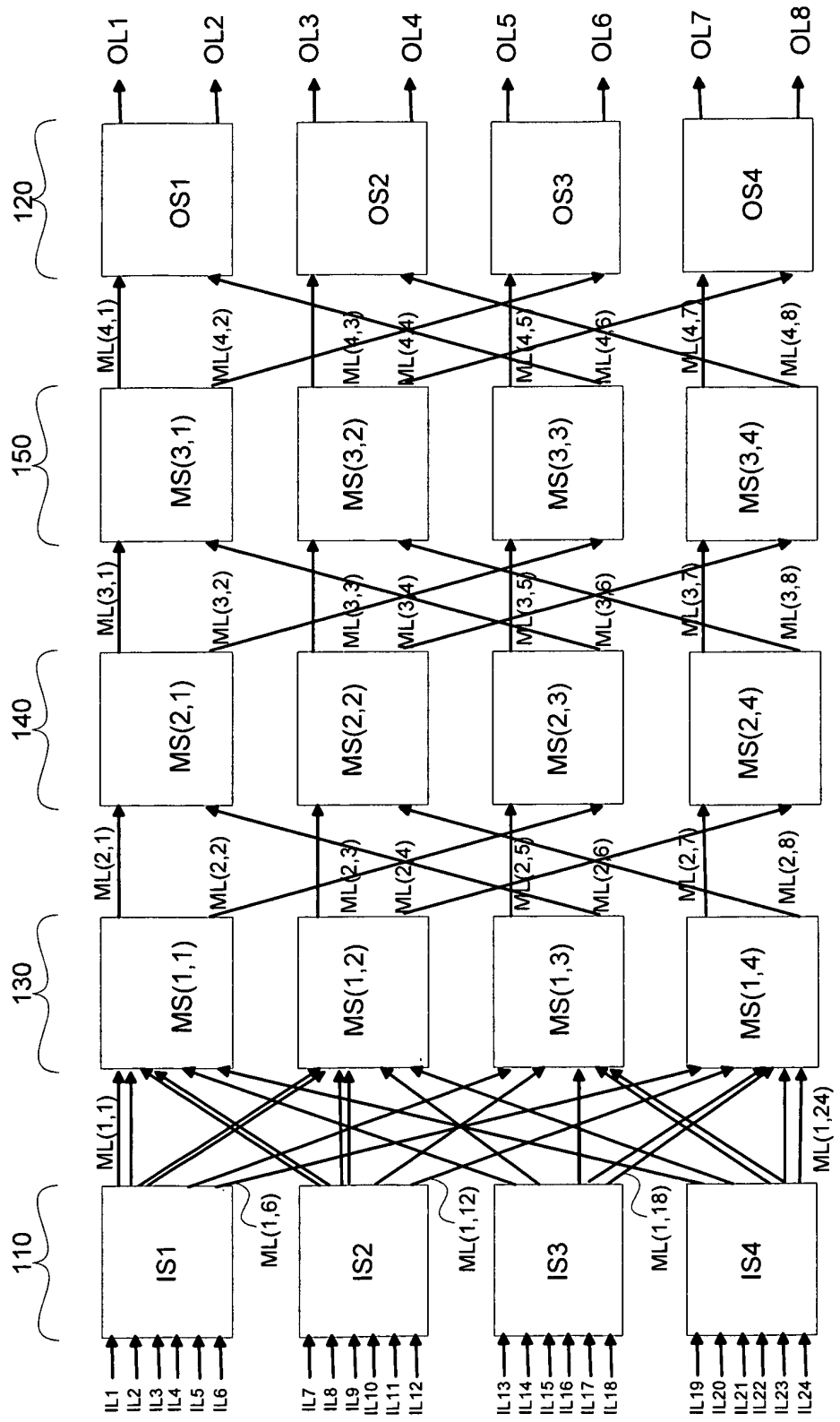


FIG. 6I2

60012

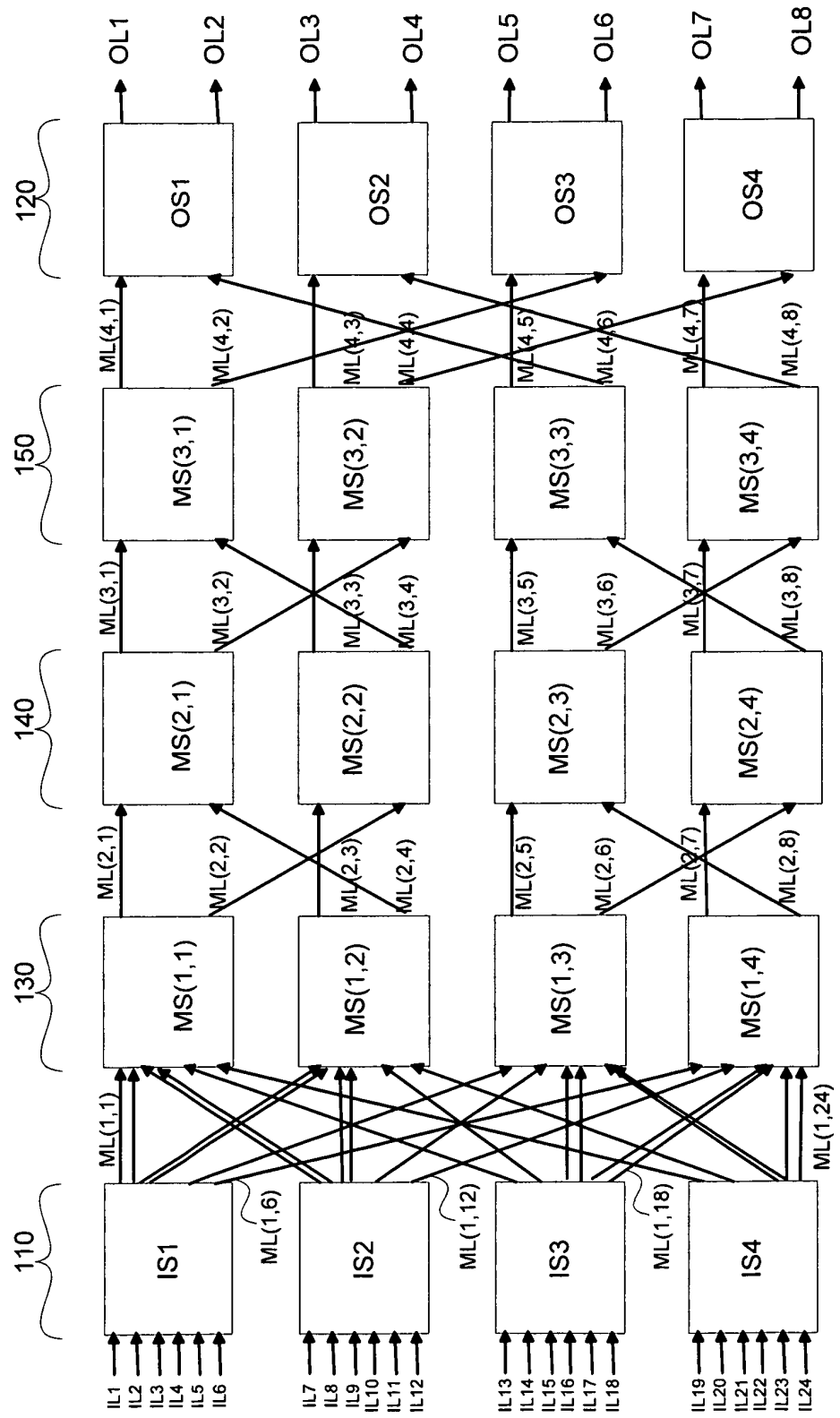


FIG. 6J2

600J2

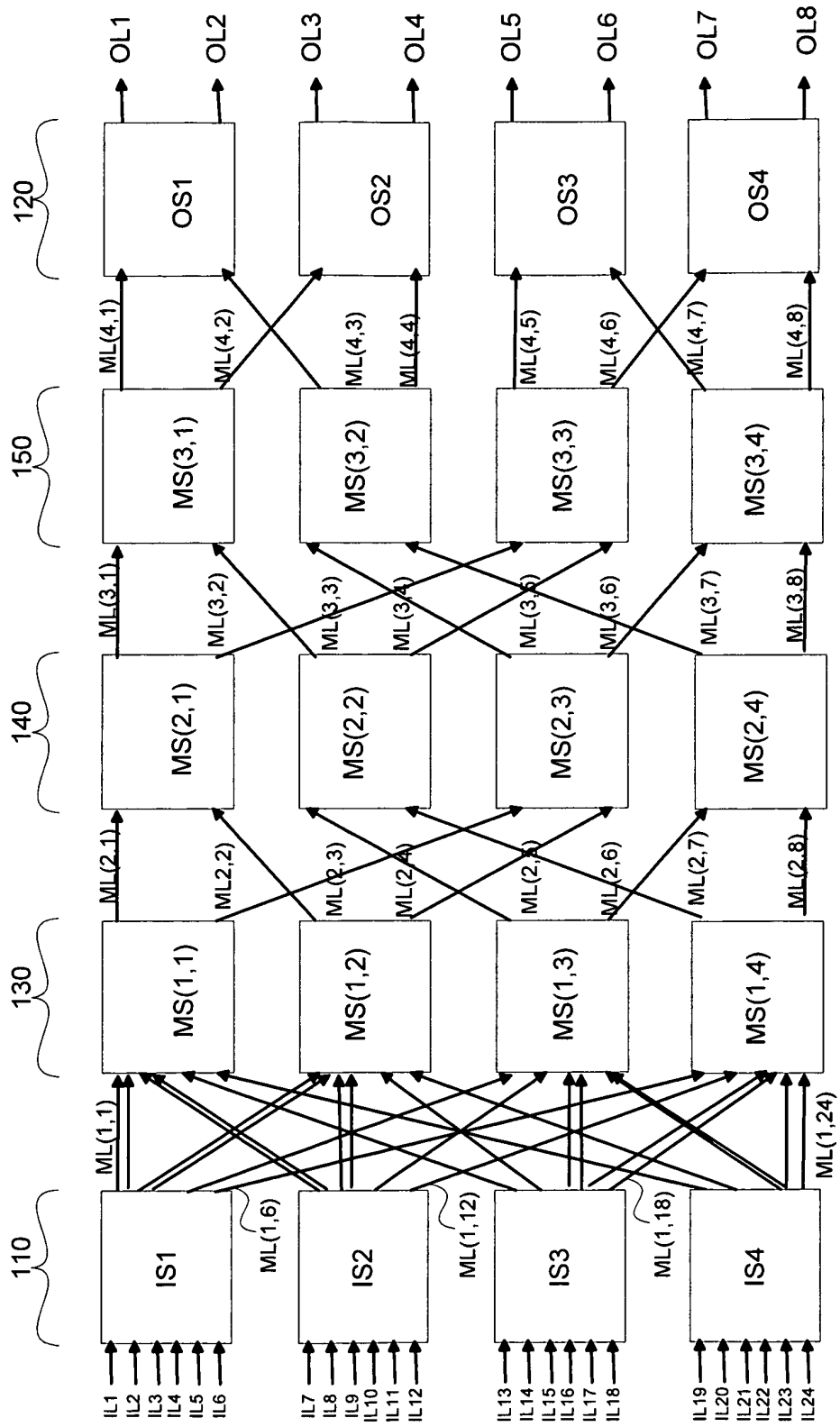
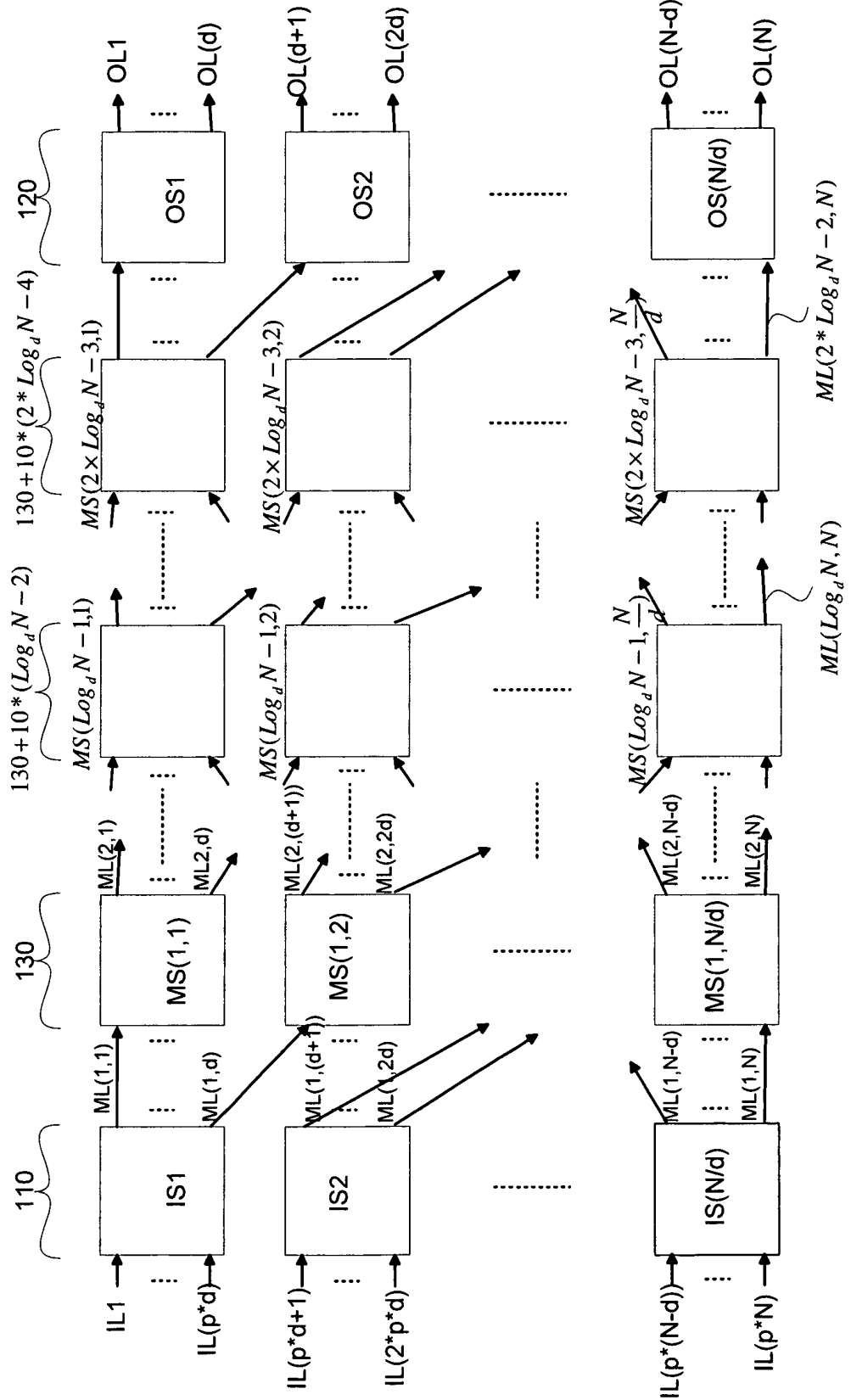


FIG. 6K2

600K2



1000

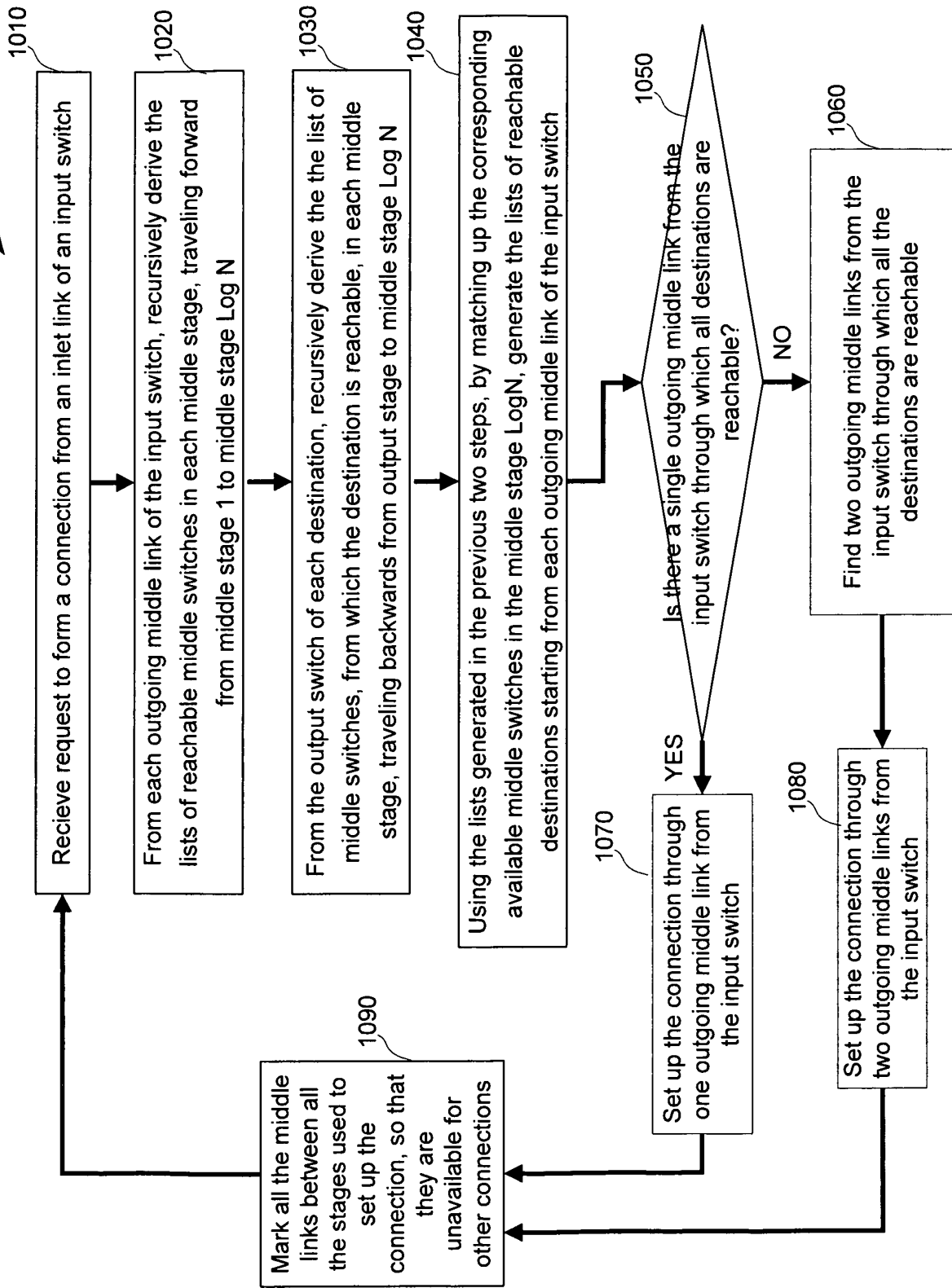


FIG. 8A

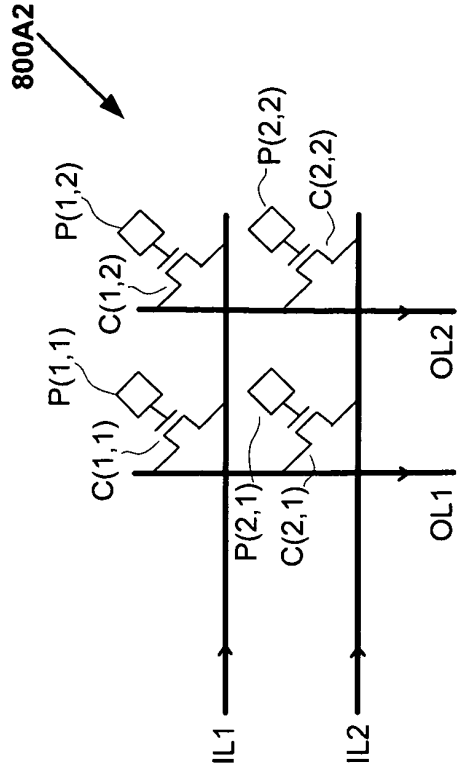


FIG. 8A2
 (Prior Art)

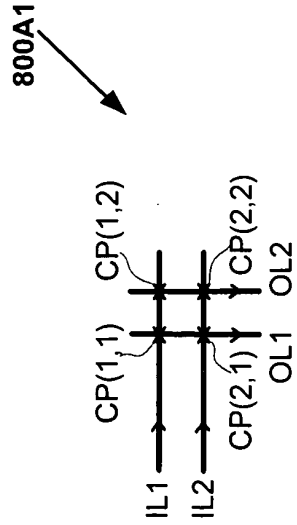


FIG. 8A1
 (Prior Art)

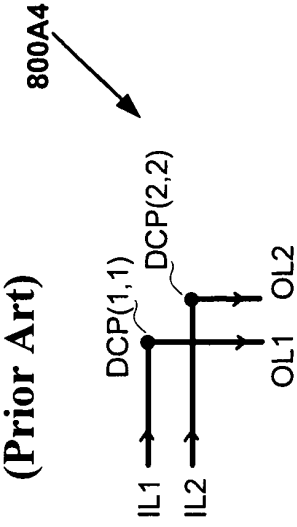


FIG. 8A4

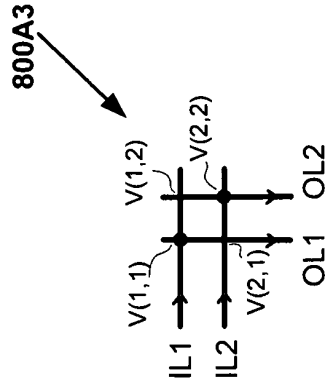


FIG. 8A3
 (Prior Art)

PATENT COOPERATION TREATY

From the RECEIVING OFFICE

PCT

NOTIFICATION CONCERNING PAYMENT
OF PRESCRIBED FEES

(PCT Rules 14, 15 and 16 and Administrative
Instructions, Sections 102bis(c), 304,
323(b), 707(b) and 803)

To: VENKAT KONDA 6278, GRAND OAK WAY SAN JOSE, CALIFORNIA 95135		Date of mailing <i>(day/month/year)</i>		06 Jun 2008
Applicant's or agent's file reference S-0039 PCT		PAYMENT DUE see item 3 for time limits		
International application No. PCT/US2008/064604	International filing date/Date of receipt <i>(day/month/year)</i> 22 May 2008	Priority date <i>(day/month/year)</i> 25 May 2007		
Applicant KONDA, VENKAT				

1. The applicant is hereby notified that this receiving Office has received:

- the payment of all the prescribed fees, and an overpayment, which will be refunded in due course.
 no or insufficient payment of the prescribed fees and the applicant is hereby invited to pay the balance due, as summarized under item 2, within the time limit(s) indicated under item 3.

2. Fees and payment calculation:

7,753.00	-	0.00	=	7,753.00
Total fees payable		Amount paid		Balance

- The details of the calculation are given in the Annex.

3. Time limit(s) for payment and amount(s) payable (Rules 14.1, 15.4 and 16.1(f)):

- within ONE MONTH from the date of receipt of the international application (for the transmittal fee (if any), the search fee and the international filing fee). The amount payable for each fee is the amount applicable on the date of receipt of the international application.
 within 16 MONTHS from the priority date (only for the fee for priority document). The applicant's attention is drawn to the fact that the request made by the applicant under Rule 17.1(b) will be considered not to have been made unless the fee is paid within that time limit.

4. Additional observations *(if necessary)*:

- The search copy will not be transmitted to the International Searching Authority until the search fee is paid (therefore the start of the international search will be delayed) (Rule 23.1(a) and (b)).

Name and mailing address of the receiving Office Mail Stop PCT, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 Facsimile No. 571-273-3201	Authorized officer Larry Hammond Telephone No. 703-308-9290 EX 101
---	--

ANNEX TO FORM PCT/RO/102
CALCULATION OF THE PRESCRIBED FEES

International application No.
PCT/US2008/064604

T Transmittal Fee

Prescribed amount: 300.00 **T**
 Amount paid: - 0.00
 Balance: = 300.00

- correct amount
 overpayment
 balance due

S Search Fee

Prescribed amount: 1,800.00 **S**
 Amount paid: - 0.00
 Balance: = 1,800.00

- correct amount
 overpayment
 balance due

I International Filing Fee

Fixed amount for first 30 sheets: 1,173.00 **i1**
 $\frac{320}{\text{Number of sheets in excess of 30}} \times \frac{14.00}{\text{Fee per sheet}} = 4,480.00$ **i2**
 Additional component: . . . 400 x $\frac{0.00}{\text{Fee per sheet}} = 0.00$ **i3**

Reduction where the international application is filed
 (See PCT Applicant's Guide, Volume I, General Part,
 for details on the availability of this reduction):

using the PCT-EASY software: - 0.00 **r**
 or
 in electronic form where the text of the
 description, claims and abstract is not in
 character coded format: - 0.00 **r**
 or
 in electronic form where the text of the
 description, claims and abstract is in character
 coded format: - 0.00 **r**

Sub-total: = 5,653.00 **i1+i2+i3-r**

Prescribed total amount (The amount to be entered at I is the sub-total
 entered at (i1+i2+i3-r), except where the applicant is (or all applicants
 are) entitled to a reduction of 75%, in which case the amount to be
 entered at I is 25% of the sub-total (i1+i2+i3-r); certain applicants from
 certain States are entitled to a reduction of 75% of the international
 filing fee; see Notes to the Fee Calculation Sheet as annexed to the
 Request Form, PCT/RO/101, for details): = 5,653.00 **I**

Amount paid: - 0.00
 Balance: = 5,653.00

- correct amount
 overpayment
 balance due

P Fee for Priority Document

Prescribed amount: 0.00 **P**
 Amount paid: - 0.00
 Balance: = 0.00

- correct amount
 overpayment
 balance due

PATENT COOPERATION TREATY

From the RECEIVING OFFICE

PCT

To:
 VENKAT KONDA
 6278, GRAND OAK WAY
 SAN JOSE, CALIFORNIA 95135

Confirmation No: 5419

NOTIFICATION OF THE INTERNATIONAL
 APPLICATION NUMBER AND OF THE
 INTERNATIONAL FILING DATE

(PCT Rule 20.2(c))

Date of mailing (day/month/year)	06 Jun 2008
-------------------------------------	-------------

Applicant's or agent's file reference
 S-0039 PCT

IMPORTANT NOTIFICATION

International application No.
 PCT/US2008/064604

International filing date (day/month/year)
 22 May 2008

Priority date (day/month/year)
 25 May 2007

Applicant
 KONDA, VENKAT

Title of the invention
 FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS

- The applicant is hereby notified that the international application has been accorded the international application number and the international filing date indicated above.
- The applicant is further notified that the record copy of the international application:
 - was transmitted to the International Bureau on 06 Jun 2008.
 - has not yet been transmitted to the International Bureau for the reason indicated below and a copy of this notification has been sent to the International Bureau*:
 - because the necessary national security clearance has not yet been obtained.
 - because (reason to be specified):

* The International Bureau monitors the transmittal of the record copy by the receiving Office and will notify the applicant (with Form PCT/IB/301) of its receipt. Should the record copy not have been received by the expiration of 14 months from the priority date, the International Bureau will notify the applicant (Rule 22.1(c)).

3. FOREIGN TRANSMITTAL LICENSE INFORMATION Completed by: LH
- Additional license for foreign transmittal not required. This subject matter is covered by a license already granted or the equivalent U.S. national application. Refer to that license for information concerning its scope.
 - License for foreign transmittal not required. 37 CFR. 5.11(e)(1) or 37 CFR 5.11(e)(2). However, a license may be required for additional subject matter. See 37 CFR 5.15(b).
 - Foreign transmittal license granted. 35 U.S.C. 184; 37 CFR 5.11 on 01 Jun 2008 :
 (date)
 - 37 CFR 5.15(a)
 - 37 CFR 5.15(b)

Name and mailing address of the receiving Office
 Mail Stop PCT, Commissioner for Patents
 P.O. Box 1450, Alexandria, VA 22313-1450
 Facsimile No. 571-273-3201

Authorized officer
Larry Hammond
 Telephone No. 703-308-9290 EX 101

Electronic Patent Application Fee Transmittal

Application Number:	PCT/US08/64604
Filing Date:	22-May-2008
Title of Invention:	FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS
First Named Inventor/Applicant Name:	VENKAT KONDA
Filer:	Venkar Konda
Attorney Docket Number:	S-0039 PCT

International Application for filing in the US receiving office Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Transmittal fee	1601	1	300	300
PCT Search Fee- no prior US appl filed	1602	1	1800	1800
Intl Filing Fee (1st-30 Pgs.) PCT Easy	1701	1	1173	1173
Suppl. Intl Filing Fee (each page > 30)	1703	320	14	4480

Pages:

Claims:

Miscellaneous-Filing:

Petition:

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				7753

Electronic Acknowledgement Receipt

EFS ID:	3489290
Application Number:	
International Application Number:	PCT/US08/64604
Confirmation Number:	5419
Title of Invention:	FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS
First Named Inventor/Applicant Name:	VENKAT KONDA
Customer Number:	38139
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Filer:	Venkar Konda
Filer Authorized By:	
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Application Type:	International Application for filing in the US receiving office

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Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Fee Worksheet (PTO-06)	fee-info.pdf	8600 6788241c0b9d642d2d44f8e64ec1aa095656d3af	no	2

Warnings:

Information:

Total Files Size (in bytes):	8600
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

PCT

NOTIFICATION OF RECEIPT
OF SEARCH COPY

(PCT Rule 25.1)

To:
VENKAT KONDA
6278, GRAND OAK WAY
SAN JOSE, CALIFORNIA 95135

PALM Tracking Number = 51864604

Date of mailing (day/month/year) 02 Jul 2008

Applicant's or agent's file reference
S-0039 PCT

IMPORTANT NOTIFICATION

International application No.
PCT/US2008/064604

International filing date (day/month/year)
22 May 2008

Priority date (day/month/year)
25 May 2007

Applicant
KONDA, VENKAT

1. Where the International Searching Authority and the receiving Office are not the same Office:
The applicant is hereby notified that the search copy of the international application was received by this International Searching Authority on the date indicated below.

Where the International Searching Authority and the receiving Office are the same Office:
The applicant is hereby notified that the search copy of the international application was received on the date indicated below.

02 Jul 2008 _____ (date of receipt).
2. The search copy was accompanied by a nucleotide and/or amino acid sequence listing or tables related thereto in computer readable form.
3. Time limit for establishment of international search report and written opinion of the International Searching Authority
The applicant is informed that the time limit for establishing the international search report and the written opinion of the International Searching Authority is three months from the date of receipt indicated above or nine months from the priority date, whichever time limit expires later (Rules 42.1 and 43bis.1(a)).
4. A copy of this notification has been sent to the International Bureau and, where the first sentence of paragraph 1 applies, to the receiving Office.

Name and mailing address of the ISA/
Mail Stop PCT, Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450
Facsimile No. 571-273-3201

Authorized officer
Phyllis Williams
Telephone No. 703-308-9290 EX 140

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

PCT

NOTIFICATION OF TRANSMITTAL OF
THE INTERNATIONAL SEARCH REPORT AND
THE WRITTEN OPINION OF THE INTERNATIONAL
SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

To: VENKAT KONDA 6278 GRAND OAK WAY SAN JOSE, CA 95135		Date of mailing (day/month/year) 15 AUG 2008
Applicant's or agent's file reference S-0039 PCT	FOR FURTHER ACTION See paragraphs 1 and 4 below	
International application No. PCT/US 08/64604	International filing date (day/month/year) 22 May 2008 (22.05.2008)	
Applicant VENKAT KONDA		

1. The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:
 The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes
 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 740 1435

For more detailed instructions, see the notes on the accompanying sheet.

2. The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. **With regard to the protest against payment of (an) additional fee(s) under Rule 40.2,** the applicant is notified that:

the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**
 Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90bis.1 and 90bis.3, respectively, before the completion of the technical preparations for international publication.

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774
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Form PCT/ISA/220 (January 2004)

(See notes on accompanying sheet)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference S-0039 PCT	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US 08/64604	International filing date (<i>day/month/year</i>) 22 May 2008 (22.05.2008)	(Earliest) Priority Date (<i>day/month/year</i>) 25 May 2007 (25.05.2007)
Applicant VENKAT KONDA		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 23 sheets.

It is also accompanied by a copy of each prior art document cited in this report.

1. Basis of the report

a. With regard to the **language**, the international search was carried out on the basis of:

the international application in the language in which it was filed.

a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6bis(a)).

c. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. **Certain claims were found unsearchable** (see Box No. II).

3. **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

the text is approved as submitted by the applicant.

the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

the text is approved as submitted by the applicant.

the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 1A

as suggested by the applicant.

as selected by this Authority, because the applicant failed to suggest a figure.

as selected by this Authority, because this figure better characterizes the invention.

b. none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 08/64604

Box No. IV Text of the abstract (Continuation of item 5 of the first sheet)

A generalized multi-link multi-stage network comprising $(2 \times \log_2 N) - 1$ stages is operated in strictly nonblocking manner for unicast includes an input stage having N/d switches with each of them having d inlet links and $2 \times d$ outgoing links connecting to second stage switches, an output stage having N/d switches with each of them having d outlet links and $2 \times d$ incoming links connecting from switches in the penultimate stage. The network also has $(2 \times \log_2 N) - 3$ middle stages with each middle stage having N/d switches, and each switch in the middle stage has $2 \times d$ incoming links connecting from the switches in its immediate preceding stage, and $2 \times d$ outgoing links connecting to the switches in its immediate succeeding stage. Also the same generalized multi-link multistage network is operated in rearrangeably nonblocking manner for arbitrary fan-out multicast and each multicast connection is set up by use of at most two outgoing links from the input stage switch.

Form PCT/ISA/210 (continuation of first sheet (3)) (April 2007)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 08/64604

<p>A. CLASSIFICATION OF SUBJECT MATTER IPC(8) - H04L 12/50 (2008.04) USPC - 370/388 According to International Patent Classification (IPC) or to both national classification and IPC</p>																				
<p>B. FIELDS SEARCHED</p> <p>Minimum documentation searched (classification system followed by classification symbols) IPC(8): H04L 12/50 (2008.04) USPC: 370/388</p> <p>Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched USPC: 370/254, 351, 360, 388; 709/220, 223, 227, 228</p> <p>Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) Electronic databases: USPTO WEST (PGPB, USPT, EPAB, JPAB); Google Scholar Search Terms Used: multi-stage or multistage switch or network, multicast or multi-cast network or connections, input or output or middle or penultimate stages, checking or fanning connections, inlet or incoming or outlet or outgoing links or paths et</p>																				
<p>C. DOCUMENTS CONSIDERED TO BE RELEVANT</p> <table border="1"> <thead> <tr> <th>Category*</th> <th>Citation of document, with indication, where appropriate, of the relevant passages</th> <th>Relevant to claim No.</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>US 2006/0165085 A1 (Konda) 27 July 2006 (27.07.2006) (abstract, and para [0009], [0022]-[0036], [0041]-[0051], [0087]-[0106], [0110]-[0117])</td> <td>1-22</td> </tr> <tr> <td>A</td> <td>US 2006/0013207 A1 (McMillen et al.) 19 January 2006 (19.01.2006)</td> <td>1-22</td> </tr> <tr> <td>A</td> <td>US 2005/0105517 A1 (Konda) 19 May 2005 (19.05.2005)</td> <td>1-22</td> </tr> <tr> <td>A</td> <td>US 6,816,487 B1 (Roberts et al.) 09 November 2004 (09.11.2004)</td> <td>1-22</td> </tr> <tr> <td>A</td> <td>US 6,473,428 B1 (Nichols et al.) 29 October 2002 (29.10.2002)</td> <td>1-22</td> </tr> </tbody> </table>			Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.	X	US 2006/0165085 A1 (Konda) 27 July 2006 (27.07.2006) (abstract, and para [0009], [0022]-[0036], [0041]-[0051], [0087]-[0106], [0110]-[0117])	1-22	A	US 2006/0013207 A1 (McMillen et al.) 19 January 2006 (19.01.2006)	1-22	A	US 2005/0105517 A1 (Konda) 19 May 2005 (19.05.2005)	1-22	A	US 6,816,487 B1 (Roberts et al.) 09 November 2004 (09.11.2004)	1-22	A	US 6,473,428 B1 (Nichols et al.) 29 October 2002 (29.10.2002)	1-22
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<p><input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/></p>																				
<p>* Special categories of cited documents:</p> <table border="0"> <tr> <td> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier application or patent but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> </td> <td> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</p> <p>"&" document member of the same patent family</p> </td> </tr> </table>			<p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier application or patent but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p>	<p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</p> <p>"&" document member of the same patent family</p>																
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<p>Date of the actual completion of the international search 11 August 2008 (11.08.2008)</p>		<p>Date of mailing of the international search report 15 AUG 2008</p>																		
<p>Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201</p>		<p>Authorized officer: Lee W. Young</p> <p>PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774</p>																		

Form PCT/ISA/210 (second sheet) (April 2007)