US008363649B2

(12) **United States Patent**
Konda

(10) **Patent No.: US 8,363,649 B2**
(45) **Date of Patent: *Jan. 29, 2013**

(54) **FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS**

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(73) Assignee: **Konda Technologies Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 297 days.

This patent is subject to a terminal disclaimer.

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(86) PCT No.: **PCT/US2008/064604**

§ 371 (c)(1), (2), (4) Date: **May 31, 2010**

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PCT Pub. Date: **Dec. 4, 2008**

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Related U.S. Application Data

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(51) **Int. Cl.**
H04L 12/50 (2006.01)

(52) **U.S. Cl.** **370/388**; 370/390; 370/419; 370/413

(58) **Field of Classification Search** 370/388, 370/389, 395.4, 462
See application file for complete search history.

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Primary Examiner — Dang Ton
Assistant Examiner — Mohamed Kamara

(57) **ABSTRACT**

A generalized multi-link multi-stage network comprising $(2\times\log_d N)-1$ stages is operated in strictly nonblocking manner for unicast, also in rearrangeably nonblocking manner for arbitrary fan-out multicast when $s\geqq 2$, and in strictly nonblocking manner for arbitrary fan-out multicast when $s\geqq 3$, includes an input stage having N/d switches with each of them having d inlet links and s×d outgoing links connecting to second stage switches, an output stage having N/d switches with each of them having d outlet links and s×d incoming links connecting from switches in the penultimate stage. The network also has $(2\times\log_d N)-3$ middle stages with each middle stage having N/d switches, and each switch in the middle stage has s×d incoming links connecting from the switches in its immediate preceding stage, and s×d outgoing links connecting to the switches in its immediate succeeding stage. Also each multicast connection is set up by use of at most two outgoing links from the input stage switch.

22 Claims, 125 Drawing Sheets

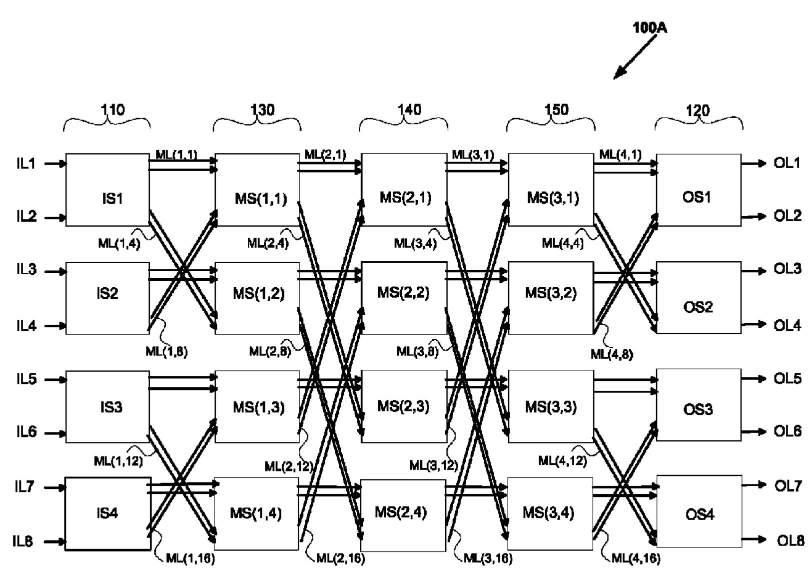

FIG. 1A

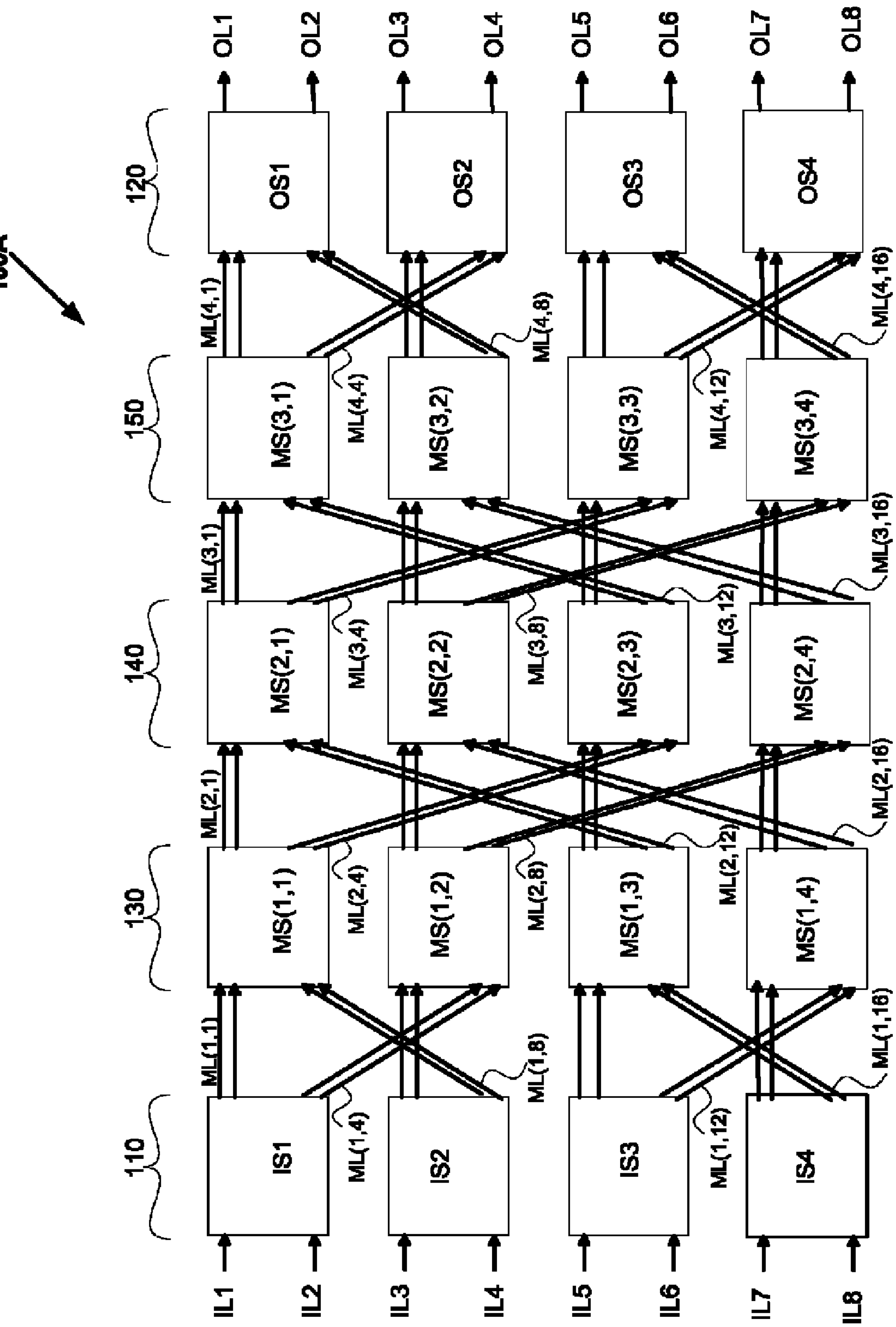
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FIG. 1B

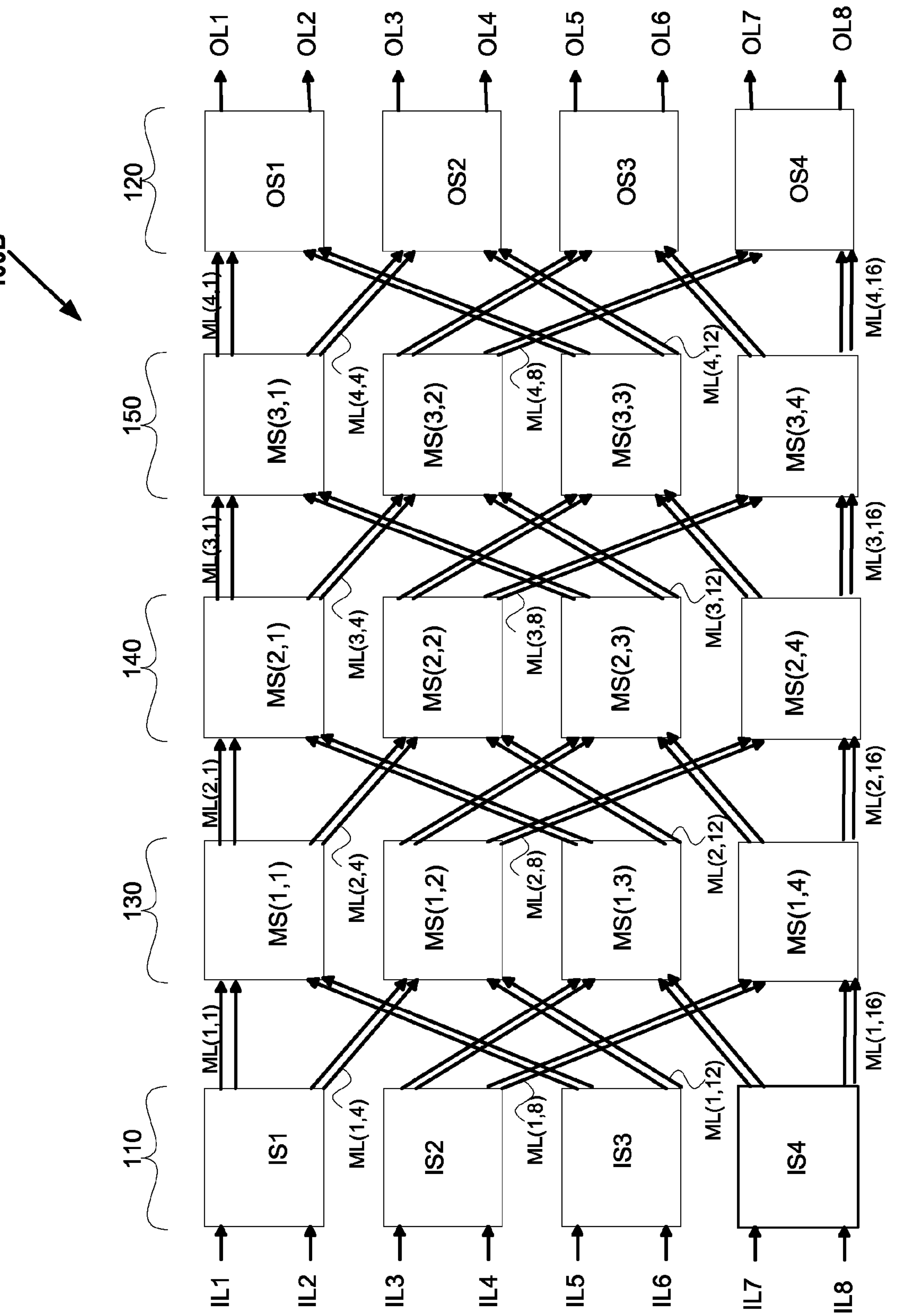
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FIG. 1C

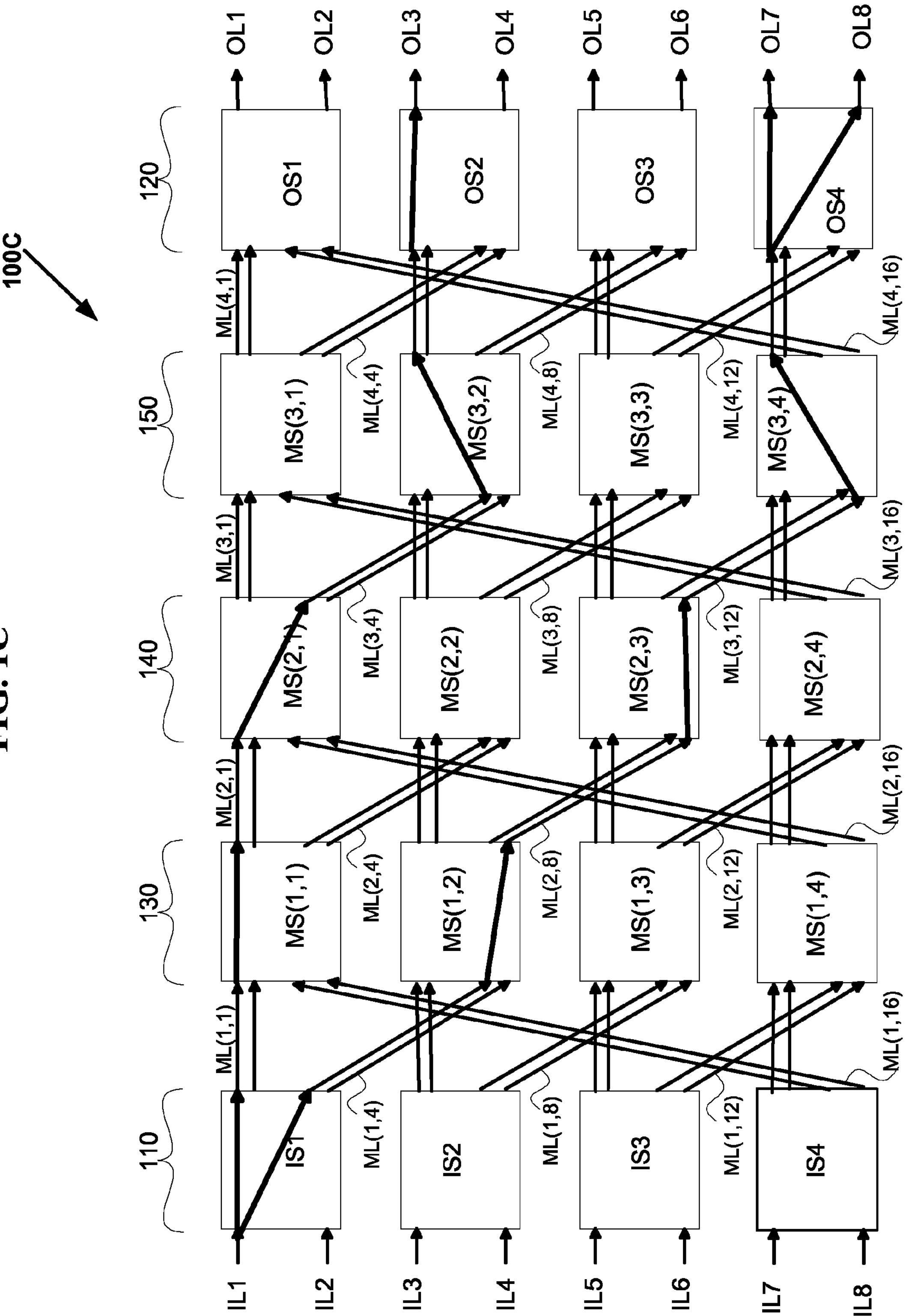
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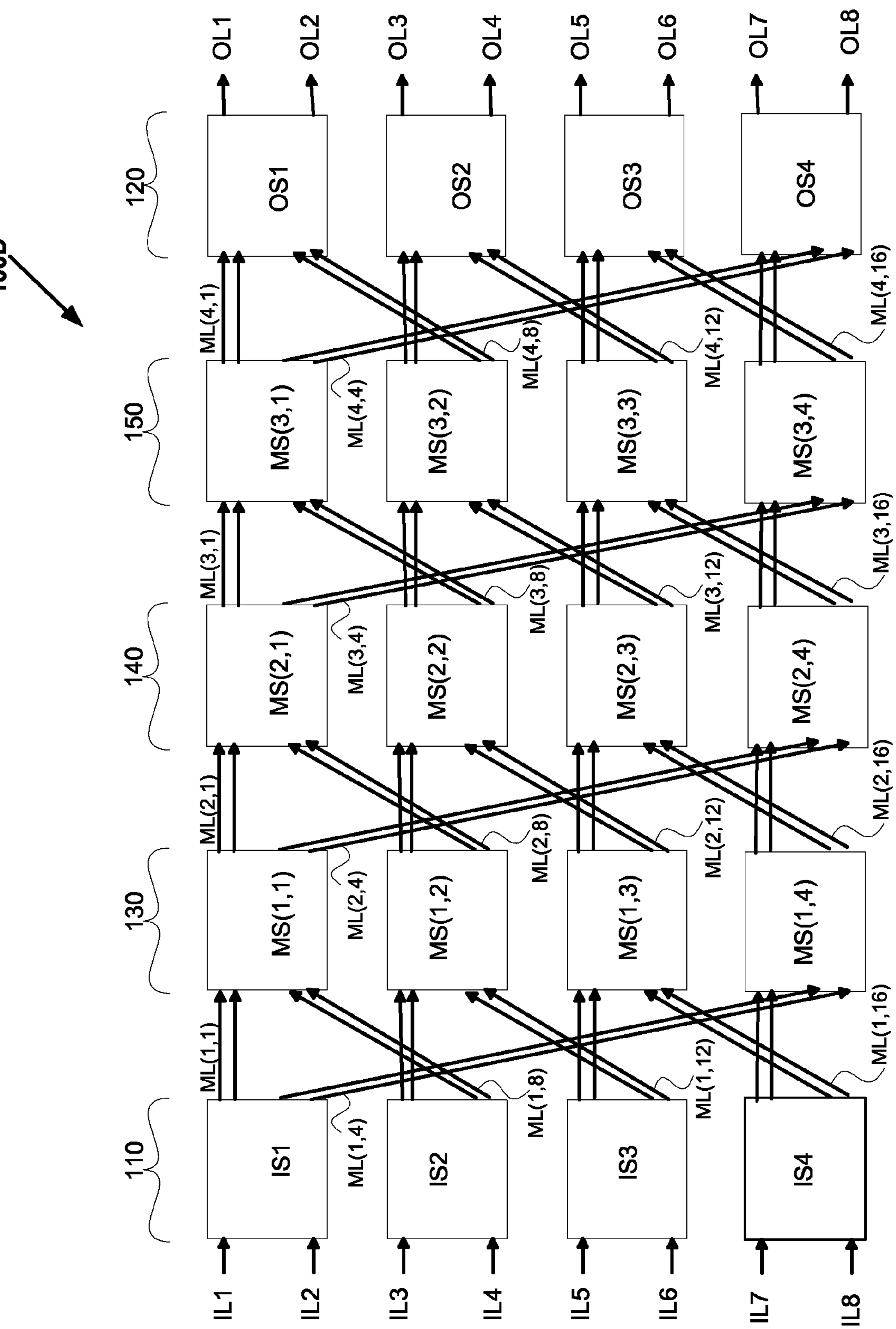
FIG. 1D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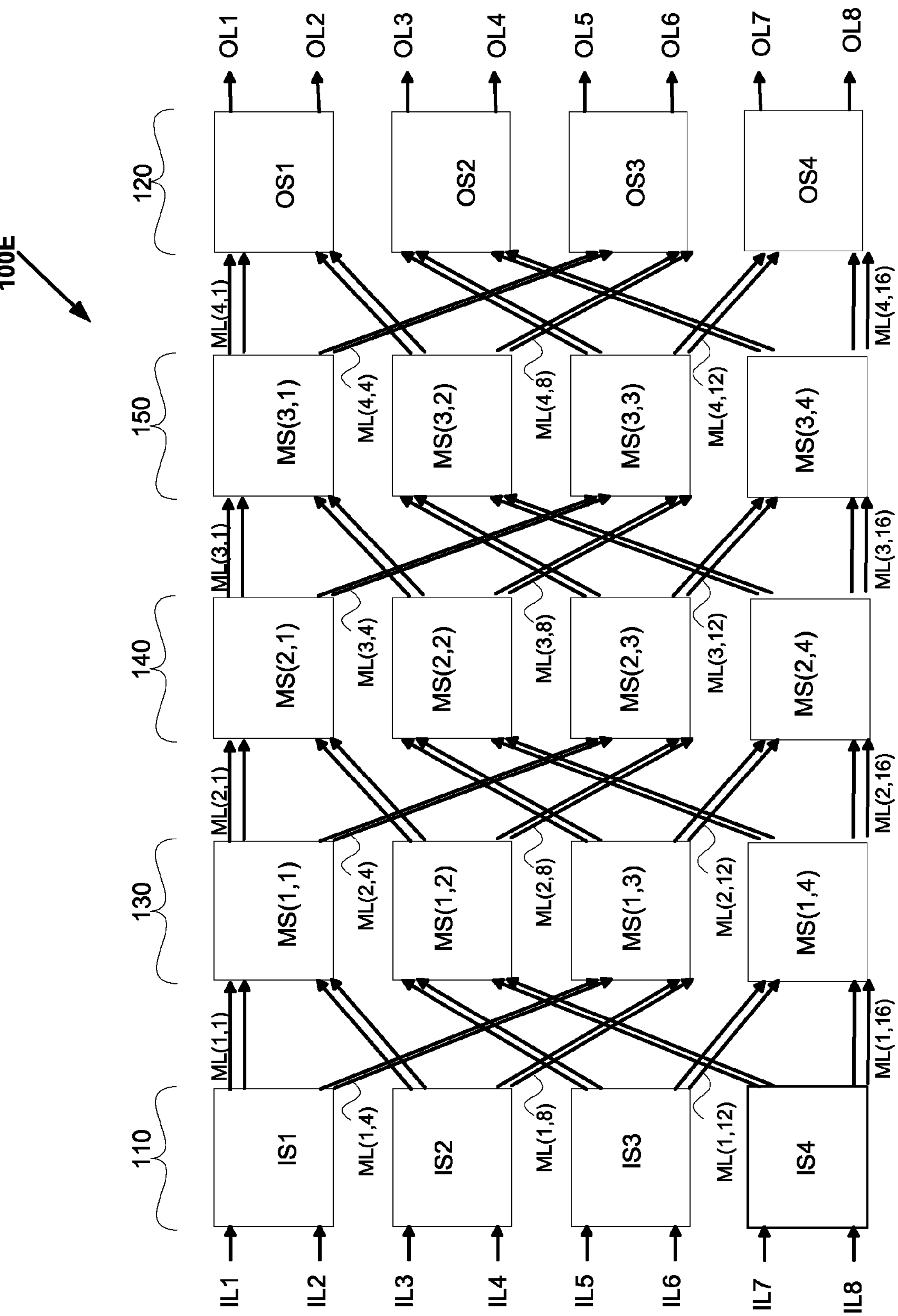
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FIG. 1E

FIG. 1F

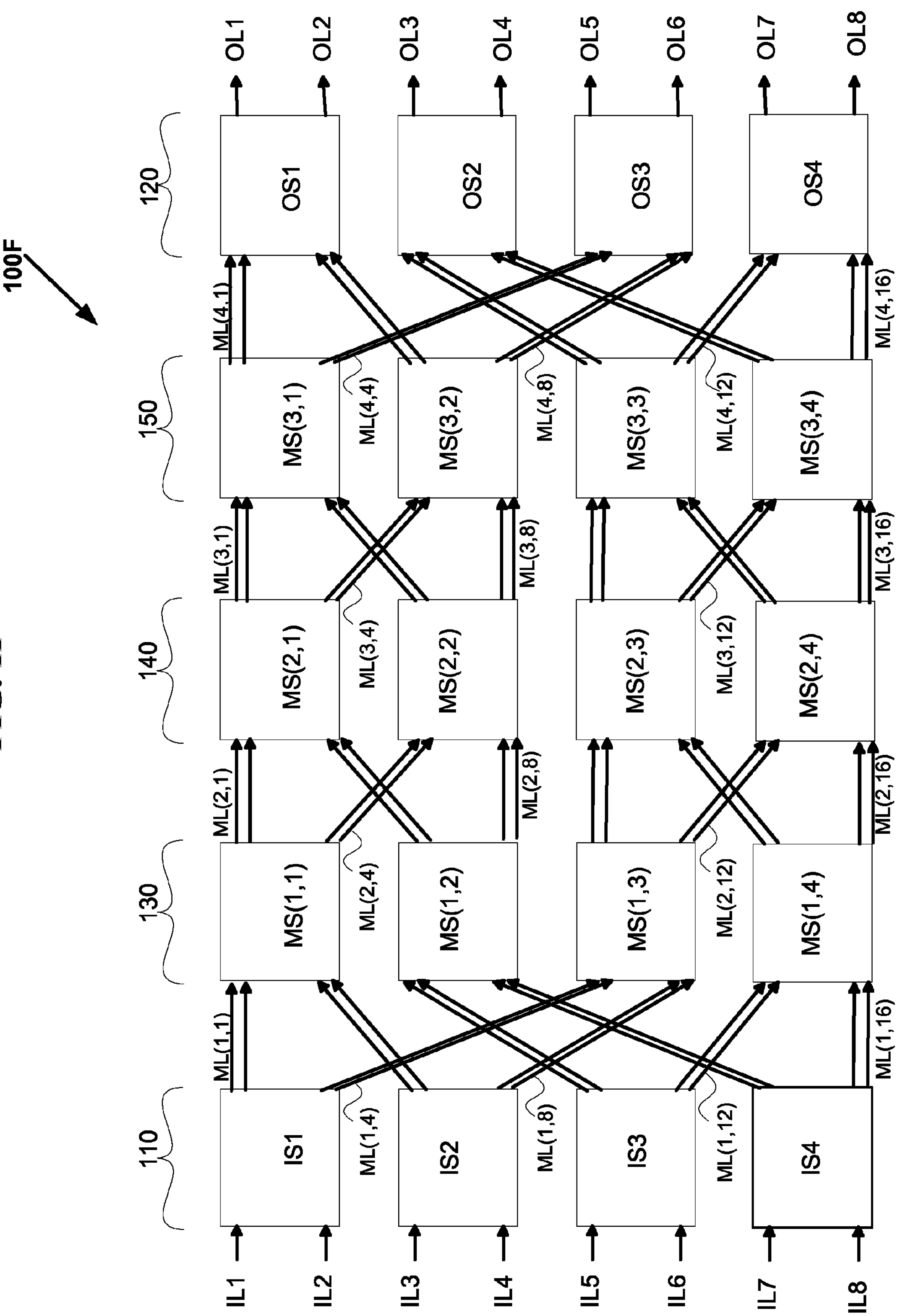
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FIG. 1G

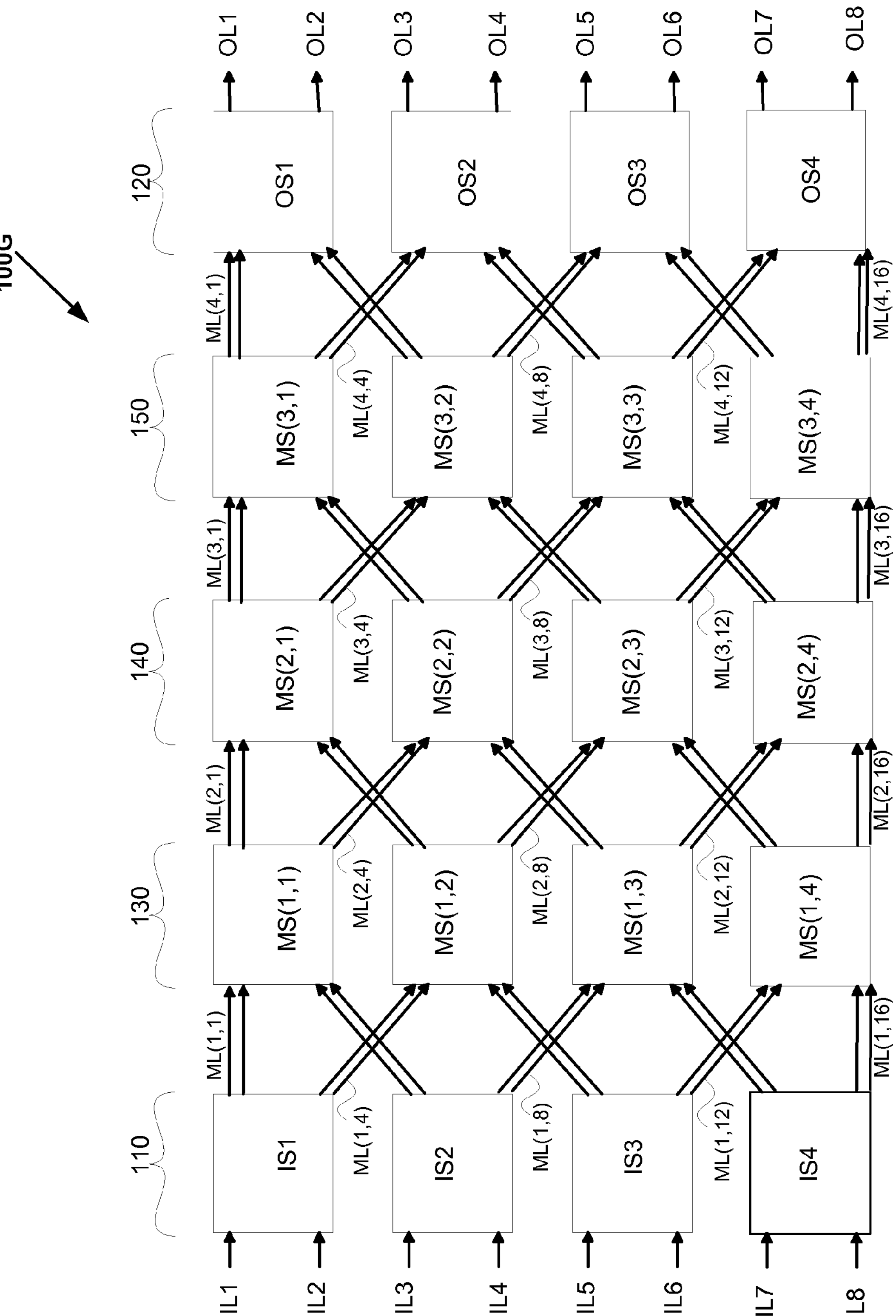
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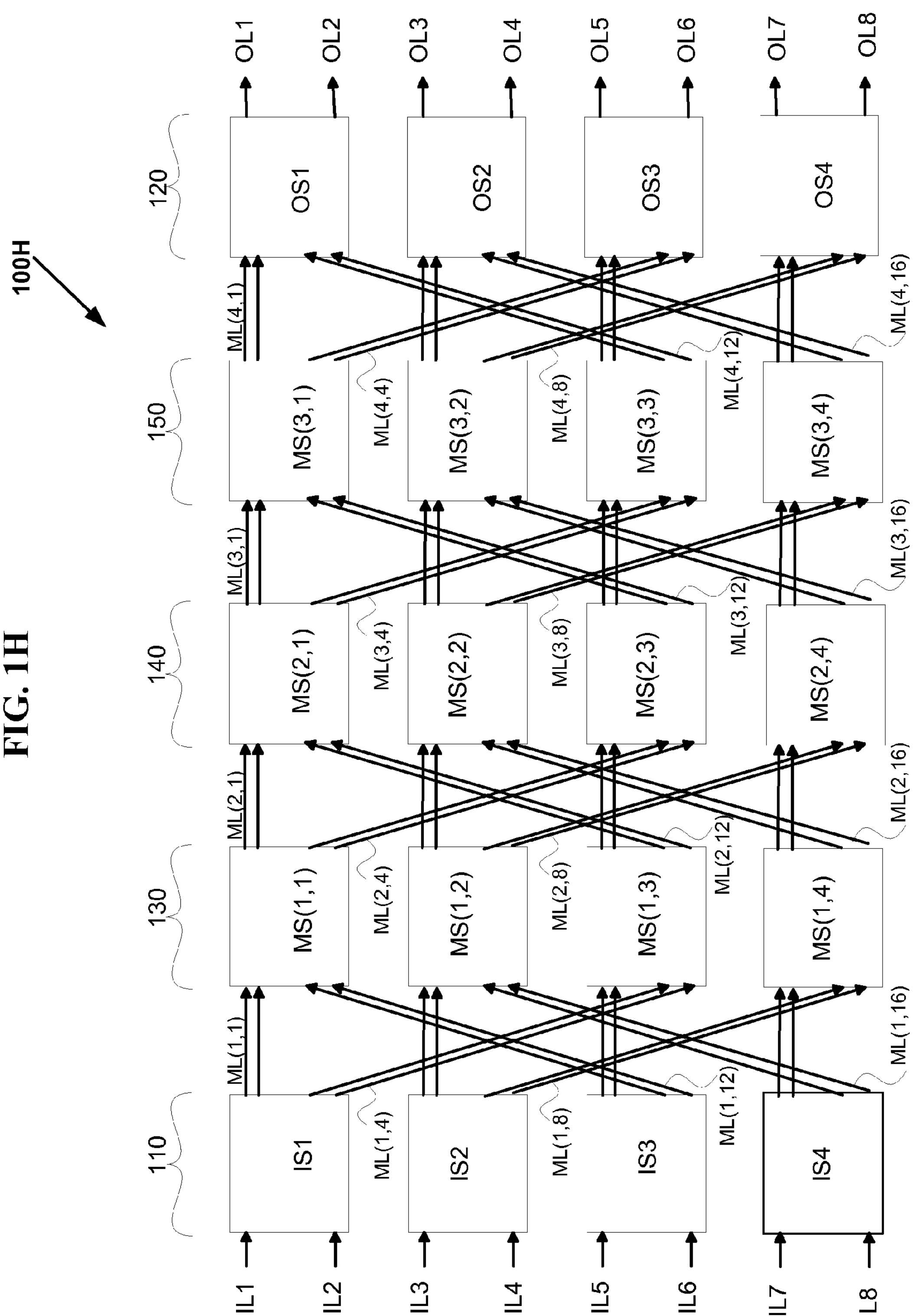
FIG. 1H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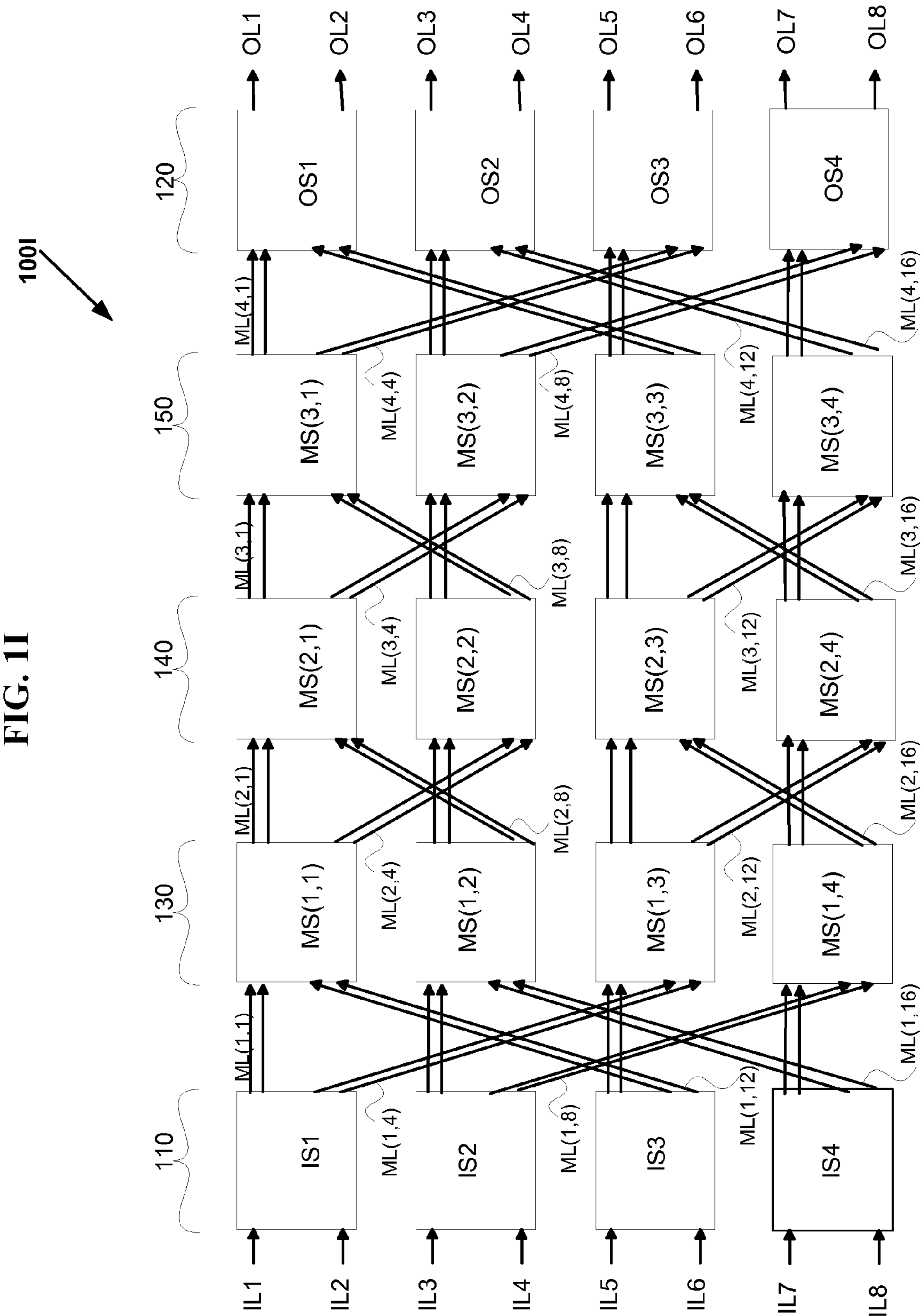
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FIG. 1I

FIG. 1J

100J

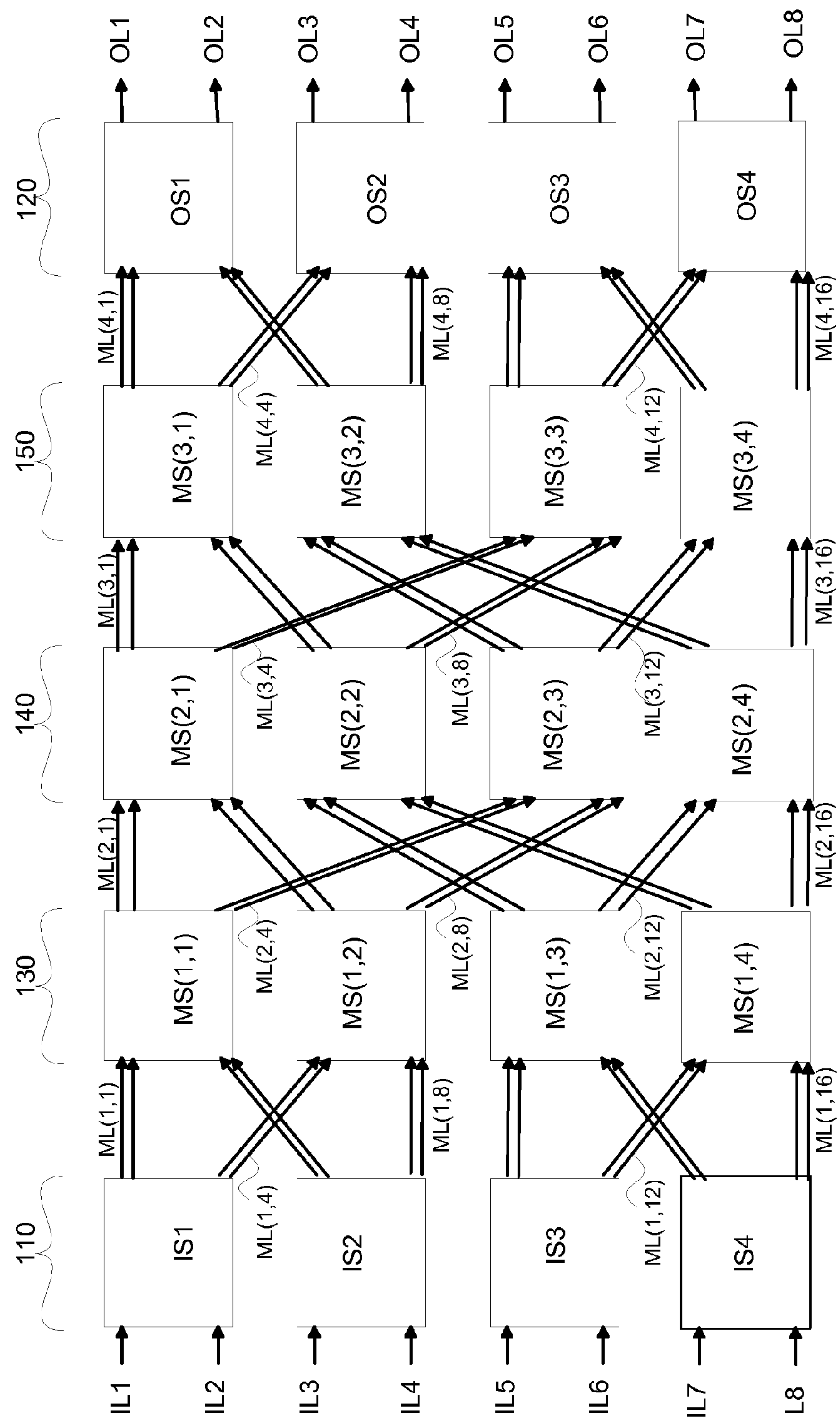
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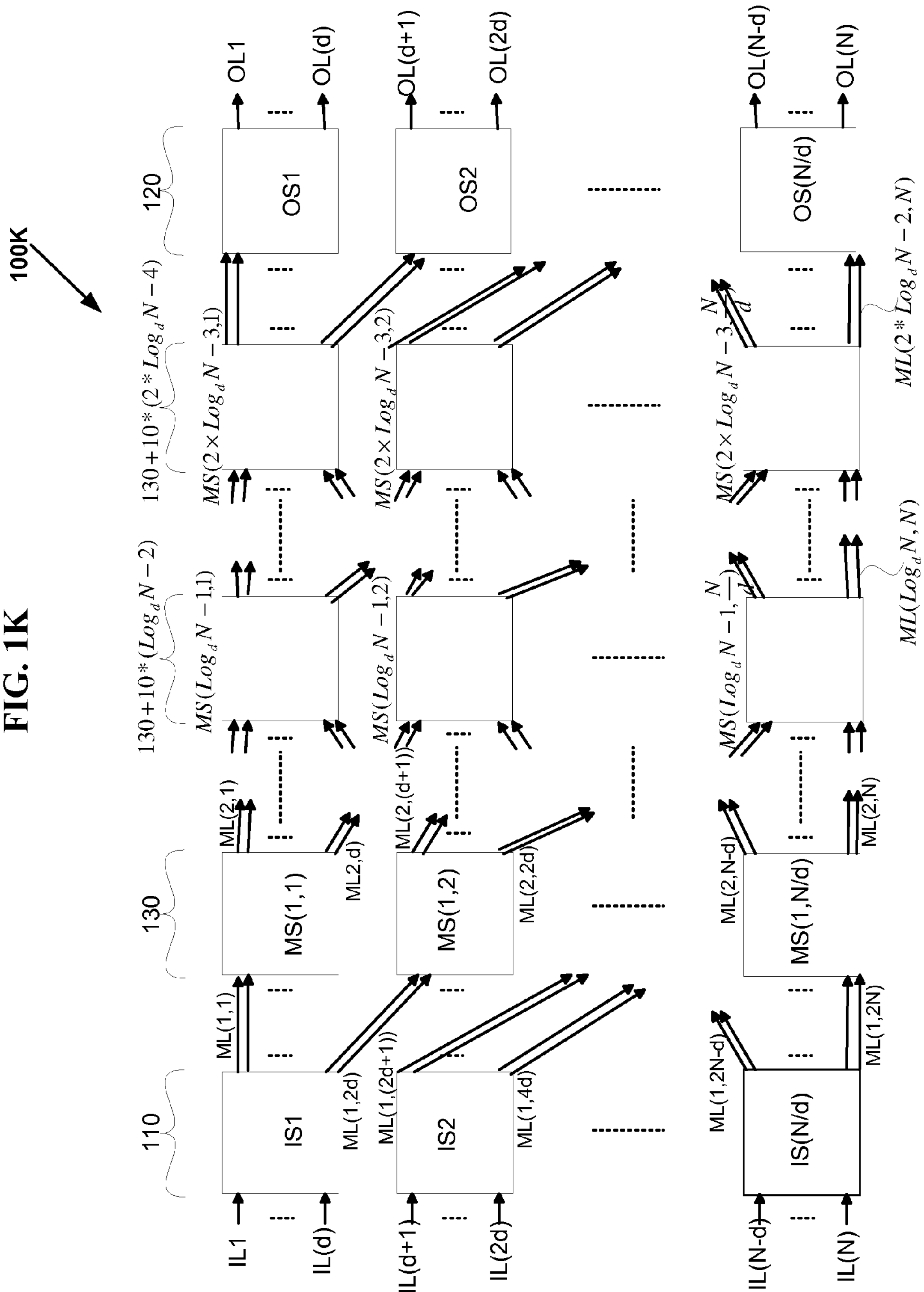
FIG. 1K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120
130
$130+10*(Log_d N-2)$
$130+10*(2*Log_d N-4)$
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IL(d+1)
IL(2d)
IL(N-d)
IL(N)
IS1
IS2
IS(N/d)
ML(1,1)
ML(1,2d)
ML(1,(2d+1))
ML(1,4d)
ML(1,2N-d)
ML(1,2N)
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MS(1,2)
MS(1,N/d)
ML(2,1)
ML2,d)
ML(2,(d+1))
ML(2,2d)
ML(2,N-d)
ML(2,N)
$MS(Log_d N-1,1)$
$MS(Log_d N-1,2)$
$MS(Log_d N-1,\frac{N}{d})$
$ML(Log_d N,N)$
$MS(2\times Log_d N-3,1)$
$MS(2\times Log_d N-3,2)$
$MS(2\times Log_d N-3,\frac{N}{d})$
$ML(2*Log_d N-2,N)$
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OL(2d)
OL(N-d)
OL(N)

FIG. 1A1

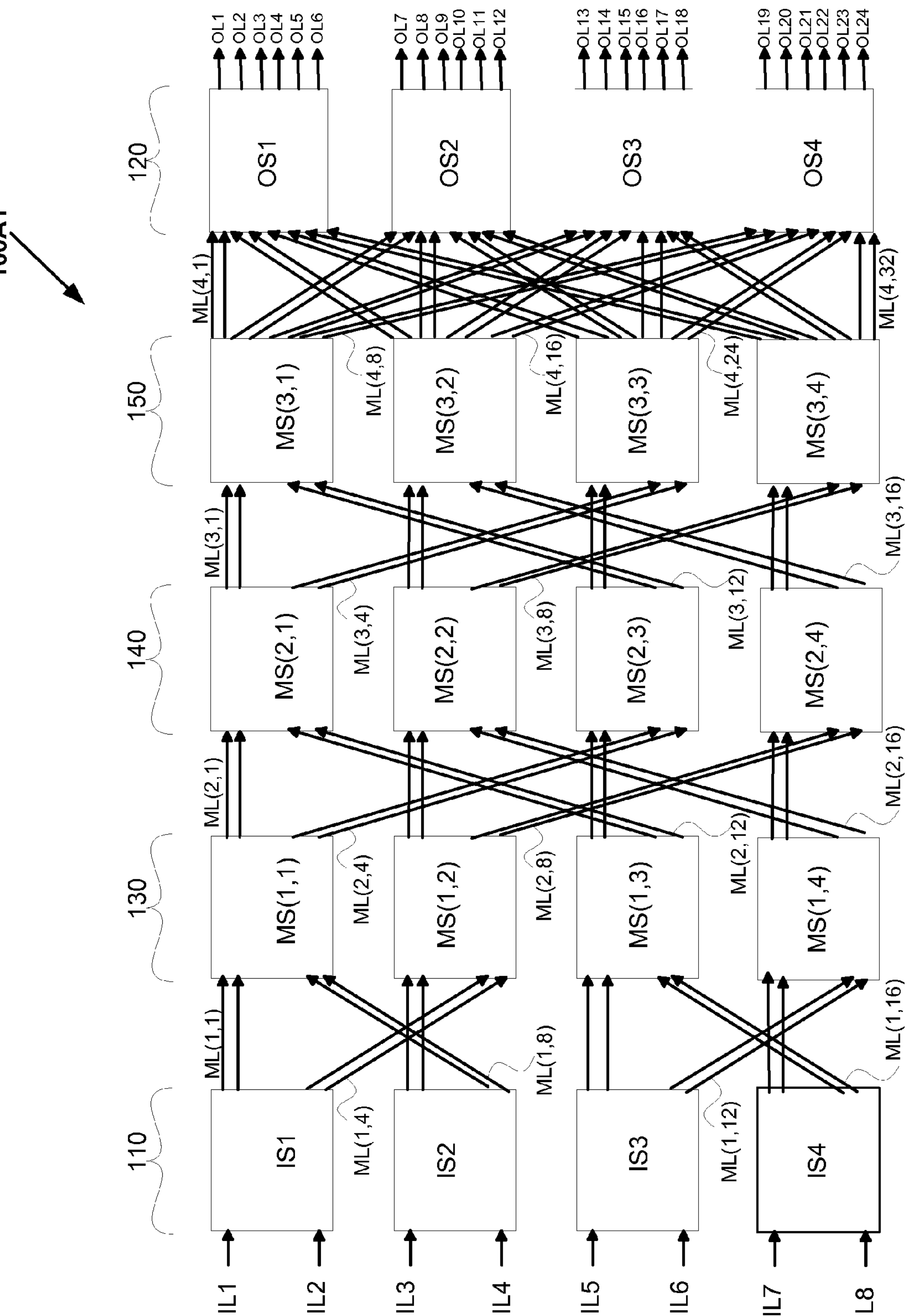
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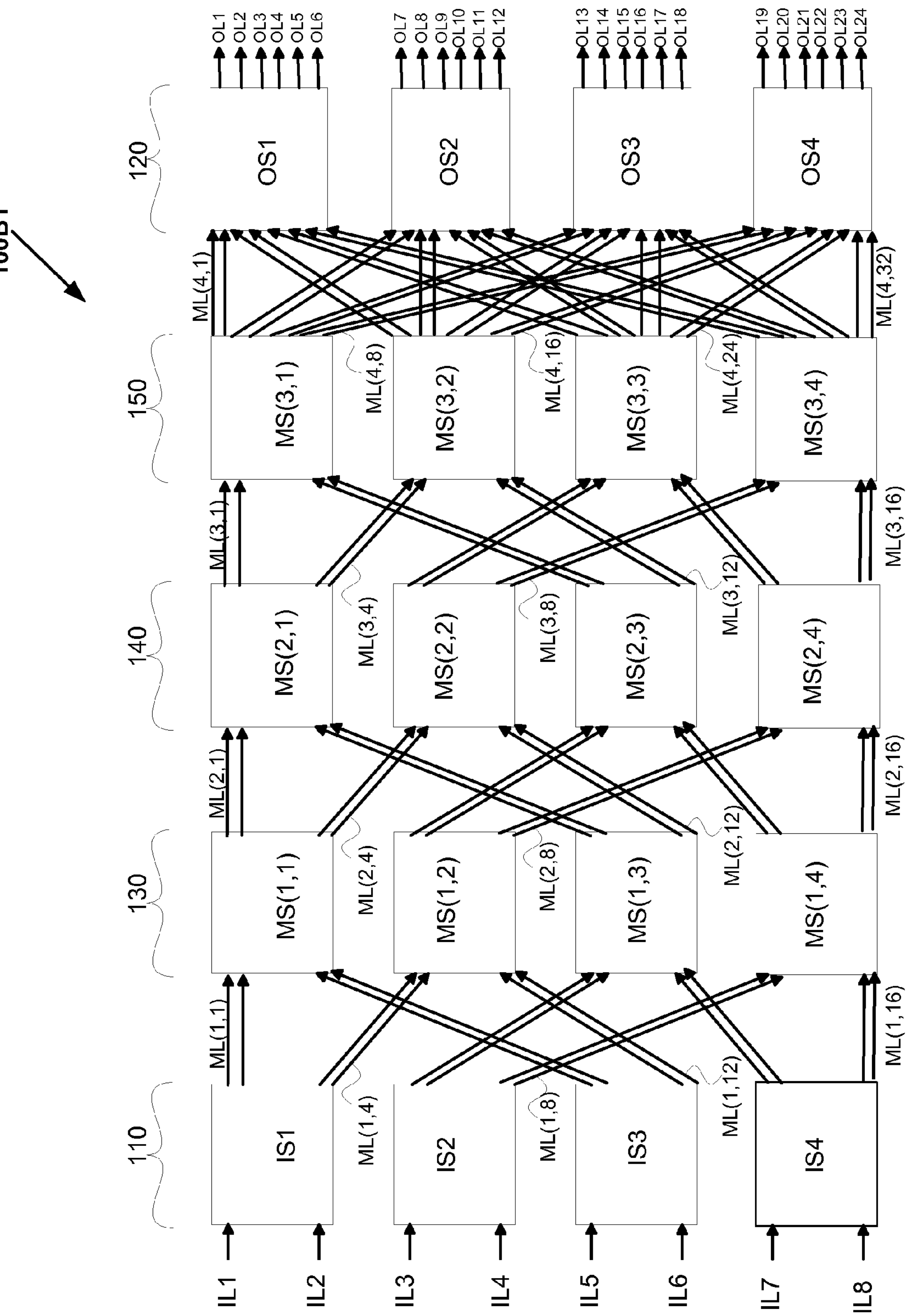
FIG. 1B1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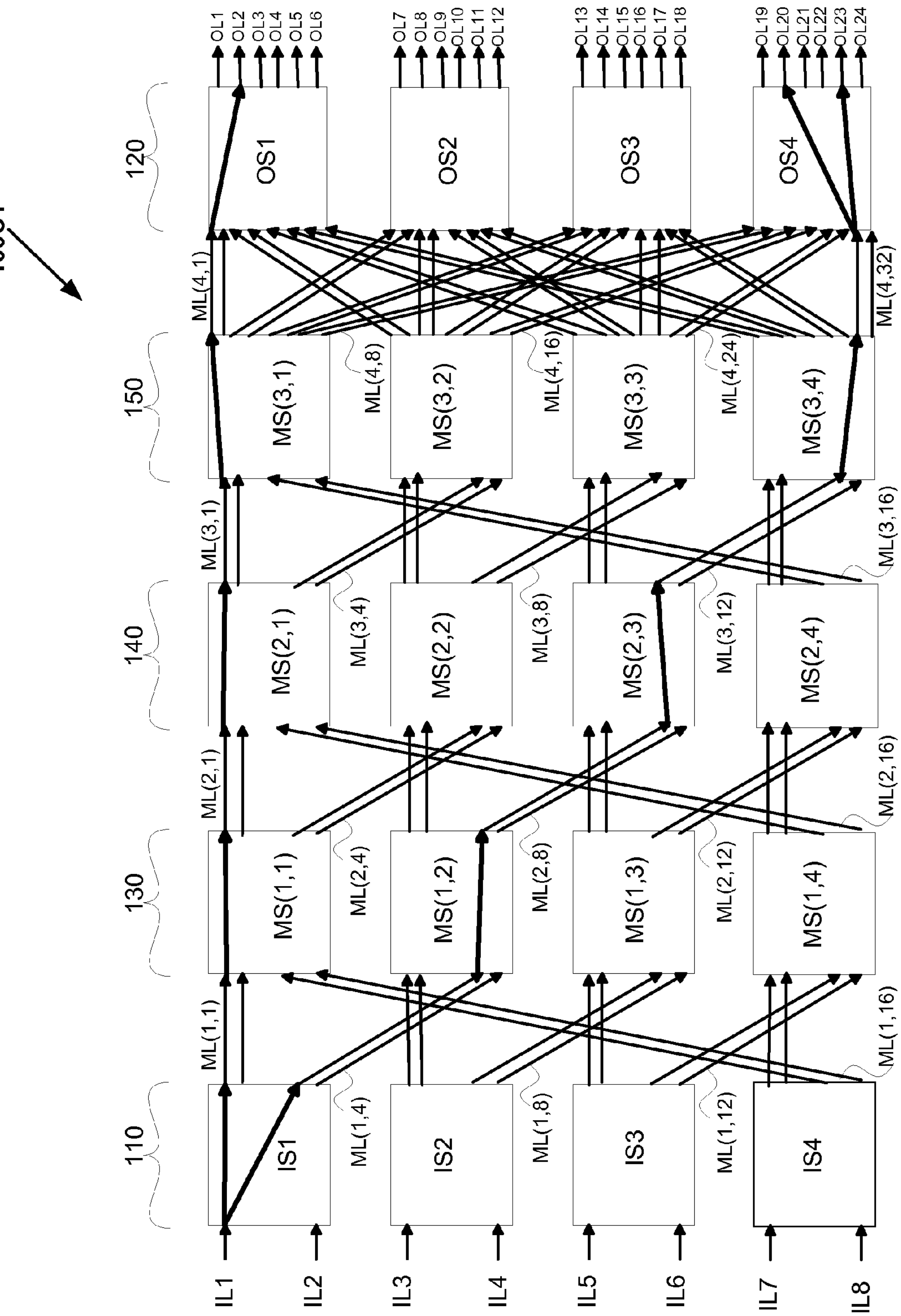
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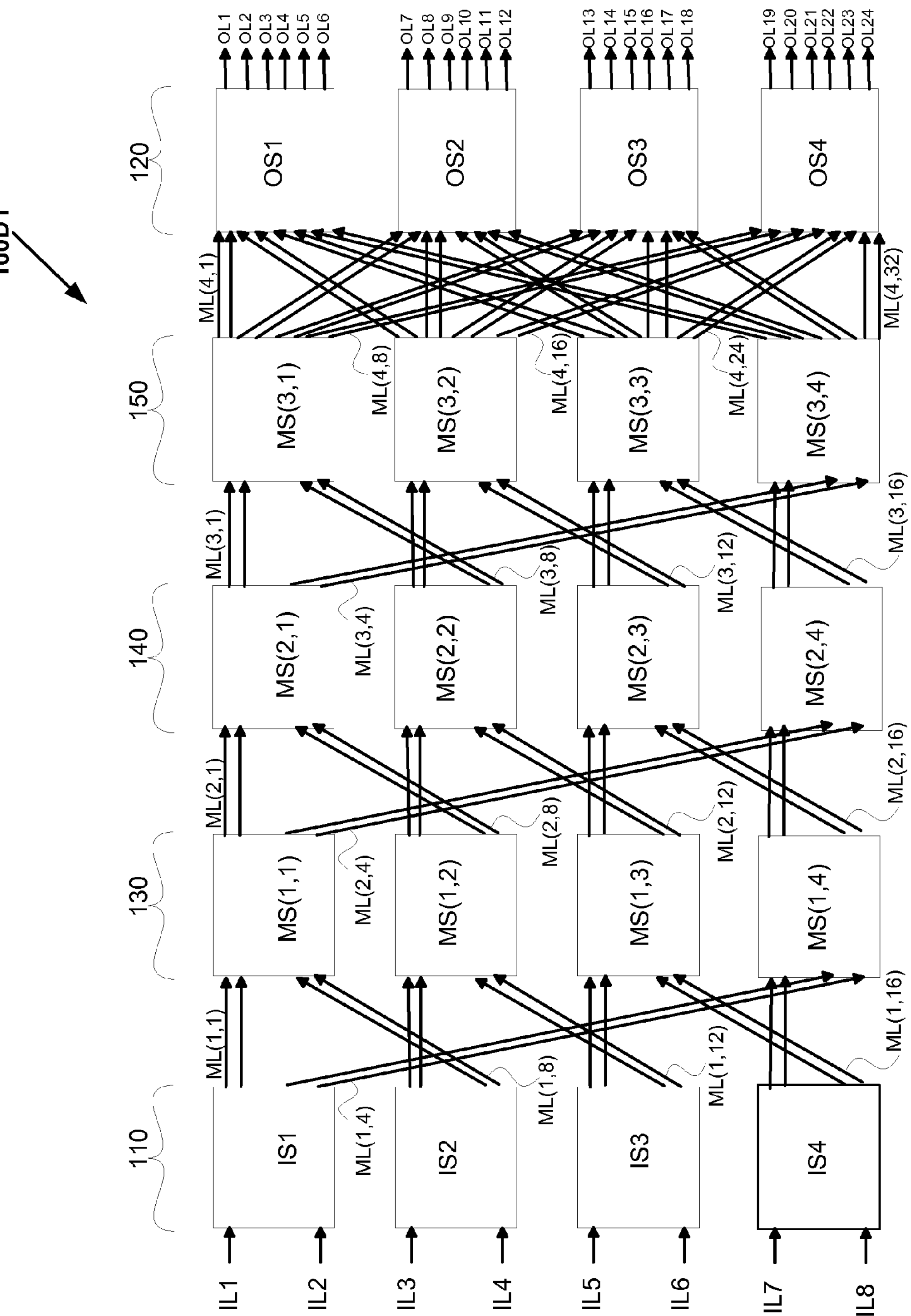
FIG. 1C1

FIG. 1D1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MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
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ML(1,1)
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ML(1,16)
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ML(3,8)
ML(3,12)
ML(3,16)
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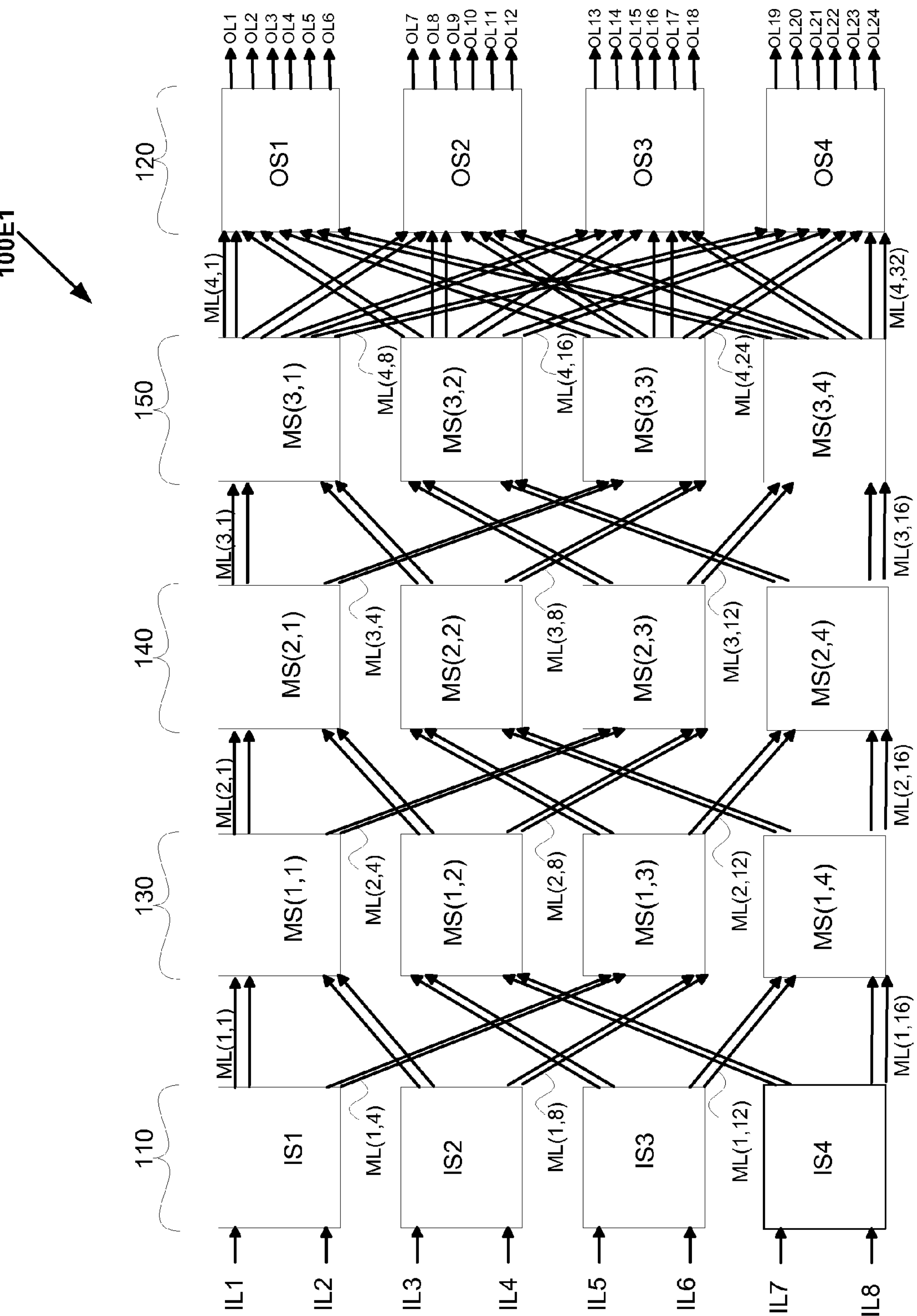
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IS2
IS3
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MS(1,3)
MS(1,4)
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MS(2,2)
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ML(4,1)
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ML(4,24)
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FIG. 1E1

FIG. 1F1

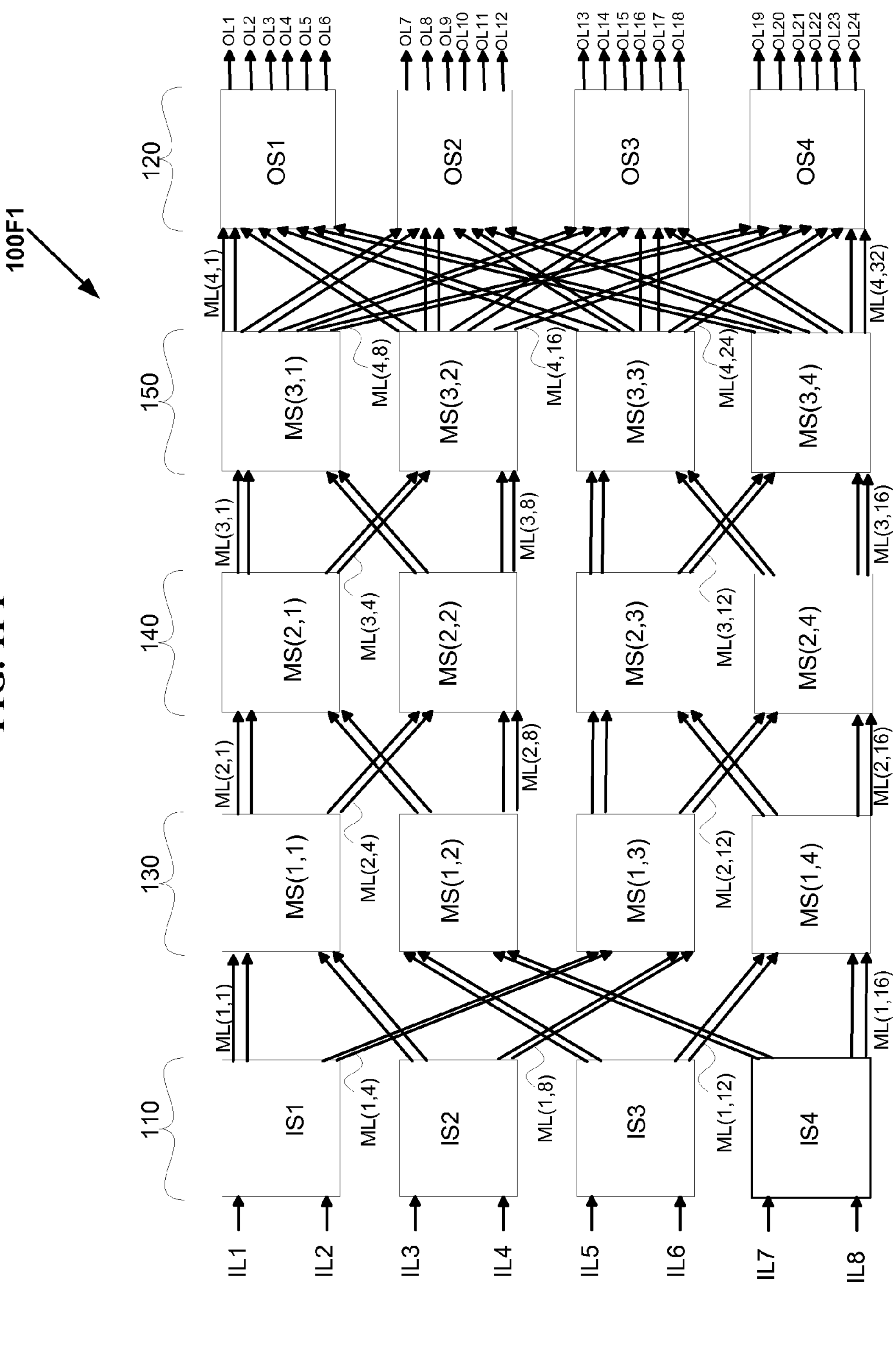
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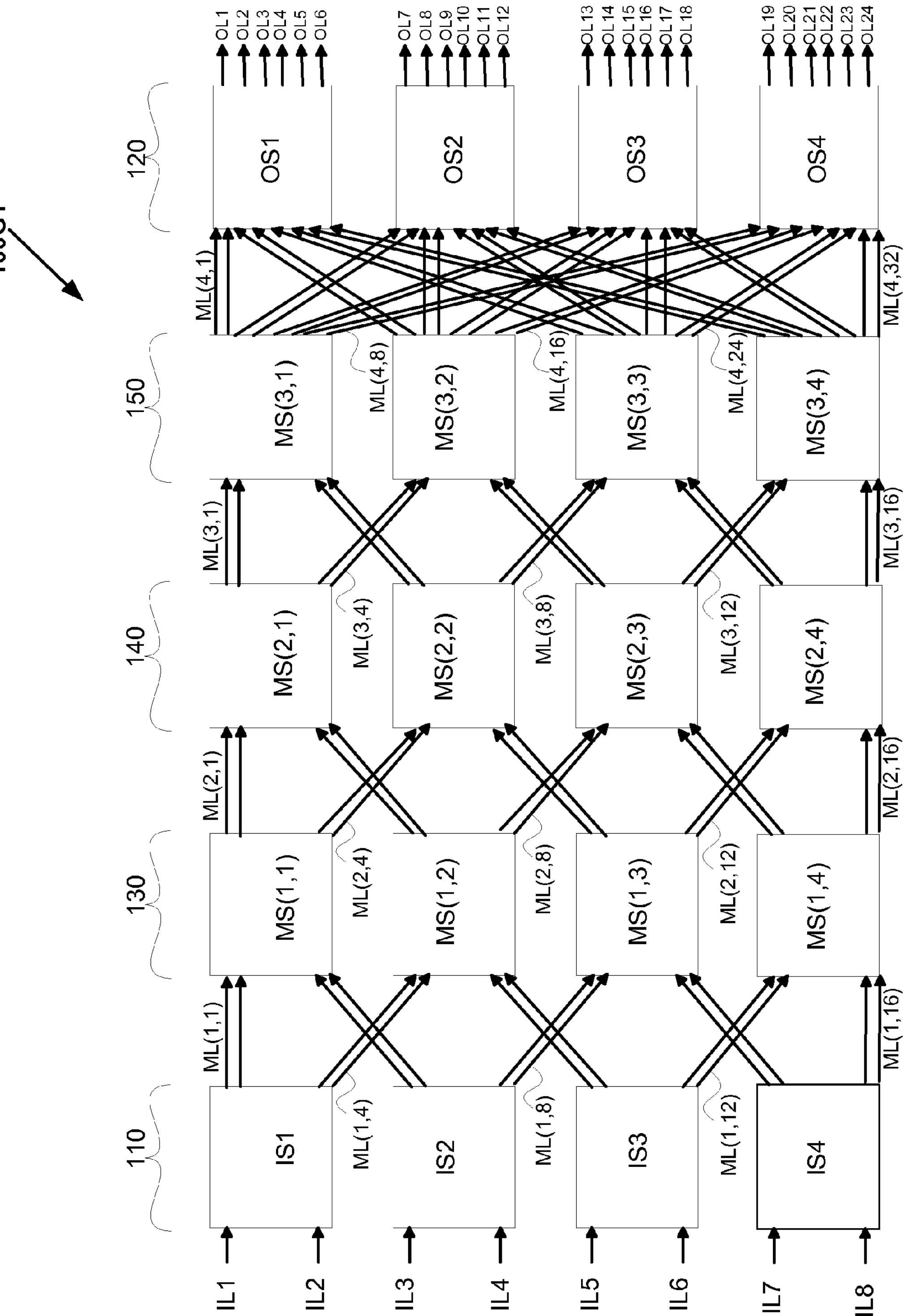
FIG. 1G1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MS(1,4)
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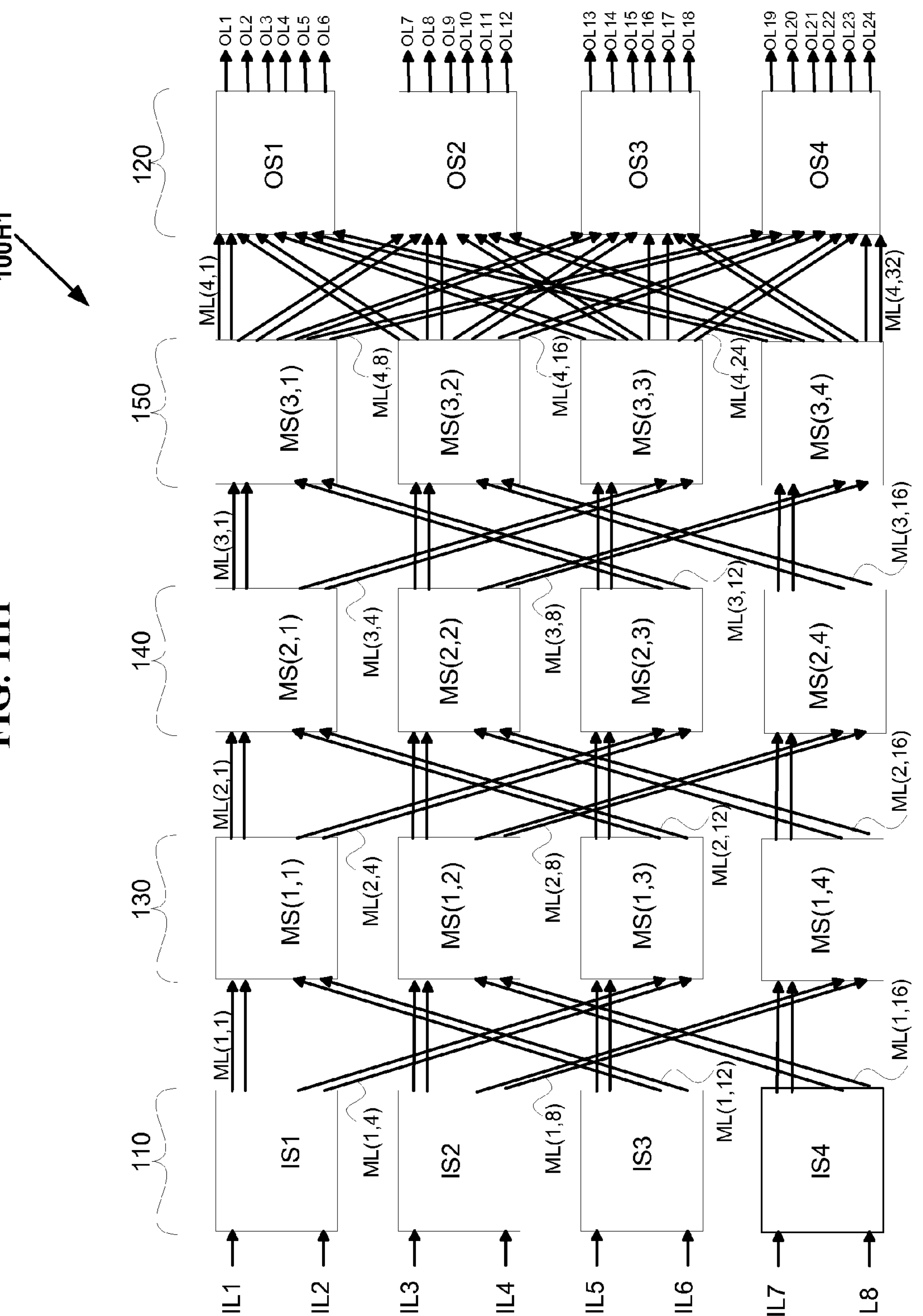
FIG. 1H1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MS(1,4)
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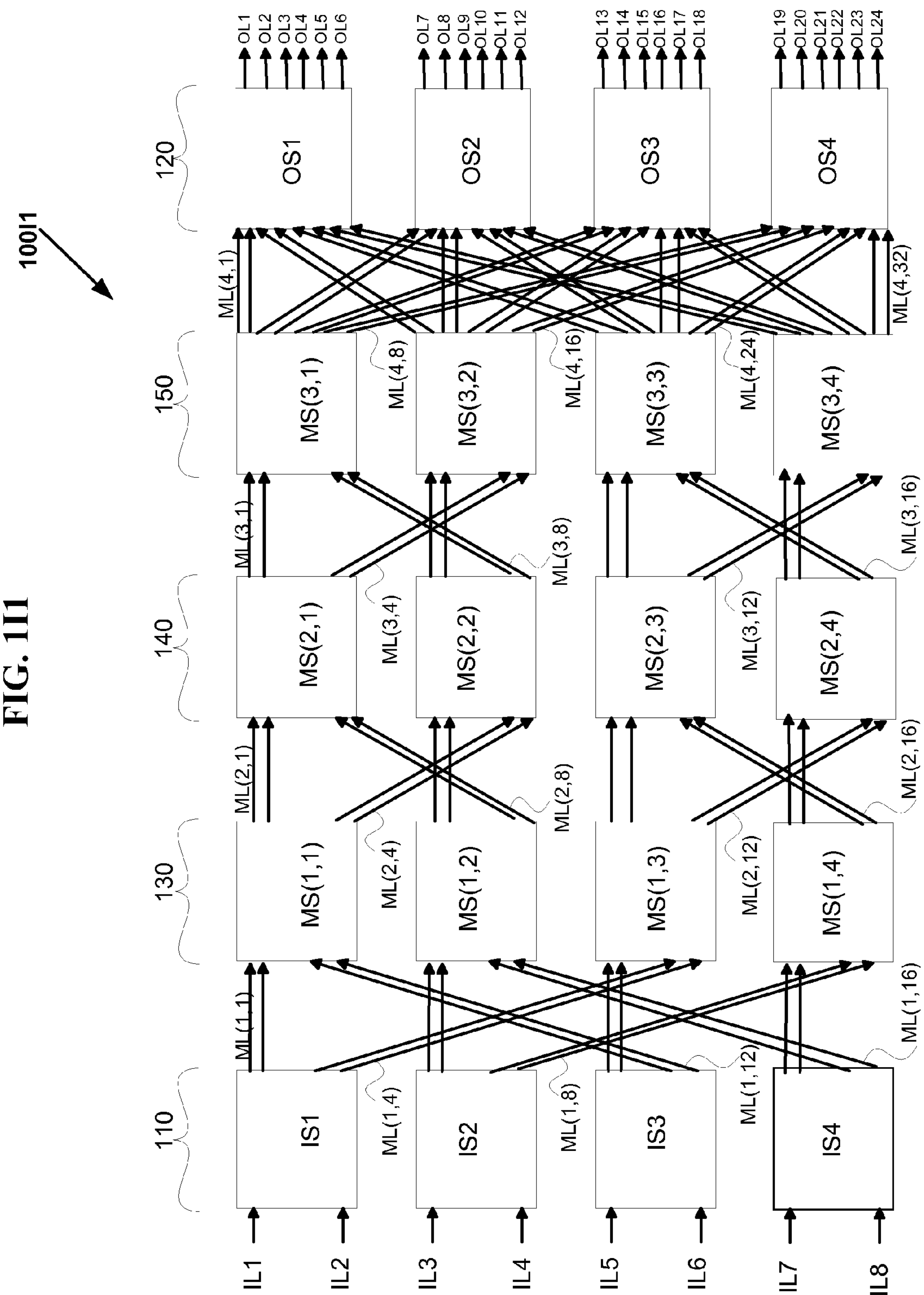
FIG. 1I1


100I1
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MS(1,3)
MS(1,4)
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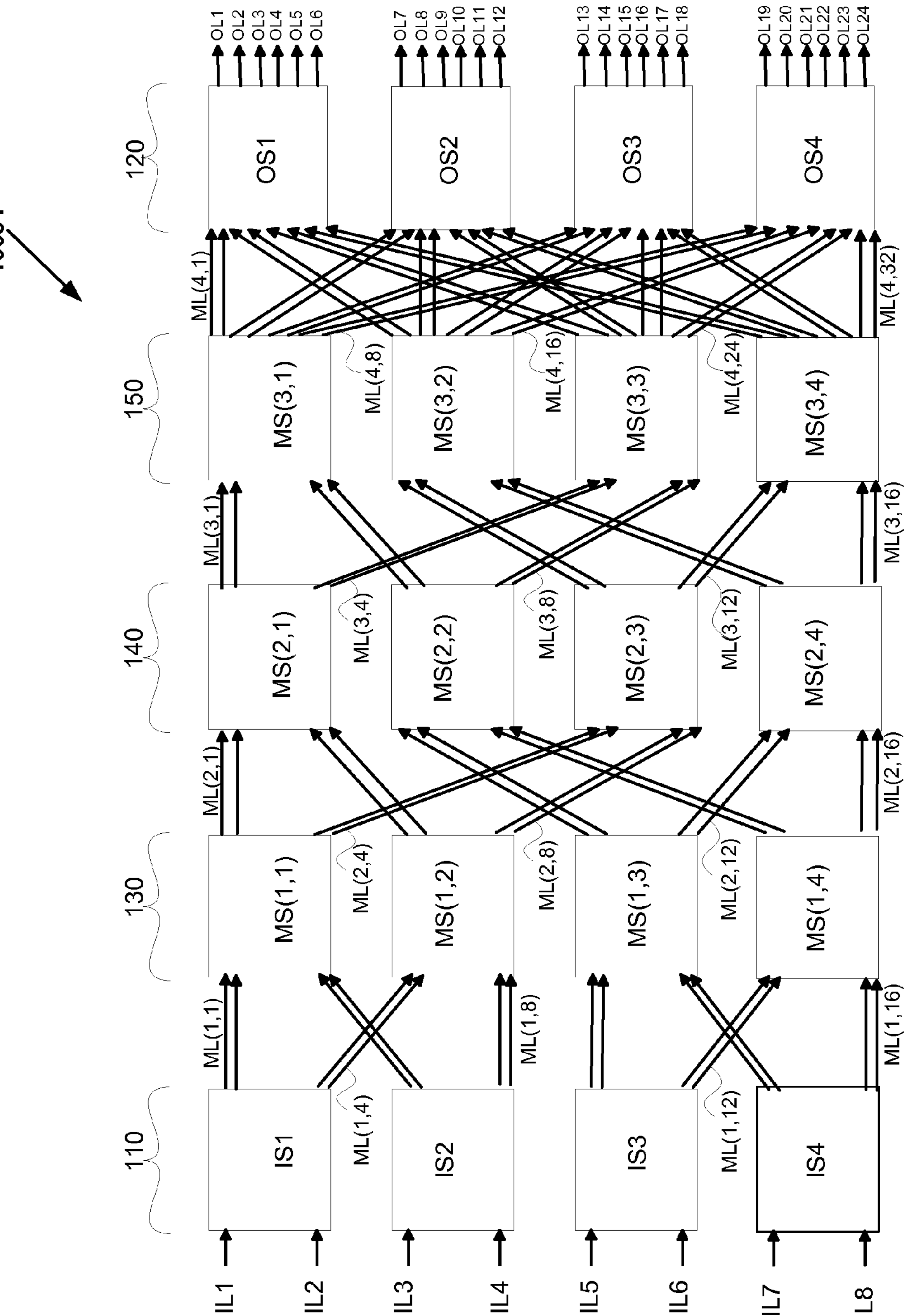
100J1
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140
150
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IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
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ML(1,1)
ML(1,4)
ML(1,8)
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ML(1,16)
ML(2,1)
ML(2,4)
ML(2,8)
ML(2,12)
ML(2,16)
ML(3,1)
ML(3,4)
ML(3,8)
ML(3,12)
ML(3,16)
ML(4,1)
ML(4,8)
ML(4,16)
ML(4,24)
ML(4,32)
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OL11
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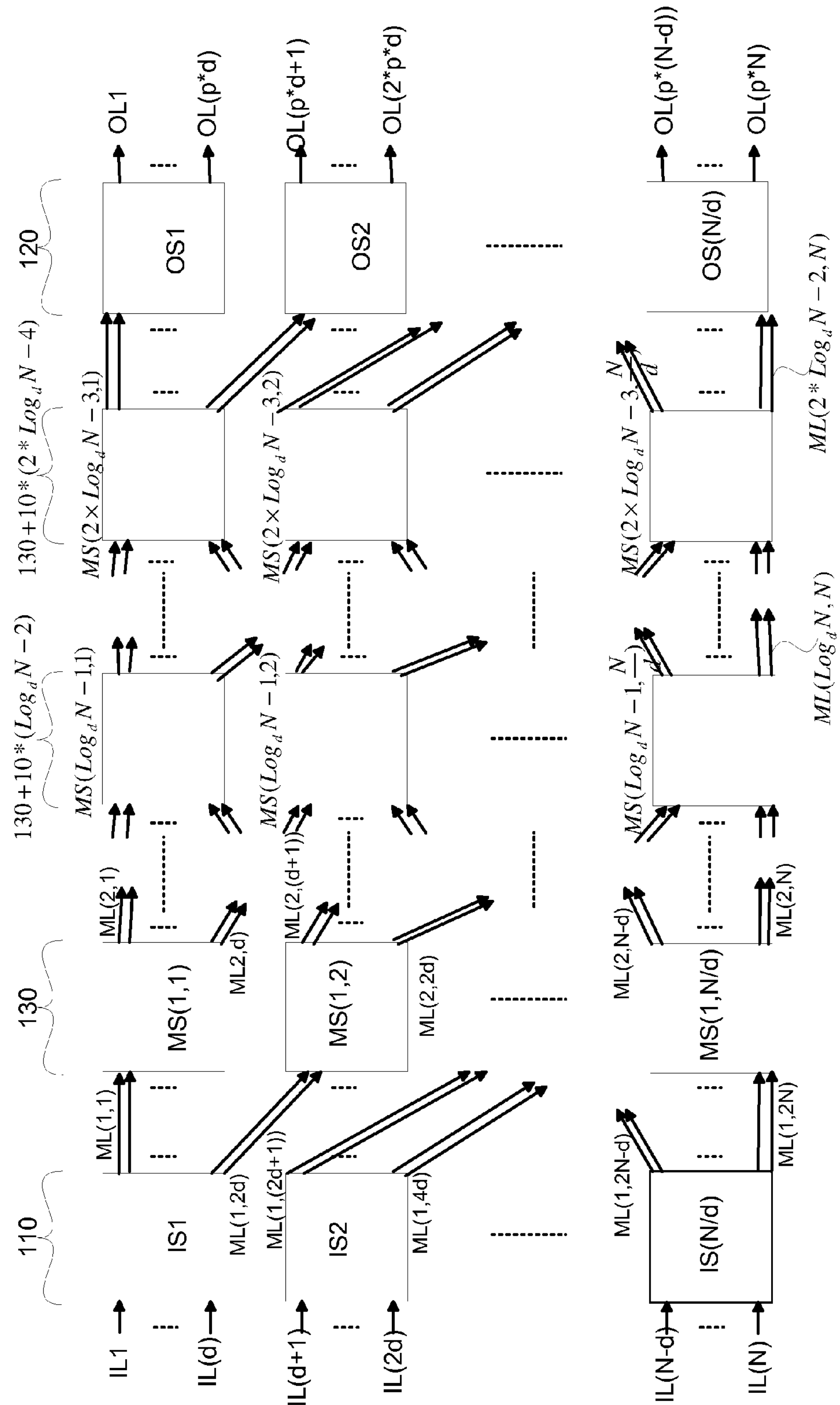
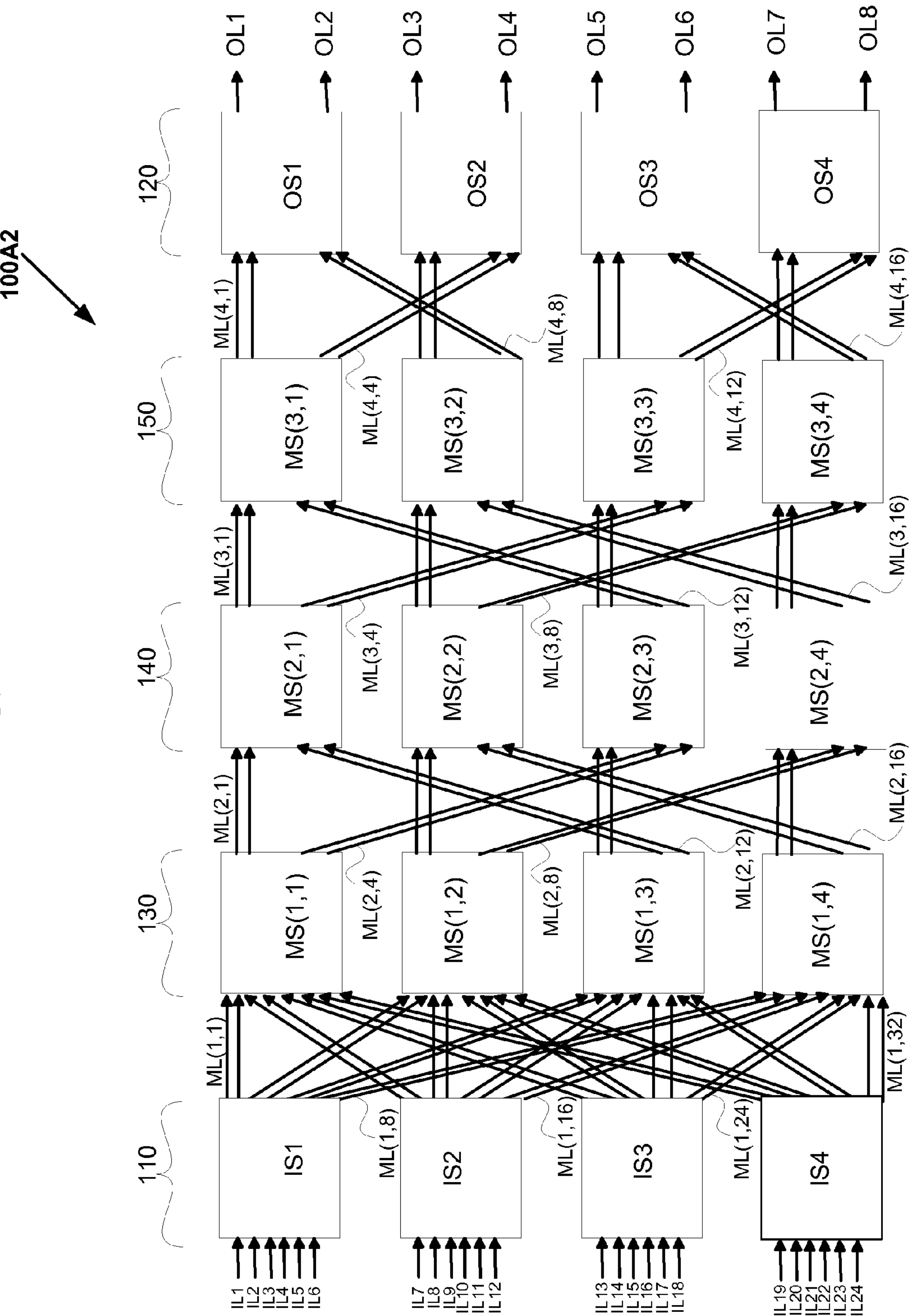
FIG. 1J1

FIG. 1K1



100K1
110
120
130
IS1
IS2
IS(N/d)
MS(1,1)
MS(1,2)
MS(1,N/d)
OS1
OS2
OS(N/d)
IL1
IL(d)
IL(d+1)
IL(2d)
IL(N-d)
IL(N)
OL1
OL(p*d)
OL(p*d+1)
OL(2*p*d)
OL(p*(N-d))
OL(p*N)
ML(1,1)
ML(1,2d)
ML(1,(2d+1))
ML(1,4d)
ML(1,2N-d)
ML(1,2N)
ML(2,1)
ML(2,d)
ML(2,(d+1))
ML(2,2d)
ML(2,N-d)
ML(2,N)

FIG. 1A2


100A2
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120
130
140
150
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IS2
IS3
IS4
MS(1,1)
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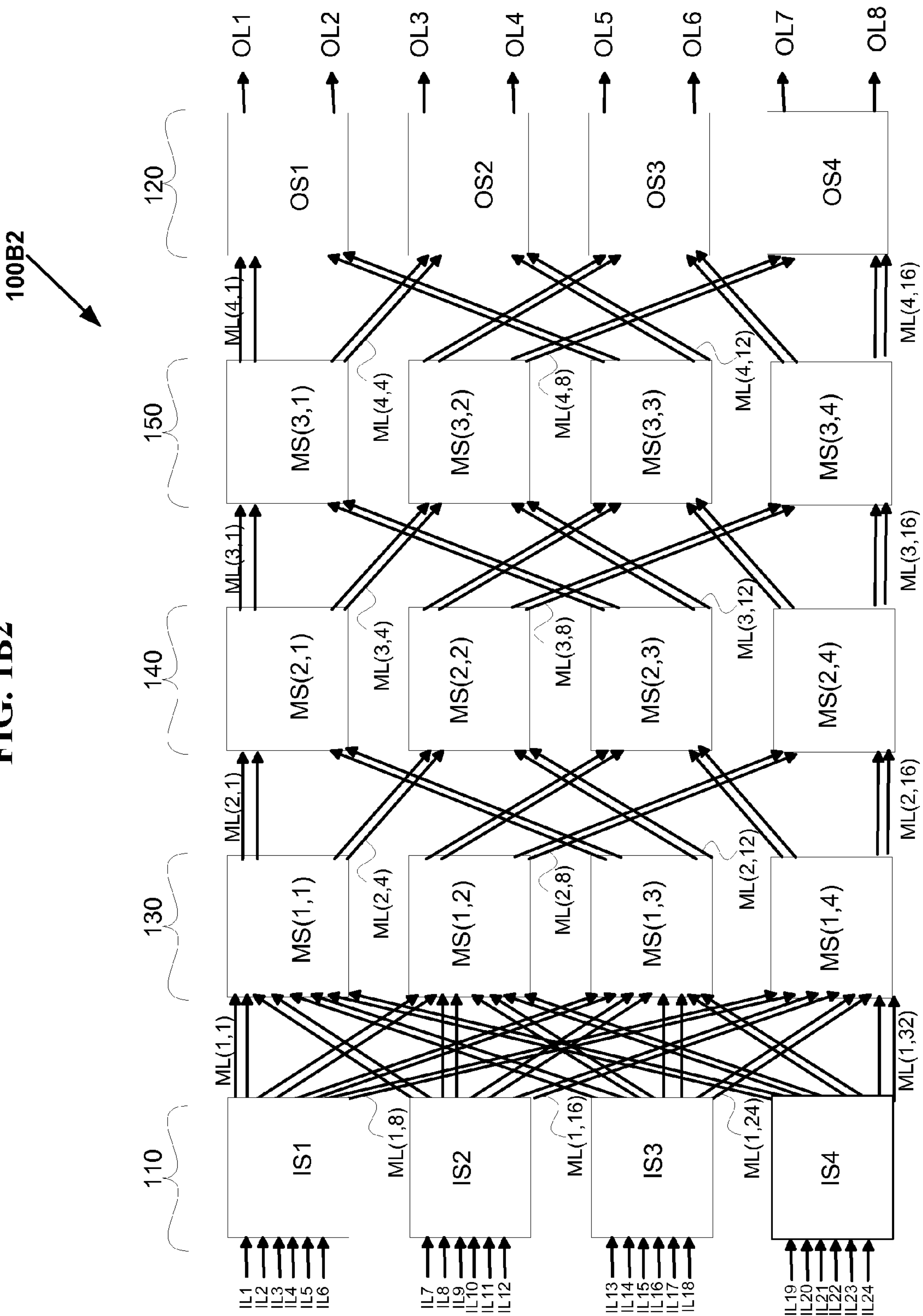
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
OL1 OL2 OL3 OL4 OL5 OL6 OL7 OL8
ML(1,1)
ML(1,8)
ML(1,16)
ML(1,24)
ML(1,32)
ML(2,1)
ML(2,4)
ML(2,8)
ML(2,12)
ML(2,16)
ML(3,1)
ML(3,4)
ML(3,8)
ML(3,12)
ML(3,16)
ML(4,1)
ML(4,4)
ML(4,8)
ML(4,12)
ML(4,16)

FIG. 1B2


100B2
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
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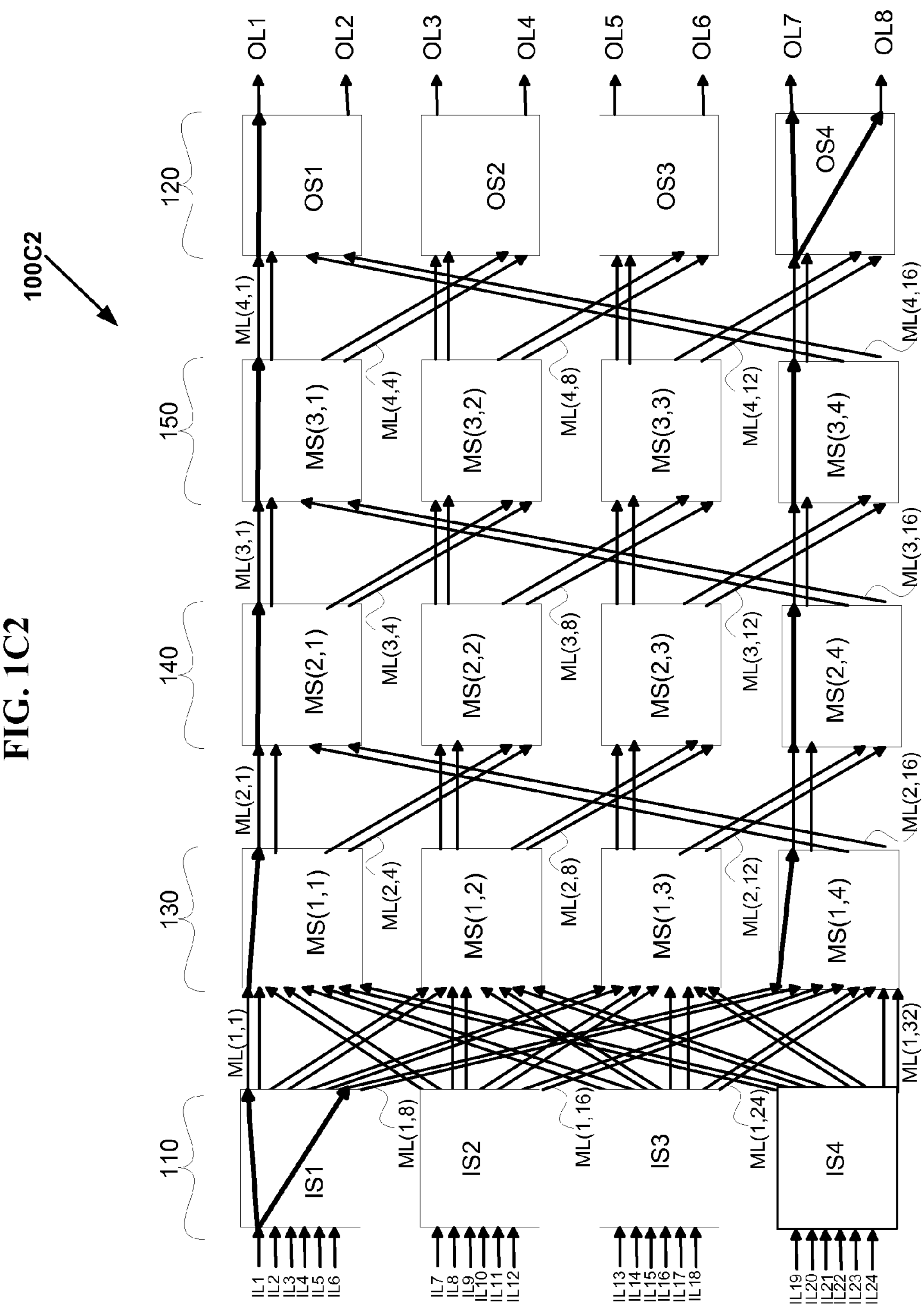
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
ML(1,1)
ML(1,8)
ML(1,16)
ML(1,24)
ML(1,32)
ML(2,1)
ML(2,4)
ML(2,8)
ML(2,12)
ML(2,16)
ML(3,1)
ML(3,4)
ML(3,8)
ML(3,12)
ML(3,16)
ML(4,1)
ML(4,4)
ML(4,8)
ML(4,12)
ML(4,16)
OL1 OL2 OL3 OL4 OL5 OL6 OL7 OL8

FIG. 1C2


100C2
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IS2
IS3
IS4
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MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
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OS4
IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
OL1 OL2 OL3 OL4 OL5 OL6 OL7 OL8
ML(1,1)
ML(1,8)
ML(1,16)
ML(1,24)
ML(1,32)
ML(2,1)
ML(2,4)
ML(2,8)
ML(2,12)
ML(2,16)
ML(3,1)
ML(3,4)
ML(3,8)
ML(3,12)
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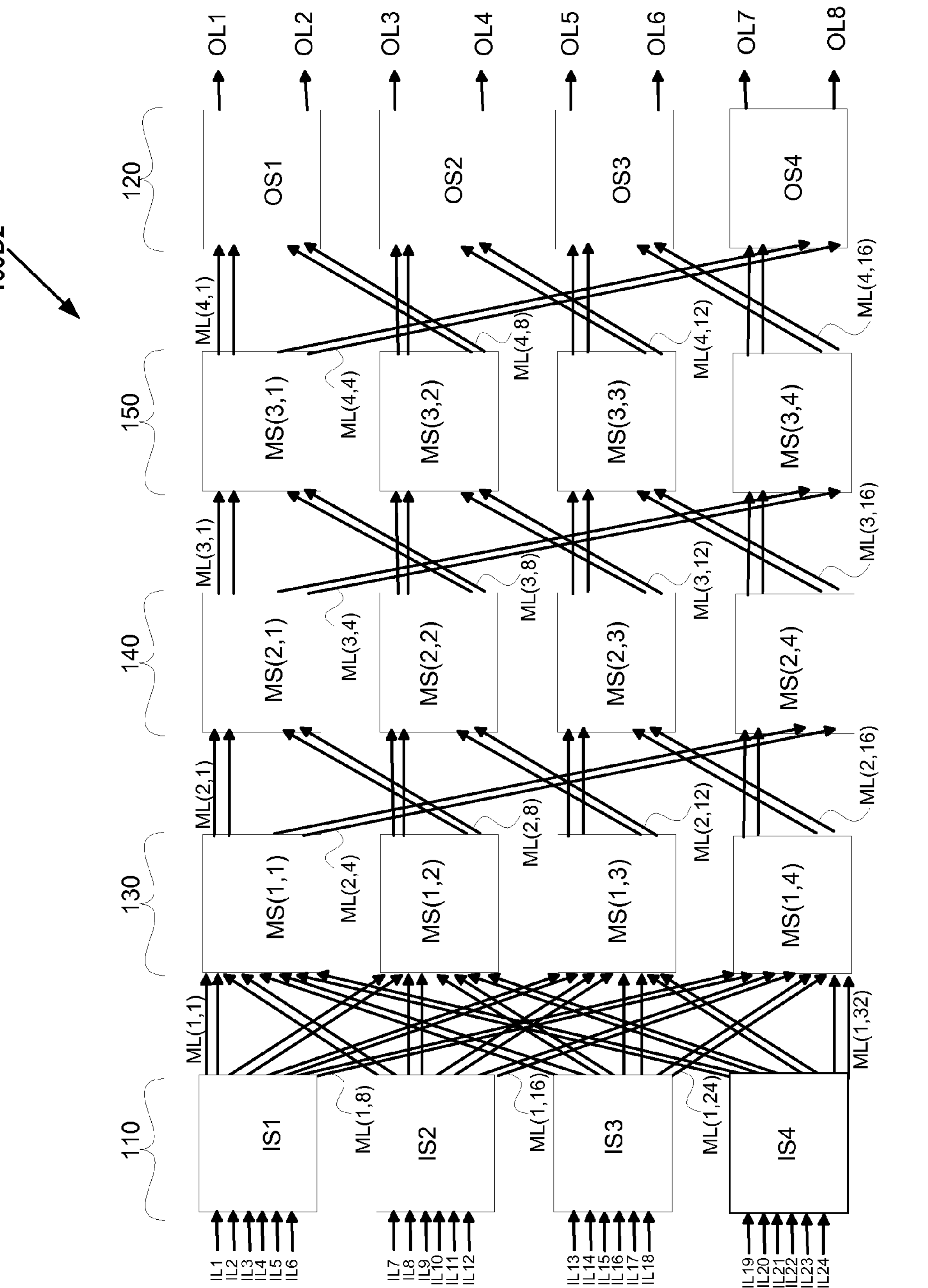
ML(4,1)
ML(4,4)
ML(4,8)
ML(4,12)
ML(4,16)

FIG. 1D2


100D2
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IS3
IS4
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MS(2,2)
MS(2,3)
MS(2,4)
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MS(3,2)
MS(3,3)
MS(3,4)
OS1
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OS4
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ML(1,8)
ML(1,16)
ML(1,24)
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ML(2,16)
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ML(3,8)
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ML(4,4)
ML(4,8)
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ML(4,16)
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OL1
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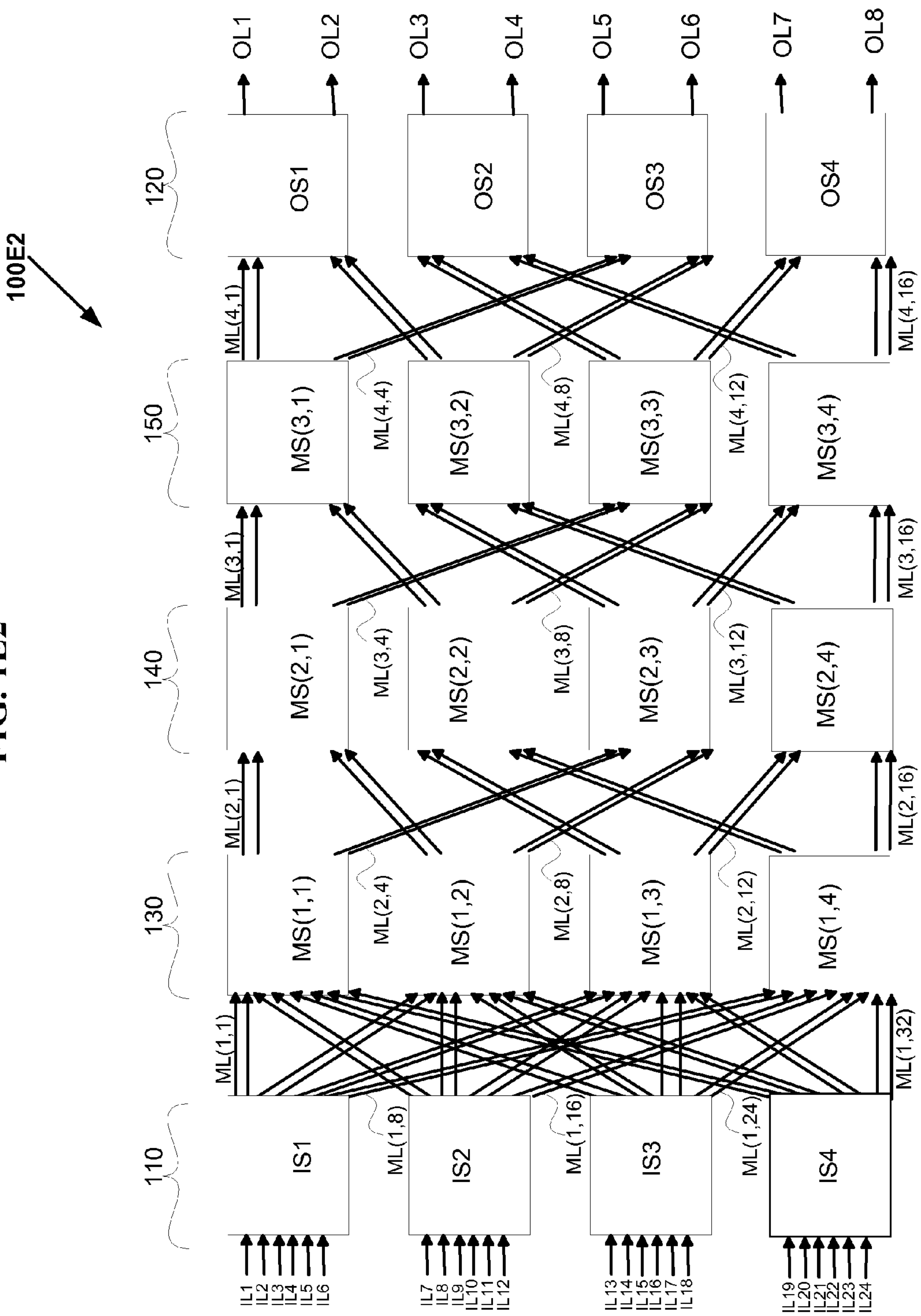
FIG. 1E2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IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
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ML(1,8)
ML(1,16)
ML(1,24)
ML(1,32)
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ML(2,4)
ML(2,8)
ML(2,12)
ML(2,16)
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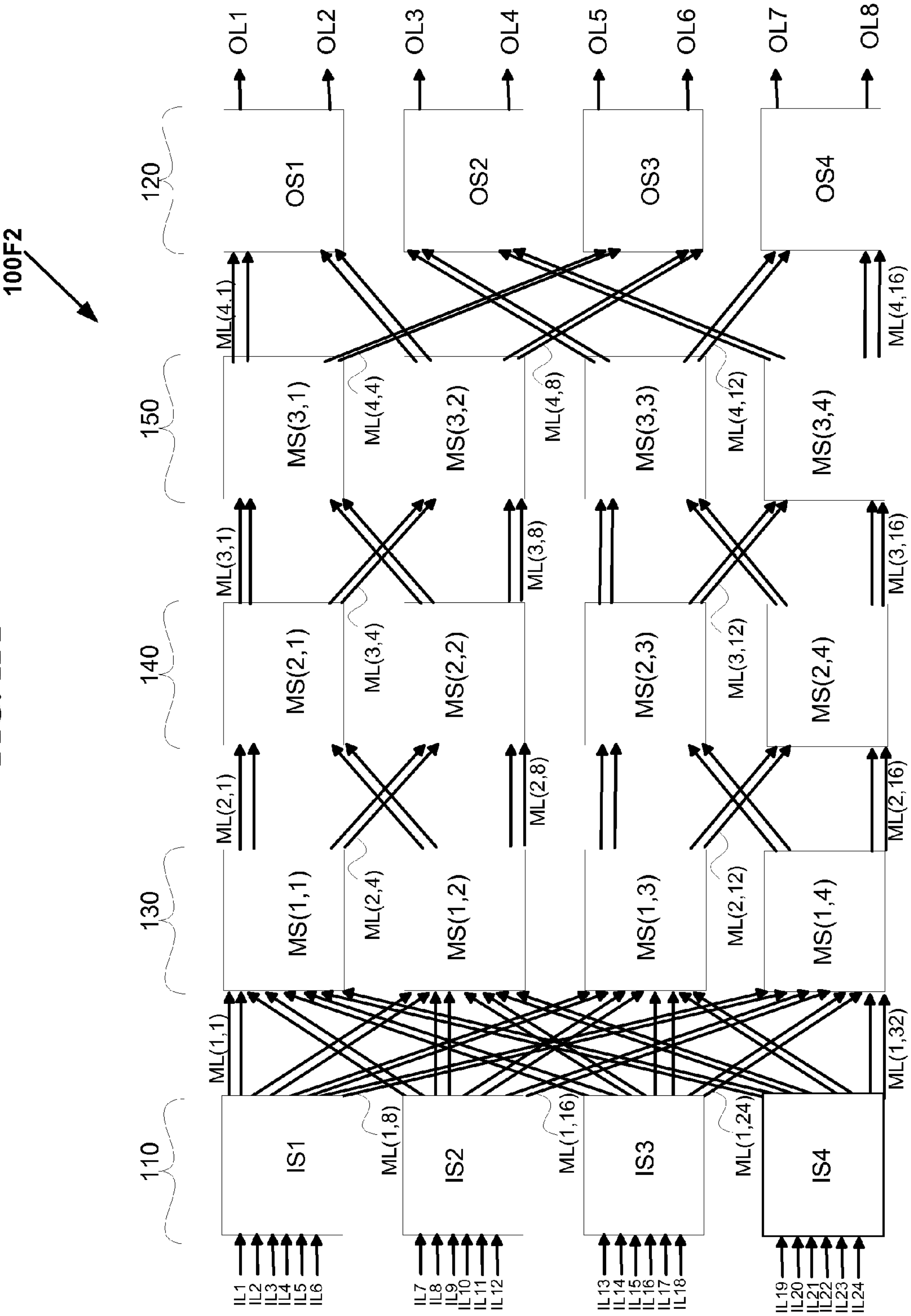
ML(3,4)
ML(3,8)
ML(3,12)
ML(3,16)
ML(4,1)
ML(4,4)
ML(4,8)
ML(4,12)
ML(4,16)
OL1 OL2 OL3 OL4 OL5 OL6 OL7 OL8

FIG. 1F2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ML(3,16)
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ML(4,4)
ML(4,8)
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ML(4,16)
IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
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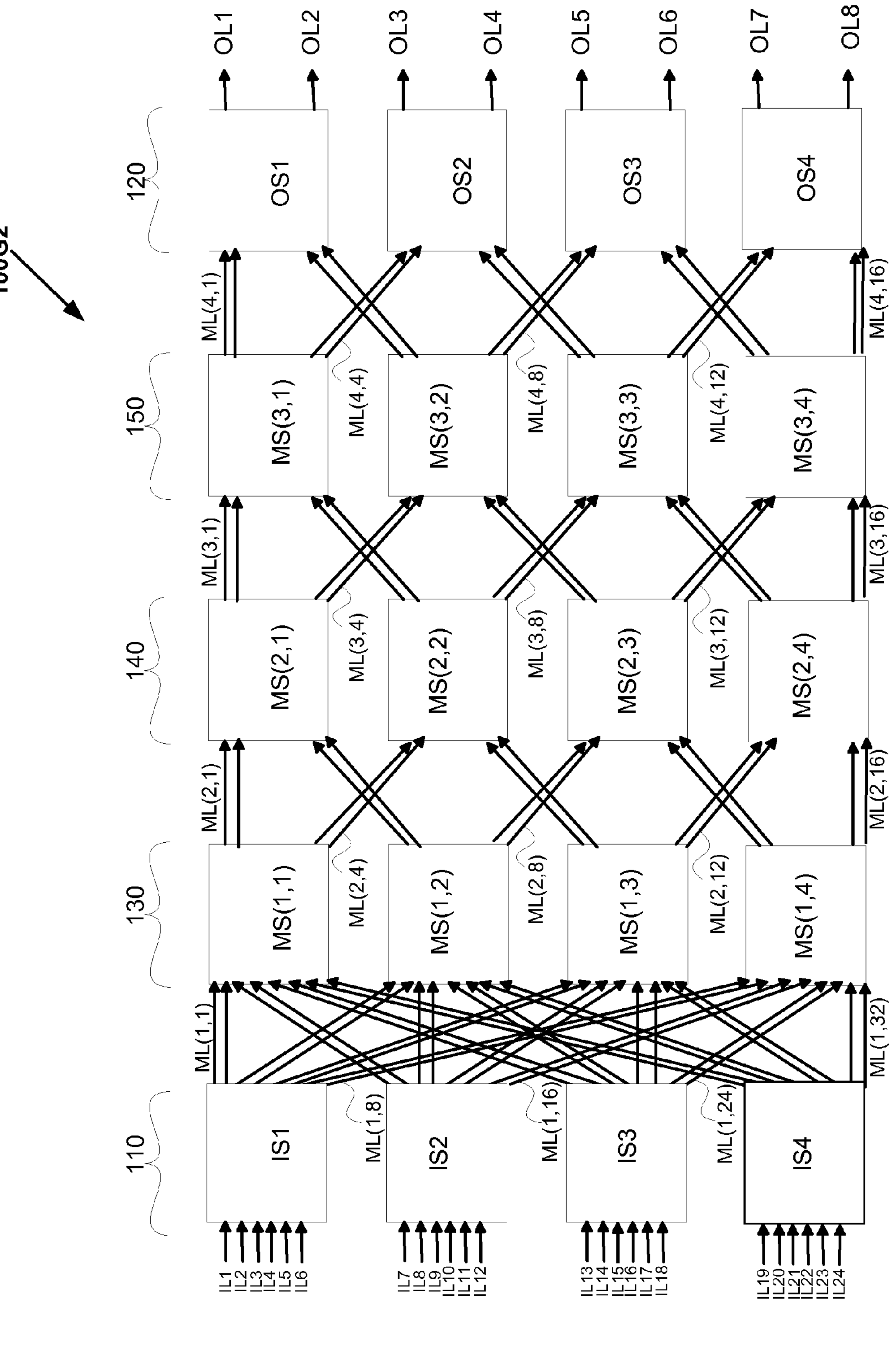
FIG. 1G2


100G2
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ML(4,1)
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ML(4,8)
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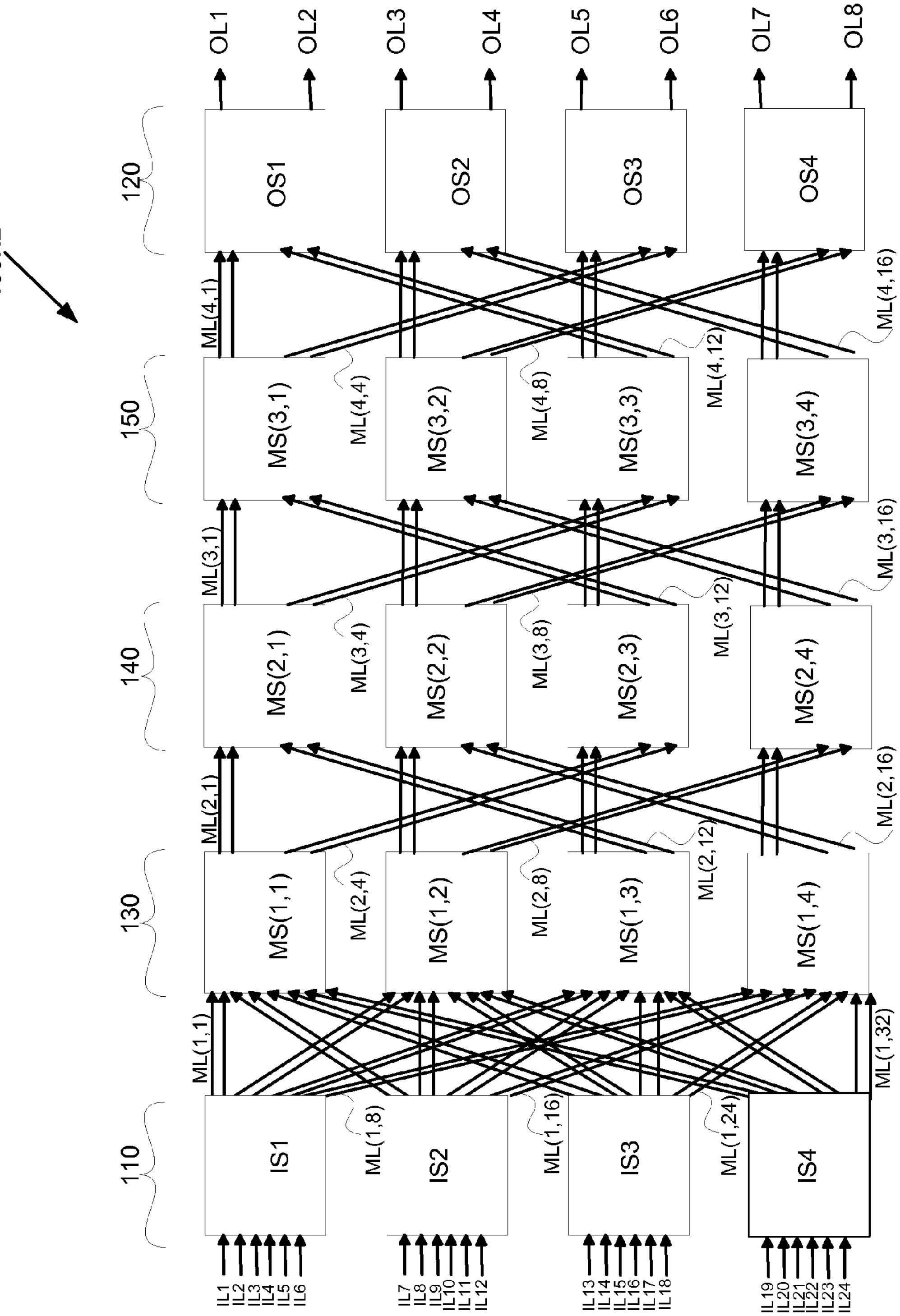
FIG. 1H2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IS3
IS4
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IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
OL1 OL2 OL3 OL4 OL5 OL6 OL7 OL8
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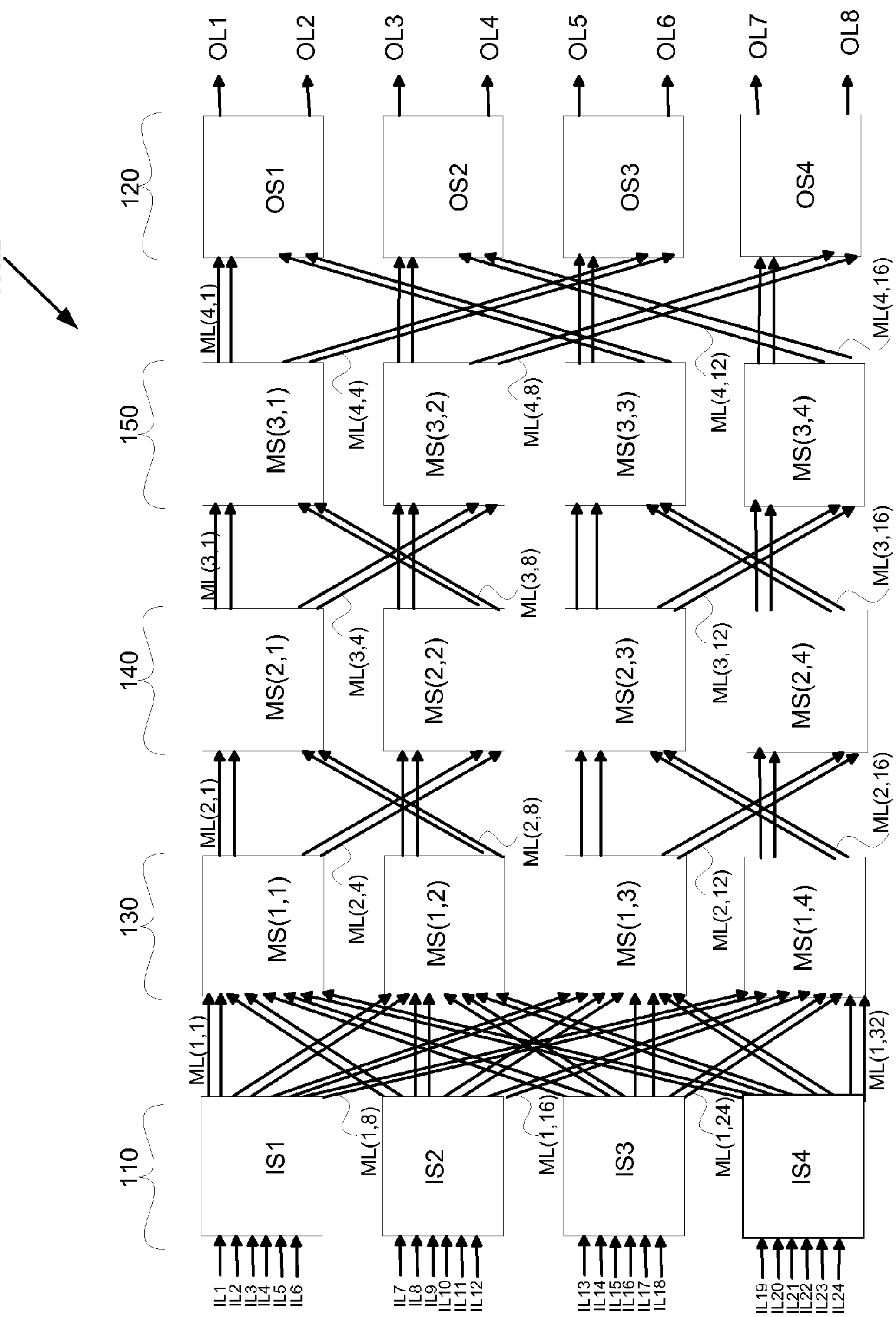
ML(3,16)
ML(4,1)
ML(4,4)
ML(4,8)
ML(4,12)
ML(4,16)

FIG. 1I2


100I2
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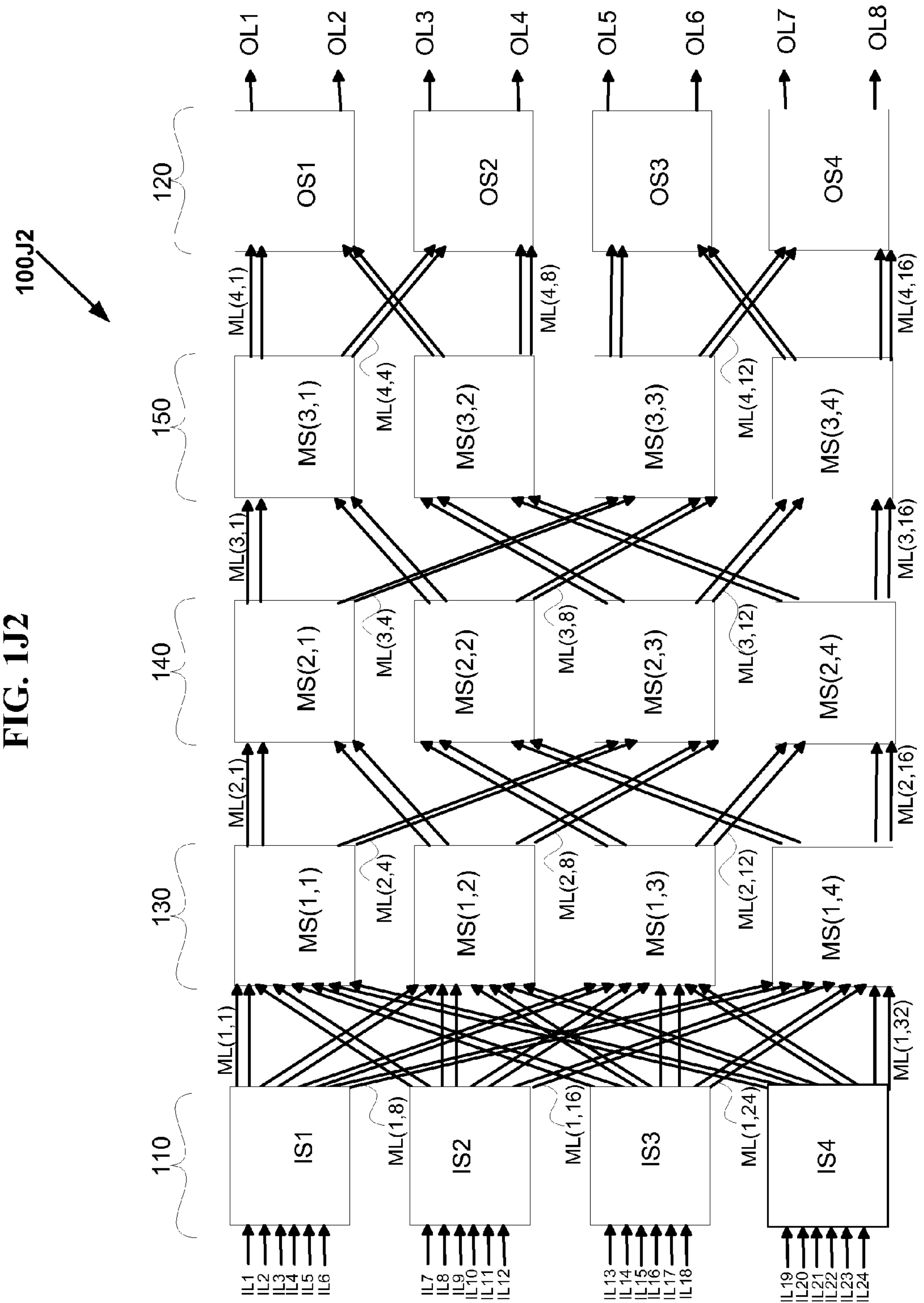
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
OL1 OL2 OL3 OL4 OL5 OL6 OL7 OL8
ML(1,1)
ML(1,8)
ML(1,16)
ML(1,24)
ML(1,32)
ML(2,1)
ML(2,4)
ML(2,8)
ML(2,12)
ML(2,16)
ML(3,1)
ML(3,4)
ML(3,8)
ML(3,12)
ML(3,16)
ML(4,1)
ML(4,4)
ML(4,8)
ML(4,12)
ML(4,16)

FIG. 1J2


100J2
110
120
130
140
150
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
OL1 OL2 OL3 OL4 OL5 OL6 OL7 OL8
ML(1,1)
ML(1,8)
ML(1,16)
ML(1,24)
ML(1,32)
ML(2,1)
ML(2,4)
ML(2,8)
ML(2,12)
ML(2,16)
ML(3,1)
ML(3,4)
ML(3,8)
ML(3,12)
ML(3,16)
ML(4,1)
ML(4,4)
ML(4,8)
ML(4,12)
ML(4,16)

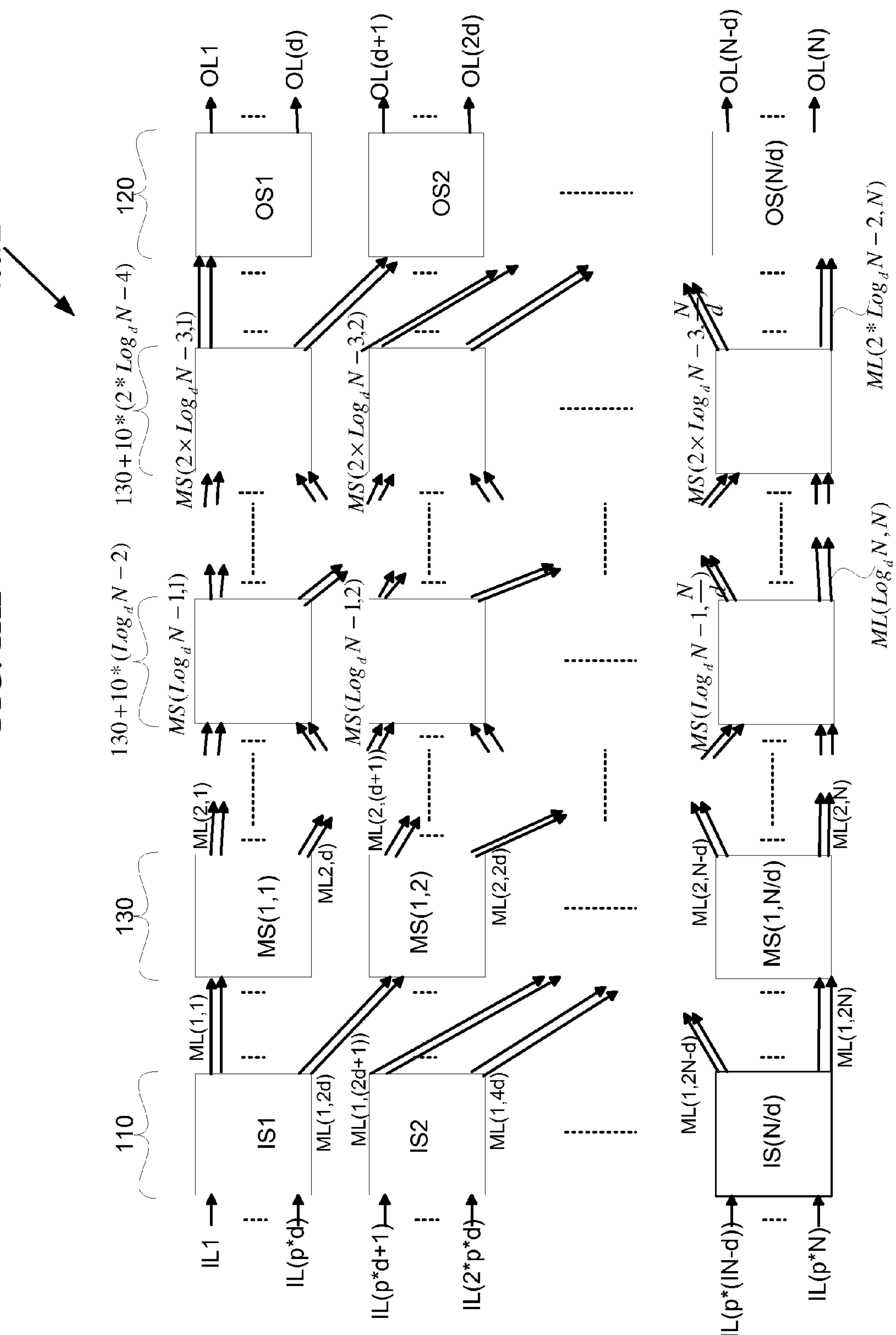
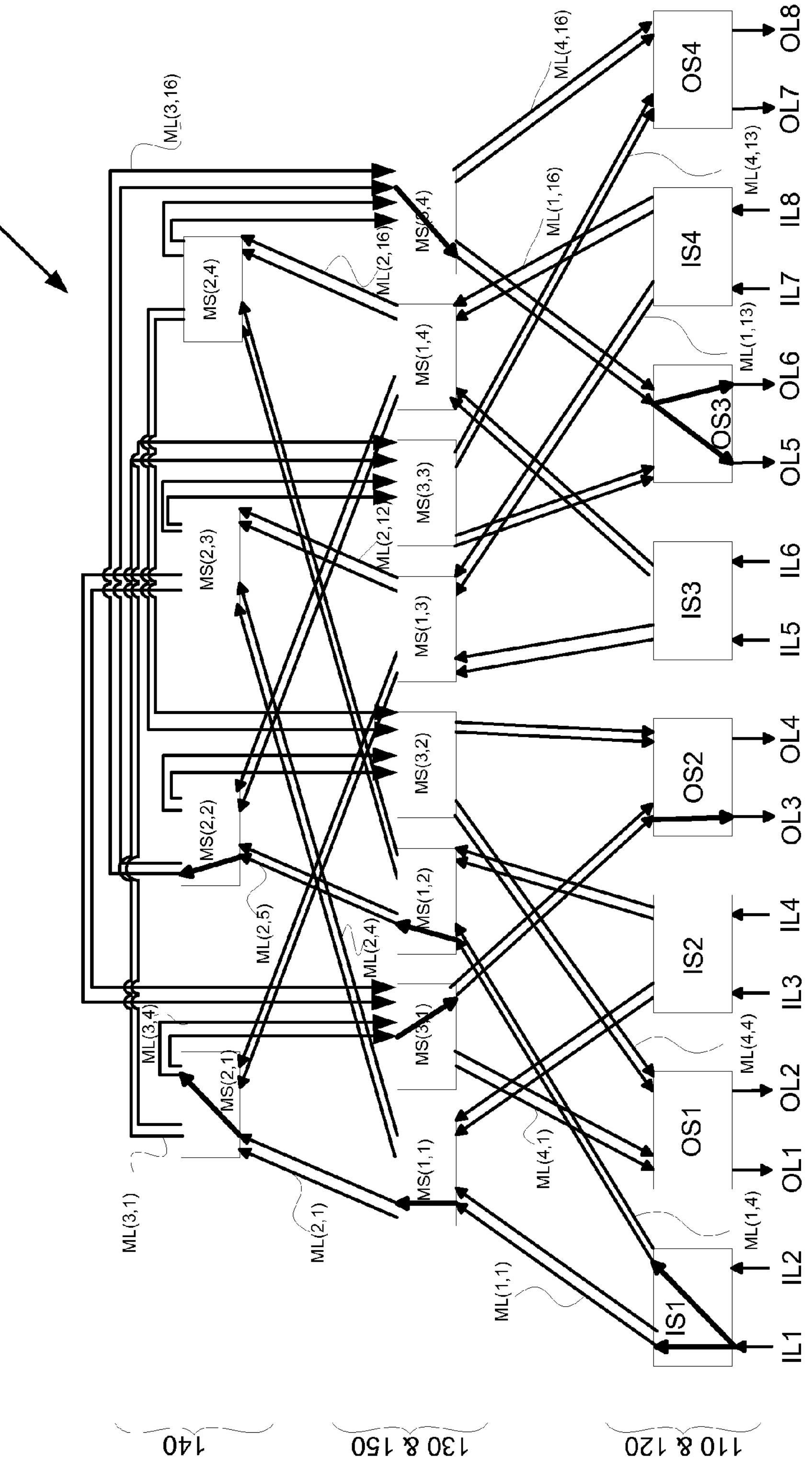

100K2
110
130
$130+10*(Log_d N-2)$
$130+10*(2*Log_d N-4)$
120
IS1
IS2
IS(N/d)
MS(1,1)
MS(1,2)
MS(1,N/d)
$MS(Log_d N-1,1)$
$MS(Log_d N-1,2)$
$MS(Log_d N-1,\frac{N}{d})$
$MS(2\times Log_d N-3,1)$
$MS(2\times Log_d N-3,2)$
$MS(2\times Log_d N-3,\frac{N}{d})$
OS1
OS2
OS(N/d)
IL1
IL(p*d)
IL(p*d+1)
IL(2*p*d)
IL(p*(N-d))
IL(p*N)
ML(1,1)
ML(1,2d)
ML(1,(2d+1))
ML(1,4d)
ML(1,2N-d)
ML(1,2N)
ML(2,1)
ML2,d)
ML(2,(d+1))
ML(2,2d)
ML(2,N-d)
ML(2,N)
$ML(Log_d N,N)$
$ML(2*Log_d N-2,N)$
OL1
OL(d)
OL(d+1)
OL(2d)
OL(N-d)
OL(N)

FIG. 1K2

FIG. 2A


200A
IS1
IS2
IS3
IS4
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
ML(1,1)
ML(1,4)
ML(1,13)
ML(1,16)
ML(2,1)
ML(2,4)
ML(2,5)
ML(2,12)
ML(2,16)
ML(3,1)
ML(3,4)
ML(3,16)
ML(4,1)
ML(4,4)
ML(4,13)
ML(4,16)
140
130 & 150
110 & 120

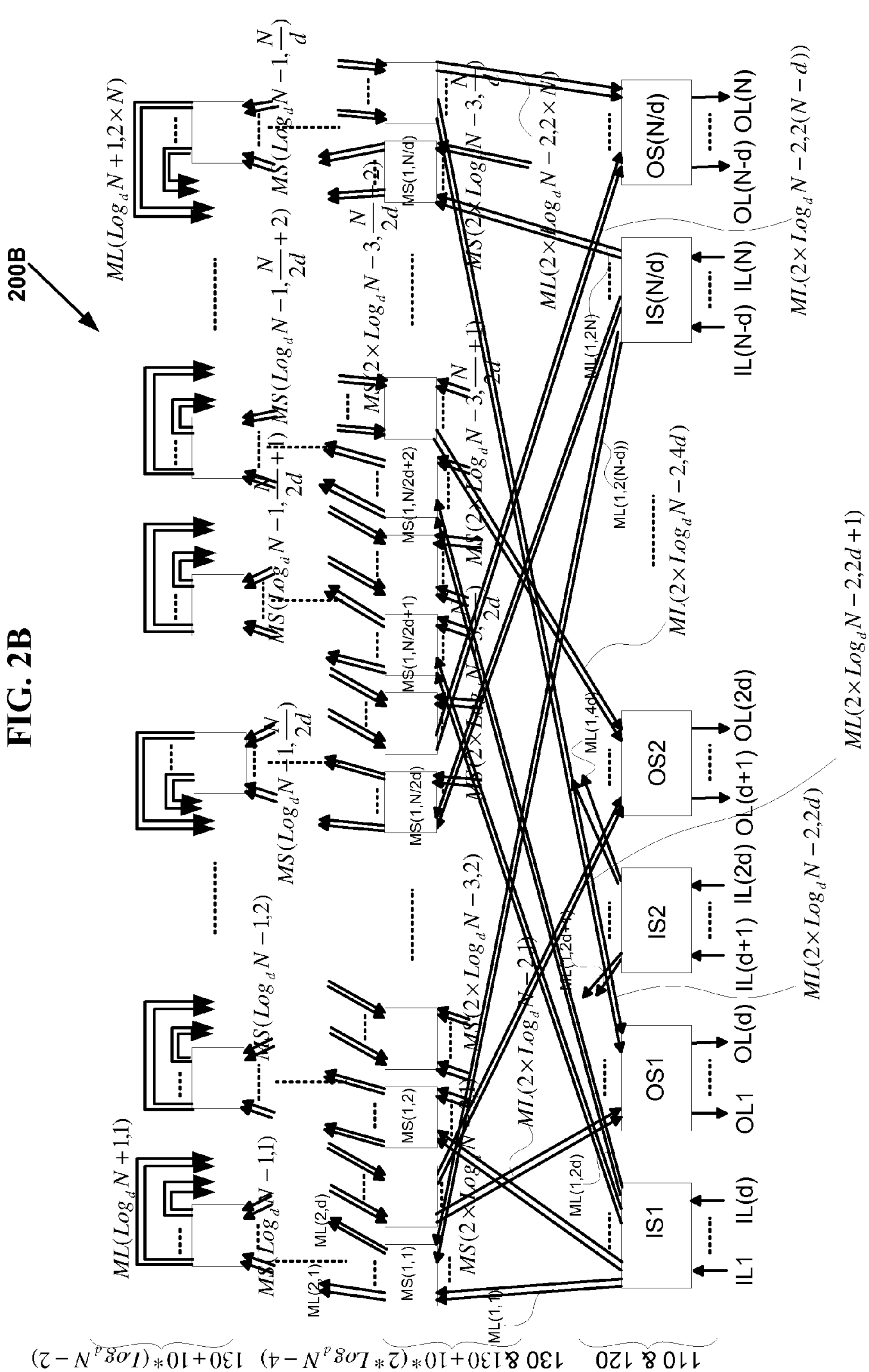

200B
IS1
OS1
IS2
OS2
IS(N/d)
OS(N/d)
IL1
IL(d)
OL1
OL(d)
IL(d+1)
IL(2d)
OL(d+1)
OL(2d)
IL(N-d)
IL(N)
OL(N-d)
OL(N)
MS(1,1)
MS(1,2)
MS(1,N/2d)
MS(1,N/2d+1)
MS(1,N/2d+2)
MS(1,N/d)
ML(1,1)
ML(1,2d)
ML(1,2d+1)
ML(1,4d)
ML(1,2(N-d))
ML(1,2N)
ML(2,1)
ML(2,d)
110 & 120
130 & 130+10*(2*Log_d N-4)
130+10*(Log_d N-2)

FIG. 2B

FIG. 2C

200C

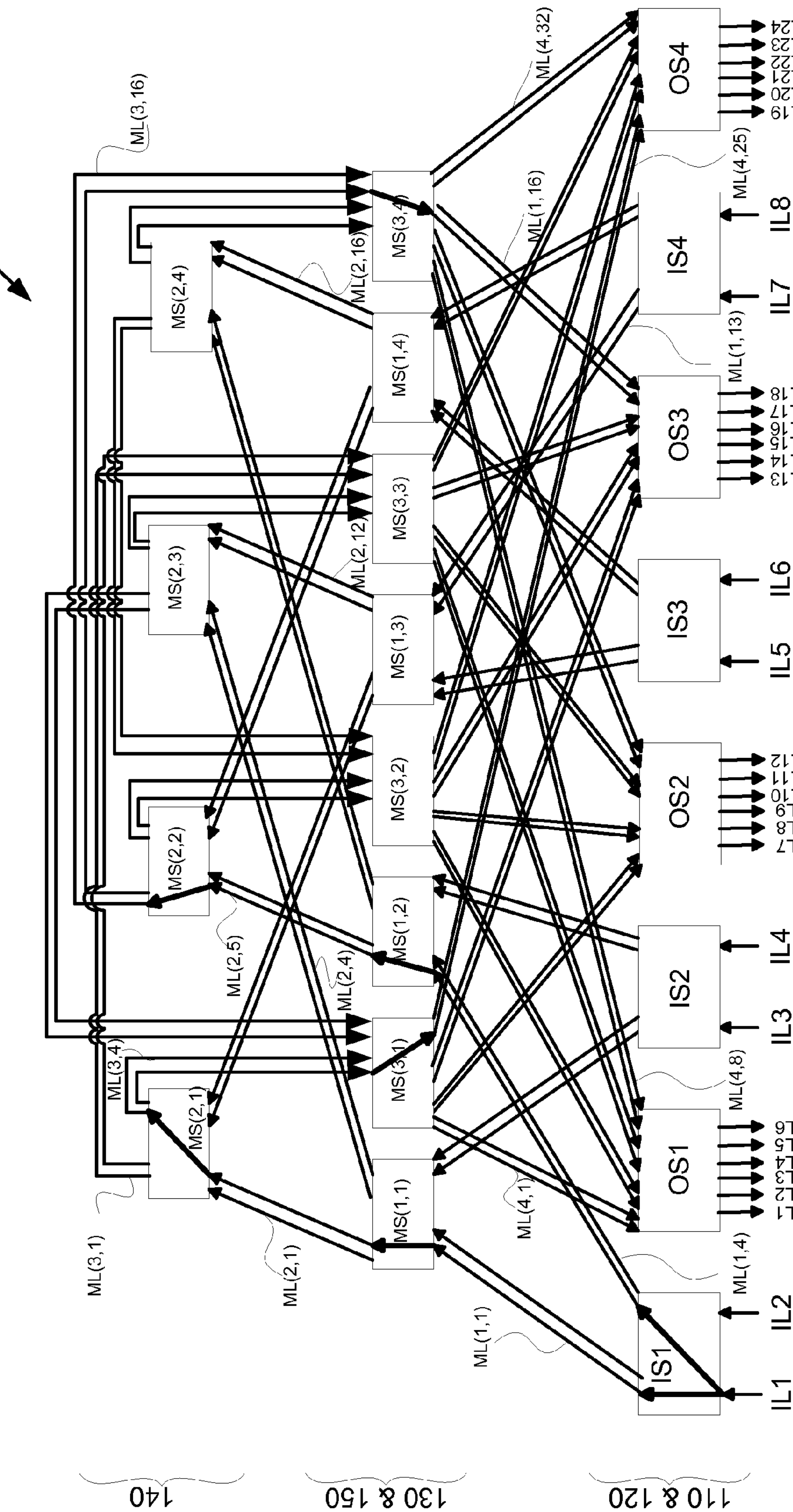

ML(3,16)
ML(4,32)
OS4
OL19
OL20
OL21
OL22
OL23
OL24
ML(4,25)
IS4
IL7
IL8
ML(1,16)
MS(3,4)
MS(2,4)
ML(2,16)
MS(1,4)
ML(1,13)
OS3
OL13
OL14
OL15
OL16
OL17
OL18
MS(3,3)
MS(2,3)
ML(2,12)
MS(1,3)
IS3
IL5
IL6
MS(3,2)
OS2
OL7
OL8
OL9
OL10
OL11
OL12
MS(2,2)
MS(1,2)
ML(2,5)
ML(2,4)
IS2
IL3
IL4
MS(3,1)
ML(3,4)
ML(4,8)
MS(2,1)
OS1
OL1
OL2
OL3
OL4
OL5
OL6
ML(4,1)
MS(1,1)
ML(3,1)
ML(2,1)
ML(1,4)
ML(1,1)
IS1
IL1
IL2
140
130 & 150
110 & 120

FIG. 2D

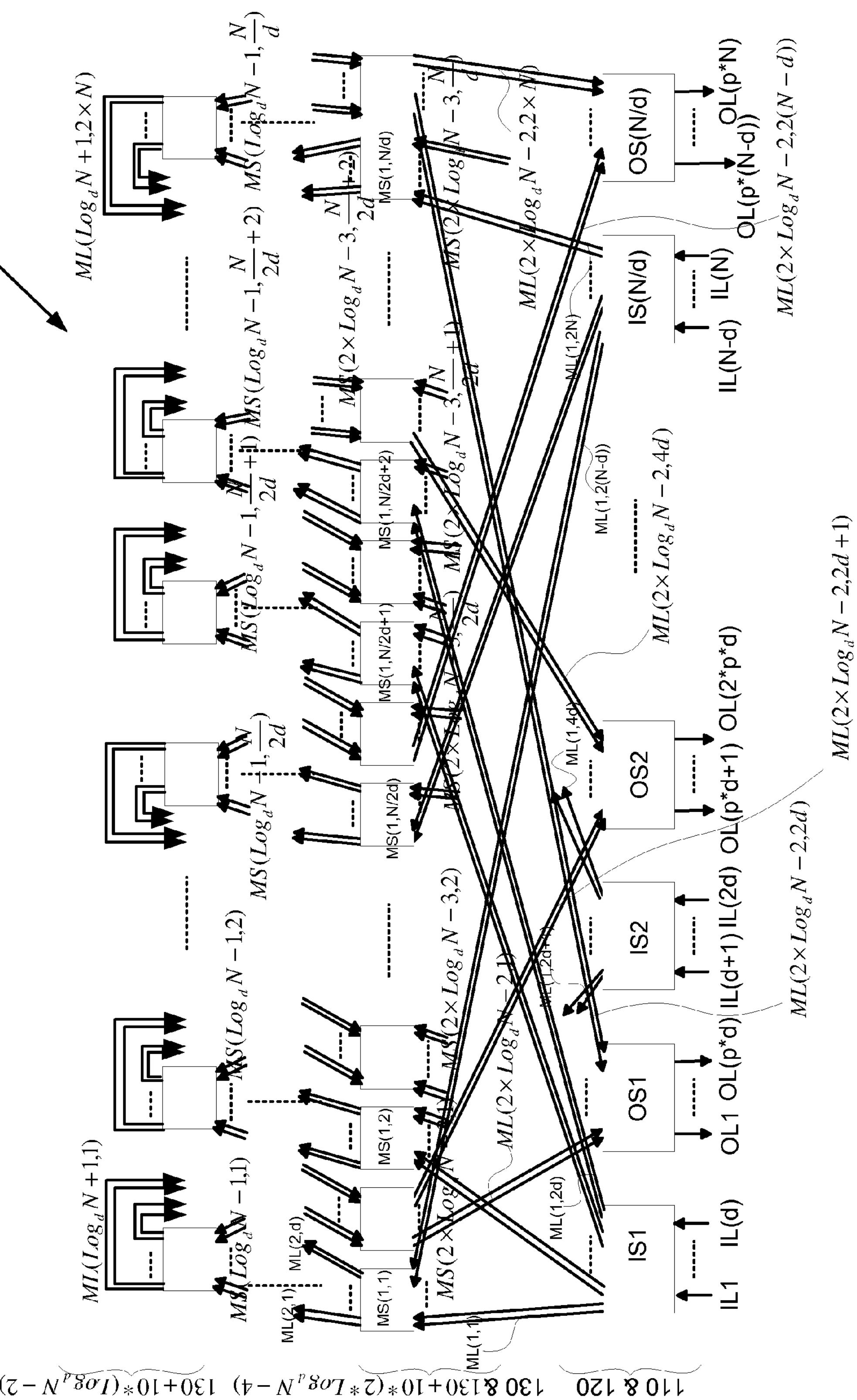

200D
IS1
IS2
IS(N/d)
OS1
OS2
OS(N/d)
IL1
IL(d)
IL(d+1)
IL(2d)
IL(N-d)
IL(N)
OL1
OL(p*d)
OL(p*d+1)
OL(2*p*d)
OL(p*(N-d))
OL(p*N)
MS(1,1)
MS(1,2)
MS(1,N/2d)
MS(1,N/2d+1)
MS(1,N/2d+2)
MS(1,N/d)
ML(1,1)
ML(1,2d)
ML(1,4d)
ML(1,2N)
ML(2,1)
ML(2,d)
110 & 120
130 & 130+10*(2*Log_d N-4)
130+10*(Log_d N-2)

FIG. 2E

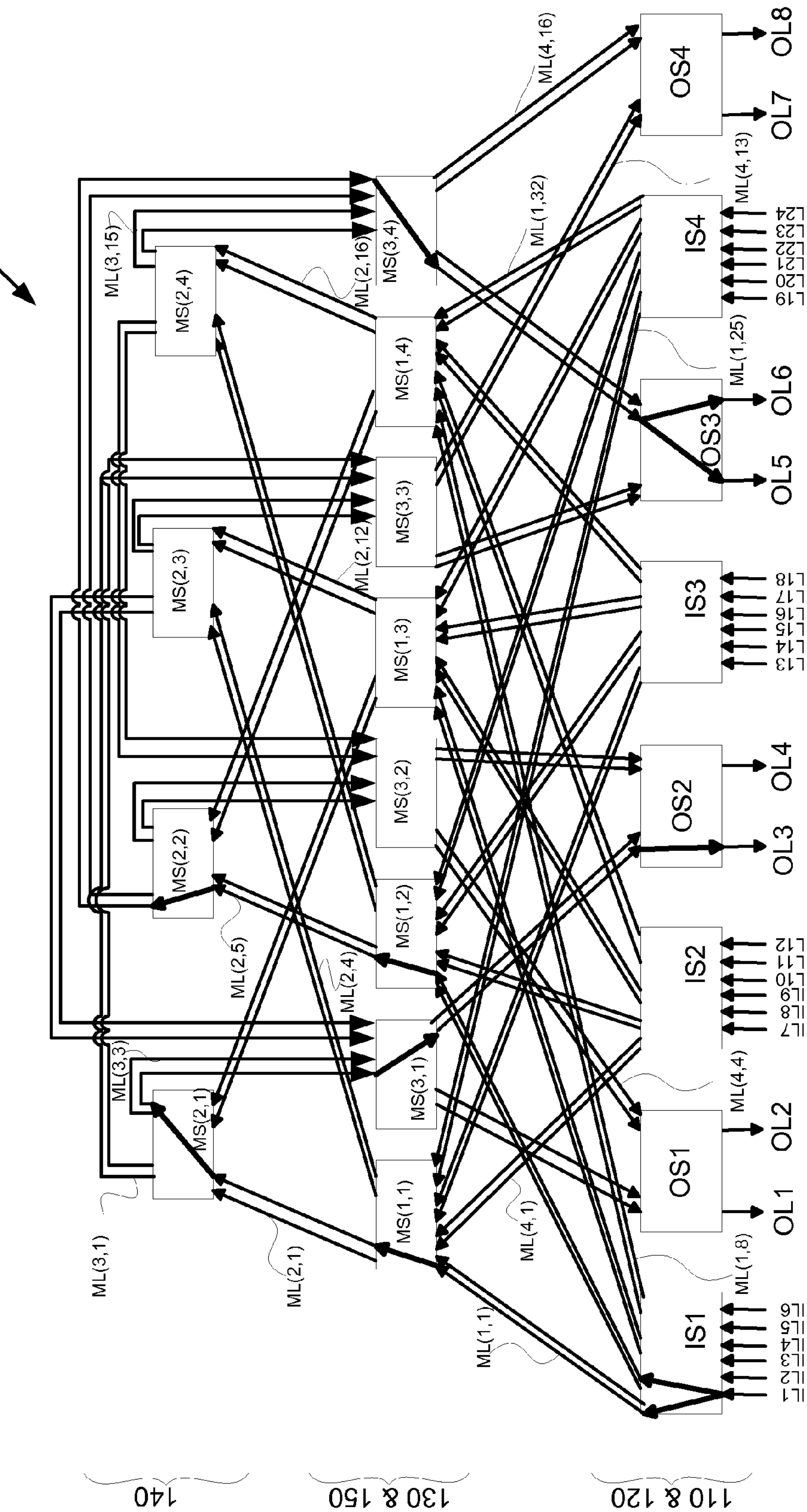

200E
IS1
IS2
IS3
IS4
OS1
OS2
OS3
OS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
IL9
IL10
IL11
IL12
IL13
IL14
IL15
IL16
IL17
IL18
IL19
IL20
IL21
IL22
IL23
IL24
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
ML(1,1)
ML(1,8)
ML(1,25)
ML(1,32)
ML(2,1)
ML(2,4)
ML(2,5)
ML(2,12)
ML(2,16)
ML(3,1)
ML(3,3)
ML(3,15)
ML(4,1)
ML(4,4)
ML(4,13)
ML(4,16)
110 & 120
130 & 150
140

FIG. 2F

200F

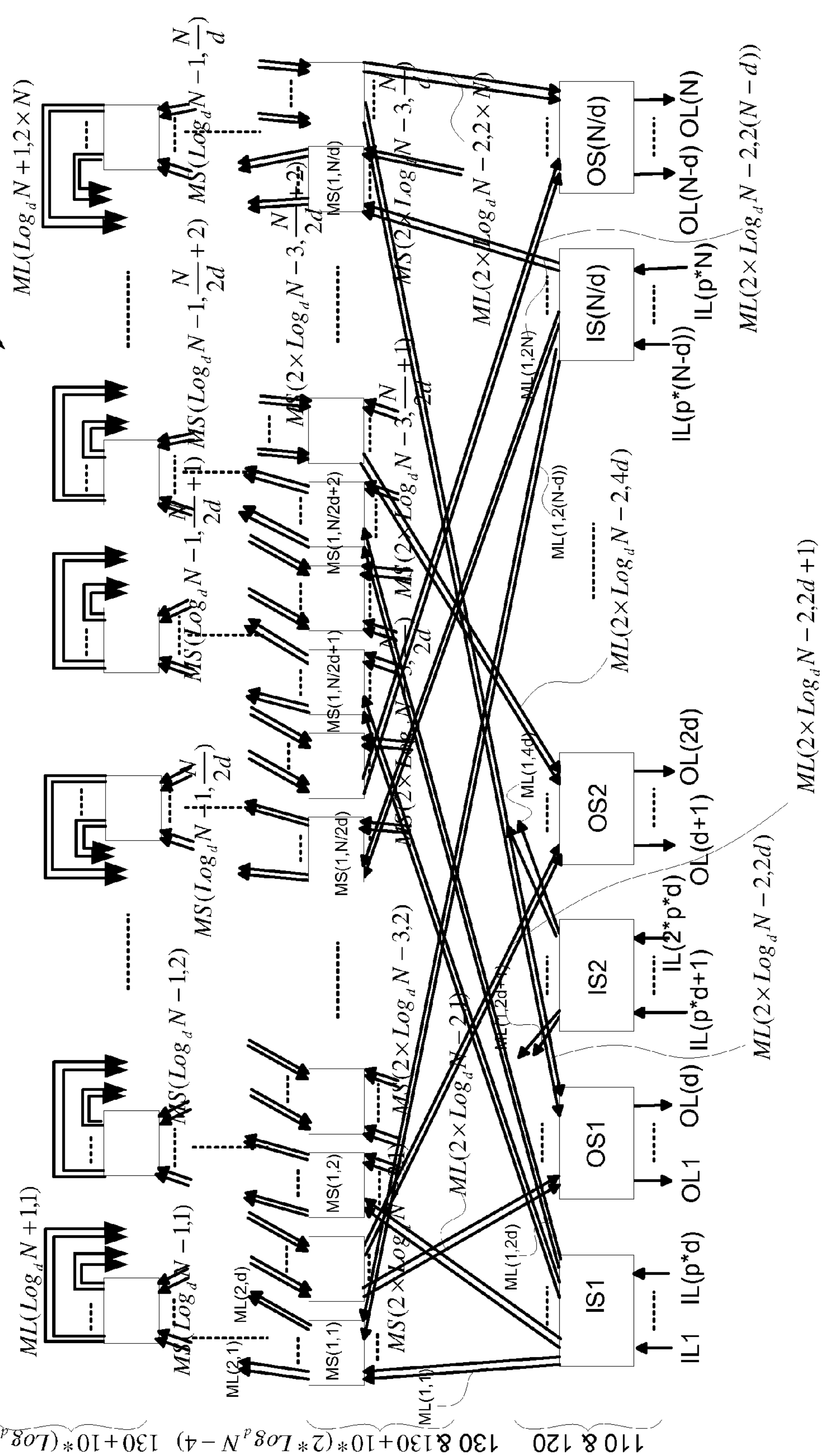

IS1
IS2
IS(N/d)
OS1
OS2
OS(N/d)
MS(1,1)
MS(1,2)
MS(1,N/2d)
MS(1,N/2d+1)
MS(1,N/2d+2)
MS(1,N/d)
IL1
IL(p*d)
IL(p*d+1)
IL(2*p*d)
IL(p*(N-d))
IL(p*N)
OL1
OL(d)
OL(d+1)
OL(2d)
OL(N-d)
OL(N)
ML(1,1)
ML(1,2d)
ML(1,2d+1)
ML(1,4d)
ML(1,2(N-d))
ML(1,2N)
ML(2,1)
ML(2,d)
110 & 120
130 & 130+10*(2*Log_d N-4)
130+10*(Log_d N-2)

FIG. 3A

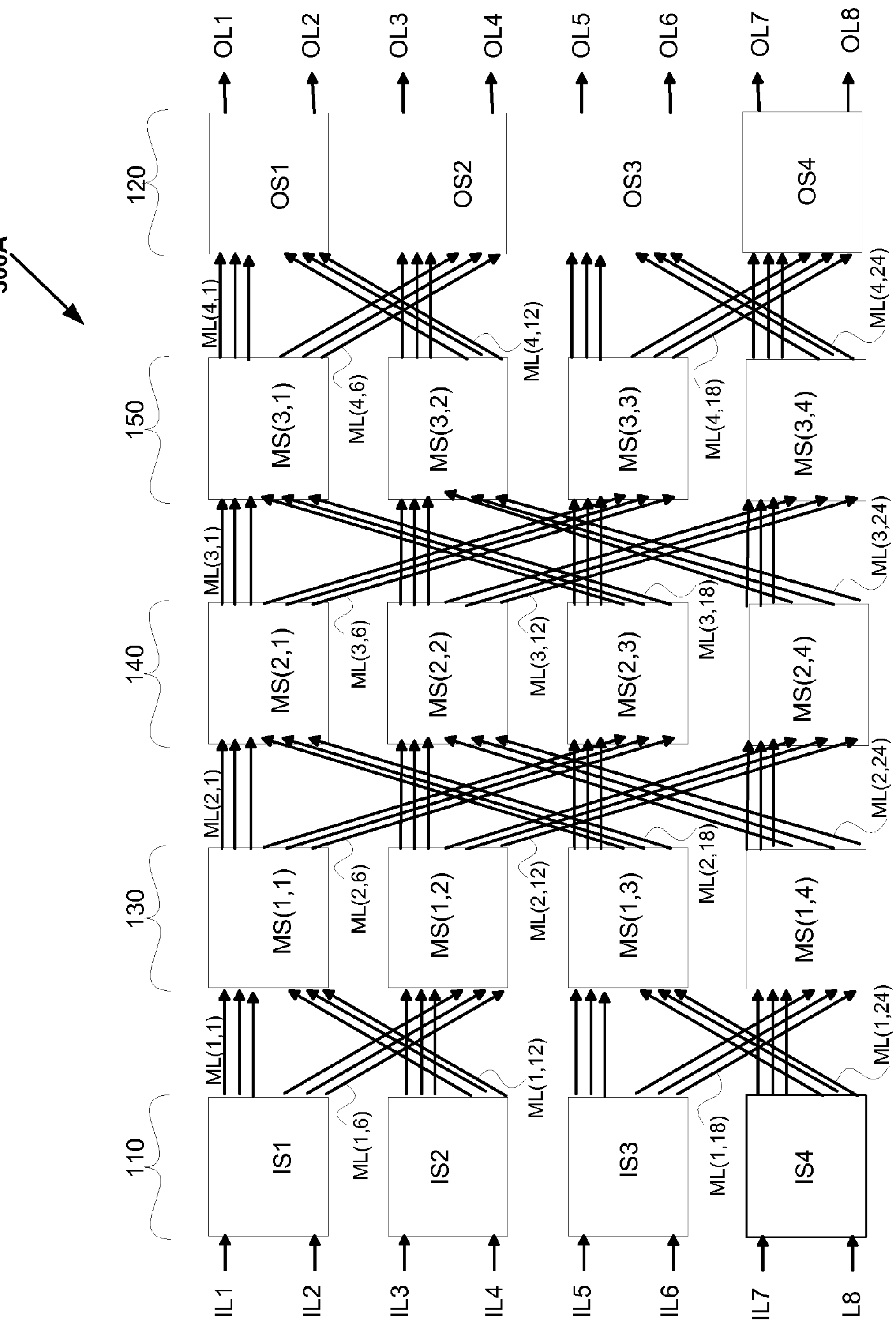

300A
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)

FIG. 3B

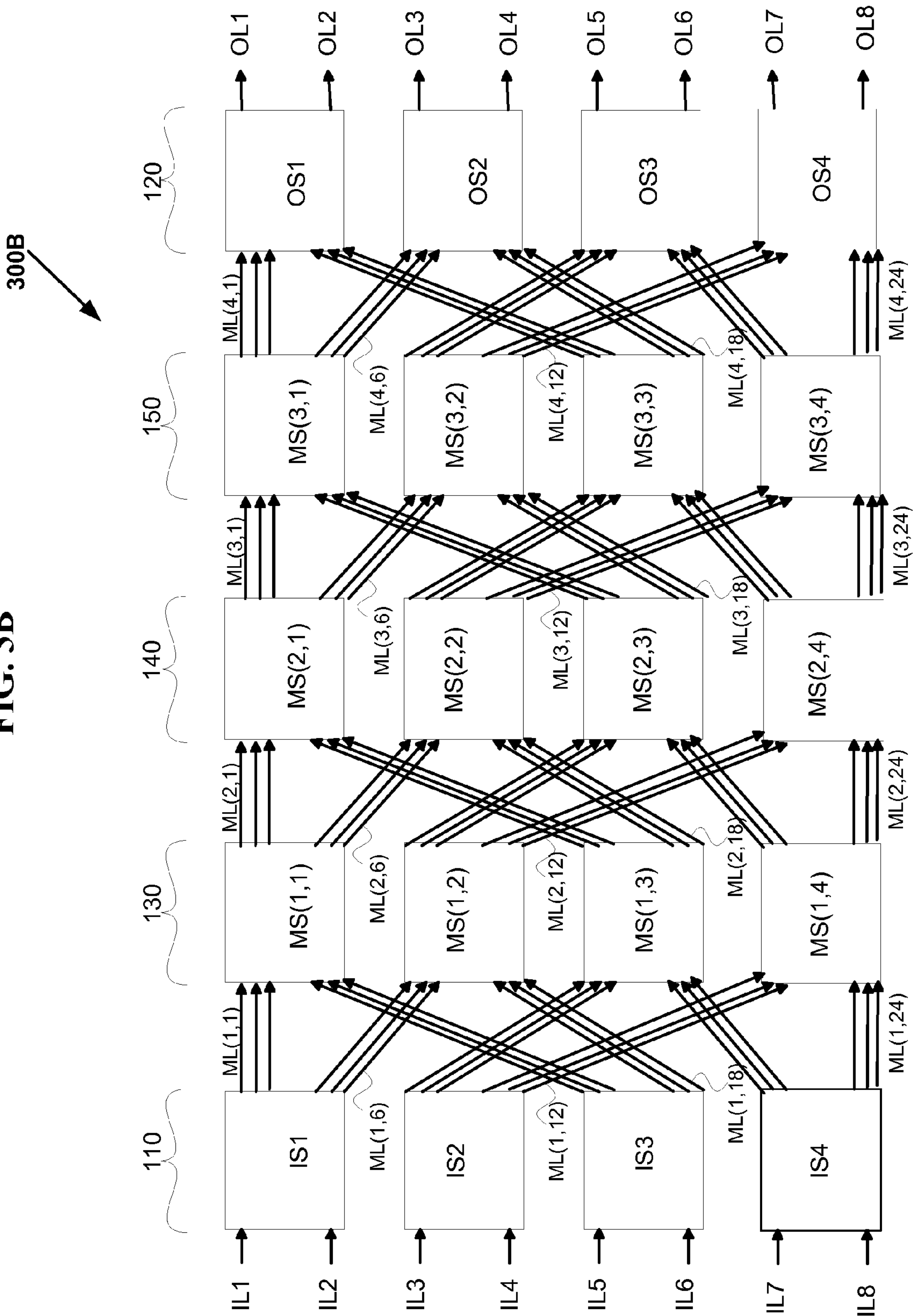

300B
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)

FIG. 3C

300C

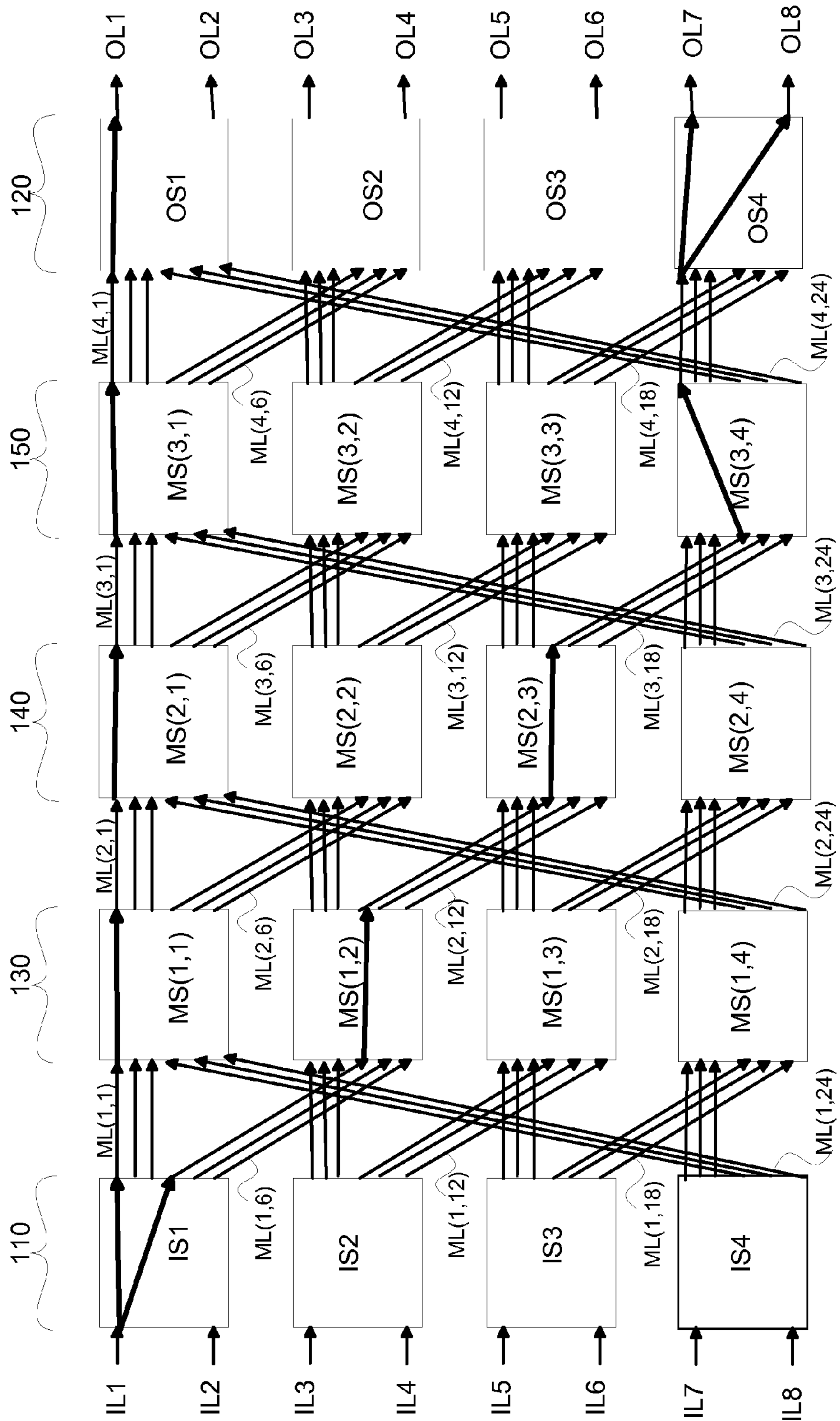

110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)

FIG. 3D

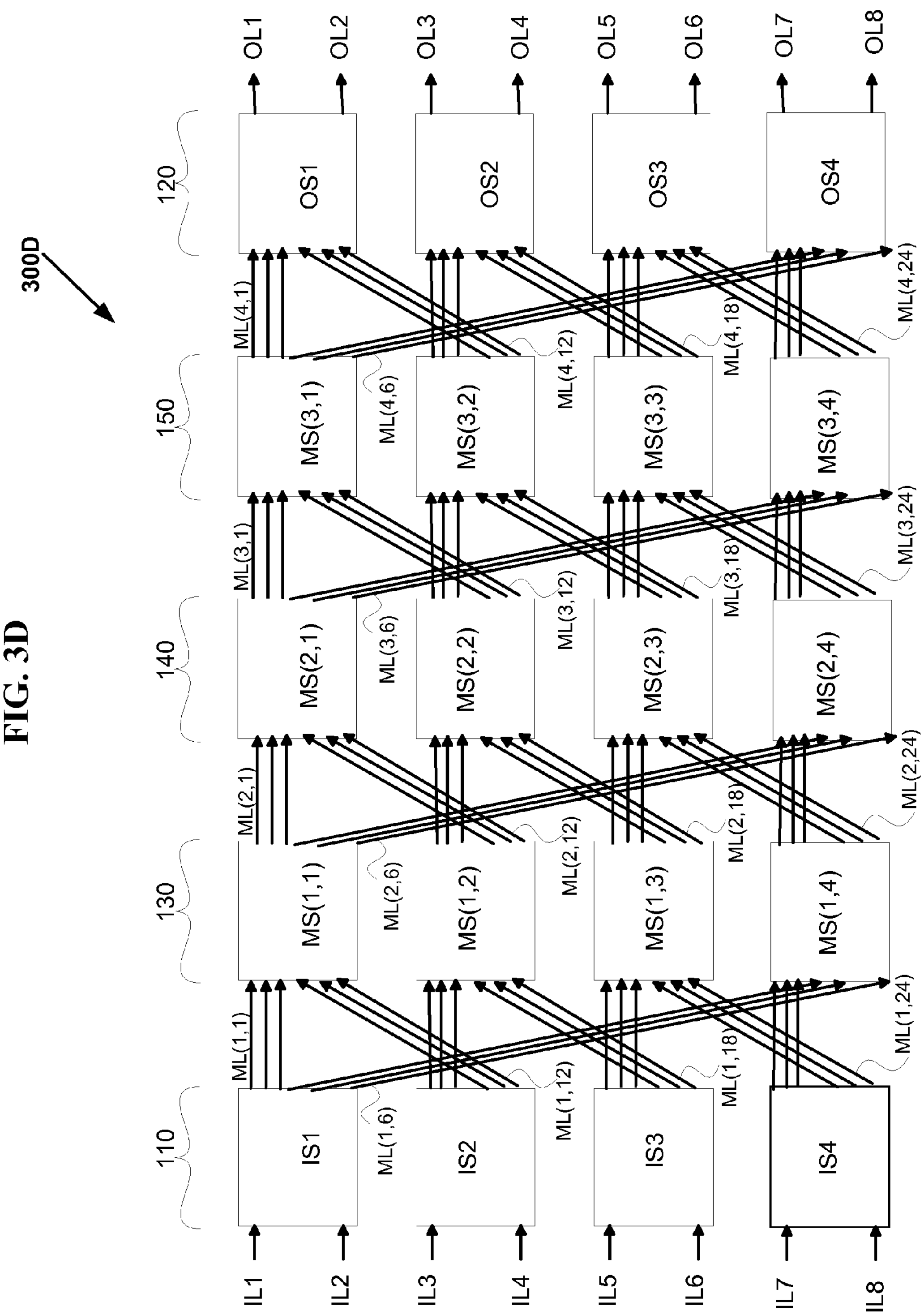
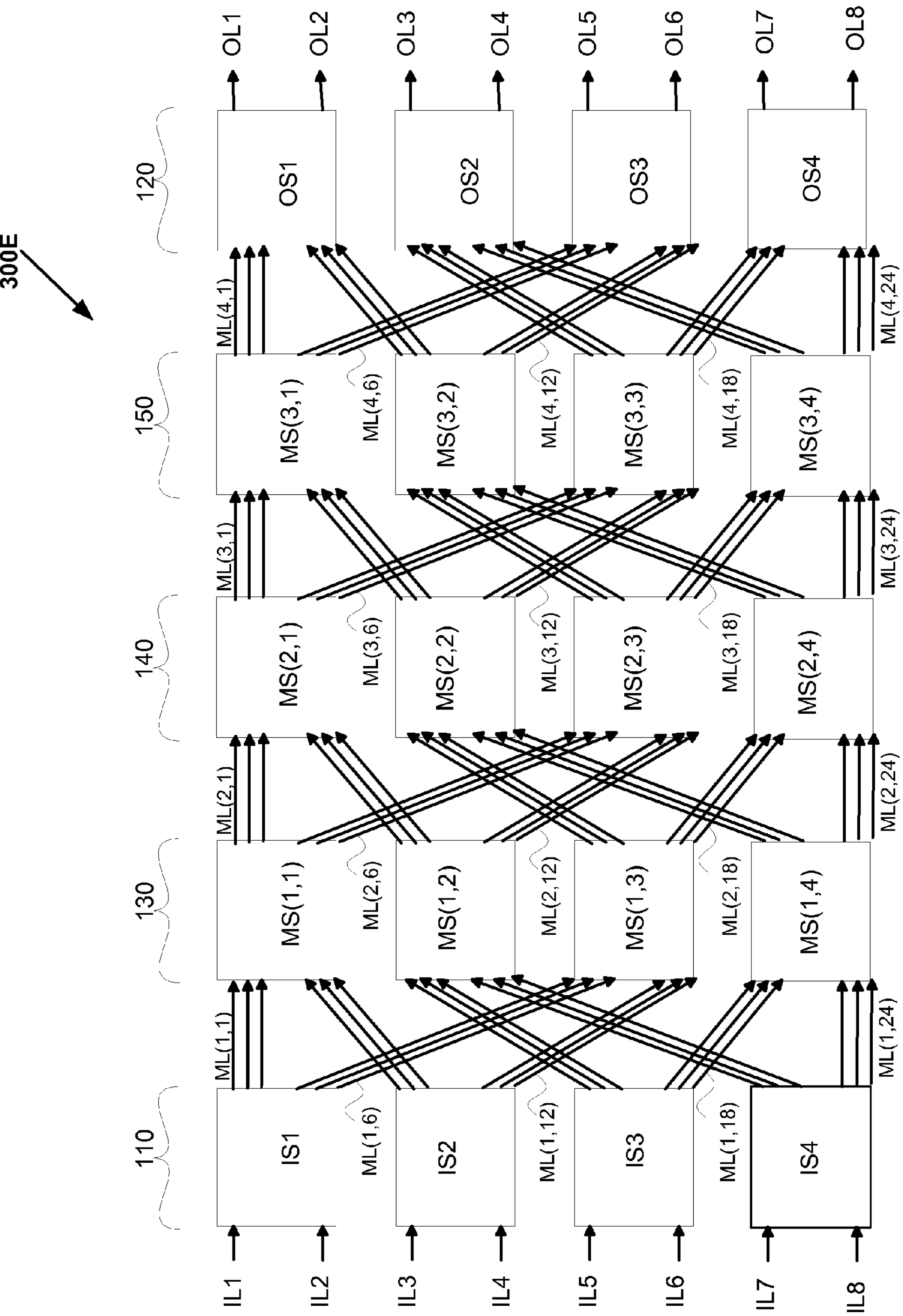

300D
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)

FIG. 3E


300E
110
120
130
140
150
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)

300F

FIG. 3F

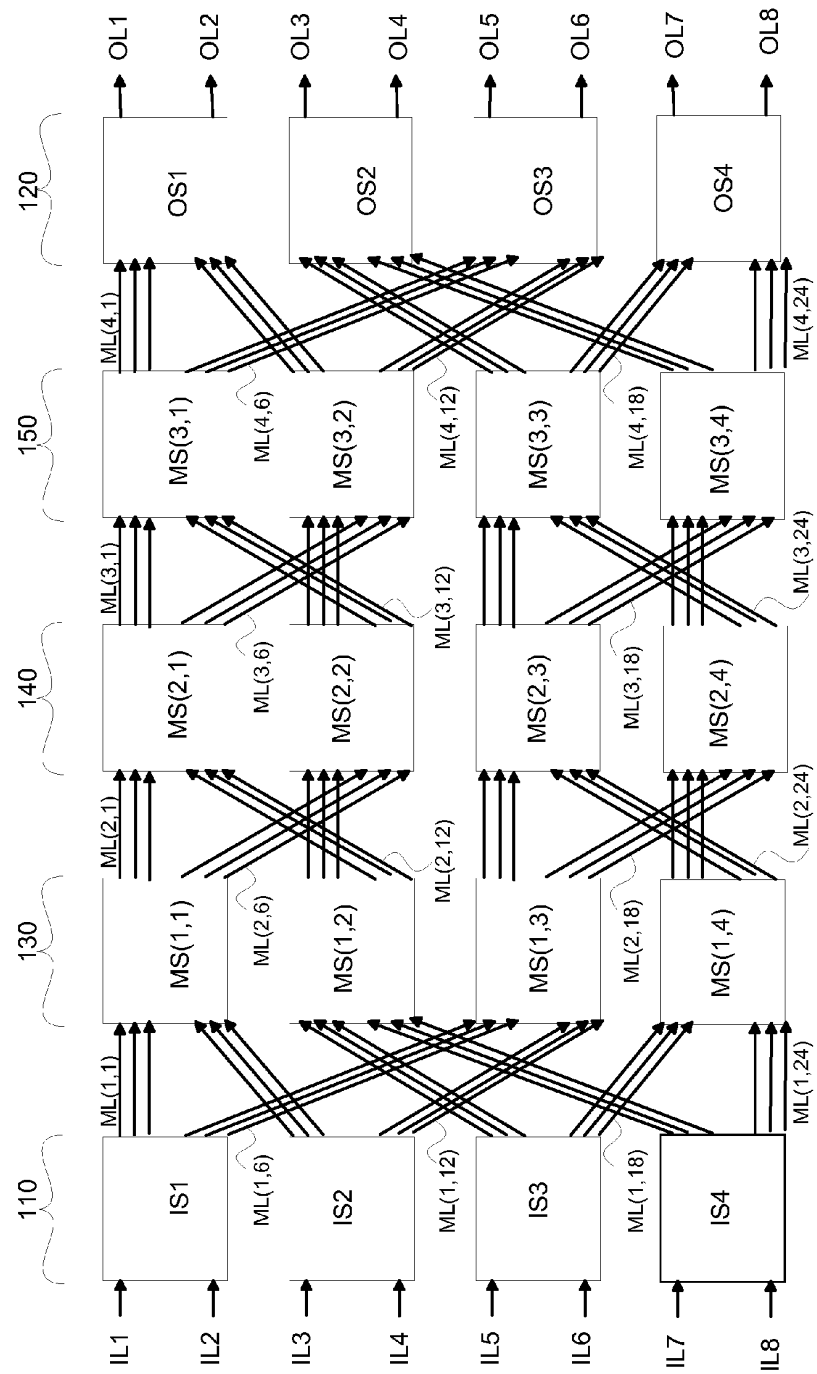

OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
120
OS1
OS2
OS3
OS4
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)
150
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
140
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
130
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
110
IS1
IS2
IS3
IS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8

FIG. 3G

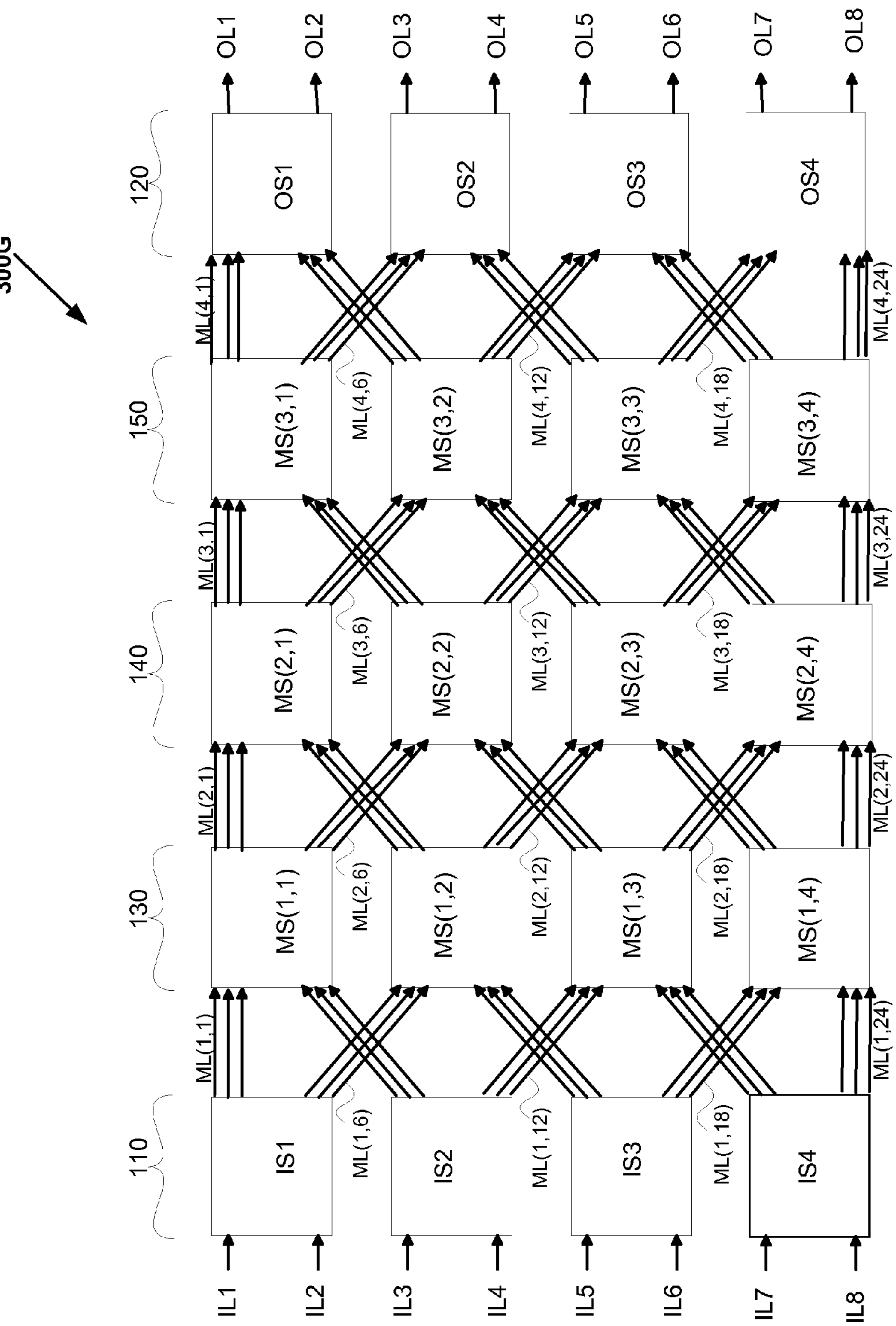

300G
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)

FIG. 3H

300H

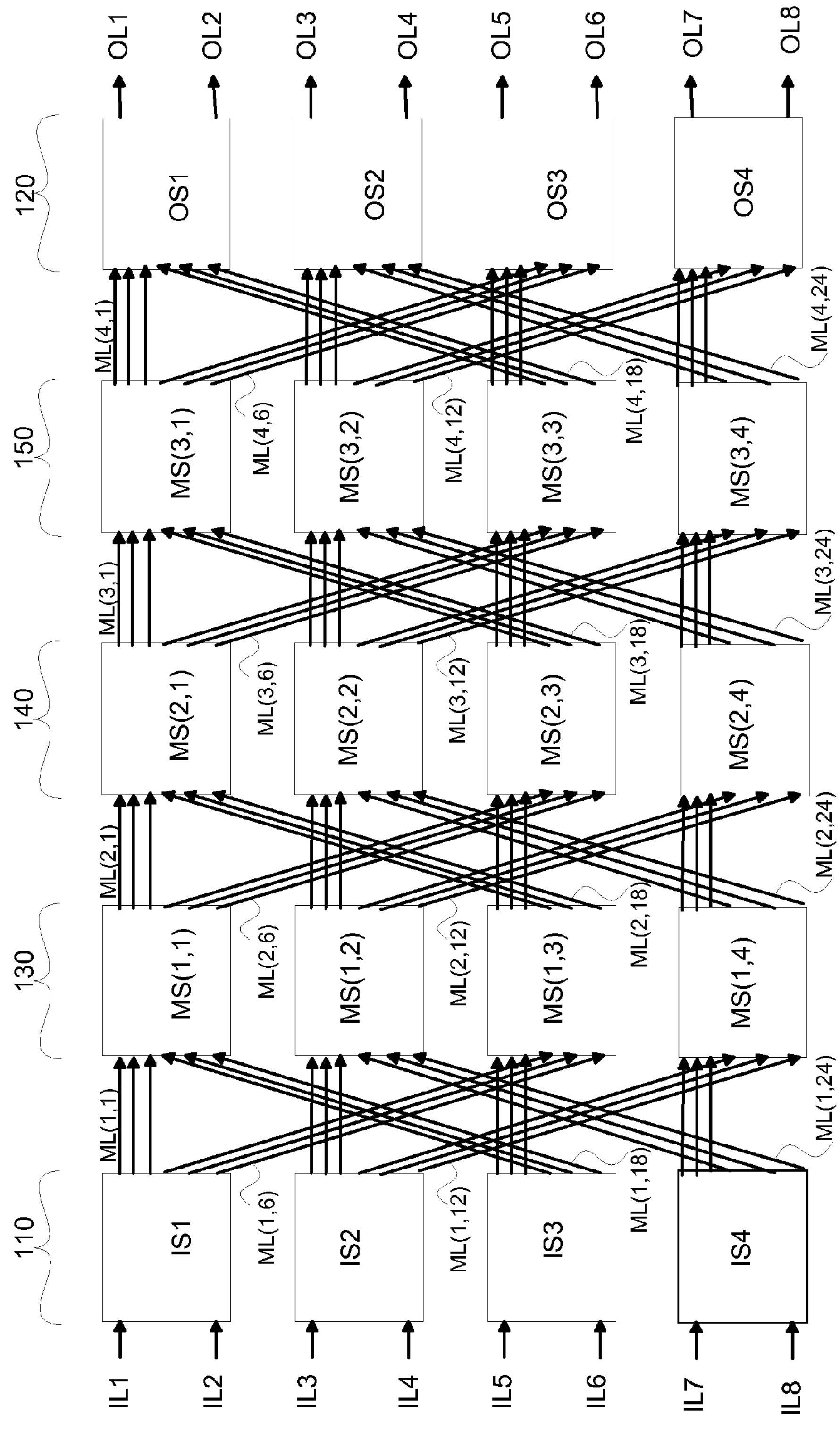

OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
120
OS1
OS2
OS3
OS4
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)
150
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
140
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
130
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
110
IS1
IS2
IS3
IS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8

FIG. 3I

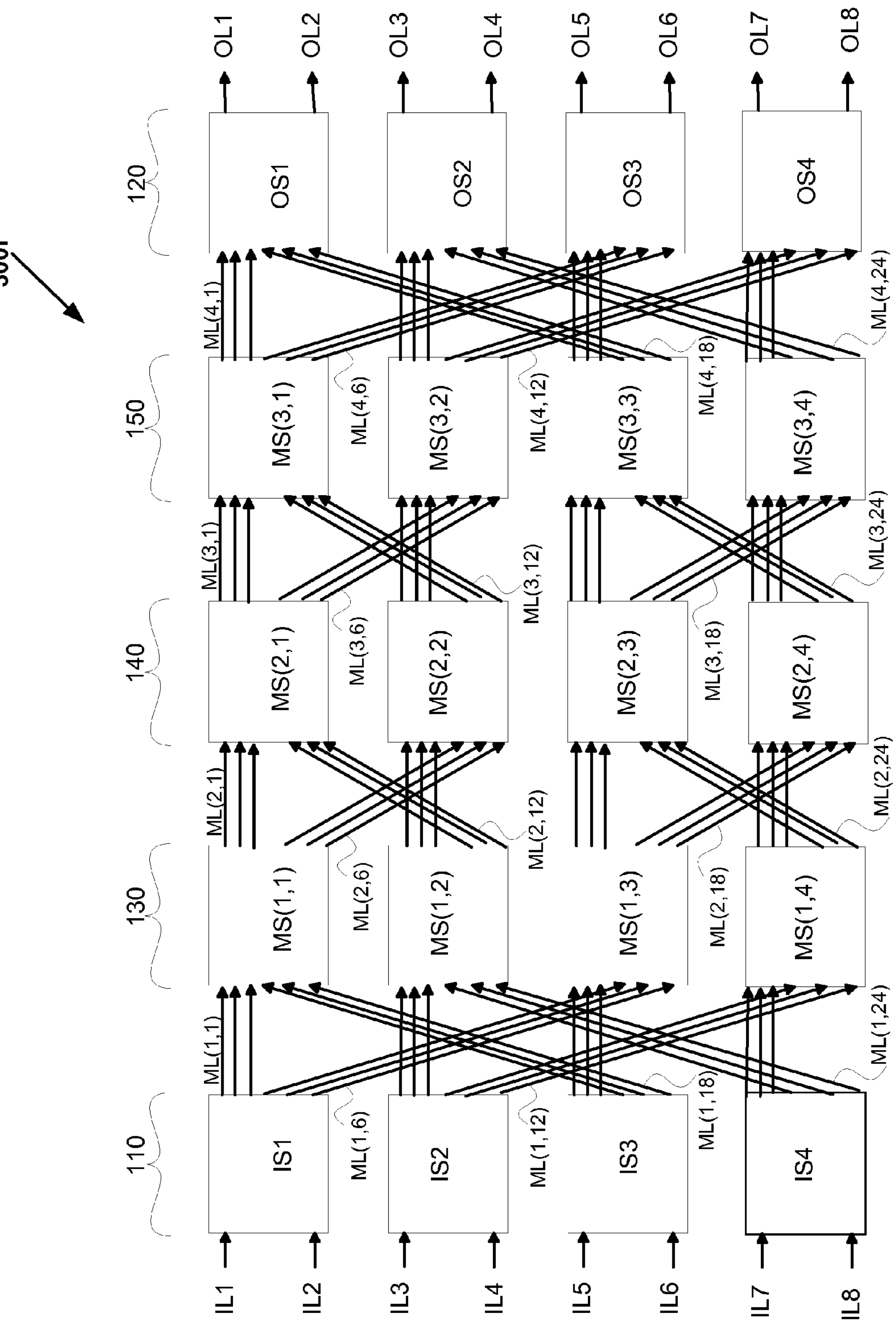
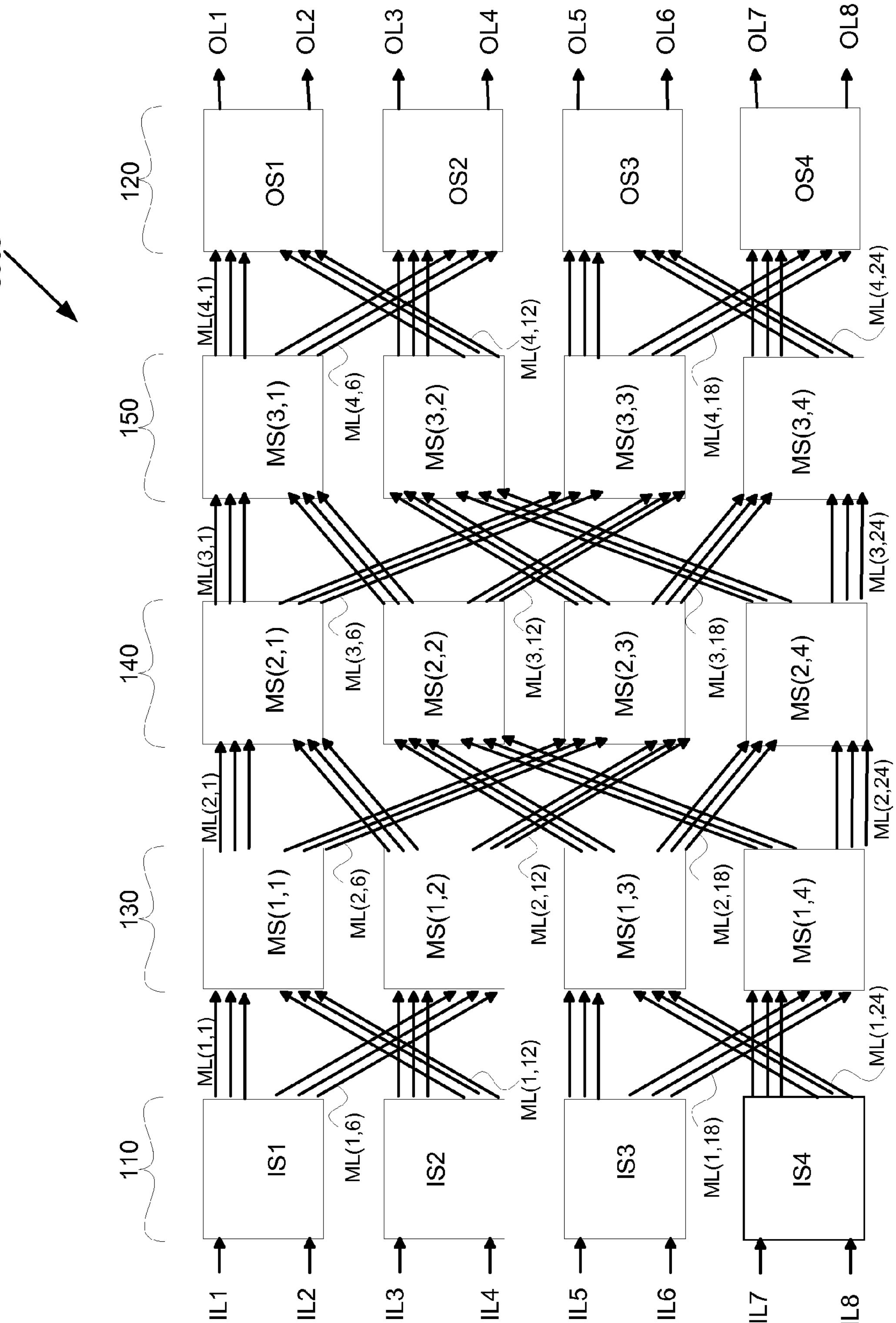

300I
110
120
130
140
150
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)

FIG. 3J


300J
110
130
140
150
120
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
OL1
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OL7
OL8
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)

300K

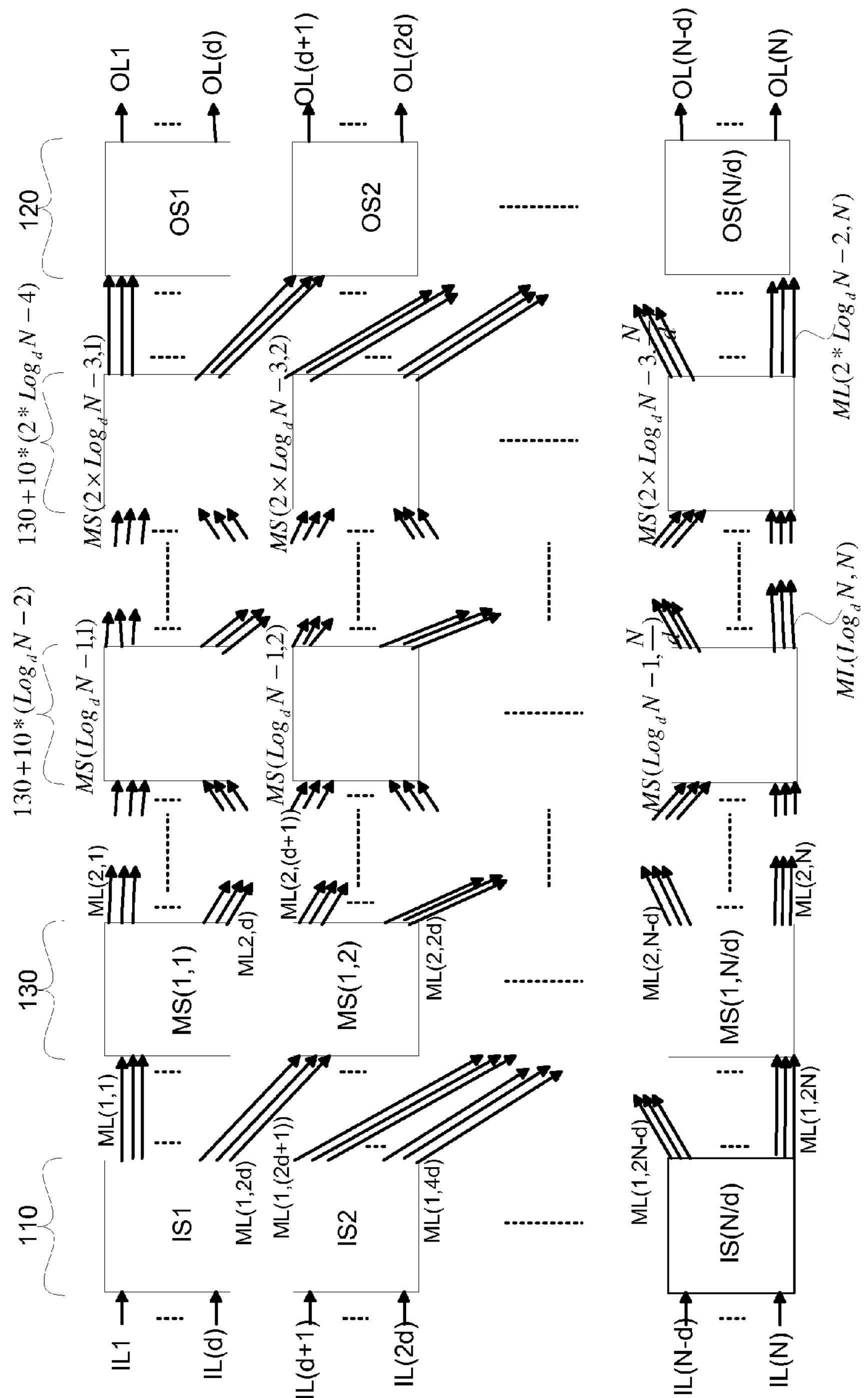
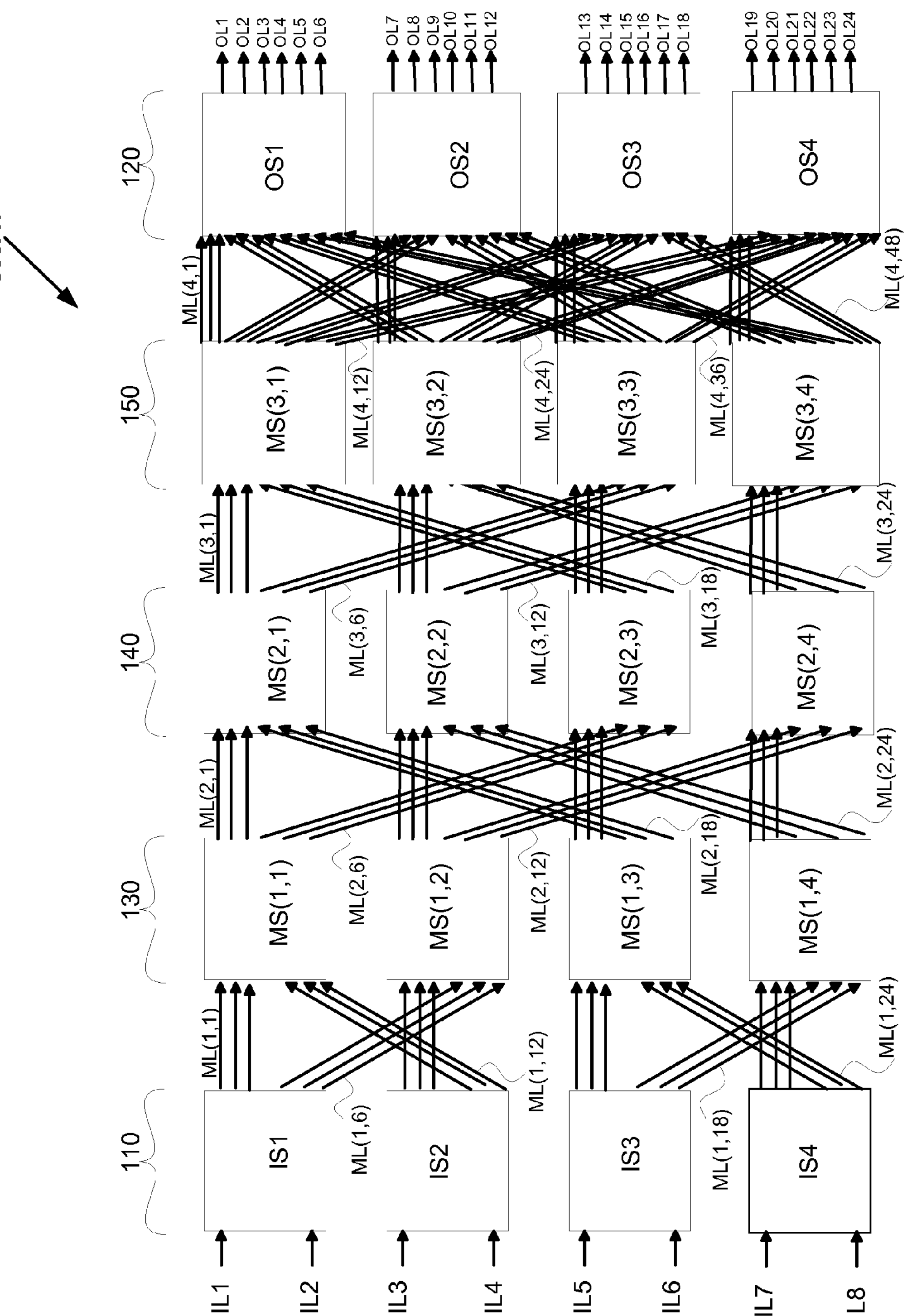

110
130
120
IS1
IS2
IS(N/d)
MS(1,1)
MS(1,2)
MS(1,N/d)
OS1
OS2
OS(N/d)
IL1
IL(d)
IL(d+1)
IL(2d)
IL(N-d)
IL(N)
OL1
OL(d)
OL(d+1)
OL(2d)
OL(N-d)
OL(N)
ML(1,1)
ML(1,2d)
ML(1,(2d+1))
ML(1,4d)
ML(1,2N-d)
ML(1,2N)
ML(2,1)
ML2,d)
ML(2,(d+1))
ML(2,2d)
ML(2,N-d)
ML(2,N)

FIG. 3K


300A1
110
120
130
140
150
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
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IL5
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IL8
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,12)
ML(4,24)
ML(4,36)
ML(4,48)
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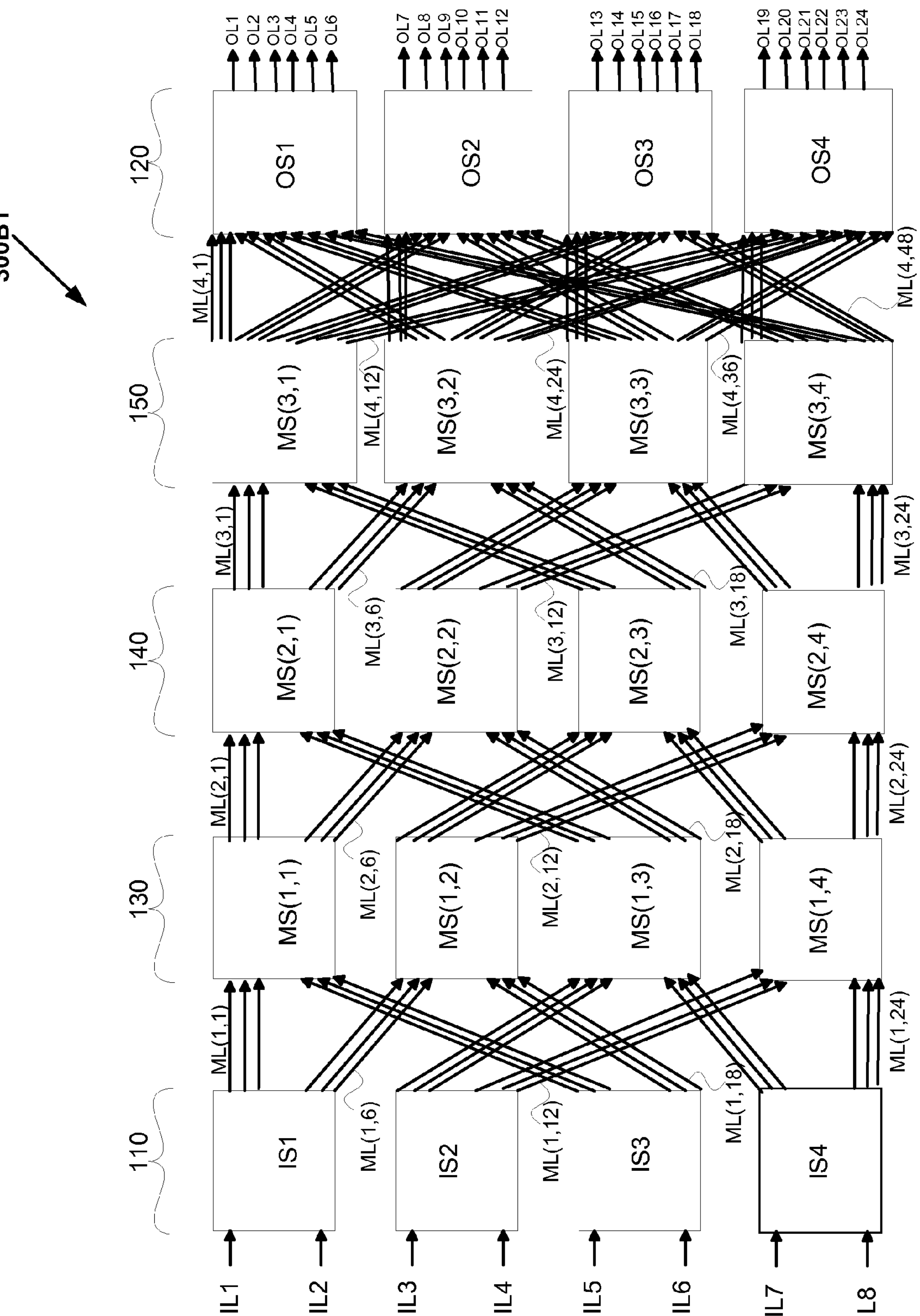
FIG. 3A1

FIG. 3B1


300B1
110
130
140
150
120
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
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ML(1,1)
ML(1,6)
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ML(1,18)
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ML(2,1)
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ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
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ML(4,24)
ML(4,36)
ML(4,48)
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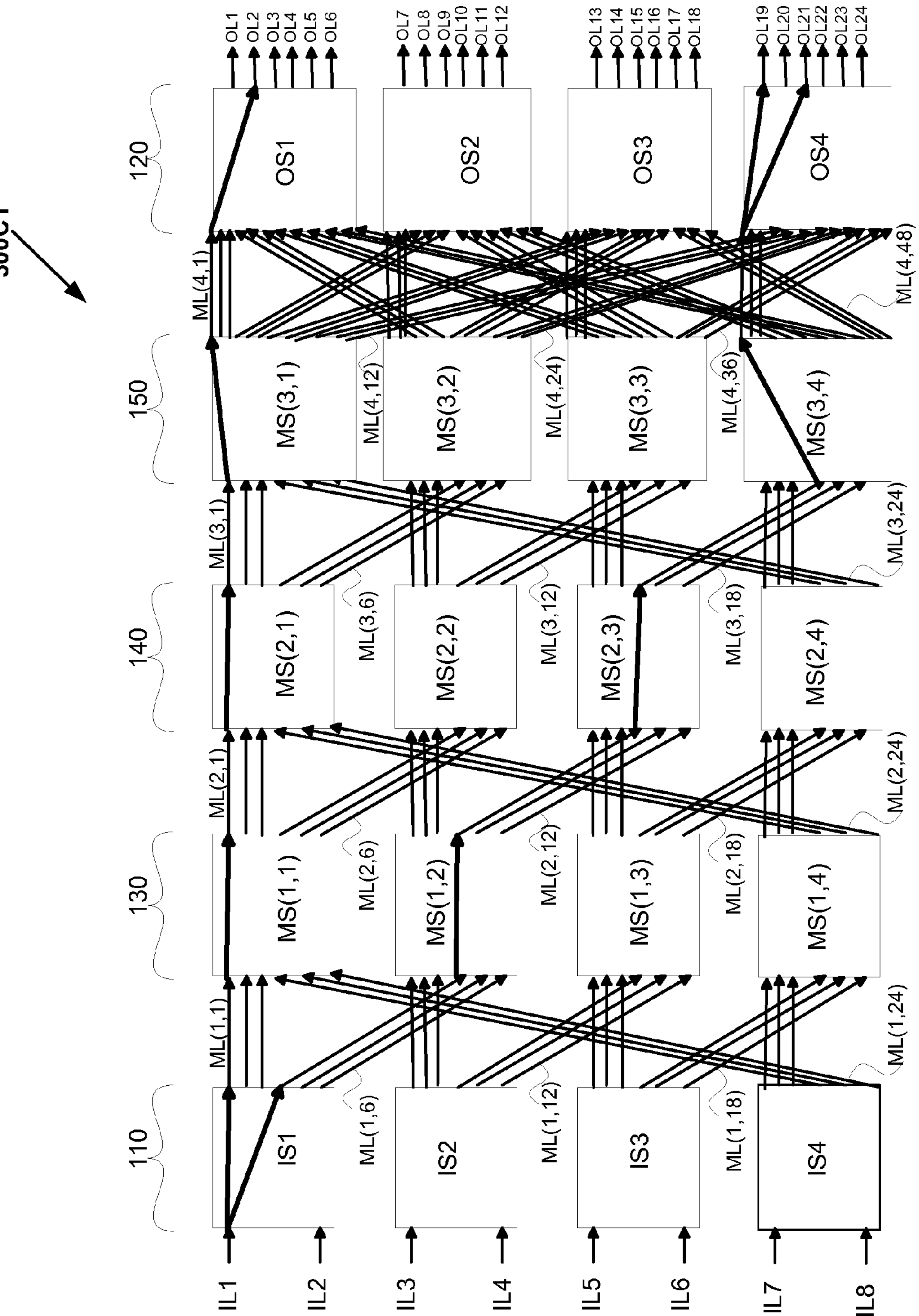
FIG. 3C1


300C1
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130
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IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
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ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1)
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ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,12)
ML(4,24)
ML(4,36)
ML(4,48)
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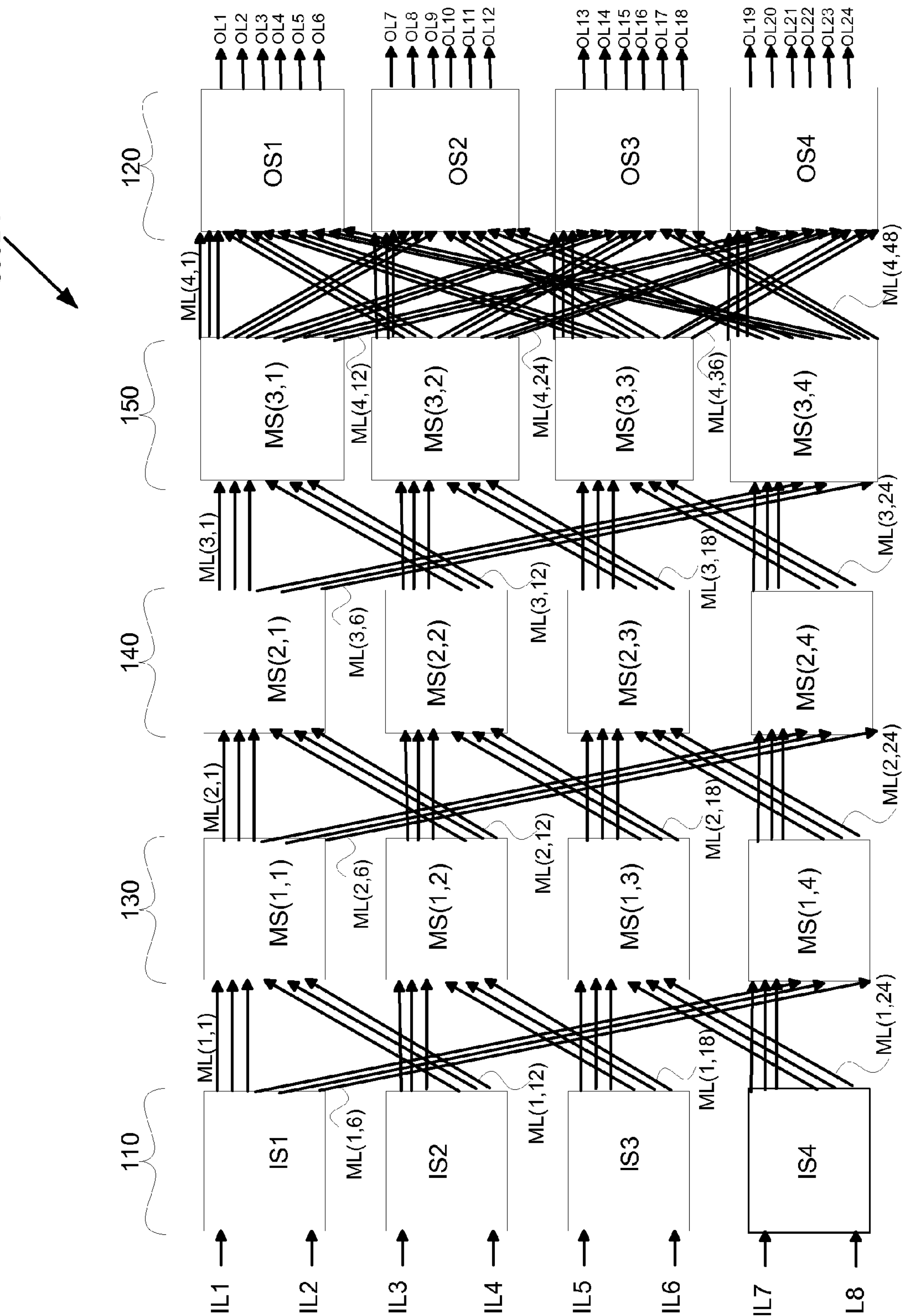
FIG. 3D1


300D1
110
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140
150
120
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
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ML(1,1)
ML(1,6)
ML(1,12)
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ML(1,24)
ML(2,1)
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ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,12)
ML(4,24)
ML(4,36)
ML(4,48)
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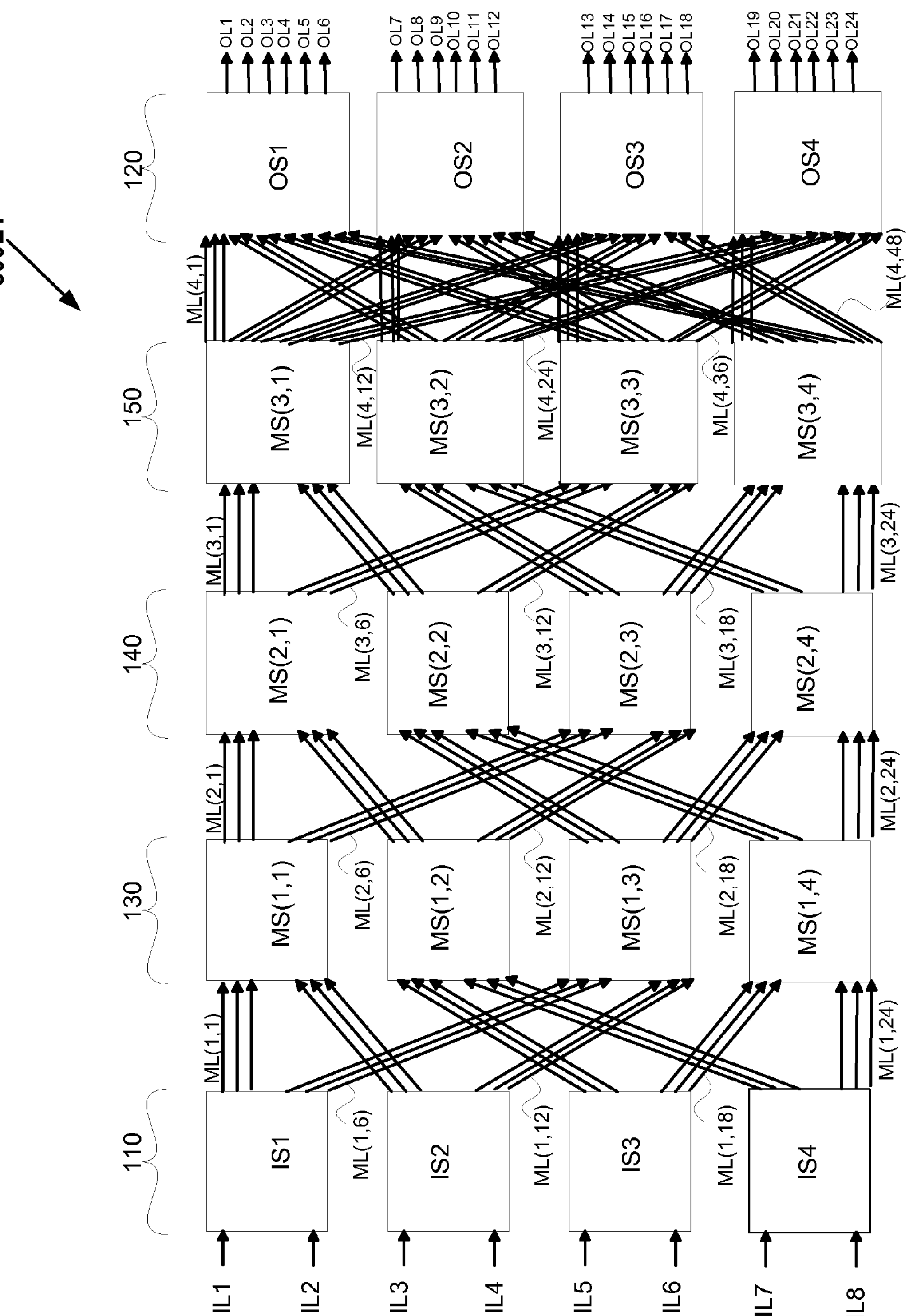
FIG. 3E1


300E1
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
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IL4
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ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
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ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,12)
ML(4,24)
ML(4,36)
ML(4,48)
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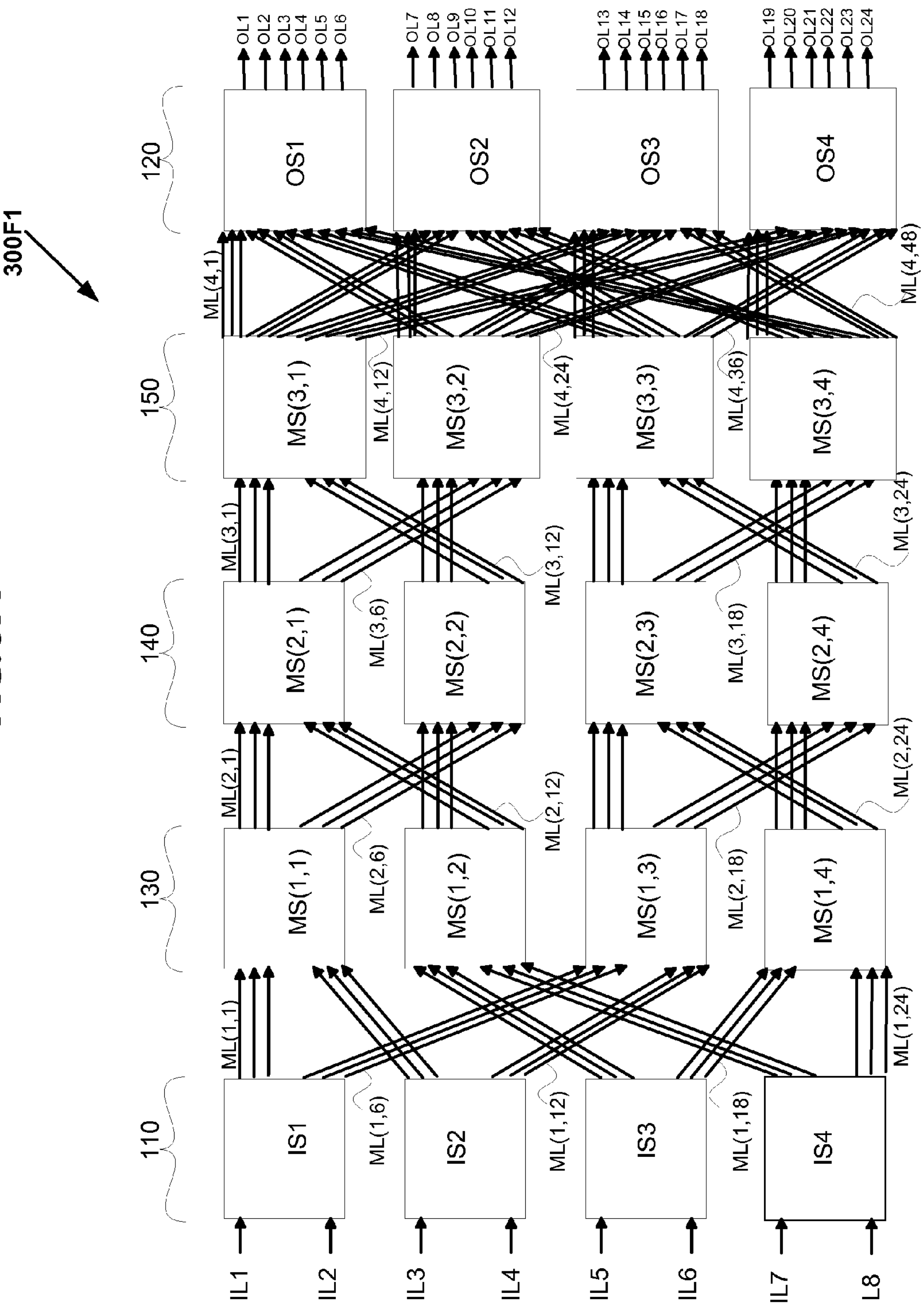
FIG. 3F1



300F1
110
130
140
150
120
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1)
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ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,12)
ML(4,24)
ML(4,36)
ML(4,48)
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FIG. 3G1

300G1

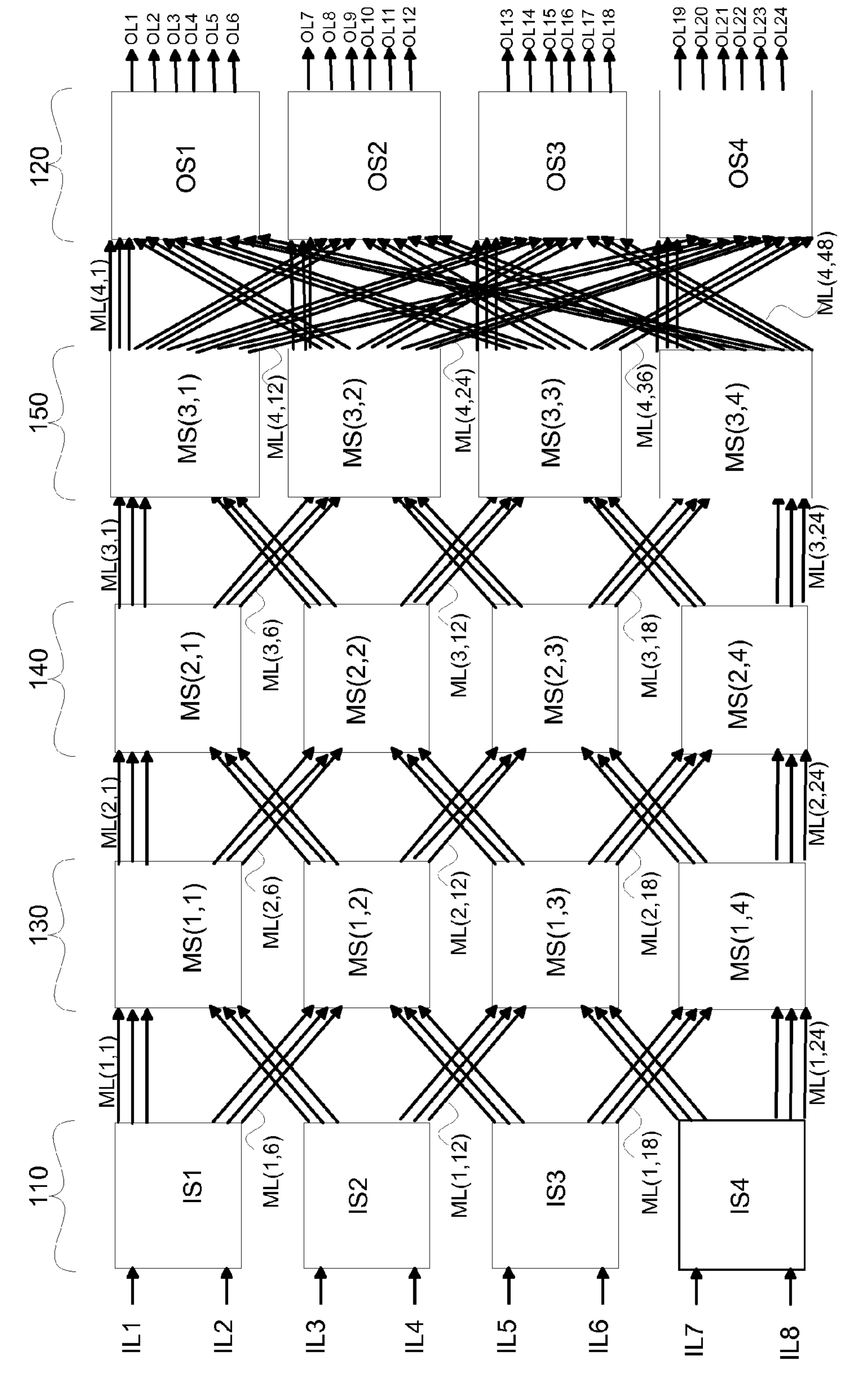

FIG. 3H1

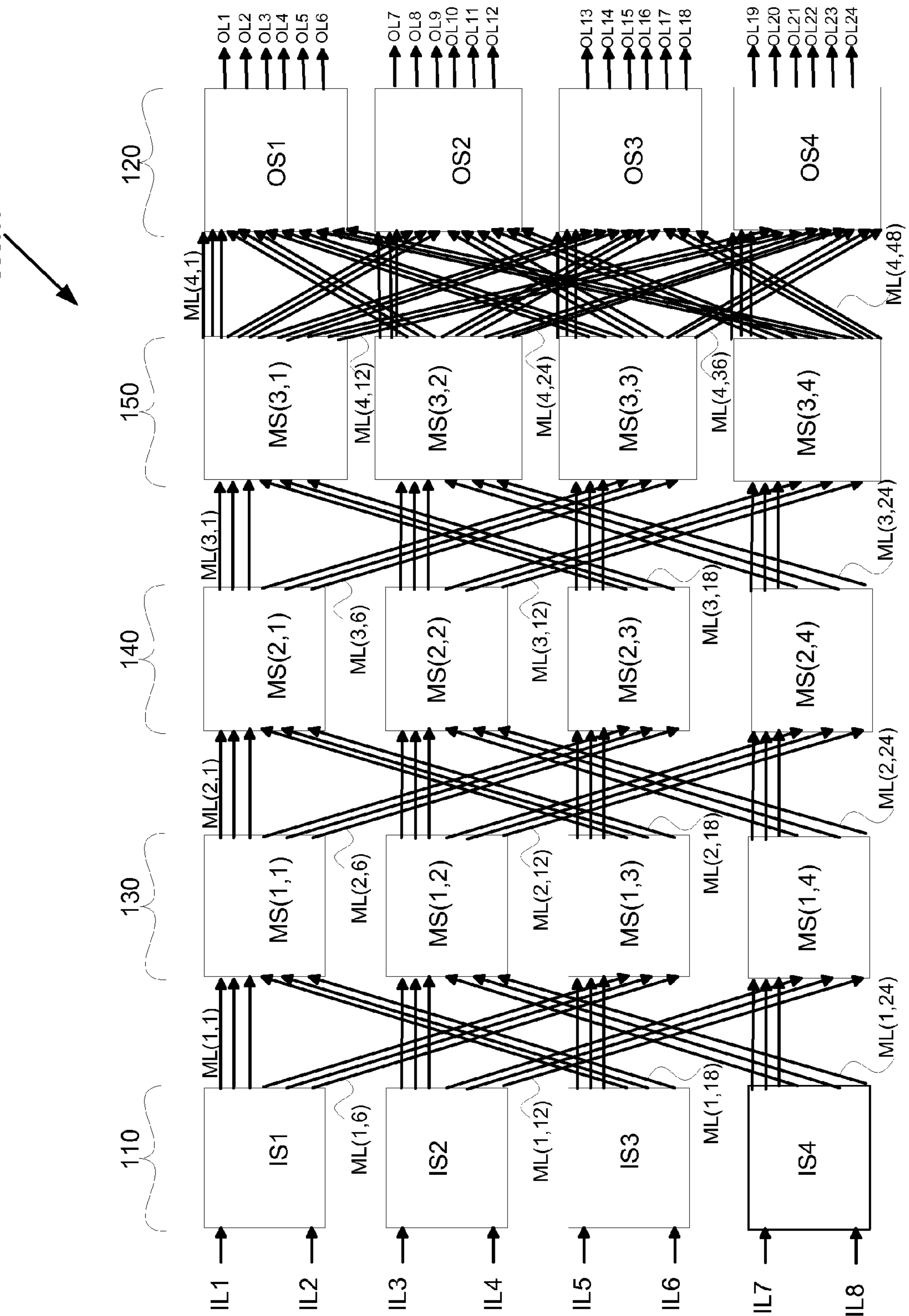
300H1
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,12)
ML(4,24)
ML(4,36)
ML(4,48)
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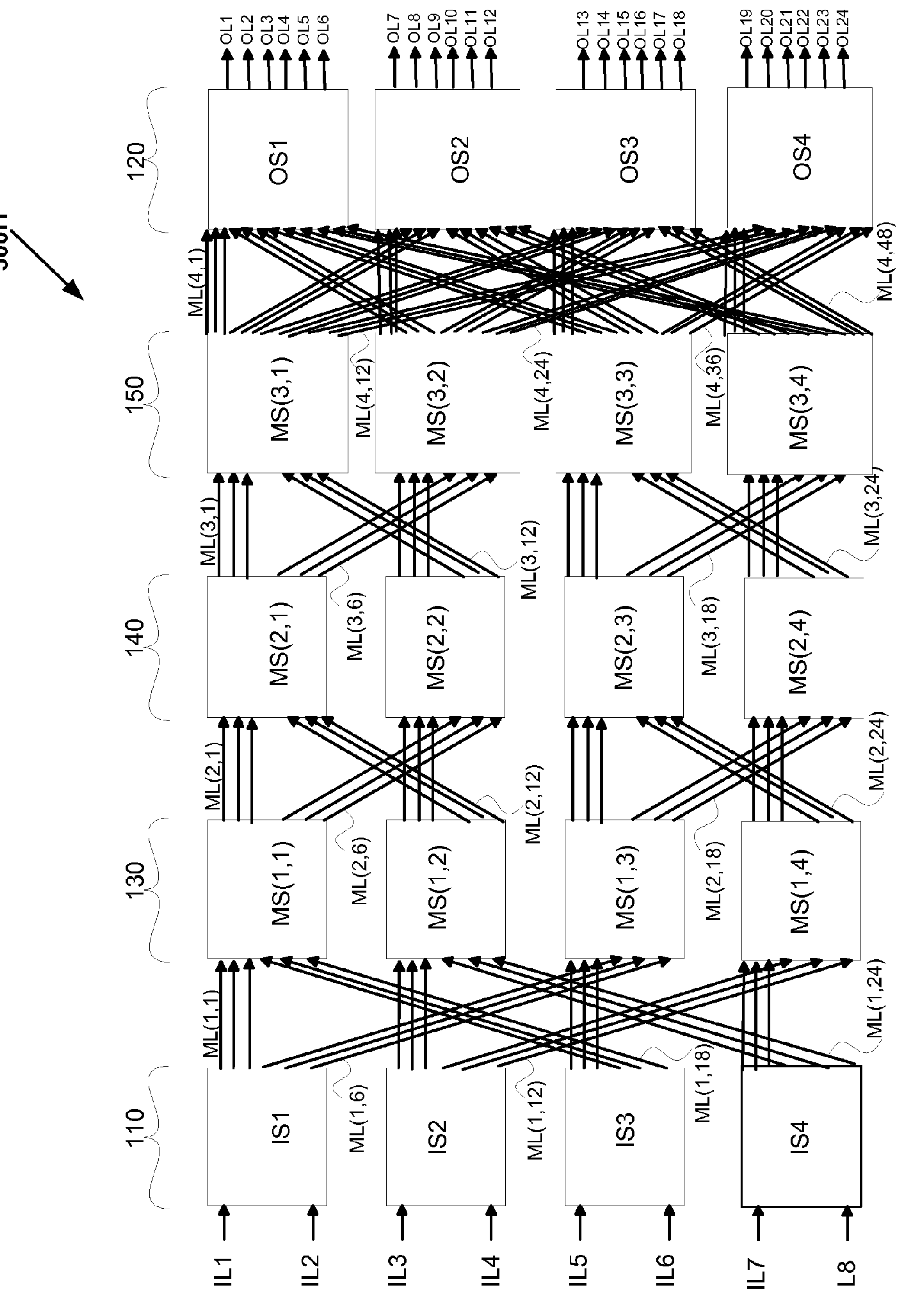
FIG. 3I1


300I1
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130
140
150
120
IS1
IS2
IS3
IS4
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MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
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ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,12)
ML(4,24)
ML(4,36)
ML(4,48)
OL1
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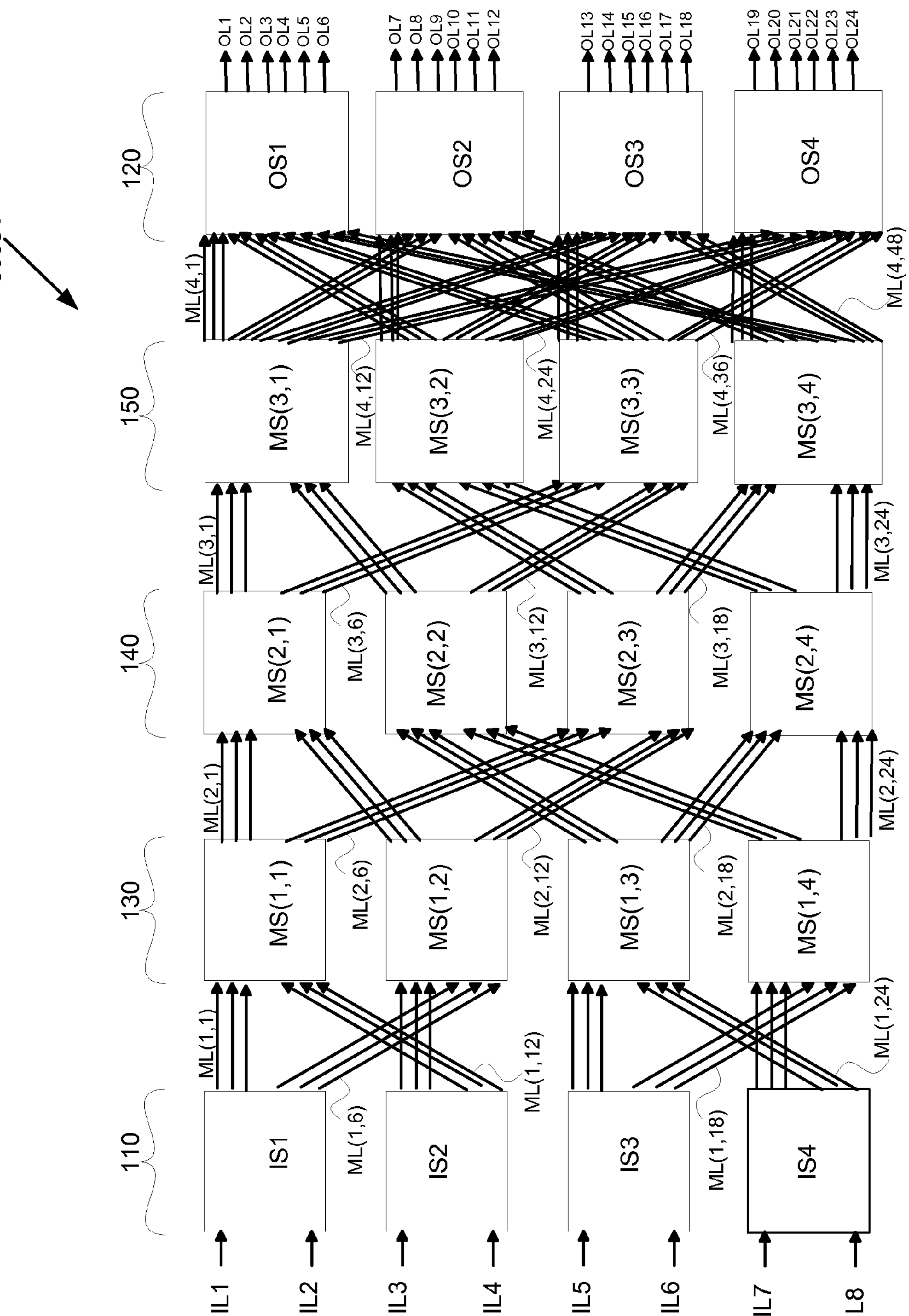
OL24

FIG. 3J1


300J1
110
120
130
140
150
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,12)
ML(4,24)
ML(4,36)
ML(4,48)
OL1
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OL18
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OL20
OL21
OL22
OL23
OL24

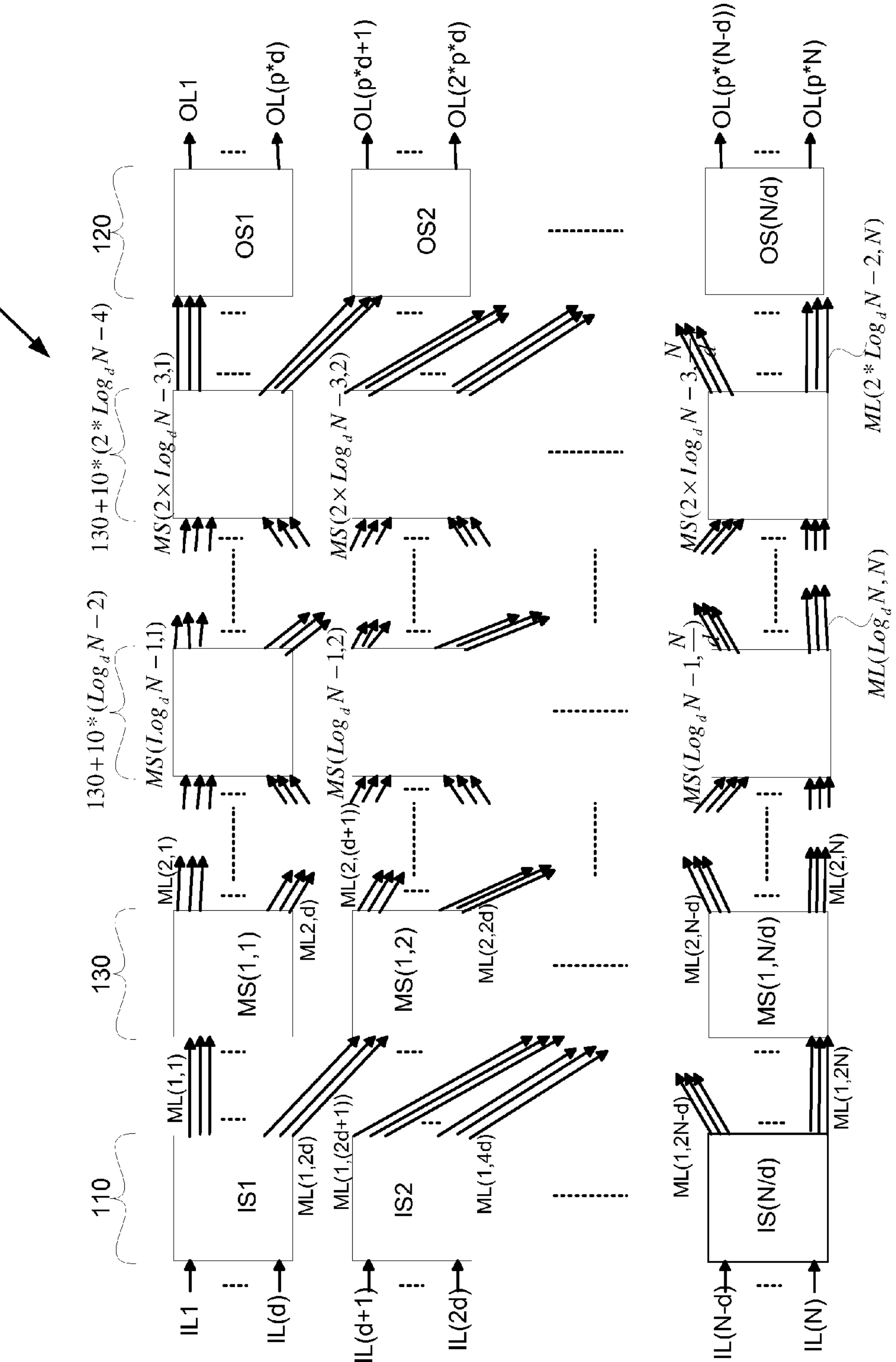

300K1
110
130
120
IL1
IL(d)
IL(d+1)
IL(2d)
IL(N-d)
IL(N)
IS1
IS2
IS(N/d)
ML(1,1)
ML(1,2d)
ML(1,(2d+1))
ML(1,4d)
ML(1,2N-d)
ML(1,2N)
MS(1,1)
MS(1,2)
MS(1,N/d)
ML(2,1)
ML(2,d)
ML(2,(d+1))
ML(2,2d)
ML(2,N-d)
ML(2,N)
130+10*(Log_d N − 2)
MS(Log_d N − 1,1)
MS(Log_d N − 1,2)
ML(Log_d N, N)
130+10*(2*Log_d N − 4)
MS(2×Log_d N − 3,1)
MS(2×Log_d N − 3,2)
ML(2*Log_d N − 2, N)
OS1
OS2
OS(N/d)
OL1
OL(p*d)
OL(p*d+1)
OL(2*p*d)
OL(p*(N-d))
OL(p*N)

FIG. 3K1

FIG. 3A2

300A2

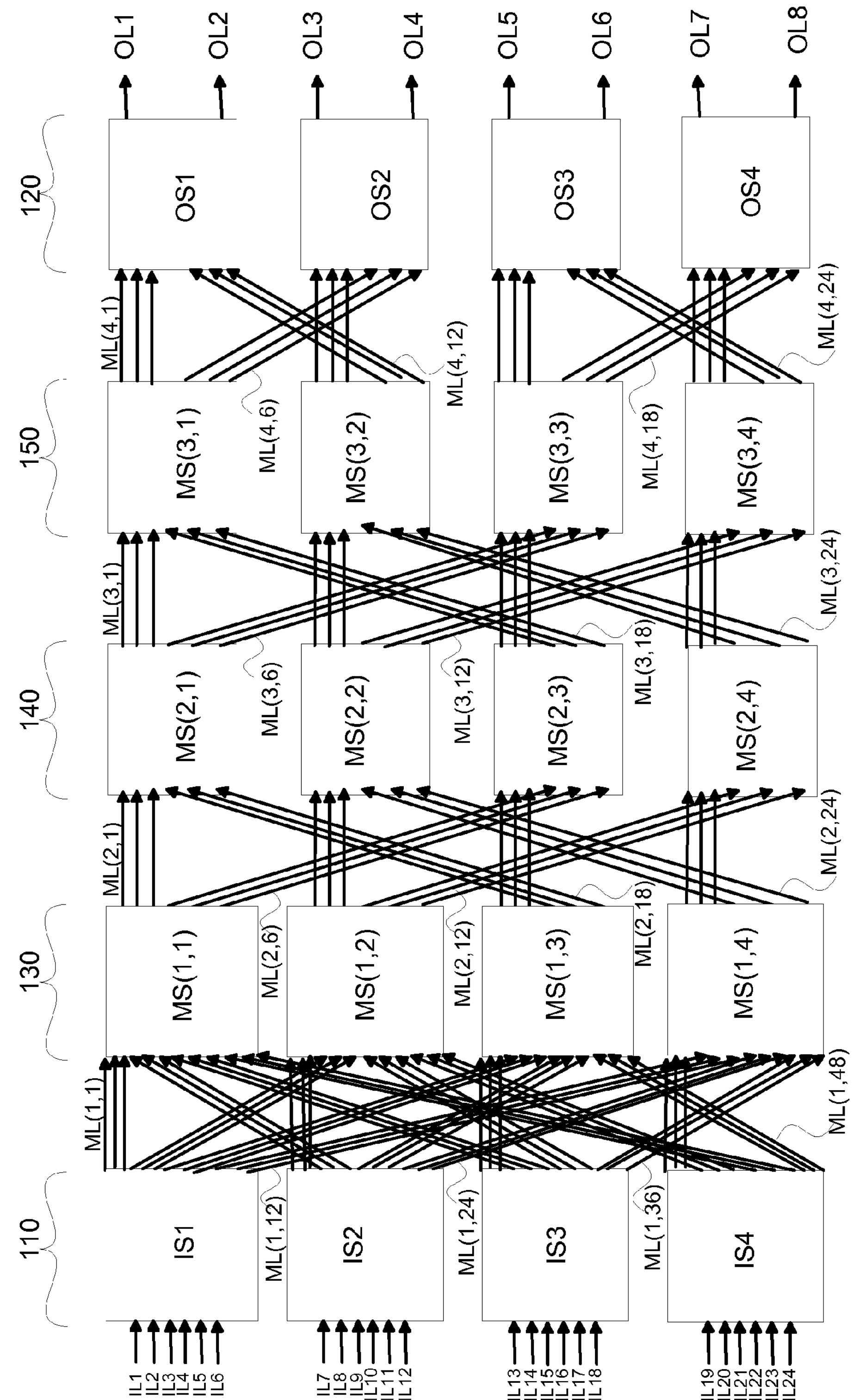


FIG. 3B2

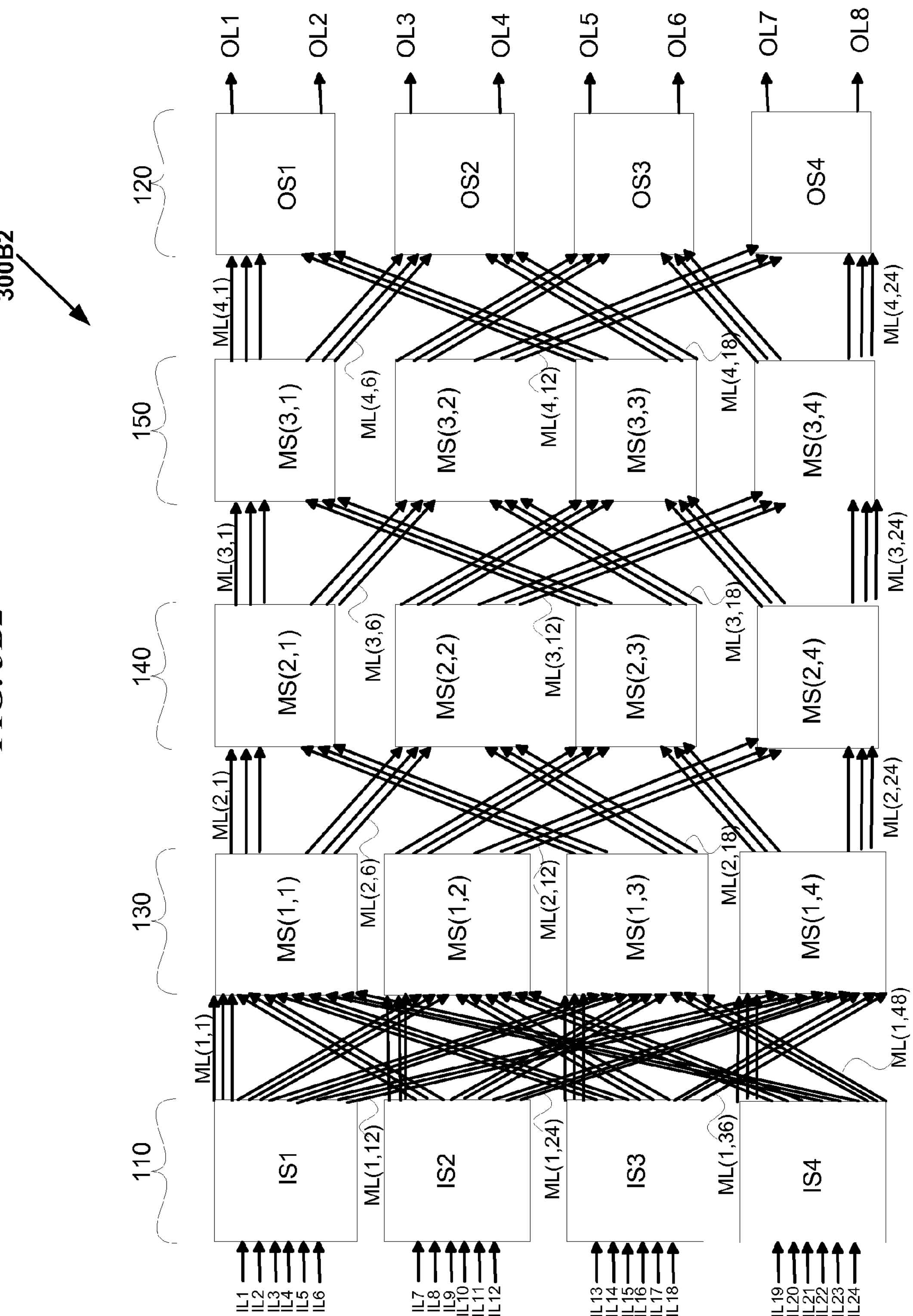
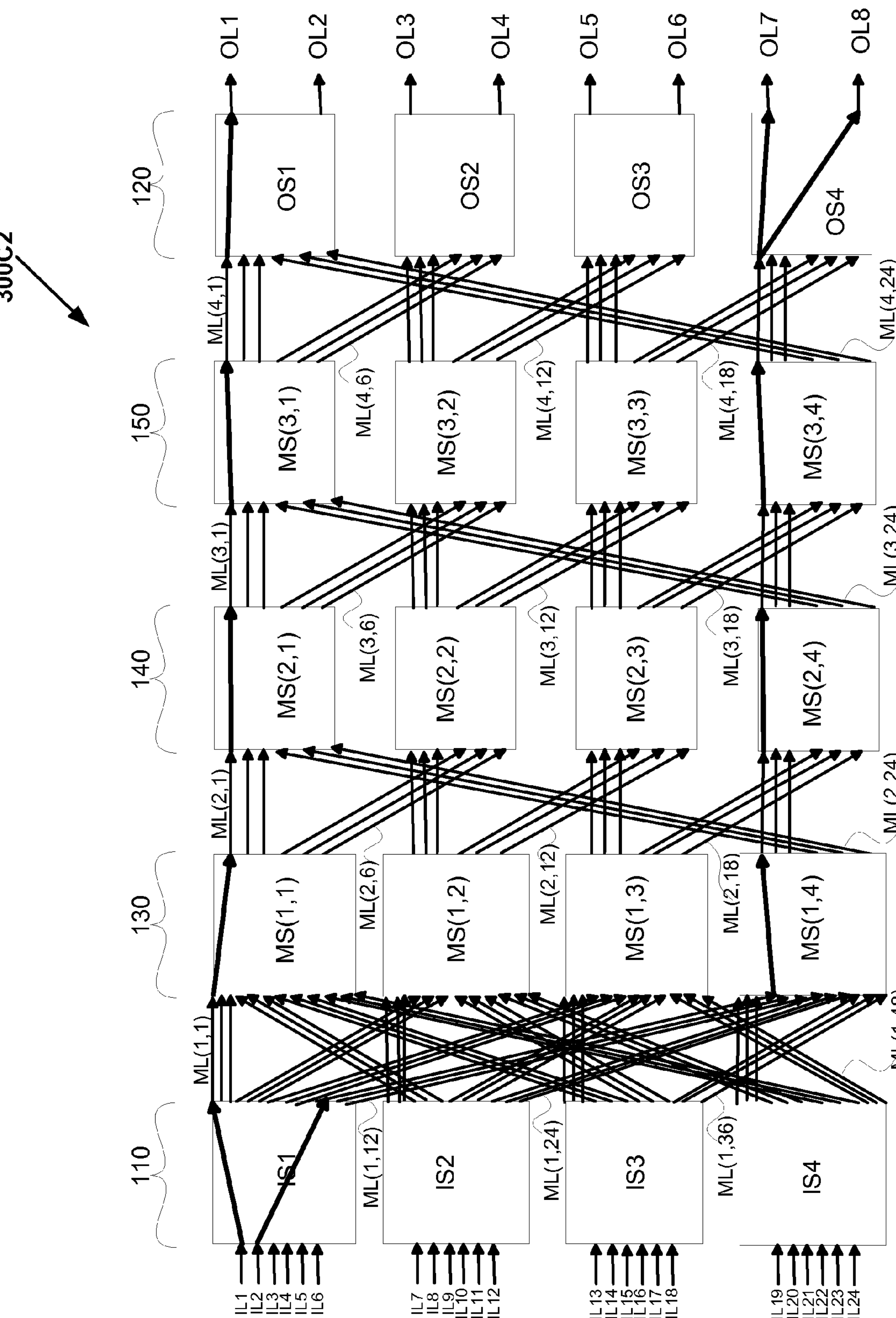

300B2
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
ML(1,1)
ML(1,12)
ML(1,24)
ML(1,36)
ML(1,48)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8

FIG. 3C2


300C2
110
120
130
140
150
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
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OS4
IL1
IL2
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IL20
IL21
IL22
IL23
IL24
OL1
OL2
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OL4
OL5
OL6
OL7
OL8
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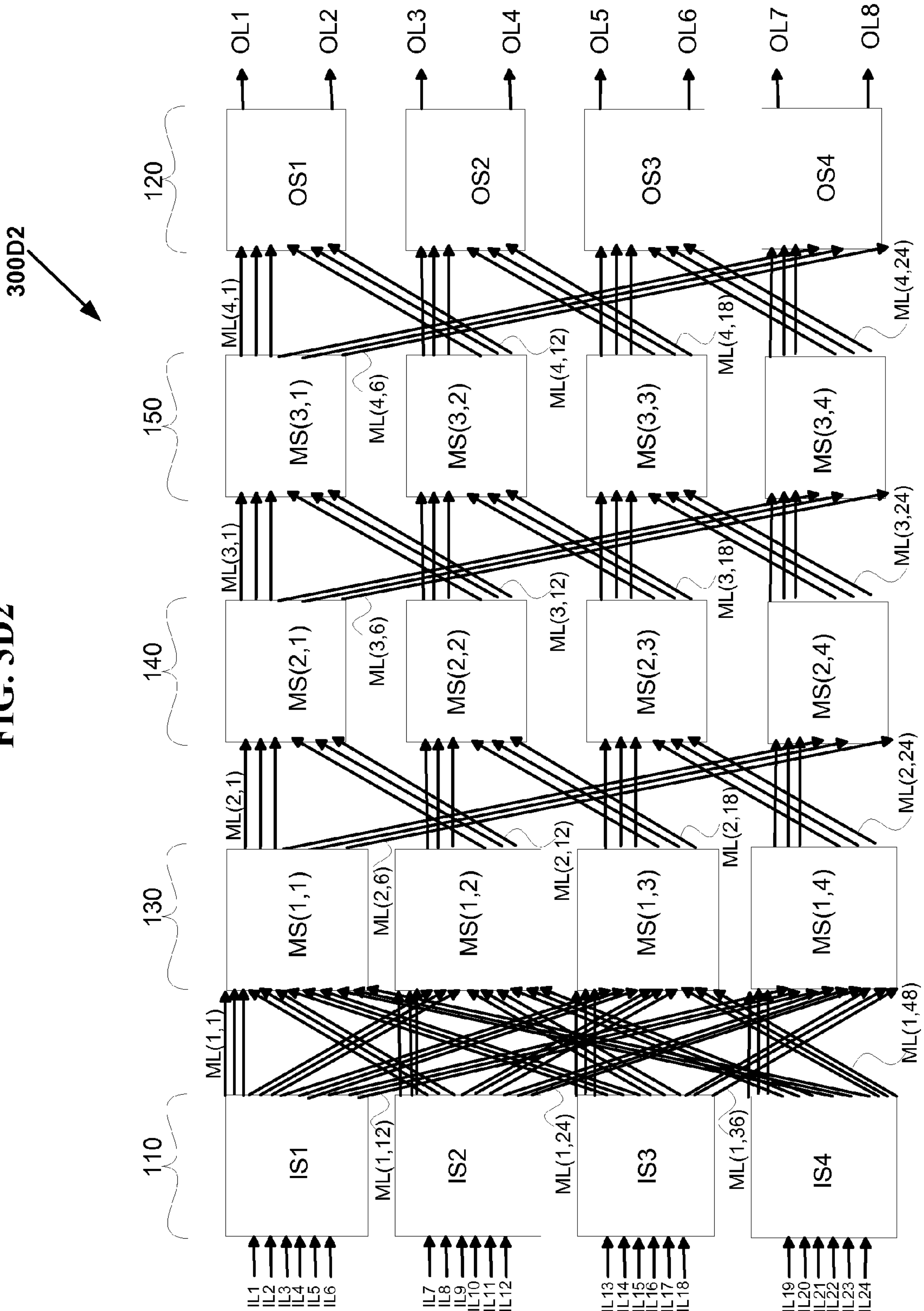
ML(1,24)
ML(1,36)
ML(1,48)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)

FIG. 3D2


300D2
110
120
130
140
150
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IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
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OS4
IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
ML(1,1)
ML(1,12)
ML(1,24)
ML(1,36)
ML(1,48)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8

FIG. 3E2

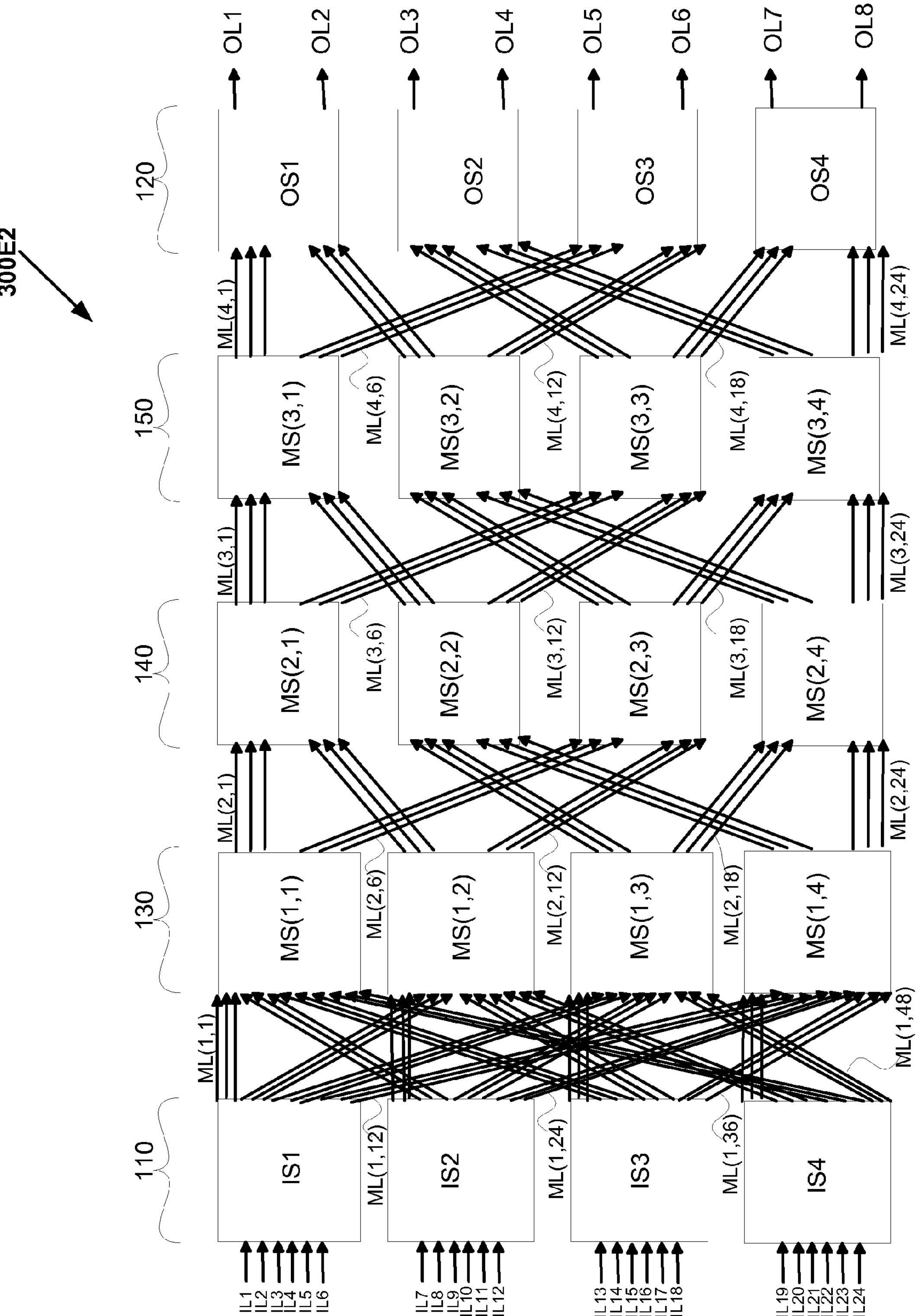

300E2
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
OL1 OL2 OL3 OL4 OL5 OL6 OL7 OL8
ML(1,1)
ML(1,12)
ML(1,24)
ML(1,36)
ML(1,48)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)

FIG. 3F2

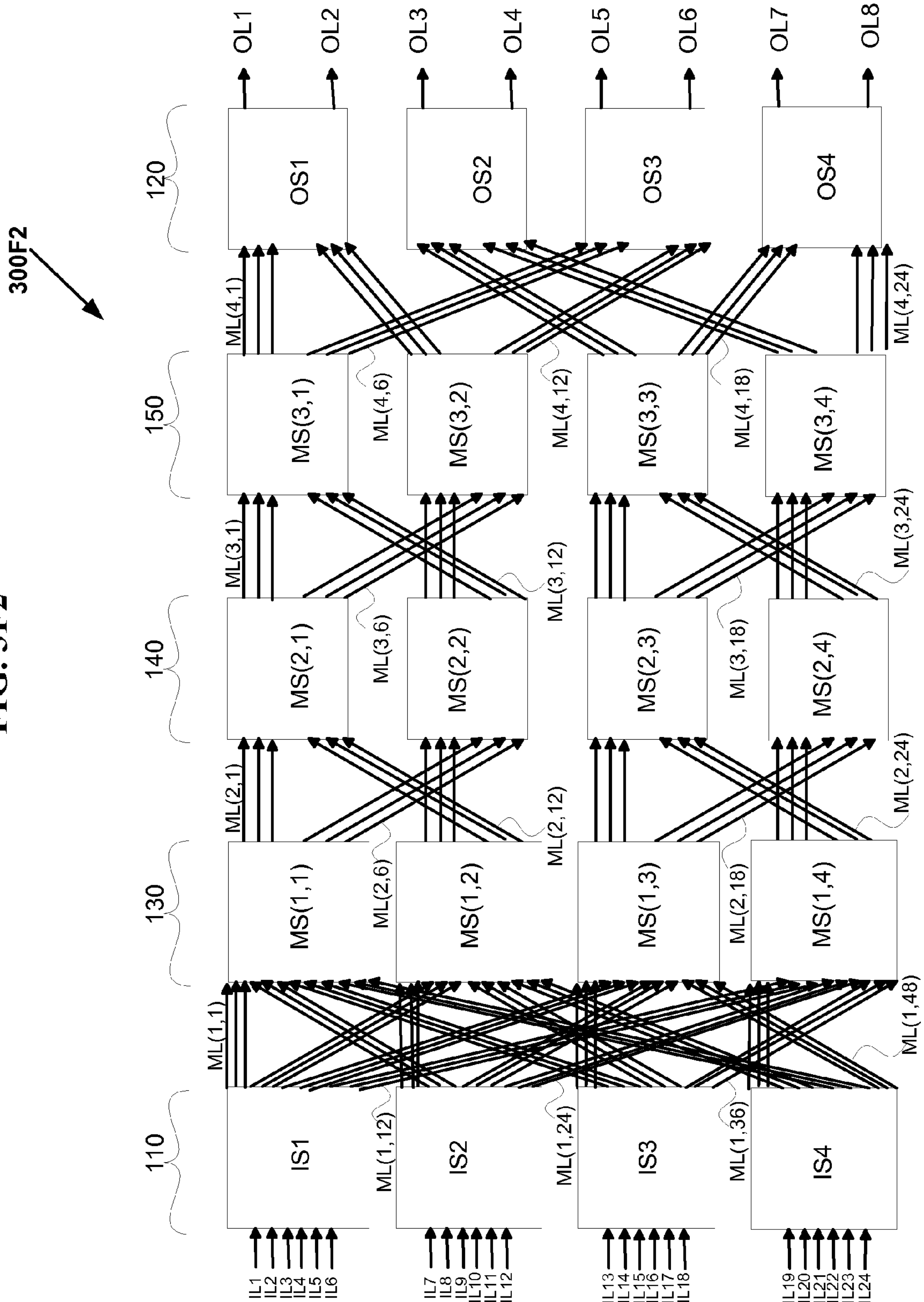
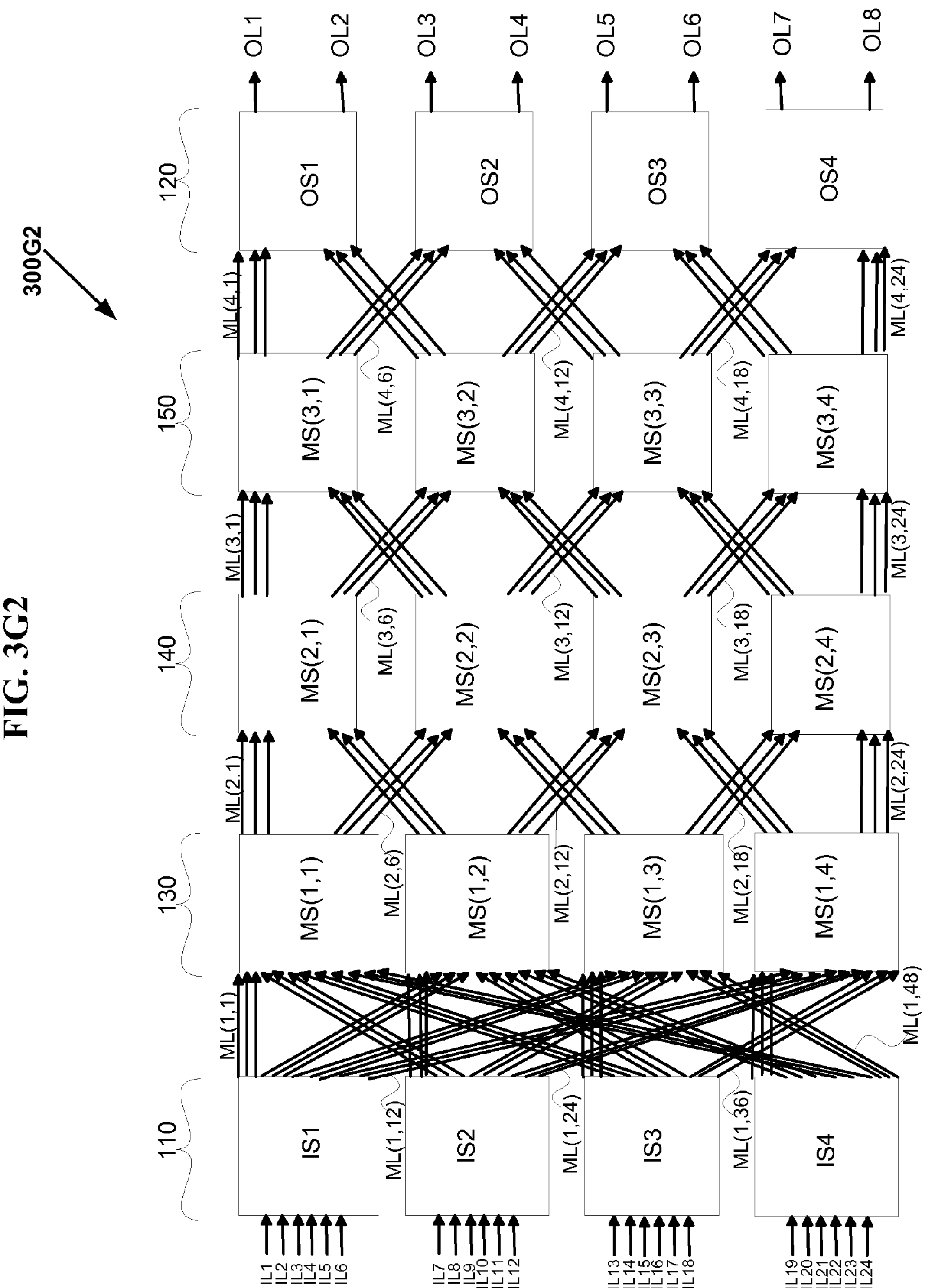

300F2
110
120
130
140
150
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
OL1 OL2 OL3 OL4 OL5 OL6 OL7 OL8
ML(1,1)
ML(1,12)
ML(1,24)
ML(1,36)
ML(1,48)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)

FIG. 3G2


300G2
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
ML(1,1)
ML(1,12)
ML(1,24)
ML(1,36)
ML(1,48)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)

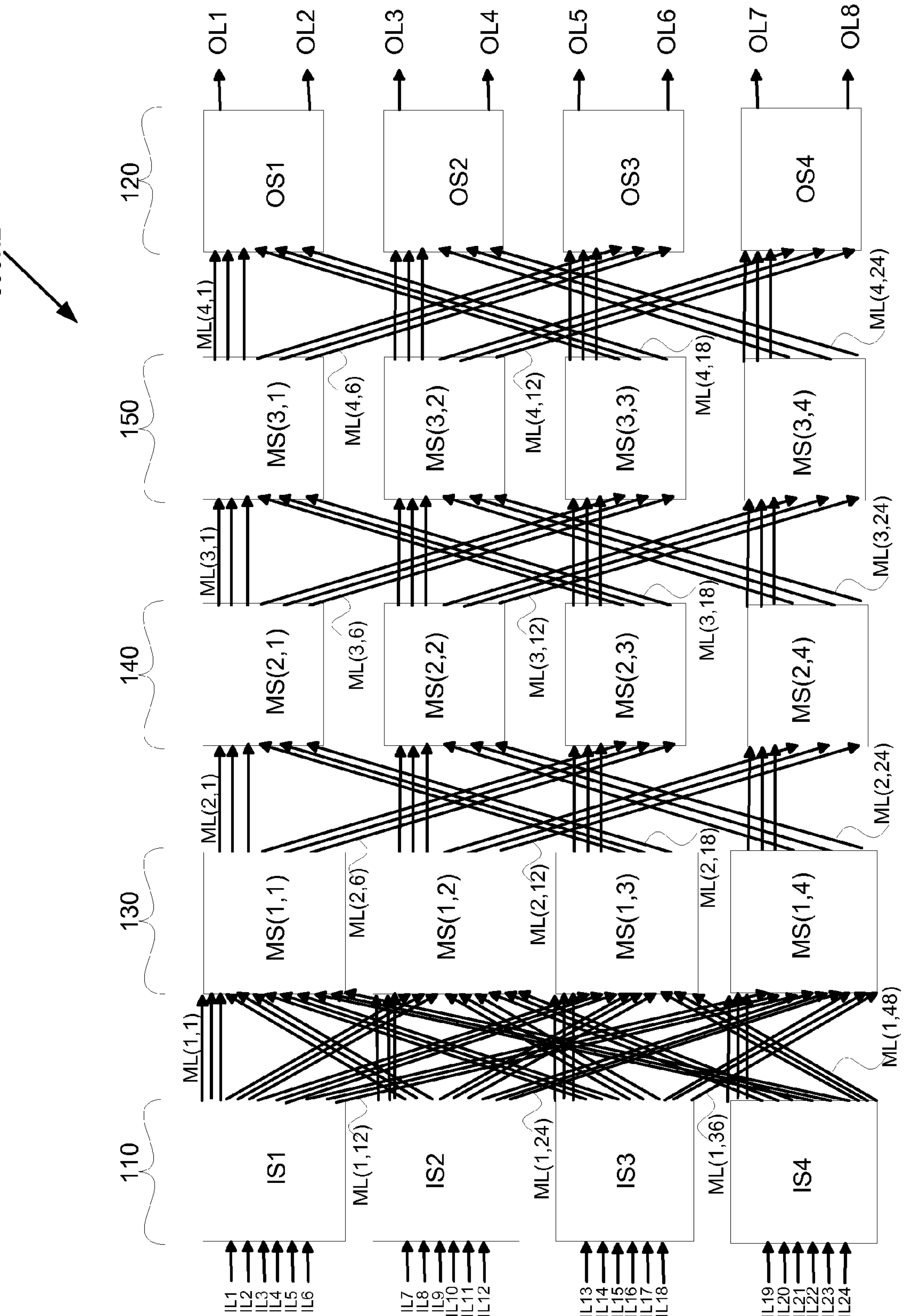

300H2
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
OL1 OL2 OL3 OL4 OL5 OL6 OL7 OL8
ML(1,1)
ML(1,12)
ML(1,24)
ML(1,36)
ML(1,48)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)

FIG. 3H2

FIG. 3I2

300I2

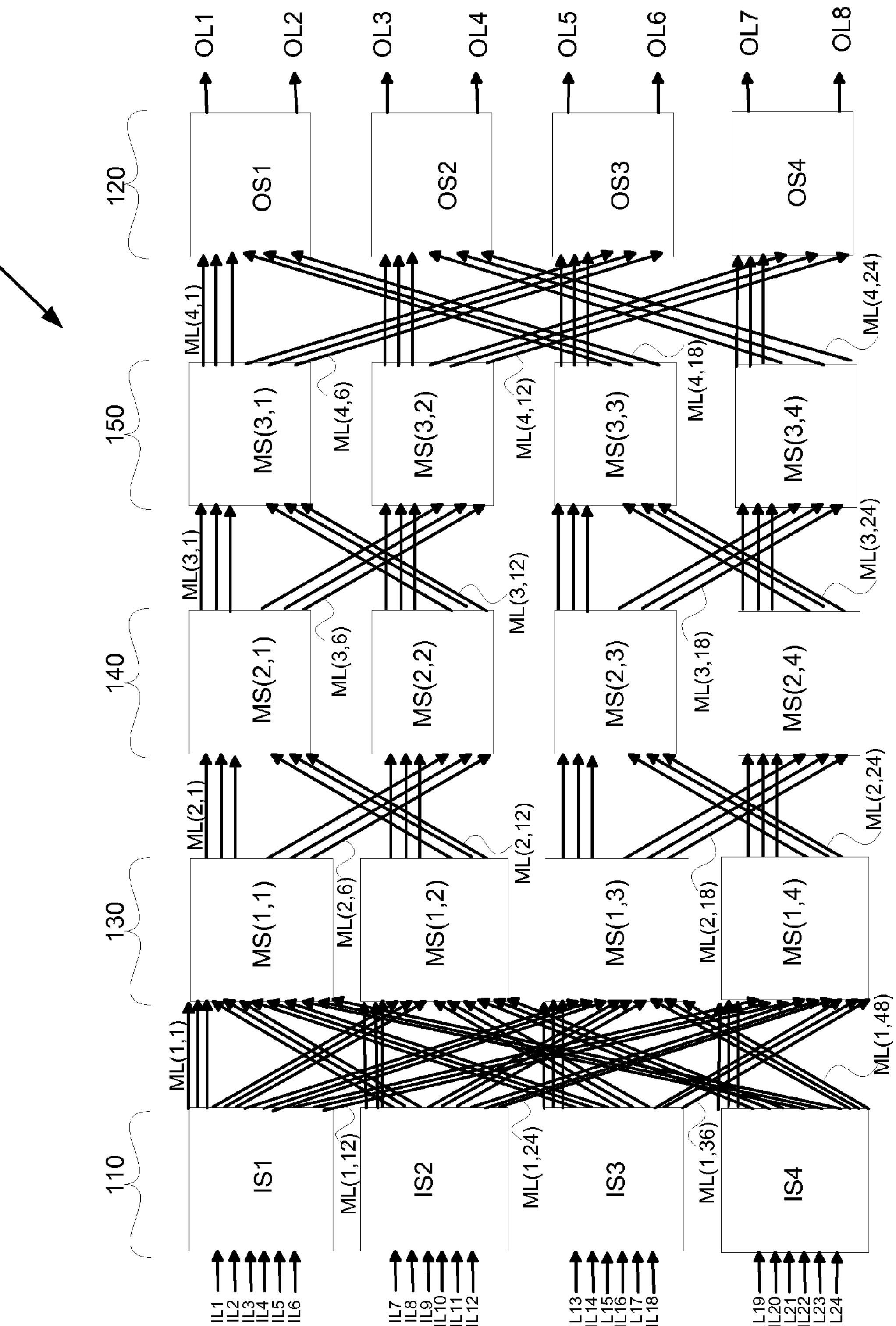
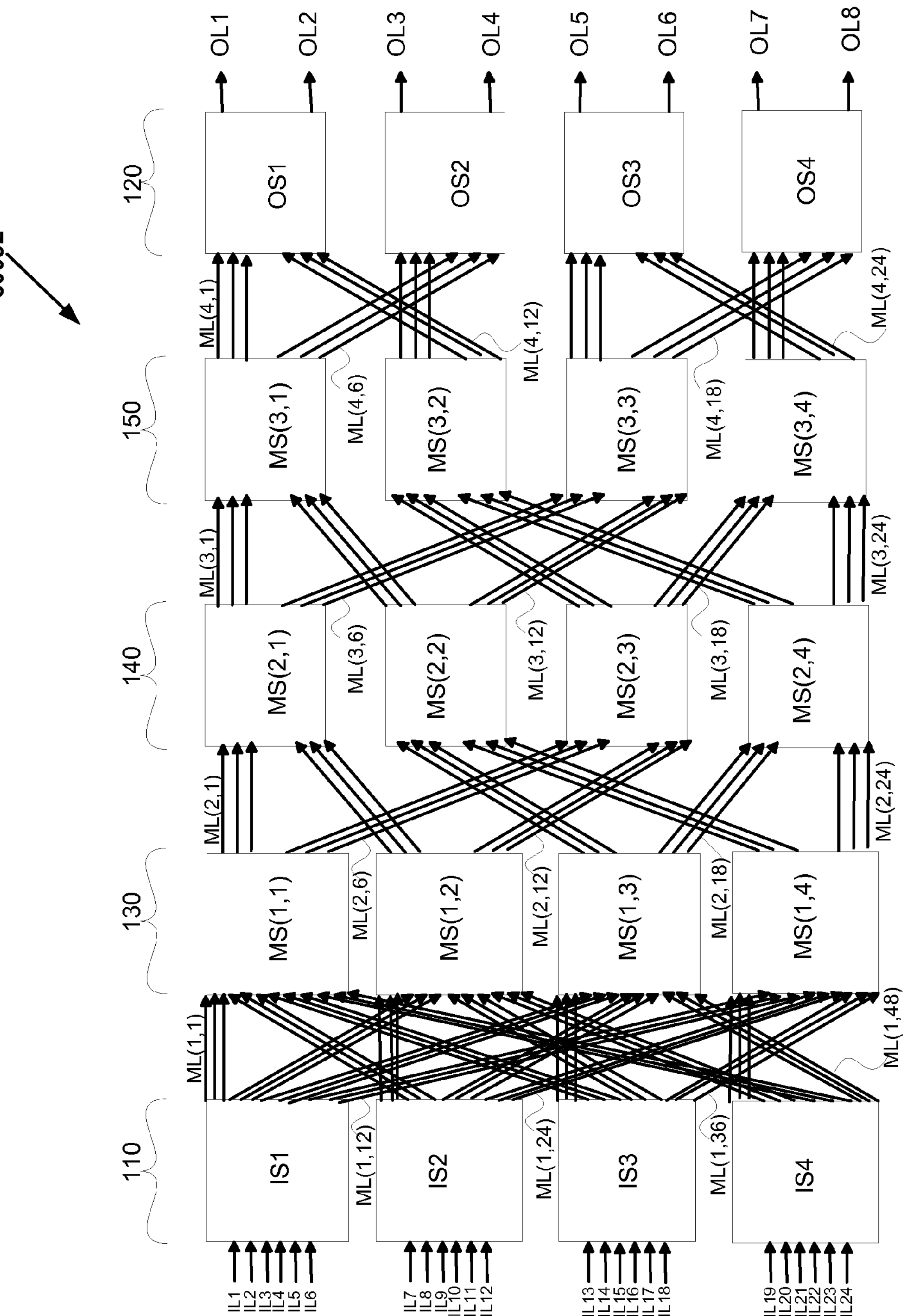


FIG. 3J2


300J2
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
OL1 OL2 OL3 OL4 OL5 OL6 OL7 OL8
ML(1,1)
ML(1,12)
ML(1,24)
ML(1,36)
ML(1,48)
ML(2,1)
ML(2,6)
ML(2,12)
ML(2,18)
ML(2,24)
ML(3,1)
ML(3,6)
ML(3,12)
ML(3,18)
ML(3,24)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)

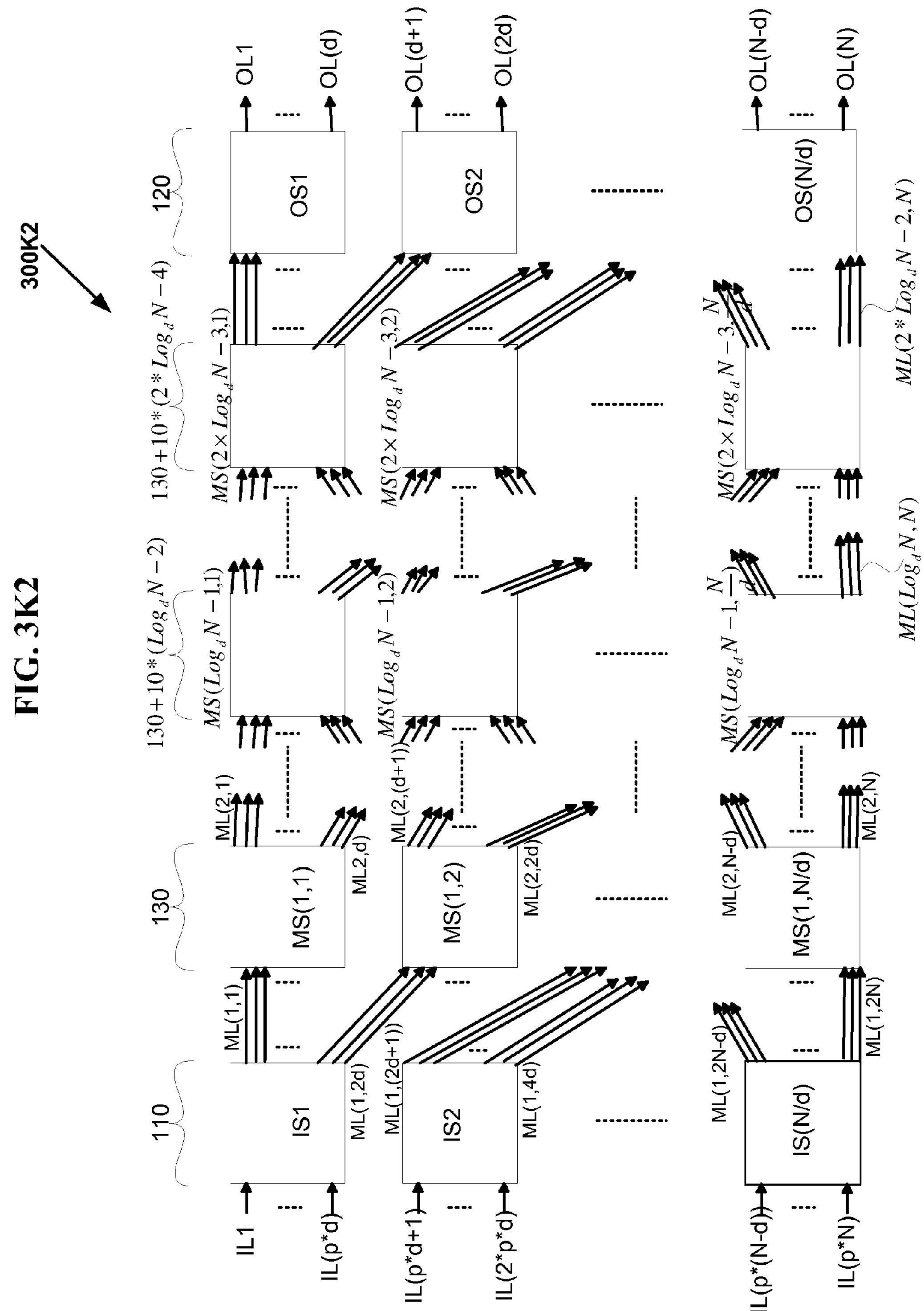
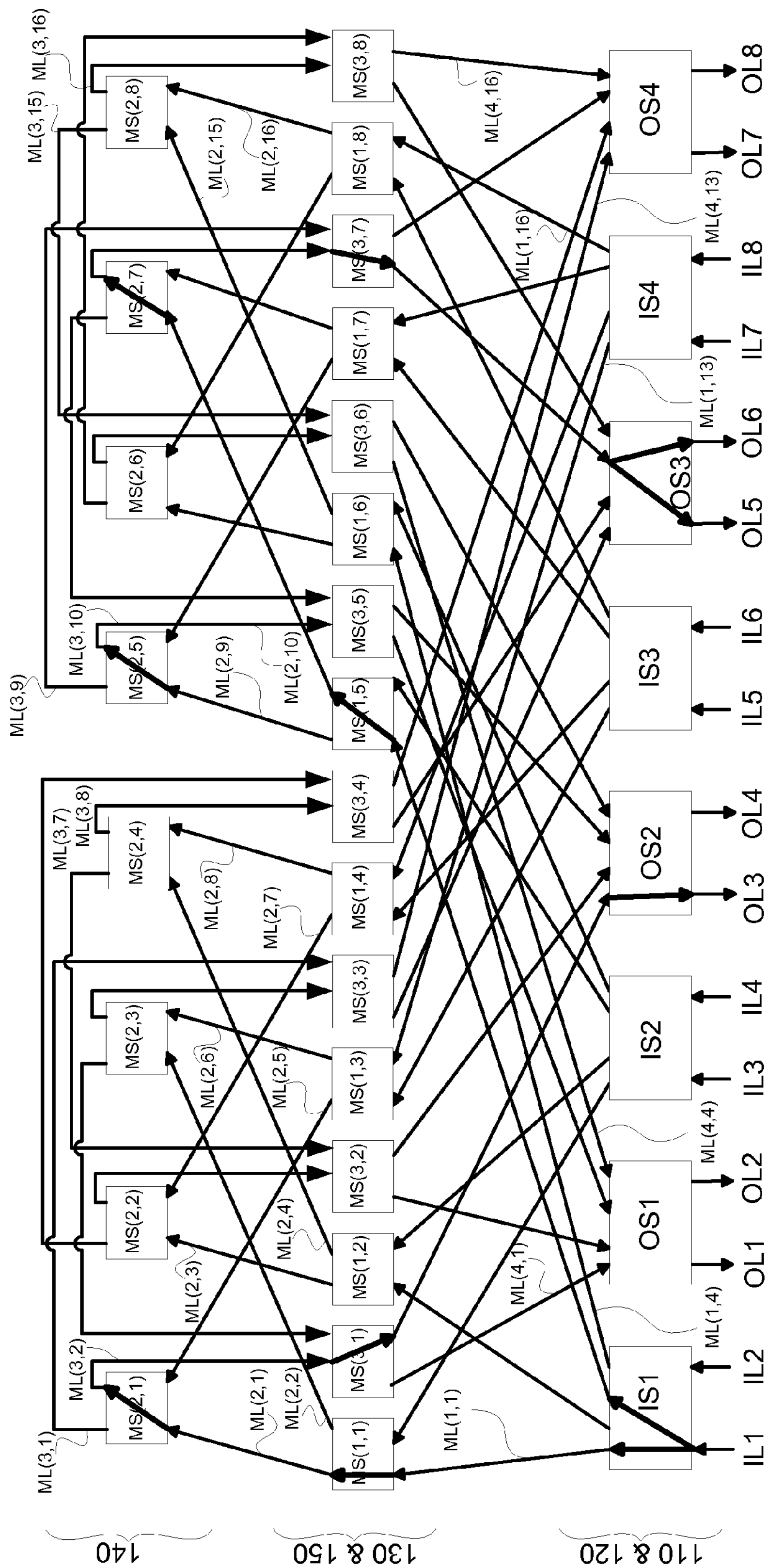

300K2
110
120
130
$130+10*(Log_d N-2)$
$130+10*(2*Log_d N-4)$
IS1
IS2
IS(N/d)
MS(1,1)
MS(1,2)
MS(1,N/d)
$MS(Log_d N-1,1)$
$MS(Log_d N-1,2)$
$MS(Log_d N-1,\frac{N}{d})$
$MS(2\times Log_d N-3,1)$
$MS(2\times Log_d N-3,2)$
$MS(2\times Log_d N-3,\frac{N}{d})$
OS1
OS2
OS(N/d)
IL1
IL(p*d)
IL(p*d+1)
IL(2*p*d)
IL(p*(N-d))
IL(p*N)
ML(1,1)
ML(1,2d)
ML(1,(2d+1))
ML(1,4d)
ML(1,2N-d)
ML(1,2N)
ML(2,1)
ML2,d)
ML(2,(d+1))
ML(2,2d)
ML(2,N-d)
ML(2,N)
$ML(Log_d N,N)$
$ML(2*Log_d N-2,N)$
OL1
OL(d)
OL(d+1)
OL(2d)
OL(N-d)
OL(N)

FIG. 3K2

FIG. 4A

400A



IS1
IS2
IS3
IS4
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(1,5)
MS(1,6)
MS(1,7)
MS(1,8)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(2,5)
MS(2,6)
MS(2,7)
MS(2,8)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
MS(3,5)
MS(3,6)
MS(3,7)
MS(3,8)
ML(1,1)
ML(1,4)
ML(4,1)
ML(4,4)
ML(1,13)
ML(1,16)
ML(4,13)
ML(4,16)
ML(2,1)
ML(2,2)
ML(2,3)
ML(2,4)
ML(2,5)
ML(2,6)
ML(2,7)
ML(2,8)
ML(2,9)
ML(2,10)
ML(2,15)
ML(2,16)
ML(3,1)
ML(3,2)
ML(3,7)
ML(3,8)
ML(3,9)
ML(3,10)
ML(3,15)
ML(3,16)
140
130 & 150
110 & 120

400A1

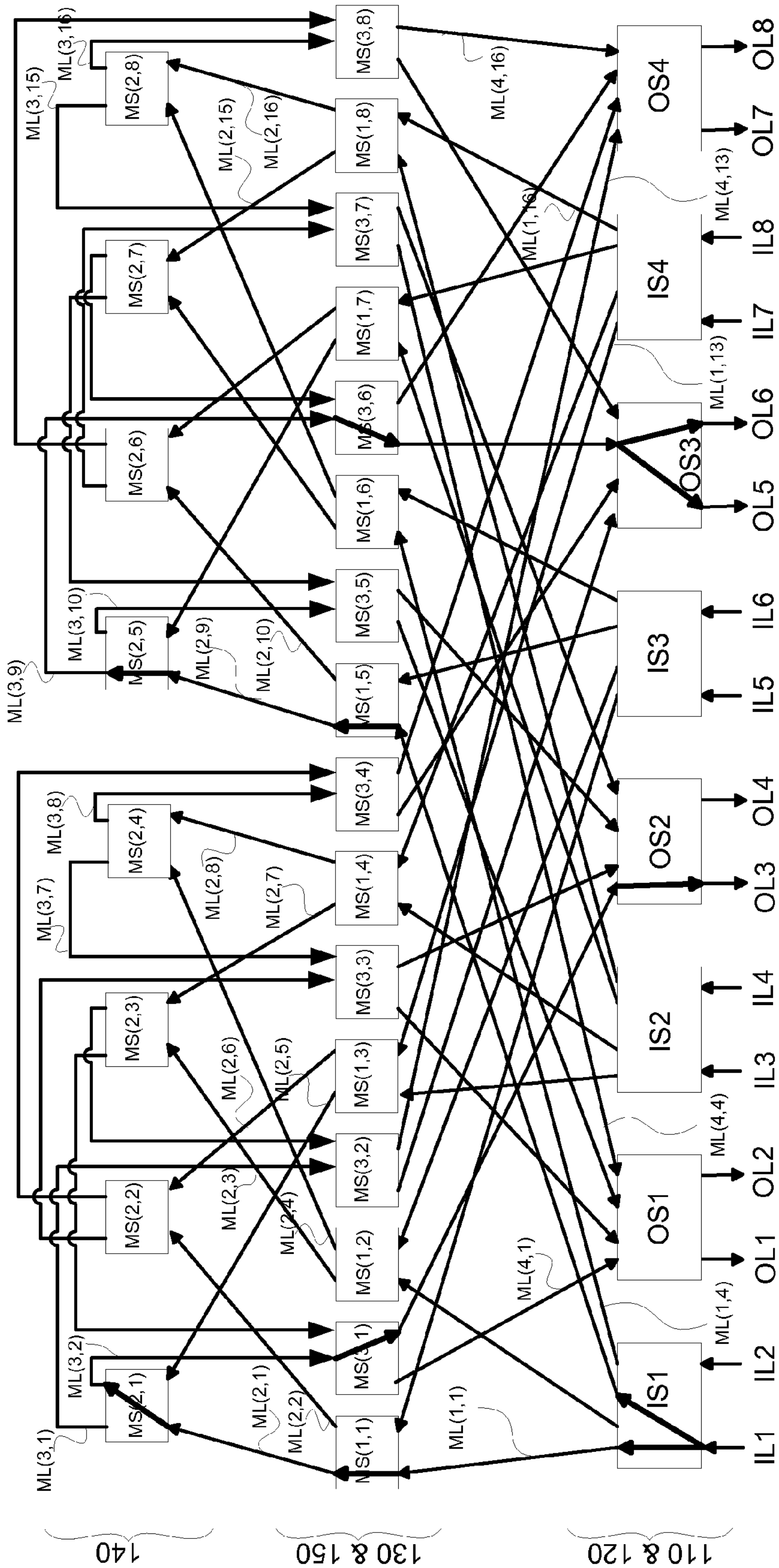
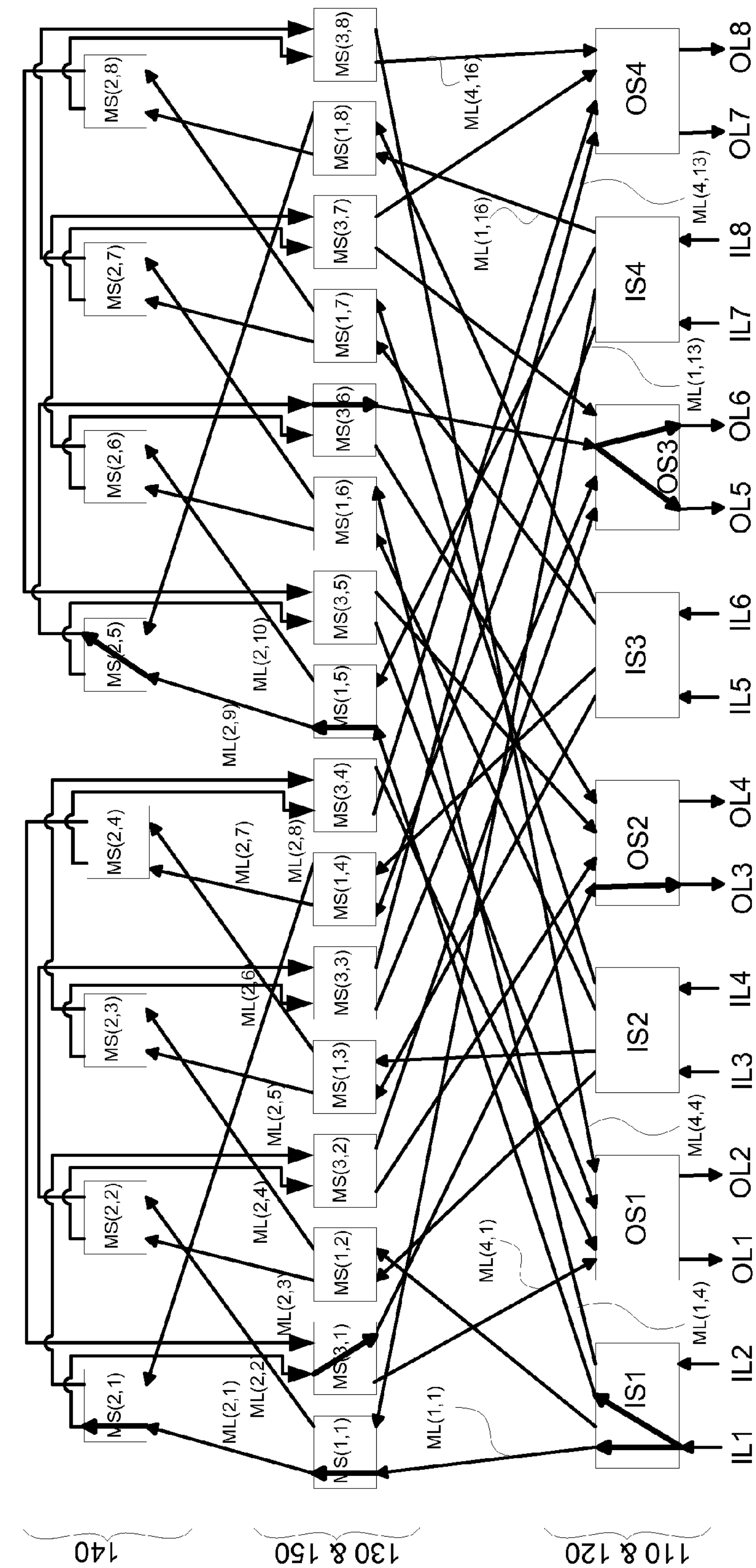
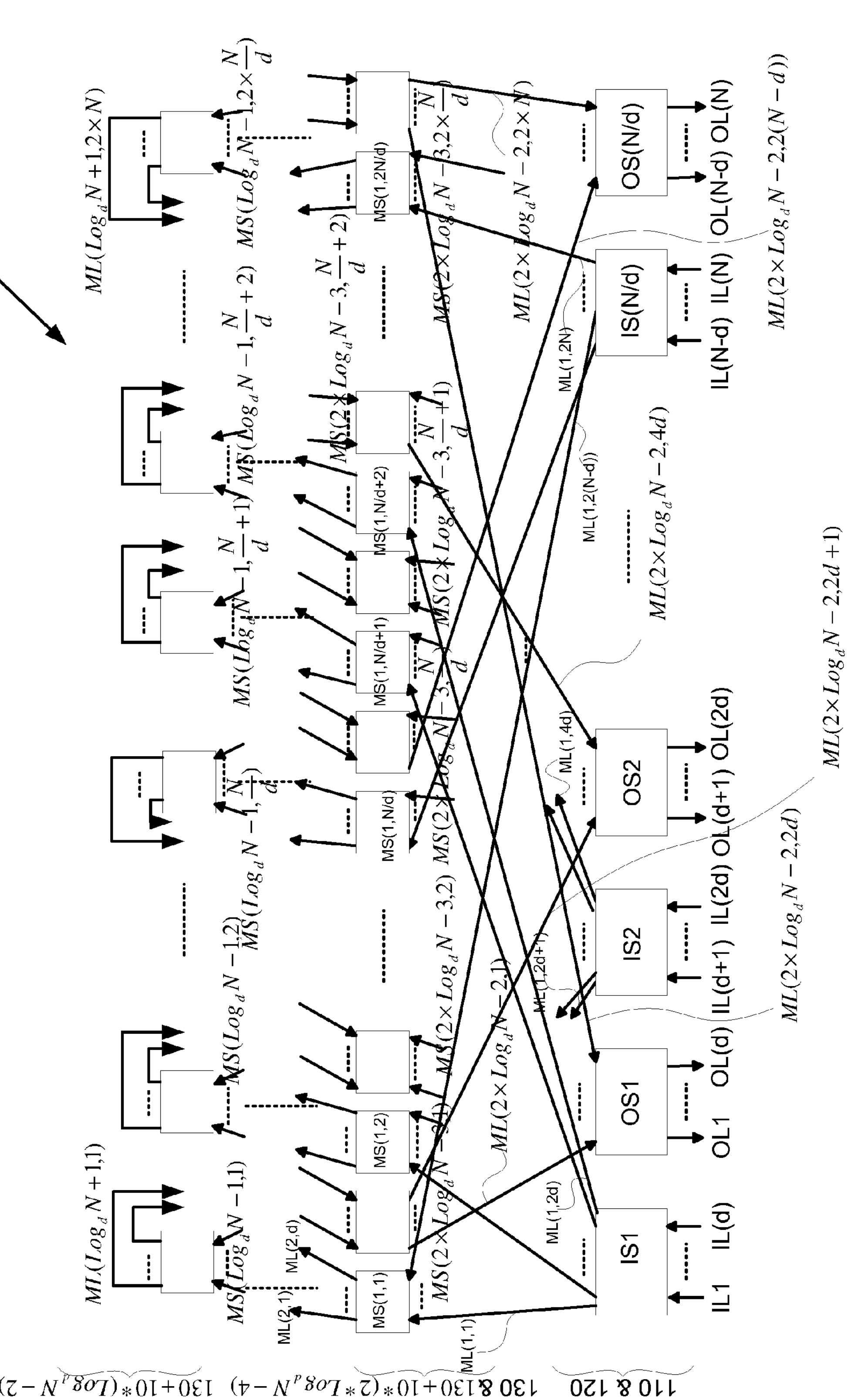


FIG. 4A1

400A2

FIG. 4A2





400B
IS1
IS2
IS(N/d)
OS1
OS2
OS(N/d)
MS(1,1)
MS(1,2)
MS(1,N/d)
MS(1,N/d+1)
MS(1,N/d+2)
MS(1,2N/d)
IL1
IL(d)
IL(d+1)
IL(2d)
IL(N-d)
IL(N)
OL1
OL(d)
OL(d+1)
OL(2d)
OL(N-d)
OL(N)
ML(1,1)
ML(1,2d)
ML(1,2d+1)
ML(1,4d)
ML(1,2(N-d))
ML(1,2N)
ML(2,1)
ML(2,d)
110 & 120
130 & 130+10*(2*Log_d N-4)
130+10*(Log_d N-2)

FIG. 4B

FIG. 4C

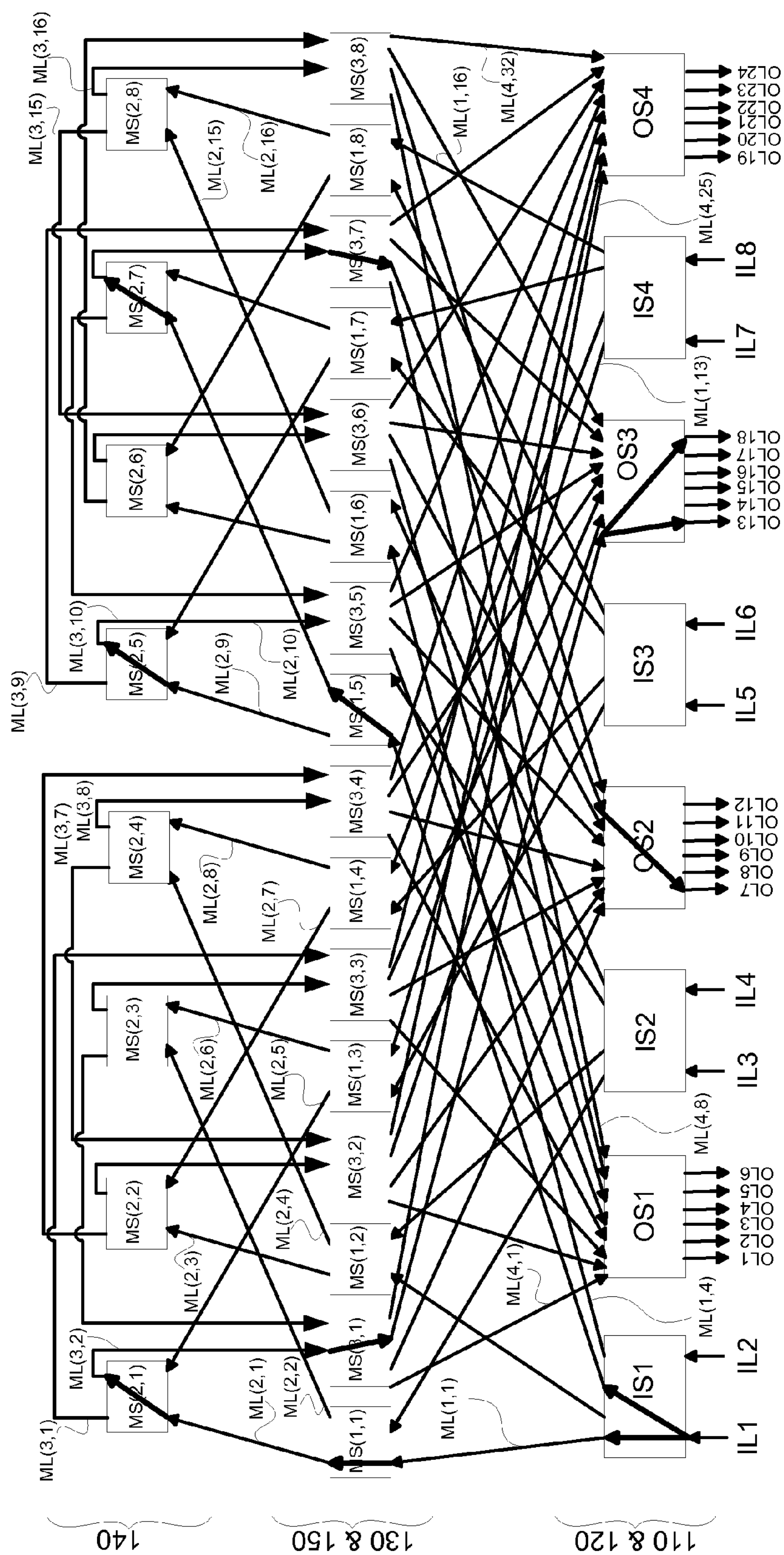

400C
MS(1,1)
MS(3,1)
MS(1,2)
MS(3,2)
MS(1,3)
MS(3,3)
MS(1,4)
MS(3,4)
MS(1,5)
MS(3,5)
MS(1,6)
MS(3,6)
MS(1,7)
MS(3,7)
MS(1,8)
MS(3,8)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(2,5)
MS(2,6)
MS(2,7)
MS(2,8)
IS1
IS2
IS3
IS4
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
OL9
OL10
OL11
OL12
OL13
OL14
OL15
OL16
OL17
OL18
OL19
OL20
OL21
OL22
OL23
OL24
ML(1,1)
ML(1,4)
ML(4,1)
ML(4,8)
ML(1,13)
ML(4,25)
ML(1,16)
ML(4,32)
ML(2,1)
ML(2,2)
ML(2,3)
ML(2,4)
ML(2,5)
ML(2,6)
ML(2,7)
ML(2,8)
ML(2,9)
ML(2,10)
ML(2,15)
ML(2,16)
ML(3,1)
ML(3,2)
ML(3,7)
ML(3,8)
ML(3,9)
ML(3,10)
ML(3,15)
ML(3,16)
140
130 & 150
110 & 120

FIG. 4C1

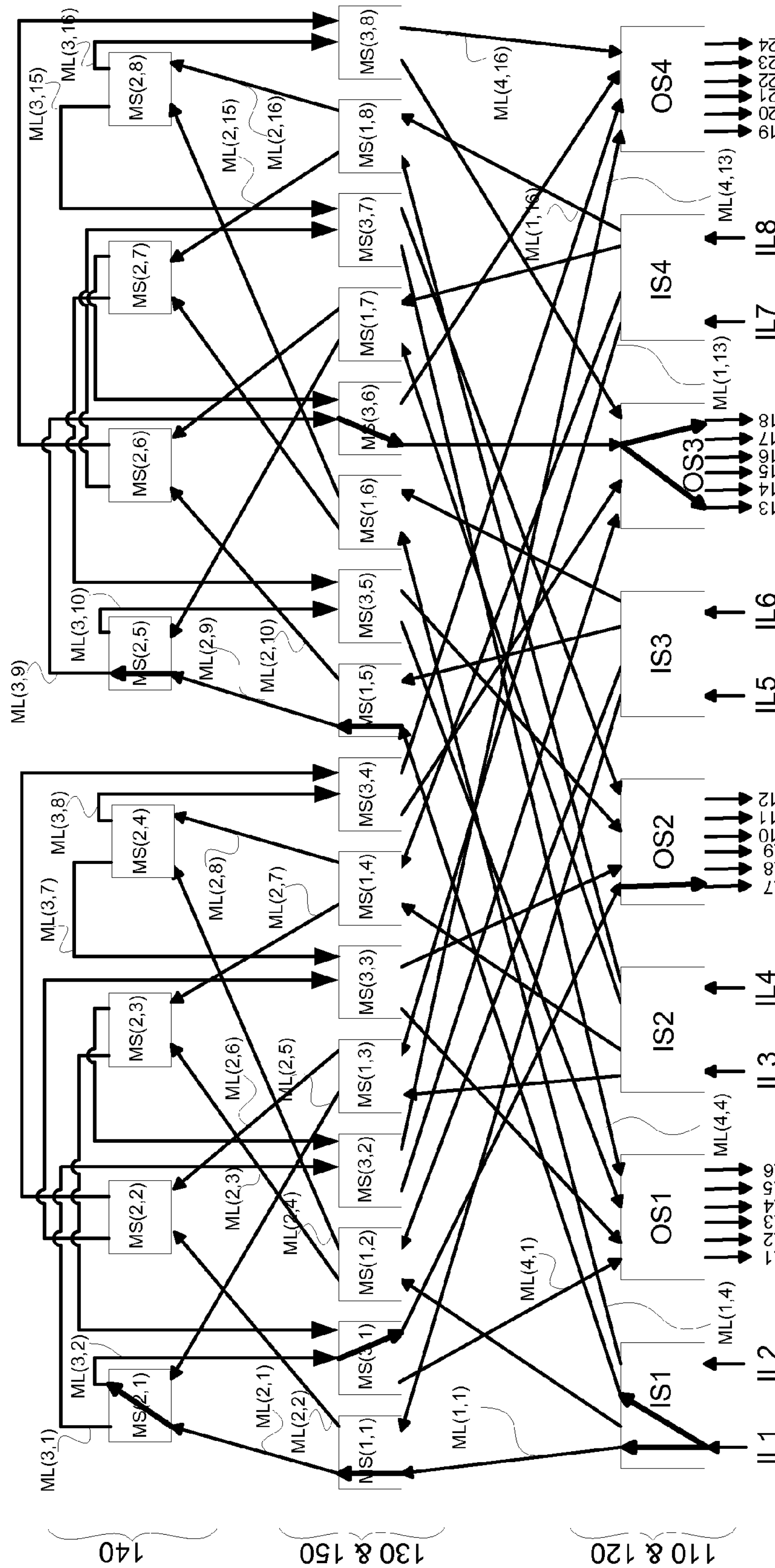

400C1
MS(1,1)
MS(3,1)
MS(1,2)
MS(3,2)
MS(1,3)
MS(3,3)
MS(1,4)
MS(3,4)
MS(1,5)
MS(3,5)
MS(1,6)
MS(3,6)
MS(1,7)
MS(3,7)
MS(1,8)
MS(3,8)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(2,5)
MS(2,6)
MS(2,7)
MS(2,8)
IS1
IS2
IS3
IS4
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
OL9
OL10
OL11
OL12
OL13
OL14
OL15
OL16
OL17
OL18
OL19
OL20
OL21
OL22
OL23
OL24
ML(1,1)
ML(1,4)
ML(1,13)
ML(1,16)
ML(4,1)
ML(4,4)
ML(4,13)
ML(4,16)
ML(2,1)
ML(2,2)
ML(2,3)
ML(2,4)
ML(2,5)
ML(2,6)
ML(2,7)
ML(2,8)
ML(2,9)
ML(2,10)
ML(2,15)
ML(2,16)
ML(3,1)
ML(3,2)
ML(3,7)
ML(3,8)
ML(3,9)
ML(3,10)
ML(3,15)
ML(3,16)
140
130 & 150
110 & 120

FIG. 4C2

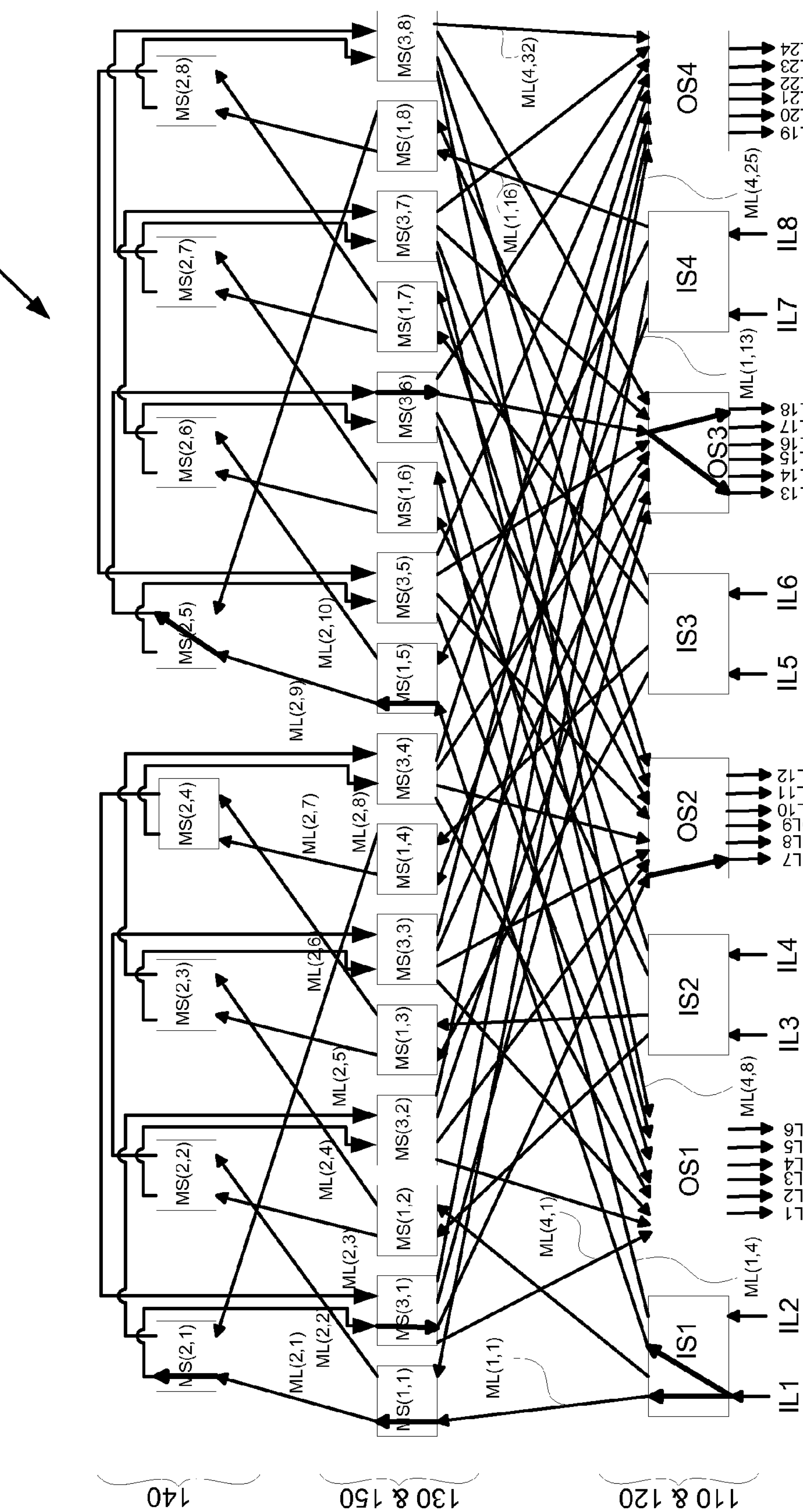

400C2
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(2,5)
MS(2,6)
MS(2,7)
MS(2,8)
MS(1,1)
MS(3,1)
MS(1,2)
MS(3,2)
MS(1,3)
MS(3,3)
MS(1,4)
MS(3,4)
MS(1,5)
MS(3,5)
MS(1,6)
MS(3,6)
MS(1,7)
MS(3,7)
MS(1,8)
MS(3,8)
ML(2,1)
ML(2,2)
ML(2,3)
ML(2,4)
ML(2,5)
ML(2,6)
ML(2,7)
ML(2,8)
ML(2,9)
ML(2,10)
ML(1,1)
ML(4,1)
ML(1,4)
ML(4,8)
ML(1,13)
ML(1,16)
ML(4,25)
ML(4,32)
IS1
IS2
IS3
IS4
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
OL9
OL10
OL11
OL12
OL13
OL14
OL15
OL16
OL17
OL18
OL19
OL20
OL21
OL22
OL23
OL24
140
130 & 150
110 & 120

FIG. 4D

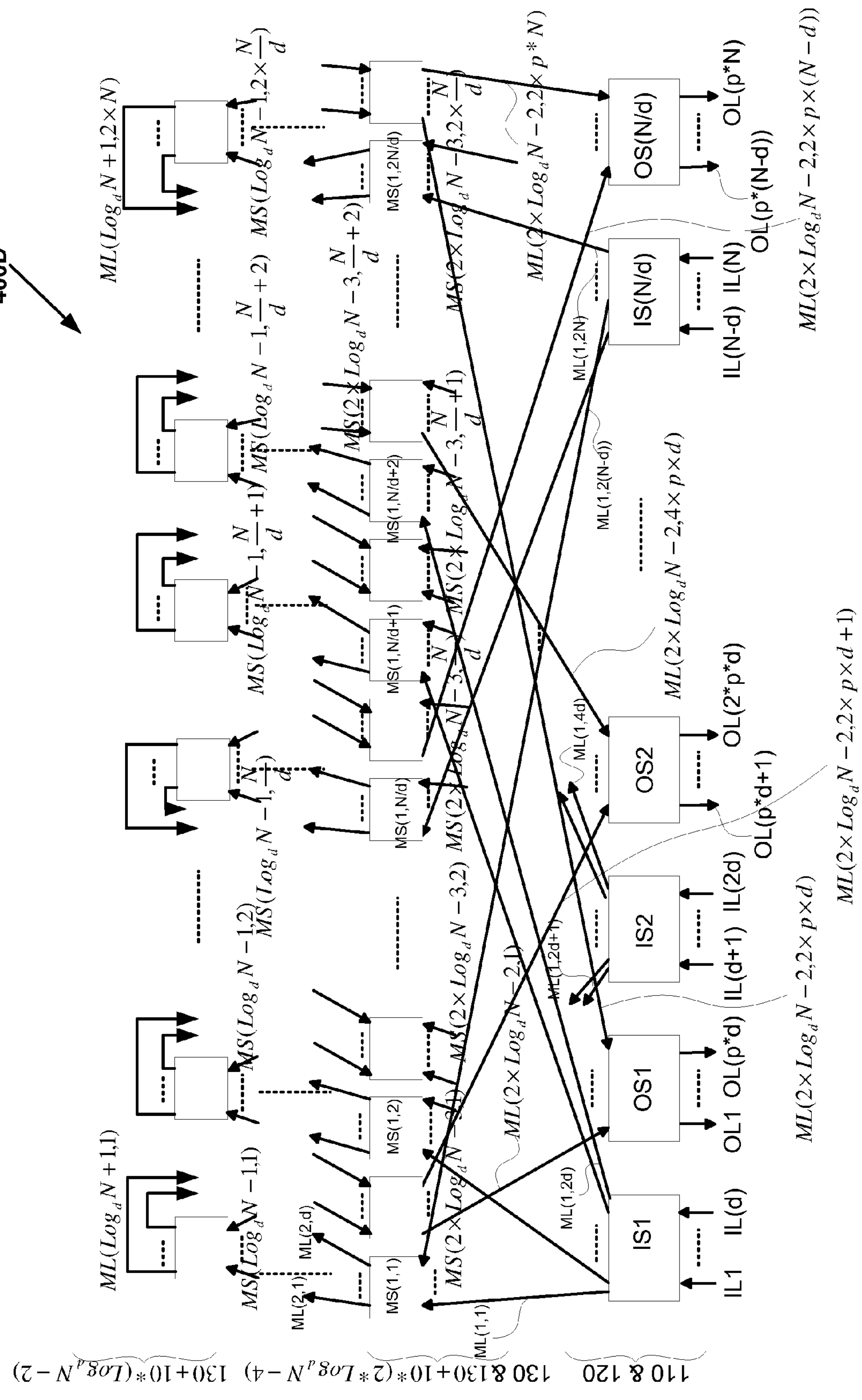
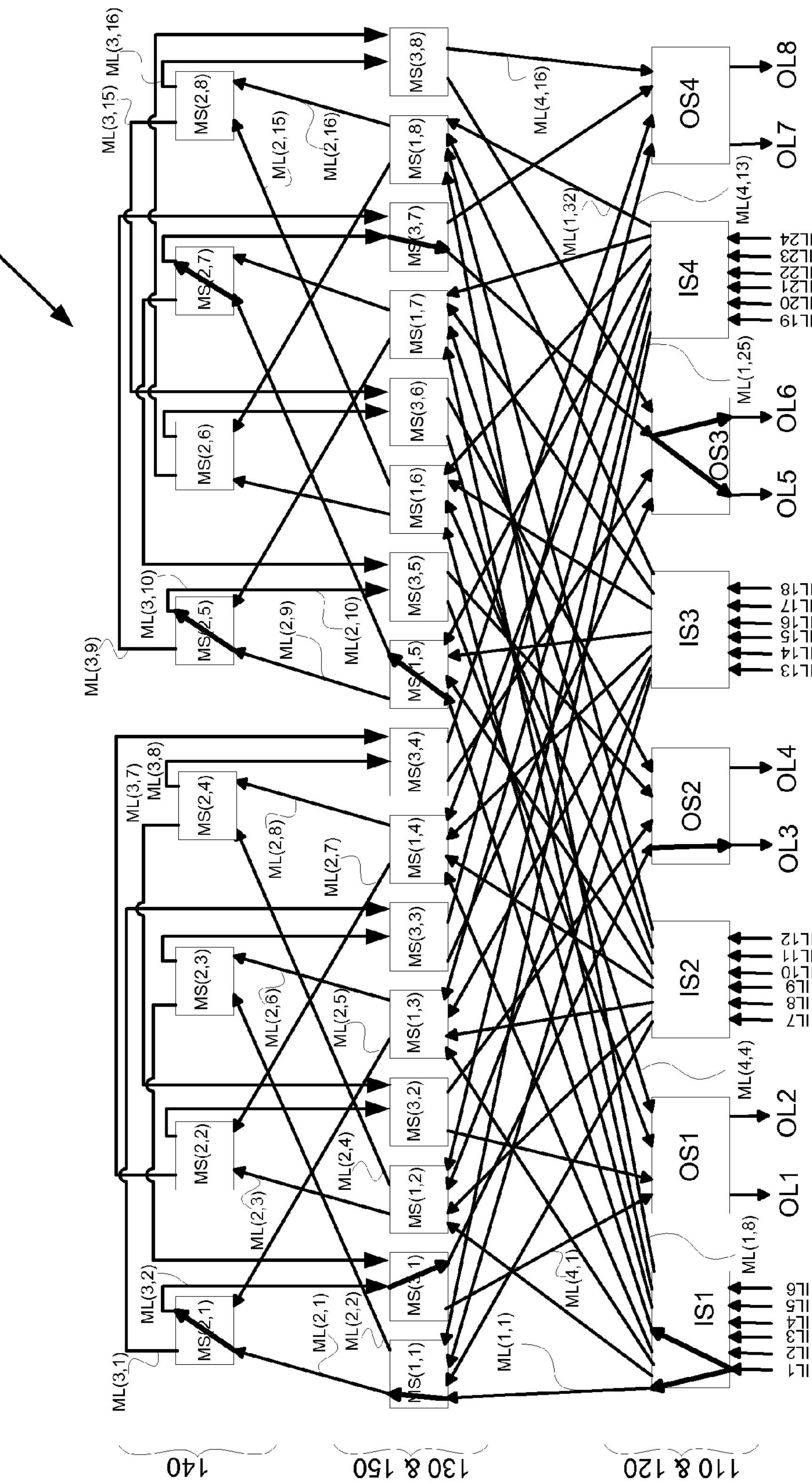

400D
IS1
IS2
IS(N/d)
OS1
OS2
OS(N/d)
MS(1,1)
MS(1,2)
MS(1,N/d)
MS(1,N/d+1)
MS(1,N/d+2)
MS(1,2N/d)
IL1
IL(d)
IL(d+1)
IL(2d)
IL(N-d)
IL(N)
OL1
OL(p*d)
OL(p*d+1)
OL(2*p*d)
OL(p*(N-d))
OL(p*N)
110 & 120
130 & 130+10*(2*Log_d N-4)
130+10*(Log_d N-2)

FIG. 4E

400E



MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(1,5)
MS(1,6)
MS(1,7)
MS(1,8)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(2,5)
MS(2,6)
MS(2,7)
MS(2,8)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
MS(3,5)
MS(3,6)
MS(3,7)
MS(3,8)
IS1
IS2
IS3
IS4
OS1
OS2
OS3
OS4
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
ML(1,1)
ML(1,8)
ML(1,25)
ML(1,32)
ML(2,1)
ML(2,2)
ML(2,3)
ML(2,4)
ML(2,5)
ML(2,6)
ML(2,7)
ML(2,8)
ML(2,9)
ML(2,10)
ML(2,15)
ML(2,16)
ML(3,1)
ML(3,2)
ML(3,7)
ML(3,8)
ML(3,9)
ML(3,10)
ML(3,15)
ML(3,16)
ML(4,1)
ML(4,4)
ML(4,13)
ML(4,16)
140
130 & 150
110 & 120

FIG. 4E1

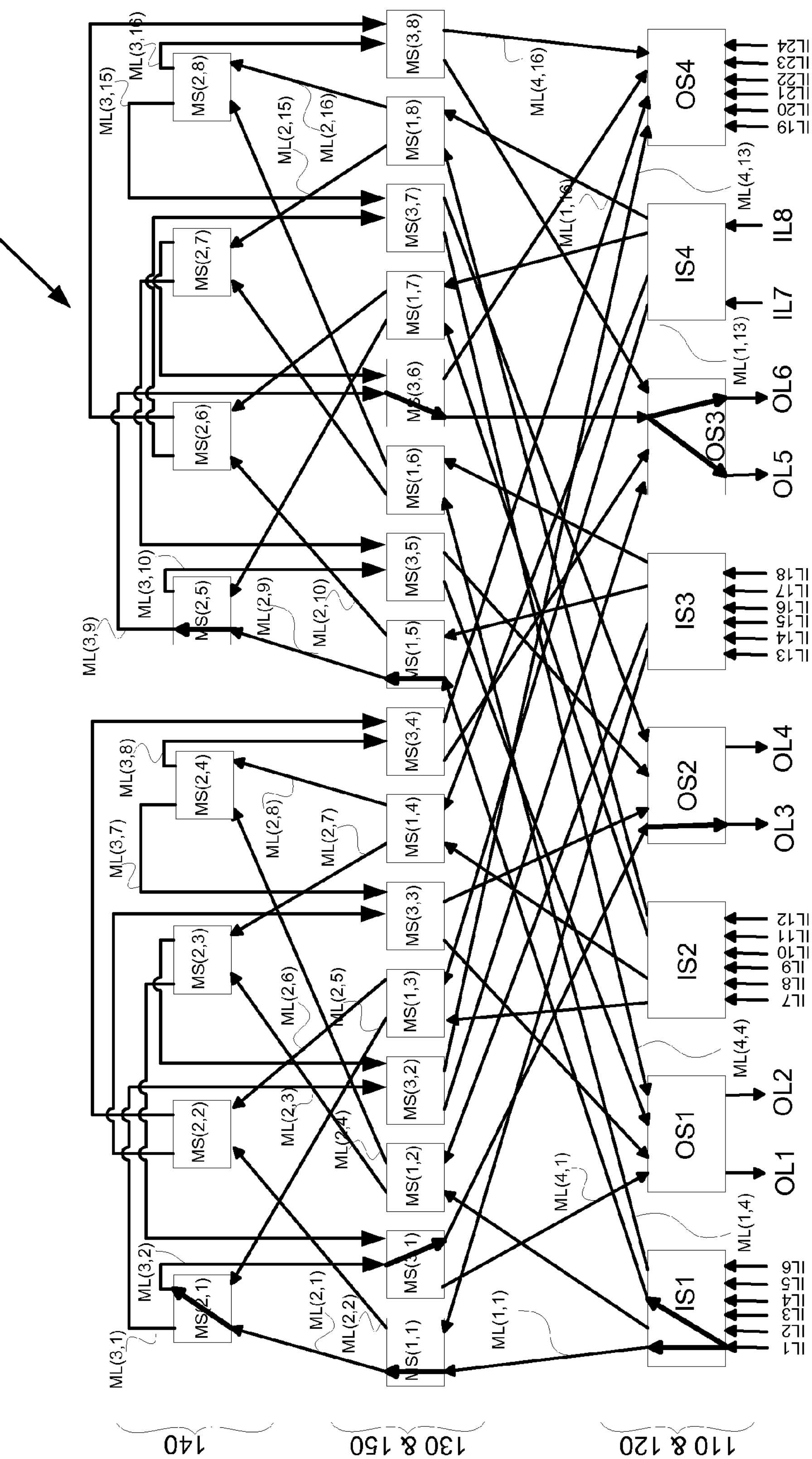
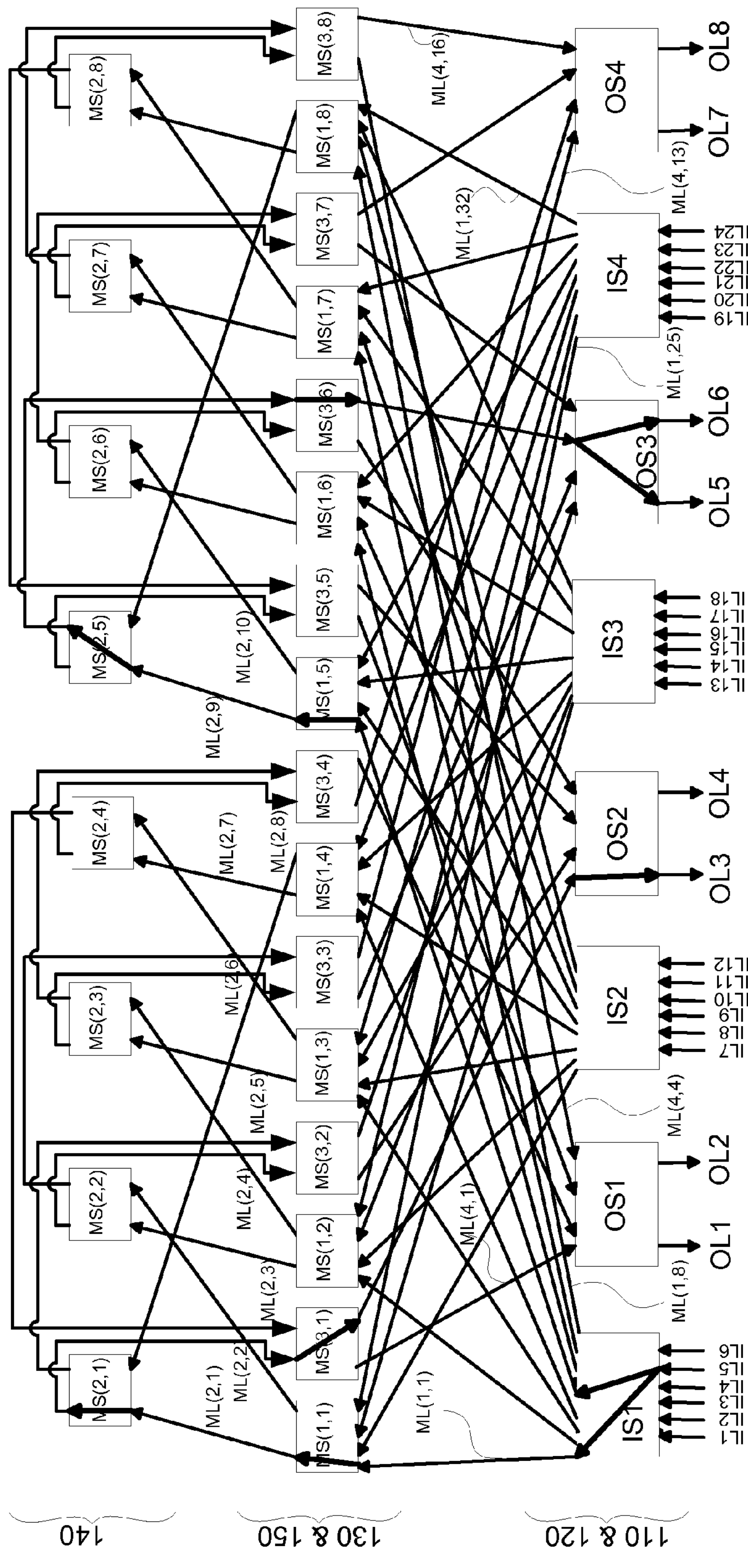

400E1
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(1,5)
MS(1,6)
MS(1,7)
MS(1,8)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(2,5)
MS(2,6)
MS(2,7)
MS(2,8)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
MS(3,5)
MS(3,6)
MS(3,7)
MS(3,8)
IS1
IS2
IS3
IS4
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
IL9
IL10
IL11
IL12
IL13
IL14
IL15
IL16
IL17
IL18
IL19
IL20
IL21
IL22
IL23
IL24
OL1
OL2
OL3
OL4
OL5
OL6
ML(1,1)
ML(1,4)
ML(1,13)
ML(1,16)
ML(2,1)
ML(2,2)
ML(2,3)
ML(2,4)
ML(2,5)
ML(2,6)
ML(2,7)
ML(2,8)
ML(2,9)
ML(2,10)
ML(2,15)
ML(2,16)
ML(3,1)
ML(3,2)
ML(3,7)
ML(3,8)
ML(3,9)
ML(3,10)
ML(3,15)
ML(3,16)
ML(4,1)
ML(4,4)
ML(4,13)
ML(4,16)
140
130 & 150
110 & 120

FIG. 4E2

400E2



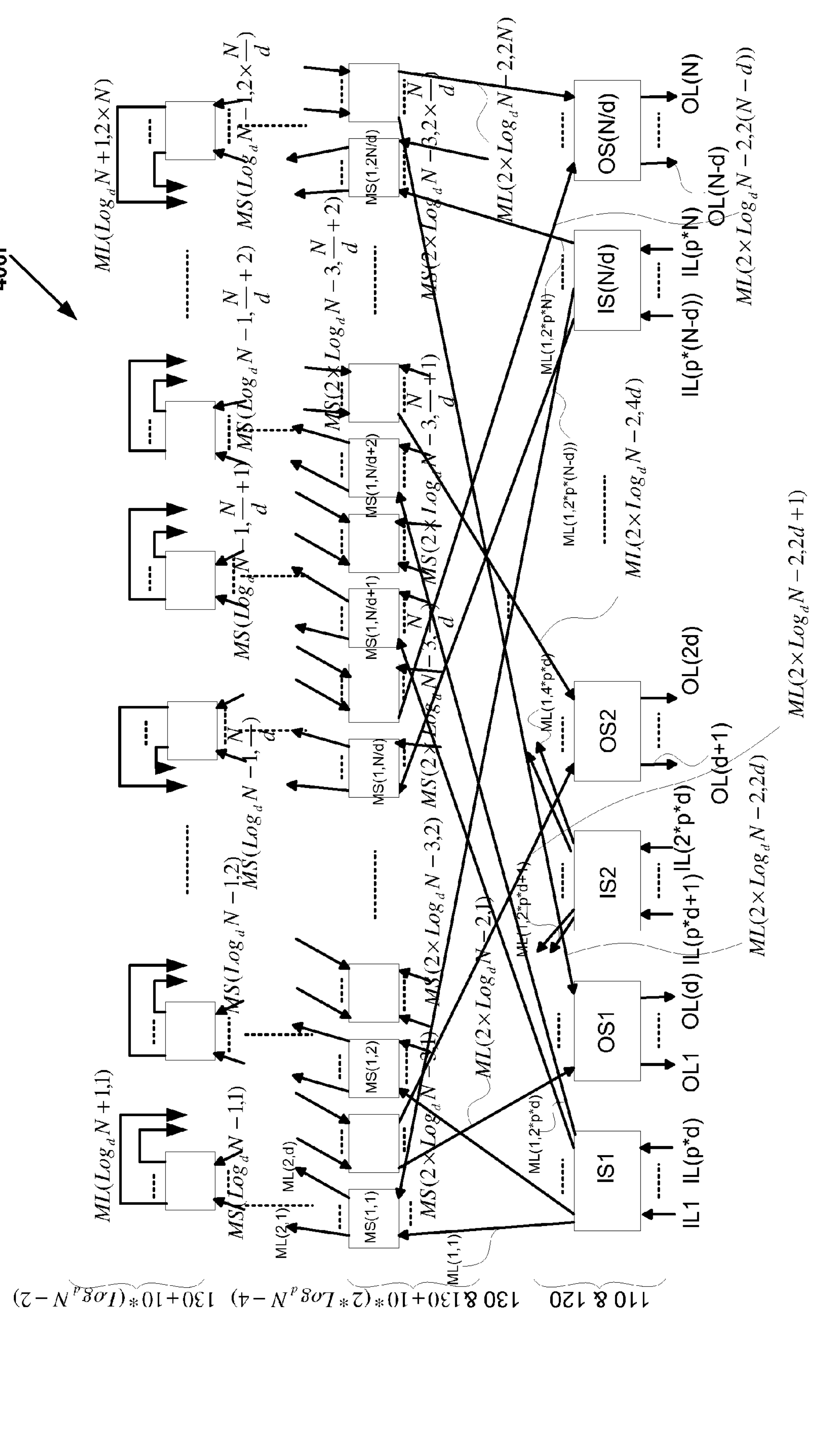
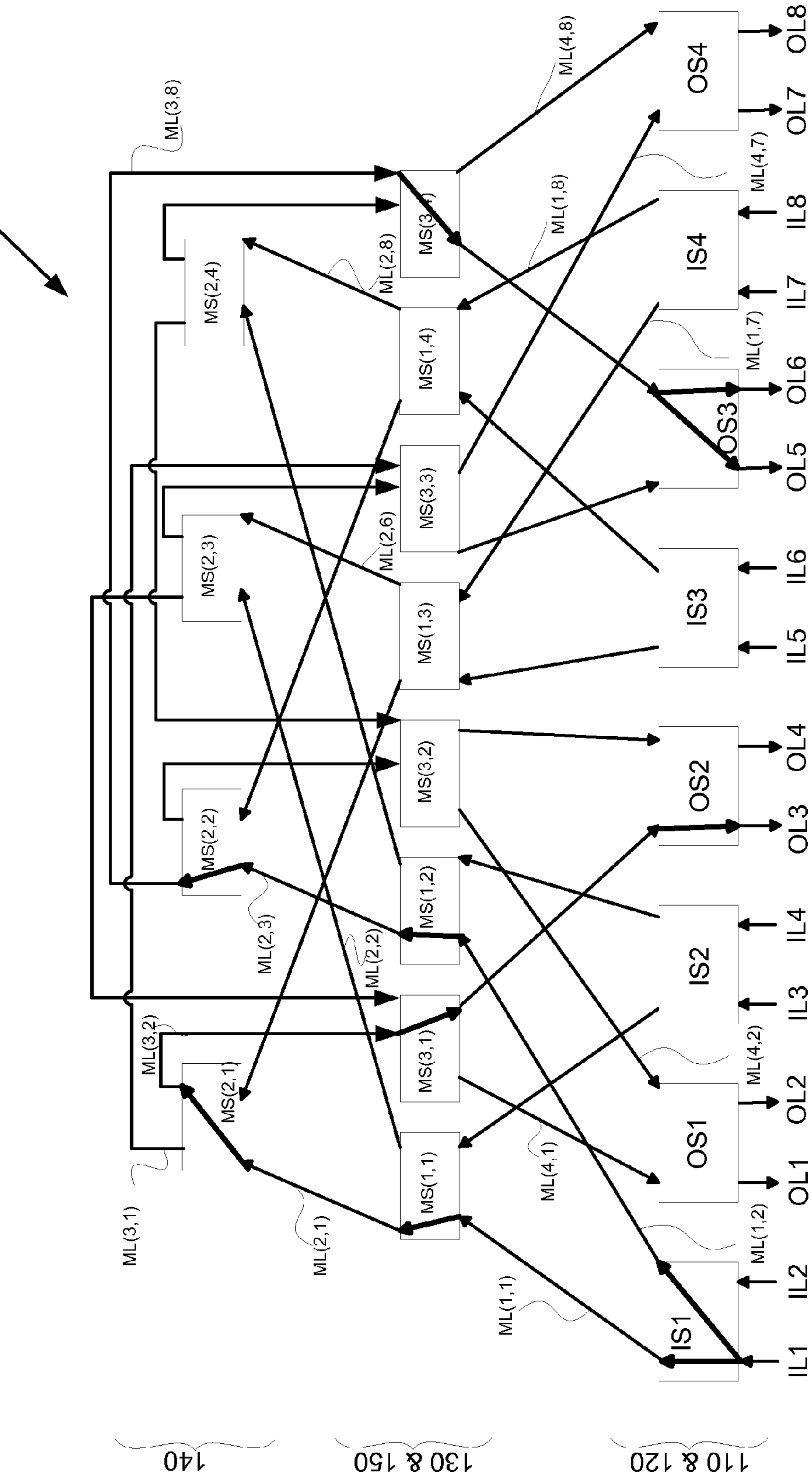

400F
IS1
IS2
IS(N/d)
OS1
OS2
OS(N/d)
MS(1,1)
MS(1,2)
MS(1,N/d)
MS(1,N/d+1)
MS(1,N/d+2)
MS(1,2N/d)
IL1
IL(p*d)
IL(p*d+1)
IL(2*p*d)
IL(p*(N-d))
IL(p*N)
OL1
OL(d)
OL(d+1)
OL(2d)
OL(N-d)
OL(N)
ML(1,1)
ML(2,1)
ML(2,d)
ML(1,2*p*d)
ML(1,2*p*d+1)
ML(1,4*p*d)
ML(1,2*p*(N-d))
ML(1,2*p*N)
110 & 120
130 & 130+10*(2*Log_d N-4)
130+10*(Log_d N-2)

FIG. 4F

FIG. 5A


500A
IS1
IS2
IS3
IS4
OS1
OS2
OS3
OS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
ML(1,1)
ML(1,2)
ML(1,7)
ML(1,8)
ML(2,1)
ML(2,2)
ML(2,3)
ML(2,6)
ML(2,8)
ML(3,1)
ML(3,2)
ML(3,8)
ML(4,1)
ML(4,2)
ML(4,7)
ML(4,8)
140
130 & 150
110 & 120

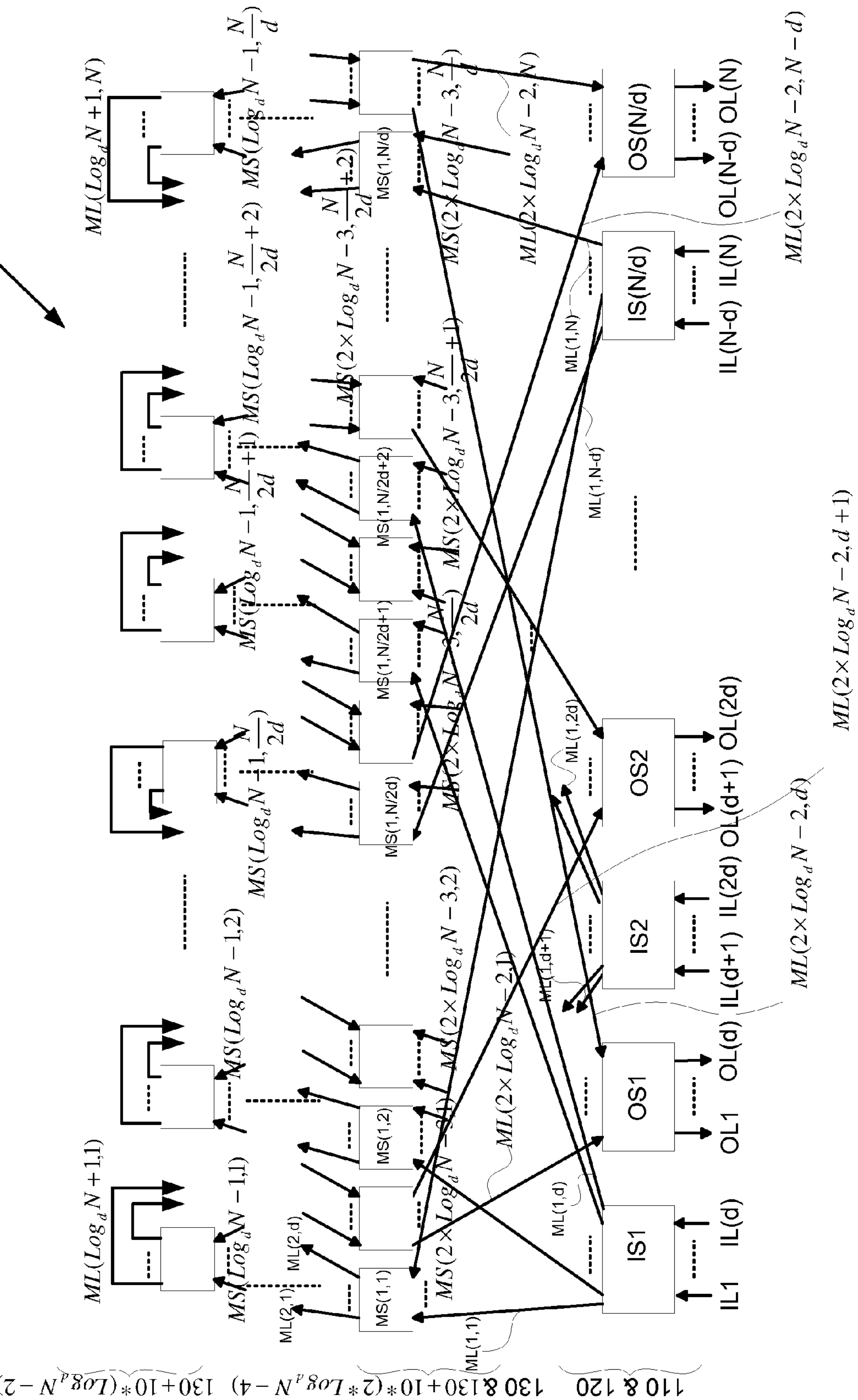

500B
IS1
IS2
IS(N/d)
OS1
OS2
OS(N/d)
MS(1,1)
MS(1,2)
MS(1,N/2d)
MS(1,N/2d+1)
MS(1,N/2d+2)
MS(1,N/d)
IL1
IL(d)
IL(d+1)
IL(2d)
IL(N-d)
IL(N)
OL1
OL(d)
OL(d+1)
OL(2d)
OL(N-d)
OL(N)
ML(1,1)
ML(1,d)
ML(1,d+1)
ML(1,2d)
ML(1,N-d)
ML(1,N)
ML(2,1)
ML(2,d)

FIG. 5B

FIG. 5C

500C

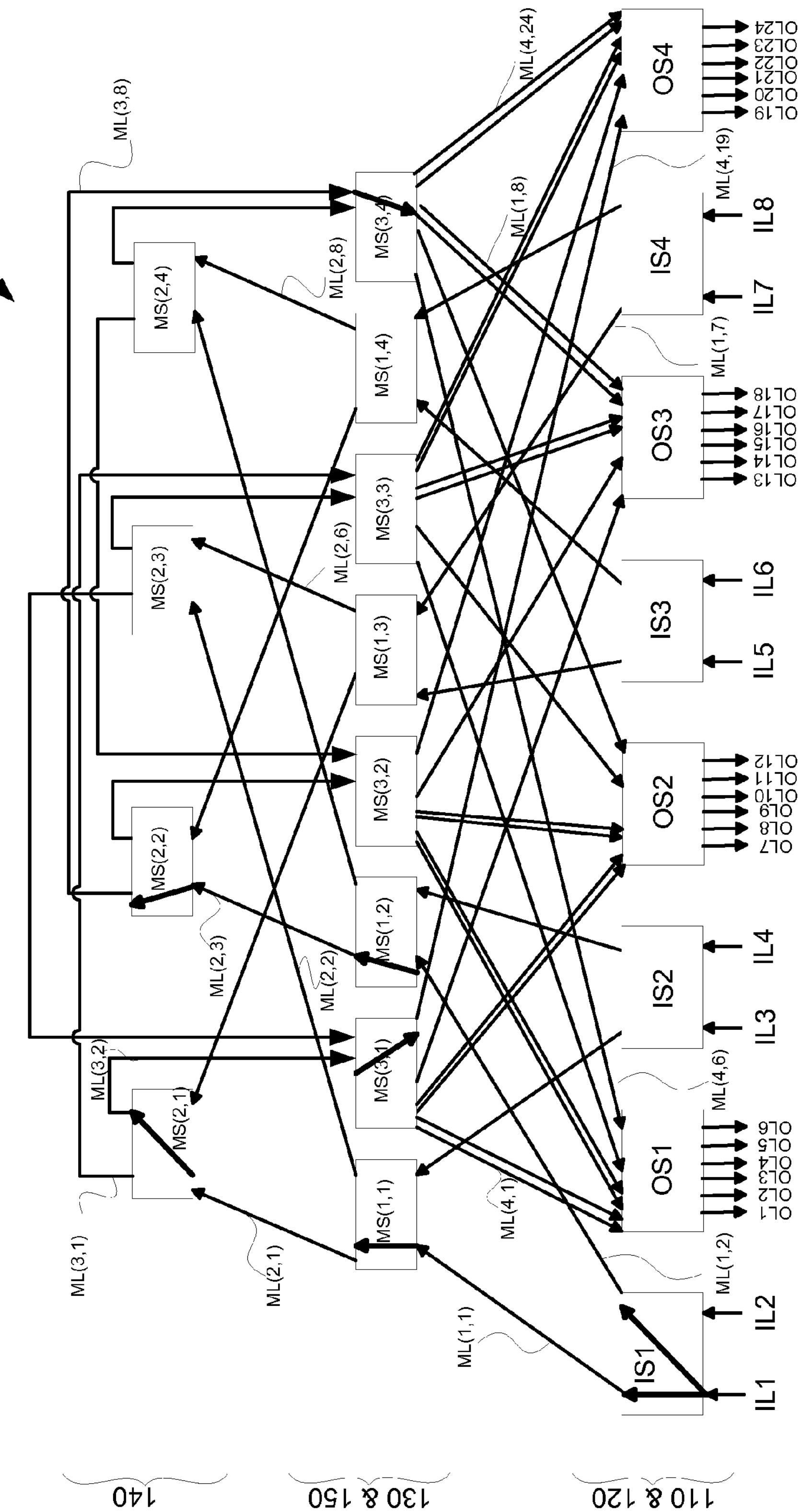

140
130 & 150
110 & 120
IS1
IS2
IS3
IS4
OS1
OS2
OS3
OS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
OL9
OL10
OL11
OL12
OL13
OL14
OL15
OL16
OL17
OL18
OL19
OL20
OL21
OL22
OL23
OL24
ML(1,1)
ML(1,2)
ML(1,7)
ML(1,8)
ML(2,1)
ML(2,2)
ML(2,3)
ML(2,6)
ML(2,8)
ML(3,1)
ML(3,2)
ML(3,8)
ML(4,1)
ML(4,6)
ML(4,19)
ML(4,24)

FIG. 5D

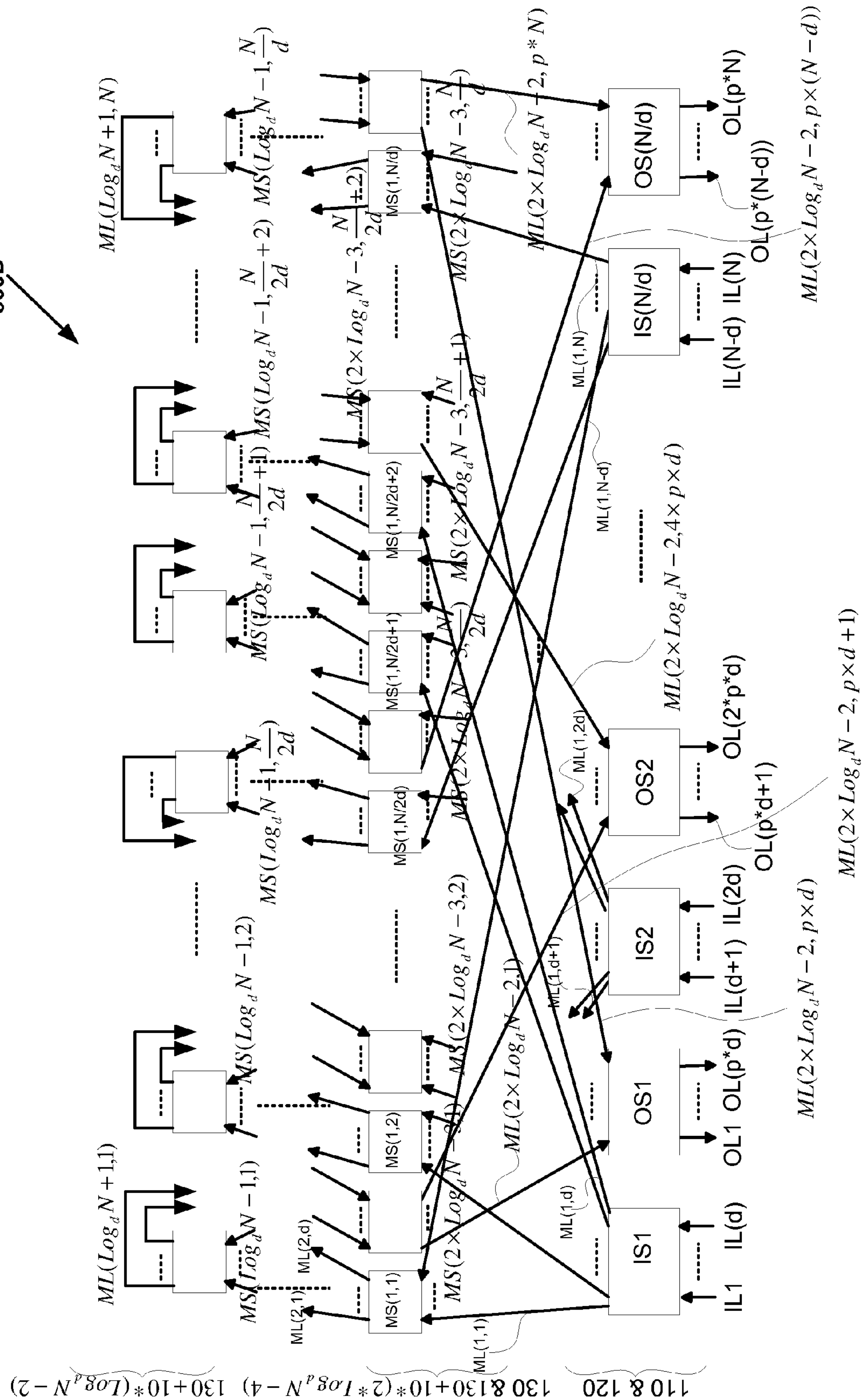
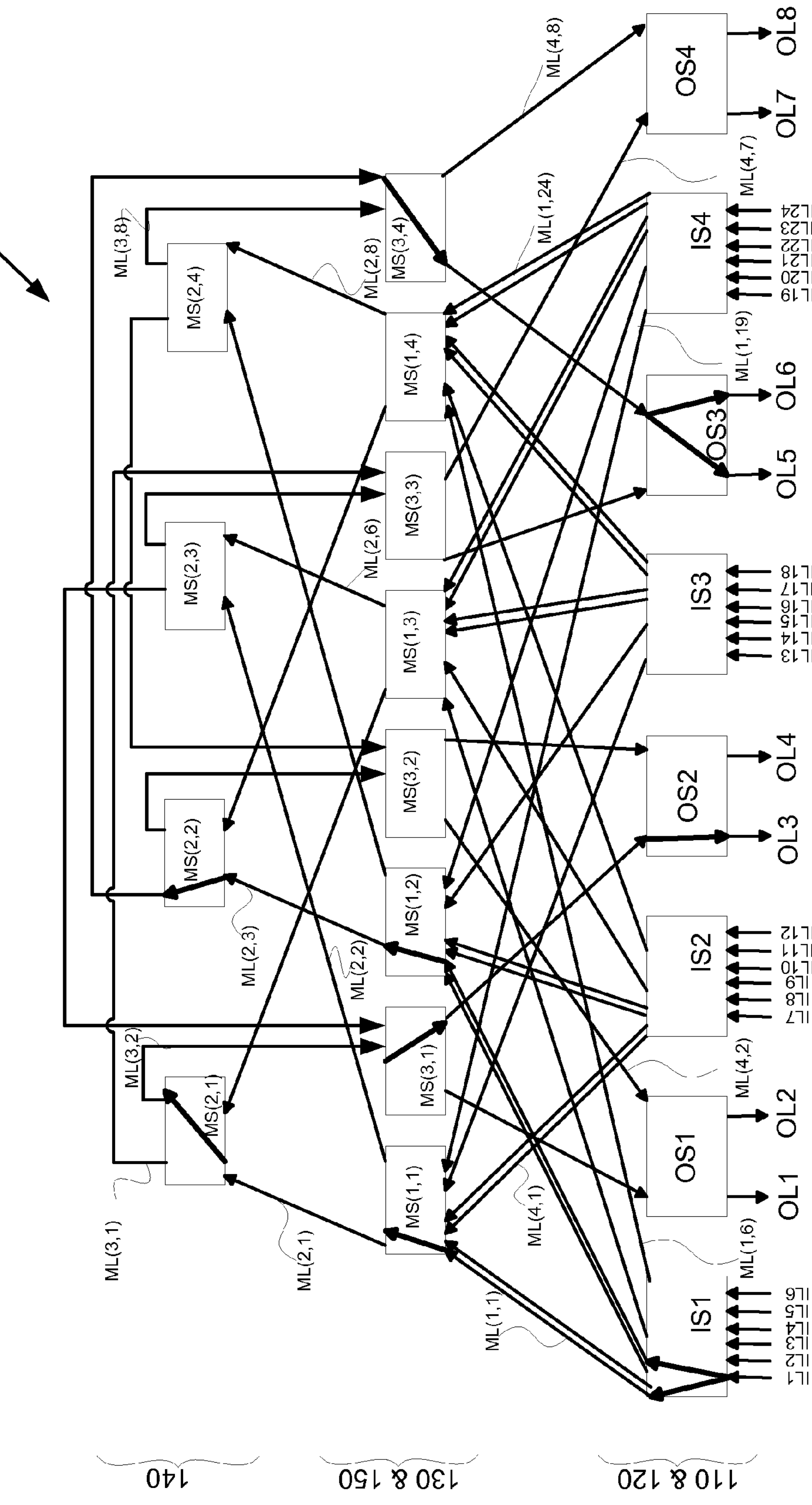

500D
IS1
IS2
IS(N/d)
OS1
OS2
OS(N/d)
MS(1,1)
MS(1,2)
MS(1,N/2d)
MS(1,N/2d+1)
MS(1,N/2d+2)
MS(1,N/d)
IL1
IL(d)
IL(d+1)
IL(2d)
IL(N-d)
IL(N)
OL1
OL(p*d)
OL(p*d+1)
OL(2*p*d)
OL(p*(N-d))
OL(p*N)
ML(1,1)
ML(1,d)
ML(1,d+1)
ML(1,2d)
ML(1,N-d)
ML(1,N)
ML(2,1)
ML(2,d)
110 & 120
130 & 130+10*(2*Log_d N-4)
130+10*(Log_d N-2)

FIG. 5E

500E



MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
IS1
IS2
IS3
IS4
OS1
OS2
OS3
OS4
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
IL9
IL10
IL11
IL12
IL13
IL14
IL15
IL16
IL17
IL18
IL19
IL20
IL21
IL22
IL23
IL24
ML(1,1)
ML(1,6)
ML(1,19)
ML(1,24)
ML(2,1)
ML(2,2)
ML(2,3)
ML(2,6)
ML(2,8)
ML(3,1)
ML(3,2)
ML(3,8)
ML(4,1)
ML(4,2)
ML(4,7)
ML(4,8)
140
130 & 150
110 & 120

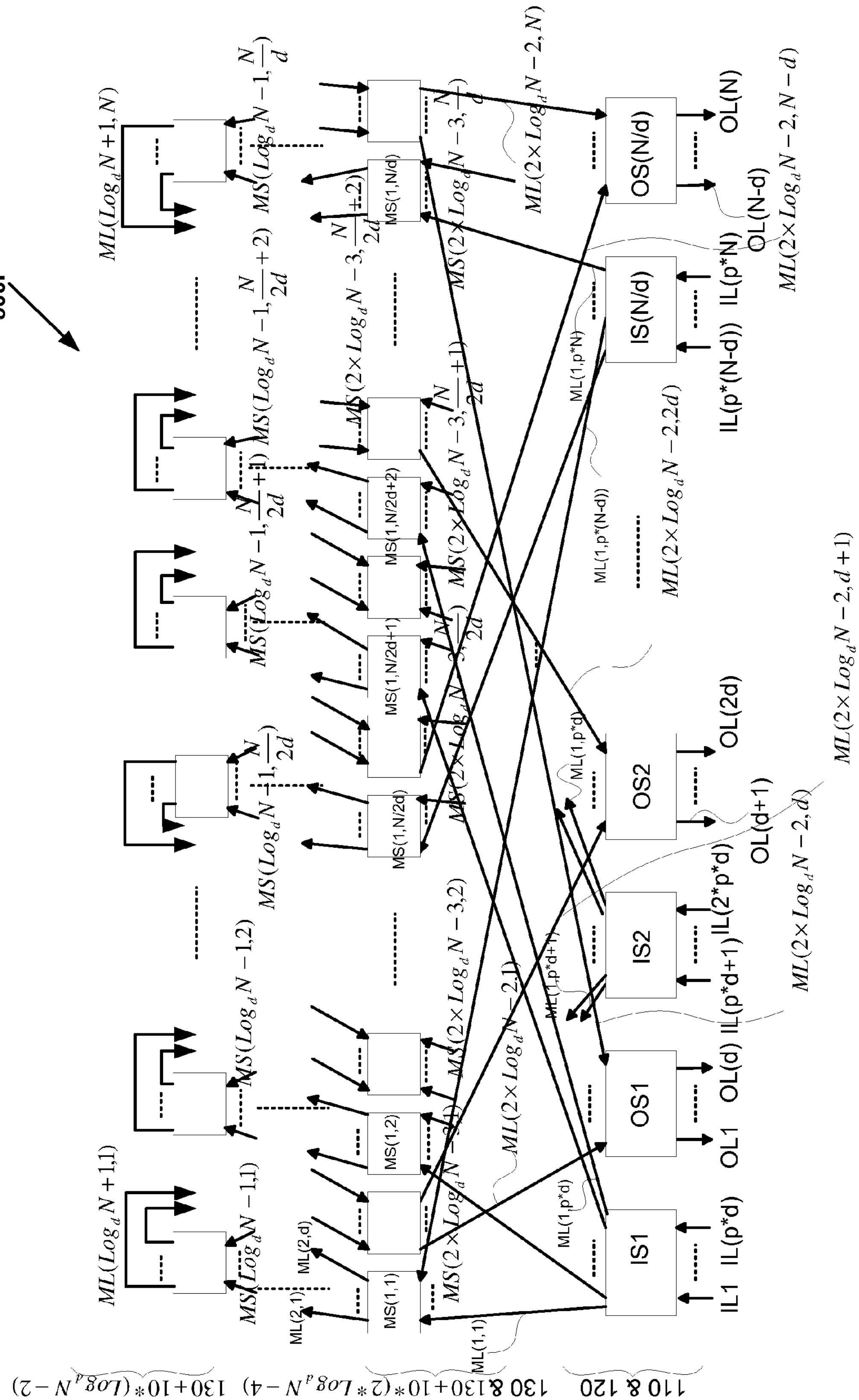
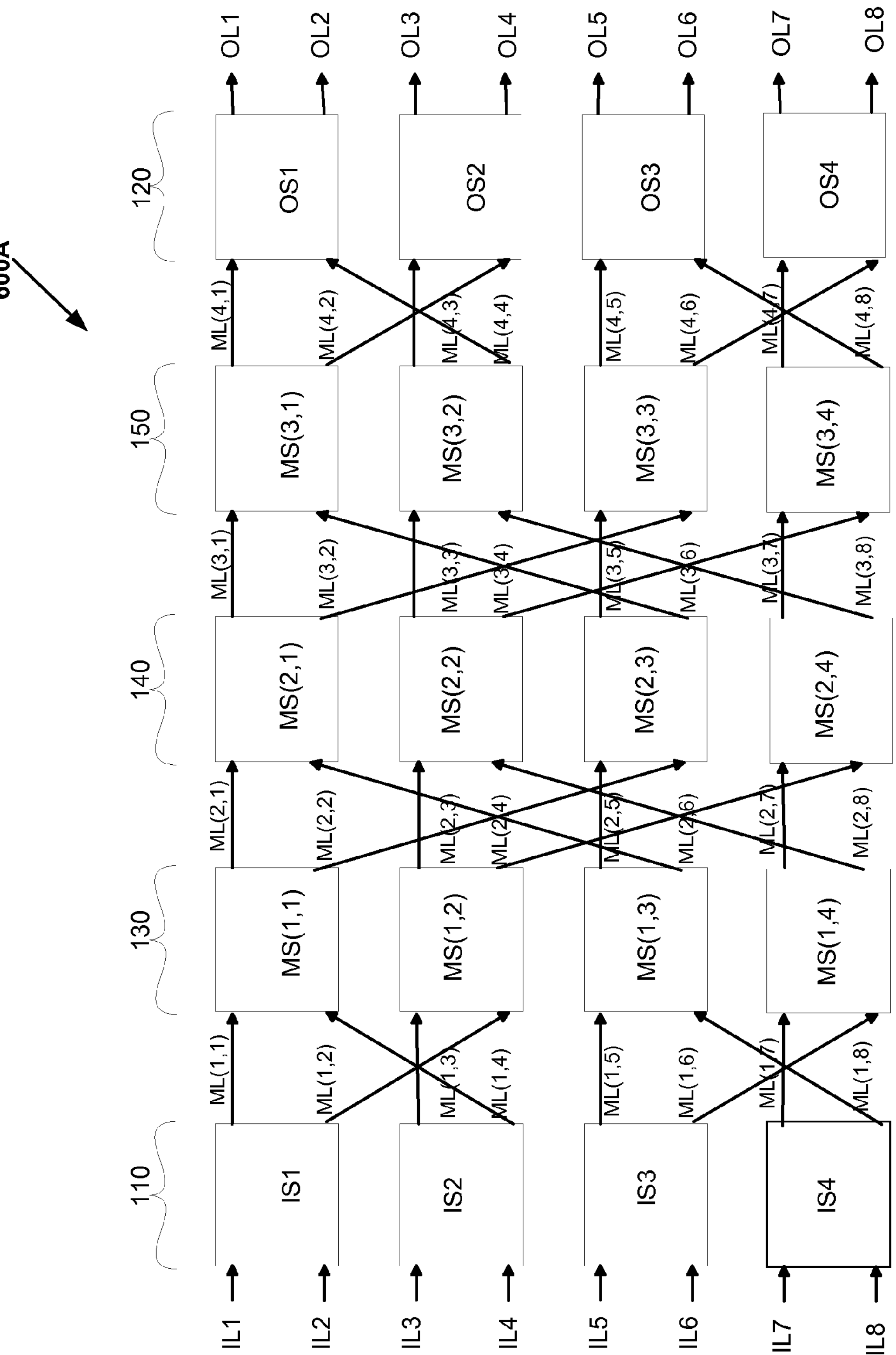

500F
MS(1,1)
MS(1,2)
MS(1,N/2d)
MS(1,N/2d+1)
MS(1,N/2d+2)
MS(1,N/d)
IS1
IS2
IS(N/d)
OS1
OS2
OS(N/d)
IL1
IL(p*d)
OL1
OL(d)
OL(2d)
OL(N)
ML(1,1)
ML(2,1)
ML(2,d)
110 & 120

FIG. 5F

FIG. 6A


600A
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
ML(1,1)
ML(1,2)
ML(1,3)
ML(1,4)
ML(1,5)
ML(1,6)
ML(1,7)
ML(1,8)
ML(2,1)
ML(2,2)
ML(2,3)
ML(2,4)
ML(2,5)
ML(2,6)
ML(2,7)
ML(2,8)
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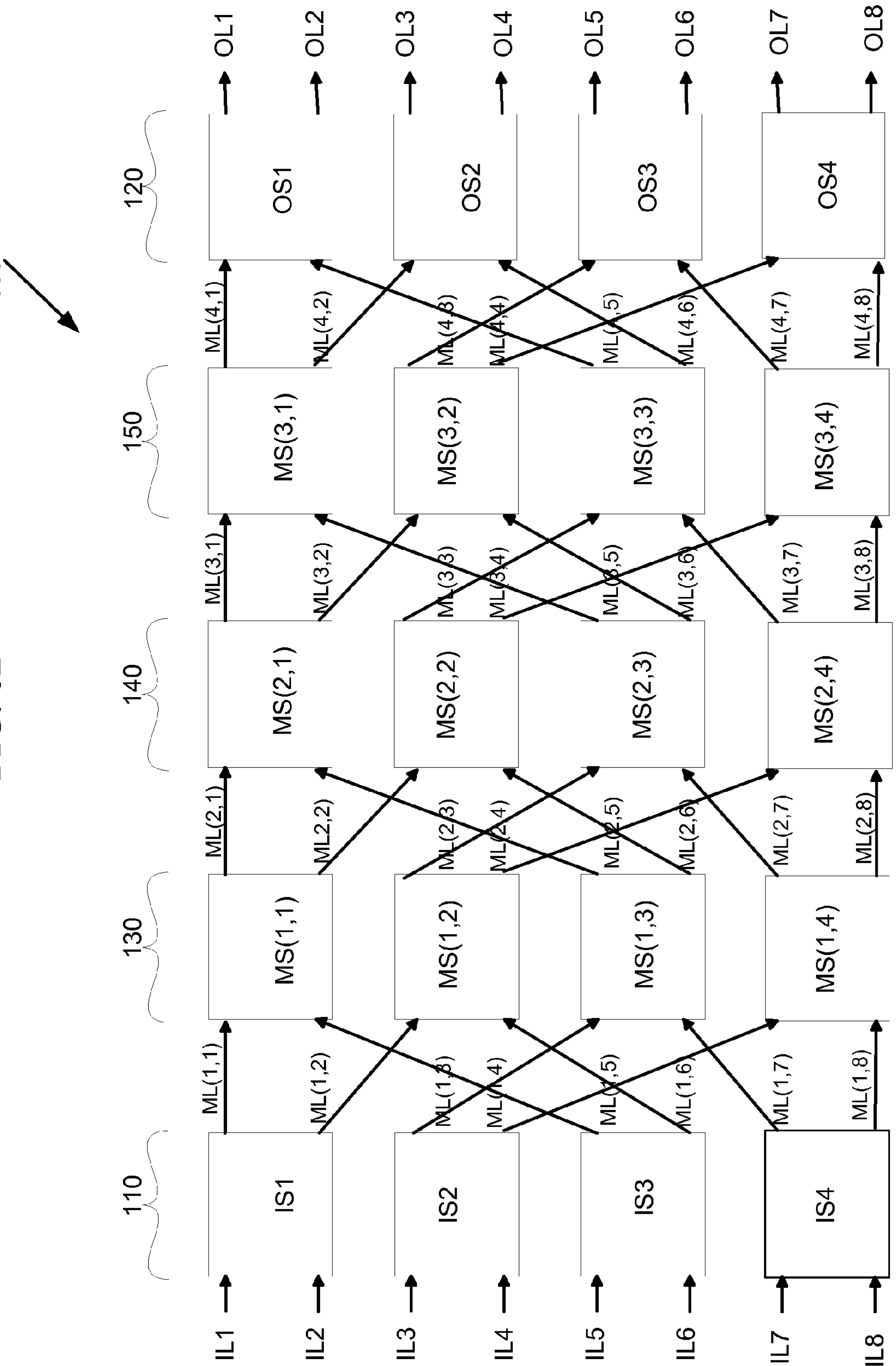
ML(3,2)
ML(3,3)
ML(3,4)
ML(3,5)
ML(3,6)
ML(3,7)
ML(3,8)
ML(4,1)
ML(4,2)
ML(4,3)
ML(4,4)
ML(4,5)
ML(4,6)
ML(4,7)
ML(4,8)

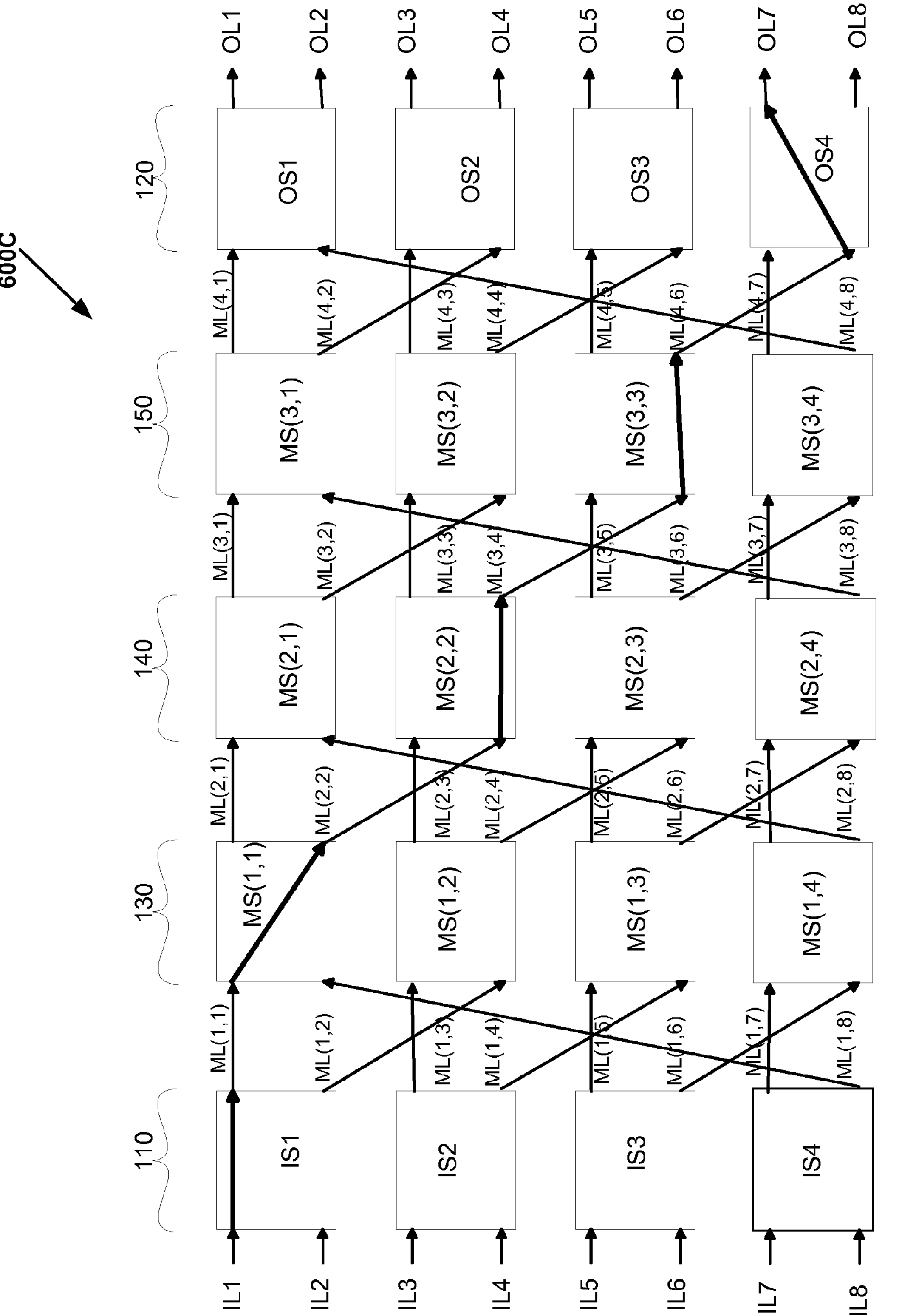
FIG. 6B

600B



110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
ML(1,1)
ML(1,2)
ML(1,7)
ML(1,8)
ML(2,1)
ML2,2)
ML(2,7)
ML(2,8)
ML(3,1)
ML(3,2)
ML(3,7)
ML(3,8)
ML(4,1)
ML(4,2)
ML(4,7)
ML(4,8)

FIG. 6C


600C
110
120
130
140
150
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
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IL5
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OL1
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ML(1,1)
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ML(2,8)
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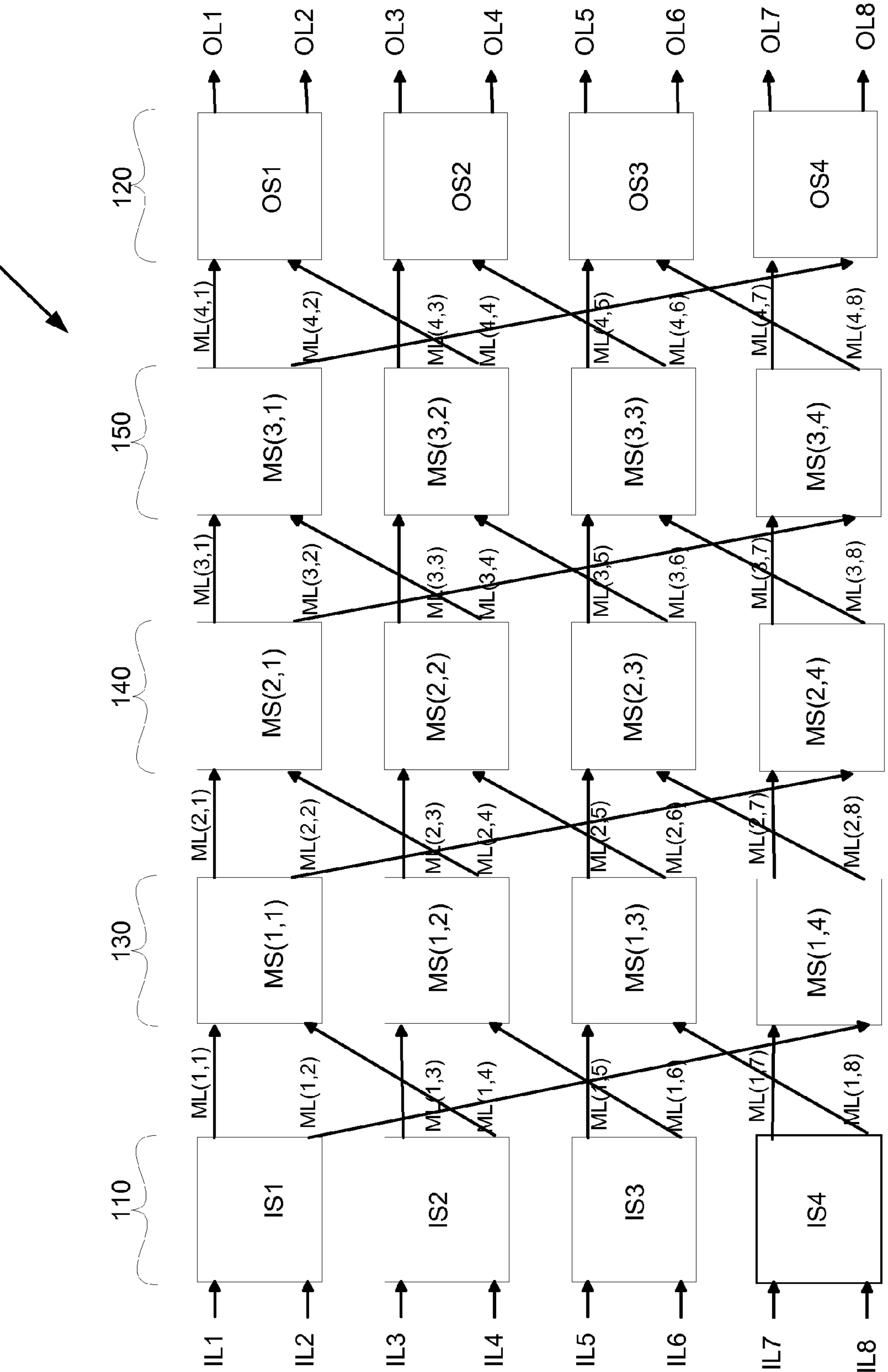
ML(3,2)
ML(3,3)
ML(3,4)
ML(3,5)
ML(3,6)
ML(3,7)
ML(3,8)
ML(4,1)
ML(4,2)
ML(4,3)
ML(4,4)
ML(4,5)
ML(4,6)
ML(4,7)
ML(4,8)

FIG. 6D

600D


110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
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OL7
OL8
ML(1,1)
ML(1,2)
ML(1,3)
ML(1,4)
ML(1,5)
ML(1,6)
ML(1,7)
ML(1,8)
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ML(2,2)
ML(2,3)
ML(2,4)
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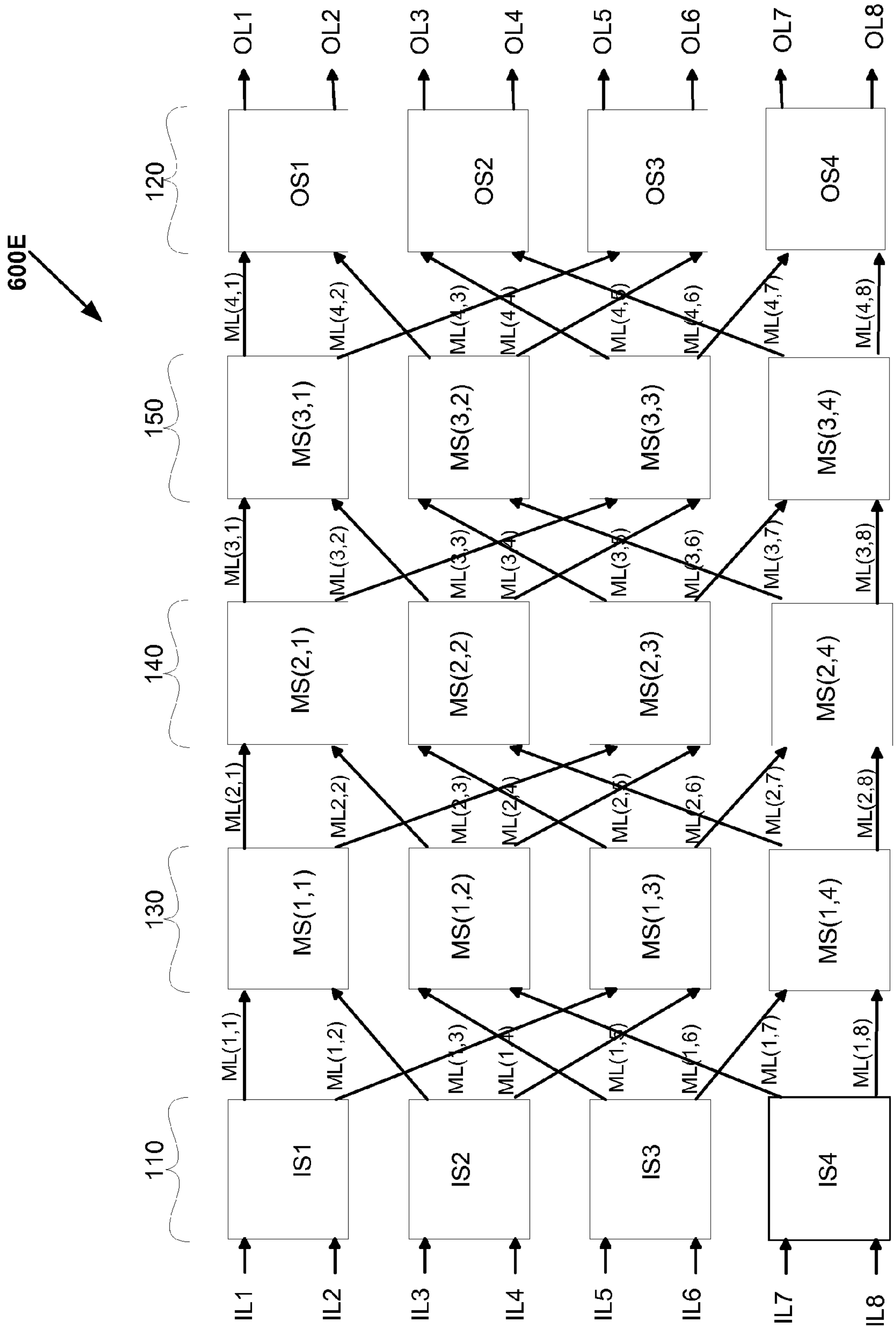
ML(2,6)
ML(2,7)
ML(2,8)
ML(3,1)
ML(3,2)
ML(3,3)
ML(3,4)
ML(3,5)
ML(3,6)
ML(3,7)
ML(3,8)
ML(4,1)
ML(4,2)
ML(4,3)
ML(4,4)
ML(4,5)
ML(4,6)
ML(4,7)
ML(4,8)

FIG. 6E


600E
110
120
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140
150
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IS3
IS4
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MS(1,4)
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MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
OL2
OL3
OL4
OL5
OL6
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OL8
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ML(1,2)
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ML(1,4)
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ML(1,7)
ML(1,8)
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ML2,2)
ML(2,3)
ML(2,4)
ML(2,5)
ML(2,6)
ML(2,7)
ML(2,8)
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ML(3,3)
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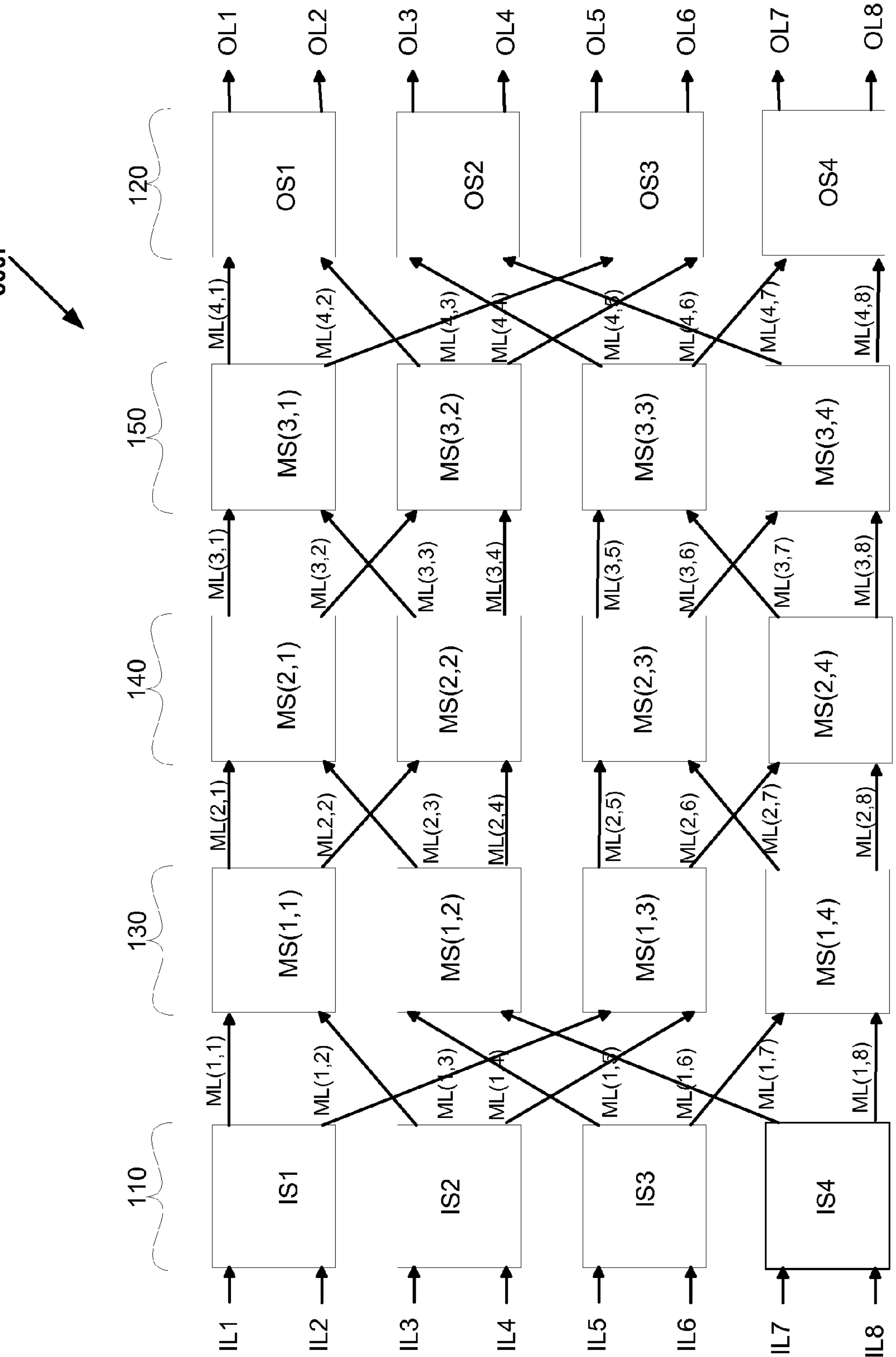
ML(4,1)
ML(4,2)
ML(4,3)
ML(4,4)
ML(4,5)
ML(4,6)
ML(4,7)
ML(4,8)

FIG. 6F


600F
110
120
130
140
150
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
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ML(2,8)
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ML(3,2)
ML(3,3)
ML(3,4)
ML(3,5)
ML(3,6)
ML(3,7)
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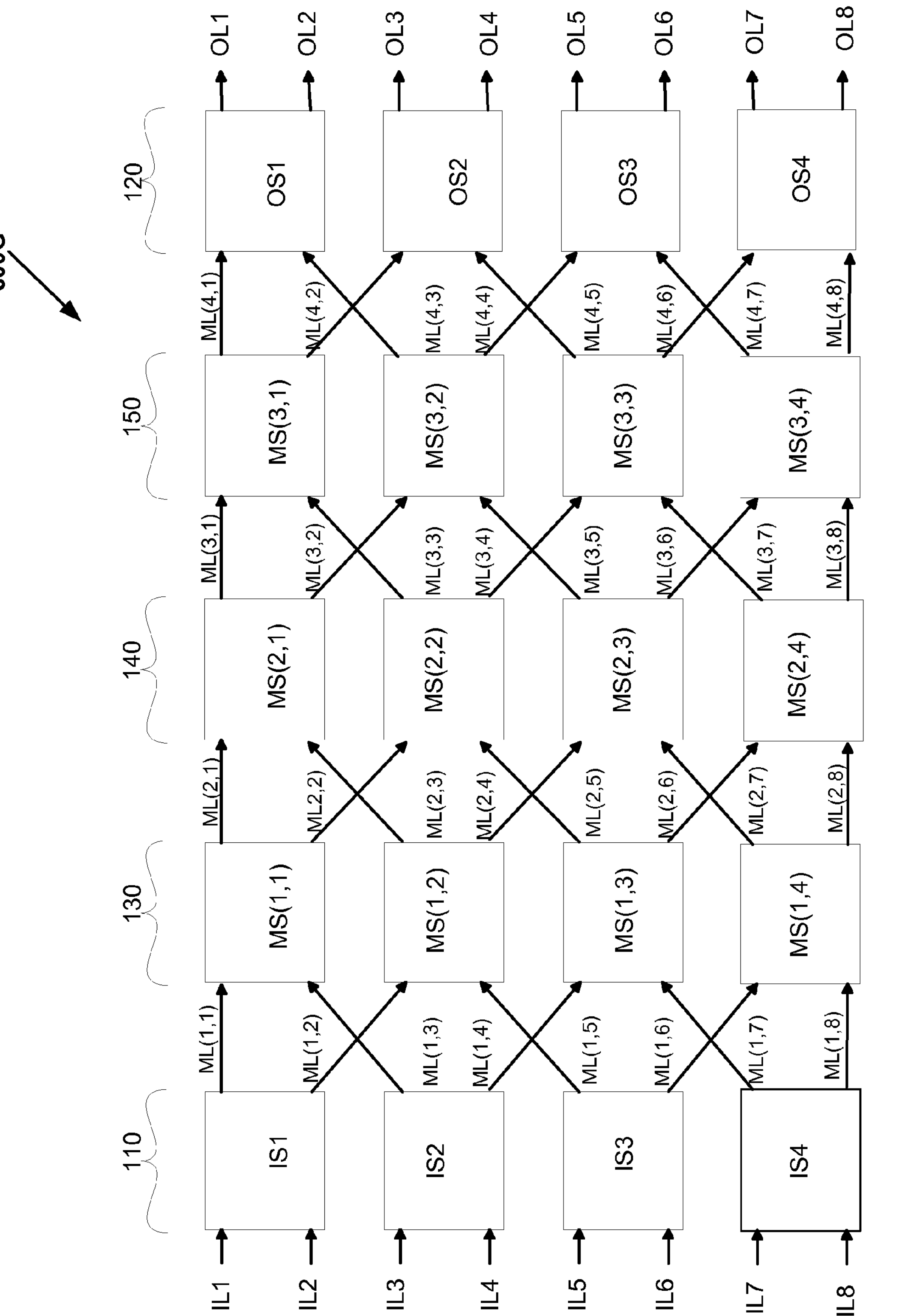
ML(4,1)
ML(4,2)
ML(4,3)
ML(4,6)
ML(4,8)

FIG. 6G


600G
110
120
130
140
150
IS1
IS2
IS3
IS4
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MS(1,2)
MS(1,3)
MS(1,4)
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MS(2,2)
MS(2,3)
MS(2,4)
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MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
OL1
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OL5
OL6
OL7
OL8
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ML(3,4)
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ML(3,6)
ML(3,7)
ML(3,8)
ML(4,1)
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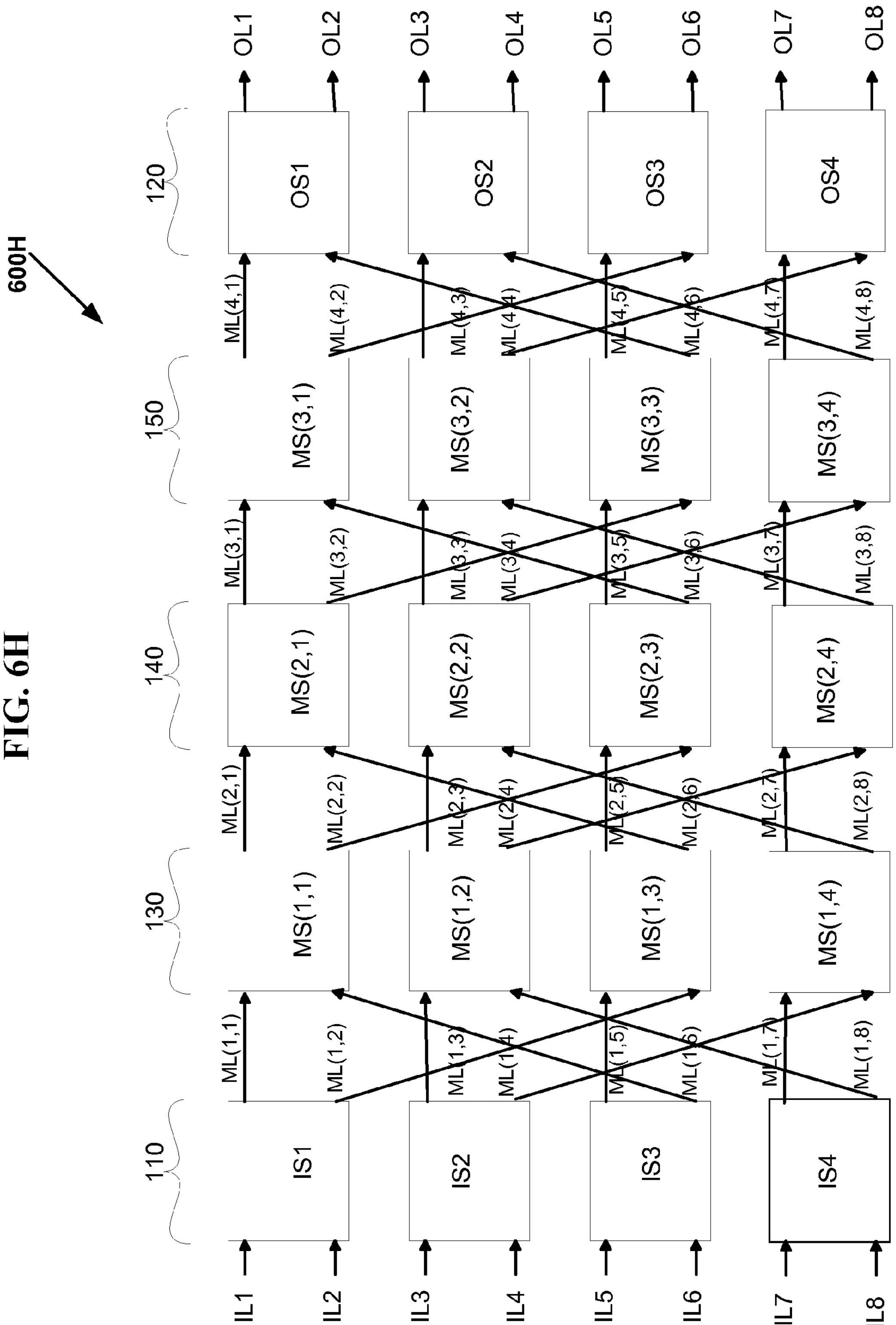
ML(4,3)
ML(4,4)
ML(4,5)
ML(4,6)
ML(4,7)
ML(4,8)


600H
110
120
130
140
150
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
IS1
IS2
IS3
IS4
ML(1,1)
ML(1,2)
ML(1,3)
ML(1,4)
ML(1,5)
ML(1,6)
ML(1,7)
ML(1,8)
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MS(1,2)
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MS(1,4)
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MS(2,4)
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ML(3,6)
ML(3,7)
ML(3,8)
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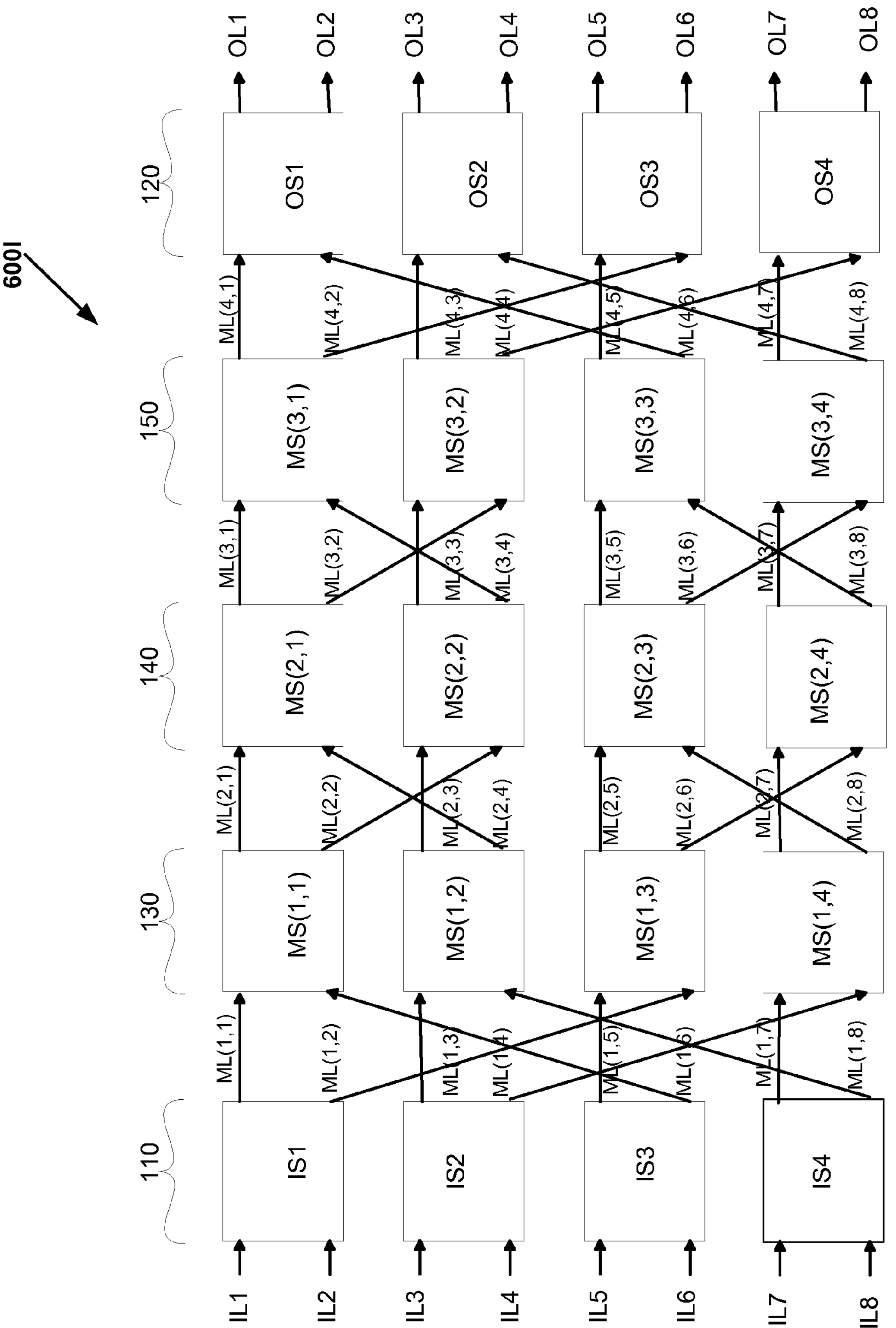
MS(3,3)
MS(3,4)
ML(4,1)
ML(4,2)
ML(4,3)
ML(4,4)
ML(4,5)
ML(4,6)
ML(4,7)
ML(4,8)
OS1
OS2
OS3
OS4
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8

FIG. 6H

FIG. 6I


600I
110
130
140
150
120
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
IS1
IS2
IS3
IS4
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MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
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ML(1,8)
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ML(2,3)
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ML(2,7)
ML(2,8)
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ML(3,7)
ML(3,8)
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ML(4,5)
ML(4,6)
ML(4,7)
ML(4,8)

FIG. 6J

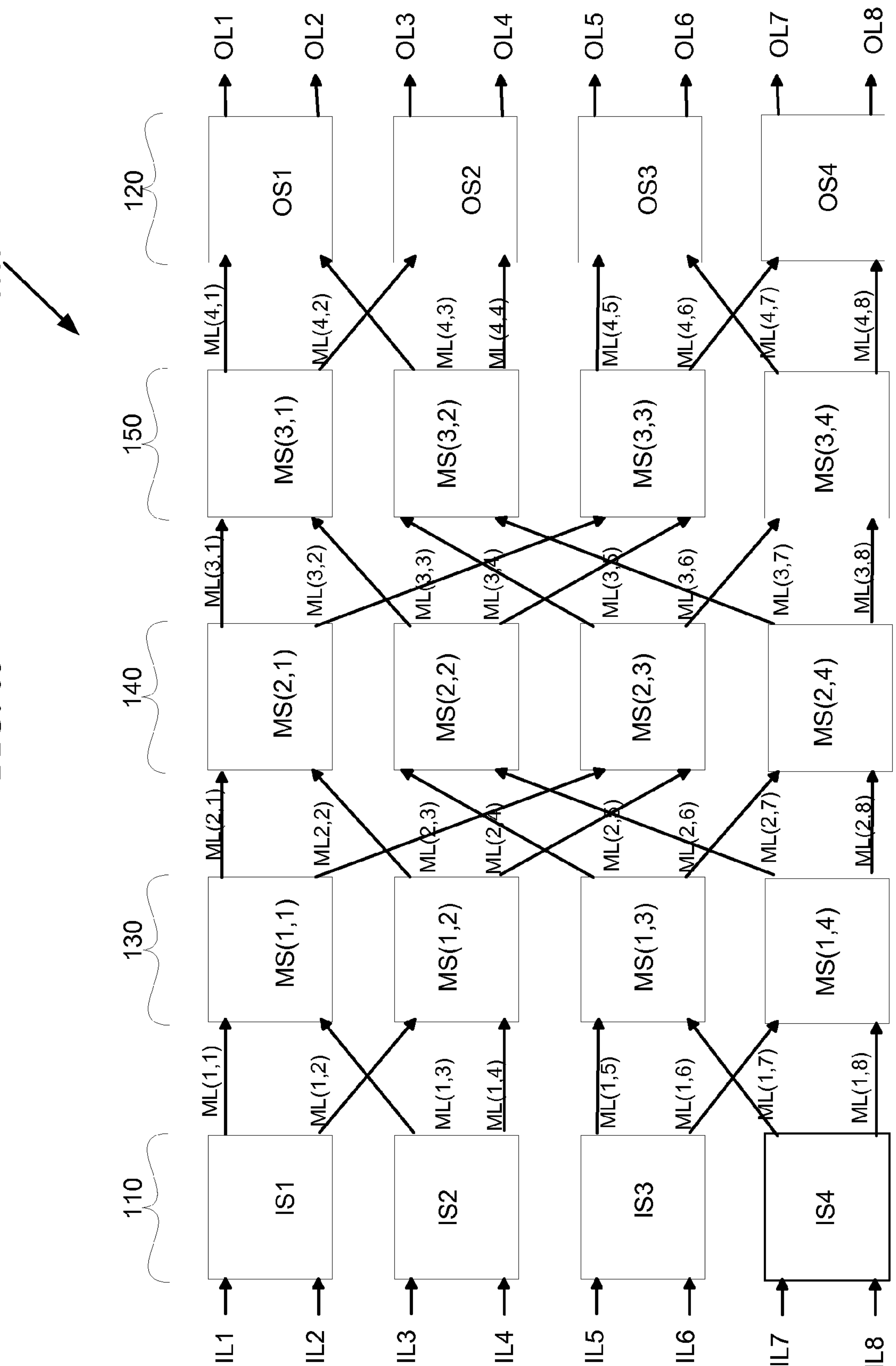

600J
110
120
130
140
150
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
IS1
IS2
IS3
IS4
ML(1,1)
ML(1,2)
ML(1,3)
ML(1,4)
ML(1,5)
ML(1,6)
ML(1,7)
ML(1,8)
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
ML(2,1)
ML2,2)
ML(2,3)
ML(2,4)
ML(2,5)
ML(2,6)
ML(2,7)
ML(2,8)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
ML(3,1)
ML(3,2)
ML(3,3)
ML(3,4)
ML(3,5)
ML(3,6)
ML(3,7)
ML(3,8)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
ML(4,1)
ML(4,2)
ML(4,3)
ML(4,4)
ML(4,5)
ML(4,6)
ML(4,7)
ML(4,8)
OS1
OS2
OS3
OS4
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8

FIG. 6K

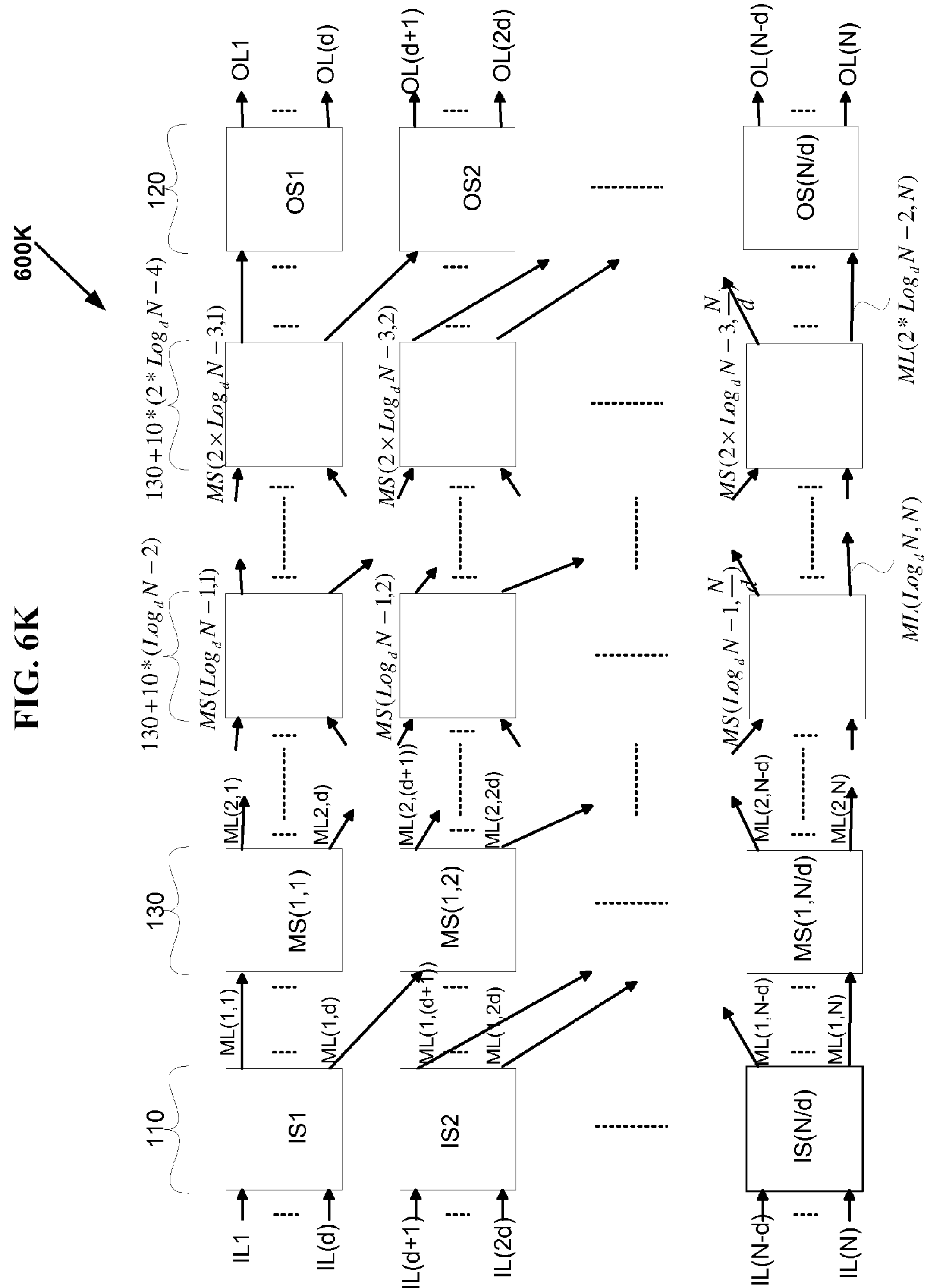
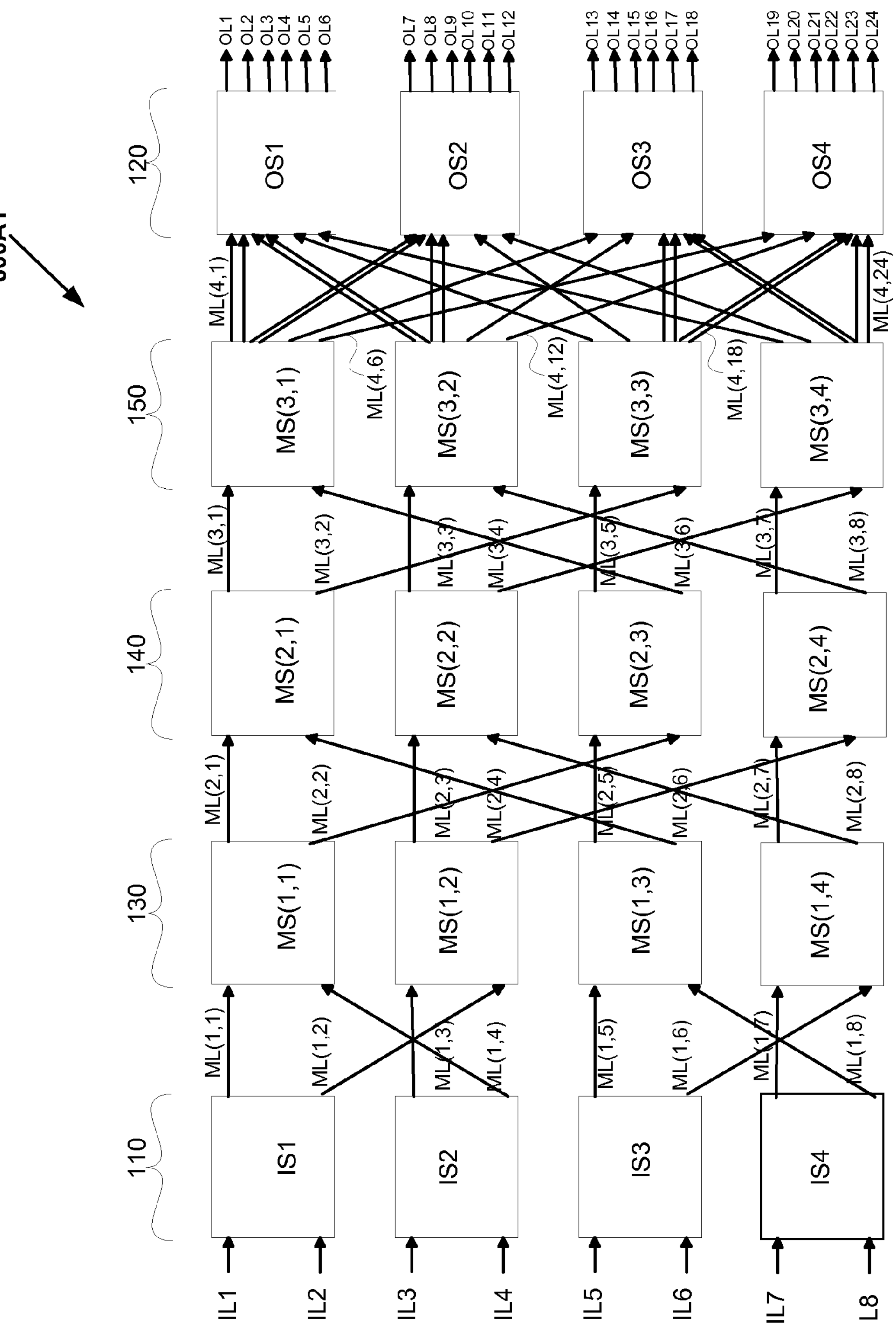

600K
110
130
120
IS1
IS2
IS(N/d)
MS(1,1)
MS(1,2)
MS(1,N/d)
OS1
OS2
OS(N/d)
IL1
IL(d)
IL(d+1)
IL(2d)
IL(N-d)
IL(N)
OL1
OL(d)
OL(d+1)
OL(2d)
OL(N-d)
OL(N)
ML(1,1)
ML(1,d)
ML(1,(d+1))
ML(1,2d)
ML(1,N-d)
ML(1,N)
ML(2,1)
ML(2,d)
ML(2,(d+1))
ML(2,2d)
ML(2,N-d)
ML(2,N)
130+10*(Log_d N-2)
130+10*(2*Log_d N-4)
MS(Log_d N-1,1)
MS(Log_d N-1,2)
MS(Log_d N-1,N/d)
MS(2×Log_d N-3,1)
MS(2×Log_d N-3,2)
MS(2×Log_d N-3,N/d)
ML(Log_d N,N)
ML(2*Log_d N-2,N)

FIG. 6A1


600A1
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
ML(1,1)
ML(1,2)
ML(1,3)
ML(1,4)
ML(1,5)
ML(1,6)
ML(1,7)
ML(1,8)
ML(2,1)
ML(2,2)
ML(2,3)
ML(2,4)
ML(2,5)
ML(2,6)
ML(2,7)
ML(2,8)
ML(3,1)
ML(3,2)
ML(3,3)
ML(3,4)
ML(3,5)
ML(3,6)
ML(3,7)
ML(3,8)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)
OL1
OL2
OL3
OL4
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OL11
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OL15
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OL17
OL18
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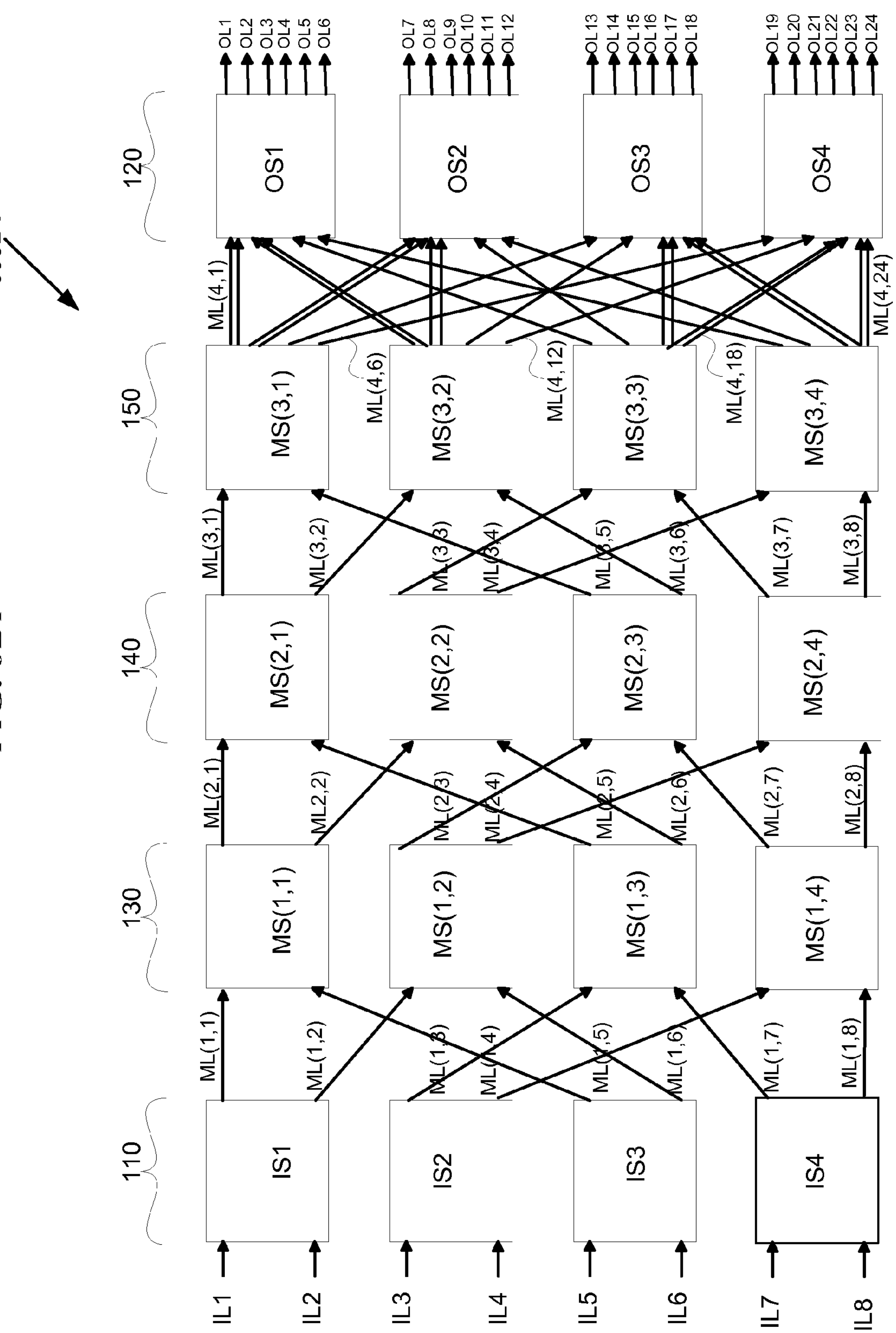
OL20
OL21
OL22
OL23
OL24

FIG. 6B1


600B1
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
ML(1,1)
ML(1,2)
ML(1,3)
ML(1,4)
ML(1,5)
ML(1,6)
ML(1,7)
ML(1,8)
ML(2,1)
ML(2,2)
ML(2,3)
ML(2,4)
ML(2,5)
ML(2,6)
ML(2,7)
ML(2,8)
ML(3,1)
ML(3,2)
ML(3,3)
ML(3,4)
ML(3,5)
ML(3,6)
ML(3,7)
ML(3,8)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)
OL1
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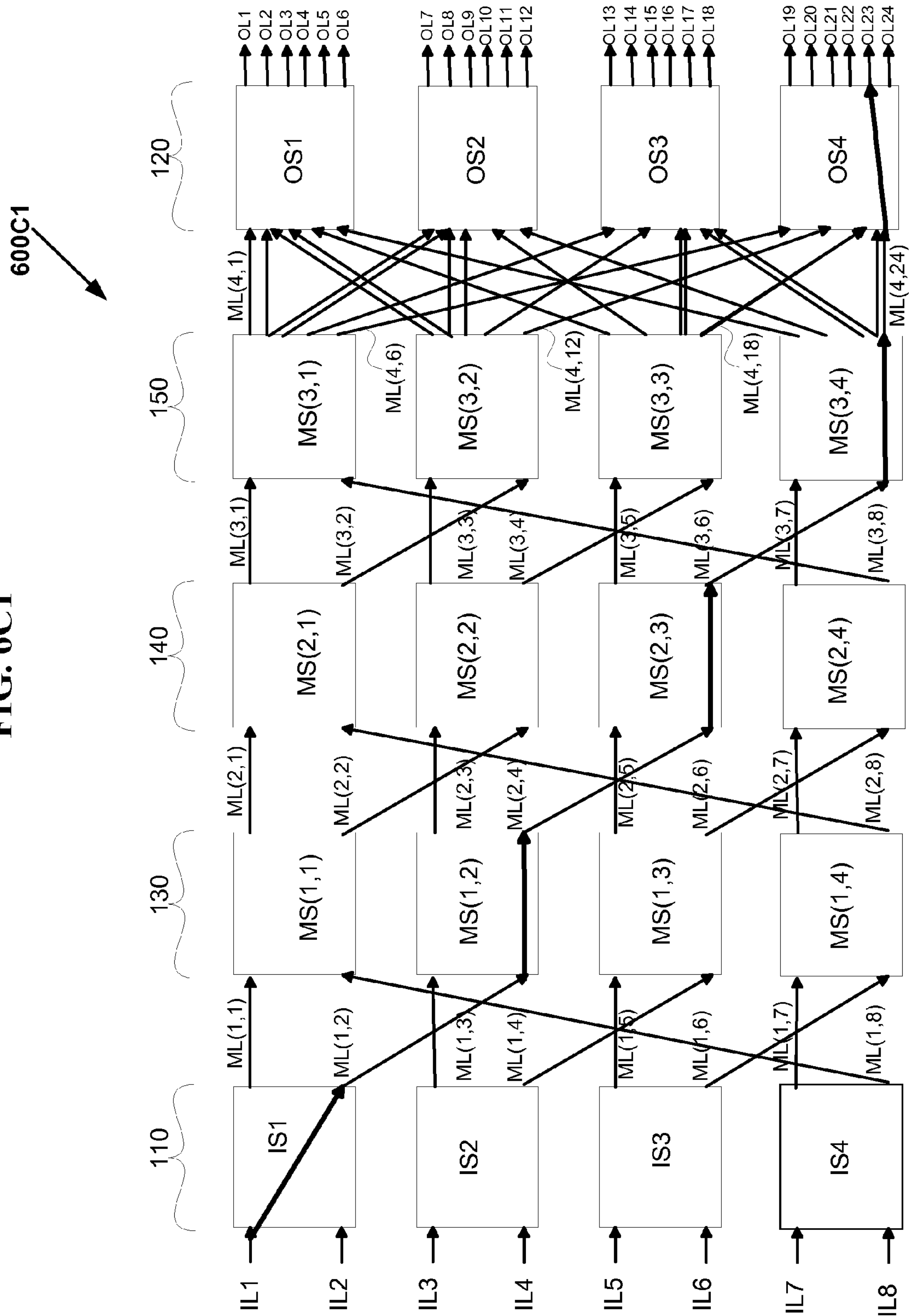
OL24

FIG. 6C1


600C1
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
ML(1,1)
ML(1,2)
ML(1,3)
ML(1,4)
ML(1,5)
ML(1,6)
ML(1,7)
ML(1,8)
ML(2,1)
ML(2,2)
ML(2,3)
ML(2,4)
ML(2,5)
ML(2,6)
ML(2,7)
ML(2,8)
ML(3,1)
ML(3,2)
ML(3,3)
ML(3,4)
ML(3,5)
ML(3,6)
ML(3,7)
ML(3,8)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)
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600D1

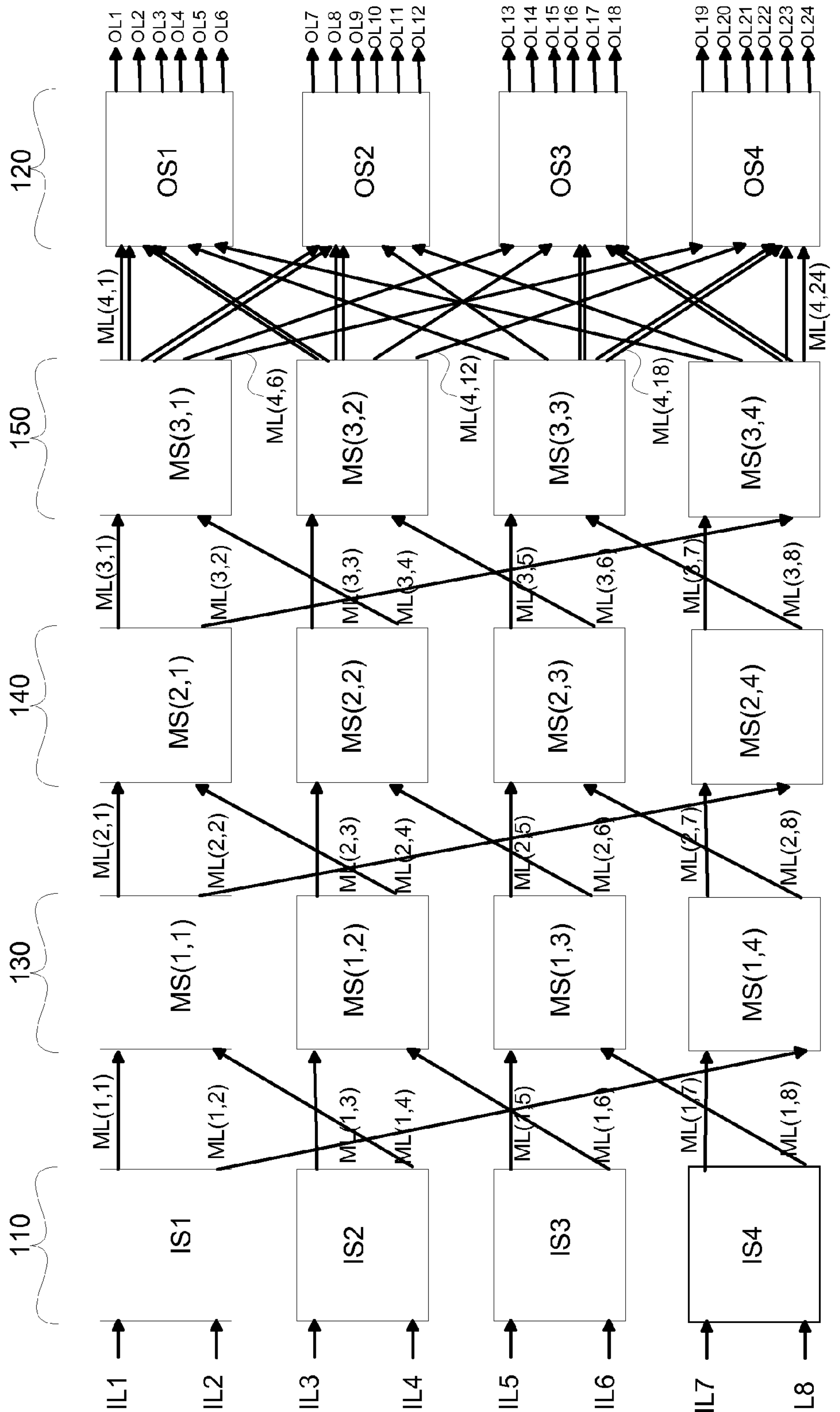
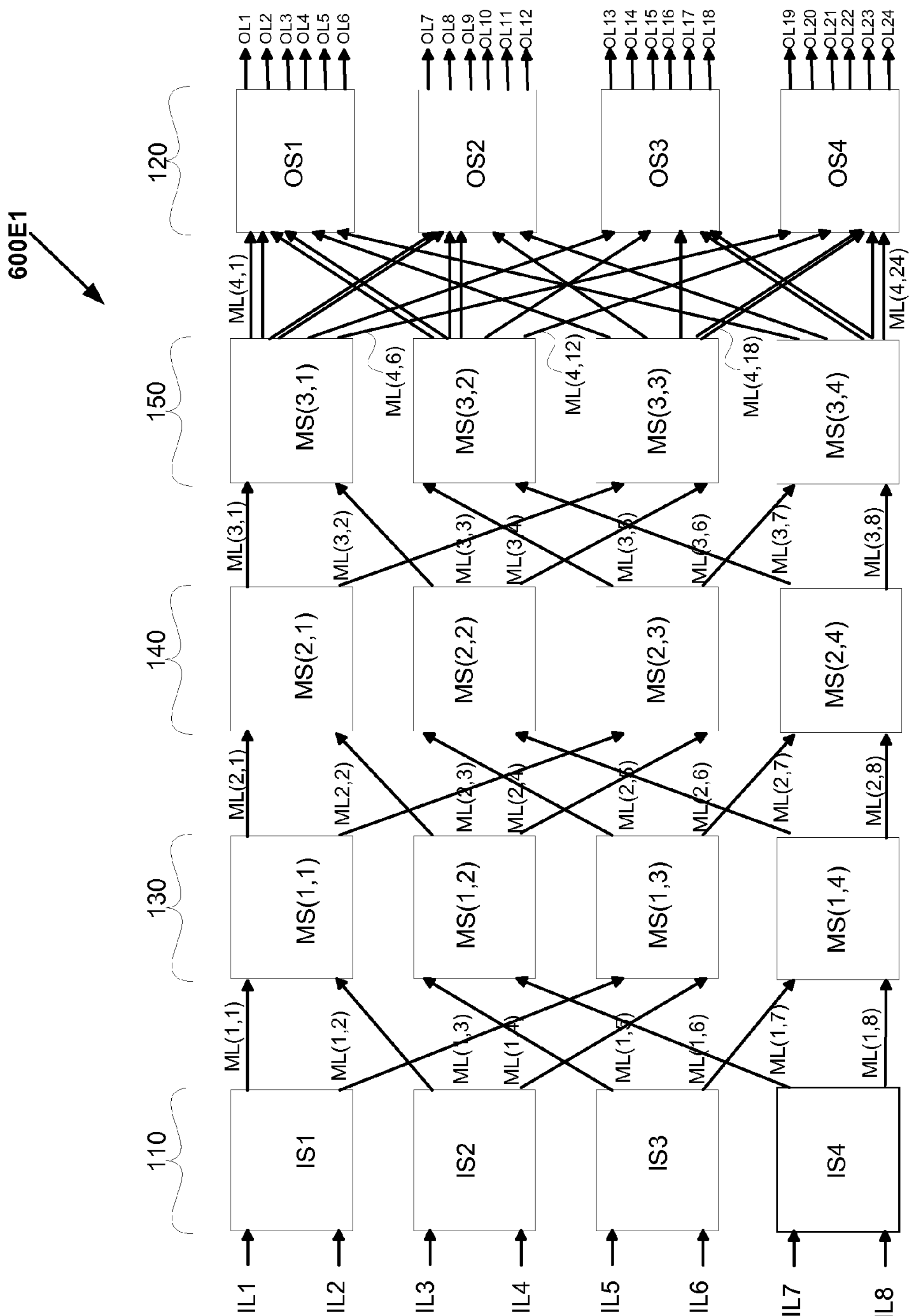


FIG. 6D1

FIG. 6E1


600E1
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
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ML(1,1)
ML(1,2)
ML(1,3)
ML(1,4)
ML(1,5)
ML(1,6)
ML(1,7)
ML(1,8)
ML(2,1)
ML2,2)
ML(2,3)
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ML(2,6)
ML(2,7)
ML(2,8)
ML(3,1)
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ML(3,4)
ML(3,5)
ML(3,6)
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ML(3,8)
ML(4,1)
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ML(4,12)
ML(4,18)
ML(4,24)
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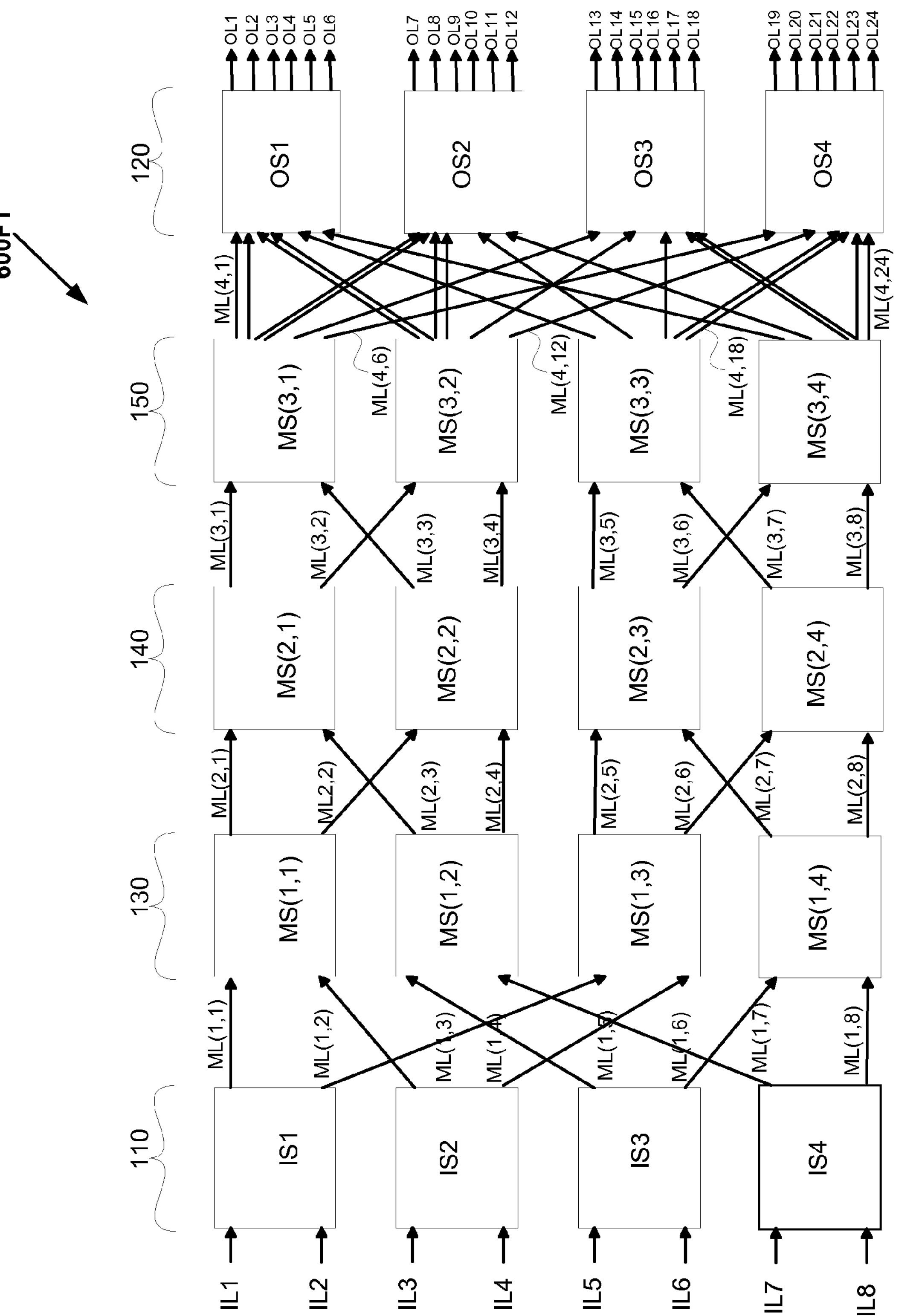
OL24


600F1
110
130
140
150
120
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
ML(1,1)
ML(1,2)
ML(1,3)
ML(1,6)
ML(1,7)
ML(1,8)
ML(2,1)
ML(2,2)
ML(2,3)
ML(2,4)
ML(2,5)
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ML(2,8)
ML(3,1)
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ML(3,3)
ML(3,4)
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ML(3,8)
ML(4,1)
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ML(4,12)
ML(4,18)
ML(4,24)
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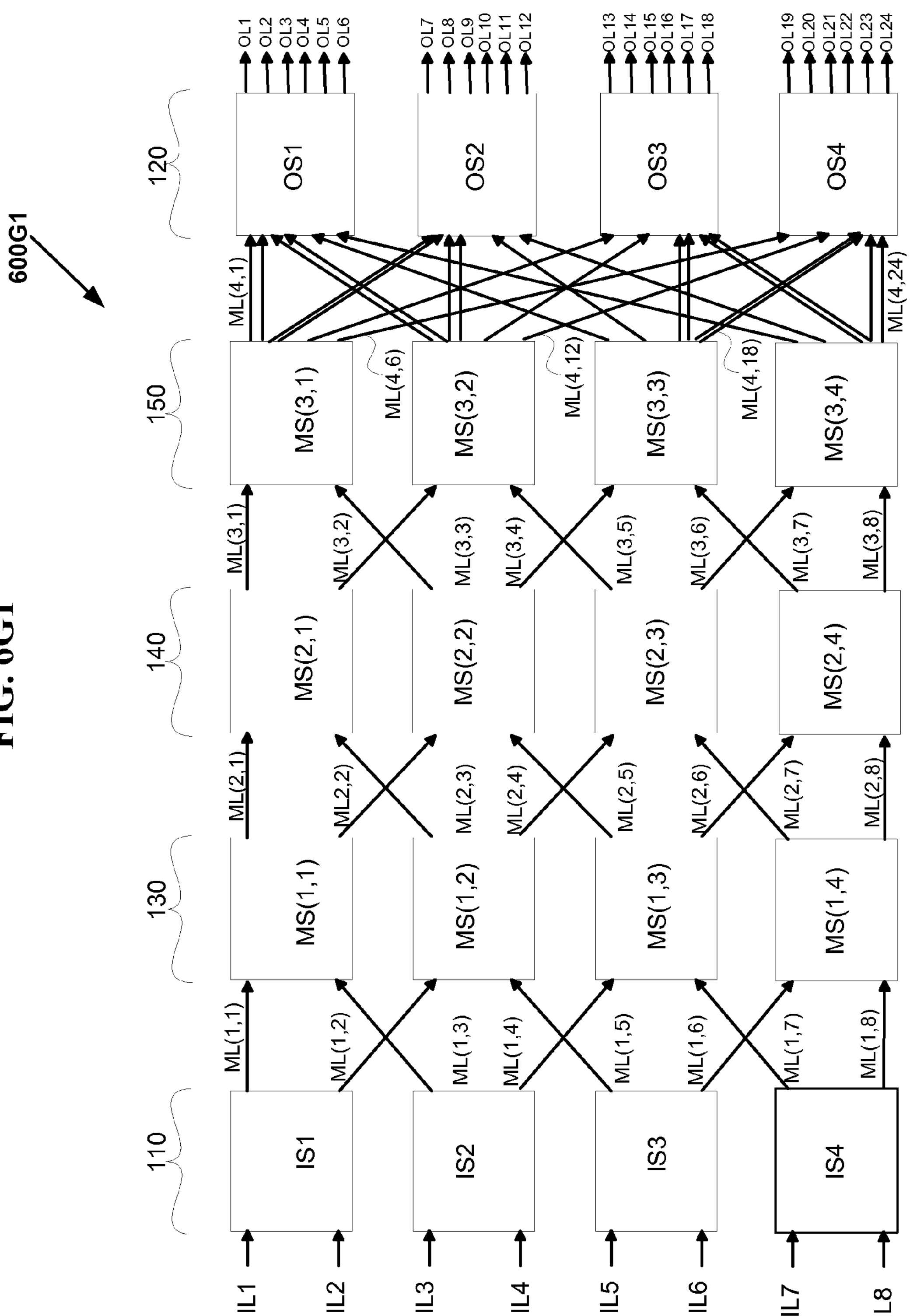
OL24

FIG. 6F1


600G1
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
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IL8
ML(1,1)
ML(1,2)
ML(1,3)
ML(1,4)
ML(1,5)
ML(1,6)
ML(1,7)
ML(1,8)
ML(2,1)
ML(2,2)
ML(2,3)
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ML(2,8)
ML(3,1)
ML(3,2)
ML(3,3)
ML(3,4)
ML(3,5)
ML(3,6)
ML(3,7)
ML(3,8)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)
OL1
OL2
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FIG. 6G1

FIG. 6H1

600H1

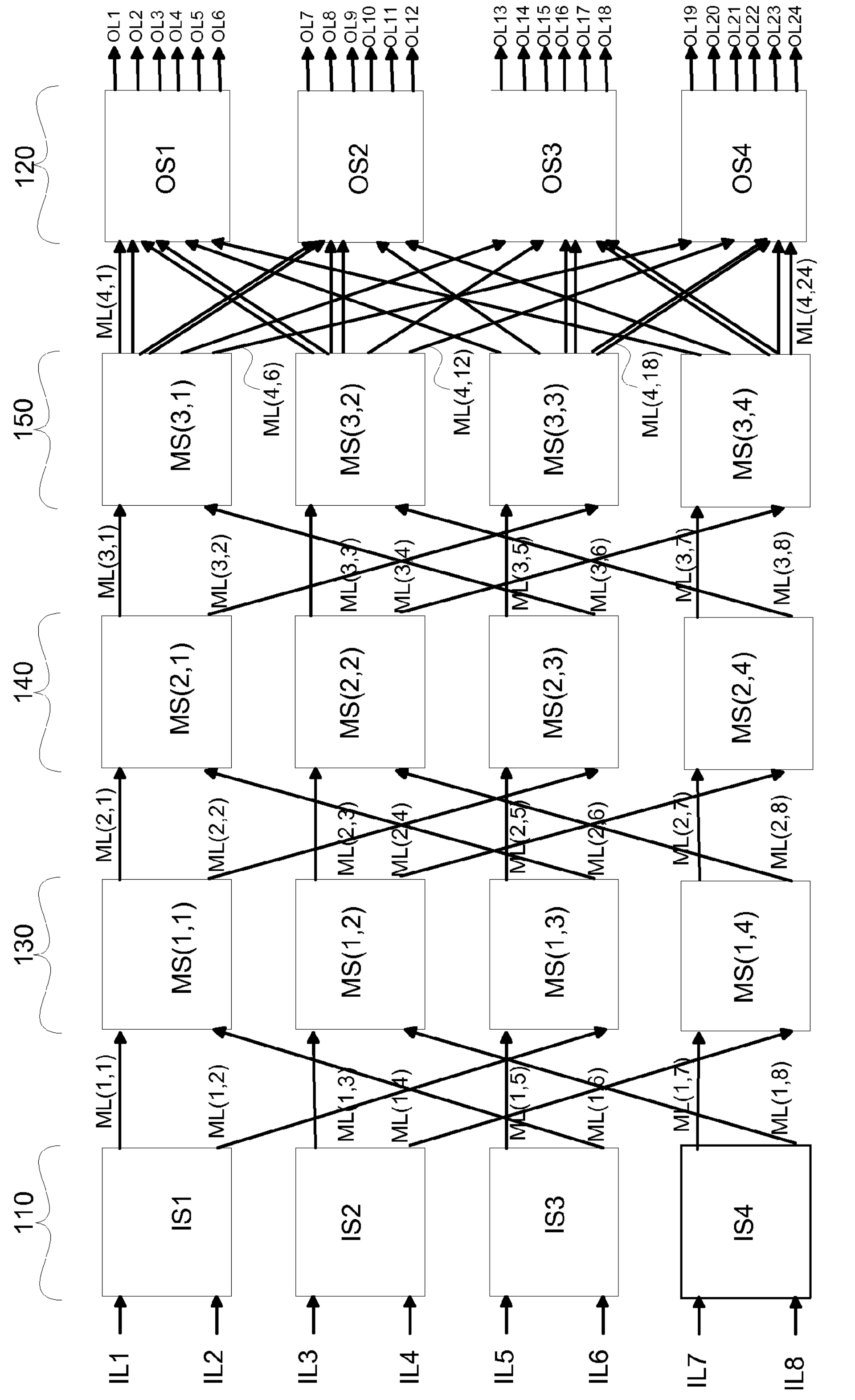
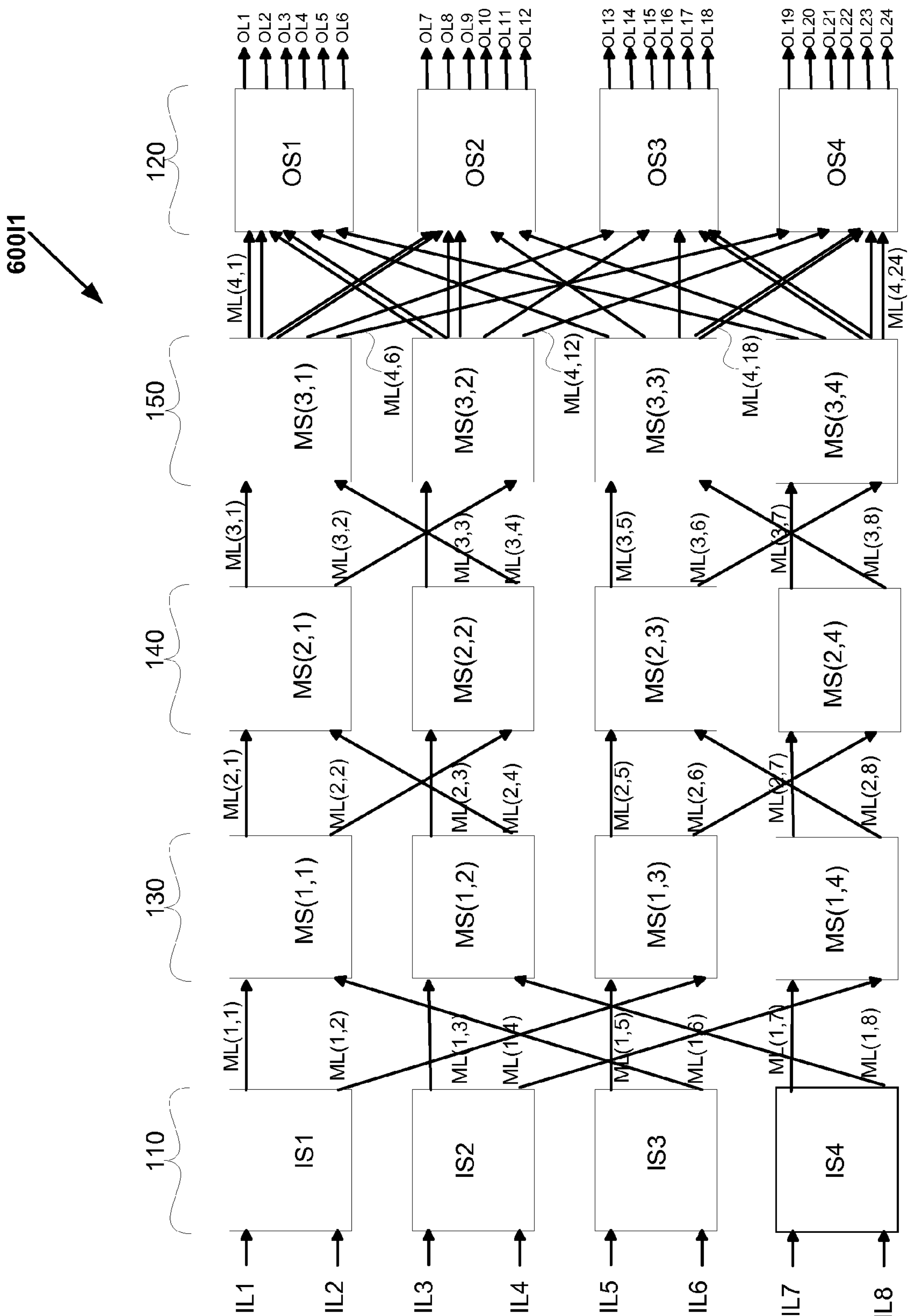


FIG. 6I1


600I1
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
ML(1,1)
ML(1,2)
ML(1,3)
ML(1,4)
ML(1,5)
ML(1,6)
ML(1,7)
ML(1,8)
ML(2,1)
ML(2,2)
ML(2,3)
ML(2,4)
ML(2,5)
ML(2,6)
ML(2,7)
ML(2,8)
ML(3,1)
ML(3,2)
ML(3,3)
ML(3,4)
ML(3,5)
ML(3,6)
ML(3,7)
ML(3,8)
ML(4,1)
ML(4,6)
ML(4,12)
ML(4,18)
ML(4,24)
OL1
OL2
OL3
OL4
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OL6
OL7
OL8
OL9
OL10
OL11
OL12
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OL14
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OL16
OL17
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OL19
OL20
OL21
OL22
OL23
OL24

FIG. 6J1

600J1

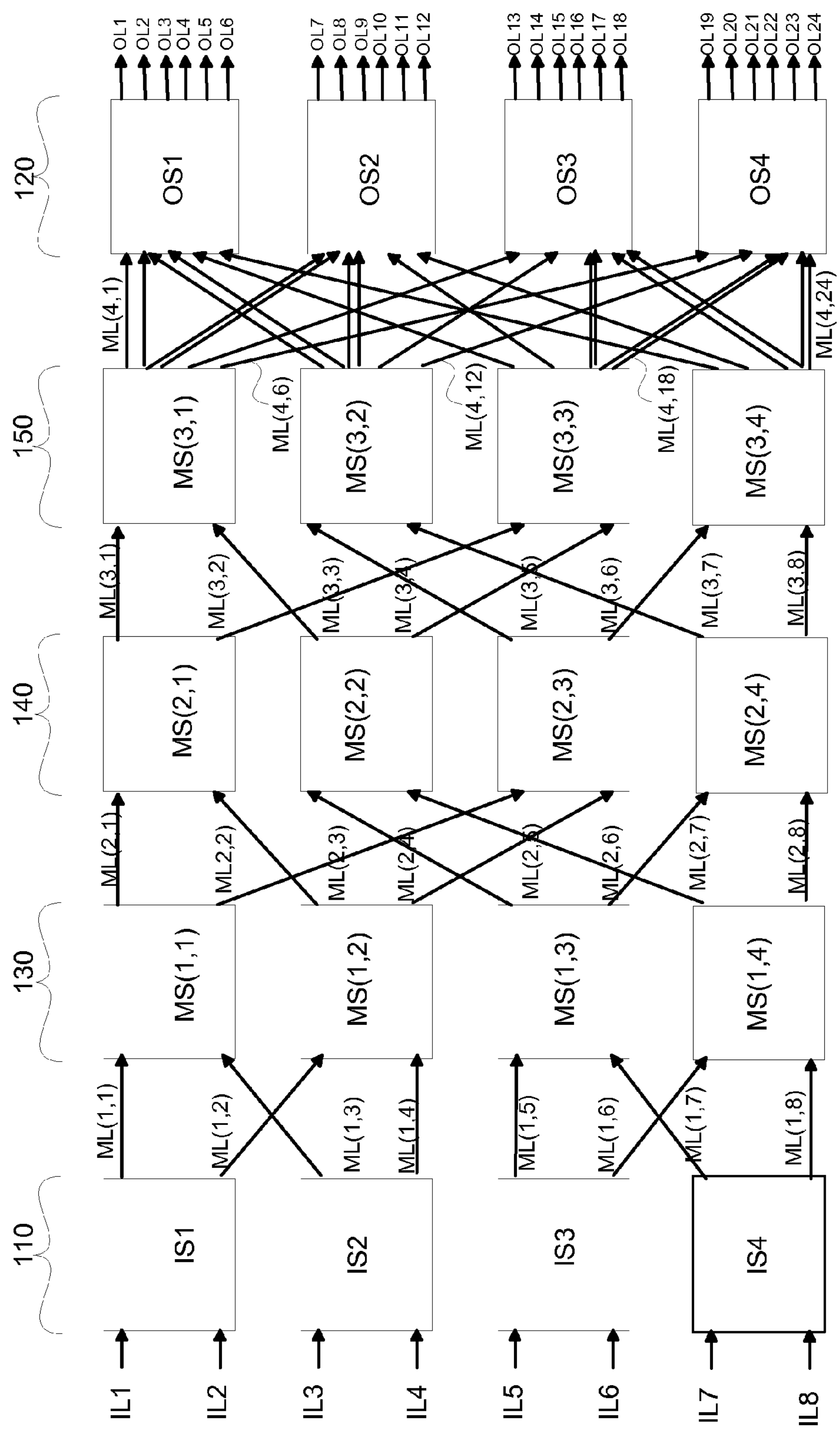


FIG. 6K1

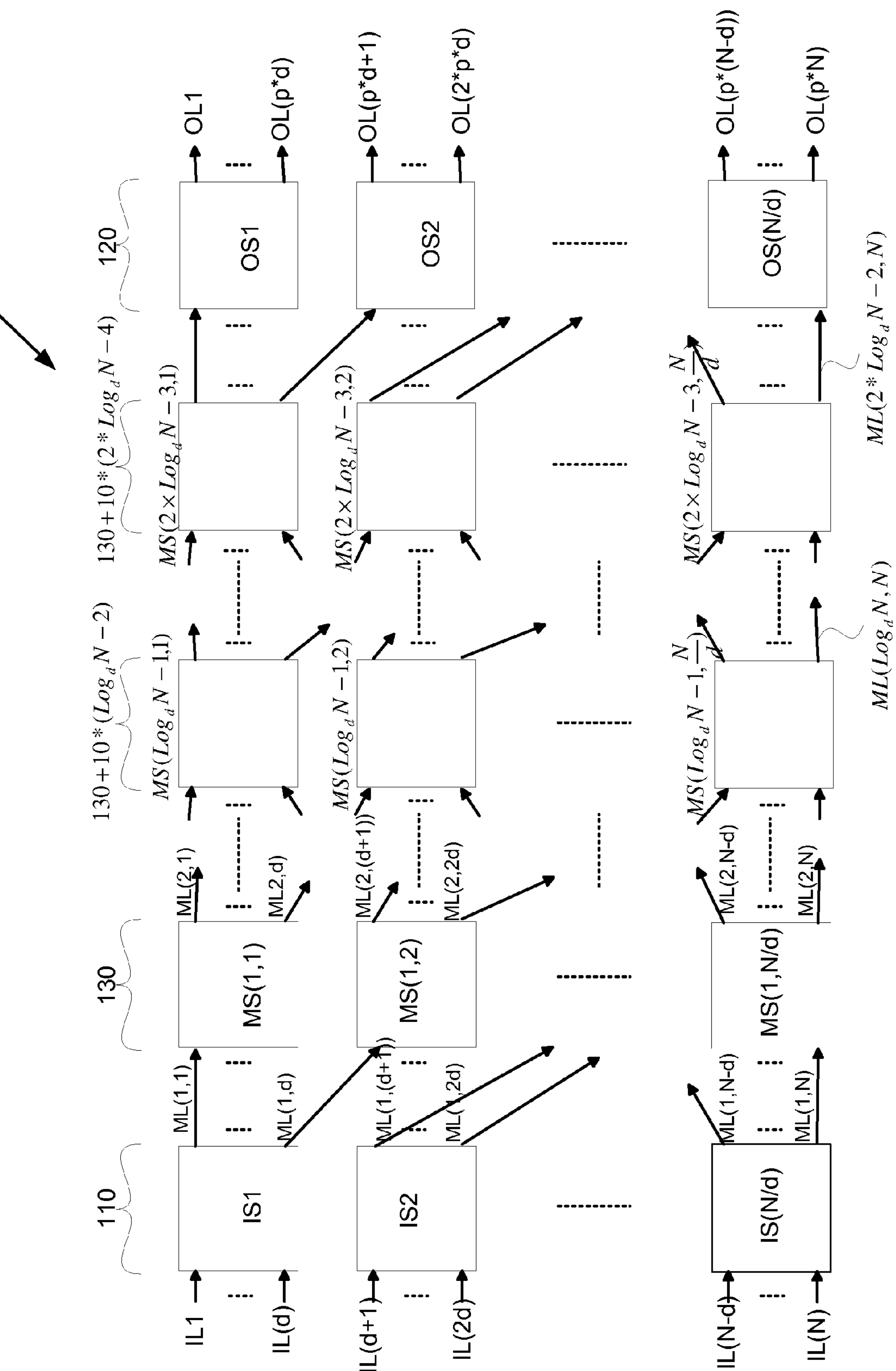
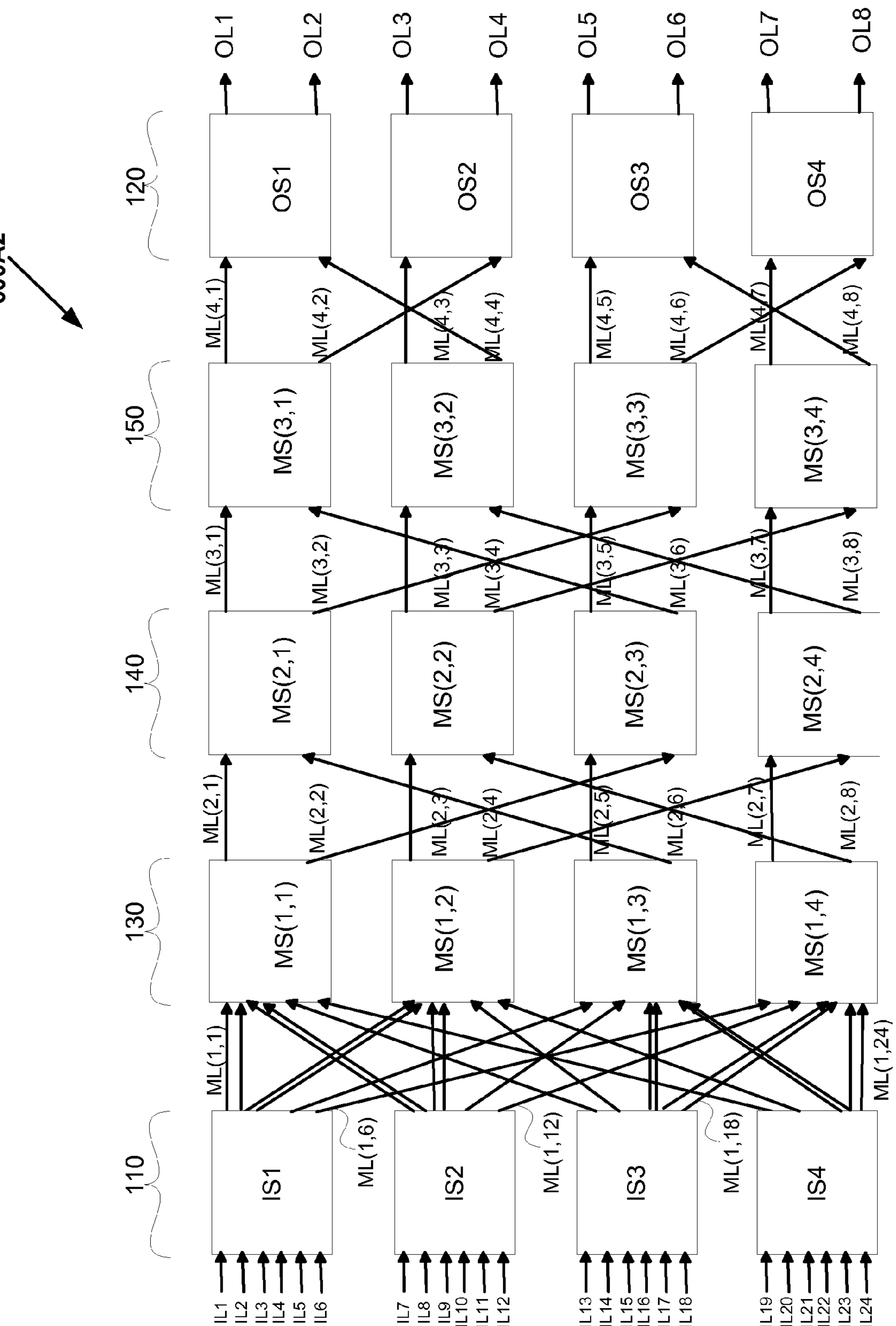

600K1
110
130
120
IS1
IS2
IS(N/d)
MS(1,1)
MS(1,2)
MS(1,N/d)
OS1
OS2
OS(N/d)
IL1
IL(d)
IL(d+1)
IL(2d)
IL(N-d)
IL(N)
ML(1,1)
ML(1,d)
ML(1,(d+1))
ML(1,2d)
ML(1,N-d)
ML(1,N)
ML(2,1)
ML(2,d)
ML(2,(d+1))
ML(2,2d)
ML(2,N-d)
ML(2,N)
OL1
OL(p*d)
OL(p*d+1)
OL(2*p*d)
OL(p*(N-d))
OL(p*N)

FIG. 6A2


600A2
110
120
130
140
150
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1) ML(2,2) ML(2,3) ML(2,4) ML(2,5) ML(2,6) ML(2,7) ML(2,8)
ML(3,1) ML(3,2) ML(3,3) ML(3,4) ML(3,5) ML(3,6) ML(3,7) ML(3,8)
ML(4,1) ML(4,2) ML(4,3) ML(4,4) ML(4,5) ML(4,6) ML(4,7) ML(4,8)
OL1 OL2 OL3 OL4 OL5 OL6 OL7 OL8

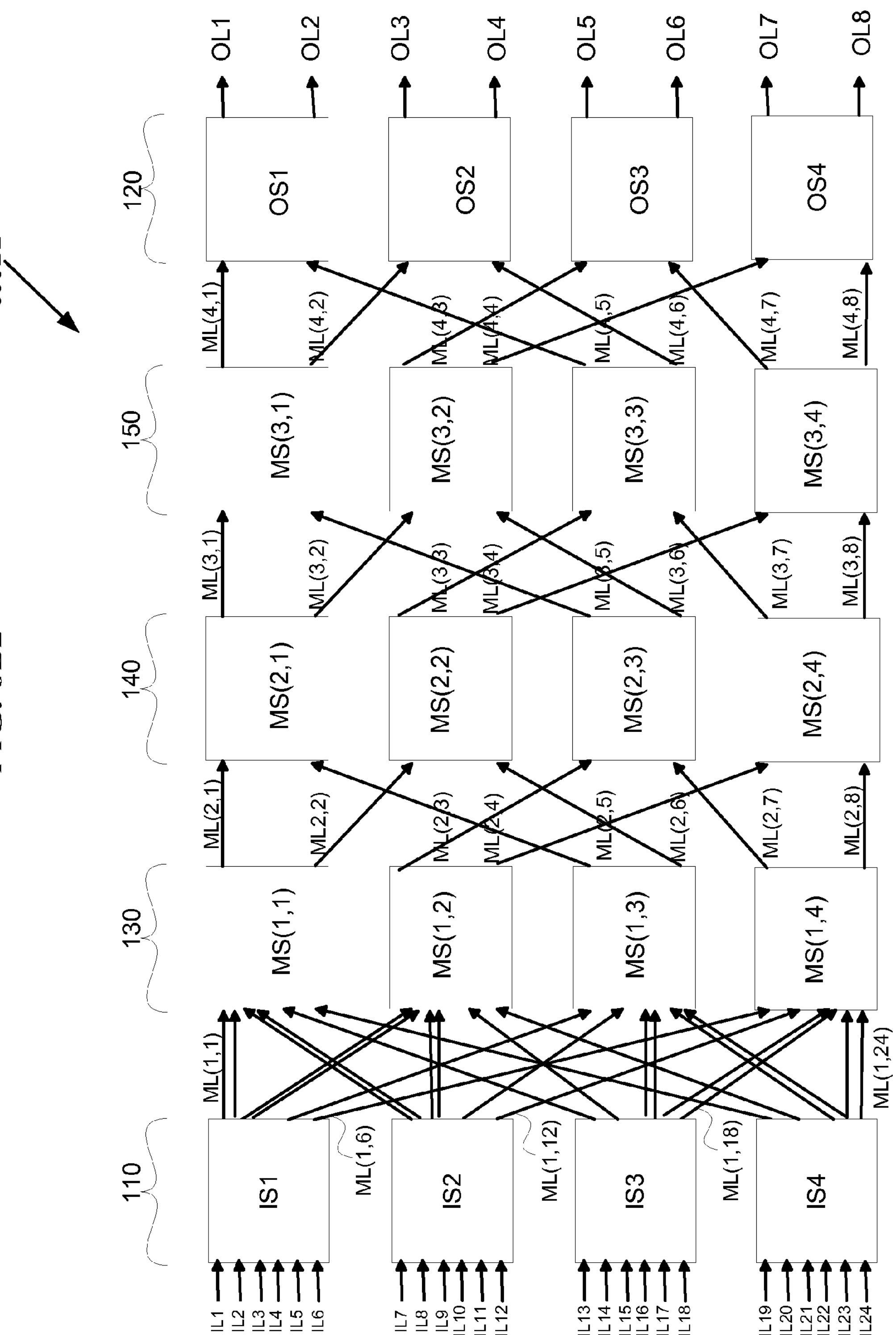

600B2
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1) ML(2,2) ML(2,3) ML(2,4) ML(2,5) ML(2,6) ML(2,7) ML(2,8)
ML(3,1) ML(3,2) ML(3,3) ML(3,4) ML(3,5) ML(3,6) ML(3,7) ML(3,8)
ML(4,1) ML(4,2) ML(4,3) ML(4,4) ML(4,5) ML(4,6) ML(4,7) ML(4,8)
OL1 OL2 OL3 OL4 OL5 OL6 OL7 OL8

FIG. 6B2

FIG. 6C2

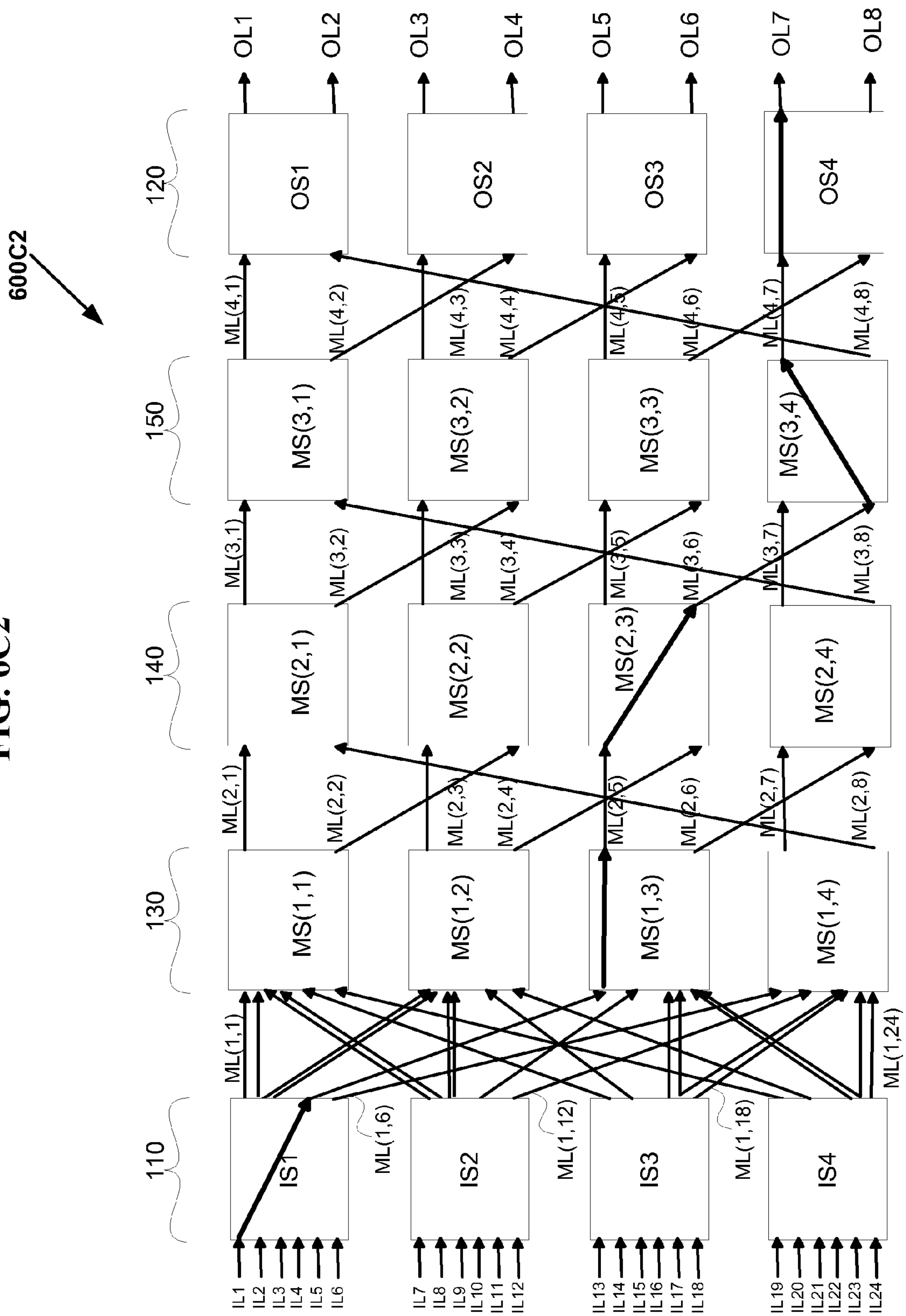

600C2
110
120
130
140
150
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1
IL2
IL3
IL4
IL5
IL6
IL7
IL8
IL9
IL10
IL11
IL12
IL13
IL14
IL15
IL16
IL17
IL18
IL19
IL20
IL21
IL22
IL23
IL24
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1)
ML(2,2)
ML(2,3)
ML(2,4)
ML(2,5)
ML(2,6)
ML(2,7)
ML(2,8)
ML(3,1)
ML(3,2)
ML(3,3)
ML(3,4)
ML(3,5)
ML(3,6)
ML(3,7)
ML(3,8)
ML(4,1)
ML(4,2)
ML(4,3)
ML(4,4)
ML(4,5)
ML(4,6)
ML(4,7)
ML(4,8)

FIG. 6D2

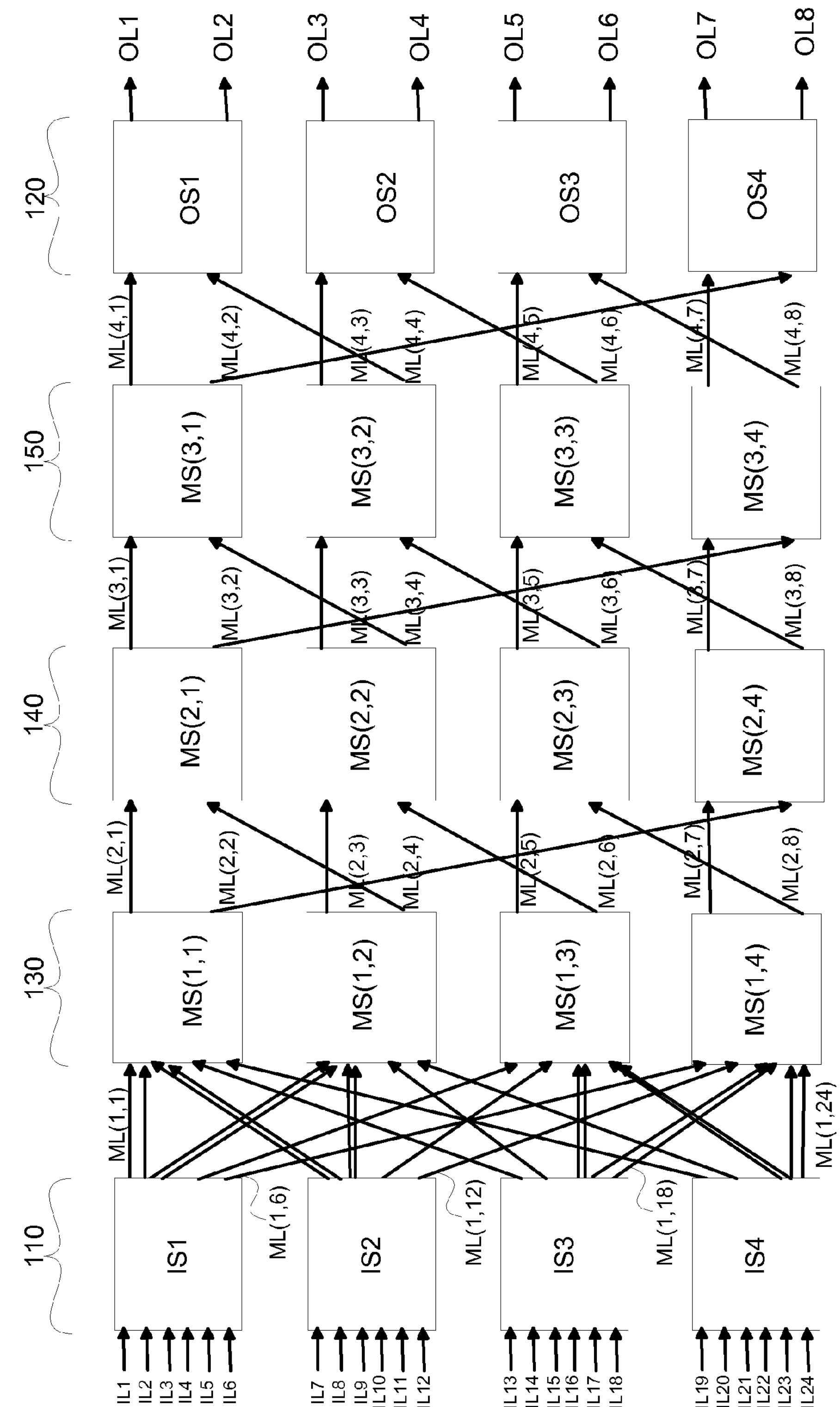
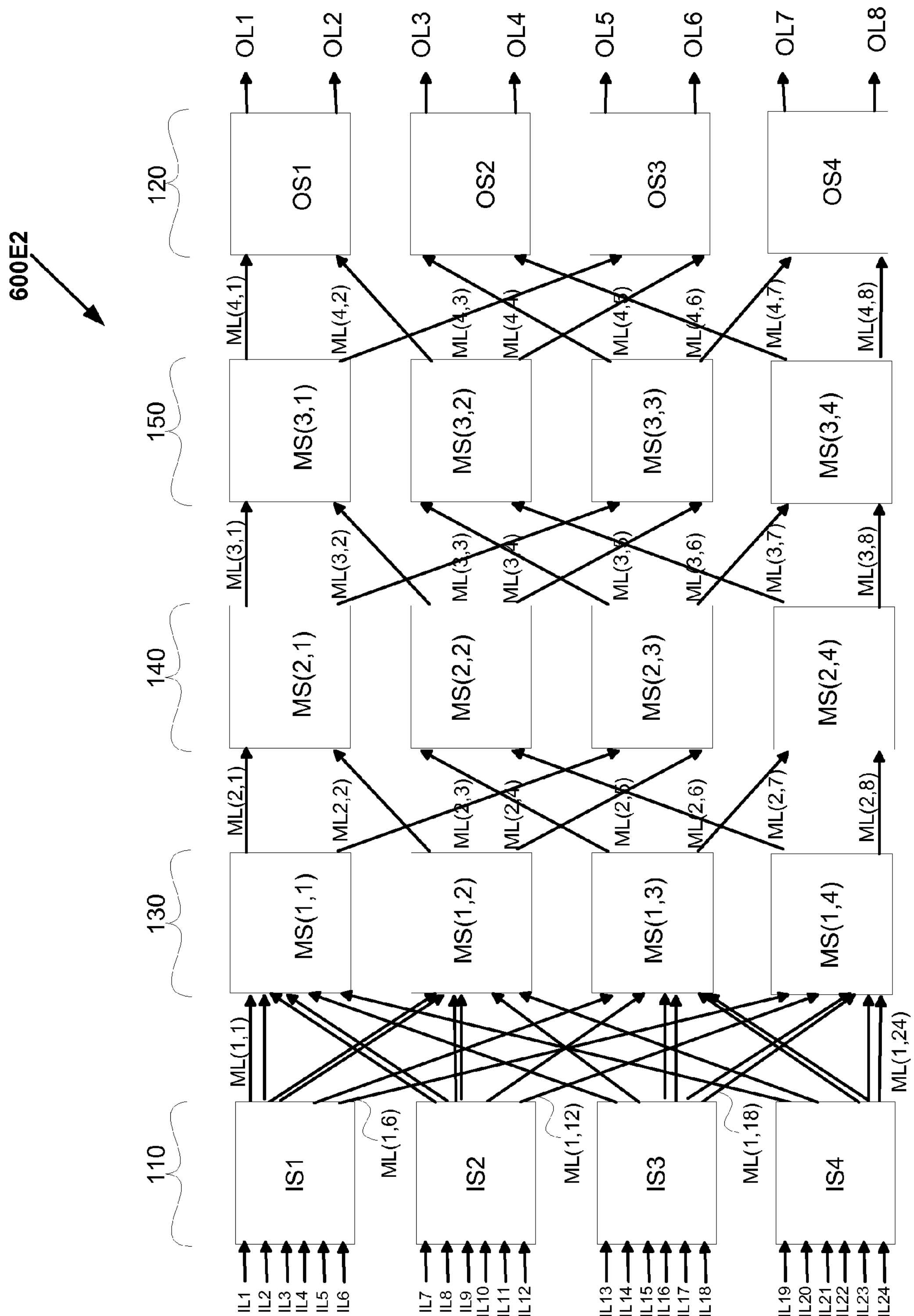

600D2
110
130
140
150
120
IS1
IS2
IS3
IS4
MS(1,1)
MS(1,2)
MS(1,3)
MS(1,4)
MS(2,1)
MS(2,2)
MS(2,3)
MS(2,4)
MS(3,1)
MS(3,2)
MS(3,3)
MS(3,4)
OS1
OS2
OS3
OS4
IL1 IL2 IL3 IL4 IL5 IL6
IL7 IL8 IL9 IL10 IL11 IL12
IL13 IL14 IL15 IL16 IL17 IL18
IL19 IL20 IL21 IL22 IL23 IL24
ML(1,1)
ML(1,6)
ML(1,12)
ML(1,18)
ML(1,24)
ML(2,1) ML(2,2) ML(2,3) ML(2,4) ML(2,5) ML(2,6) ML(2,7) ML(2,8)
ML(3,1) ML(3,2) ML(3,3) ML(3,4) ML(3,5) ML(3,6) ML(3,7) ML(3,8)
ML(4,1) ML(4,2) ML(4,3) ML(4,4) ML(4,5) ML(4,6) ML(4,7) ML(4,8)
OL1 OL2 OL3 OL4 OL5 OL6 OL7 OL8

FIG. 6E2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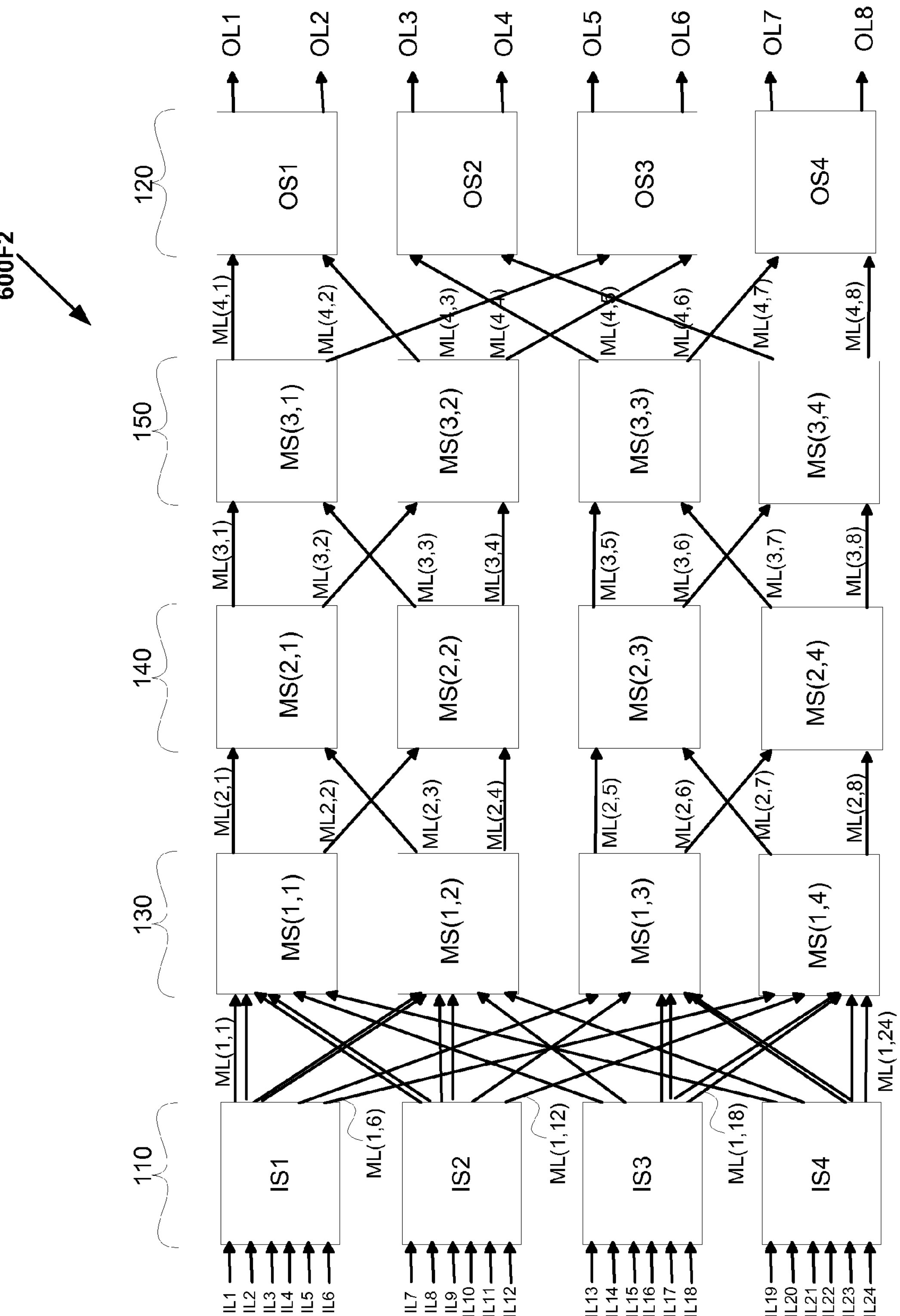
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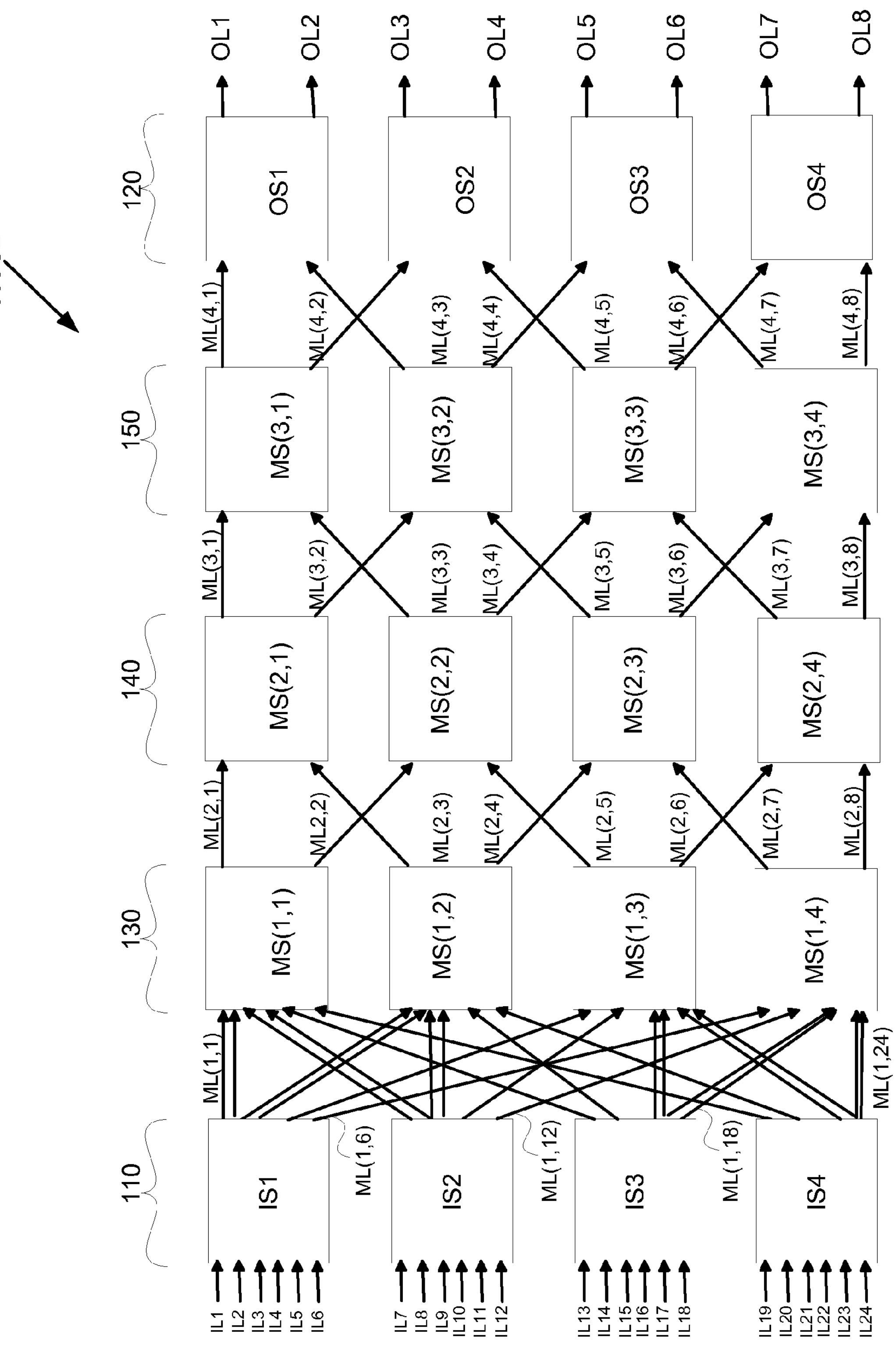
FIG. 6F2

FIG. 6G2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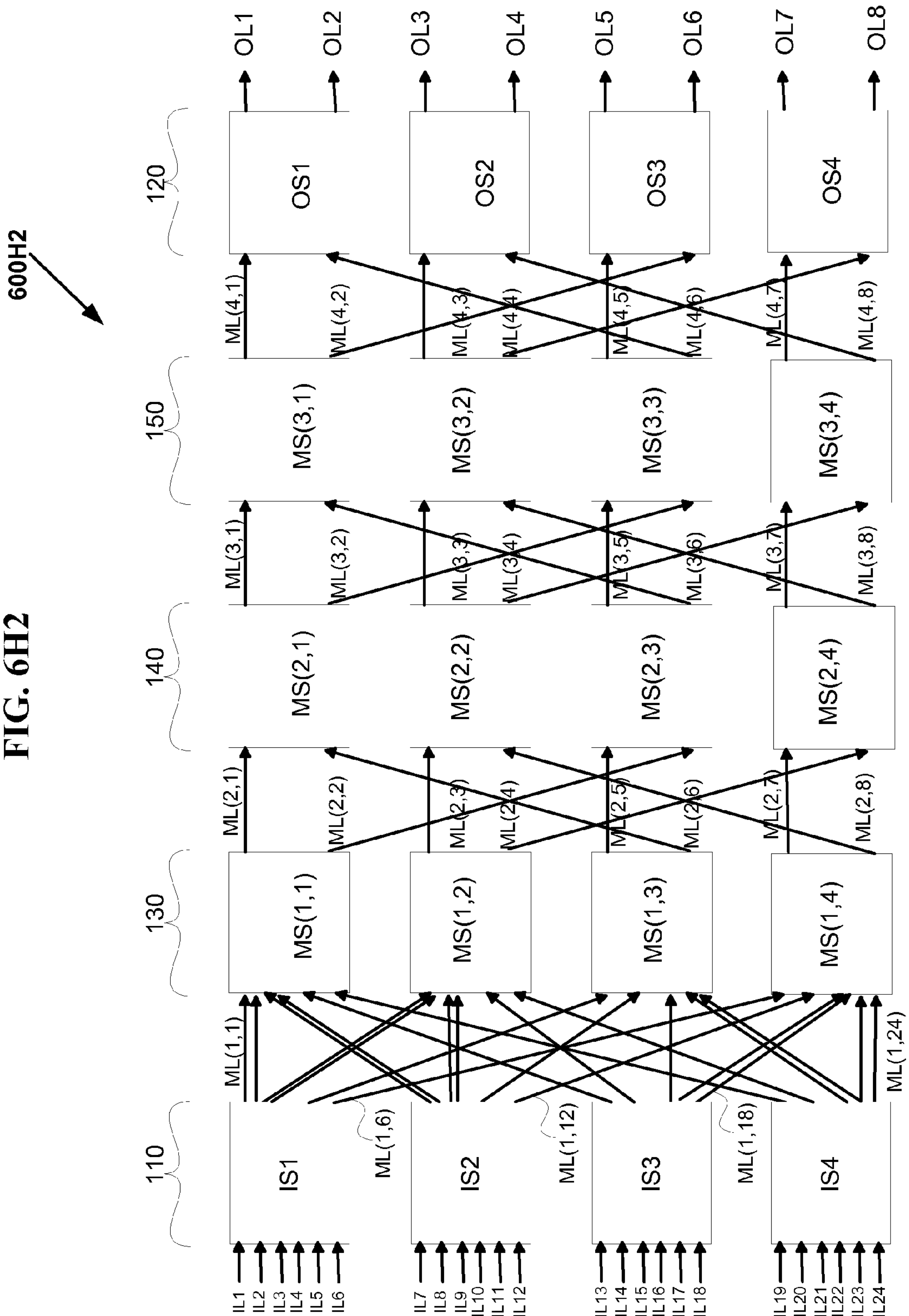
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FIG. 6H2

FIG. 6I2

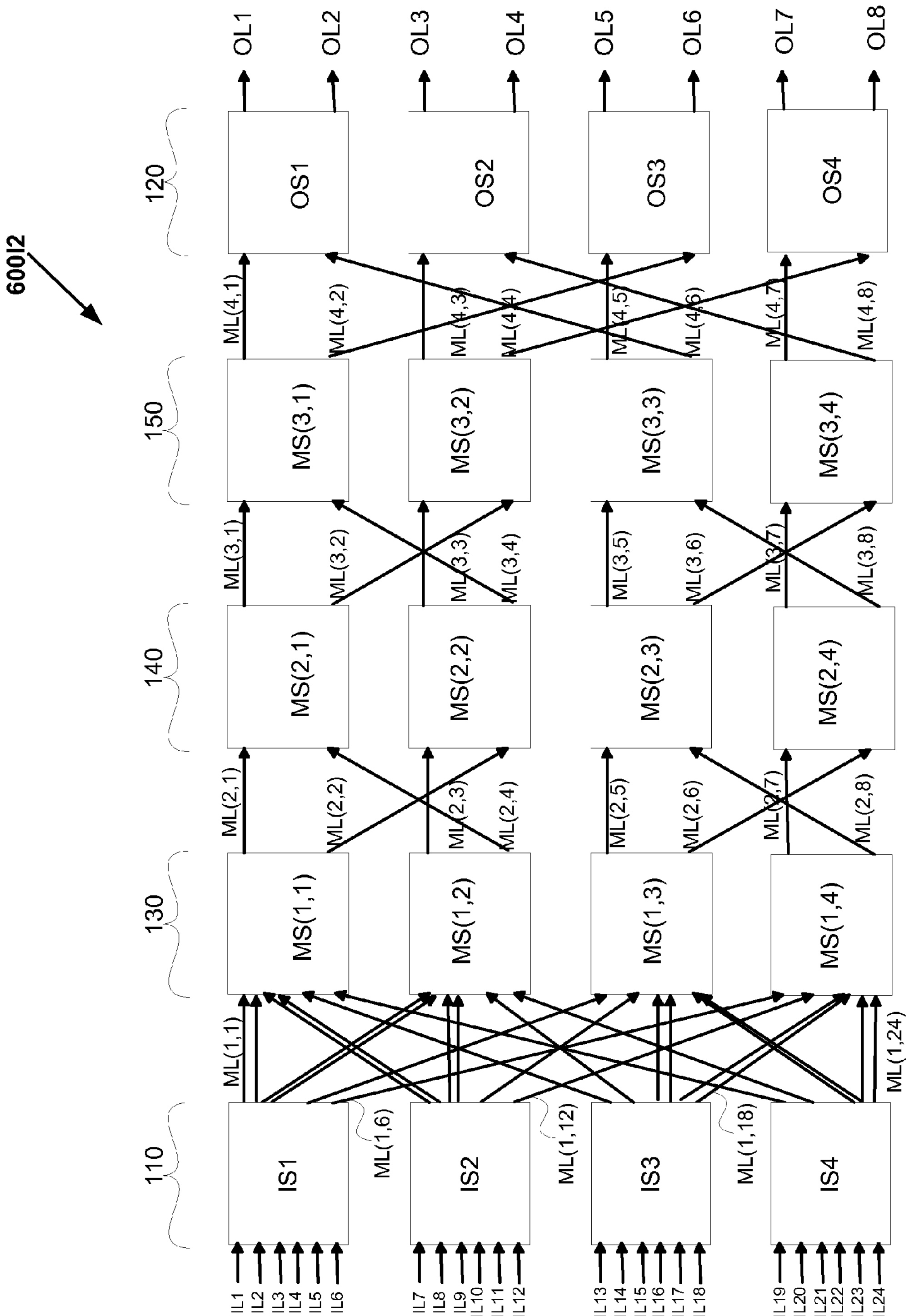
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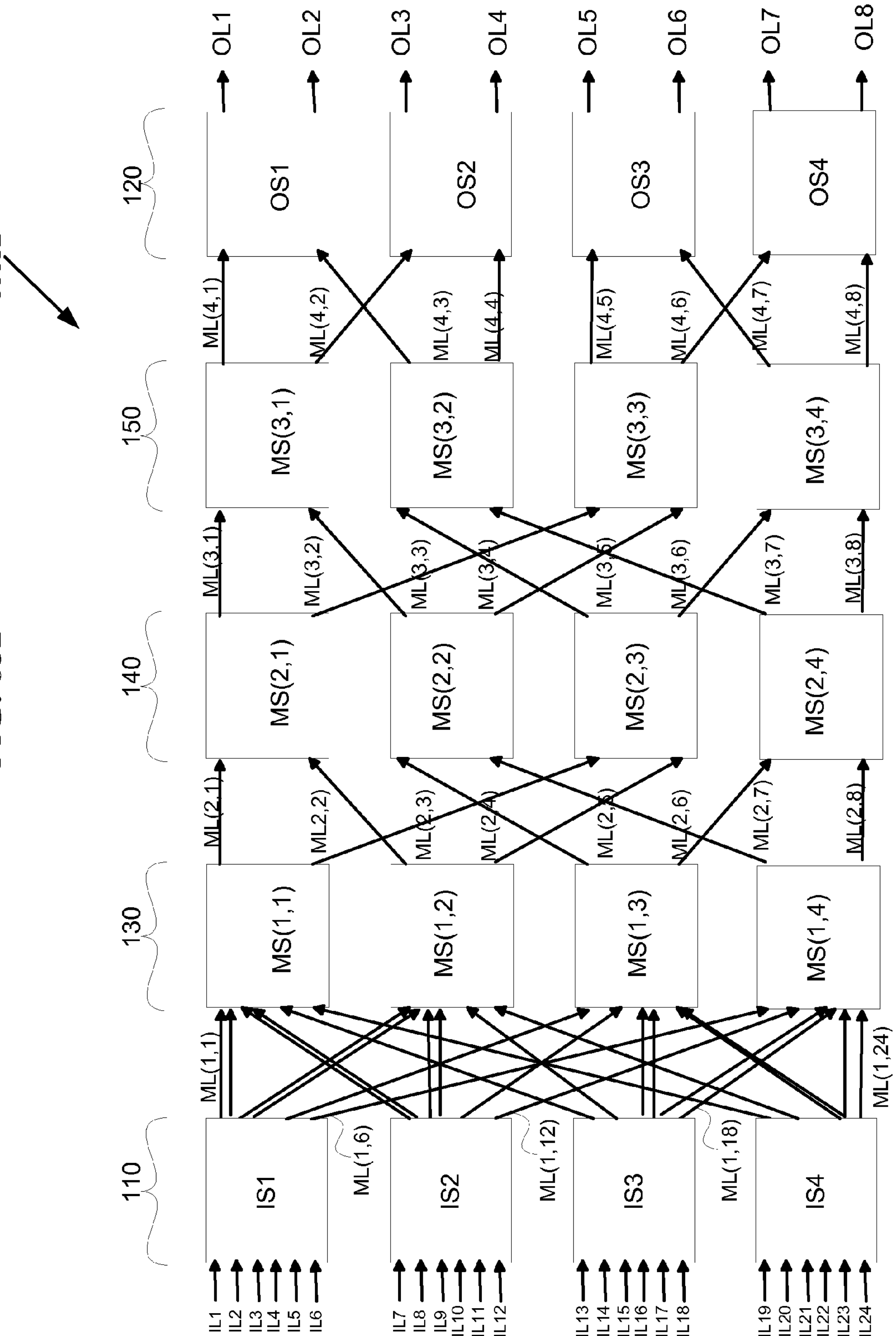
FIG. 6J2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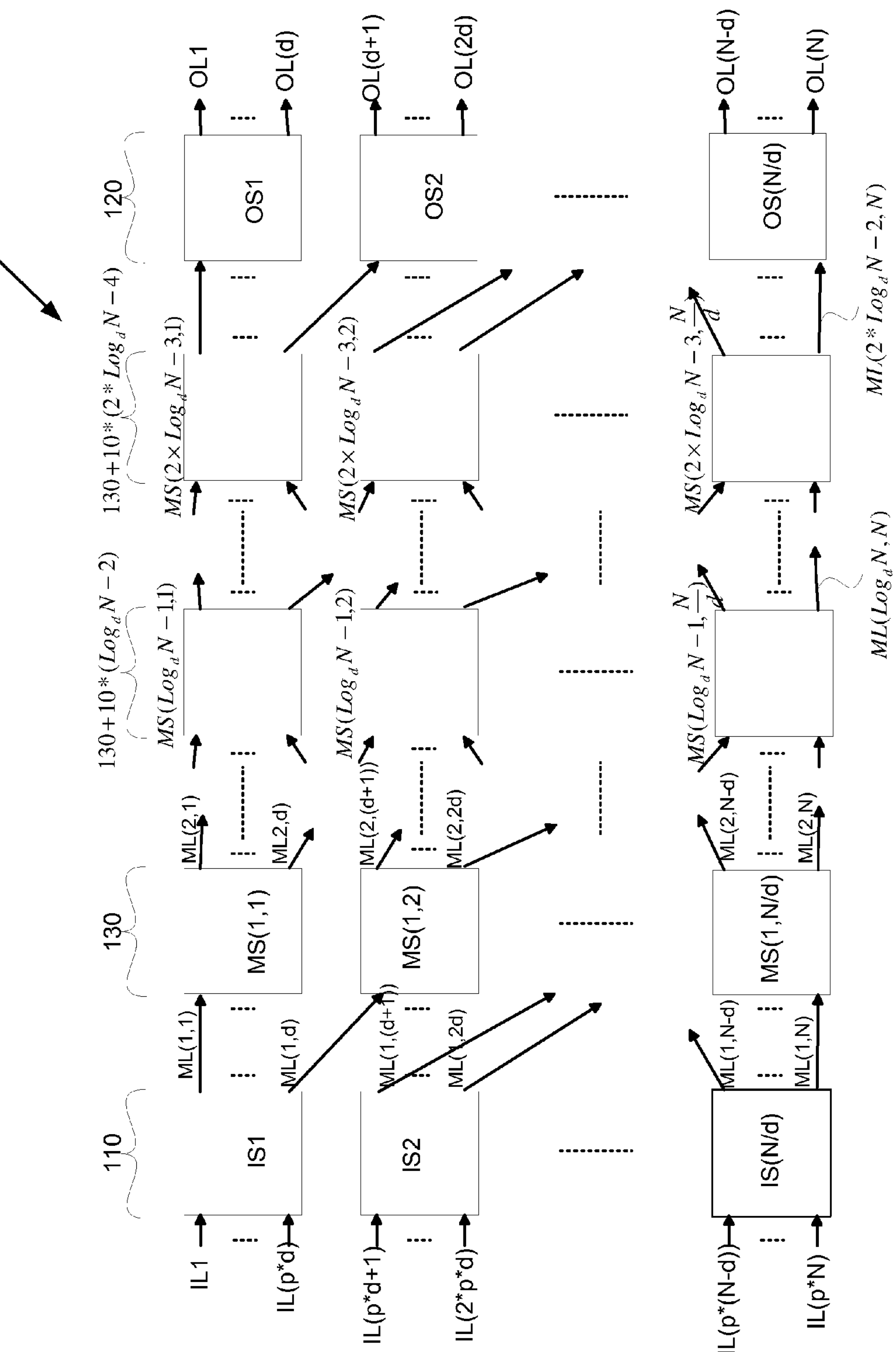
OL1 OL2 OL3 OL4 OL5 OL6 OL7 OL8

FIG. 6K2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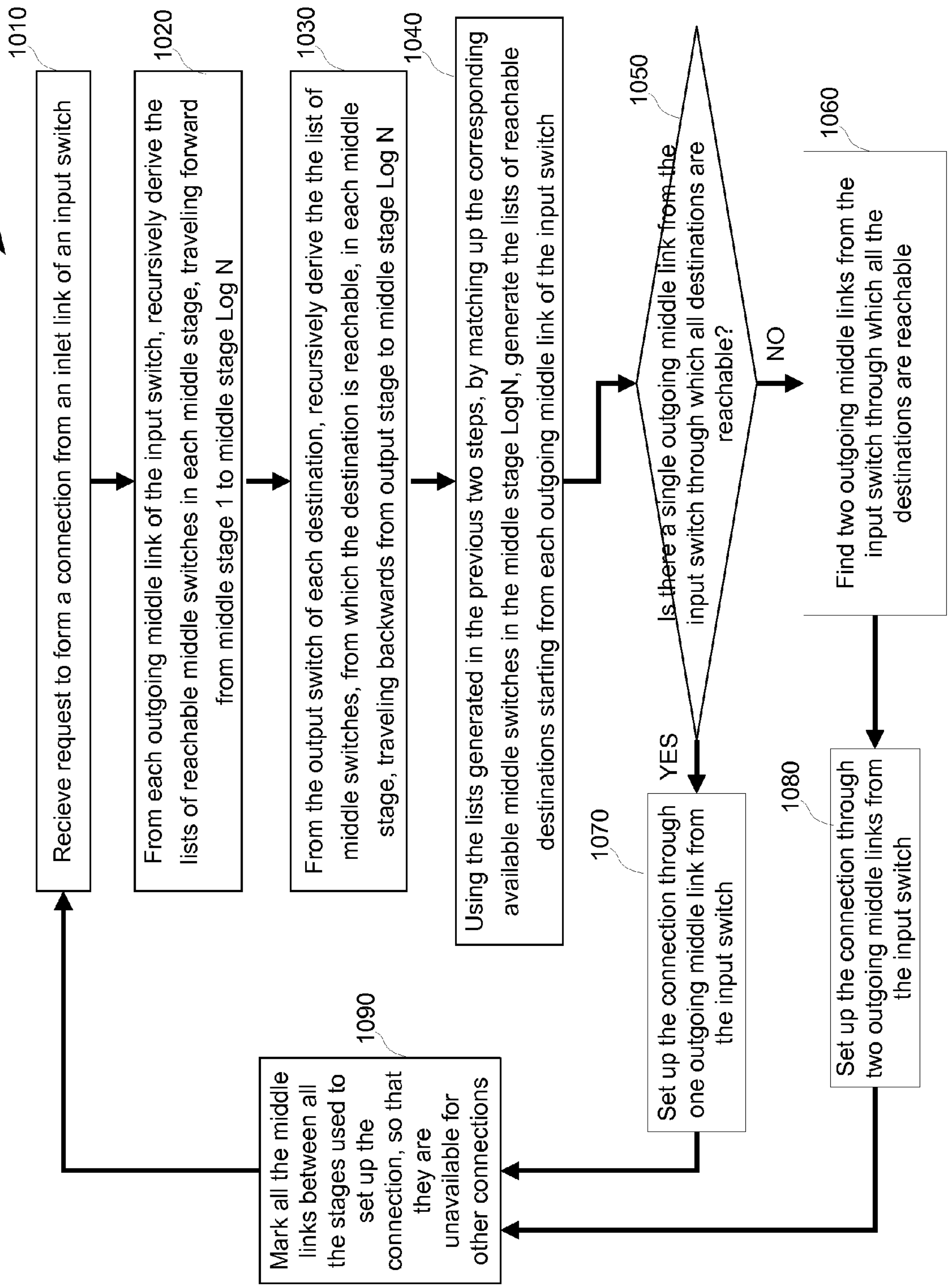
1010
Recieve request to form a connection from an inlet link of an input switch
1020
From each outgoing middle link of the input switch, recursively derive the lists of reachable middle switches in each middle stage, traveling forward from middle stage 1 to middle stage Log N
1030
From the output switch of each destination, recursively derive the the list of middle switches, from which the destination is reachable, in each middle stage, traveling backwards from output stage to middle stage Log N
1040
Using the lists generated in the previous two steps, by matching up the corresponding available middle switches in the middle stage LogN, generate the lists of reachable destinations starting from each outgoing middle link of the input switch
1050
Is there a single outgoing middle link from the input switch through which all destinations are reachable?
NO
YES
1060
Find two outgoing middle links from the input switch through which all the destinations are reachable
1070
Set up the connection through one outgoing middle link from the input switch
1080
Set up the connection through two outgoing middle links from the input switch
1090
Mark all the middle links between all the stages used to set up the connection, so that they are unavailable for other connections

FIG. 7A

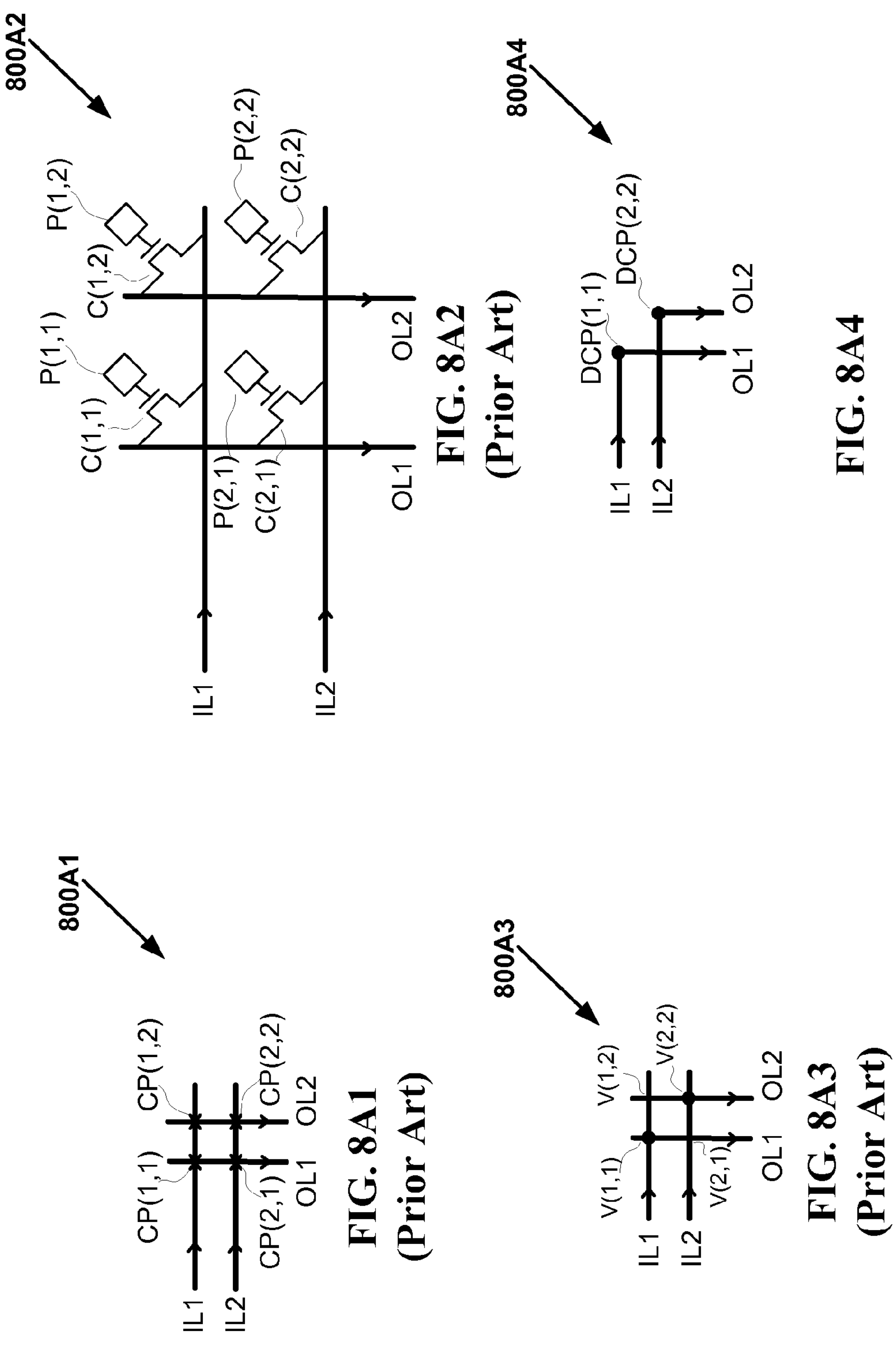

FIG. 8A

FIG. 8A1 (Prior Art)

FIG. 8A2 (Prior Art)

FIG. 8A3 (Prior Art)

FIG. 8A4

FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS

CROSS REFERENCE TO RELATED APPLICATIONS

This application is related to and claims priority of the PCT Application Serial No. PCT/US08/64604 entitled "FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, the U.S. Provisional Patent Application Ser. No. 60/940,389 entitled "FULLY CONNECTED GENERALIZED REARRANGEABLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007, the U.S. Provisional Patent Application Ser. No. 60/940,391 entitled "FULLY CONNECTED GENERALIZED FOLDED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007 and the U.S. Provisional Patent Application Ser. No. 60/940,392 entitled "FULLY CONNECTED GENERALIZED STRICTLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the U.S. application Ser. No. 12/530,207 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed Sep. 6, 2009, the PCT Application Serial No. PCT/US08/56064 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed Mar. 6, 2008, the U.S. Provisional Patent Application Ser. No. 60/905,526 entitled "LARGE SCALE CROSSPOINT REDUCTION WITH NONBLOCKING UNICAST & MULTICAST IN ARBITRARILY LARGE MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed Mar. 6, 2007, and the U.S. Provisional Patent Application Ser. No. 60/940,383 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the U.S. patent application Ser. No. 12/601,273 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application filed concurrently, the PCT Application Serial No. PCT/US08/64603 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, the U.S. Provisional Patent Application Ser. No. 60/940,387 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007, and the U.S. Provisional Patent Application Ser. No. 60/940,390 entitled "FULLY CONNECTED GENERALIZED MULTI-LINK BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the U.S. patent application Ser. No. 12/601,275 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS" by Venkat Konda assigned to the same assignee as the current application filed concurrently, the PCT Application Serial No. PCT/US08/64605 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, and the U.S. Provisional Patent Application Ser. No. 60/940,394 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application Ser. No. 61/252,603 entitled "VLSI LAYOUTS OF FULLY CONNECTED NETWORKS WITH LOCALITY EXPLOITATION" by Venkat Konda assigned to the same assignee as the current application, filed Oct. 16, 2009.

This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application Ser. No. 61/252,609 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED AND PYRAMID NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed Oct. 16, 2009.

BACKGROUND OF INVENTION

Clos switching network, Benes switching network, and Cantor switching network are a network of switches configured as a multi-stage network so that fewer switching points are necessary to implement connections between its inlet links (also called "inputs") and outlet links (also called "outputs") than would be required by a single stage (e.g. crossbar) switch having the same number of inputs and outputs. Clos and Benes networks are very popularly used in digital cross-connects, switch fabrics and parallel computer systems. However Clos and Benes networks may block some of the connection requests.

There are generally three types of nonblocking networks: strictly nonblocking; wide sense nonblocking; and rearrangeably nonblocking (See V. E. Benes, "Mathematical Theory of Connecting Networks and Telephone Traffic" Academic Press, 1965 that is incorporated by reference, as background). In a rearrangeably nonblocking network, a connection path is guaranteed as a result of the networks ability to rearrange prior connections as new incoming calls are received. In strictly nonblocking network, for any connection request from an inlet link to some set of outlet links, it is always possible to provide a connection path through the network to satisfy the request without disturbing other existing connections, and if more than one such path is available, any path can be selected without being concerned about realization of future potential connection requests. In wide-sense nonblocking networks, it is also always possible to provide a connection path through the network to satisfy the request without disturbing other existing connections, but in this case the path used to satisfy the connection request must be carefully selected so as to maintain the nonblocking connecting capability for future potential connection requests.

Butterfly Networks, Banyan Networks, Batcher-Banyan Networks, Baseline Networks, Delta Networks, Omega Networks and Flip networks have been widely studied particularly for self routing packet switching applications. Also Benes Networks with radix of two have been widely studied and it is known that Benes Networks of radix two are shown to be built with back to back baseline networks which are rearrangeably nonblocking for unicast connections.

U.S. Pat. No. 5,451,936 entitled "Non-blocking Broadcast Network" granted to Yang et al. is incorporated by reference herein as background of the invention. This patent describes a number of well known nonblocking multi-stage switching network designs in the background section at column 1, line 22 to column 3, 59. An article by Y. Yang, and G. M., Masson entitled, "Non-blocking Broadcast Switching Networks" IEEE Transactions on Computers, Vol. 40, No. 9, September 1991 that is incorporated by reference as background indicates that if the number of switches in the middle stage, m, of a three-stage network satisfies the relation $m \geqq \min((n-1)(x+r^{1/x}))$ where $1 \leqq x \leqq \min(n-1,r)$, the resulting network is nonblocking for multicast assignments. In the relation, r is the number of switches in the input stage, and n is the number of inlet links in each input switch.

U.S. Pat. No. 6,885,669 entitled "Rearrangeably Nonblocking Multicast Multi-stage Networks" by Konda showed that three-stage Clos network is rearrangeably nonblocking for arbitrary fan-out multicast connections when $m \geqq 2 \times n$. And U.S. Pat. No. 6,868,084 entitled "Strictly Nonblocking Multicast Multi-stage Networks" by Konda showed that three-stage Clos network is strictly nonblocking for arbitrary fan-out multicast connections when $m \geqq 3 \times n-1$.

In general multi-stage networks for stages of more than three and radix of more than two are not well studied. An article by Charles Clos entitled "A Study of Non-Blocking Switching Networks" The Bell Systems Technical Journal, Volume XXXII, January 1953, No. 1, pp. 406-424 showed a way of constructing large multi-stage networks by recursive substitution with a crosspoint complexity of $d^2 \times N \times (\log_d N)^{2.58}$ for strictly nonblocking unicast network. Similarly U.S. Pat. No. 6,885,669 entitled "Rearrangeably Nonblocking Multicast Multi-stage Networks" by Konda showed a way of constructing large multi-stage networks by recursive substitution for rearrangeably nonblocking multicast network. An article by D. G. Cantor entitled "On Non-Blocking Switching Networks" 1: pp. 367-377, 1972 by John Wiley and Sons, Inc., showed a way of constructing large multi-stage networks with a crosspoint complexity of $d^2 \times N \times (\log_d N)^2$ for strictly nonblocking unicast, (by using $\log_d N$ number of Benes Networks for d=2) and without counting the crosspoints in multiplexers and demultiplexers. Jonathan Turner studied the cascaded Benes Networks with radices larger than two, for nonblocking multicast with 10 times the crosspoint complexity of that of nonblocking unicast for a network of size N=256.

The crosspoint complexity of all these networks is prohibitively large to implement the interconnect for multicast connections particularly in field programmable gate array (FPGA) devices, programmable logic devices (PLDs), field programmable interconnect Chips (FPICs), digital crossconnects, switch fabrics and parallel computer systems.

SUMMARY OF INVENTION

A generalized multi-link multi-stage network comprising $(2 \times \log_d N)-1$ stages is operated in strictly nonblocking manner for unicast includes an input stage having N/d switches with each of them having d inlet links and 2×d outgoing links connecting to second stage switches, an output stage having N/d switches with each of them having d outlet links and 2×d incoming links connecting from switches in the penultimate stage. The network also has $(2 \times \log_d N)-3$ middle stages with each middle stage having N/d switches, and each switch in the middle stage has 2×d incoming links connecting from the switches in its immediate preceding stage, and 2×d outgoing links connecting to the switches in its immediate succeeding stage. Also the same generalized multi-link multi-stage network is operated in rearrangeably nonblocking manner for arbitrary fan-out multicast and each multicast connection is set up by use of at most two outgoing links from the input stage switch.

A generalized multi-link multi-stage network comprising $(2 \times \log_d N)-1$ stages is operated in strictly nonblocking manner for multicast includes an input stage having N/d switches with each of them having d inlet links and 3×d outgoing links connecting to second stage switches, an output stage having N/d switches with each of them having d outlet links and 3×d incoming links connecting from switches in the penultimate stage. The network also has $(2 \times \log_d N)-3$ middle stages with each middle stage having N/d switches, and each switch in the middle stage has 3×d incoming links connecting from the switches in its immediate preceding stage, and 3×d outgoing links connecting to the switches in its immediate succeeding stage.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1**A is a diagram **100**A of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having inverse Benes connection topology of five stages with N=8, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**B is a diagram **100**B of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with N=8, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**C is a diagram **100**C of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with N=8, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**D is a diagram **100**D of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with N=8, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**E is a diagram **100**E of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with N=8, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**F is a diagram **100**F of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having Baseline connection topology of five stages with N=8, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**G is a diagram **100**G of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with N=8, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**H is a diagram **100**H of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with N=8, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**I is a diagram **100**I of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five stages with N=8, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**J is a diagram **100**J of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with N=8, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**K is a diagram **100**K of a general symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ with $(2\times\log_d N)-1$ stages with s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1A1** is a diagram **100A1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having inverse Benes connection topology of five stages with N_1=8, N_2=p*N_1=24 where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1B1** is a diagram **100B1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with N_1=8, N_2=p*N_1=24 where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1C1** is a diagram **100C1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with N_1=8, N_2=p*N_1=24 where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1D1** is a diagram **100D1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with N_1=8, N_2=p*N_1=24 where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1E1** is a diagram **100E1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with N_1=8, N_2=p*N_1=24 where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1F1** is a diagram **100F1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having Baseline connection topology of five stages with N_1=8, N_2=p*N_1=24 where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1G1** is a diagram **100G1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with N_1=8, N_2=p*N_1=24 where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1H1** is a diagram **100H1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with N_1=8, N_2=p*N_1=24 where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1I1** is a diagram **100I1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five stages with N_1=8, N_2=p*N_1=24 where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1J1** is a diagram **100J1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with N_1=8, N_2=p*N_1=24 where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1K1** is a diagram **100K1** of a general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2\times\log_d N)-1$ stages with N_1=p*N_2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1A2** is a diagram **100A2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having inverse Benes connection topology of five stages with N_2=8, N_1=p*N_2=24, where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1B2** is a diagram **100B2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with N_2=8, N_1=p*N_2=24, where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1C2** is a diagram **100C2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with N_2=8, N_1=p*N_2=24, where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1D2** is a diagram **100D2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with N_2=8, N_1=p*N_2=24, where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**E**2** is a diagram **100**E**2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**F**2** is a diagram **100**F**2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having Baseline connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**G**2** is a diagram **100**G**2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**H**2** is a diagram **100**H**2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**I**2** is a diagram **100**I**2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**J**2** is a diagram **100**J**2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **1**K**2** is a diagram **100**K**2** of a general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2\times\log_d N)-1$ stages with $N_2=p*N_1$ and s=2, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **2**A is a diagram **200**A of an exemplary symmetrical folded multi-link multi-stage network $V_{fold-link}(N, d, s)$ having inverse Benes connection topology of five stages with N=8, d=2 and s=2 with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **2**B is a diagram **200**B of a general symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N, d, 2)$ with $(2\times\log_d N)-1$ stages strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections in accordance with the invention.

FIG. **2**C is a diagram **200**C of an exemplary asymmetrical folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, 2)$ having inverse Benes connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, and d=2 with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **2**D is a diagram **200**D of a general asymmetrical folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, 2)$ with $N_2=p*N_1$ and with $(2\times\log_d N)-1$ stages strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections in accordance with the invention.

FIG. **2**E is a diagram **200**E of an exemplary asymmetrical folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, 2)$ having inverse Benes connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, and d=2 with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **2**F is a diagram **200**F of a general asymmetrical folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, 2)$ with $N_1=p*N_2$ and with $(2\times\log_d N)-1$ stages strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections in accordance with the invention.

FIG. **3**A is a diagram **300**A of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having inverse Benes connection topology of five stages with N=8, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3**B is a diagram **300**B of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with N=8, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3**C is a diagram **300**C of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with N=8, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3**D is a diagram **300**D of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with N=8, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3**E is a diagram **300**E of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with N=8, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3**F is a diagram **300**F of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having Baseline connection topology of five stages with N=8, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3**G is a diagram **300**G of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with N=8, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3**H is a diagram **300**H of an exemplary symmetrical multi-link multi-stage network $V_{mlink}(N, d, s)$ having an exemplary connection topology of five stages with N=8, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3**I is a diagram **300**I of an exemplary symmetrical multi-link multi-stage network V_{mlink}(N, d, s) (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five stages with N=8, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3**J is a diagram **300**J of an exemplary symmetrical multi-link multi-stage network V_{mlink}(N, d, s) having an exemplary connection topology of five stages with N=8, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3**K is a diagram **300**K of a general symmetrical multi-link multi-stage network V_{mlink}(N, d, s) with $(2\times\log_d N)-1$ stages with s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3A1** is a diagram **300A1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having inverse Benes connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3B1** is a diagram **300B1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections.

FIG. **3C1** is a diagram **300C1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3D1** is a diagram **300D1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3E1** is a diagram **300E1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3F1** is a diagram **300F1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having Baseline connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3G1** is a diagram **300G1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3H1** is a diagram **300H1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3I1** is a diagram **300I1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3J1** is a diagram **300J1** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3K1** is a diagram **300K1** of a general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2\times\log_d N)-1$ stages with $N_1=p*N_2$ and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3A2** is a diagram **300A2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having inverse Benes connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3B2** is a diagram **300B2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3C2** is a diagram **300C2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3D2** is a diagram **300D2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3E2** is a diagram **300E2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3F2** is a diagram **300F2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having Baseline connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. **3G2** is a diagram **300G2** of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3H2 is a diagram 300H2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3I2 is a diagram 300I2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3J2 is a diagram 300J2 of an exemplary asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3K2 is a diagram 300K2 of a general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2\times\log_d N)-1$ stages with $N_2=p*N_1$ and s=3, strictly nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4A is a diagram 400A of an exemplary symmetrical folded multi-stage network $V_{fold}(N, d, s)$ having inverse Benes connection topology of five stages with N=8, d=2 and s=2 with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4A1 is a diagram 400A1 of an exemplary symmetrical folded multi-stage network $V_{fold}(N, d, 2)$ having Omega connection topology of five stages with N=8, d=2 and s=2 with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4A2 is a diagram 400A2 of an exemplary symmetrical folded multi-stage network $V_{fold}(N, d, 2)$ having nearest neighbor connection topology of five stages with N=8, d=2 and s=2 with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4B is a diagram 400B of a general symmetrical folded multi-stage network $V_{fold}(N, d, 2)$ with $(2\times\log_d N)-1$ stages strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections in accordance with the invention.

FIG. 4C is a diagram 400C of an exemplary asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 2)$ having inverse Benes connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, and d=2 with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4C1 is a diagram 400C1 of an exemplary asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 2)$ having Omega connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, and d=2 with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4C2 is a diagram 400C2 of an exemplary asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 2)$ having nearest neighbor connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, and d=2 with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4D is a diagram 400D of a general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 2)$ with $N_2=p*N_1$ and with $(2\times\log_d N)-1$ stages strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections in accordance with the invention.

FIG. 4E is a diagram 400E of an exemplary asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 2)$ having inverse Benes connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, and d=2 with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4E1 is a diagram 400E1 of an exemplary asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 2)$ having Omega connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, and d=2 with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4E2 is a diagram 400E2 of an exemplary asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 2)$ having nearest neighbor connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, and d=2 with exemplary multicast connections, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 4F is a diagram 400F of a general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 2)$ with $N_1=p*N_2$ and with $(2\times\log_d N)-1$ stages strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections in accordance with the invention.

FIG. 5A is a diagram 500A of an exemplary symmetrical folded multi-stage network $V_{fold}(N, d, s)$ having inverse Benes connection topology of five stages with N=8, d=2 and s=1 with exemplary unicast connections rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. 5B is a diagram 500B of a general symmetrical folded multi-stage network $V_{fold}(N, d, 1)$ with $(2\times\log_d N)-1$ stages rearrangeably nonblocking network for unicast connections in accordance with the invention.

FIG. 5C is a diagram 500C of an exemplary asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 1)$ having inverse Benes connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, and d=2 with exemplary unicast connections rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. 5D is a diagram 500D of a general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 1)$ with $N_2=p*N_1$ and with $(2\times\log_d N)-1$ stages rearrangeably nonblocking network for unicast connections in accordance with the invention.

FIG. 5E is a diagram 500E of an exemplary asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 1)$ having inverse

Benes connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, and d=2 with exemplary unicast connections rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. **5**F is a diagram **500**F of a general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, 1)$ with $N_1=p*N_2$ and with $(2\times\log_d N)-1$ stages rearrangeably nonblocking network for unicast connections in accordance with the invention.

FIG. **6**A is a diagram **600**A of an exemplary symmetrical multi-stage network V(N, d, s) having inverse Benes connection topology of five stages with N=8, d=2 and s=1, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. **6**B is a diagram **600**B of an exemplary symmetrical multi-stage network V(N, d, s) (having a connection topology built using back-to-back Omega Networks) of five stages with N=8, d=2 and s=1, rearrangeably nonblocking network for unicast connections.

FIG. **6**C is a diagram **600**C of an exemplary symmetrical multi-stage network V(N, d, s) having an exemplary connection topology of five stages with N=8, d=2 and s=1, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. **6**D is a diagram **600**D of an exemplary symmetrical multi-stage network V(N, d, s) having an exemplary connection topology of five stages with N=8, d=2 and s=1, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. **6**E is a diagram **600**E of an exemplary symmetrical multi-stage network V(N, d, s) (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with N=8, d=2 and s=1, rearrangeably nonblocking network for unicast connections.

FIG. **6**F is a diagram **600**F of an exemplary symmetrical multi-stage network V(N, d, s) having Baseline connection topology of five stages with N=8, d=2 and s=1, rearrangeably nonblocking network for unicast connections.

FIG. **6**G is a diagram **600**G of an exemplary symmetrical multi-stage network V(N, d, s) having an exemplary connection topology of five stages with N=8, d=2 and s=1, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. **6**H is a diagram **600**H of an exemplary symmetrical multi-stage network V(N, d, s) having an exemplary connection topology of five stages with N=8, d=2 and s=1, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. **6**I is a diagram **600**I of an exemplary symmetrical multi-stage network V(N, d, s) (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five stages with N=8, d=2 and s=1, rearrangeably nonblocking network for unicast connections.

FIG. **6**J is a diagram **600**J of an exemplary symmetrical multi-stage network V(N, d, s) having an exemplary connection topology of five stages with N=8, d=2 and s=1, rearrangeably nonblocking network for unicast connections.

FIG. **6**K is a diagram **600**K of a general symmetrical multi-stage network V(N, d, s) with $(2\times\log_d N)-1$ stages with s=1, rearrangeably nonblocking network for unicast connections in accordance with the invention.

FIG. **6A1** is a diagram **600A1** of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having inverse Benes connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. **6**B**1** is a diagram **600**B**1** of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections.

FIG. **6**C**1** is a diagram **600**C**1** of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1=8$, $N2=p*N_1=24$ where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. **6**D**1** is a diagram **600**D**1** of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. **6**E**1** is a diagram **600**E**1** of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections.

FIG. **6**F**1** is a diagram **600**F**1** of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having Baseline connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections.

FIG. **6**G**1** is a diagram **600**G**1** of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. **6**H**1** is a diagram **600**H**1** of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. **6**I**1** is a diagram **600**I**1** of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections.

FIG. **6**J**1** is a diagram **600**J**1** of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_1=8$, $N_2=p*N_1=24$ where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections.

FIG. **6K1** is a diagram **600K1** of a general asymmetrical multi-stage network $V(N_1, N_2, d, s)$ with $(2\times\log_d N)-1$ stages with $N_1=p*N_2$ and s=1, rearrangeably nonblocking network for unicast connections in accordance with the invention.

FIG. **6**A**2** is a diagram **600**A**2** of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having inverse Benes connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. **6**B**2** is a diagram **600**B**2** of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ (having a connection topology built using back-to-back Omega Networks) of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections.

FIG. **6**C**2** is a diagram **600**C**2** of an exemplary asymmetrical multi-stage network $V(N_1, N_2, d, s)$ having an exemplary connection topology of five stages with $N_2=8$, $N_1=p*N_2=24$, where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. **6**D**2** is a diagram **600**D**2** of an exemplary asymmetrical multi-stage network V(N_1, N_2, d, s) having an exemplary connection topology of five stages with N_2=8, N_1=p*N_2=24, where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. **6**E**2** is a diagram **600**E**2** of an exemplary asymmetrical multi-stage network V(N_1, N_2, d, s) (having a connection topology called flip network and also known as inverse shuffle exchange network) of five stages with N_2=8, N_1=p*N_2=24, where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections.

FIG. **6**F**2** is a diagram **600**F**2** of an exemplary asymmetrical multi-stage network V(N_1, N_2, d, s) having Baseline connection topology of five stages with N_2=8, N_1=p*N_2=24, where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections.

FIG. **6**G**2** is a diagram **600**G**2** of an exemplary asymmetrical multi-stage network V(N_1, N_2, d, s) having an exemplary connection topology of five stages with N_2=8, N_1=p*N_2=24, where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. **6**H**2** is a diagram **600**H**2** of an exemplary asymmetrical multi-stage network V(N_1, N_2, d, s) having an exemplary connection topology of five stages with N_2=8, N_1=p*N_2=24, where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections, in accordance with the invention.

FIG. **6**I**2** is a diagram **600**I**2** of an exemplary asymmetrical multi-stage network V(N_1, N_2, d, s) (having a connection topology built using back-to-back Banyan Networks or back-to-back Delta Networks or equivalently back-to-back Butterfly networks) of five stages with N_2=8, N_1=p*N_2=24, where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections.

FIG. **6**J**2** is a diagram **600**J**2** of an exemplary asymmetrical multi-stage network V(N_1, N_2, d, s) having an exemplary connection topology of five stages with N_2=8, N_1=p*N_2=24, where p=3, d=2 and s=1, rearrangeably nonblocking network for unicast connections.

FIG. **6**K**2** is a diagram **600**K**2** of a general asymmetrical multi-stage network V(N_1, N_2, d, s) with $(2\times\log_d N)-1$ stages with N_2=p*N_1 and s=1, rearrangeably nonblocking network for unicast connections in accordance with the invention.

FIG. **7**A is high-level flowchart of a scheduling method according to the invention, used to set up the multicast connections in all the networks disclosed in this invention.

FIG. **8**A**1** is a diagram **800**A**1** of an exemplary prior art implementation of a two by two switch; FIG. **8**A**2** is a diagram **800**A**2** for programmable integrated circuit prior art implementation of the diagram **800**A**1** of FIG. **8**A**1**; FIG. **8**A**3** is a diagram **800**A**3** for one-time programmable integrated circuit prior art implementation of the diagram **800**A**1** of FIG. **8**A**1**; FIG. **8**A**4** is a diagram **800**A**4** for integrated circuit placement and route implementation of the diagram **800**A**1** of FIG. **8**A**1**.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is concerned with the design and operation of large scale crosspoint reduction using arbitrarily large multi-link multi-stage switching networks for broadcast, unicast and multicast connections. Particularly multi-link multi-stage networks with stages more than three and radices greater than or equal to two offer large scale crosspoint reduction when configured with optimal links as disclosed in this invention.

When a transmitting device simultaneously sends information to more than one receiving device, the one-to-many connection required between the transmitting device and the receiving devices is called a multicast connection. A set of multicast connections is referred to as a multicast assignment. When a transmitting device sends information to one receiving device, the one-to-one connection required between the transmitting device and the receiving device is called unicast connection. When a transmitting device simultaneously sends information to all the available receiving devices, the one-to-all connection required between the transmitting device and the receiving devices is called a broadcast connection.

In general, a multicast connection is meant to be one-to-many connection, which includes unicast and broadcast connections. A multicast assignment in a switching network is nonblocking if any of the available inlet links can always be connected to any of the available outlet links.

In certain multi-link multi-stage networks, folded multi-link multi-stage networks, and folded multi-stage networks of the type described herein, any connection request of arbitrary fan-out, i.e. from an inlet link to an outlet link or to a set of outlet links of the network, can be satisfied without blocking if necessary by rearranging some of the previous connection requests. In certain other multi-link multi-stage networks of the type described herein, any connection request of arbitrary fan-out, i.e. from an inlet link to an outlet link or to a set of outlet links of the network, can be satisfied without blocking with never needing to rearrange any of the previous connection requests.

In certain multi-link multi-stage networks, folded multi-link multi-stage networks, and folded multi-stage networks of the type described herein, any connection request of unicast from an inlet link to an outlet link of the network, can be satisfied without blocking if necessary by rearranging some of the previous connection requests. In certain other multi-link multi-stage networks of the type described herein, any connection request of unicast from an inlet link to an outlet link of the network, can be satisfied without blocking with never needing to rearrange any of the previous connection requests.

Nonblocking configurations for other types of networks with numerous connection topologies and scheduling methods are disclosed as follows:

1) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-stage networks V(N_1, N_2, d, s) with numerous connection topologies and the scheduling methods are described in detail in the U.S. application Ser. No. 12/530,207 that is incorporated by reference above.

2) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized butterfly fat tree networks V_{bft}(N_1, N_2, d, s) with numerous connection topologies and the scheduling methods are described in detail in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above.

3) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link butterfly fat tree networks $V_{mlink\text{-}bft}$(N_1, N_2, d, s) with numerous connection topologies and the scheduling methods are described in detail in PCT Application Serial No. PCT/US08/64603 that is incorporated by reference above.

4) VLSI layouts of generalized multi-stage networks V(N_1, N_2, d, s), generalized folded multi-stage networks V_{fold}(N_1, N_2, d, s), generalized butterfly fat tree networks V_{bft}(N_1, N_2, d, s), generalized multi-link multi-stage networks V_{mlink}(N_1, N_2, d, s), generalized folded multi-link multi-stage networks $V_{fold\text{-}mlink}$(N_1, N_2, d, s), generalized multi-link butterfly fat tree networks $V_{mlink\text{-}bft}$(N_1, N_2, d, s), and generalized hyper-

cube networks $V_{hcube}(N_1, N_2, d, s)$ for s=1, 2, 3 or any number in general, are described in detail in the PCT Application Serial No. PCT/US08/64605 that is incorporated by reference above.

5) VLSI layouts of numerous types of multi-stage networks with locality exploitation are described in U.S. Provisional Patent Application Ser. No. 61/252,603 that is incorporated by reference above.

6) VLSI layouts of numerous types of multistage pyramid networks are described in U.S. Provisional Patent Application Ser. No. 61/252,609 that is incorporated by reference above.

RNB Multi-Link Multi-Stage Embodiments:

Symmetric RNB Embodiments:

Referring to FIG. **1**A, in one embodiment, an exemplary symmetrical multi-link multi-stage network **100**A with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by four switches IS**1**-IS**4** and output stage **120** consists of four, four by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, four by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, four by four switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, four by four switches MS(**3**,**1**)-MS (**3**,**4**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable N/d, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by N/d, The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*2d and each output switch OS**1**-OS**4** can be denoted in general with the notation 2d*d. Likewise, the size of each switch in any of the middle stages can be denoted as 2d*2d. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL**1**-IL**8** as there are outlet links OL**1**-OL**8**, in a symmetrical network they are the same.

Each of the N/d input switches IS**1**-IS**4** are connected to exactly 2×d switches in middle stage **130** through 2×d links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**), and also to middle switch MS(**1**,**2**) through the links ML(**1**,**3**) and ML(**1**, **4**)).

Each of the N/d middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through 2×d links (for example the links ML(**1**,**1**) and ML(**1**, **2**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**, and the links ML(**1**,**7**) and ML(**1**,**8**) are connected to the middle switch MS(**1**,**1**) from input switch IS**2**) and also are connected to exactly d switches in middle stage **140** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**, **2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**3**) and ML(**2**,**4**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**, **3**)).

Similarly each of the N/d middle switches MS(**2**,**1**)-MS(**2**, **4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**11**) and ML(**2**,**12**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**3**)) and also are connected to exactly d switches in middle stage **150** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**3**) and ML(**3**,**4**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**3**)).

Similarly each of the N/d middle switches MS(**3**,**1**)-MS(**3**, **4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**11**) and ML(**3**,**12**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**3**)) and also are connected to exactly d output switches in output stage **120** through 2×d links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switch OS**1** from Middle switch MS(**3**,**1**), and the links ML(**4**,**3**) and ML(**4**,**4**) are connected to output switch OS**2** from middle switch MS(**3**,**1**)).

Each of the N/d output switches OS**1**-OS**4** are connected from exactly 2×d switches in middle stage **150** through 2×d links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**) and ML(**4**, **2**), and output switch OS**1** is also connected from middle switch MS(**3**,**2**) through the links ML(**4**,**7**) and ML(**4**,**8**)).

Finally the connection topology of the network **100**A shown in FIG. **1**A is known to be back to back inverse Benes connection topology.

Referring to FIG. **1**B, in another embodiment of network $V_{mlink}(N, d, s)$, an exemplary symmetrical multi-link multi-stage network **100**B with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by four switches IS**1**-IS**4** and output stage **120** consists of four, four by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, four by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, four by four switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, four by four switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable N/d, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by N/d. The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*2d and each output switch OS**1**-OS**4** can be denoted in general with the notation 2d*d. Likewise, the size of each switch in any of the middle stages can be denoted as 2d*2d. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The symmetric multi-link multi-stage network of FIG. **1**B is also the network of the type V_{link}(N, d, s), where N represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL**1**-IL**8** as there are outlet links OL**1**-OL**8**, in a symmetrical network they are the same.

Each of the N/d input switches IS**1**-IS**4** are connected to exactly 2×d switches in middle stage **130** through 2×d links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**), and also to middle switch MS(**1**,**2**) through the links ML(**1**,**3**) and ML(**1**, **4**)).

Each of the N/d middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through 2×d links (for example the links ML(**1**,**1**) and ML(**1**, **2**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**, and the links ML(**1**,**9**) and ML(**1**,**10**) are connected to the middle switch MS(**1**,**1**) from input switch IS**3**) and also are connected to exactly d switches in middle stage **140** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**3**) and ML(**2**,**4**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**2**)).

Similarly each of the N/d middle switches MS(**2**,**1**)-MS(**2**, **4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**9**) and ML(**2**,**10**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**3**)) and also are connected to exactly d switches in middle stage **150** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**3**) and ML(**3**,**4**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**2**)).

Similarly each of the N/d middle switches MS(**3**,**1**)-MS(**3**, **4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**9**) and ML(**3**,**10**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**3**)) and also are connected to exactly d output switches in output stage **120** through 2×d links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switch OS**1** from Middle switch MS(**3**,**1**), and the links ML(**4**,**3**) and ML(**4**,**4**) are connected to output switch OS**2** from middle switch MS(**3**,**1**)).

Each of the N/d output switches OS**1**-OS**4** are connected from exactly 2×d switches in middle stage **150** through 2×d links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**) and ML(**4**, **2**), and output switch OS**1** is also connected from middle switch MS(**3**,**3**) through the links ML(**4**,**9**) and ML(**4**,**10**)).

Finally the connection topology of the network **100**B shown in FIG. **1**B is known to be back to back Omega connection topology.

Referring to FIG. **1**C, in another embodiment of network V_{mlink}(N, d, s), an exemplary symmetrical multi-link multi-stage network **100**C with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by four switches IS**1**-IS**4** and output stage **120** consists of four, four by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, four by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, four by four switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, four by four switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable N/d, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by N/d. The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*2d and each output switch OS**1**-OS**4** can be denoted in general with the notation 2d*d. Likewise, the size of each switch in any of the middle stages can be denoted as 2d*2d. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The symmetric multi-link multi-stage network of FIG. **1**C is also the network of the type V_{mlink}(N, d, s), where N represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL**1**-IL**8** as there are outlet links OL**1**-OL**8**, in a symmetrical network they are the same.

Each of the N/d input switches IS**1**-IS**4** are connected to exactly 2×d switches in middle stage **130** through 2×d links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**), and also to middle switch MS(**1**,**2**) through the links ML(**1**,**3**) and ML(**1**, **4**)).

Each of the N/d middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through 2×d links (for example the links ML(**1**,**1**) and ML(**1**,**2**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**, and the links ML(**1**,**15**) and ML(**1**,**16**) are connected to the middle switch MS(**1**,**1**) from input switch IS**4**) and also are connected to exactly d switches in middle stage **140** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**3**) and ML(**2**,**4**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**2**)).

Similarly each of the N/d middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**15**) and ML(**2**,**16**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**4**)) and also are connected to exactly d switches in middle stage **150** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**3**) and ML(**3**,**4**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**2**)).

Similarly each of the N/d middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**15**) and ML(**3**,**16**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**4**)) and also are connected to exactly d output switches in output stage **120** through 2×d links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switch OS**1** from middle switch MS(**3**,**1**), and the links ML(**4**,**3**) and ML(**4**,**4**) are connected to output switch OS**2** from middle switch MS(**3**,**1**)).

Each of the N/d output switches OS**1**-OS**4** are connected from exactly 2×d switches in middle stage **150** through 2×d links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**) and ML(**4**,**2**), and output switch OS**1** is also connected from middle switch MS(**3**,**4**) through the links ML(**4**,**15**) and ML(**4**,**16**)).

Finally the connection topology of the network **100**C shown in FIG. **1**C is hereinafter called nearest neighbor connection topology.

Similar to network **100**A of FIG. **1**A, **100**B of FIG. **1**B, and **100**C of FIG. **1**C, referring to FIG. **1**D, FIG. **1**E, FIG. **1**F, FIG. **1**G, FIG. **1**H, FIG. **1**I and FIG. **1**J with exemplary symmetrical multi-link multi-stage networks **100**D, **100**E, **100**F, **100**G, **100**H, **100**I, and **100**J respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by four switches IS**1**-IS**4** and output stage **120** consists of four, four by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, four by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, four by four switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, four by four switches MS(**3**,**1**)-MS(**3**,**4**).

Such networks can also be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

The networks **100**D, **100**E, **100**F, **100**G, **100**H, **100**I and **100**J of FIG. **1**D, FIG. **1**E, FIG. **1**F, FIG. **1**G, FIG. **1**H, FIG. **1**I, and FIG. **1**J are also embodiments of symmetric multi-link multi-stage network can be represented with the notation V_{link} (N, d, s), where N represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL**1**-IL**8** as there are outlet links OL**1**-OL**8**, in a symmetrical network they are the same.

Just like networks of **100**A, **100**B and **100**C, for all the networks **100**D, **100**E, **100**F, **100**G, **100**H, **100**I and **100**J of FIG. **1**D, FIG. **1**E, FIG. **1**F, FIG. **1**G, FIG. **1**H, FIG. **1**I, and FIG. **1**J, each of the N/d input switches IS**1**-IS**4** are connected to exactly 2×d switches in middle stage **130** through 2×d links.

Each of the N/d middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through 2×d links and also are connected to exactly d switches in middle stage **140** through 2×d links.

Similarly each of the N/d middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 2×d links and also are connected to exactly d switches in middle stage **150** through 2×d links.

Similarly each of the N/d middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 2×d links and also are connected to exactly d output switches in output stage **120** through 2×d links.

Each of the N/d output switches OS**1**-OS**4** are connected from exactly 2×d switches in middle stage **150** through 2×d links.

In all the ten embodiments of FIG. **1**A to FIG. **1**J the connection topology is different. That is the way the links ML(**1**,**1**)-ML(**1**,**16**), ML(**2**,**1**)-ML(**2**,**16**), ML(**3**,**1**)-ML(**3**,**16**), and ML(**4**,**1**)-ML(**4**,**16**) are connected between the respective stages is different. Even though only ten embodiments are illustrated, in general, the network V_{mlink}(N, d, s) can comprise any arbitrary type of connection topology. For example the connection topology of the network V_{mlink}(N, d, s) may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the V_{mlink}(N, d, s) network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network V_{mlink}(N, d, s) can be built. The ten embodiments of FIG. **1**A to FIG. **1**J are only three examples of network V_{mlink} (N, d, s).

In all the ten embodiments of FIG. **1**A to FIG. **1**J, each of the links ML(**1**,**1**)-ML(**1**,**16**), ML(**2**,**1**)-ML(**2**,**16**), ML(**3**,**1**)-ML(**3**,**16**) and ML(**4**,**1**)-ML(**4**,**16**) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS**1**-IS**4** are also referred to as the network input ports. The input stage **110** is often referred to as the first stage. The output switches OS**1**-OS**4** are also referred to as the network output ports. The output stage **120** is often referred to as the last stage. The middle stage switches MS(**1**,**1**)-MS(**1**,**4**), MS(**2**,**1**)-MS(**2**,**4**), and MS(**3**,**1**)-MS(**3**,**4**) are referred to as middle switches or middle ports.

In the example illustrated in FIG. **1**A (or in FIG. **1**B to FIG. **1**J), a fan-out of four is possible to satisfy a multicast connection request if input switch is IS**2**, but only two switches in middle stage **130** will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS**1**, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage **130** when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network **100**A (or **100**B to **100**J), to be operated in rearrangeably nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage **130** is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage **130**, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the rearrangeably nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Symmetric RNB Embodiments:

Network **100**K of FIG. **1**K is an example of general symmetrical multi-link multi-stage network V_{mlink}(N, d, s) with (2×$\log_d$ N)−1 stages. The general symmetrical multi-link multi-stage network V_{mlink}(N, d, s) can be operated in rearrangeably nonblocking manner for multicast when s≧2 according to the current invention. Also the general symmetrical multi-link multi-stage network V_{mlink}(N, d, s) can be operated in strictly nonblocking manner for unicast if s≧2 according to the current invention. (And in the example of FIG. **1**K, s=2). The general symmetrical multi-link multi-stage network V_{mlink}(N, d, s) with (2×$\log_d$ N)−1 stages has d inlet links for each of N/d input switches IS**1**-IS(N/d) (for example the links IL**1**-IL(d) to the input switch IS**1**) and 2×d outgoing links for each of N/d input switches IS**1**-IS(N/d) (for example the links ML(**1**,**1**)-ML(**1**,2d) to the input switch IS**1**). There are d outlet links for each of N/d output switches OS**1**-OS(N/d) (for example the links OL**1**-OL(d) to the output switch OS**1**) and 2×d incoming links for each of N/d output switches OS**1**-OS(N/d) (for example ML(2×Log_d N−2,**1**)-ML(2×Log_d N−2,2×d) to the output switch OS**1**).

Each of the N/d input switches IS**1**-IS(N/d) are connected to exactly d switches in middle stage **130** through 2×d links.

Each of the N/d middle switches MS(**1**,**1**)-MS(**1**,N/d) in the middle stage **130** are connected from exactly d input switches through 2×d links and also are connected to exactly d switches in middle stage **140** through 2×d links.

Similarly each of the N/d middle switches

$$MS(\text{Log}_d N-1,\ 1)-MS\left(\text{Log}_d N-1,\ \frac{N}{d}\right)$$

in the middle stage **130**+10*(Log_d N−2) are connected from exactly d switches in middle stage **130**+10*(Log_d N−3) through 2×d links and also are connected to exactly d switches in middle stage **130**+10*(Log_d N−1) through 2×d links.

Similarly each of the N/d middle switches

$$MS(2\times\text{Log}_d N-3,\ 1)-MS\left(2\times\text{Log}_d N-3,\ \frac{N}{d}\right)$$

in the middle stage **130**+10*(2*Log_d N−4) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N−5) through 2×d links and also are connected to exactly d output switches in output stage **120** through 2×d links.

Each of the N/d output switches OS**1**-OS(N/d) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N−4) through 2×d links.

As described before, again the connection topology of a general V_{mlink}(N, d, s) may be any one of the connection topologies. For example the connection topology of the network V_{mlink}(N, d, s) may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general V_{mlink}(N, d, s) network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network V_{mlink}(N, d, s) can be built. The embodiments of FIG. **1**A to FIG. **1**J are ten examples of network V_{mlink}(N, d, s).

The general symmetrical multi-link multi-stage network V_{mlink}(N, d, s) can be operated in rearrangeably nonblocking manner for multicast when s≧2 according to the current invention. Also the general symmetrical multi-link multi-stage network V_{mlink}(N, d, s) can be operated in strictly nonblocking manner for unicast if S≧2 according to the current invention.

Every switch in the multi-link multi-stage networks discussed herein has multicast capability. In a V_{mlink}(N, d, s) network, if a network inlet link is to be connected to more than one outlet link on the same output switch, then it is only necessary for the corresponding input switch to have one path to that output switch. This follows because that path can be multicast within the output switch to as many outlet links as necessary. Multicast assignments can therefore be described in terms of connections between input switches and output switches. An existing connection or a new connection from an input switch to r' output switches is said to have fan-out r'. If all multicast assignments of a first type, wherein any inlet link of an input switch is to be connected in an output switch to at most one outlet link are realizable, then multicast assignments of a second type, wherein any inlet link of each input switch is to be connected to more than one outlet link in the same output switch, can also be realized. For this reason, the following discussion is limited to general multicast connections of the first type

$$\left(\text{with fan-out } r',\ 1\le r'\le\frac{N}{d}\right)$$

although the same discussion is applicable to the second type.

To characterize a multicast assignment, for each inlet link

$$i \in \left\{1, 2, \ldots, \frac{N}{d}\right\},$$

let I_i=O, where

$$O \subset \left\{1, 2, \ldots, \frac{N}{d}\right\},$$

denote the subset of output switches to which inlet link i is to be connected in the multicast assignment. For example, the network of FIG. **1**C shows an exemplary five-stage network, namely V_{mlink}(**8**,**2**,**2**), with the following multicast assignment I_1={2,4} and all other I_j=ϕ for j=[2-8]. It should be noted that the connection I_1 fans out in the first stage switch IS**1** into middle switches MS(**1**,**1**) and MS(**1**,**2**) in middle stage **130**, and fans out in middle switches MS(**1**,**1**) and MS(**1**,**2**) only once into middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively in middle stage **140**.

The connection I_1 also fans out in middle switches MS(**2**,**1**) and MS(**2**,**3**) only once into middle switches MS(**3**,**2**) and MS(**3**,**4**) respectively in middle stage **150**. The connection I_1 also fans out in middle switches MS(**3**,**2**) and MS(**3**,**4**) only once into output switches OS**2** and OS**4** in output stage **120**. Finally the connection I_1 fans out once in the output stage switch OS**2** into outlet link OL**3** and in the output stage switch OS**4** twice into the outlet links OL**7** and OL**8**. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage **130**.

Asymmetric RNB (N_2>N_1) Embodiments:

Referring to FIG. **1A1**, in one embodiment, an exemplary asymmetrical multi-link multi-stage network **100A1** with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by four switches IS**1**-IS**4** and output stage **120** consists of four, eight by six switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, four by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, four by four switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, four by eight switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size eight by six, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_1}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and N_2>N_1 and N_2=p*N, where p>1. The number of middle switches in each middle stage is denoted by

$$\frac{N_1}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*2d and each output switch OS**1**-OS**4** can be denoted in general with the notation (d+d_2)*d_2, where

$$d_2 = N_2 \times \frac{d}{N_1} = p \times d.$$

The size of each switch in any of the middle stages excepting the last middle stage can be denoted as 2d*2d. The size of each switch in the last middle stage can be denoted as 2d*(d+d_2). A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation V_{mlink}(N_1, N_2, d, s), where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**24**), d represents the inlet links of each input switch where N_2>N_1, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the

$$\frac{N_1}{d}$$

input switches IS**1**-IS**4** are connected to exactly d switches in middle stage **130** through 2×d links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**), and also to middle switch MS(**1**,**2**) through the links ML(**1**,**3**) and ML(**1**,**4**)).

Each of the

$$\frac{N_1}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through 2×d links (for example the links ML(**1**,**1**) and ML(**1**,**2**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**, and the links ML(**1**,**7**) and ML(**1**,**8**) are connected to the middle switch MS(**1**,**1**) from input switch IS**2**) and also are connected to exactly d switches in middle stage **140** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**3**) and ML(**2**,**4**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**3**)).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**11**) and ML(**2**,**12**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**3**)) and also are connected to exactly d switches in middle stage **150** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**3**) and ML(**3**,**4**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**3**)).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**11**) and ML(**3**,**12**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**3**)) and also are connected to exactly

$$\frac{d+d_2}{2}$$

output switches in output stage **120** through $d+d_2$ links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switch OS**1** from Middle switch MS(**3**,**1**); the links ML(**4**,**3**) and ML(**4**,**4**) are connected to output switch OS**2** from middle switch MS(**3**,**1**); the links ML(**4**,**5**) and ML(**4**,**6**) are connected to output switch OS**3** from Middle switch MS(**3**,**1**); and the links ML(**4**,**7**) and ML(**4**,**8**) are connected to output switch OS**4** from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS**4** are connected from exactly

$$\frac{d+d_2}{2}$$

switches in middle stage **150** through $d+d_2$ links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**) and ML(**4**,**2**); output switch OS**1** is also connected from middle switch MS(**3**,**2**) through the links ML(**4**,**9**) and ML(**4**,**10**); output switch OS**1** is connected from middle switch MS(**3**,**3**) through the links ML(**4**,**17**) and ML(**4**,**18**); and output switch OS**1** is also connected from middle switch MS(**3**,**4**) through the links ML(**4**,**25**) and ML(**4**,**26**)).

Finally the connection topology of the network **100A1** shown in FIG. **1A1** is known to be back to back inverse Benes connection topology.

Referring to FIG. **1B1**, in one embodiment, an exemplary asymmetrical multi-link multi-stage network **100B1** with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by four switches IS**1**-IS**4** and output stage **120** consists of four, eight by six switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, four by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, four by four switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, four by eight switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size eight by six, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_1}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_2>N_1$ and $N_2=p*N$, where p>1. The number of middle switches in each middle stage is denoted by

$$\frac{N_1}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*2d and each output switch OS**1**-OS**4** can be denoted in general with the notation $(d+d_2)*d_2$, where

$$d_2 = N_2 \times \frac{d}{N_1} = p \times d.$$

The size of each switch in any of the middle stages excepting the last middle stage can be denoted as 2d*2d. The size of each switch in the last middle stage can be denoted as $2d*(d+d_2)$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**24**), d represents the inlet links of each input switch where $N_2>N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the

$$\frac{N_1}{d}$$

input switches IS1-IS4 are connected to exactly 2×d switches in middle stage **130** through 2×d links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**), and also to middle switch MS(**1**,**2**) through the links ML(**1**,**3**) and ML(**1**,**4**)).

Each of the

$$\frac{N_1}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through 2×d links (for example the links ML(**1**,**1**) and ML(**1**,**2**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**, and the links ML(**1**,**9**) and ML(**1**,**10**) are connected to the middle switch MS(**1**,**1**) from input switch IS**3**) and also are connected to exactly d switches in middle stage **140** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**3**) and ML(**2**,**4**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**2**)).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**9**) and ML(**2**,**10**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**3**)) and also are connected to exactly d switches in middle stage **150** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**3**) and ML(**3**,**4**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**2**)).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**9**) and ML(**3**,**10**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**3**)) and also are connected to exactly

$$\frac{d+d_2}{2}$$

output switches in output stage **120** through $d+d_2$ links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switch OS**1** from middle switch MS(**3**,**1**); the links ML(**4**,**3**) and ML(**4**,**4**) are connected to output switch OS**2** from middle switch MS(**3**,**1**); the links ML(**4**,**5**) and ML(**4**,**6**) are connected to output switch OS**3** from Middle switch MS(**3**,**1**); and the links ML(**4**,**7**) and ML(**4**,**8**) are connected to output switch OS**4** from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS**4** are connected from exactly

$$\frac{d+d_2}{2}$$

switches in middle stage **150** through $d+d_2$ links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**) and ML(**4**,**2**); output switch OS**1** is also connected from middle switch MS(**3**,**2**) through the links ML(**4**,**9**) and ML(**4**,**10**); output switch OS**1** is connected from middle switch MS(**3**,**3**) through the links ML(**4**,**17**) and ML(**4**,**18**); and output switch OS**1** is also connected from middle switch MS(**3**,**4**) through the links ML(**4**,**25**) and ML(**4**,**26**)).

Finally the connection topology of the network **100**B**1** shown in FIG. **1**B**1** is known to be back to back Omega connection topology.

Referring to FIG. **1**C**1**, in one embodiment, an exemplary asymmetrical multi-link multi-stage network **100**C**1** with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by four switches IS**1**-IS**4** and output stage **120** consists of four, eight by six switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, four by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, four by four switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, four by eight switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size eight by six, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_1}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_2>N_1$ and $N_2=p*N$, where p>1. The number of middle switches in each middle stage is denoted by

$$\frac{N_1}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*2d and each output switch OS**1**-OS**4** can be denoted in general with the notation $(d+d_2)*d_2$, where

$$d_2 = N_2 \times \frac{d}{N_1} = p \times d.$$

The size of each switch in any of the middle stages excepting the last middle stage can be denoted as 2d*2d. The size of each switch in the last middle stage can be denoted as $2d*(d+d_2)$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N, represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), N represents the total number of outlet links of all output switches (for example the links OL**1**-OL**24**), d represents the inlet links of each input switch where $N_2>N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the

$$\frac{N_1}{d}$$

input switches IS**1**-IS**4** are connected to exactly 2×d switches in middle stage **130** through 2×d links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**), and also to middle switch MS(**1**,**2**) through the links ML(**1**,**3**) and ML(**1**,**4**)).

Each of the

$$\frac{N_1}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through 2×d links (for example the links ML(**1**,**1**) and ML(**1**,**2**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**, and the links ML(**1**,**15**) and ML(**1**,**16**) are connected to the middle switch MS(**1**,**1**) from input switch IS**4**) and also are connected to exactly d switches in middle stage **140** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**3**) and ML(**2**,**4**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**2**)).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**15**) and ML(**2**,**16**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**4**)) and also are connected to exactly d switches in middle stage **150** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**3**) and ML(**3**,**4**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**2**)).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**15**) and ML(**3**,**16**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**4**)) and also are connected to exactly

$$\frac{d+d_2}{2}$$

output switches in output stage **120** through $d+d_2$ links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switch OS**1** from middle switch MS(**3**,**1**); the links ML(**4**,**3**) and ML(**4**,**4**) are connected to output switch OS**2** from middle switch MS(**3**,**1**); the links ML(**4**,**5**) and ML(**4**,**6**) are connected to output switch OS**3** from Middle switch MS(**3**,**1**); and the links ML(**4**,**7**) and ML(**4**,**8**) are connected to output switch OS**4** from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS**4** are connected from exactly

$$\frac{d+d_2}{2}$$

switches in middle stage **150** through $d+d_2$ links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**) and ML(**4**,**2**); output switch OS**1** is also connected from middle switch MS(**3**,**2**) through the links ML(**4**,**9**) and ML(**4**,**10**); output switch OS**1** is connected from middle switch MS(**3**,**3**) through the links ML(**4**,**17**) and

ML(**4**,**18**); and output switch OS**1** is also connected from middle switch MS(**3**,**4**) through the links ML(**4**,**25**) and ML(**4**,**26**)).

Finally the connection topology of the network **100**C**1** shown in FIG. **1**C**1** is hereinafter called nearest neighbor connection topology.

Similar to network **100**A**1** of FIG. **1**A**1**, **100**B**1** of FIG. **1**B**1**, and **100**C**1** of FIG. **1**C**1**, referring to FIG. **1**D**1**, FIG. **1**E**1**, FIG. **1**F**1**, FIG. **1**G**1**, FIG. **1**H**1**, FIG. **1**I**1** and FIG. **1**J**1** with exemplary asymmetrical multi-link multi-stage networks **100**D**1**, **100**E**1**, **100**F**1**, **100**G**1**, **100**H**1**, **100**I**1**, and **100**J**1** respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by four switches IS**1**-IS**4** and output stage **120** consists of four, four by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, four by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, four by four switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, four by four switches MS(**3**,**1**)-MS(**3**,**4**).

Such networks can also be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

The networks **100**D**1**, **100**E**1**, **100**F**1**, **100**G**1**, **100**H**1**, **100**I**1** and **100**J**1** of FIG. **1**D**1**, FIG. **1**E**1**, FIG. **1**F**1**, FIG. **1**G**1**, FIG. **1**H**1**, FIG. **1**I**1**, and FIG. **1**J**1** are also embodiments of asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**24**), d represents the inlet links of each input switch where $N_2>N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Just like networks of **100**A**1**, **100**B**1** and **100**C**1**, for all the networks **100**D**1**, **100**E**1**, **100**F**1**, **100**G**1**, **100**H**1**, **100**I**1** and **100**J**1** of FIG. **1**D**1**, FIG. **1**E**1**, FIG. **1**F**1**, FIG. **1**G**1**, FIG. **1**H**1**, FIG. **1**I**1**, and FIG. **1**J**1**, each of the

$$\frac{N_1}{d}$$

input switches IS**1**-IS**4** are connected to exactly d switches in middle stage **130** through 2×d links.

Each of the

$$\frac{N_1}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through 2×d links and also are connected to exactly d switches in middle stage **140** through 2×d links.

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 2×d links and also are connected to exactly d switches in middle stage **150** through 2×d links.

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 2×d links and also are connected to exactly

$$\frac{d+d_2}{2}$$

output switches in output stage **120** through $d+d_2$ links.

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS**4** are connected from exactly

$$\frac{d+d_2}{2}$$

switches in middle stage **150** through $d+d_2$ links.

In all the ten embodiments of FIG. **1**A**1** to FIG. **1**J**1** the connection topology is different. That is the way the links ML(**1**,**1**)-ML(**1**,**16**), ML(**2**,**1**)-ML(**2**,**16**), ML(**3**,**1**)-ML(**3**,**16**), and ML(**4**,**1**)-ML(**4**,**16**) are connected between the respective stages is different. Even though only ten embodiments are illustrated, in general, the network $V_{mlink}(N_1, N_2, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{mlink}(N_1, N_2, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{mlink}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{mlink}(N_1, N_2, d, s)$ can be built. The ten embodiments of FIG. **1**A**1** to FIG. **1**J**1** are only three examples of network $V_{mlink}(N_1, N_2, d, s)$.

In all the ten embodiments of FIG. **1**A**1** to FIG. **1**J**1**, each of the links ML(**1**,**1**)-ML(**1**,**16**), ML(**2**,**1**)-ML(**2**,**16**), ML(**3**,**1**)-ML(**3**,**16**) and ML(**4**,**1**)-ML(**4**,**16**) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS**1**-IS**4** are also referred to as the network input ports. The input stage **110** is often referred to as the first stage. The output switches OS**1**-OS**4** are also referred to as the network output ports. The output stage **120** is often referred to as the last stage. The middle stage switches MS(**1**,**1**)-MS(**1**,**4**), MS(**2**,**1**)-MS(**2**,**4**), and MS(**3**,**1**)-MS(**3**,**4**) are referred to as middle switches or middle ports.

In the example illustrated in FIG. **1A1** (or in FIG. **1B1** to FIG. **1J1**), a fan-out of four is possible to satisfy a multicast connection request if input switch is IS**2**, but only two switches in middle stage **130** will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS**1**, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage **130** when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network **100A1** (or **100B1** to **100J1**), to be operated in rearrangeably nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage **130** is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage **130**, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the rearrangeably nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Asymmetric RNB ($N_2>N_1$) Embodiments:

Network **100K1** of FIG. **1K1** is an example of general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2\times\log_d N_1)-1$ stages where $N_2>N_1$ and $N_2=p*N$, where p>1. In network **100K1** of FIG. **1K1**, $N_1=N$ and $N_2=p*N$. The general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s\geqq 2$ according to the current invention. Also the general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if $S\geqq 2$ according to the current invention. (And in the example of FIG. **1K1**, s=2). The general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2\times\log_d N_1)-1$ stages has d inlet links for each of

$$\frac{N_1}{d}$$

input switches IS**1**-IS(N_1/d) (for example the links IL**1**-IL(d) to the input switch IS**1**) and 2×d outgoing links for each of

$$\frac{N_1}{d}$$

input switches IS**1**-IS(N_1/d) (for example the links ML(**1**,**1**)-ML(**1**,2d) to the input switch IS**1**). There are d_2

$$\left(\text{where } d_2 = N_2\times\frac{d}{N_1} = p\times d\right)$$

outlet links for each of

$$\frac{N_1}{d}$$

output switches OS**1**-OS(N_1/d) (for example the links OL**1**-OL(p*d) to the output switch OS**1**) and $d+d_2$ (=d+p×d) incoming links for each of

$$\frac{N_1}{d}$$

output switches OS**1**-OS(N_1/d) (for example ML($2\times\text{Log}_d N_1-2$,1)-ML($2\times\text{Log}_d N_1-2$, $d+d_2$) to the output switch OS**1**).

Each of the

$$\frac{N_1}{d}$$

input switches IS**1**-IS(N_1/d) are connected to exactly 2×d switches in middle stage **130** through 2×d links.

Each of the

$$\frac{N_1}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,N_1/d) in the middle stage **130** are connected from exactly d input switches through 2×d links and also are connected to exactly d switches in middle stage **140** through 2×d links.

Similarly each of the

$$\frac{N_1}{d}$$

middle switches

$$MS(\text{Log}_d N_1-1,\ 1)-MS\left(\text{Log}_d N_1-1,\ \frac{N_1}{d}\right)$$

in the middle stage **130**+10*($\text{Log}_d N_1-2$) are connected from exactly d switches in middle stage **130**+10*($\text{Log}_d N_1-3$) through 2×d links and also are connected to exactly d switches in middle stage **130**+10*($\text{Log}_d N_1-1$) through 2×d links.

Similarly each of the

$$\frac{N_1}{d}$$

middle switches

$$MS(2\times\text{Log}_d N_1-3,\ 1)-MS\left(2\times\text{Log}_d N_1-3,\ \frac{N_1}{d}\right)$$

in the middle stage **130**+10*(2*Log$_d$ N$_1$−4) are connected from exactly d switches in middle stage **130**+10*(2*Log$_d$ N$_1$−5) through 2×d links and also are connected to exactly

$$\frac{d+d_2}{2}$$

output switches in output stage **120** through d+d$_2$ links.

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS(N$_1$/d) are connected from exactly

$$\frac{d+d_2}{2}$$

switches in middle stage **130**+10*(2*Log$_d$ N$_1$−4) through d+d$_2$ links

As described before, again the connection topology of a general V$_{mlink}$(N$_1$, N$_2$, d, s) may be any one of the connection topologies. For example the connection topology of the network V$_{mlink}$(N$_1$, N$_2$, d, s) may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general V$_{mlink}$(N$_1$, N$_2$, d, s) network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network V$_{mlink}$(N$_1$, N$_2$, d, s) can be built. The embodiments of FIG. **1A1** to FIG. **1J1** are ten examples of network V$_{mlink}$(N$_1$, N$_2$, d, s) for s=2 and N$_2$>N$_1$.

The general symmetrical multi-link multi-stage network V$_{mlink}$(N$_1$, N$_2$, d, s) can be operated in rearrangeably non-blocking manner for multicast when s=2 according to the current invention. Also the general symmetrical multi-link multi-stage network V$_{mlink}$(N$_1$, N$_2$, d, s) can be operated in strictly nonblocking manner for unicast if s=2 according to the current invention.

For example, the network of FIG. **1C1** shows an exemplary five-stage network, namely V$_{mlink}$(**8**,**24**,**2**,**2**), with the following multicast assignment I$_1$={1,4} and all other I$_j$=φ for j=[2-8]. It should be noted that the connection I$_1$ fans out in the first stage switch IS**1** into middle switches MS(**1**,**1**) and MS(**1**,**2**) in middle stage **130**, and fans out in middle switches MS(**1**,**1**) and MS(**1**,**2**) only once into middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively in middle stage **140**.

The connection I$_1$ also fans out in middle switches MS(**2**,**1**) and MS(**2**,**3**) only once into middle switches MS(**3**,**1**) and MS(**3**,**4**) respectively in middle stage **150**. The connection I$_1$ also fans out in middle switches MS(**3**,**1**) and MS(**3**,**4**) only once into output switches OS**1** and OS**4** in output stage **120**. Finally the connection I$_1$ fans out once in the output stage switch OS**1** into outlet link OL**2** and in the output stage switch OS**4** twice into the outlet links OL**20** and OL**23**. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage **130**.

Asymmetric RNB (N$_1$>N$_2$) Embodiments:

Referring to FIG. **1A2**, in one embodiment, an exemplary asymmetrical multi-link multi-stage network **100A2** with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, six by eight switches IS**1**-IS**4** and output stage **120** consists of four, four by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, eight by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, four by four switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, four by four switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_2}{d},$$

where N$_1$ is the total number of inlet links or and N$_2$ is the total number of outlet links and N$_1$>N$_2$ and N$_1$=p*N$_2$ where p>1. The number of middle switches in each middle stage is denoted by

$$\frac{N_2}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d$_1$*(d+d$_1$) and each output switch OS**1**-OS**4** can be denoted in general with the notation (2×d*d), where

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d.$$

The size of each switch in any of the middle stages excepting the first middle stage can be denoted as 2d*2d. The size of each switch in the first middle stage can be denoted as (d+d$_1$)*2d. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation V$_{mlink}$(N$_1$, N$_2$, d, s), where N, represents the total number of inlet links of all input switches (for example the links IL**1**-IL**24**), N$_2$ represents the total number of outlet links of all output switches (for example the links OL**1**-OL**8**), d represents the inlet links of each input switch where N$_1$>N$_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the

$$\frac{N_2}{d}$$

input switches IS1-IS4 are connected to exactly

$$\frac{d+d_1}{2}$$

switches in middle stage **130** through $d+d_1$ links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**); input switch IS**1** is connected to middle switch MS(**1**,**2**) through the links ML(**1**,**3**) and ML(**1**,**4**); input switch IS**1** is connected to middle switch MS(**1**,**3**) through the links ML(**1**,**5**), ML(**1**,**6**); and input switch IS**1** is also connected to middle switch MS(**1**,**4**) through the links ML(**1**,**7**) and ML(**1**,**8**)).

Each of the

$$\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly

$$\frac{d+d_1}{2}$$

input switches through $d+d_1$ links (for example the links ML(**1**,**1**) and ML(**1**,**2**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**; the links ML(**1**,**9**) and ML(**1**,**10**) are connected to the middle switch MS(**1**,**1**) from input switch IS**2**; the links ML(**1**,**17**) and ML(**1**,**18**) are connected to the middle switch MS(**1**,**1**) from input switch IS**3**; and the links ML(**1**,**25**) and ML(**1**,**26**) are connected to the middle switch MS(**1**,**1**) from input switch IS**4**) and also are connected to exactly d switches in middle stage **140** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**3**) and ML(**2**,**4**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**3**)).

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**11**) and ML(**2**,**12**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**3**)) and also are connected to exactly d switches in middle stage **150** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**3**) and ML(**3**,**4**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**3**)).

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**11**) and ML(**3**,**12**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**3**)) and also are connected to exactly d output switches in output stage **120** through 2×d links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switch OS**1** from middle switch MS(**3**,**1**); and the links ML(**4**,**3**) and ML(**4**,**4**) are connected to output switch OS**2** from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_2}{d}$$

output switches OS**1**-OS**4** are connected from exactly d switches in middle stage **150** through 2×d links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**) and ML(**4**,**2**); and output switch OS**1** is also connected from middle switch MS(**3**,**2**) through the links ML(**4**,**7**) and ML(**4**,**8**)).

Finally the connection topology of the network **100A2** shown in FIG. **1A2** is known to be back to back inverse Benes connection topology.

Referring to FIG. **1B2**, in one embodiment, an exemplary asymmetrical multi-link multi-stage network **100B2** with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, six by eight switches IS**1**-IS**4** and output stage **120** consists of four, four by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, eight by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, four by four switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, four by four switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_2}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1>N_2$ and $N_1=p*N_2$ where p>1. The number of middle switches in each middle stage is denoted by

$$\frac{N_2}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation $d_1*(d+d_1)$ and each output switch OS**1**-OS**4** can be denoted in general with the notation (2×d*d), where

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d.$$

The size of each switch in any of the middle stages excepting the first middle stage can be denoted as 2d*2d. The size of each switch in the first middle stage can be denoted as $(d+d_1)*2d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**24**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**8**), d represents the inlet links of each input switch where $N_1>N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the

$$\frac{N_2}{d}$$

input switches IS**1**-IS**4** are connected to exactly

$$\frac{d+d_1}{2}$$

switches in middle stage **130** through $d+d_1$ links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**); input switch IS**1** is connected to middle switch MS(**1**,**2**) through the links ML(**1**,**3**) and ML(**1**,**4**); input switch IS**1** is connected to middle switch MS(**1**,**3**) through the links ML(**1**,**5**), ML(**1**,**6**); and input switch IS**1** is also connected to middle switch MS(**1**,**4**) through the links ML(**1**,**7**) and ML(**1**,**8**)).

Each of the

$$\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly

$$\frac{d+d_1}{2}$$

input switches through $d+d_1$ links (for example the links ML(**1**,**1**) and ML(**1**,**2**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**; the links ML(**1**,**9**) and ML(**1**,**10**) are connected to the middle switch MS(**1**,**1**) from input switch IS**2**; the links ML(**1**,**17**) and ML(**1**,**18**) are connected to the middle switch MS(**1**,**1**) from input switch IS**3**; and the links ML(**1**,**25**) and ML(**1**,**26**) are connected to the middle switch MS(**1**,**1**) from input switch IS**4**) and also are connected to exactly d switches in middle stage **140** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**3**) and ML(**2**,**4**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**2**)).

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**9**) and ML(**2**,**10**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**3**)) and also are connected to exactly d switches in middle stage **150** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**3**) and ML(**3**,**4**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**2**)).

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**9**) and ML(**3**,**10**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**3**)) and also are connected to exactly d output switches in output stage **120** through 2×d links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switch OS**1** from middle switch MS(**3**,**1**); and the links ML(**4**,**3**) and ML(**4**,**4**) are connected to output switch OS**2** from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_2}{d}$$

output switches OS**1**-OS**4** are connected from exactly d switches in middle stage **150** through 2×d links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**) and ML(**4**,**2**); and output switch OS**1** is also connected from middle switch MS(**3**,**3**) through the links ML(**4**,**9**) and ML(**4**,**10**)).

Finally the connection topology of the network **100B2** shown in FIG. **1B2** is known to be back to back Omega connection topology.

Referring to FIG. **1C2**, in one embodiment, an exemplary asymmetrical multi-link multi-stage network **100C2** with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, six by eight switches IS**1**-IS**4** and output stage **120** consists of four, four by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, eight by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, four by four switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, four by four switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_2}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1>N_2$ and $N_1=p*N_2$ where $p>1$. The number of middle switches in each middle stage is denoted by

$$\frac{N_2}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation $d_1*(d+d_1)$ and each output switch OS**1**-OS**4** can be denoted in general with the notation $(2\times d*d)$, where

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d.$$

The size of each switch in any of the middle stages excepting the first middle stage can be denoted as 2d*2d. The size of each switch in the first middle stage can be denoted as $(d+d_1)*2d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**24**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**8**), d represents the inlet links of each input switch where $N_1>N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the

$$\frac{N_2}{d}$$

input switches IS**1**-IS**4** are connected to exactly

$$\frac{d+d_1}{2}$$

switches in middle stage **130** through $d+d_1$ links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**); input switch IS**1** is connected to middle switch MS(**1**,**2**) through the links ML(**1**,**3**) and ML(**1**,**4**); input switch IS**1** is connected to middle switch MS(**1**,**3**) through the links ML(**1**,**5**), ML(**1**,**6**); and input switch IS**1** is also connected to middle switch MS(**1**,**4**) through the links ML(**1**,**7**) and ML(**1**,**8**)).

Each of the

$$\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly

$$\frac{d+d_1}{2}$$

input switches through $d+d_1$ links (for example the links ML(**1**,**1**) and ML(**1**,**2**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**; the links ML(**1**,**9**) and ML(**1**,**10**) are connected to the middle switch MS(**1**,**1**) from input switch IS**2**; the links ML(**1**,**17**) and ML(**1**,**18**) are connected to the middle switch MS(**1**,**1**) from input switch IS**3**; and the links ML(**1**,**25**) and ML(**1**,**26**) are connected to the middle switch MS(**1**,**1**) from input switch IS**4**) and also are connected to exactly d switches in middle stage **140** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**3**) and ML(**2**,**4**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**2**)).

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**15** and ML(**2**,**16**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**4**)) and also are connected to exactly d switches in middle stage **150** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**3**) and ML(**3**,**4**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**2**)).

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**15**) and ML(**3**,**16**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**4**)) and also are connected to exactly d output switches in output stage **120** through 2×d links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switch OS**1** from middle switch MS(**3**,**1**); and the links ML(**4**,**3**) and ML(**4**,**4**) are connected to output switch OS**2** from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_2}{d}$$

output switches OS**1**-OS**4** are connected from exactly d switches in middle stage **150** through 2×d links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**) and ML(**4**,**2**); and output switch OS**1** is also connected from middle switch MS(**3**,**4**) through the links ML(**4**,**15**) and ML(**4**,**16**)).

Finally the connection topology of the network **100**C**2** shown in FIG. **1**C**2** is hereinafter called nearest neighbor connection topology.

Similar to network **100**A**2** of FIG. **1**A**2**, **100**B**2** of FIG. **1**B**2**, and **100**C**2** of FIG. **1**C**2**, referring to FIG. **1**D**2**, FIG. **1**E**2**, FIG. **1**F**2**, FIG. **1**G**2**, FIG. **1**H**2**, FIG. **1**I**2** and FIG. **1**J**2** with exemplary asymmetrical multi-link multi-stage networks **100**D**2**, **100**E**2**, **100**F**2**, **100**G**2**, **100**H**2**, **100**I**2**, and **100**J**2** respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, six by eight switches IS**1**-IS**4** and output stage **120** consists of four, four by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, eight by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, four by four switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, four by four switches MS(**3**,**1**)-MS(**3**,**4**).

Such networks can also be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

The networks **100**D**2**, **100**E**2**, **100**F**2**, **100**G**2**, **100**H**2**, **100**I**2** and **100**J**2** of FIG. **1**D**2**, FIG. **1**E**2**, FIG. **1**F**2**, FIG. **1**G**2**, FIG. **1**H**2**, FIG. **1**I**2**, and FIG. **1**J**2** are also embodiments of asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**24**), d represents the inlet links of each input switch where $N_1>N_2$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Just like networks of **100**A**2**, **100**B**2** and **100**C**2**, for all the networks **100**D**2**, **100**E**2**, **100**F**2**, **100**G**2**, **100**H**2**, **100**I**2** and **100**J**2** of FIG. **1**D**2**, FIG. **1**E**2**, FIG. **1**F**2**, FIG. **1**G**2**, FIG. **1**H**2**, FIG. **1**I**2**, and FIG. **1**J**2**, each of the

$$\frac{N_2}{d}$$

input switches IS**1**-IS**4** are connected to exactly

$$\frac{d+d_2}{2}$$

switches in middle stage **130** through $d+d_2$ links.

Each of the

$$\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly

$$\frac{d+d_2}{2}$$

input switches through $d+d_2$ links and also are connected to exactly d switches in middle stage **140** through 2×d links.

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 2×d links and also are connected to exactly d switches in middle stage **150** through 2×d links.

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 2×d links and also are connected to exactly d output switches in output stage **120** through 2×d links.

Each of the

$$\frac{N_2}{d}$$

output switches OS**1**-OS**4** are connected from exactly d switches in middle stage **150** through 2×d links.

In all the ten embodiments of FIG. **1A2** to FIG. **1J2** the connection topology is different. That is the way the links ML(**1**,**1**)-ML(**1**,**16**), ML(**2**,**1**)-ML(**2**,**16**), ML(**3**,**1**)-ML(**3**,**16**), and ML(**4**,**1**)-ML(**4**,**16**) are connected between the respective stages is different. Even though only ten embodiments are illustrated, in general, the network $V_{mlink}(N_1, N_2, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{mlink}(N_1, N_2, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{mlink}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{mlink}(N_1, N_2, d, s)$ can be built. The ten embodiments of FIG. **1A2** to FIG. **1J2** are only three examples of network $V_{mlink}(N_1, N_2, d, s)$.

In all the ten embodiments of FIG. **1A2** to FIG. **1J2**, each of the links ML(**1**,**1**)-ML(**1**,**16**), ML(**2**,**1**)-ML(**2**,**16**), ML(**3**,**1**)-ML(**3**,**16**) and ML(**4**,**1**)-ML(**4**,**16**) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS**1**-IS**4** are also referred to as the network input ports. The input stage **110** is often referred to as the first stage. The output switches OS**1**-OS**4** are also referred to as the network output ports. The output stage **120** is often referred to as the last stage. The middle stage switches MS(**1**,**1**)-MS(**1**,**4**), MS(**2**,**1**)-MS(**2**,**4**), and MS(**3**,**1**)-MS(**3**,**4**) are referred to as middle switches or middle ports.

In the example illustrated in FIG. **1A2** (or in FIG. **1B2** to FIG. **1J2**), a fan-out of four is possible to satisfy a multicast connection request if input switch is IS**2**, but only two switches in middle stage **130** will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS**1**, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage **130** when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network **100A2** (or **100B2** to **100J2**), to be operated in rearrangeably nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage **130** is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage **130**, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the rearrangeably nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Asymmetric RNB ($N_2>N_1$) Embodiments:

Network **1001K2** of FIG. **1K2** is an example of general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2\times\log_d N_2)-1$ stages where $N_1>N_2$ and $N_1=p*N_2$ where p>1. In network **100K2** of FIG. **1K2**, N_2=N and N_1=p*N. The general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when s≧2 according to the current invention. Also the general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if S≧2 according to the current invention. (And in the example of FIG. **1K2**, s=2). The general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2\times\log_d N_2)-1$ stages has d_1 (where

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d$$

inlet links for each of

$$\frac{N_2}{d}$$

input switches IS**1**-IS(N_2/d) (for example the links IL**1**-IL(p*d) to the input switch IS**1**) and $d+d_1$ (=d+p×d) outgoing links for each of

$$\frac{N_2}{d}$$

input switches IS**1**-IS(N_2/d) (for example the links ML(**1**,**1**)-ML(**1**,(d+p*d)) to the input switch IS**1**). There are d outlet links for each of

$$\frac{N_2}{d}$$

output switches OS**1**-OS(N_2/d) (for example the links OL**1**-OL(d) to the output switch OS**1**) and 2×d incoming links for each of

$$\frac{N_2}{d}$$

output switches OS**1**-OS(N_2/d) (for example ML($2\times\text{Log}_d N_2$2,1)-ML($2\times\text{Log}_d N_2-2$,2×d) to the output switch OS**1**).

Each of the

$$\frac{N_2}{d}$$

input switches IS**1**-IS(N_2/d) are connected to exactly

$$\frac{d+d_1}{2}$$

switches in middle stage **130** through $d+d_1$ links.

Each of the

$$\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,N_2/d) in the middle stage **130** are connected from exactly d input switches through 2×d links and also are connected to exactly d switches in middle stage **140** through 2×d links.

Similarly each of the

$$\frac{N_2}{d}$$

middle switches

$$MS(\text{Log}_d N_2 - 1, 1) - MS\left(\text{Log}_d N_2 - 1, \frac{N_2}{d}\right)$$

in the middle stage 130+10*(Log_d N_2−2) are connected from exactly d switches in middle stage 130+10*(Log_d N_2−3) through 2×d links and also are connected to exactly d switches in middle stage 130+10*(Log_d N_2−1) through 2×d links.

Similarly each of the

$$\frac{N_2}{d}$$

middle switches

$$MS(2 \times \text{Log}_d N_2 - 3, 1) - MS\left(2 \times \text{Log}_d N_2 - 3, \frac{N_2}{d}\right)$$

in the middle stage 130+10*(2*Log_d N_2−4) are connected from exactly d switches in middle stage 130+10*(2*Log_d N_2−5) through 2×d links and also are connected to exactly d output switches in output stage 120 through 2×d links.

Each of the

$$\frac{N_2}{d}$$

output switches OS1-OS(N_2/d) are connected from exactly d switches in middle stage 130+10*(2*Log_d N_2−4) through 2×d links.

As described before, again the connection topology of a general $V_{mlink}(N_1, N_2, d, s)$ may be any one of the connection topologies. For example the connection topology of the network $V_{mlink}(N_1, N_2, d, s)$ may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general $V_{mlink}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network $V_{mlink}(N_1, N_2, d, s)$ can be built. The embodiments of FIG. 1A2 to FIG. 1J2 are ten examples of network $V_{mlink}(N_1, N_2, d, s)$ for s=2 and N_2>N_1.

The general symmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in rearrangeably non-blocking manner for multicast when s≧2 according to the current invention. Also the general symmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if S≧2 according to the current invention.

For example, the network of FIG. 1C2 shows an exemplary five-stage network, namely V_{mlink}(8,24,2,2), with the following multicast assignment I_1={1,4} and all other I_j=ϕ for j=[2-8]. It should be noted that the connection I_1 fans out in the first stage switch IS1 into middle switches MS(1,1) and MS(1,4) in middle stage 130, and fans out in middle switches MS(1,1) and MS(1,4) only once into middle switches MS(2,1) and MS(2,4) respectively in middle stage 140.

The connection I_1 also fans out in middle switches MS(2,1) and MS(2,4) only once into middle switches MS(3,1) and MS(3,4) respectively in middle stage 150. The connection I_1 also fans out in middle switches MS(3,1) and MS(3,4) only once into output switches OS1 and OS4 in output stage 120. Finally the connection I_1 fans out once in the output stage switch OS1 into outlet link OL1 and in the output stage switch OS4 twice into the outlet links OL7 and OL8. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage 130.

Symmetric Folded RNB Embodiments:

The folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ disclosed, in the current invention, is topologically exactly the same as the multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$, disclosed in the current invention so far, excepting that in the illustrations folded network $V_{fold-mlink}(N_1, N_2, d, s)$ is shown as it is folded at middle stage 130+10*(Log_d N_2−2). This is true for all the embodiments presented in the current invention.

Referring to FIG. 2A, in one embodiment, an exemplary symmetrical folded multi-link multi-stage network 200A with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by four switches IS1-IS4 and output stage 120 consists of four, four by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, four by four switches MS(1,1)-MS(1,4), middle stage 140 consists of four, four by four switches MS(2,1)-MS(2,4), and middle stage 150 consists of four, four by four switches MS(3,1)-MS(3,4).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable N/d, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by N/d. The size of each input switch IS1-IS4 can be denoted in general with the notation d*2d and each output switch OS1-OS4 can be denoted in general with the notation 2d*d. Likewise, the size of each switch in any of the middle stages can be denoted as 2d*2d. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric folded multi-link multi-stage network can be represented with the notation $V_{fold-mlink}$(N, d, s), where N represents the total number of inlet links of all input switches (for example the links IL1-IL8), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL1-IL8 as there are outlet links OL1-OL8, in a symmetrical network they are the same.

Each of the N/d input switches IS1-IS4 are connected to exactly 2×d switches in middle stage **130** through 2×d links (for example input switch IS1 is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**), and also to middle switch MS(**1**,**2**) through the links ML(**1**,**3**) and ML(**1**, **4**)).

Each of the N/d middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through 2×d links (for example the links ML(**1**,**1**) and ML(**1**, **2**) are connected to the middle switch MS(**1**,**1**) from input switch IS1, and the links ML(**1**,**7**) and ML(**1**,**8**) are connected to the middle switch MS(**1**,**1**) from input switch IS2) and also are connected to exactly d switches in middle stage **140** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**, **2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**3**) and ML(**2**,**4**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**, **3**)).

Similarly each of the N/d middle switches MS(**2**,**1**)-MS(**2**, **4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**11**) and ML(**2**,**12**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**3**)) and also are connected to exactly d switches in middle stage **150** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**3**) and ML(**3**,**4**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**3**)).

Similarly each of the N/d middle switches MS(**3**,**1**)-MS(**3**, **4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**11**) and ML(**3**,**12**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**3**)) and also are connected to exactly d output switches in output stage **120** through 2×d links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switch OS1 from Middle switch MS(**3**,**1**), and the links ML(**4**,**3**) and ML(**4**,**4**) are connected to output switch OS2 from middle switch MS(**3**,**1**)).

Each of the N/d output switches OS1-OS4 are connected from exactly 2×d switches in middle stage **150** through 2×d links (for example output switch OS1 is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**) and ML(**4**, **2**), and output switch OS1 is also connected from middle switch MS(**3**,**2**) through the links ML(**4**,**7**) and ML(**4**,**8**)).

Finally the connection topology of the network **200**A shown in FIG. **2**A is known to be back to back inverse Benes connection topology.

In other embodiments the connection topology may be different from the network **200**A of FIG. **2**A. That is the way the links ML(**1**,**1**)-ML(**1**,**16**), ML(**2**,**1**)-ML(**2**,**16**), ML(**3**,**1**)-ML(**3**,**16**), and ML(**4**,**1**)-ML(**4**,**16**) are connected between the respective stages is different. Even though only one embodiment is illustrated, in general, the network $V_{fold-mlink}$(N, d, s) can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{fold-mlink}$ (N, d, s) may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{fold-mlink}$(N, d, s) network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{fold-mlink}$(N, d, s) can be built. The embodiment of FIG. **2**A is only one example of network $V_{fold-mlink}$(N, d, s).

In the embodiment of FIG. **2**A each of the links ML(**1**,**1**)-ML(**1**,**16**), ML(**2**,**1**)-ML(**2**,**16**), ML(**3**,**1**)-ML(**3**,**16**) and ML(**4**,**1**)-ML(**4**,**16**) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS1-IS4 are also referred to as the network input ports. The input stage **110** is often referred to as the first stage. The output switches OS1-OS4 are also referred to as the network output ports. The output stage **120** is often referred to as the last stage. The middle stage switches MS(**1**, **1**)-MS(**1**,**4**) and MS(**2**,**1**)-MS(**2**,**4**) are referred to as middle switches or middle ports. The middle stage **130** is also referred to as root stage and middle stage switches MS(**2**,**1**)-MS(**2**,**4**) are referred to as root stage switches.

In the example illustrated in FIG. **2**A, a fan-out of four is possible to satisfy a multicast connection request if input switch is IS2, but only two switches in middle stage **130** will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS1, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage **130** when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network **200**A, to be operated in rearrangeably nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage **130** is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage **130**, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the rearrangeably nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Symmetric Folded RNB Embodiments:

Network **200**B of FIG. **2**B is an example of general symmetrical folded multi-link multi-stage network $V_{fold-mlink}$(N, d, s) with $(2\times\log_d N)-1$ stages. The general symmetrical folded multi-link multi-stage network $V_{fold-mlink}$(N, d, s) can be operated in rearrangeably nonblocking manner for multicast when $s\geqq 2$ according to the current invention. Also the general symmetrical folded multi-link multi-stage network $V_{fold-mlink}$(N, d, s) can be operated in strictly nonblocking manner for unicast if $S\geqq 2$ according to the current invention. (And in the example of FIG. **2**B, s=2). The general symmetrical folded multi-link multi-stage network $V_{fold-mlink}$(N, d, s) with $(2\times\log_d N)-1$ stages has d inlet links for each of N/d input switches IS1-IS(N/d) (for example the links IL1-IL(d) to the input switch IS1) and 2×d outgoing links for each of N/d input switches IS1-IS(N/d) (for example the links ML(**1**, **1**)-ML(**1**,2d) to the input switch IS1). There are d outlet links for each of N/d output switches OS1-OS(N/d) (for example the links OL1-OL(d) to the output switch OS1) and 2×d incoming links for each of N/d output switches OS1-OS(N/d) (for example ML(2×Log_d N−2,1)-ML(2×Log_d N−2,2×d) to the output switch OS1).

Each of the N/d input switches IS1-IS(N/d) are connected to exactly d switches in middle stage **130** through 2×d links.

Each of the N/d middle switches MS(**1**,**1**)-MS(**1**,N/d) in the middle stage **130** are connected from exactly d input switches through 2×d links and also are connected to exactly d switches in middle stage **140** through 2×d links.

Similarly each of the N/d middle switches

$$MS(\text{Log}_d N-1,1)-MS\left(\text{Log}_d N-1,\frac{N}{d}\right)$$

in the middle stage **130**+10*(Log_d N−2) are connected from exactly d switches in middle stage **130**+10*(Log_d N−3) through 2×d links and also are connected to exactly d switches in middle stage **130**+10*(Log_d N−1) through 2×d links.

Similarly each of the N/d middle switches

$$MS(2\times\text{Log}_d N-3,1)-MS\left(2\times\text{Log}_d N-3,\frac{N}{d}\right)$$

in the middle stage **130**+10*(2*Log_d N−4) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N−5) through 2×d links and also are connected to exactly d output switches in output stage **120** through 2×d links.

Each of the N/d output switches OS1-OS(N/d) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N−4) through 2×d links.

As described before, again the connection topology of a general $V_{fold\text{-}mlink}$(N, d, s) may be any one of the connection topologies. For example the connection topology of the network $V_{fold\text{-}mlink}$(N, d, s) may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general $V_{fold\text{-}mlink}$(N, d, s) network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network $V_{fold\text{-}mlink}$(N, d, s) can be built. The embodiment of FIG. **1**A is one example of network $V_{fold\text{-}mlink}$(N, d, s).

The general symmetrical folded multi-link multi-stage network $V_{fold\text{-}mlink}$(N, d, s) can be operated in rearrangeably nonblocking manner for multicast when s≧2 according to the current invention. Also the general symmetrical folded multi-link multi-stage network $V_{fold\text{-}mlink}$(N, d, s) can be operated in strictly nonblocking manner for unicast if s≧2 according to the current invention.

Every switch in the folded multi-link multi-stage networks discussed herein has multicast capability. In a $V_{fold\text{-}mlink}$(N, d, s) network, if a network inlet link is to be connected to more than one outlet link on the same output switch, then it is only necessary for the corresponding input switch to have one path to that output switch. This follows because that path can be multicast within the output switch to as many outlet links as necessary. Multicast assignments can therefore be described in terms of connections between input switches and output switches. An existing connection or a new connection from an input switch to r' output switches is said to have fan-out r'. If all multicast assignments of a first type, wherein any inlet link of an input switch is to be connected in an output switch to at most one outlet link are realizable, then multicast assignments of a second type, wherein any inlet link of each input switch is to be connected to more than one outlet link in the same output switch, can also be realized. For this reason, the following discussion is limited to general multicast connections of the first type

$$\left(\text{with fan-out } r',\ 1\le r'\le\frac{N}{d}\right)$$

although the same discussion is applicable to the second type.

To characterize a multicast assignment, for each inlet link

$$i\in\left\{1,2,\ldots,\frac{N}{d}\right\},$$

let I_i=O, where

$$O\subset\left\{1,2,\ldots,\frac{N}{d}\right\},$$

denote the subset of output switches to which inlet link i is to be connected in the multicast assignment. For example, the network of FIG. **1**C shows an exemplary five-stage network, namely V_{mlink}(**8**,**2**,**2**), with the following multicast assignment I_1={2,4} and all other I_j=φ for j=[2-8]. It should be noted that the connection I_1 fans out in the first stage switch IS**1** into middle switches MS(**1**,**1**) and MS(**1**,**2**) in middle stage **130**, and fans out in middle switches MS(**1**,**1**) and MS(**1**,**2**) only once into middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively in middle stage **140**.

The connection I_1 also fans out in middle switches MS(**2**,**1**) and MS(**2**,**3**) only once into middle switches MS(**3**,**2**) and MS(**3**,**4**) respectively in middle stage **150**. The connection I_1 also fans out in middle switches MS(**3**,**2**) and MS(**3**,**4**) only once into output switches OS**2** and OS**4** in output stage **120**. Finally the connection I_1 fans out once in the output stage switch OS**2** into outlet link OL**3** and in the output stage switch OS**4** twice into the outlet links OL**7** and OL**8**. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage **130**.

Asymmetric Folded RNB (N_2>N_1) Embodiments:

Referring to FIG. **2**C, in one embodiment, an exemplary asymmetrical folded multi-link multi-stage network **200**C with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by four switches IS**1**-IS**4** and output stage **120** consists of four, eight by six switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, four by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, four by four switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, four by eight switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size eight by six, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_1}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_2>N_1$ and $N_2=p*N$, where p>1. The number of middle switches in each middle stage is denoted by

$$\frac{N_1}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*2d and each output switch OS**1**-OS**4** can be denoted in general with the notation $(d+d_2)*d_2$, where

$$d_2 = N_2 \times \frac{d}{N_1} = p \times d.$$

The size of each switch in any of the middle stages excepting the last middle stage can be denoted as 2d*2d. The size of each switch in the last middle stage can be denoted as $2d*(d+d_2)$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric folded multi-link multi-stage network can be represented with the notation $V_{fold\text{-}mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**24**), d represents the inlet links of each input switch where $N_2>N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the

$$\frac{N_1}{d}$$

input switches IS**1**-IS**4** are connected to exactly d switches in middle stage **130** through 2×d links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**), and also to middle switch MS(**1**,**2**) through the links ML(**1**,**3**) and ML(**1**,**4**)).

Each of the

$$\frac{N_1}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through 2×d links (for example the links ML(**1**,**1**) and ML(**1**,**2**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**, and the links ML(**1**,**7**) and ML(**1**,**8**) are connected to the middle switch MS(**1**,**1**) from input switch IS**2**) and also are connected to exactly d switches in middle stage **140** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**3**) and ML(**2**,**4**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**3**)).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**11**) and ML(**2**,**12**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**3**)) and also are connected to exactly d switches in middle stage **150** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**3**) and ML(**3**,**4**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**3**)).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**11**) and ML(**3**,**12**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**3**)) and also are connected to exactly

$$\frac{d+d_2}{2}$$

output switches in output stage **120** through $d+d_2$ links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switch OS**1** from Middle switch MS(**3**,**1**); the links ML(**4**,**3**) and ML(**4**,**4**) are connected to output switch OS**2** from middle switch MS(**3**,**1**); the links ML(**4**,**5**) and ML(**4**,**6**) are connected to output switch OS**3** from Middle switch MS(**3**,**1**); and the links ML(**4**,**7**) and ML(**4**,**8**) are connected to output switch OS**4** from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_1}{d}$$

output switches OS1-OS4 are connected from exactly

$$\frac{d+d_2}{2}$$

switches in middle stage **150** through $d+d_2$ links (for example output switch OS1 is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**) and ML(**4**,**2**); output switch OS**1** is also connected from middle switch MS(**3**,**2**) through the links ML(**4**,**9**) and ML(**4**,**10**); output switch OS**1** is connected from middle switch MS(**3**,**3**) through the links ML(**4**,**17**) and ML(**4**,**18**); and output switch OS**1** is also connected from middle switch MS(**3**,**4**) through the links ML(**4**,**25**) and ML(**4**,**26**)).

Finally the connection topology of the network **200**C shown in FIG. **2**C is known to be back to back inverse Benes connection topology.

In other embodiments the connection topology may be different from the network **200**C of FIG. **2**C. That is the way the links ML(**1**,**1**)-ML(**1**,**16**), ML(**2**,**1**)-ML(**2**,**16**), ML(**3**,**1**)-ML(**3**,**16**), and ML(**4**,**1**)-ML(**4**,**16**) are connected between the respective stages is different. Even though only one embodiment is illustrated, in general, the network $V_{fold-mlink}$(N, d, s) can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{fold-mlink}$ (N, d, s) may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{fold-mlink}$(N, d, s) network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{fold-mlink}$(N, d, s) can be built. The embodiment of FIG. **2**C is only one example of network $V_{fold-mlink}$(N d, s).

In the embodiment of FIG. **2**C each of the links ML(**1**,**1**)-ML(**1**,**16**), ML(**2**,**1**)-ML(**2**,**16**), ML(**3**,**1**)-ML(**3**,**16**) and ML(**4**,**1**)-ML(**4**,**16**) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS**1**-IS**4** are also referred to as the network input ports. The input stage **110** is often referred to as the first stage. The output switches OS**1**-OS**4** are also referred to as the network output ports. The output stage **120** is often referred to as the last stage. The middle stage switches MS(**1**, **1**)-MS(**1**,**4**) and MS(**2**,**1**)-MS(**2**,**4**) are referred to as middle switches or middle ports. The middle stage **130** is also referred to as root stage and middle stage switches MS(**2**,**1**)-MS(**2**,**4**) are referred to as root stage switches.

In the example illustrated in FIG. **2**C, a fan-out of four is possible to satisfy a multicast connection request if input switch is IS**2**, but only two switches in middle stage **130** will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS**1**, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage **130** when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network **200**C, to be operated in rearrangeably nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage **130** is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage **130**, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the rearrangeably nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Asymmetric Folded RNB ($N_2>N_1$) Embodiments:

Network **200**D of FIG. **2**D is an example of general asymmetrical folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ with $(2\times\log_d N_1)-1$ stages where $N_2>N_1$ and $N_2=p*N$, where p>1. In network **200**D of FIG. **2**D, $N_1=N$ and $N_2=p*N$. The general asymmetrical folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s\geqq 2$ according to the current invention. Also the general asymmetrical folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if $s\geqq 2$ according to the current invention. (And in the example of FIG. **2**D, s=2). The general asymmetrical folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ with $(2\times\log_d N_1)-1$ stages has d inlet links for each of

$$\frac{N_1}{d}$$

input switches IS1-IS(N_1/d) (for example the links IL**1**-IL(d) to the input switch IS**1**) and 2×d outgoing links for each of

$$\frac{N_1}{d}$$

input switches IS**1**-IS(N_1/d) (for example the links ML(**1**,**1**)-ML(**1**,2d) to the input switch IS**1**). There are d_2

$$\left(\text{where } d_2 = N_2\times\frac{d}{N_1} = p\times d\right)$$

outlet links for each of

$$\frac{N_1}{d}$$

output switches OS**1**-OS(N_1/d) (for example the links OL**1**-OL(p*d) to the output switch OS**1**) and $d+d_2$ (=d+p×d) incoming links for each of

$$\frac{N_1}{d}$$

output switches OS**1**-OS(N_1/d) (for example ML($2\times\text{Log}_d N_1-2$,1)-ML($2\times\text{Log}_d N_1-2$, $d+d_2$) to the output switch OS**1**).

Each of the

$$\frac{N_1}{d}$$

input switches IS1-IS(N_1/d) are connected to exactly 2×d switches in middle stage **130** through 2×d links.

Each of the

$$\frac{N_1}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,N_1/d) in the middle stage **130** are connected from exactly d input switches through 2×d links and also are connected to exactly d switches in middle stage **140** through 2×d links.

Similarly each of the

$$\frac{N_1}{d}$$

middle switches

$$MS(\mathrm{Log}_d N_1 - 1, 1) - MS\left(\mathrm{Log}_d N_1 - 1, \frac{N_1}{d}\right)$$

in the middle stage **130**+10*(Log_d N_1−2) are connected from exactly d switches in middle stage **130**+10*(Log_d N_1−3) through 2×d links and also are connected to exactly d switches in middle stage **130**+10*(Log_d N_1−1) through 2×d links.

Similarly each of the

$$\frac{N_1}{d}$$

middle switches

$$MS(2 \times \mathrm{Log}_d N_1 - 3, 1) - MS\left(2 \times \mathrm{Log}_d N_1 - 3, \frac{N_1}{d}\right)$$

in the middle stage **130**+10*(2*Log_d N_1−4) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N_1−5) through 2×d links and also are connected to exactly

$$\frac{d + d_2}{2}$$

output switches in output stage **120** through d+d_2 links.

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS(N_1/d) are connected from exactly

$$\frac{d + d_2}{2}$$

switches in middle stage **130**+10*(2*Log_d N_1−4) through d+d_2 links.

As described before, again the connection topology of a general $V_{fold\text{-}mlink}(N_1, N_2, d, s)$ may be any one of the connection topologies. For example the connection topology of the network $V_{fold\text{-}mlink}(N_1, N_2, d, s)$ may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general $V_{fold\text{-}mlink}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network $V_{fold\text{-}mlink}(N_1, N_2, d, s)$ can be built. The embodiment of FIG. **1**C is one example of network $V_{fold\text{-}mlink}(N_1, N_2, d, s)$ for s=2 and N_2>N_1.

The general symmetrical folded multi-link multi-stage network $V_{fold\text{-}mlink}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when s≧2 according to the current invention. Also the general symmetrical folded multi-link multi-stage network $V_{fold\text{-}mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if s≧2 according to the current invention.

For example, the network of FIG. **2**C shows an exemplary five-stage network, namely $V_{fold\text{-}mlink}$(**8**,**24**,**2**,**2**), with the following multicast assignment I_1={1,4} and all other I_j=ϕ for j=[2-8]. It should be noted that the connection I_1 fans out in the first stage switch IS**1** into middle switches MS(**1**,**1**) and MS(**1**,**2**) in middle stage **130**, and fans out in middle switches MS(**1**,**1**) and MS(**1**,**2**) only once into middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively in middle stage **140**.

The connection I_1 also fans out in middle switches MS(**2**,**1**) and MS(**2**,**3**) only once into middle switches MS(**3**,**1**) and MS(**3**,**4**) respectively in middle stage **150**. The connection I_1 also fans out in middle switches MS(**3**,**1**) and MS(**3**,**4**) only once into output switches OS**1** and OS**4** in output stage **120**. Finally the connection I_1 fans out once in the output stage switch OS**1** into outlet link OL**2** and in the output stage switch OS**4** twice into the outlet links OL**20** and OL**23**. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage **130**.

Asymmetric Folded RNB (N_1>N_2) Embodiments:

Referring to FIG. **2**E, in one embodiment, an exemplary asymmetrical folded multi-link multi-stage network **200**E with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, six by eight switches IS**1**-IS**4** and output stage **120** consists of four, four by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, eight by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, four by four switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, four by four switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size four by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_2}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1>N_2$ and $N_1=p*N_2$ where p>1. The number of middle switches in each middle stage is denoted by

$$\frac{N_2}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation $d_1*(d+d_1)$ and each output switch OS**1**-OS**4** can be denoted in general with the notation (2×d*d), where

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d.$$

The size of each switch in any of the middle stages excepting the first middle stage can be denoted as 2d*2d. The size of each switch in the first middle stage can be denoted as $(d+d_1)*2d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric folded multi-link multi-stage network can be represented with the notation $V_{fold-mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**24**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**8**), d represents the inlet links of each input switch where $N_1>N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the

$$\frac{N_2}{d}$$

input switches IS**1**-IS**4** are connected to exactly

$$\frac{d+d_1}{2}$$

switches in middle stage **130** through $d+d_1$ links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**); input switch IS**1** is connected to middle switch MS(**1**,**2**) through the links ML(**1**,**3**) and ML(**1**,**4**); input switch IS**1** is connected to middle switch MS(**1**,**3**) through the links ML(**1**,**5**), ML(**1**,**6**); and input switch IS**1** is also connected to middle switch MS(**1**,**4**) through the links ML(**1**,**7**) and ML(**1**,**8**)).

Each of the

$$\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly

$$\frac{d+d_1}{2}$$

input switches through $d+d_1$ links (for example the links ML(**1**,**1**) and ML(**1**,**2**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**; the links ML(**1**,**9**) and ML(**1**,**10**) are connected to the middle switch MS(**1**,**1**) from input switch IS**2**; the links ML(**1**,**17**) and ML(**1**,**18**) are connected to the middle switch MS(**1**,**1**) from input switch IS**3**; and the links ML(**1**,**25**) and ML(**1**,**26**) are connected to the middle switch MS(**1**,**1**) from input switch IS**4**) and also are connected to exactly d switches in middle stage **140** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**3**) and ML(**2**,**4**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**3**)).

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 2×d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**11**) and ML(**2**,**12**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**3**)) and also are connected to exactly d switches in middle stage **150** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**3**) and ML(**3**,**4**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**3**)).

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 2×d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**11**) and ML(**3**,**12**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**3**)) and also are connected to exactly d output switches in output stage **120** through 2×d links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switch OS**1** from middle switch MS(**3**,**1**); and the links ML(**4**,**3**) and ML(**4**,**4**) are connected to output switch OS**2** from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_2}{d}$$

output switches OS**1**-OS**4** are connected from exactly d switches in middle stage **150** through 2×d links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**) and ML(**4**,**2**); and output switch OS**1** is also connected from middle switch MS(**3**,**2**) through the links ML(**4**,**7**) and ML(**4**,**8**)).

Finally the connection topology of the network **200**E shown in FIG. **2**E is known to be back to back inverse Benes connection topology.

In other embodiments the connection topology may be different from the network **200**E of FIG. **2**E. That is the way the links ML(**1**,**1**)-ML(**1**,**16**), ML(**2**,**1**)-ML(**2**,**16**), ML(**3**,**1**)-ML(**3**,**16**), and ML(**4**,**1**)-ML(**4**,**16**) are connected between the respective stages is different. Even though only one embodiment is illustrated, in general, the network $V_{fold\text{-}mlink}(N, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{fold\text{-}mlink}(N, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{fold\text{-}mlink}(N, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{fold\text{-}mlink}(N, d, s)$ can be built. The embodiment of FIG. **2**E is only one example of network $V_{fold\text{-}mlink}(N, d, s)$.

In the embodiment of FIG. **2**E each of the links ML(**1**,**1**)-ML(**1**,**16**), ML(**2**,**1**)-ML(**2**,**16**), ML(**3**,**1**)-ML(**3**,**16**) and ML(**4**,**1**)-ML(**4**,**16**) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS**1**-IS**4** are also referred to as the network input ports. The input stage **110** is often referred to as the first stage. The output switches OS**1**-OS**4** are also referred to as the network output ports. The output stage **120** is often referred to as the last stage. The middle stage switches MS(**1**,**1**)-MS(**1**,**4**) and MS(**2**,**1**)-MS(**2**,**4**) are referred to as middle switches or middle ports. The middle stage **130** is also referred to as root stage and middle stage switches MS(**2**,**1**)-MS(**2**,**4**) are referred to as root stage switches.

In the example illustrated in FIG. **2**E, a fan-out of four is possible to satisfy a multicast connection request if input switch is IS**2**, but only two switches in middle stage **130** will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS**1**, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage **130** when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network **200**E, to be operated in rearrangeably nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage **130**, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the rearrangeably nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Asymmetric Folded RNB ($N_2>N_1$) Embodiments:

Network **200**F of FIG. **2**F is an example of general asymmetrical folded multi-link multi-stage network $V_{fold\text{-}mlink}(N_1, N_2, d, s)$ with $(2\times\log_d N_2)-1$ stages where $N_1>N_2$ and $N_1=p^*N_2$ where p>1. In network **200**F of FIG. **2**F, N_2=N and N_1=p*N. The general asymmetrical folded multi-link multi-stage network $V_{fold\text{-}mlink}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when s≧2 according to the current invention. Also the general asymmetrical folded multi-link multi-stage network $V_{fold\text{-}mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if s≧2 according to the current invention. (And in the example of FIG. **2**F, s=2). The general asymmetrical folded multi-link multi-stage network $V_{fold\text{-}mlink}(N_1, N_2, d, s)$ with $(2\times\log_d N_2)-1$ stages has d, (where

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d$$

inlet links for each of

$$\frac{N_2}{d}$$

input switches IS**1**-IS(N_2/d) (for example the links IL**1**-IL(p*d) to the input switch IS**1**) and d+d, (=d+p×d) outgoing links for each of

$$\frac{N_2}{d}$$

input switches IS**1**-IS(N_2/d) (for example the links ML(**1**,**1**)-ML(**1**,(d+p*d)) to the input switch IS**1**). There are d outlet links for each of

$$\frac{N_2}{d}$$

output switches OS**1**-OS(N_2/d) (for example the links OL**1**-OL(d) to the output switch OS**1**) and 2×d incoming links for each of

$$\frac{N_2}{d}$$

output switches OS**1**-OS(N_2/d) (for example ML($2\times\text{Log}_d N_2-2$,1)-ML($2\times\text{Log}_d N_2-2$,2×d) to the output switch OS**1**).

Each of the

$$\frac{N_2}{d}$$

input switches IS**1**-IS(N_2/d) are connected to exactly

$$\frac{d+d_1}{2}$$

switches in middle stage **130** through d+d_1 links.

Each of the

$$\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,N_2/d) in the middle stage **130** are connected from exactly d input switches through 2×d links and also are connected to exactly d switches in middle stage **140** through 2×d links.

Similarly each of the

$$\frac{N_2}{d}$$

middle switches

$$MS(\text{Log}_d N_2-1,1)-MS\left(\text{Log}_d N_2-1,\ \frac{N_2}{d}\right)$$

in the middle stage **130**+10*($\text{Log}_d N_2$−2) are connected from exactly d switches in middle stage **130**+10*($\text{Log}_d N_2$−3) through 2×d links and also are connected to exactly d switches in middle stage **130**+10*($\text{Log}_d N_2$−1) through 2×d links.

Similarly each of the

$$\frac{N_2}{d}$$

middle switches

$$MS(2\times\text{Log}_d N_2-3,1)-MS\left(2\times\text{Log}_d N_2-3,\ \frac{N_2}{d}\right)$$

in the middle stage **130**+10*(2*$\text{Log}_d N_2$−4) are connected from exactly d switches in middle stage **130**+10*(2*$\text{Log}_d N_2$−5) through 2×d links and also are connected to exactly d output switches in output stage **120** through 2×d links.

Each of the

$$\frac{N_2}{d}$$

output switches OS**1**-OS(N_2/d) are connected from exactly d switches in middle stage **130**+10*(2*$\text{Log}_d N_2$−4) through 2×d links.

As described before, again the connection topology of a general $V_{fold-mlink}(N_1, N_2, d, s)$ may be any one of the connection topologies. For example the connection topology of the network $V_{fold-mlink}(N_1, N_2, d, s)$ may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general $V_{fold-mlink}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network $V_{fold-mlink}(N_1, N_2, d, s)$ can be built. The embodiment of FIG. **2**F is one example of network $V_{fold-mlink}(N_1, N_2, d, s)$ for s=2 and $N_2>N_1$.

The general symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when s≧2 according to the current invention. Also the general symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if s≧2 according to the current invention.

For example, the network of FIG. **2**E shows an exemplary five-stage network, namely $V_{fold-mlink}$(**8**,**24**,**2**,**2**), with the following multicast assignment $I_1=\{1,4\}$ and all other $I_1=\phi$ for j=[2-8]. It should be noted that the connection I_1 fans out in the first stage switch IS**1** into middle switches MS(**1**,**1**) and MS(**1**,**4**) in middle stage **130**, and fans out in middle switches MS(**1**,**1**) and MS(**1**,**4**) only once into middle switches MS(**2**,**1**) and MS(**2**,**4**) respectively in middle stage **140**.

The connection I_1 also fans out in middle switches MS(**2**,**1**) and MS(**2**,**4**) only once into middle switches MS(**3**,**1**) and MS(**3**,**4**) respectively in middle stage **150**. The connection I_1 also fans out in middle switches MS(**3**,**1**) and MS(**3**,**4**) only once into output switches OS**1** and OS**4** in output stage **120**. Finally the connection I_1 fans out once in the output stage switch OS**1** into outlet link OL**1** and in the output stage switch OS**4** twice into the outlet links OL**7** and OL**8**. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage **130**.

SNB Multi-Link Multi-Stage Embodiments:

Symmetric SNB Embodiments:

Referring to FIG. **3**A, in one embodiment, an exemplary symmetrical multi-link multi-stage network **300**A with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by six switches IS**1**-IS**4** and output stage **120** consists of four, six by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, six by six switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, six by six switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, six by six switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by six, the switches in output stage **120** are of size six by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable N/d, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by N/d. The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*3d and each output switch OS**1**-OS**4** can be denoted in general with the notation 3d*d. Likewise, the size of each switch in any of the middle stages can be denoted as 3d*3d. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric multi-link multi-stage network can be represented with the notation V_{mlink}(N, d, s), where N represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL**1**-IL**8** as there are outlet links OL**1**-OL**8**, in a symmetrical network they are the same.

Each of the N/d input switches IS**1**-IS**4** are connected to exactly 3×d switches in middle stage **130** through 3×d links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**), and ML(**1**,**3**); and also to middle switch MS(**1**,**2**) through the links ML(**1**,**4**), ML(**1**,**5**), and ML(**1**,**6**)).

Each of the N/d middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through 3×d links (for example the links ML(**1**,**1**), ML(**1**,**2**), and ML(**1**,**3**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**, and the links ML(**1**,**10**), ML(**1**,**11**), and ML(**1**,**12**) are connected to the middle switch MS(**1**,**1**) from input switch IS**2**) and also are connected to exactly d switches in middle stage **140** through 3×d links (for example the links ML(**2**,**1**), ML(**2**,**2**), and ML(**2**,**3**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**4**), ML(**2**,**5**), and ML(**2**,**6**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**3**)).

Similarly each of the N/d middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 3×d links (for example the links ML(**2**,**1**), ML(**2**,**2**), and ML(**2**,**3**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**16**), ML(**2**,**17**), and ML(**2**,**18**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**3**)) and also are connected to exactly d switches in middle stage **150** through 3×d links (for example the links ML(**3**,**1**), ML(**3**,**2**), and ML(**3**,**3**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**4**), ML(**3**,**5**), and ML(**3**,**6**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**3**)).

Similarly each of the N/d middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 3×d links (for example the links ML(**3**,**1**), ML(**3**,**2**), and ML(**3**,**3**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**16**), ML(**3**,**17**), and ML(**3**,**18**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**3**)) and also are connected to exactly d output switches in output stage **120** through 3×d links (for example the links ML(**4**,**1**), ML(**4**,**2**), and ML(**4**,**3**) are connected to output switch OS**1** from Middle switch MS(**3**,**1**), and the links ML(**4**,**10**), ML(**4**,**11**), and ML(**4**,**12**) are connected to output switch OS**2** from middle switch MS(**3**,**1**)).

Each of the N/d output switches OS**1**-OS**4** are connected from exactly 3×d switches in middle stage **150** through 3×d links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**), ML(**4**,**2**), and ML(**4**,**3**), and output switch OS**1** is also connected from middle switch MS(**3**,**2**) through the links ML(**4**,**10**), ML(**4**,**11**) and ML(**4**,**12**)).

Finally the connection topology of the network **300**A shown in FIG. **3**A is known to be back to back inverse Benes connection topology.

Referring to FIG. **3**B, in another embodiment of network V_{mlink}(N, d, s), an exemplary symmetrical multi-link multi-stage network **300**B with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by six switches IS**1**-IS**4** and output stage **120** consists of four, six by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, six by six switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, six by six switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, six by six switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by six, the switches in output stage **120** are of size six by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable N/d, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by N/d. The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*3d and each output switch OS**1**-OS**4** can be denoted in general with the notation 3d*d. Likewise, the size of each switch in any of the middle stages can be denoted as 3d*3d. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The symmetric multi-link multi-stage network of FIG. **3**B is also the network of the type V_{mlink}(N, d, s), where N represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL**1**-IL**8** as there are outlet links OL**1**-OL**8**, in a symmetrical network they are the same.

Each of the N/d input switches IS**1**-IS**4** are connected to exactly 3×d switches in middle stage **130** through 3×d links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**), and ML(**1**,**3**); and also to middle switch MS(**1**,**2**) through the links ML(**1**,**4**), ML(**1**,**5**), and ML(**1**,**6**)).

Each of the N/d middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through 3×d links (for example the links ML(**1**,**1**), ML(**1**,**2**), and ML(**1**,**3**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**, and the links ML(**1**,**13**), ML(**1**,**14**), and ML(**1**,**15**) are connected to the middle switch MS(**1**,**1**) from input switch IS**3**) and also are connected to exactly d switches in middle stage **140** through 3×d links (for example the links ML(**2**,**1**), ML(**2**,**2**), and ML(**2**,**3**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**); and the links ML(**2**,**4**), ML(**2**,**5**), and ML(**2**,**6**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**2**)).

Similarly each of the N/d middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 3×d links (for example the links ML(**2**,**1**), ML(**2**,**2**), and ML(**2**,**3**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**13**), ML(**2**,**14**), and ML(**2**,**15**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**3**)) and also are connected to exactly d switches in middle stage **150** through 3×d links (for example the links ML(**3**,**1**), ML(**3**,**2**), and ML(**3**,**3**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**4**), ML(**3**,**5**) and ML(**3**,**6**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**2**)).

Similarly each of the N/d middle switches MS(**3**,**1**)-MS(**3**, **4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 3×d links (for example the links ML(**3**,**1**), ML(**3**,**2**), and ML(**3**,**3**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**13**), ML(**3**,**14**), and ML(**3**,**15**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**3**)) and also are connected to exactly d output switches in output stage **120** through 3×d links (for example the links ML(**4**,**1**), ML(**4**, **2**), and ML(**4**,**3**) are connected to output switch OS**1** from Middle switch MS(**3**,**1**), and the links ML(**4**,**4**), ML(**4**.**5**), and ML(**4**,**6**) are connected to output switch OS**2** from middle switch MS(**3**,**1**)).

Each of the N/d output switches OS**1**-OS**4** are connected from exactly 3×d switches in middle stage **150** through 3×d links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**), ML(**4**,**2**), and ML(**4**,**3**), and output switch OS**1** is also connected from middle switch MS(**3**,**3**) through the links ML(**4**,**13**), ML(**4**, **14**), and ML(**4**,**15**)).

Finally the connection topology of the network **300**B shown in FIG. **3**B is known to be back to back Omega connection topology.

Referring to FIG. **3**C, in another embodiment of network V_{mlink}(N, d, s), an exemplary symmetrical multi-link multi-stage network **300**C with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by six switches IS**1**-IS**4** and output stage **120** consists of four, six by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, six by six switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, six by six switches MS(**2**,**1**)-MS (**2**,**4**), and middle stage **150** consists of four, six by six switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by six, the switches in output stage **120** are of size six by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable N/d, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by N/d. The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*3d and each output switch OS**1**-OS**4** can be denoted in general with the notation 3d*d. Likewise, the size of each switch in any of the middle stages can be denoted as 3d*3d. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The symmetric multi-link multi-stage network of FIG. **3**C is also the network of the type V_{mlink}(N, d, s), where N represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL**1**-IL**8** as there are outlet links OL**1**-OL**8**, in a symmetrical network they are the same.

Each of the N/d input switches IS**1**-IS**4** are connected to exactly 3×d switches in middle stage **130** through 3×d links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**), and ML(**1**,**3**); and also to middle switch MS(**1**,**2**) through the links ML(**1**,**4**), ML(**1**,**5**), and ML(**1**,**6**)).

Each of the N/d middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through 3×d links (for example the links ML(**1**,**1**), ML(**1**,**2**), and ML(**1**,**3**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**, and the links ML(**1**,**22**), ML(**1**,**23**), and ML(**1**,**24**) are connected to the middle switch MS(**1**,**1**) from input switch IS**4**) and also are connected to exactly d switches in middle stage **140** through 3×d links (for example the links ML(**2**,**1**), Ml(**2**,**2**), and ML(**2**,**3**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**4**), ML(**2**,**5**), and ML(**2**,**6**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**2**)).

Similarly each of the N/d middle switches MS(**2**,**1**)-MS(**2**, **4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 3×d links (for example the links ML(**2**,**1**), ML(**2**,**2**), and ML(**2**,**3**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**22**), ML(**2**,**23**), and ML(**2**,**24**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**4**)) and also are connected to exactly d switches in middle stage **150** through 3×d links (for example the links ML(**3**,**1**), ML(**3**,**2**), and ML(**3**,**3**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**4**), ML(**3**,**5**), and ML(**3**,**6**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**2**)).

Similarly each of the N/d middle switches MS(**3**,**1**)-MS(**3**, **4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 3×d links (for example the links ML(**3**,**1**), ML(**3**,**2**), and ML(**3**,**3**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**22**), ML(**3**,**23**), and ML(**3**,**24**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**4**)) and also are connected to exactly d output switches in output stage **120** through 3×d links (for example the links ML(**4**,**1**), ML(**4**, **2**), and ML(**4**,**3**) are connected to output switch OS**1** from middle switch MS(**3**,**1**), and the links ML(**4**,**4**), ML(**4**,**5**), and ML(**4**,**6**) are connected to output switch OS**2** from middle switch MS(**3**,**1**)).

Each of the N/d output switches OS**1**-OS**4** are connected from exactly 3×d switches in middle stage **150** through 3×d links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**), ML(**4**,**2**), and ML(**4**,**3**), and output switch OS**1** is also connected from middle switch MS(**3**,**4**) through the links ML(**4**,**22**), ML(**4**, **23**), and ML(**4**,**24**)).

Finally the connection topology of the network **300**C shown in FIG. **3**C is hereinafter called nearest neighbor connection topology.

Similar to network **300**A of FIG. **3**A, **300**B of FIG. **3**B, and **300**C of FIG. **3**C, referring to FIG. **3**D, FIG. **3**E, FIG. **3**F, FIG. **3**G, FIG. **3**H, FIG. **3**I and FIG. **3**J with exemplary symmetrical multi-link multi-stage networks **300**D, **300**E, **300**F, **300**G, **300**H, **300**I, and **300**J respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by six switches IS**1**-IS**4** and output stage **120** consists of four, six by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, six by six switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, six by six switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, six by six switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by six, the switches in output stage **120** are of size six by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

The networks **300**D, **300**E, **300**F, **300**G, **300**H, **300**I and **300**J of FIG. **3**D, FIG. **3**E, FIG. **3**F, FIG. **3**G, FIG. **3**H, FIG. **3**I, and FIG. **3**J are also embodiments of symmetric multi-link multi-stage network can be represented with the notation V_{mlink}(N, d, s), where N represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL**1**-IL**8** as there are outlet links OL**1**-OL**8**, in a symmetrical network they are the same.

Just like networks of **300**A, **300**B and **300**C, for all the networks **300**D, **300**E, **300**F, **300**G, **300**H, **300**I and **300**J of FIG. **3**D, FIG. **3**E, FIG. **3**F, FIG. **3**G, FIG. **3**H, FIG. **3**I, and FIG. **3**J, each of the N/d input switches IS**1**-IS**4** are connected to exactly 3×d switches in middle stage **130** through 3×d links.

Each of the N/d middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through 3×d links and also are connected to exactly d switches in middle stage **140** through 3×d links.

Similarly each of the N/d middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 3×d links and also are connected to exactly d switches in middle stage **150** through 3×d links.

Similarly each of the N/d middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 3×d links and also are connected to exactly d output switches in output stage **120** through 3×d links.

Each of the N/d output switches OS**1**-OS**4** are connected from exactly 3×d switches in middle stage **150** through 3×d links.

In all the ten embodiments of FIG. **3**A to FIG. **3**J the connection topology is different. That is the way the links ML(**1**,**1**)-ML(**1**,**24**), ML(**2**,**1**)-ML(**2**,**24**), ML(**3**,**1**)-ML(**3**,**24**), and ML(**4**,**1**)-ML(**4**,**24**) are connected between the respective stages is different. Even though only ten embodiments are illustrated, in general, the network V_{mlink}(N, d, s) can comprise any arbitrary type of connection topology. For example the connection topology of the network V_{mlink}(N, d, s) may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the V_{mlink}(N d, s) network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network V_{mlink}(N, d, s) can be built. The ten embodiments of FIG. **3**A to FIG. **3**J are only three examples of network V_{mlink}(N, d, s).

In all the ten embodiments of FIG. **3**A to FIG. **3**J, each of the links ML(**1**,**1**)-ML(**1**,**24**), ML(**2**,**1**)-ML(**2**,**24**), ML(**3**,**1**)-ML(**3**,**24**) and ML(**4**,**1**)-ML(**4**,**24**) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS**1**-IS**4** are also referred to as the network input ports. The input stage **110** is often referred to as the first stage. The output switches OS**1**-OS**4** are also referred to as the network output ports. The output stage **120** is often referred to as the last stage. The middle stage switches MS(**1**,**1**)-MS(**1**,**4**), MS(**2**,**1**)-MS(**2**,**4**), and MS(**3**,**1**)-MS(**3**,**4**) are referred to as middle switches or middle ports.

In the example illustrated in FIG. **3**A (or in FIG. **1**B to FIG. **3**J), a fan-out of four is possible to satisfy a multicast connection request if input switch is IS**2**, but only two switches in middle stage **130** will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS**1**, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage **130** when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network **300**A (or **300**B to **300**J), to be operated in strictly nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage **130** is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage **130**, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the strictly nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Symmetric SNB Embodiments:

Network **300**K of FIG. **3**K is an example of general symmetrical multi-link multi-stage network V_{mlink}(N, d, s) with $(2\times\log_d N)-1$ stages. The general symmetrical multi-link multi-stage network V_{mlink}(N, d, s) can be operated in strictly nonblocking manner for multicast when $s \geqq 3$ according to the current invention (and in the example of FIG. **3**K, s=3). The general symmetrical multi-link multi-stage network V_{mlink}(N, d, s) with $(2\times\log_d N)-1$ stages has d inlet links for each of N/d input switches IS**1**-IS(N/d) (for example the links IL**1**-IL(d) to the input switch IS**1**) and 3×d outgoing links for each of N/d input switches IS**1**-IS(N/d) (for example the links ML(**1**,**1**)-ML(**1**,3d) to the input switch IS**1**). There are d outlet links for each of N/d output switches OS**1**-OS(N/d) (for example the links OL**1**-OL(d) to the output switch OS**1**) and 3×d incoming links for each of N/d output switches OS**1**-OS(N/d) (for example ML($2\times\text{Log}_d N-2$,**1**)-ML($2\times\text{Log}_d N-2$,3×d) to the output switch OS**1**).

Each of the N/d input switches IS**1**-IS(N/d) are connected to exactly d switches in middle stage **130** through 3×d links.

Each of the N/d middle switches MS(**1**,**1**)-MS(**1**,N/d) in the middle stage **130** are connected from exactly d input switches through 3×d links and also are connected to exactly d switches in middle stage **140** through 3×d links.

Similarly each of the N/d middle switches

$$MS(\mathrm{Log}_d N-1,1)-MS\left(\mathrm{Log}_d N-1,\frac{N}{d}\right)$$

in the middle stage **130**+10*(Log_d N−2) are connected from exactly d switches in middle stage **130**+10*(Log_d N−3) through 3×d links and also are connected to exactly d switches in middle stage **130**+10*(Log_d N−1) through 3×d links.

Similarly each of the N/d middle switches

$$MS(2\times\mathrm{Log}_d N-3,1)-MS\left(2\times\mathrm{Log}_d N-3,\frac{N}{d}\right)$$

in the middle stage **130**+10*(2*Log_d N−4) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N−5) through 3×d links and also are connected to exactly d output switches in output stage **120** through 3×d links.

Each of the N/d output switches OS**1**-OS(N/d) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N−4) through 3×d links.

As described before, again the connection topology of a general V_{mlink}(N, d, s) may be any one of the connection topologies. For example the connection topology of the network V_{mlink}(N, d, s) may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general V_{mlink}(N, d, s) network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network V_{mlink}(N, d, s) can be built. The embodiments of FIG. **3**A to FIG. **3**J are ten examples of network V_{mlink}(N, d, s).

The general symmetrical multi-link multi-stage network V_{mlink}(N, d, s) can be operated in strictly nonblocking manner for multicast when s≧3 according to the current invention.

Every switch in the multi-link multi-stage networks discussed herein has multicast capability. In a V_{mlink}(N, d, s) network, if a network inlet link is to be connected to more than one outlet link on the same output switch, then it is only necessary for the corresponding input switch to have one path to that output switch. This follows because that path can be multicast within the output switch to as many outlet links as necessary. Multicast assignments can therefore be described in terms of connections between input switches and output switches. An existing connection or a new connection from an input switch to r' output switches is said to have fan-out r'. If all multicast assignments of a first type, wherein any inlet link of an input switch is to be connected in an output switch to at most one outlet link are realizable, then multicast assignments of a second type, wherein any inlet link of each input switch is to be connected to more than one outlet link in the same output switch, can also be realized. For this reason, the following discussion is limited to general multicast connections of the first type

$$\left(\text{with fan-out } r',\ 1\le r'\le\frac{N}{d}\right)$$

although the same discussion is applicable to the second type.

To characterize a multicast assignment, for each inlet link

$$i\in\left\{1,2,\ldots,\frac{N}{d}\right\},$$

let I_i=O, where

$$O\subset\left\{1,2,\ldots,\frac{N}{d}\right\},$$

denote the subset of output switches to which inlet link i is to be connected in the multicast assignment. For example, the network of FIG. **3**C shows an exemplary five-stage network, namely V_{mlink}(**8**,**2**,**3**), with the following multicast assignment I_1={1,4} and all other I_j=ϕ for j=[2-8]. It should be noted that the connection I_1 fans out in the first stage switch IS**1** into middle switches MS(**1**,**1**) and MS(**1**,**2**) in middle stage **130**, and fans out in middle switches MS(**1**,**1**) and MS(**1**,**2**) only once into middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively in middle stage **140**.

The connection I_1 also fans out in middle switches MS(**2**,**1**) and MS(**2**,**3**) only once into middle switches MS(**3**,**1**) and MS(**3**,**4**) respectively in middle stage **150**. The connection I_1 also fans out in middle switches MS(**3**,**1**) and MS(**3**,**4**) only once into output switches OS**1** and OS**4** in output stage **120**. Finally the connection I_1 fans out once in the output stage switch OS**1** into outlet link OL**1** and in the output stage switch OS**4** twice into the outlet links OL**7** and OL**8**. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage **130**.

Asymmetric SNB (N_2>N_1) Embodiments:

Referring to FIG. **3A1**, in one embodiment, an exemplary asymmetrical multi-link multi-stage network **300A1** with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by six switches IS**1**-IS**4** and output stage **120** consists of four, eight by six switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, six by six switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, six by six switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, four by eight switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by six, the switches in output stage **120** are of size eight by six, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_1}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and N_2>N_1 and N_2=p*N_1 where p>1.

The number of middle switches in each middle stage is denoted by

$$\frac{N_1}{d}.$$

The size of each input switch IS1-IS4 can be denoted in general with the notation d*3d and each output switch OS1-OS4 can be denoted in general with the notation $(2d+d_2)*d_2$, where

$$d_2 = N_2 \times \frac{d}{N_1} = p \times d.$$

The size of each switch in any of the middle stages excepting the last middle stage can be denoted as 3d*3d. The size of each switch in the last middle stage can be denoted as $3d*(2d+d_2)$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL8), N represents the total number of outlet links of all output switches (for example the links OL1-OL24), d represents the inlet links of each input switch where $N_2>N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the

$$\frac{N_1}{d}$$

input switches IS1-IS4 are connected to exactly d switches in middle stage 130 through 3×d links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and ML(1,3); and also to middle switch MS(1,2) through the links ML(1,4), ML(1,5), and ML(1,6)).

Each of the

$$\frac{N_1}{d}$$

middle switches MS(1,1)-MS(1,4) in the middle stage 130 are connected from exactly d input switches through 3×d links (for example the links ML(1,1), ML(1,2), and ML(1,3) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,13), ML(1,14), and ML(1,15) are connected to the middle switch MS(1,1) from input switch IS3) and also are connected to exactly d switches in middle stage 140 through 3×d links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected from middle switch MS(1,1) to middle switch MS(2,1); and the links ML(2,4), ML(2,5), and ML(2,6) are connected from middle switch MS(1,1) to middle switch MS(2,2)).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(2,1)-MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through 3×d links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,13), ML(2,14), and ML(2,15) are connected to the middle switch MS(2,1) from middle switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through 3×d links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,4), ML(3,5) and ML(3,6) are connected from middle switch MS(2,1) to middle switch MS(3,2)).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(3,1)-MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through 3×d links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,13), ML(3,14), and ML(3,15) are connected to the middle switch MS(3,1) from middle switch MS(2,3)) and also are connected to exactly

$$\frac{2d + d_2}{3}$$

output switches in output stage 120 through $2d+d_1$ links (For example the links ML(4,1), ML(4,2), and ML(4,3) are connected to output switch OS1 from Middle switch MS(3,1); the links ML(4,4), ML(4.5), and ML(4,6) are connected to output switch OS2 from middle switch MS(3,1); the links ML(4,7), ML(4,8), and ML(4,9) are connected to output switch OS3 from Middle switch MS(3,1); the links ML(4,10), ML(4.11), and ML(4,12) are connected to output switch OS2 from middle switch MS(3,1)).

Each of the

$$\frac{N_1}{d}$$

output switches ON1-OS4 are connected from exactly

$$\frac{2d + d_2}{3}$$

switches in middle stage 150 through $2d+d_2$ links (for example output switch OS1 is connected from middle switch MS(3,1) through the links ML(4,1), ML(4,2), and ML(4,3); output switch OS1 is also connected from middle switch MS(3,2) through the links ML(4,16), ML(4,17), and ML(4,18); output switch OS1 is connected from middle switch MS(3,3) through the links ML(4,28), ML(4,29), and ML(4,30); and output switch OS1 is also connected from middle switch MS(3,4) through the links ML(4,43), ML(4,44), and ML(4,45)).

Finally the connection topology of the network 300A1 shown in FIG. 3A1 is known to be back to back inverse Benes connection topology.

Referring to FIG. 3B1, in one embodiment, an exemplary asymmetrical multi-link multi-stage network 300B1 with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by six switches IS1-IS4 and output stage 120 consists of four, eight by six switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, six by six switches MS(1,1)-MS(1,4), middle stage 140 consists of four, six by six switches MS(2,1)-MS(2,4), and middle stage 150 consists of four, four by eight switches MS(3,1)-MS(3,4).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by six, the switches in output stage 120 are of size eight by six, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable

$$\frac{N_1}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_2>N_1$ and $N_2=p*N_1$ where $p>1$. The number of middle switches in each middle stage is denoted by

$$\frac{N_1}{d}.$$

The size of each input switch IS1-IS4 can be denoted in general with the notation d*3d and each output switch OS1-OS4 can be denoted in general with the notation $(2d+d_2)*d_2$, where

$$d_2 = N_2 \times \frac{d}{N_1} = p \times d.$$

The size of each switch in any of the middle stages excepting the last middle stage can be denoted as 3d*3d. The size of each switch in the last middle stage can be denoted as $2d*(2d+d_2)$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL1-IL8), N_2 represents the total number of outlet links of all output switches (for example the links OL1-OL24), d represents the inlet links of each input switch where $N_2>N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the

$$\frac{N_1}{d}$$

input switches IS1-IS4 are connected to exactly 3×d switches in middle stage 130 through 3×d links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and ML(1,3); and also to middle switch MS(1,2) through the links ML(1,4), ML(1,5), and ML(1,6)).

Each of the

$$\frac{N_1}{d}$$

middle switches MS(1,1)-MS(1,4) in the middle stage 130 are connected from exactly d input switches through 3×d links (for example the links ML(1,1), ML(1,2), and ML(1,3) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,13), ML(1,14), and ML(1,15) are connected to the middle switch MS(1,1) from input switch IS3) and also are connected to exactly d switches in middle stage 140 through 3×d links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected from middle switch MS(1,1) to middle switch MS(2,1); and the links ML(2,4), ML(2,5), and ML(2,6) are connected from middle switch MS(1,1) to middle switch MS(2,2)).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(2,1)-MS(2,4) in the middle stage 140 are connected from exactly d switches in middle stage 130 through 3×d links (for example the links ML(2,1), ML(2,2), and ML(2,3) are connected to the middle switch MS(2,1) from middle switch MS(1,1), and the links ML(2,13), ML(2,14), and ML(2,15) are connected to the middle switch MS(2,1) from middle switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through 3×d links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,4), ML(3,5) and ML(3,6) are connected from middle switch MS(2,1) to middle switch MS(3,2)).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(3,1)-MS(3,4) in the middle stage 150 are connected from exactly d switches in middle stage 140 through 3×d links (for example the links ML(3,1), ML(3,2), and ML(3,3) are connected to the middle switch MS(3,1) from middle switch MS(2,1), and the links ML(3,13), ML(3,14), and ML(3,15) are connected to the middle switch MS(3,

1) from middle switch MS(**2**,**3**)) and also are connected to exactly

$$\frac{2d+d_2}{3}$$

output switches in output stage **120** through 2d+d_2 links (For example the links ML(**4**,**1**), ML(**4**,**2**), and ML(**4**,**3**) are connected to output switch OS**1** from Middle switch MS(**3**,**1**); the links ML(**4**,**4**), ML(**4**.**5**), and ML(**4**,**6**) are connected to output switch OS**2** from middle switch MS(**3**,**1**); the links ML(**4**,**7**), ML(**4**,**8**), and ML(**4**,**9**) are connected to output switch OS**3** from Middle switch MS(**3**,**1**); the links ML(**4**,**10**), ML(**4**.**11**), and ML(**4**,**12**) are connected to output switch OS**2** from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS**4** are connected from exactly

$$\frac{2d+d_2}{3}$$

switches in middle stage **150** through 2d+d_2 links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**), ML(**4**,**2**), and ML(**4**,**3**); output switch OS**1** is also connected from middle switch MS(**3**,**2**) through the links ML(**4**,**16**), ML(**4**,**17**), and ML(**4**,**18**); output switch OS**1** is connected from middle switch MS(**3**,**3**) through the links ML(**4**,**28**), ML(**4**,**29**), and ML(**4**,**30**); and output switch OS**1** is also connected from middle switch MS(**3**,**4**) through the links ML(**4**,**43**), ML(**4**,**44**), and ML(**4**,**45**)).

Finally the connection topology of the network **300**B**1** shown in FIG. **3**B**1** is known to be back to back Omega connection topology.

Referring to FIG. **3**C**1**, in one embodiment, an exemplary asymmetrical multi-link multi-stage network **300**C**1** with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by six switches IS**1**-IS**4** and output stage **120** consists of four, eight by six switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, six by six switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, six by six switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, four by eight switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by six, the switches in output stage **120** are of size eight by six, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_1}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_2>N_1$ and $N_2=p*N_1$ where p>1. The number of middle switches in each middle stage is denoted by

$$\frac{N_1}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*3d and each output switch OS**1**-OS**4** can be denoted in general with the notation (2d+d_2)*d_2, where

$$d_2 = N_2\times\frac{d}{N_1} = p\times d.$$

The size of each switch in any of the middle stages excepting the last middle stage can be denoted as 3d*3d. The size of each switch in the last middle stage can be denoted as 2d*(2d+d_2). A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**24**), d represents the inlet links of each input switch where $N_2>N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the

$$\frac{N_1}{d}$$

input switches IS**1**-IS**4** are connected to exactly 3×d switches in middle stage **130** through 3×d links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**), and ML(**1**,**3**); and also to middle switch MS(**1**,**2**) through the links ML(**1**,**4**), ML(**1**,**5**), and ML(**1**,**6**)).

Each of the

$$\frac{N_1}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through 3×d links (for example the links ML(**1**,**1**), ML(**1**,**2**), and ML(**1**,**3**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**, and the links ML(**1**,**22**), ML(**1**,**23**), and ML(**1**,**24**) are connected to the middle switch MS(**1**,**1**) from input switch IS**4**)) and also are connected to exactly d switches in middle stage **140** through 3×d links (for example the links ML(**2**,**1**), Ml(**2**,**2**), and ML(**2**,**3**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**4**), ML(**2**,**5**), and ML(**2**,**6**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**2**)).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 3×d links (for example the links ML(**2**,**1**), ML(**2**,**2**), and ML(**2**,**3**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**22**), ML(**2**,**23**), and ML(**2**,**24**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**4**)) and also are connected to exactly d switches in middle stage **150** through 3×d links (for example the links ML(**3**,**1**), ML(**3**,**2**), and ML(**3**,**3**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**4**), ML(**3**,**5**), and ML(**3**,**6**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**2**)).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 3×d links (for example the links ML(**3**,**1**), ML(**3**,**2**), and ML(**3**,**3**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**22**), ML(**3**,**23**), and ML(**3**,**24**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**4**)) and also are connected to exactly

$$\frac{2d + d_2}{3}$$

output switches in output stage **120** through $2d+d_2$ links

(For example the links ML(**4**,**1**), ML(**4**,**2**), and ML(**4**,**3**) are connected to output switch OS**1** from Middle switch MS(**3**,**1**); the links ML(**4**,**4**), ML(**4**.**5**), and ML(**4**,**6**) are connected to output switch OS**2** from middle switch MS(**3**,**1**); the links ML(**4**,**7**), ML(**4**,**8**), and ML(**4**,**9**) are connected to output switch OS**3** from Middle switch MS(**3**,**1**); the links ML(**4**,**10**), ML(**4**.**11**), and ML(**4**,**12**) are connected to output switch OS**2** from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS**4** are connected from exactly

$$\frac{2d + d_2}{3}$$

switches in middle stage **150** through $2d+d_2$ links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**), ML(**4**,**2**), and ML(**4**,**3**); output switch OS**1** is also connected from middle switch MS(**3**,**2**) through the links ML(**4**,**16**), ML(**4**,**17**), and ML(**4**,**18**); output switch OS**1** is connected from middle switch MS(**3**,**3**) through the links ML(**4**,**28**), ML(**4**,**29**), and ML(**4**,**30**); and output switch OS**1** is also connected from middle switch MS(**3**,**4**) through the links ML(**4**,**43**), ML(**4**,**44**), and ML(**4**,**45**)).

Finally the connection topology of the network **300C1** shown in FIG. **3C1** is hereinafter called nearest neighbor connection topology.

Similar to network **300A1** of FIG. **3A1**, **300B1** of FIG. **3B1**, and **300C1** of FIG. **3C1**, referring to FIG. **3D1**, FIG. **3E1**, FIG. **3F1**, FIG. **3G1**, FIG. **3H1**, FIG. **3I1** and FIG. **3J1** with exemplary asymmetrical multi-link multi-stage networks **300D1**, **300E1**, **300F1**, **300G1**, **300H1**, **300I1**, and **300J1** respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by six switches IS**1**-IS**4** and output stage **120** consists of four, six by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, six by six switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, six by six switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, six by six switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by six, the switches in output stage **120** are of size six by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

The networks **300D1**, **300E1**, **300F1**, **300G1**, **300H1**, **300I1** and **300J1** of FIG. **3D1**, FIG. **3E1**, FIG. **3F1**, FIG. **3G1**, FIG. **3H1**, FIG. **3I1**, and FIG. **3J1** are also embodiments of asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**24**), d represents the inlet links of each input switch where $N_2>N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Just like networks of **300A1**, **300B1** and **300C1**, for all the networks **300D1**, **300E1**, **300F1**, **300G1**, **300H1**, **300I1** and **300J1** of FIG. **3D1**, FIG. **3E1**, FIG. **3F1**, FIG. **3G1**, FIG. **3H1**, FIG. **3I1**, and FIG. **3J1**, each of the

$$\frac{N_1}{d}$$

input switches IS**1**-IS**4** are connected to exactly d switches in middle stage **130** through 3×d links.

Each of the

$$\frac{N_1}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through 3×d links and also are connected to exactly d switches in middle stage **140** through 3×d links.

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 3×d links and also are connected to exactly d switches in middle stage **150** through 3×d links.

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 3×d links and also are connected to exactly

$$\frac{2d + d_2}{3}$$

output switches in output stage **120** through 2d+d links.

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS**4** are connected from exactly

$$\frac{2d + d_2}{3}$$

switches in middle stage **150** through 2d+d_2 links

In all the ten embodiments of FIG. **3A1** to FIG. **3J1** the connection topology is different. That is the way the links ML(**1**,**1**)-ML(**1**,**24**), ML(**2**,**1**)-ML(**2**,**24**), ML(**3**,**1**)-ML(**3**,**24**), and ML(**4**,**1**)-ML(**4**,**48**) are connected between the respective stages is different. Even though only ten embodiments are illustrated, in general, the network $V_{mlink}(N_1, N_2, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{mlink}(N_1, N_2, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{mlink}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{mlink}(N_1, N_2, d, s)$ can be built. The ten embodiments of FIG. **3A1** to FIG. **3J1** are only three examples of network $V_{mlink}(N_1, N_2, d, s)$.

In all the ten embodiments of FIG. **3A1** to FIG. **3J1**, each of the links ML(**1**,**1**)-ML(**1**,**24**), ML(**2**,**1**)-ML(**2**,**24**), ML(**3**,**1**)-ML(**3**,**24**) and ML(**4**,**1**)-ML(**4**,**48**) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS**1**-IS**4** are also referred to as the network input ports. The input stage **110** is often referred to as the first stage. The output switches OS**1**-OS**4** are also referred to as the network output ports. The output stage **120** is often referred to as the last stage. The middle stage switches MS(**1**,**1**)-MS(**1**,**4**), MS(**2**,**1**)-MS(**2**,**4**), and MS(**3**,**1**)-MS(**3**,**4**) are referred to as middle switches or middle ports.

In the example illustrated in FIG. **3A1** (or in FIG. **3**B**1** to FIG. **3**J**1**), a fan-out of four is possible to satisfy a multicast connection request if input switch is IS**2**, but only two switches in middle stage **130** will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS**1**, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage **130** when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network **300**A**1** (or **300**B**1** to **300**J**1**), to be operated in strictly nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage **130** is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage **130**, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the strictly nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Asymmetric SNB (N_2>N_1) Embodiments:

Network **300**K**1** of FIG. **3**K**1** is an example of general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2\times\log_d N_1)-1$ stages where $N_2>N_1$ and $N=p*N_1$ where p>1. In network **300**K**1** of FIG. **3**K**1**, $N_1=N$ and $N_2=p*N$. The general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for multicast when 3 according to the current invention (and in the example of FIG. **3**K**1**, s=3). The general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2\times\log_d N_1)-1$ stages has d inlet links for each of

$$\frac{N_1}{d}$$

input switches IS**1**-IS(N_1/d) (for example the links IL**1**-IL(d) to the input switch IS**1**) and 3×d outgoing links for each of

$$\frac{N_1}{d}$$

input switches IS**1**-IS(N_1/d) (for example the links ML(**1**,**1**)-ML(1,3d) to the input switch IS**1**). There are d_2

$$\left(\text{where } d_2 = N_2 \times \frac{d}{N_1} = p \times d\right)$$

outlet links for each of

$$\frac{N_1}{d}$$

output switches OS**1**-OS(N_1/d) (for example the links OL**1**-OL(p*d) to the output switch OS**1**) and 2d+d_2 (=2d+p×d) incoming links for each of

$$\frac{N_1}{d}$$

output switches OS**1**-OS(N_1/d) (for example ML(2×Log_d N_1−2,1)-ML(2×Log_d N_1−2,2d+d_2) to the output switch OS**1**).

Each of the

$$\frac{N_1}{d}$$

input switches IS**1**-IS(N_1/d) are connected to exactly 3×d switches in middle stage **130** through 3×d links.

Each of the

$$\frac{N_1}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,N_1/d) in the middle stage **130** are connected from exactly d input switches through 3×d links and also are connected to exactly d switches in middle stage **140** through 3×d links.

Similarly each of the

$$\frac{N_1}{d}$$

middle switches

$$MS(\text{Log}_d N_1 - 1, 1) - MS\left(\text{Log}_d N_1 - 1, \frac{N_1}{d}\right)$$

in the middle stage **130**+10*(Log_d N_1−2) are connected from exactly d switches in middle stage **130**+10*(Log_d N_1−3) through 3×d links and also are connected to exactly d switches in middle stage **130**+10*(Log_d N_1−1) through 3×d links.

Similarly each of the

$$\frac{N_1}{d}$$

middle switches

$$MS(2 \times \text{Log}_d N_1 - 3, 1) - MS\left(2 \times \text{Log}_d N_1 - 3, \frac{N_1}{d}\right)$$

in the middle stage **130**+10*(2*Log_d N_1−4) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N_1−5) through 3×d links and also are connected to exactly

$$\frac{2d + d_2}{3}$$

output switches in output stage **120** through 2d+d_2 links.

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS(N_1/d) are connected from exactly

$$\frac{2d + d_2}{3}$$

switches in middle stage **130**+10*(2*Log_d N_1−4) through 2d+d_2 links.

As described before, again the connection topology of a general $V_{mlink}(N_1, N_2, d, s)$ may be any one of the connection topologies. For example the connection topology of the network $V_{mlink}(N_1, N_2, d, s)$ may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general $V_{mlink}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network $V_{mlink}(N_1, N_2, d, s)$ can be built. The embodiments of FIG. **3A1** to FIG. **3J1** are ten examples of network $V_{mlink}(N_1, N_2, d, s)$ for s=3 and N_2>N_1.

The general symmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for multicast when 3 according to the current invention.

For example, the network of FIG. **3C1** shows an exemplary five-stage network, namely V_{mlink}(**8**,**24**,**2**,**3**), with the following multicast assignment I_1={1,4} and all other I_j=φ for j=[2-8]. It should be noted that the connection I_1 fans out in the first stage switch IS**1** into middle switches MS(**1**,**1**) and MS(**1**,**2**) in middle stage **130**, and fans out in middle switches MS(**1**,**1**) and MS(**1**,**2**) only once into middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively in middle stage **140**.

The connection I_1 also fans out in middle switches MS(**2**,**1**) and MS(**2**,**3**) only once into middle switches MS(**3**,**1**) and MS(**3**,**4**) respectively in middle stage **150**. The connection I_1 also fans out in middle switches MS(**3**,**1**) and MS(**3**,**4**) only once into output switches OS**1** and OS**4** in output stage **120**. Finally the connection I_1 fans out once in the output stage switch OS**1** into outlet link OL**2** and in the output stage switch OS**4** twice into the outlet links OL**19** and OL**21**. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage **130**.

Asymmetric SNB (N_1>N_2) Embodiments:

Referring to FIG. **3A2**, in one embodiment, an exemplary asymmetrical multi-link multi-stage network **300A2** with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, six by eight switches IS**1**-IS**4** and output stage **120** consists of four, six by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, eight by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, six by six switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, six by six switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size six by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_2}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1>N_2$ and $N_1=p*N_2$ where p>1. The number of middle switches in each middle stage is denoted by

$$\frac{N_2}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation $d_1*(2d+d_1)$ and each output switch OS**1**-OS**4** can be denoted in general with the notation 3d*d, where

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d.$$

The size of each switch in any of the middle stages excepting the first middle stage can be denoted as 3d*3d. The size of each switch in the first middle stage can be denoted as $(2d+d_1)*3d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**24**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**8**), d represents the inlet links of each input switch where $N_1>N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the

$$\frac{N_2}{d}$$

input switches IS**1**-IS**4** are connected to exactly

$$\frac{2d+d_1}{3}$$

switches in middle stage **130** through $2d+d_1$ links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**), and ML(**1**,**3**); input switch IS**1** is also connected to middle switch MS(**1**,**2**) through the links ML(**1**,**4**), ML(**1**,**5**), and ML(**1**,**6**); input switch IS**1** is connected to middle switch MS(**1**,**3**) through the links ML(**1**,**7**), ML(**1**,**8**), and ML(**1**,**9**); and input switch IS**1** is also connected to middle switch MS(**1**,**4**) through the links ML(**1**,**10**), ML(**1**,**11**), and ML(**1**,**12**)).

Each of the

$$\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly

$$\frac{2d+d_1}{3}$$

input switches through $2d+d_1$ links (for example middle switch MS(**1**,**1**) is connected from input switch IS**1** through the links ML(**1**,**1**), ML(**1**,**2**), and ML(**1**,**3**); middle switch MS(**1**,**1**) is connected from input switch IS**2** through the links ML(**1**,**16**), ML(**1**,**17**), and ML(**1**,**18**); middle switch MS(**1**,**1**) is connected from input switch IS**3** through the links ML(**1**, **28**), ML(**1**,**29**), and ML(**1**,**30**); and middle switch MS(**1**,**1**) is connected from input switch IS**4** through the links ML(**1**,**43**), ML(**1**,**44**), and ML(**1**,**45**)) and also are connected to exactly d switches in middle stage **140** through 3×d links (for example the links ML(**2**,**1**), ML(**2**,**2**), and ML(**2**,**3**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**4**), ML(**2**,**5**), and ML(**2**,**6**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**3**)).

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 3×d links (for example the links ML(**2**,**1**), ML(**2**,**2**), and ML(**2**,**3**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**16**), ML(**2**, **17**), and ML(**2**,**18**) are connected to the middle switch MS(**2**, **1**) from middle switch MS(**1**,**3**)) and also are connected to exactly d switches in middle stage **150** through 3×d links (for example the links ML(**3**,**1**), ML(**3**,**2**), and ML(**3**,**3**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**, **1**), and the links ML(**3**,**4**), ML(**3**,**5**), and ML(**3**,**6**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**, **3**)).

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 3×d links (for example the links ML(**3**,**1**), ML(**3**,**2**), and ML(**3**,**3**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**16**), ML(**3**, **17**), and ML(**3**,**18**) are connected to the middle switch MS(**3**, **1**) from middle switch MS(**2**,**3**)) and also are connected to exactly d output switches in output stage **120** through 3×d links (for example the links ML(**4**,**1**), ML(**4**,**2**), and ML(**4**,**3**) are connected to output switch OS**1** from Middle switch MS(**3**,**1**), and the links ML(**4**,**10**), ML(**4**,**11**), and ML(**4**,**12**) are connected to output switch OS**2** from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_2}{d}$$

output switches OS**1**-OS**4** are connected from exactly d switches in middle stage **150** through 3×d links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**), ML(**4**,**2**), and ML(**4**,**3**), and output switch OS**1** is also connected from middle switch MS(**3**,**2**) through the links ML(**4**,**10**), ML(**4**,**11**) and ML(**4**,**12**)).

Finally the connection topology of the network **300**A**2** shown in FIG. **3**A**2** is known to be back to back inverse Benes connection topology.

Referring to FIG. **3**B**2**, in one embodiment, an exemplary asymmetrical multi-link multi-stage network **300**B**2** with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, six by eight switches IS**1**-IS**4** and output stage **120** consists of four, six by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, eight by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, six by six switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, six by six switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size six by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_2}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1>N_2$ and $N_1=p*N_2$ where p>1. The number of middle switches in each middle stage is denoted by

$$\frac{N_2}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation $d_1*(2d+d_1)$ and each output switch OS**1**-OS**4** can be denoted in general with the notation 3d*d, where

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d.$$

The size of each switch in any of the middle stages excepting the first middle stage can be denoted as 3d*3d. The size of each switch in the first middle stage can be denoted as $(2d+d_1)*3d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**24**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**8**), d represents the inlet links of each input switch where $N_1>N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the

$$\frac{N_2}{d}$$

input switches IS**1**-IS**4** are connected to exactly

$$\frac{2d+d_1}{3}$$

switches in middle stage **130** through $2d+d_1$ links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**), and ML(**1**,**3**); input switch IS**1** is also connected to middle switch MS(**1**,**2**) through the links ML(**1**,**4**), ML(**1**,**5**), and ML(**1**,**6**); input switch IS**1** is connected to middle switch MS(**1**,**3**) through the links ML(**1**,**7**), ML(**1**,**8**), and ML(**1**,**9**); and input switch IS**1** is also connected to middle switch MS(**1**,**4**) through the links ML(**1**,**10**), ML(**1**,**11**), and ML(**1**,**12**)).

Each of the

$$\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly

$$\frac{2d+d_1}{3}$$

input switches through $2d+d_1$ links (for example middle switch MS(**1**,**1**) is connected from input switch IS**1** through the links ML(**1**,**1**), ML(**1**,**2**), and ML(**1**,**3**); middle switch MS(**1**,**1**) is connected from input switch IS**2** through the links ML(**1**,**16**), ML(**1**,**17**), and ML(**1**,**18**); middle switch MS(**1**,**1**) is connected from input switch IS**3** through the links ML(**1**, **28**), ML(**1**,**29**), and ML(**1**,**30**); and middle switch MS(**1**,**1**) is connected from input switch IS**4** through the links ML(**1**,**43**), ML(**1**,**44**), and ML(**1**,**45**)) and also are connected to exactly d switches in middle stage **140** through 2×d links (for example the links ML(**2**,**1**), ML(**2**,**2**), and ML(**2**,**3**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**); and the links ML(**2**,**4**), ML(**2**,**5**), and ML(**2**,**6**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**2**)).

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 3×d links (for example the links ML(**2**,**1**), ML(**2**,**2**), and ML(**2**,**3**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**13**), ML(**2**,**14**), and ML(**2**,**15**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**3**)) and also are connected to exactly d switches in middle stage **150** through 3×d links (for example the links ML(**3**,**1**), ML(**3**,**2**), and ML(**3**,**3**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**4**), ML(**3**,**5**) and ML(**3**,**6**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**2**)).

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 3×d links (for example the links ML(**3**,**1**), ML(**3**,**2**), and ML(**3**,**3**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**13**), ML(**3**,**14**), and ML(**3**,**15**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**3**)) and also are connected to exactly d output switches in output stage **120** through 3×d links (for example the links ML(**4**,**1**), ML(**4**,**2**), and ML(**4**,**3**) are connected to output switch OS**1** from Middle switch MS(**3**,**1**), and the links ML(**4**,**4**), ML(**4**.**5**), and ML(**4**,**6**) are connected to output switch OS**2** from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_2}{d}$$

output switches OS**1**-OS**4** are connected from exactly d switches in middle stage **150** through 3×d links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**), ML(**4**,**2**), and ML(**4**,**3**), and output switch OS**1** is also connected from middle switch MS(**3**,**3**) through the links ML(**4**,**13**), ML(**4**,**14**), and ML(**4**,**15**)).

Finally the connection topology of the network **300**B**2** shown in FIG. **3**B**2** is known to be back to back Omega connection topology.

Referring to FIG. **3**C**2**, in one embodiment, an exemplary asymmetrical multi-link multi-stage network **300**C**2** with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, six by eight switches IS**1**-IS**4** and output stage **120** consists of four, six by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, eight by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, six by six switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, six by six switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size six by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_2}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1>N_2$ and $N_1=p*N_2$ where p>1. The number of middle switches in each middle stage is denoted by

$$\frac{N_2}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation $d_1*(2d+d_1)$ and each output switch OS**1**-OS**4** can be denoted in general with the notation 3d*d, where

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d.$$

The size of each switch in any of the middle stages excepting the first middle stage can be denoted as 3d*3d. The size of each switch in the first middle stage can be denoted as $(2d+d_1)*3d$. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**24**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**8**), d represents the inlet links of each input switch where $N_1>N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the

$$\frac{N_2}{d}$$

input switches IS**1**-IS**4** are connected to exactly

$$\frac{2d+d_1}{3}$$

switches in middle stage **130** through $2d+d_1$ links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**), ML(**1**,**2**), and ML(**1**,**3**); input switch IS**1** is also connected to middle switch MS(**1**,**2**) through the links ML(**1**,**4**), ML(**1**,**5**), and ML(**1**,**6**); input switch IS**1** is connected to middle switch MS(**1**,**3**) through the links ML(**1**,**7**), ML(**1**,**8**), and ML(**1**,**9**); and input switch IS**1** is also connected to middle switch MS(**1**,**4**) through the links ML(**1**,**10**), ML(**1**,**11**), and ML(**1**,**12**)).

Each of the

$$\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly

$$\frac{2d+d_1}{3}$$

input switches through $2d+d_1$ links (for example middle switch MS(**1**,**1**) is connected from input switch IS**1** through the links ML(**1**,**1**), ML(**1**,**2**), and ML(**1**,**3**); middle switch MS(**1**,**1**) is connected from input switch IS**2** through the links ML(**1**,**16**), ML(**1**,**17**), and ML(**1**,**18**); middle switch MS(**1**,**1**) is connected from input switch IS**3** through the links ML(**1**,**28**), ML(**1**,**29**), and ML(**1**,**30**); and middle switch MS(**1**,**1**) is connected from input switch IS**4** through the links ML(**1**,**43**), ML(**1**,**44**), and ML(**1**,**45**)) and also are connected to exactly d switches in middle stage **140** through 3×d links (for example the links ML(**2**,**1**), Ml(**2**,**2**), and ML(**2**,**3**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**), and the links ML(**2**,**4**), ML(**2**,**5**), and ML(**2**,**6**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**2**)).

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 3×d links (for example the links ML(**2**,**1**), ML(**2**,**2**), and ML(**2**,**3**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**1**), and the links ML(**2**,**22**), ML(**2**,**23**), and ML(**2**,**24**) are connected to the middle switch MS(**2**,**1**) from middle switch MS(**1**,**4**)) and also are connected to exactly d switches in middle stage **150** through 3×d links (for example the links ML(**3**,**1**), ML(**3**,**2**), and ML(**3**,**3**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**), and the links ML(**3**,**4**), ML(**3**,**5**), and ML(**3**,**6**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**2**)).

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 3×d links (for example the links ML(**3**,**1**), ML(**3**,**2**), and ML(**3**,**3**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**1**), and the links ML(**3**,**22**), ML(**3**,**23**), and ML(**3**,**24**) are connected to the middle switch MS(**3**,**1**) from middle switch MS(**2**,**4**)) and also are connected to exactly d output switches in output stage **120** through 3×d links (for example the links ML(**4**,**1**), ML(**4**,**2**), and ML(**4**,**3**) are connected to output switch OS**1** from middle switch MS(**3**,**1**), and the links ML(**4**,**4**), ML(**4**,**5**), and ML(**4**,**6**) are connected to output switch OS**2** from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_2}{d}$$

output switches OS**1**-OS**4** are connected from exactly d switches in middle stage **150** through 3×d links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**), ML(**4**,**2**), and ML(**4**,**3**), and output switch OS**1** is also connected from middle switch MS(**3**,**4**) through the links ML(**4**,**22**), ML(**4**,**23**), and ML(**4**,**24**)).

Finally the connection topology of the network **300**C**2** shown in FIG. **3**C**2** is hereinafter called nearest neighbor connection topology.

Similar to network **300**A**2** of FIG. **3**A**2**, **300**B**2** of FIG. **3**B**2**, and **300**C**2** of FIG. **3**C**2**, referring to FIG. **3**D**2**, FIG. **3**E**2**, FIG. **3**F**2**, FIG. **3**G**2**, FIG. **3**H**2**, FIG. **3**I**2** and FIG. **3**J**2** with exemplary asymmetrical multi-link multi-stage networks **300**D**2**, **300**E**2**, **300**F**2**, **300**G**2**, **300**H**2**, **300**I**2**, and **300**J**2** respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, six by eight switches IS**1**-IS**4** and output stage **120** consists of four, six by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, eight by four switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, six by six switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, six by six switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in strictly non-blocking manner for multicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size six by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

The networks **300**D**2**, **300**E**2**, **300**F**2**, **300**G**2**, **300**H**2**, **300**I**2** and **300**J**2** of FIG. **3**D**2**, FIG. **3**E**2**, FIG. **3**F**2**, FIG. **3**G**2**, FIG. **3**H**2**, FIG. **3**I**2**, and FIG. **3**J**2** are also embodiments of asymmetric multi-link multi-stage network can be represented with the notation $V_{mlink}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**24**), d represents the inlet links of each input switch where $N_1>N_2$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Just like networks of **300**A**2**, **300**B**2** and **300**C**2**, for all the networks **300**D**2**, **300**E**2**, **300**F**2**, **300**G**2**, **300**H**2**, **300**I**2** and

300J2 of FIG. **3D2**, FIG. **3E2**, FIG. **3F2**, FIG. **3G2**, FIG. **3H2**, FIG. **3I2**, and FIG. **3J2**, each of the

$$\frac{N_2}{d}$$

input switches IS**1**-IS**4** are connected to exactly

$$\frac{2d+d_1}{3}$$

switches in middle stage **130** through $2d+d_2$ links.

Each of the

$$\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly

$$\frac{2d+d_1}{3}$$

input switches through $2d+d_2$ links and also are connected to exactly d switches in middle stage **140** through 3×d links.

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through 3×d links and also are connected to exactly d switches in middle stage **150** through 3×d links.

Similarly each of the

$$\frac{N_2}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through 3×d links and also are connected to exactly d output switches in output stage **120** through 3×d links.

Each of the

$$\frac{N_2}{d}$$

output switches OS**1**-OS**4** are connected from exactly d switches in middle stage **150** through 3×d links.

In all the ten embodiments of FIG. **3A2** to FIG. **3J2** the connection topology is different. That is the way the links ML(**1**,**1**)-ML(**1**,**48**), ML(**2**,**1**)-ML(**2**,**24**), ML(**3**,**1**)-ML(**3**,**24**), and ML(**4**,**1**)-ML(**4**,**24**) are connected between the respective stages is different. Even though only ten embodiments are illustrated, in general, the network $V_{mlink}(N_1, N_2, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{mlink}(N_1, N_2, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{mlink}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{mlink}(N_1, N_2, d, s)$ can be built. The ten embodiments of FIG. **3A2** to FIG. **3J2** are only three examples of network $V_{mlink}(N_1, N_2, d, s)$.

In all the ten embodiments of FIG. **3A2** to FIG. **3J2**, each of the links ML(**1**,**1**)-ML(**1**,**48**), ML(**2**,**1**)-ML(**2**,**24**), ML(**3**,**1**)-ML(**3**,**24**) and ML(**4**,**1**)-ML(**4**,**24**) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS**1**-IS**4** are also referred to as the network input ports. The input stage **110** is often referred to as the first stage. The output switches OS**1**-OS**4** are also referred to as the network output ports. The output stage **120** is often referred to as the last stage. The middle stage switches MS(**1**,**1**)-MS(**1**,**4**), MS(**2**,**1**)-MS(**2**,**4**), and MS(**3**,**1**)-MS(**3**,**4**) are referred to as middle switches or middle ports.

In the example illustrated in FIG. **3A2** (or in FIG. **3B2** to FIG. **3J2**), a fan-out of four is possible to satisfy a multicast connection request if input switch is IS**2**, but only two switches in middle stage **130** will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS**1**, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage **130** when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network **300A2** (or **300B2** to **300J2**), to be operated in strictly nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage **130** is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage **130**, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the strictly nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Asymmetric SNB ($N_2>N_1$) Embodiments:

Network **3001K2** of FIG. **3K2** is an example of general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2\times\log_d N_2)-1$ stages where $N_1>N_2$ and $N_1=p*N_2$ where p>1. In network **300K2** of FIG. **3K2**, $N_2=N$ and $N_1=p*N$. The general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for multicast when s=3 according to the current invention (and in the example of FIG. **3K2**, s=3). The general asymmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ with $(2\times\log_d N_2)-1$ stages has d_1 (where

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d$$

inlet links for each of

$$\frac{N_2}{d}$$

input switches IS1-IS(N_2/d) (for example the links IL1-IL (p*d) to the input switch IS1) and 2d+d_1 (=2d+p×d) outgoing links for each of

$$\frac{N_2}{d}$$

input switches IS1-IS(N_2/d) (for example the links ML(1,1)-ML(1,(d+p*d)) to the input switch IS1). There are d outlet links for each of

$$\frac{N_2}{d}$$

output switches OS1-OS(N_2/d) (for example the links OL1-OL(d) to the output switch OS1) and 2×d incoming links for each of

$$\frac{N_2}{d}$$

output switches OS1-OS(N_2/d) (for example ML(2×Log_d N_2−2,1)-ML(2×Log_d N_2−2,3×d) to the output switch OS1).

Each of the

$$\frac{N_2}{d}$$

input switches IS1-IS(N_2/d) are connected to exactly

$$\frac{2d+d_1}{3}$$

switches in middle stage **130** through 2d+d_2 links.

Each of the

$$\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,N_2/d) in the middle stage **130** are connected from exactly d input switches through 3×d links and also are connected to exactly d switches in middle stage **140** through 3×d links.

Similarly each of the

$$\frac{N_2}{d}$$

middle switches

$$MS(\text{Log}_d N_2-2)-MS\left(\text{Log}_d N_2-1,\ \frac{N_2}{d}\right)$$

in the middle stage **130**+10*(Log_d N_2−2) are connected from exactly d switches in middle stage **130**+10*(Log_d N_2−3) through 3×d links and also are connected to exactly d switches in middle stage **130**+10*(Log_d N_2−1) through 3×d links.

Similarly each of the

$$\frac{N_2}{d}$$

middle switches

$$MS(\text{Log}_d N_2-3,\ 1)-MS\left(2\times\text{Log}_d N_2-3,\ \frac{N_2}{d}\right)$$

in the middle stage **130**+10*(2*Log_d N_2−4) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N_2−5) through 3×d links and also are connected to exactly d output switches in output stage **120** through 3×d links.

Each of the

$$\frac{N_2}{d}$$

output switches OS1-OS(N_2/d) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N_2−4) through 2×d links.

As described before, again the connection topology of a general $V_{mlink}(N_1, N_2, d, s)$ may be any one of the connection topologies. For example the connection topology of the network $V_{mlink}(N_1, N_2, d, s)$ may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general $V_{mlink}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network $V_{mlink}(N_1, N_2, d, s)$ can be built. The embodiments of FIG. **3A2** to FIG. **3J2** are ten examples of network $V_{mlink}(N_1, N_2, d, s)$ for s=3 and $N_2>N_1$.

The general symmetrical multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for multicast when s≧3 according to the current invention.

For example, the network of FIG. **3C2** shows an exemplary five-stage network, namely V_{mlink}(**8**,**24**,**2**,**3**), with the following multicast assignment $I_1=\{1,4\}$ and all other $I_j=\phi$ for j=[2-8]. It should be noted that the connection I_1 fans out in the first stage switch IS**1** into middle switches MS(**1**,**1**) and MS(**1**,**4**) in middle stage **130**, and fans out in middle switches MS(**1**,**1**) and MS(**1**,**4**) only once into middle switches MS(**2**,**1**) and MS(**2**,**4**) respectively in middle stage **140**.

The connection I_1 also fans out in middle switches MS(**2**,**1**) and MS(**2**,**4**) only once into middle switches MS(**3**,**1**) and MS(**3**,**4**) respectively in middle stage **150**. The connection I_1

also fans out in middle switches MS(**3**,**1**) and MS(**3**,**4**) only once into output switches OS**1** and OS**4** in output stage **120**. Finally the connection I_1 fans out once in the output stage switch OS**1** into outlet link OL**1** and in the output stage switch OS**4** twice into the outlet links OL**7** and OL**8**. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage **130**.

Folded Strictly Nonblocking Multi-link Multi-stage Networks:

The folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$, disclosed in the current invention, is topologically exactly the same as the multi-stage network $V_{mlink}(N_1, N_2, d, s)$, disclosed in U.S. Provisional Patent Application Ser. No. 60/940,392 that is incorporated by reference above, excepting that in the illustrations folded network $V_{fold-mlink}(N_1, N_2, d, s)$ is shown as it is folded at middle stage **130**+10*($\text{Log}_d N_2-2$).

The general symmetrical folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ can also be operated in strictly nonblocking manner for multicast when $s\geqq 3$ according to the current invention. Similarly the general asymmetrical folded multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ can also be operated in strictly nonblocking manner for multicast when $s\geqq 3$ according to the current invention.

Folded Multi-Stage Network Embodiments:

Symmetric Folded RNB Embodiments:

Referring to FIG. **4**A, in one embodiment, an exemplary symmetrical folded multi-stage network **400**A with five stages of thirty two switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by four switches IS**1**-IS**4** and output stage **120** consists of four, four by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of eight, two by two switches MS(**1**,**1**)-MS(**1**,**8**), middle stage **140** consists of eight, two by two switches MS(**2**,**1**)-MS(**2**,**8**), and middle stage **150** consists of eight, two by two switches MS(**3**,**1**)-MS(**3**,**8**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are eight switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are eight switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable N/d, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by

$$2\times\frac{N}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*2d and each output switch OS**1**-OS**4** can be denoted in general with the notation 2d*d. Likewise, the size of each switch in any of the middle stages can be denoted as d*d. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric folded multi-stage network can be represented with the notation $V_{fold}(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL**1**-IL**8** as there are outlet links OL**1**-OL**8**, in a symmetrical network they are the same.

Each of the N/d input switches IS**1**-IS**4** are connected to exactly 2×d switches in middle stage **130** through 2×d links (for example input switch IS**1** is connected to middle switches MS(**1**,**1**), MS(**1**,**2**), MS(**1**,**5**) and MS(**1**,**6**) through the links ML(**1**,**1**), ML(**1**,**2**), ML(**1**,**3**) and ML(**1**,**4**) respectively).

Each of the

$$2\times\frac{N}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**8**) in the middle stage **130** are connected from exactly d input switches through d links (for example the links ML(**1**,**1**) and ML(**1**,**5**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1** and IS**2** respectively) and also are connected to exactly d switches in middle stage **140** through d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**) and MS(**2**,**3**) respectively).

Similarly each of the

$$2\times\frac{N}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**8**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through d links (for example the links ML(**2**,**1**) and ML(**2**,**6**) are connected to the middle switch MS(**2**,**1**) from middle switches MS(**1**,**1**) and MS(**1**,**3**) respectively) and also are connected to exactly d switches in middle stage **150** through d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**) and MS(**3**,**3**) respectively).

Similarly each of the

$$2\times\frac{N}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**8**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through d links (for example the links ML(**3**,**1**) and ML(**3**,**6**) are connected to the middle switch MS(**3**,**1**) from middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively) and also are connected to exactly d output switches in output stage **120** through d links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switches OS**1** and OS**2** respectively from middle switches MS(**3**,**1**)).

Each of the N/d output switches OS**1**-OS**4** are connected from exactly 2×d switches in middle stage **150** through 2×d links (for example output switch OS**1** is connected from middle switches MS(**3**,**1**), MS(**3**,**2**), MS(**3**,**5**) and MS(**3**,**6**) through the links ML(**4**,**1**), ML(**4**,**3**), ML(**4**,**9**) and ML(**4**,**11**) respectively).

Finally the connection topology of the network **400**A shown in FIG. **4**A is known to be back to back inverse Benes connection topology.

Referring to FIG. **4A1**, in another embodiment of network V_{fold}(N, d, s), an exemplary symmetrical folded multi-stage network **400A1** with five stages of thirty two switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by four switches IS**1**-IS**4** and output stage **120** consists of four, four by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of eight, two by two switches MS(**1**,**1**)-MS(**1**,**8**), middle stage **140** consists of eight, two by two switches MS(**2**,**1**)-MS(**2**,**8**), and middle stage **150** consists of eight, two by two switches MS(**3**,**1**)-MS(**3**,**8**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are eight switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size four by two, and there are eight switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable N/d, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by

$$2\times\frac{N}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*2d and each output switch OS**1**-OS**4** can be denoted in general with the notation 2d*d. Likewise, the size of each switch in any of the middle stages can be denoted as d*d. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The symmetric folded multi-stage network of FIG. **4A1** is also the network of the type V_{fold}(N, d, s), where N represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL**1**-IL**8** as there are outlet links OL**1**-OL**8**, in a symmetrical network they are the same.

Each of the N/d input switches IS**1**-IS**4** are connected to exactly 2×d switches in middle stage **130** through 2×d links (for example input switch IS**1** is connected to middle switches MS(**1**,**1**), MS(**1**,**2**), MS(**1**,**5**) and MS(**1**,**6**) through the links ML(**1**,**1**), ML(**1**,**2**), ML(**1**,**3**) and ML(**1**,**4**) respectively).

Each of the

$$2\times\frac{N}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**8**) in the middle stage **130** are connected from exactly d input switches through d links (for example the links ML(**1**,**1**) and ML(**1**,**9**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1** and IS**3** respectively) and also are connected to exactly d switches in middle stage **140** through d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**) and MS(**2**,**2**) respectively).

Similarly each of the

$$2\times\frac{N}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**8**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through d links (for example the links ML(**2**,**1**) and ML(**2**,**5**) are connected to the middle switch MS(**2**,**1**) from middle switches MS(**1**,**1**) and MS(**1**,**3**) respectively) and also are connected to exactly d switches in middle stage **150** through d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**) and MS(**3**,**2**) respectively).

Similarly each of the

$$2\times\frac{N}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**8**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through d links (for example the links ML(**3**,**1**) and ML(**3**,**5**) are connected to the middle switch MS(**3**,**1**) from middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively) and also are connected to exactly d output switches in output stage **120** through d links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switches OS**1** and OS**2** respectively from middle switches MS(**3**,**1**)).

Each of the N/d output switches OS**1**-OS**4** are connected from exactly 2×d switches in middle stage **150** through 2×d links (for example output switch OS**1** is connected from middle switches MS(**3**,**1**), MS(**3**,**3**), MS(**3**,**5**) and MS(**3**,**7**) through the links ML(**4**,**1**), ML(**4**,**5**), ML(**4**,**9**) and ML(**4**,**13**) respectively).

Finally the connection topology of the network **400A1** shown in FIG. **4A1** is known to be back to back Omega connection topology.

Referring to FIG. **4A2**, in another embodiment of network V_{fold}(N, d, s), an exemplary symmetrical folded multi-stage network **400A2** with five stages of thirty two switches for satisfying communication requests, such as setting up a telephone call or

a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by four switches IS**1**-IS**4** and output stage **120** consists of four, four by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of eight, two by two switches MS(**1**,**1**)-MS(**1**,**8**), middle stage

140 consists of eight, two by two switches MS(2,1)-MS(2,8), and middle stage 150 consists of eight, two by two switches MS(3,1)-MS(3,8).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are eight switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size four by two, and there are eight switches in each of middle stage 130, middle stage 140 and middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable N/d, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by

$$2 \times \frac{N}{d}.$$

The size of each input switch IS1-IS4 can be denoted in general with the notation d*2d and each output switch OS1-OS4 can be denoted in general with the notation 2d*d. Likewise, the size of each switch in any of the middle stages can be denoted as d*d. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The symmetric folded multi-stage network of FIG. 4A2 is also the network of the type V_{fold}(N, d, s), where N represents the total number of inlet links of all input switches (for example the links IL1-IL8), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL1-IL8 as there are outlet links OL1-OL8, in a symmetrical network they are the same.

Each of the N/d input switches IS1-IS4 are connected to exactly 2×d switches in middle stage 130 through 2×d links (for example input switch IS1 is connected to middle switches MS(1,1), MS(1,2), MS(1,5) and MS(1,6) through the links ML(1,1), ML(1,2), ML(1,3) and ML(1,4) respectively).

Each of the

$$2 \times \frac{N}{d}$$

middle switches MS(1,1)-MS(1,8) in the middle stage 130 are connected from exactly d input switches through d links (for example the links ML(1,1) and ML(1,14) are connected to the middle switch MS(1,1) from input switch IS1 and IS4 respectively) and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,2) respectively).

Similarly each of the

$$2 \times \frac{N}{d}$$

middle switches MS(2,1)-MS(2,8) in the middle stage 140 are connected from exactly d switches in middle stage 130 through d links (for example the links ML(2,1) and ML(2,8) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,4) respectively) and also are connected to exactly d switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and MS(3,2) respectively).

Similarly each of the

$$2 \times \frac{N}{d}$$

middle switches MS(3,1)-MS(3,8) in the middle stage 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,8) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,4) respectively) and also are connected to exactly d output switches in output stage 120 through d links (for example the links ML(4,1) and ML(4,2) are connected to output switches OS1 and OS2 respectively from middle switches MS(3,1)).

Each of the N/d output switches OS1-OS4 are connected from exactly 2×d switches in middle stage 150 through 2×d links (for example output switch OS1 is connected from middle switches MS(3,1), MS(3,4), MS(3,5) and MS(3,8) through the links ML(4,1), ML(4,2), ML(4,3) and ML(4,4) respectively).

Finally the connection topology of the network 400A2 shown in FIG. 4A2 is hereinafter called nearest neighbor connection topology.

In the three embodiments of FIG. 4A, FIG. 4A1 and FIG. 4A2 the connection topology is different. That is the way the links ML(1,1)-ML(1,16), ML(2,1)-ML(2,16), ML(3,1)-ML(3,16), and ML(4,1)-ML(4,16) are connected between the respective stages is different. Even though only three embodiments are illustrated, in general, the network V_{fold}(N, d, s) can comprise any arbitrary type of connection topology. For example the connection topology of the network V_{fold}(N, d, s) may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the V_{fold}(N, d, s) network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network V_{fold}(N, d, s) can be built. The embodiments of FIG. 4A, FIG. 4A1, and FIG. 4A2 are only three examples of network V_{fold}(N, d, s).

In the three embodiments of FIG. 4A, FIG. 4A1 and FIG. 4A2, each of the links ML(1,1)-ML(1,16), ML(2,1)-ML(2,16), ML(3,1)-ML(3,16) and ML(4,1)-ML(4,16) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS1-IS4 are also referred to as the network input ports. The input stage 110 is often referred to as the first stage. The output switches OS1-OS4 are also referred to as the network output ports. The output stage 120 is often referred to as the last stage. The middle stage switches MS(1,1)-MS(1,8), MS(**2**,**1**)-MS(**2**,**8**), and MS(**3**,**1**)-MS(**3**,**8**) are referred to as middle switches or middle ports.

In the example illustrated in FIG. **4**A (or in FIG. **1**A**1**, or in FIG. **4**A**2**), a fan-out of four is possible to satisfy a multicast connection request if input switch is IS**2**, but only two switches in middle stage **130** will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS**1**, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage **130** when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network **400**A (or **400**A**1**, or **400**A**2**), to be operated in rearrangeably nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage **130** is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage **130**, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the rearrangeably nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Symmetric Folded RNB Embodiments:

Network **400**B of FIG. **4**B is an example of general symmetrical folded multi-stage network V_{fold}(N, d, s) with (2×$\log_d$ N)−1 stages. The general symmetrical folded multi-stage network V_{fold}(N, d, s) can be operated in rearrangeably nonblocking manner for multicast when s≧2 according to the current invention. Also the general symmetrical folded multi-stage network V_{fold}(N, d, s) can be operated in strictly nonblocking manner for unicast if s≧2 according to the current invention. (And in the example of FIG. **4**B, s=2). The general symmetrical folded multi-stage network V_{fold}(N, d, s) with (2×$\log_d$ N)−1 stages has d inlet links for each of N/d input switches IS**1**-IS(N/d) (for example the links IL**1**-IL(d) to the input switch IS**1**) and 2×d outgoing links for each of N/d input switches IS**1**-IS(N/d) (for example the links ML(**1**,**1**)-ML(**1**, 2d) to the input switch IS**1**). There are d outlet links for each of N/d output switches OS**1**-OS(N/d) (for example the links OL**1**-OL(d) to the output switch OS**1**) and 2×d incoming links for each of N/d output switches OS**1**-OS(N/d) (for example ML(2×Log_d N−2,1)-ML(2×Log_d N−2,2×d) to the output switch OS**1**).

Each of the N/d input switches IS**1**-IS(N/d) are connected to exactly 2×d switches in middle stage **130** through 2×d links (for example input switch IS**1** is connected to middle switches MS(**1**,**1**)-MS(1, d) through the links ML(**1**,**1**)-ML(**1**, d) and to middle switches MS(**1**,N/d+1)-MS(**1**,{N/d}+d) through the links ML(**1**, d+1)-ML(**1**,2d) respectively.

Each of the

$$2\times\frac{N}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**2**N/d) in the middle stage **130** are connected from exactly d input switches through d links and also are connected to exactly d switches in middle stage **140** through d links.

Similarly each of the

$$2\times\frac{N}{d}$$

middle switches

$$MS(\text{Log}_d N-1,1)-MS\left(\text{Log}_d N-1,2\times\frac{N}{d}\right)$$

in the middle stage **130**+10*(Log_d N−2) are connected from exactly d switches in middle stage **130**+10*(Log_d N−3) through d links and also are connected to exactly d switches in middle stage **130**+10*(Log_d N−1) through d links.

Similarly each of the

$$2\times\frac{N}{d}$$

middle switches

$$MS(2\times\text{Log}_d N-3,1)-MS\left(2\times\text{Log}_d N-3,2\times\frac{N}{d}\right)$$

in the middle stage **130**+10*(2*Log_d N−4) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N−5) through d links and also are connected to exactly d output switches in output stage **120** through d links.

Each of the N/d output switches OS**1**-OS(N/d) are connected from exactly 2×d switches in middle stage **130**+10*(2*Log_d N−4) through 2×d links.

As described before, again the connection topology of a general V_{fold}(N, d, s) may be any one of the connection topologies. For example the connection topology of the network V_{fold}(N, d, s) may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general V_{fold}(N, d, s) network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network V_{fold}(N, d, s) can be built. The embodiments of FIG. **4**A, FIG. **4**A**1**, and FIG. **4**A**2** are three examples of network V_{fold}(N, d, s).

The general symmetrical folded multi-stage network V_{fold}(N, d, s) can be operated in rearrangeably nonblocking manner for multicast when s≧2 according to the current invention. Also the general symmetrical folded multi-stage network V_{fold}(N, d, s) can be operated in strictly nonblocking manner for unicast if s≧2 according to the current invention.

Every switch in the folded multi-stage networks discussed herein has multicast capability. In a V_{fold}(N, d, s) network, if a network inlet link is to be connected to more than one outlet link on the same output switch, then it is only necessary for the corresponding input switch to have one path to that output switch. This follows because that path can be multicast within the output switch to as many outlet links as necessary. Multicast assignments can therefore be described in terms of connections between input switches and output switches. An existing connection or a new connection from an input switch to r' output switches is said to have fan-out r'. If all multicast assignments of a first type, wherein any inlet link of an input switch is to be connected in an output switch to at most one outlet link are realizable, then multicast assignments of a second type, wherein any inlet link of each input switch is to be connected to more than one outlet link in the same output switch, can also be realized. For this reason, the following discussion is limited to general multicast connections of the first type (with fan-out r',

$$\left(\text{With fan-out } r',\ 1 \le r' \le \frac{N}{d}\right)$$

although the same discussion is applicable to the second type.

To characterize a multicast assignment, for each inlet link

$$i \in \left\{1, 2, \ldots, \frac{N}{d}\right\},$$

let I_i=O, where

$$O \subset \left\{1, 2, \ldots, \frac{N}{d}\right\},$$

denote the subset of output switches to which inlet link i is to be connected in the multicast assignment. For example, the network of FIG. **4**A shows an exemplary five-stage network, namely V_{fold}(**8**,**2**,**2**), with the following multicast assignment I_1={2,3} and all other I_j=φ for j=[2-8]. It should be noted that the connection I_1 fans out in the first stage switch IS**1** into middle switches MS(**1**,**1**) and MS(**1**,**5**) in middle stage **130**, and fans out in middle switches MS(**1**,**1**) and MS(**1**,**5**) only once into middle switches MS(**2**,**1**) and MS(**2**,**5**) respectively in middle stage **140**.

The connection I_1 also fans out in middle switches MS(**2**,**1**) and MS(**2**,**5**) only once into middle switches MS(**3**,**1**) and MS(**3**,**7**) respectively in middle stage **150**. The connection I_1 also fans out in middle switches MS(**3**,**1**) and MS(**3**,**7**) only once into output switches OS**2** and OS**3** in output stage **120**. Finally the connection I_1 fans out once in the output stage switch OS**2** into outlet link OL**3** and in the output stage switch OS**3** twice into the outlet links OL**5** and OL**6**. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage **130**.

Asymmetric Folded RNB (N_2>N_1) Embodiments:

Referring to FIG. **4**C, in one embodiment, an exemplary asymmetrical folded multi-stage network **400**C with five stages of thirty two switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by four switches IS**1**-IS**4** and output stage **120** consists of four, eight by six switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of eight, two by two switches MS(**1**,**1**)-MS(**1**,**8**), middle stage **140** consists of eight, two by two switches MS(**2**,**1**)-MS(**2**,**8**), and middle stage **150** consists of eight, two by four switches MS(**3**,**1**)-MS(**3**,**8**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size two by four, the switches in output

stage **120** are of size eight by six, and there are eight switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size eight by six, and there are eight switches of size two by two in each of middle stage **130** and middle stage **140**, and eight switches of size two by four in middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_1}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and N_2>N_1 and N_2=p*N_1 where p>1. The number of middle switches in each middle stage is denoted by

$$2 \times \frac{N_1}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*2d and each output switch OS**1**-OS**4** can be denoted in general with the notation (d+d_2)*d, where

$$d_2 = N_2 \times \frac{d}{N_1} = p \times d.$$

The size of each switch in any of the middle stages excepting the last middle stage can be denoted as d*d. The size of each switch in the last middle stage can be denoted as

$$d * \frac{(d + d_2)}{2}.$$

A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric folded multi-stage network can be represented with the notation V_{fold}(N_1, N_1, d, s), where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**24**), d represents the inlet links of each input switch where N_2>N_1, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the

$$\frac{N_1}{d}$$

input switches IS**1**-IS**4** are connected to exactly 2×d switches in middle stage **130** through 2×d links (for example input switch IS**1** is connected to middle switches MS(**1**,**1**), MS(**1**, 2), MS(1,5) and MS(1,6) through the links ML(1,1), ML(1,2), ML(1,3) and ML(1,4) respectively).

Each of the

$$2\times\frac{N_1}{d}$$

middle switches MS(1,1)-MS(1,8) in the middle stage 130 are connected from exactly d input switches through d links (for example the links ML(1,1) and ML(1,5) are connected to the middle switch MS(1,1) from input switch IS1 and IS2 respectively) and also are connected to exactly d switches in middle stage 140 through d links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1) and MS(2,3) respectively).

Similarly each of the

$$2\times\frac{N_1}{d}$$

middle switches MS(2,1)-MS(2,8) in the middle stage 140 are connected from exactly d switches in middle stage 130 through d links (for example the links ML(2,1) and ML(2,6) are connected to the middle switch MS(2,1) from middle switches MS(1,1) and MS(1,3) respectively) and also are connected to exactly d switches in middle stage 150 through d links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1) and MS(3,3) respectively).

Similarly each of the

$$2\times\frac{N_1}{d}$$

middle switches MS(3,1)-MS(3,8) in the middle stage 150 are connected from exactly d switches in middle stage 140 through d links (for example the links ML(3,1) and ML(3,6) are connected to the middle switch MS(3,1) from middle switches MS(2,1) and MS(2,3) respectively) and also are connected to exactly

$$\frac{d+d_2}{2}$$

output switches in output stage 120 through

$$\frac{d+d_2}{2}$$

links (for example the links ML(4,1), ML(4,2), ML(4,3) and ML(4,4) are connected to output switches OS1, OS2, OS3, and OS4 respectively from middle switches MS(3,1)).

Each of the

$$\frac{N_1}{d}$$

output switches OS1-OS4 are connected from exactly $d+d_2$ switches in middle stage 150 through $d+d_2$ links (for example output switch OS1 is connected from middle switches MS(3,1), MS(3,2), MS(3,3), MS(3,4), MS(3,5), MS(3,6), MS(3,7), and MS(3,8) through the links ML(4,1), ML(4,5), ML(4,9), ML(4,13), ML(4,17), ML(4,21), ML(4,25) and ML(4,29) respectively).

Finally the connection topology of the network 400C shown in FIG. 4C is known to be back to back inverse Benes connection topology.

Referring to FIG. 4C1, in another embodiment of network $V_{fold}(N_1, N_2, d, s)$, an exemplary asymmetrical folded multi-stage network 400C1 with five stages of thirty two switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, two by four switches IS1-IS4 and output stage 120 consists of four, eight by six switches OS1-OS4. And all the middle stages namely middle stage 130 consists of eight, two by two switches MS(1,1)-MS(1,8), middle stage 140 consists of eight, two by two switches MS(2,1)-MS(2,8), and middle stage 150 consists of eight, two by four switches MS(3,1)-MS(3,8).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size eight by six, and there are eight switches in each of middle stage 130, middle stage 140 and middle stage 150. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage 110 are of size two by four, the switches in output stage 120 are of size eight by six, and there are eight switches of size two by two in each of middle stage 130 and middle stage 140, and eight switches of size two by four in middle stage 150.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable

$$\frac{N_1}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_2>N_1$ and $N_2=p*N_1$ where p>1. The number of middle switches in each middle stage is denoted by

$$2\times\frac{N_1}{d}.$$

The size of each input switch IS1-IS4 can be denoted in general with the notation d*2d and each output switch OS1-OS4 can be denoted in general with the notation $(d+d_2)*d$, where

$$d_2 = N_2\times\frac{d}{N_1} = p\times d.$$

The size of each switch in any of the middle stages excepting the last middle stage can be denoted as d*d. The size of each switch in the last middle stage can be denoted as

$$d*\frac{(d+d_2)}{2}.$$

A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The asymmetric folded multi-stage network of FIG. 4C1 is also the network of the type $V_{fold}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**24**), d represents the inlet links of each input switch where $N_2>N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the

$$\frac{N_1}{d}$$

input switches IS**1**-IS**4** are connected to exactly 2×d switches in middle stage **130** through 2×d links (for example input switch IS**1** is connected to middle switches MS(**1**,**1**), MS(**1**,**2**), MS(**1**,**5**) and MS(**1**,**6**) through the links ML(**1**,**1**), ML(**1**,**2**), ML(**1**,**3**) and ML(**1**,**4**) respectively).

Each of the

$$2\times\frac{N_1}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**8**) in the middle stage **130** are connected from exactly d input switches through d links (for example the links ML(**1**,**1**) and ML(**1**,**9**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1** and IS**3** respectively) and also are connected to exactly d switches in middle stage **140** through d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**) and MS(**2**,**2**) respectively).

Similarly each of the

$$2\times\frac{N_1}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**8**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through d links (for example the links ML(**2**,**1**) and ML(**2**,**5**) are connected to the middle switch MS(**2**,**1**) from middle switches MS(**1**,**1**) and MS(**1**,**3**) respectively) and also are connected to exactly d switches in middle stage **150** through d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**) and MS(**3**,**2**) respectively).

Similarly each of the

$$2\times\frac{N_1}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**8**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through d links (for example the links ML(**3**,**1**) and ML(**3**,**5**) are connected to the middle switch MS(**3**,**1**) from middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively) and also are connected to exactly

$$\frac{d+d_2}{2}$$

output switches in output stage **120** through

$$\frac{d+d_2}{2}$$

links (for example the links ML(**4**,**1**), ML(**4**,**2**), ML(**4**,**3**) and ML(**4**,**4**) are connected to output switches OS**1**, OS**2**, OS**3**, and OS**4** respectively from middle switches MS(**3**,**1**)).

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS**4** are connected from exactly $d+d_2$ switches in middle stage **150** through $d+d_2$ links (for example output switch OS**1** is connected from middle switches MS(**3**,**1**), MS(**3**,**2**), MS(**3**,**3**), MS(**3**,**4**), MS(**3**,**5**), MS(**3**,**6**), MS(**3**,**7**), and MS(**3**,**8**) through the links ML(**4**,**1**), ML(**4**,**5**), ML(**4**,**9**), ML(**4**,**13**), ML(**4**,**17**), ML(**4**,**21**), ML(**4**,**25**) and ML(**4**,**29**) respectively).

Finally the connection topology of the network **400C1** shown in FIG. **4C1** is known to be back to back Omega connection topology.

Referring to FIG. **4C2**, in another embodiment of network $V_{fold}(N_1, N_2, d, s)$, an exemplary asymmetrical folded multi-stage network **400C2** with five stages of thirty two switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by four switches IS**1**-IS**4** and output stage **120** consists of four, eight by six switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of eight, two by two switches MS(**1**,**1**)-MS(**1**,**8**), middle stage **140** consists of eight, two by two switches MS(**2**,**1**)-MS(**2**,**8**), and middle stage **150** consists of eight, two by four switches MS(**3**,**1**)-MS(**3**,**8**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size eight by six, and there are eight switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size two by four, the switches in output stage **120** are of size eight by six, and there are eight switches of size two by two in each of middle stage **130** and middle stage **140**, and eight switches of size two by four in middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_1}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_2>N_1$ and $N_2=p*N_1$ where $p>1$. The number of middle switches in each middle stage is denoted by

$$2\times\frac{N_1}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*2d and each output switch OS**1**-

OS4 can be denoted in general with the notation $(d+d_2)*d$, where

$$d_2 = N_2 \times \frac{d}{N_1} = p \times d.$$

The size of each switch in any of the middle stages excepting the last middle stage can be denoted as d*d. The size of each switch in the last middle stage can be denoted as

$$d * \frac{(d+d_2)}{2}.$$

A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The asymmetric folded multi-stage network of FIG. **4C2** is also the network of the type $V_{fold}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**24**), d represents the inlet links of each input switch where $N_2>N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the

$$\frac{N_1}{d}$$

input switches IS**1**-IS**4** are connected to exactly 2×d switches in middle stage **130** through 2×d links (for example input switch IS**1** is connected to middle switches MS(**1**,**1**), MS(**1**,**2**), MS(**1**,**5**) and MS(**1**,**6**) through the links ML(**1**,**1**), ML(**1**,**2**), ML(**1**,**3**) and ML(**1**,**4**) respectively).

Each of the

$$2 \times \frac{N_1}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**8**) in the middle stage **130** are connected from exactly d input switches through d links (for example the links ML(**1**,**1**) and ML(**1**,**14**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1** and IS**4** respectively) and also are connected to exactly d switches in middle stage **140** through d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**) and MS(**2**,**2**) respectively).

Similarly each of the

$$2 \times \frac{N_1}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**8**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through d links (for example the links ML(**2**,**1**) and ML(**2**,**8**) are connected to the middle switch MS(**2**,**1**) from middle switches MS(**1**,**1**) and MS(**1**,**4**) respectively) and also are connected to exactly d switches in middle stage **150** through d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**) and MS(**3**,**2**) respectively).

Similarly each of the

$$2 \times \frac{N_1}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**8**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through d links (for example the links ML(**3**,**1**) and ML(**3**,**8**) are connected to the middle switch MS(**3**,**1**) from middle switches MS(**2**,**1**) and MS(**2**,**4**) respectively) and also are connected to exactly

$$\frac{d+d_2}{2}$$

output switches in output stage **120** through

$$\frac{d+d_2}{2}$$

links (for example the links ML(**4**,**1**), ML(**4**,**2**), ML(**4**,**3**) and ML(**4**,**4**) are connected to output switches OS**1**, OS**2**, OS**3**, and OS**4** respectively from middle switches MS(**3**,**1**)).

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS**4** are connected from exactly $d+d_2$ switches in middle stage **150** through $d+d_1$ links (for example output switch OS**1** is connected from middle switches MS(**3**,**1**), MS(**3**,**2**), MS(**3**,**3**), MS(**3**,**4**), MS(**3**,**5**), MS(**3**,**6**), MS(**3**,**7**), and MS(**3**,**8**) through the links ML(**4**,**1**), ML(**4**,**5**), ML(**4**,**9**), ML(**4**,**13**), ML(**4**,**17**), ML(**4**,**21**), ML(**4**,**25**) and ML(**4**,**29**) respectively).

Finally the connection topology of the network **400C2** shown in FIG. **4C2** is hereinafter called nearest neighbor connection topology.

In the three embodiments of FIG. **4C**, FIG. **4C1** and FIG. **4C2** the connection topology is different. That is the way the links ML(**1**,**1**)-ML(**1**,**16**), ML(**2**,**1**)-ML(**2**,**16**), ML(**3**,**1**)-ML(**3**,**16**), and ML(**4**,**1**)-ML(**4**,**16**) are connected between the respective stages is different. Even though only three embodiments are illustrated, in general, the network $V_{fold}(N_1, N_2, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{fold}(N_1, N_2, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{fold}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{fold}(N_1, N_2, d, s)$ can be built. The embodiments of FIG. **4C**, FIG. **4C1**, and FIG. **4C2** are only three examples of network $V_{fold}(N_1, N_2, d, s)$.

In the three embodiments of FIG. **4C**, FIG. **4C1** and FIG. **4C2**, each of the links ML(**1**,**1**)-ML(**1**,**32**), ML(**2**,**1**)-ML(**2**,**16**), ML(**3**,**1**)-ML(**3**,**16**) and ML(**4**,**1**)-ML(**4**,**16**) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS1-IS4 are also referred to as the network input ports. The input stage **110** is often referred to as the first stage. The output switches OS1-OS4 are also referred to as the network output ports. The output stage **120** is often referred to as the last stage. The middle stage switches MS(**1**,**1**)-MS(**1**,**8**), MS(**2**,**1**)-MS(**2**,**8**), and MS(**3**,**1**)-MS(**3**,**8**) are referred to as middle switches or middle ports.

In the example illustrated in FIG. **4**C (or in FIG. **1**C**1**, or in FIG. **4**C**2**), a fan-out of four is possible to satisfy a multicast connection request if input switch is IS**2**, but only two switches in middle stage **130** will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS**1**, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage **130** when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network **400**C (or **400**C**1**, or **400**C**2**), to be operated in rearrangeably nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage **130** is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage **130**, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the rearrangeably nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Asymmetric Folded RNB ($N_2>N_1$) Embodiments:

Network **400**D of FIG. **4**D is an example of general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ with $(2\times\log_d N_1)-1$ stages where $N_2>N_1$ and $N_2=p*N_1$ where $p>1$. In network **400**D of FIG. **4**D, $N_1=N$ and $N_2=p*N$. The general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s\geqq 2$ according to the current invention. Also the general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if $s\geqq 2$ according to the current invention. (And in the example of FIG. **4**D, s=2). The general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ with $(2\times\log_d N_1)-1$ stages has d inlet links for each of

$$\frac{N_1}{d}$$

input switches IS**1**-IS(N_1/d) (for example the links IL**1**-IL(d) to the input switch IS**1**) and 2×d outgoing links for each of

$$\frac{N_1}{d}$$

input switches IS**1**-IS(N_1/d) (for example the links ML(**1**,**1**)-ML(**1**,2d) to the input switch IS**1**). There are d_2 (where

$$\left(\text{where } d_2 = N_2\times\frac{d}{N_1} = p\times d\right)$$

outlet links for each of

$$\frac{N_1}{d}$$

output switches OS**1**-OS(N_1/d) (for example the links OL**1**-OL(p*d) to the output switch OS**1**) and $d+d_2$ (=d+p×d) incoming links for each of

$$\frac{N_1}{d}$$

output switches OS**1**-OS(N_1/d) (for example ML($2\times\text{Log}_d N_1-2$,1)-ML($2\times\text{Log}_d N_1-2$, $d+d_2$) to the output switch OS**1**).

Each of the

$$\frac{N_1}{d}$$

input switches IS**1**-IS(N_1/d) are connected to exactly 2×d switches in middle stage **130** through 2×d links (for example in one embodiment the input switch IS**1** is connected to middle switches MS(**1**,**1**)-MS(1, d) through the links ML(**1**, **1**)-ML(1, d) and to middle switches MS(**1**,N_1/d+1)-MS(**1**, {N_1/d}+d) through the links ML(**1**, d+1)-ML(**1**,2d) respectively.

Each of the

$$2\times\frac{N_1}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,2N_1/d) in the middle stage **130** are connected from exactly d input switches through d links and also are connected to exactly d switches in middle stage **140** through d links.

Similarly each of the

$$MS(\text{Log}_d N_1-1,1)-MS\left(\text{Log}_d N_1-1,2\times\frac{N_1}{d}\right)$$

middle switches

$$2\times\frac{N_1}{d}$$

in the middle stage **130**+10*($\text{Log}_d N_1-2$) are connected from exactly d switches in middle stage **130**+10*($\text{Log}_d N_1-3$) through d links and also are connected to exactly d switches in middle stage **130**+10*($\text{Log}_d N_1-1$) through d links.

Similarly each of the

$$2\times\frac{N_1}{d}$$

middle switches

$$MS(2\times \text{Log}_d N_1-3,1)-MS\left(2\times \text{Log}_d N_1-3,2\times\frac{N_1}{d}\right)$$

in the middle stage 130+10*(2*Log$_d$ N$_1$−4) are connected from exactly d switches in middle stage 130+10*(2*Log$_d$ N$_1$−5) through d links and also are connected to exactly d output switches in output stage **120** through d links.

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS(N_1/d) are connected from exactly d+d_2 switches in middle stage **130**+10*(2*Log$_d$ N$_1$−4) through d+d_1 links.

As described before, again the connection topology of a general $V_{fold}(N_1, N_2, d, s)$ may be any one of the connection topologies. For example the connection topology of the network $V_{fold}(N_1, N_2, d, s)$ may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general $V_{fold}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network $V_{fold}(N_1, N_2, d, s)$ can be built. The embodiments of FIG. **4**C, FIG. **4C1**, and FIG. **4C2** are three examples of network $V_{fold}(N_1, N_2, d, s)$ for s=2 and $N_2>N_1$.

The general symmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when s≧2 according to the current invention. Also the general symmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in strictly non-blocking manner for unicast if s≧2 according to the current invention.

For example, the network of FIG. **4**C shows an exemplary five-stage network, namely V_{fold}(**8**,**24**,**2**,**2**), with the following multicast assignment I_1={2,3} and all other I_j=ϕ for j=[2-8]. It should be noted that the connection I_1 fans out in the first stage switch IS**1** into middle switches MS(**1**,**1**) and MS(**1**,**5**) in middle stage **130**, and fans out in middle switches MS(**1**,**1**) and MS(**1**,**5**) only once into middle switches MS(**2**,**1**) and MS(**2**,**5**) respectively in middle stage **140**.

The connection I_1 also fans out in middle switches MS(**2**,**1**) and MS(**2**,**5**) only once into middle switches MS(**3**,**1**) and MS(**3**,**7**) respectively in middle stage **150**. The connection I_1 also fans out in middle switches MS(**3**,**1**) and MS(**3**,**7**) only once into output switches OS**2** and OS**3** in output stage **120**. Finally the connection I_1 fans out once in the output stage switch OS**2** into outlet link OL**7** and in the output stage switch OS**3** twice into the outlet links OL**13** and OL**16**. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage **130**.

Asymmetric Folded RNB ($N_1>N_2$) Embodiments:

Referring to FIG. **4**E, in one embodiment, an exemplary asymmetrical folded multi-stage network **400**E with five stages of thirty two switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, six by eight switches IS**1**-IS**4** and output stage **120** consists of four, four by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of eight, four by two switches MS(**1**,**1**)-MS(**1**,**8**), middle stage **140** consists of eight, two by two switches MS(**2**,**1**)-MS(**2**,**8**), and middle stage **150** consists of eight, two by two switches MS(**3**,**1**)-MS(**3**,**8**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size four by two, and there are eight switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size four by two, and there are eight switches of size four by two in middle stage **130**, and eight switches of size two by two in middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_2}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1>N_2$ and N_1=p*N_2 where p>1. The number of middle switches in each middle stage is denoted by

$$2\times\frac{N_2}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*(d+d_1) and each output switch OS**1**-OS**4** can be denoted in general with the notation (2×d*d), where

$$d_1 = N_1\times\frac{d}{N_2} = p\times d.$$

The size of each switch in any of the middle stages excepting the first middle stage can be denoted as d*d. The size of each switch in the first middle stage can be denoted as

$$\frac{(d+d_1)}{2}*d.$$

A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric folded multi-stage network can be represented with the notation $V_{fold}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**24**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**8**), d represents the inlet links of each input switch where $N_1>N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the

$$\frac{N_2}{d}$$

input switches IS**1**-IS**4** are connected to exactly $d+d_1$ switches in middle stage **130** through $d+d_1$ links (for example input switch IS**1** is connected to middle switches MS(**1**,**1**), MS(**1**,**2**), MS(**1**,**3**), MS(**1**,**4**), MS(**1**,**5**), MS(**1**,**6**), MS(**1**,**7**), and MS(**1**,**8**) through the links ML(**1**,**1**), ML(**1**,**2**), ML(**1**,**3**), ML(**1**,**4**), ML(**1**,**5**), ML(**1**,**6**), ML(**1**,**7**), and ML(**1**,**8**) respectively).

Each of the

$$2\times\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**8**) in the middle stage **130** are connected from exactly

$$\frac{(d+d_1)}{2}$$

input switches through

$$\frac{(d+d_1)}{2}$$

links (for example the links ML(**1**,**1**), ML(**1**,**9**), ML(**1**,**17**) and ML(**1**,**25**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**, IS**2**, IS**3**, and IS**4** respectively) and also are connected to exactly d switches in middle stage **140** through d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**) and MS(**2**,**3**) respectively).

Similarly each of the

$$2\times\frac{N_2}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**8**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through d links (for example the links ML(**2**,**1**) and ML(**2**,**6**) are connected to the middle switch MS(**2**,**1**) from middle switches MS(**1**,**1**) and MS(**1**,**3**) respectively) and also are connected to exactly d switches in middle stage **150** through d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**) and MS(**3**,**3**) respectively).

Similarly each of the

$$2\times\frac{N_2}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**8**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through d links (for example the links ML(**3**,**1**) and ML(**3**,**6**) are connected to the middle switch MS(**3**,**1**) from middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively) and also are connected to exactly d output switches in output stage **120** through d links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switches OS**1** and OS**2** respectively from middle switches MS(**3**,**1**)).

Each of the

$$\frac{N_2}{d}$$

output switches OS**1**-OS**4** are connected from exactly 2×d switches in middle stage **150** through 2×d links (for example output switch OS**1** is connected from middle switches MS(**3**,**1**), MS(**3**,**2**), MS(**3**,**5**), and MS(**3**,**6**) through the links ML(**4**,**1**), ML(**4**,**3**), ML(**4**,**9**), and ML(**4**,**11**) respectively).

Finally the connection topology of the network **400**E shown in FIG. **4**E is known to be back to back inverse Benes connection topology.

Referring to FIG. **4**E**1**, in another embodiment of network $V_{fold}(N_1, N_2, d, s)$, an exemplary asymmetrical folded multi-stage network **400**E**1** with five stages of thirty two switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, six by eight switches IS**1**-IS**4** and output stage **120** consists of four, four by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of eight, four by two switches MS(**1**,**1**)-MS(**1**,**8**), middle stage **140** consists of eight, two by two switches MS(**2**,**1**)-MS(**2**,**8**), and middle stage **150** consists of eight, two by two switches MS(**3**,**1**)-MS(**3**,**8**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size four by two, and there are eight switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size four by two, and there are eight switches of size four by two in middle stage **130**, and eight switches of size two by two in middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_2}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1>N_2$ and $N_1=p*N_2$ where $p>1$.

The number of middle switches in each middle stage is denoted by

$$2\times\frac{N_2}{d}.$$

The size of each input switch IS1-IS4 can be denoted in general with the notation d*(d+d_1) and each output switch OS1-OS4 can be denoted in general with the notation (2×d*d), where

$$d_1 = N_1\times\frac{d}{N_2} = p\times d.$$

The size of each switch in any of the middle stages excepting the first middle stage can be denoted as d*d. The size of each switch in the first middle stage can be denoted as

$$\frac{(d+d_1)}{2}*d.$$

A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The asymmetric folded multi-stage network of FIG. **4**E**1** is also the network of the type $V_{fold}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**24**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**8**), d represents the inlet links of each input switch where $N_1>N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the

$$\frac{N_2}{d}$$

input switches IS**1**-IS**4** are connected to exactly d+d_1 switches in middle stage **130** through d+d_1 links (for example input switch IS**1** is connected to middle switches MS(**1**,**1**), MS(**1**,**2**), MS(**1**,**3**), MS(**1**,**4**), MS(**1**,**5**), MS(**1**,**6**), MS(**1**,**7**), and MS(**1**,**8**) through the links ML(**1**,**1**), ML(**1**,**2**), ML(**1**,**3**), ML(**1**,**4**), ML(**1**,**5**), ML(**1**,**6**), ML(**1**,**7**), and ML(**1**,**8**) respectively).

Each of the

$$2\times\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**8**) in the middle stage **130** are connected from exactly

$$\frac{(d+d_1)}{2}$$

input switches through

$$\frac{(d+d_1)}{2}$$

links (for example the links ML(**1**,**1**), ML(**1**,**9**), ML(**1**,**17**) and ML(**1**,**25**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**, IS**2**, IS**3**, and IS**4** respectively) and also are connected to exactly d switches in middle stage **140** through d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**) and MS(**2**,**2**) respectively).

Similarly each of the

$$2\times\frac{N_2}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**8**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through d links (for example the links ML(**2**,**1**) and ML(**2**,**5**) are connected to the middle switch MS(**2**,**1**) from middle switches MS(**1**,**1**) and MS(**1**,**3**) respectively) and also are connected to exactly d switches in middle stage **150** through d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**) and MS(**3**,**2**) respectively).

Similarly each of the

$$2\times\frac{N_2}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**8**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through d links (for example the links ML(**3**,**1**) and ML(**3**,**5**) are connected to the middle switch MS(**3**,**1**) from middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively) and also are connected to exactly d output switches in output stage **120** through d links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switches OS**1** and OS**2** respectively from middle switches MS(**3**,**1**)).

Each of the

$$\frac{N_2}{d}$$

output switches OS**1**-OS**4** are connected from exactly 2×d switches in middle stage **150** through 2×d links (for example output switch OS**1** is connected from middle switches MS(**3**,**1**), MS(**3**,**3**), MS(**3**,**5**), and MS(**3**,**7**) through the links ML(**4**,**1**), ML(**4**,**5**), ML(**4**,**9**), and ML(**4**,**13**) respectively).

Finally the connection topology of the network **400**E**1** shown in FIG. **4**E**1** is known to be back to back Omega connection topology.

Referring to FIG. **4**E**2**, in another embodiment of network $V_{fold}(N_1, N_2, d, s)$, an exemplary asymmetrical folded multi-stage network **400**E**2** with five stages of thirty two switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, six by eight switches IS**1**-IS**4** and output stage **120** consists of four, four by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of eight, four by two switches MS(**1**,**1**)-MS(**1**,**8**), middle stage **140** consists of eight, two by two switches MS(**2**,**1**)-MS(**2**,**8**), and middle stage **150** consists of eight, two by two switches MS(**3**,**1**)-MS(**3**,**8**).

Such a network can be operated in strictly non-blocking manner for unicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size four by two, and there are eight switches in each of middle stage **130**, middle stage **140** and middle stage **150**. Such a network can be operated in rearrangeably non-blocking manner for multicast connections, because the switches in the input stage **110** are of size six by eight, the switches in output stage **120** are of size four by two, and there are eight switches of size four by two in middle stage **130**, and eight switches of size two by two in middle stage **140** and middle stage **150**.

In one embodiment of this network each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_2}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1>N_2$ and $N_1=p*N_2$ where p>1. The number of middle switches in each middle stage is denoted by

$$2\times\frac{N_2}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation $d*(d+d_1)$ and each output switch OS**1**-OS**4** can be denoted in general with the notation (2×d*d), where

$$d_1 = N_1\times\frac{d}{N_2} = p\times d.$$

The size of each switch in any of the middle stages excepting the first middle stage can be denoted as d*d. The size of each switch in the first middle stage can be denoted as

$$\frac{(d+d_1)}{2}*d.$$

A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. The asymmetric folded multi-stage network of FIG. **4**E**1** is also the network of the type $V_{fold}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**24**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**8**), d represents the inlet links of each input switch where $N_1>N_2$, and s is the ratio of number of incoming links to each output switch to the outlet links of each output switch.

Each of the

$$\frac{N_2}{d}$$

input switches IS**1**-IS**4** are connected to exactly $d+d_1$ switches in middle stage **130** through $d+d_1$ links (for example input switch IS**1** is connected to middle switches MS(**1**,**1**), MS(**1**,**2**), MS(**1**,**3**), MS(**1**,**4**), MS(**1**,**5**), MS(**1**,**6**), MS(**1**,**7**), and MS(**1**,**8**) through the links ML(**1**,**1**), ML(**1**,**2**), ML(**1**,**3**), ML(**1**,**4**), ML(**1**,**5**), ML(**1**,**6**), ML(**1**,**7**), and ML(**1**,**8**) respectively).

Each of the

$$2\times\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**8**) in the middle stage **130** are connected from exactly

$$\frac{(d+d_1)}{2}$$

input switches through

$$\frac{(d+d_1)}{2}$$

links (for example the links ML(**1**,**1**), ML(**1**,**9**), ML(**1**,**17**) and ML(**1**,**25**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**, IS**2**, IS**3**, and IS**4** respectively) and also are connected to exactly d switches in middle stage **140** through d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**) and MS(**2**,**2**) respectively).

Similarly each of the

$$2\times\frac{N_2}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**8**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through d links (for example the links ML(**2**,**1**) and ML(**2**,**8**) are connected to the middle switch MS(**2**,**1**) from middle switches MS(**1**,**1**) and MS(**1**,**4**) respectively) and also are connected to exactly d switches in middle stage **150** through d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**) and MS(**3**,**2**) respectively).

Similarly each of the

$$2\times\frac{N_2}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**8**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through d links (for example the links ML(**3**,**1**) and ML(**3**,**8**) are connected to the middle switch MS(**3**,**1**) from middle switches MS(**2**,**1**) and MS(**2**,**4**) respectively) and also are connected to exactly d output switches in output stage **120** through d links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switches OS**1** and OS**2** respectively from middle switches MS(**3**,**1**)).

Each of the

$$\frac{N_2}{d}$$

output switches OS**1**-OS**4** are connected from exactly 2×d switches in middle stage **150** through 2×d links (for example output switch OS**1** is connected from middle switches MS(**3**,**1**), MS(**3**,**4**), MS(**3**,**5**), and MS(**3**,**8**) through the links ML(**4**,**1**), ML(**4**,**8**), ML(**4**,**9**), and ML(**4**,**16**) respectively).

Finally the connection topology of the network **400**E**2** shown in FIG. **4**E**2** is hereinafter called nearest neighbor connection topology.

In the three embodiments of FIG. **4**E, FIG. **4**E**1** and FIG. **4**E**2** the connection topology is different. That is the way the links ML(**1**,**1**)-ML(**1**,**32**), ML(**2**,**1**)-ML(**2**,**16**), ML(**3**,**1**)-ML(**3**,**16**), and ML(**4**,**1**)-ML(**4**,**16**) are connected between the respective stages is different. Even though only three embodiments are illustrated, in general, the network $V_{fold}(N_1, N_2, d, s)$ can comprise any arbitrary type of connection topology. For example the connection topology of the network $V_{fold}(N_1, N_2, d, s)$ may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the $V_{fold}(N_1, N_2, d, s)$ network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network $V_{fold}(N_1, N_2, d, s)$ can be built. The embodiments of FIG. **4**E, FIG. **4**E**1**, and FIG. **4**E**2** are only three examples of network $V_{fold}(N_1, N_2, d, s)$.

In the three embodiments of FIG. **4**E, FIG. **4**E**1** and FIG. **4**E**2**, each of the links ML(**1**,**1**)-ML(**1**,**32**), ML(**2**,**1**)-ML(**2**,**16**), ML(**3**,**1**)-ML(**3**,**16**) and ML(**4**,**1**)-ML(**4**,**16**) are either available for use by a new connection or not available if currently used by an existing connection. The input switches IS**1**-IS**4** are also referred to as the network input ports. The input stage **110** is often referred to as the first stage. The output switches OS**1**-OS**4** are also referred to as the network output ports. The output stage **120** is often referred to as the last stage. The middle stage switches MS(**1**,**1**)-MS(**1**,**8**), MS(**2**,**1**)-MS(**2**,**8**), and MS(**3**,**1**)-MS(**3**,**8**) are referred to as middle switches or middle ports.

In the example illustrated in FIG. **4**E (or in FIG. **1**E**1**, or in FIG. **4**E**2**), a fan-out of four is possible to satisfy a multicast connection request if input switch is IS**2**, but only two switches in middle stage **130** will be used. Similarly, although a fan-out of three is possible for a multicast connection request if the input switch is IS**1**, again only a fan-out of two is used. The specific middle switches that are chosen in middle stage **130** when selecting a fan-out of two is irrelevant so long as at most two middle switches are selected to ensure that the connection request is satisfied. In essence, limiting the fan-out from input switch to no more than two middle switches permits the network **400**E (or **400**E**1**, or **400**E**2**), to be operated in rearrangeably nonblocking manner in accordance with the invention.

The connection request of the type described above can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, a fan-out of one is used, i.e. a single middle stage switch in middle stage **130** is used to satisfy the request. Moreover, although in the above-described embodiment a limit of two has been placed on the fan-out into the middle stage switches in middle stage **130**, the limit can be greater depending on the number of middle stage switches in a network (while maintaining the rearrangeably nonblocking nature of operation of the network for multicast connections). However any arbitrary fan-out may be used within any of the middle stage switches and the output stage switches to satisfy the connection request.

Generalized Asymmetric Folded RNB ($N_1>N_2$) Embodiments:

Network **400**F of FIG. **4**F is an example of general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ with $(2\times\log_d N_2)-1$ stages where $N_1>N_2$ and $N_1=p*N_2$ where $p>1$. In network **400**D of FIG. **4**F, $N_2=N$ and $N_1=p*N$. The general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for multicast when $s\geqq 2$ according to the current invention. Also the general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in strictly nonblocking manner for unicast if $s\geqq 2$ according to the current invention. (And in the example of FIG. **4**F, s=2). The general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ with $(2\times\log_d N_2)-1$ stages has d_1 (where

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d$$

inlet links for each of

$$\frac{N_2}{d}$$

input switches IS**1**-IS(N_2/d) (for example the links IL**1**-IL(p*d) to the input switch IS**1**) and $d+d_1$ (=d+p×d) outgoing links for each of

$$\frac{N_2}{d}$$

input switches IS**1**-IS(N_2/d) (for example the links ML(**1**,**1**)-ML(**1**,(d+p*d)) to the input switch IS**1**). There are d outlet links for each of

$$\frac{N_2}{d}$$

output switches OS**1**-OS(N_2/d) (for example the links OL**1**-OL(d) to the output switch OS**1**) and 2×d incoming links for each of

$$\frac{N_2}{d}$$

output switches OS**1**-OS(N_2/d) (for example ML($2\times\text{Log}_d N_2-2$,1)-ML($2\times\text{Log}_d N_2-2$,2×d) to the output switch OS**1**).

Each of the

$$\frac{N_2}{d}$$

input switches IS1-IS(N_2/d) are connected to exactly d+d_1 switches in middle stage **130** through d+d_1 links (for example in one embodiment the input switch IS**1** is connected to middle switches MS(**1**,**1**)-MS(**1**, (d+d_1)/2) through the links ML(**1**,**1**)-ML(**1**,(d+d_1)/2) and to middle switches MS(**1**,N_1/d+1)-MS(**1**,{N_1/d}+(d+d_1)/2) through the links ML(**1**, ((d+d_1)/2)+1)-ML(**1**, (d+d_1)) respectively.

Each of the

$$2\times\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,2*N_2/d) in the middle stage **130** are connected from exactly d input switches through d links and also are connected to exactly d switches in middle stage **140** through d links.

Similarly each of the

$$2\times\frac{N_2}{d}$$

middle switches

$$MS(\text{Log}_d N_2-1,\,1)-MS\left(\text{Log}_d N_2-1,\,2\times\frac{N_2}{d}\right)$$

in the middle stage **130**+10*(Log_d N_2−2) are connected from exactly d switches in middle stage **130**+10*(Log_d N_2−3) through d links and also are connected to exactly d switches in middle stage **130**+10*(Log_d N_2−1) through d links.

Similarly each of the

$$2\times\frac{N_2}{d}$$

middle switches

$$MS(2\times\text{Log}_d N_2-3,\,1)-MS\left(2\times\text{Log}_d N_2-3,\,2\times\frac{N_2}{d}\right)$$

in the middle stage **130**+10*(2*Log_d N_2−4) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N_2−5) through d links and also are connected to exactly d output switches in output stage **120** through d links.

Each of the

$$\frac{N_2}{d}$$

output switches OS**1**-OS(N_2/d) are connected from exactly 2×d switches in middle stage **130**+10*(2*Log_d N_2−4) through 2×d links.

As described before, again the connection topology of a general V_{fold}(N_1, N_2, d, s) may be any one of the connection topologies. For example the connection topology of the network V_{fold}(N_1, N_2, d, s) may be back to back inverse Benes networks, back to back Omega networks, back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the general V_{fold}(N_1, N_2, d, s) network is, when no connections are setup from any input link if any output link should be reachable. Based on this property numerous embodiments of the network V_{fold}(N_1, N_2, d, s) can be built. The embodiments of FIG. **4**E, FIG. **4**E**1**, and FIG. **4**E**2** are three examples of network V_{fold}(N_1, N_2, d, s) for s=2 and N_1>N_2.

The general symmetrical folded multi-stage network V_{fold} (N_1, N_2, d, s) can be operated in rearrangeably nonblocking manner for multicast when s≧2 according to the current invention. Also the general symmetrical folded multi-stage network V_{fold}(N_1, N_2, d, s) can be operated in strictly nonblocking manner for unicast if S≧2 according to the current invention.

For example, the network of FIG. **4**E shows an exemplary five-stage network, namely V_{fold}(**24**,**8**,**2**,**2**), with the following multicast assignment I_1={2,3} and all other I_j=ϕ for j=[2-8]. It should be noted that the connection I_1 fans out in the first stage switch IS**1** into middle switches MS(**1**,**1**) and MS(**1**,**5**) in middle stage **130**, and fans out in middle switches MS(**1**,**1**) and MS(**1**,**5**) only once into middle switches MS(**2**,**1**) and MS(**2**,**5**) respectively in middle stage **140**.

The connection I_1 also fans out in middle switches MS(**2**,**1**) and MS(**2**,**5**) only once into middle switches MS(**3**,**1**) and MS(**3**,**7**) respectively in middle stage **150**. The connection I_1 also fans out in middle switches MS(**3**,**1**) and MS(**3**,**7**) only once into output switches OS**2** and OS**3** in output stage **120**. Finally the connection I_1 fans out once in the output stage switch OS**2** into outlet link OL**3** and in the output stage switch OS**3** twice into the outlet links OL**5** and OL**6**. In accordance with the invention, each connection can fan out in the input stage switch into at most two middle stage switches in middle stage **130**.

SNB Embodiments:

The folded multi-stage network V_{fold}(N_1, N_2, d, s) disclosed, in the current invention, is topologically exactly the same as the multi-stage network V_{fold}(N_1, N_2, d, s), disclosed in U.S. Provisional Patent Application Ser. No. 60/940,391 that is incorporated by reference above, excepting that in the illustrations folded network V_{fold}(N_1, N_2, d, s) is shown as it is folded at middle stage **130**+10*(Log_d N_1−2).

The general symmetrical folded multi-stage network V_{fold} (N, d, s) can also be operated in strictly nonblocking manner for multicast when s≧3 according to the current invention. Similarly the general asymmetrical folded multi-stage network V_{fold}(N_1, N_2, d, s) can also be operated in strictly nonblocking manner for multicast when S≧3 according to the current invention.

Symmetric Folded RNB Unicast Embodiments:

Referring to FIG. **5**A, an exemplary symmetrical folded multi-stage network **500**A respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by two switches IS**1**-IS**4** and output stage **120** consists of four, two by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, two by two switches MS(**1**, **1**)-MS(**1**,**4**), middle stage **140** consists of four, two by two switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, two by two switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in rearrangeably nonblocking manner for unicast connections, because the switches in the input stage **110** are of size two by two, the switches in output stage **120** are of size two by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

The connection topology of the network **500**A shown in FIG. **5**A is known to be back to back inverse Benes connection topology. In other embodiments the connection topology is different. That is the way the links ML(**1**,**1**)-ML(**1**,**8**), ML(**2**,**1**)-ML(**2**,**8**), ML(**3**,**1**)-ML(**3**,**8**), and ML(**4**,**1**)-ML(**4**,**8**) are connected between the respective stages is different.

Even though only one embodiment is illustrated, in general, the network V_{fold}(N, d, s) can comprise any arbitrary type of connection topology. For example the connection topology of the network V_{fold}(N, d, s) may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the V_{fold}(N, d, s) network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network V_{fold}(N, d, s) can be built. The embodiment of FIG. **5**A is only one example of network V_{fold}(N, d, s).

The network **500**A of FIG. **5**A is also rearrangeably nonblocking for unicast according to the current invention. In one embodiment of these networks each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable N/d, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by N/d. The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*d and each output switch OS**1**-OS**4** can be denoted in general with the notation d*d. Likewise, the size of each switch in any of the middle stages can be denoted as d*d. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric folded multi-stage network can be represented with the notation V_{fold}(N, d, s), where N represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL**1**-IL**8** as there are outlet links OL**1**-OL**8**, in a symmetrical network they are the same.

In network **500**A of FIG. **5**A, each of the N/d input switches IS**1**-IS**4** are connected to exactly d switches in middle stage **130** through d links (for example input switch IS**1** is connected to middle switches MS(**1**,**1**) and MS(**1**,**2**) through the links ML(**1**,**1**) and ML(**1**,**2**) respectively).

Each of the N/d middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through d links (for example the links ML(**1**,**1**) and ML(**1**,**4**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1** and IS**2** respectively) and also are connected to exactly d switches in middle stage **140** through d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**) and MS(**2**,**3**) respectively).

Similarly each of the N/d middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through d links (for example the links ML(**2**,**1**) and ML(**2**,**6**) are connected to the middle switch MS(**2**,**1**) from middle switches MS(**1**,**1**) and MS(**1**,**3**) respectively) and also are connected to exactly d switches in middle stage **150** through d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**) and MS(**3**,**3**) respectively).

Similarly each of the N/d middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through d links (for example the links ML(**3**,**1**) and ML(**3**,**6**) are connected to the middle switch MS(**3**,**1**) from middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively) and also are connected to exactly d output switches in output stage **120** through d links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switches OS**1** and OS**2** respectively from middle switch MS(**3**,**1**)).

Each of the N/d output switches OS**1**-OS**4** are connected from exactly d switches in middle stage **150** through d links (for example output switch OS**1** is connected from middle switches MS(**3**,**1**) and MS(**3**,**2**) through the links ML(**4**,**1**) and ML(**4**,**4**) respectively).

Generalized Symmetric Folded RNB Unicast Embodiments:

Network **500**B of FIG. **5**B is an example of general symmetrical folded multi-stage network V_{fold}(N, d, s) with $(2\times\log_d N)-1$ stages. The general symmetrical folded multi-stage network V_{fold}(N, d, s) can be operated in rearrangeably nonblocking manner for unicast when $s \geqq 1$ according to the current invention (and in the example of FIG. **5**B, s=1). The general symmetrical folded multi-stage network V_{fold}(N, d, s) with $(2\times\log_d N)-1$ stages has d inlet links for each of N/d input switches IS**1**-IS(N/d) (for example the links IL**1**-IL(d) to the input switch IS**1**) and d outgoing links for each of N/d input switches IS**1**-IS(N/d) (for example the links ML(**1**,**1**)-ML(1, d) to the input switch IS**1**). There are d outlet links for each of N/d output switches OS**1**-OS(N/d) (for example OL**1**-OL(d) to the output switch OS**1**) and d incoming links for each of N/d output switches OS**1**-OS(N/d) (for example ML($2\times\text{Log}_d N-2$,**1**)-ML($2\times\text{Log}_d N-2$, d) to the output switch OS**1**).

Each of the N/d input switches IS**1**-IS(N/d) are connected to exactly d switches in middle stage **130** through d links.

Each of the N/d middle switches MS(**1**,**1**)-MS(**1**,N/d) in the middle stage **130** are connected from exactly d input switches through d links and also are connected to exactly d switches in middle stage **140** through d links.

Similarly each of the N/d middle switches

$$MS(\text{Log}_d N-1,\ 1)-MS\left(\text{Log}_d N-1,\ \frac{N}{d}\right)$$

in the middle stage **130**+10*(Log_d N−2) are connected from exactly d switches in middle stage **130**+10*(Log_d N−3) through d links and also are connected to exactly d switches in middle stage **130**+10*(Log_d N−1) through d links.

Similarly each of the N/d middle switches

$$MS(2\times\text{Log}_d N-3,\ 1)-MS\left(2\times\text{Log}_d N-3,\ \frac{N}{d}\right)$$

in the middle stage **130**+10*(2*Log_d N−4) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N−5) through d links and also are connected to exactly d output switches in output stage **120** through d links.

Each of the N/d output switches OS**1**-OS(N/d) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N−4) through d links.

The general symmetrical folded multi-stage network V_{fold}(N, d, s) can be operated in rearrangeably nonblocking manner for multicast when s=1 according to the current invention.

Asymmetric Folded RNB (N_2>N_1) Unicast Embodiments:

Referring to FIG. **5**C, an exemplary symmetrical folded multi-stage network **500**C respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by two switches IS**1**-IS**4** and output stage **120** consists of four, six by six switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, two by two switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, two by two switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, two by six switches MS(**3**,**1**)-MS(**3**,**4**).

Such networks can be operated in rearrangeably nonblocking manner for unicast connections, because the switches in the input stage **110** are of size two by two, the switches in output stage **120** are of size six by six, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

The connection topology of the network **500**C shown in FIG. **5**C is known to be back to back inverse Benes connection topology. The connection topology of the networks **500**C is different in the other embodiments. That is the way the links ML(**1**,**1**)-ML(**1**,**8**), ML(**2**,**1**)-ML(**2**,**8**), ML(**3**,**1**)-ML(**3**,**8**), and ML(**4**,**1**)-ML(**4**,**8**) are connected between the respective stages is different.

Even though only one embodiment is illustrated, in general, the network V_{fold}(N_1, N_2, d, s) can comprise any arbitrary type of connection topology. For example the connection topology of the network V_{fold}(N_1, N_2, d, s) may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the V_{fold}(N_1, N_2, d, s) network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network V_{fold}(N_1, N_2, d, s) can be built. The embodiment of FIG. **5**C is only one example of network V_{fold}(N_1, N_2, d, s).

The networks **500**C of FIG. **5**C is also rearrangeably nonblocking for unicast according to the current invention. In one embodiment of these networks each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_1}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and N_2>N_1 and N_2=p*N_1 where p>1. The number of middle switches in each middle stage is denoted by

$$\frac{N_1}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*d and each output switch OS**1**-OS**4** can be denoted in general with the notation d_2*d_2, where

$$d_2 = N_2 \times \frac{d}{N_1} = p \times d.$$

The size of each switch in any of the middle stages excepting the last middle stage can be denoted as d*d. The size of each switch in the last middle stage can be denoted as d*d_2. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric folded multi-stage network can be represented with the notation V_{fold}(N_1, N_2, d, s), where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**24**), d represents the inlet links of each input switch where N_2>N_1, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

In network **500**C of FIG. **5**C, each of the

$$\frac{N_1}{d}$$

input switches IS**1**-IS**4** are connected to exactly d switches in middle stage **130** through d links (for example input switch IS**1** is connected to middle switches MS(**1**,**1**) and MS(**1**,**2**) through the links ML(**1**,**1**) and ML(**1**,**2**) respectively).

Each of the

$$\frac{N_1}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through d links (for example the links ML(**1**,**1**) and ML(**1**,**4**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1** and IS**2** respectively) and also are connected to exactly d switches in middle stage **140** through d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**) and MS(**2**,**3**) respectively).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through d links (for example the links ML(**2**,**1**) and ML(**2**,**6**) are connected to the middle switch MS(**2**,**1**) from middle switches MS(**1**,**1**) and MS(**1**,**3**) respectively) and also are connected to exactly d switches in middle stage **150** through d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**) and MS(**3**,**3**) respectively).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through d links (for example the links ML(**3**,**1**) and ML(**3**,**6**) are connected to the middle switch MS(**3**,**1**) from middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively) and also are connected to exactly d output switches in output stage **120** through d_2 links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switches OS**1** from middle switch MS(**3**,**1**); the links ML(**4**,**3**) and ML(**4**,**4**) are connected to output switches OS**2** from middle switch MS(**3**,**1**); the link ML(**4**,**5**) is connected to output switches OS**3** from middle switch MS(**3**,**1**); and the link ML(**4**,**6**) is connected to output switches OS**4** from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS**4** are connected from exactly d switches in middle stage **150** through d_2 links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**) and ML(**4**,**2**); output switch OS**1** is connected from middle switch MS(**3**,**2**) through the links ML(**4**,**7**) and ML(**4**,**8**); output switch OS**1** is connected from middle switch MS(**3**,**3**) through the link ML(**4**,**13**); and output switch OS**1** is connected from middle switch MS(**3**,**4**) through the links ML(**4**,**19**)).

Generalized Asymmetric Folded RNB ($N_2>N_1$) Unicast Embodiments:

Network **500**D of FIG. **5**D is an example of general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ with $(2\times\log_d N)-1$ stages where $N_2>N_1$ and $N_2=p*N_1$ where $p>1$. In network **500**D of FIG. **5**D, $N_1=N$ and $N_2=p*N$. The general symmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for unicast when $s\geqq 1$ according to the current invention (and in the example of FIG. **5**D, s=1). The general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ with $(2\times\log_d N)-1$ stages has d inlet links for each of

$$\frac{N_1}{d}$$

input switches IS**1**-IS(N_1/d) (for example the links IL**1**-IL(d) to the input switch IS**1**) and d outgoing links for each of

$$\frac{N_1}{d}$$

input switches IS**1**-IS(N_1/d) (for example the links ML(**1**,**1**)-ML(1, d) to the input switch IS**1**). There are d_2 (where

$$\left(\text{where } d_2 = N_2 \times \frac{d}{N_1} = p \times d\right)$$

outlet links for each of

$$\frac{N_1}{d}$$

output switches OS**1**-OS(N_1/d) (for example the links OL**1**-OL(p*d) to the output switch OS**1**) and d_2 (=p×d) incoming links for each of

$$\frac{N_1}{d}$$

output switches OS**1**-OS(N_1/d) (for example ML($2\times\text{Log}_d N_1-2$,**1**)-ML($2\times\text{Log}_d N_1-2$, d_2) to the output switch OS**1**).

Each of the

$$\frac{N_1}{d}$$

input switches IS**1**-IS(N_1/d) are connected to exactly d switches in middle stage **130** through d links.

Each of the

$$\frac{N_1}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,N_1/d) in the middle stage **130** are connected from exactly d input switches through d links and also are connected to exactly d switches in middle stage **140** through d links.

Similarly each of the

$$\frac{N_1}{d}$$

middle switches

$$MS(\text{Log}_d N_1 - 1, 1) - MS\left(\text{Log}_d N_1 - 1, \frac{N_1}{d}\right)$$

in the middle stage **130**+10*($\text{Log}_d N_1-2$) are connected from exactly d switches in middle stage **130**+10*($\text{Log}_d N_1-3$) through d links and also are connected to exactly d switches in middle stage **130**+10*($\text{Log}_d N_1-1$) through d links.

Similarly each of the

$$\frac{N_1}{d}$$

middle switches

$$MS(2\times\text{Log}_d N_1 - 3, 1) - MS\left(2\times\text{Log}_d N_1 - 3, \frac{N_1}{d}\right)$$

in the middle stage **130**+10*($2*\text{Log}_d N_1-4$) are connected from exactly d switches in middle stage **130**+10*($2*\text{Log}_d$

N_1-5) through d links and also are connected to exactly d output switches in output stage **120** through d_1 links.

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS(N_1/d) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N−4) through d_2 links.

The general symmetrical folded multi-stage network V_{fold}(N_1, N_2, d, s) can be operated in rearrangeably nonblocking manner for multicast when s≧1 according to the current invention.

Asymmetric Folded RNB (N_1>N_2) Unicast Embodiments:

Referring to FIG. **5**E, an exemplary symmetrical folded multi-stage network **500**E with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, six by six switches IS**1**-IS**4** and output stage **120** consists of four, two by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, six by two switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, two by two switches MS(**2**, **1**)-MS(**2**,**4**), and middle stage **150** consists of four, two by two switches MS(**3**,**1**)-MS(**3**,**4**).

Such a network can be operated in rearrangeably nonblocking manner for unicast connections, because the switches in the input stage **110** are of size six by six, the switches in output stage **120** are of size two by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

The connection topology of the network **500**E shown in FIG. **5**E is known to be back to back inverse Benes connection topology. The connection topology of the networks **500**E is different in the other embodiments. That is the way the links ML(**1**,**1**)-ML(**1**,**8**), ML(**2**,**1**)-ML(**2**,**8**), ML(**3**,**1**)-ML(**3**,**8**), and ML(**4**,**1**)-ML(**4**,**8**) are connected between the respective stages is different.

Even though only one embodiment is illustrated, in general, the network V_{fold}(N_1, N_2, d, s), comprise any arbitrary type of connection topology. For example the connection topology of the network V_{fold}(N_1, N_2, d, s) may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the V_{fold}(N_1, N_2, d, s) network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network V_{fold}(N_1, N_2, d, s) can be built. The embodiment of FIG. **5**E is only one example of network V_{fold}(N_1, N_2, d, s).

The network **500**E is rearrangeably nonblocking for unicast according to the current invention. In one embodiment of these networks each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_2}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and N_1>N_2 and N_1=p*N_2 where p>1. The number of middle switches in each middle stage is denoted by

$$\frac{N_2}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d_1*d_1 and each output switch OS**1**-OS**4** can be denoted in general with the notation (d*d), where

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d.$$

The size of each switch in any of the middle stages excepting the first middle stage can be denoted as d*d. The size of each switch in the first middle stage can be denoted as d_1*d. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric folded multi-stage network can be represented with the notation V_{fold}(N_1, N_2, d, s), where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**24**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**8**), d represents the inlet links of each output switch where N_1>N_2, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

In network **500**E of FIG. **5**E, each of the

$$\frac{N_2}{d}$$

input switches IS**1**-IS**4** are connected to exactly d switches in middle stage **130** through d_1 links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**) and ML(**1**,**2**); input switch IS**1** is connected to middle switch MS(**1**,**2**) through the links ML(**1**,**3**) and ML(**1**, **4**); input switch IS**1** is connected to middle switch MS(**1**,**3**) through the link ML(**1**,**5**); and input switch IS**1** is connected to middle switch MS(**1**,**4**) through the links ML(**1**,**6**)).

Each of the

$$\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d, input switches through d links (for example the links ML(**1**,**1**) and ML(**1**,**2**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**; the links ML(**1**,**7**) and ML(**1**,**8**) are connected to the middle switch MS(**1**,**1**) from input switch IS**2**; the link ML(**1**,**13**) is connected to the middle switch MS(**1**,**1**) from input switch IS**3**; and the link ML(**1**,**19**) is connected to the middle switch MS(**1**,**1**) from input switch IS**4**), and also are connected to exactly d switches in middle stage **140** through d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**) and MS(**2**, **3**) respectively).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through d links (for example the links ML(**2**,**1**) and ML(**2**,**6**) are connected to the middle switch MS(**2**,**1**) from middle switches MS(**1**,**1**) and MS(**1**,**3**) respectively) and also are connected to exactly d switches in middle stage **150** through d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**) and MS(**3**,**3**) respectively).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through d links (for example the links ML(**3**,**1**) and ML(**3**,**6**) are connected to the middle switch MS(**3**,**1**) from middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively) and also are connected to exactly d output switches in output stage **120** through d_1 links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switches OS**1** and OS**2** respectively from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS**4** are connected from exactly d switches in middle stage **150** through d_2 links (for example output switch OS**1** is connected from middle switches MS(**3**, **1**) and MS(**3**,**2**) through the links ML(**4**,**1**) and ML(**4**,**4**) respectively).

Generalized Asymmetric Folded RNB ($N_1>N_2$) Unicast Embodiments:

Network **500**F of FIG. **5**F is an example of general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ with $(2\times\log_d N)-1$ stages where $N_1>N_2$ and $N_1=p*N_2$ where p>1. In network **500**F of FIG. **5**F, $N_2=N$ and $N_1=p*N$. The general symmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for unicast when s=1 according to the current invention (and in the example of FIG. **5**F, s=1). The general asymmetrical folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ with $(2\times\log_d N)-1$ stages has d_1 (where

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d$$

inlet links for each of

$$\frac{N_2}{d}$$

input switches IS**1**-IS(N_2/d) (for example the links IL**1**-IL(p*d) to the input switch IS**1**) and d_1 (=p×d) outgoing links for each of

$$\frac{N_2}{d}$$

input switches IS**1**-IS(N_2/d) (for example the links ML(**1**,**1**)-ML(**1**,(d+p*d)) to the input switch IS**1**). There are d outlet links for each of

$$\frac{N_2}{d}$$

output switches OS**1**-OS(N_2/d) (for example the links OL**1**-OL(d) to the output switch OS**1**) and d incoming links for each of

$$\frac{N_2}{d}$$

output switches OS**1**-OS(N_2/d) (for example ML($2\times\text{Log}_d N_2-2$,1)-ML($2\times\text{Log}_d N_2-2$, d) to the output switch OS**1**).

Each of the

$$\frac{N_2}{d}$$

input switches IS**1**-IS(N_2/d) are connected to exactly d switches in middle stage **130** through d_1 links.

Each of the

$$\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,N_2/d) in the middle stage **130** are connected from exactly d input switches through d_1 links and also are connected to exactly d switches in middle stage **140** through d links.

Similarly each of the

$$\frac{N_2}{d}$$

middle switches

$$MS(\text{Log}_d N_2 - 1, 1) - MS\left(\text{Log}_d N_2 - 1, \frac{N_2}{d}\right)$$

in the middle stage **130**+10*($\text{Log}_d N_2-2$) are connected from exactly d switches in middle stage **130**+10*($\text{Log}_d N_2-3$) through d links and also are connected to exactly d switches in middle stage **130**+10*($\text{Log}_d N_2-1$) through d links.

Similarly each of the

$$\frac{N_2}{d}$$

middle switches

$$MS(2\times\mathrm{Log}_d N_2-3,\,1)-MS\left(2\times\mathrm{Log}_d N_2-3,\,\frac{N_2}{d}\right)$$

in the middle stage **130**+10*(2*Log_d N_2−4) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N_2−5) through d links and also are connected to exactly d output switches in output stage **120** through d links.

Each of the

$$\frac{N_2}{d}$$

output switches OS**1**-OS(N_2/d) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N_2−4) through d links.

The general symmetrical folded multi-stage network V_{fold} (N_1, N_2, d, s) can be operated in rearrangeably nonblocking manner for unicast when s≧1 according to the current invention.

Symmetric RNB Unicast Embodiments:

Referring to FIG. **6**A, FIG. **6**B, FIG. **6**C, FIG. **6**D, FIG. **6**E, FIG. **6**F, FIG. **6**G, FIG. **600**H, FIG. **600**I and FIG. **6**J with exemplary symmetrical multi-stage networks **600**A, **600**B, **600**C, **600**D, **600**E, **600**F, **600**G, **600**H, **600**I, and **600**J respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by two switches IS**1**-IS**4** and output stage **120** consists of four, two by two switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, two by two switches MS(**1**,**1**)-MS(**1**,**4**), middle stage **140** consists of four, two by two switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, two by two switches MS(**3**,**1**)-MS(**3**,**4**).

Such networks can be operated in rearrangeably nonblocking manner for unicast connections, because the switches in the input stage **110** are of size two by two, the switches in output stage **120** are of size two by two, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In all the ten embodiments of FIG. **6**A to FIG. **6**J the connection topology is different. That is the way the links ML(**1**,**1**)-ML(**1**,**8**), ML(**2**,**1**)-ML(**2**,**8**), ML(**3**,**1**)-ML(**3**,**8**), and ML(**4**,**1**)-ML(**4**,**8**) are connected between the respective stages is different. For example, the connection topology of the network **600**A shown in FIG. **6**A is known to be back to back inverse Benes connection topology; the connection topology of the network **600**B shown in FIG. **6**B is known to be back to back Omega connection topology; and the connection topology of the network **600**C shown in FIG. **6**C is hereinafter called nearest neighbor connection topology.

Even though only ten embodiments are illustrated, in general, the network V(N, d, s) can comprise any arbitrary type of connection topology. For example the connection topology of the network V(N, d, s) may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the V(N, d, s) network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network V(N, d, s) can be built. The ten embodiments of FIG. **6**A to FIG. **6**J are only three examples of network V(N, d, s).

The networks **600**A-**600**J of FIG. **6**A-FIG. **6**J are also rearrangeably nonblocking for unicast according to the current invention. In one embodiment of these networks each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable N/d, where N is the total number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by N/d. The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*d and each output switch OS**1**-OS**4** can be denoted in general with the notation d*d. Likewise, the size of each switch in any of the middle stages can be denoted as d*d. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric multi-stage network can be represented with the notation V(N, d, s), where N represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), d represents the inlet links of each input switch or outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch. Although it is not necessary that there be the same number of inlet links IL**1**-IL**8** as there are outlet links OL**1**-OL**8**, in a symmetrical network they are the same.

In network **600**A of FIG. **6**A, each of the N/d input switches IS**1**-IS**4** are connected to exactly d switches in middle stage **130** through d links (for example input switch IS**1** is connected to middle switches MS(**1**,**1**) and MS(**1**,**2**) through the links ML(**1**,**1**) and ML(**1**,**2**) respectively).

Each of the N/d middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through d links (for example the links ML(**1**,**1**) and ML(**1**,**4**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1** and IS**2** respectively) and also are connected to exactly d switches in middle stage **140** through d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**) and MS(**2**,**3**) respectively).

Similarly each of the N/d middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through d links (for example the links ML(**2**,**1**) and ML(**2**,**6**) are connected to the middle switch MS(**2**,**1**) from middle switches MS(**1**,**1**) and MS(**1**,**3**) respectively) and also are connected to exactly d switches in middle stage **150** through d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**) and MS(**3**,**3**) respectively).

Similarly each of the N/d middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through d links (for example the links ML(**3**,**1**) and ML(**3**,**6**) are connected to the middle switch MS(**3**,**1**) from middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively) and also are connected to exactly d output switches in output stage **120** through d links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switches OS**1** and OS**2** respectively from middle switch MS(**3**,**1**)).

Each of the N/d output switches OS1-OS4 are connected from exactly d switches in middle stage **150** through d links (for example output switch OS1 is connected from middle switches MS(**3**,**1**) and MS(**3**,**2**) through the links ML(**4**,**1**) and ML(**4**,**4**) respectively).

Generalized Symmetric RNB Unicast Embodiments:

Network **600**K of FIG. **6**K is an example of general symmetrical multi-stage network V(N, d, s) with $(2\times\log_d N)-1$ stages. The general symmetrical multi-stage network V(N, d, s) can be operated in rearrangeably nonblocking manner for unicast when $s\geqq 1$ according to the current invention (and in the example of FIG. **6**K, s=1). The general symmetrical multi-stage network V(N, d, s) with $(2\times\log_d N)-1$ stages has d inlet links for each of N/d input switches IS**1**-IS(N/d) (for example the links IL**1**-IL(d) to the input switch IS**1**) and d outgoing links for each of N/d input switches IS**1**-IS(N/d) (for example the links ML(**1**,**1**)-ML(1, d) to the input switch IS**1**). There are d outlet links for each of N/d output switches OS**1**-OS(N/d) (for example OL**1**-OL(d) to the output switch OS**1**) and d incoming links for each of N/d output switches OS**1**-OS(N/d) (for example ML($2\times\text{Log}_d$N−2,1)-ML($2\times\text{Log}_d$ N−2,d) to the output switch OS**1**).

Each of the N/d input switches IS**1**-IS(N/d) are connected to exactly d switches in middle stage **130** through d links.

Each of the N/d middle switches MS(**1**,**1**)-MS(**1**,N/d) in the middle stage **130** are connected from exactly d input switches through d links and also are connected to exactly d switches in middle stage **140** through d links.

Similarly each of the N/d middle switches

$$MS(\text{Log}_d N-1,\,1)-MS\left(\text{Log}_d N-1,\,\frac{N}{d}\right)$$

in the middle stage **130+10***(Log_d N−2) are connected from exactly d switches in middle stage **130+10***(Log_d N−3) through d links and also are connected to exactly d switches in middle stage **130+10***(Log_d N−1) through d links.

Similarly each of the N/d middle switches

$$MS(2\times\text{Log}_d N-3,\,1)-MS\left(2\times\text{Log}_d N-3,\,\frac{N}{d}\right)$$

in the middle stage **130**+10*(2*Log_d N−4) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N−5) through d links and also are connected to exactly d output switches in output stage **120** through d links.

Each of the N/d output switches OS**1**-OS(N/d) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N−4) through d links.

The general symmetrical multi-stage network V(N, d, s) can be operated in rearrangeably nonblocking manner for unicast when $s\geqq 1$ according to the current invention.

Asymmetric RNB ($N_2>N_1$) Unicast Embodiments:

Referring to FIG. **6A1**, FIG. **6B1**, FIG. **6C1**, FIG. **6D1**, FIG. **6E1**, FIG. **6F1**, FIG. **6G1**, FIG. **600H1**, FIG. **600H1** and FIG. **6J1** with exemplary symmetrical multi-stage networks **600A1**, **600B1**, **600C1**, **600D1**, **600E1**, **600F1**, **600G1**, **600H1**, **600I1**, and **600J1** respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage **110** and output stage **120** via middle stages **130**, **140**, and **150** is shown where input stage **110** consists of four, two by two switches IS**1**-IS**4** and output stage **120** consists of four, six by six switches OS**1**-OS**4**. And all the middle stages namely middle stage **130** consists of four, two by two switches MS(**1**, **1**)-MS(**1**,**4**), middle stage **140** consists of four, two by two switches MS(**2**,**1**)-MS(**2**,**4**), and middle stage **150** consists of four, two by six switches MS(**3**,**1**)-MS(**3**,**4**).

Such networks can be operated in rearrangeably nonblocking manner for unicast connections, because the switches in the input stage **110** are of size two by two, the switches in output stage **120** are of size six by six, and there are four switches in each of middle stage **130**, middle stage **140** and middle stage **150**.

In all the ten embodiments of FIG. **6A1** to FIG. **6J1** the connection topology is different. That is the way the links ML(**1**,**1**)-ML(**1**,**8**), ML(**2**,**1**)-ML(**2**,**8**), ML(**3**,**1**)-ML(**3**,**8**), and ML(**4**,**1**)-ML(**4**,**8**) are connected between the respective stages is different. For example, the connection topology of the network **600A1** shown in FIG. **6A1** is known to be back to back inverse Benes connection topology; the connection topology of the network **600B1** shown in FIG. **6B1** is known to be back to back Omega connection topology; and the connection topology of the network **600C1** shown in FIG. **6C1** is hereinafter called nearest neighbor connection topology.

Even though only ten embodiments are illustrated, in general, the network V(N_1, N_2, d, s) can comprise any arbitrary type of connection topology. For example the connection topology of the network V(N_1, N_2, d, s) may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the V(N_1, N_2, d, s) network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network V(N_1, N_2, d, s) can be built. The ten embodiments of FIG. **6A1** to FIG. **6J1** are only three examples of network V(N_1, N_2, d, s).

The networks **600A1**-**600J1** of FIG. **6A1**-FIG. **6J1** are also rearrangeably nonblocking for unicast according to the current invention. In one embodiment of these networks each of the input switches IS**1**-IS**4** and output switches OS**1**-OS**4** are crossbar switches. The number of switches of input stage **110** and of output stage **120** can be denoted in general with the variable

$$\frac{N_1}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_2>N_1$ and $N_2=p*N_1$ where p>1. The number of middle switches in each middle stage is denoted by

$$\frac{N_1}{d}.$$

The size of each input switch IS**1**-IS**4** can be denoted in general with the notation d*d and each output switch OS**1**-OS**4** can be denoted in general with the notation d_2*d_2, where

$$d_2 = N_2\times\frac{d}{N_1} = p\times d.$$

The size of each switch in any of the middle stages excepting the last middle stage can be denoted as d*d. The size of each switch in the last middle stage can be denoted as d^*d_2. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-stage network can be represented with the notation $V(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of all input switches (for example the links IL**1**-IL**8**), N_2 represents the total number of outlet links of all output switches (for example the links OL**1**-OL**24**), d represents the inlet links of each input switch where $N_2>N_1$, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

In network **600A1** of FIG. **6A1**, each of the

$$\frac{N_1}{d}$$

input switches IS**1**-IS**4** are connected to exactly d switches in middle stage **130** through d links (for example input switch IS**1** is connected to middle switches MS(**1**,**1**) and MS(**1**,**2**) through the links ML(**1**,**1**) and ML(**1**,**2**) respectively).

Each of the

$$\frac{N_1}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d input switches through d links (for example the links ML(**1**,**1**) and ML(**1**,**4**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1** and IS**2** respectively) and also are connected to exactly d switches in middle stage **140** through d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**) and MS(**2**,**3**) respectively).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through d links (for example the links ML(**2**,**1**) and ML(**2**,**6**) are connected to the middle switch MS(**2**,**1**) from middle switches MS(**1**,**1**) and MS(**1**,**3**) respectively) and also are connected to exactly d switches in middle stage **150** through d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**) and MS(**3**,**3**) respectively).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through d links (for example the links ML(**3**,**1**) and ML(**3**,**6**) are connected to the middle switch MS(**3**,**1**) from middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively) and also are connected to exactly d output switches in output stage **120** through d_2 links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switches OS**1** from middle switch MS(**3**,**1**); the links ML(**4**,**3**) and ML(**4**,**4**) are connected to output switches OS**2** from middle switch MS(**3**,**1**); the link ML(**4**,**5**) is connected to output switches OS**3** from middle switch MS(**3**,**1**); and the link ML(**4**,**6**) is connected to output switches OS**4** from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS**4** are connected from exactly d switches in middle stage **150** through d_2 links (for example output switch OS**1** is connected from middle switch MS(**3**,**1**) through the links ML(**4**,**1**) and ML(**4**,**2**); output switch OS**1** is connected from middle switch MS(**3**,**2**) through the links ML(**4**,**7**) and ML(**4**,**8**); output switch OS**1** is connected from middle switch MS(**3**,**3**) through the link ML(**4**,**13**); and output switch OS**1** is connected from middle switch MS(**3**,**4**) through the links ML(**4**,**19**)).

Generalized Asymmetric RNB ($N_2>N_1$) Unicast Embodiments:

Network **600K1** of FIG. **6K1** is an example of general asymmetrical multi-stage network $V(N_1, N_2, d, s)$ with $(2\times\log_d N)-1$ stages where $N_2>N_1$ and $N_2=p^*N_1$ where $p>1$. In network **400K1** of FIG. **4K1**, $N_1=N$ and $N_2=p^*N$. The general symmetrical multi-stage network $V(N_1, N_2, d, s)$ can be operated in rearrangeably nonblocking manner for unicast when $s\geqq 1$ according to the current invention (and in the example of FIG. **6K1**, s=1). The general asymmetrical multi-stage network $V(N_1, N_2, d, s)$ with $(2\times\log_d N)-1$ stages has d inlet links for each of

$$\frac{N_1}{d}$$

input switches IS**1**-IS(N_1/d) (for example the links IL**1**-IL(d) to the input switch IS**1**) and d outgoing links for each of

$$\frac{N_1}{d}$$

input switches IS**1**-IS(N_1/d) (for example the links ML(**1**,**1**)-ML(1, d) to the input switch IS**1**). There are d_2 (where

$$\left(\text{where } d_2 = N_2 \times \frac{d}{N_1} = p \times d\right)$$

outlet links for each of

$$\frac{N_1}{d}$$

output switches OS**1**-OS(N_1/d) (for example the links OL**1**-OL(p*d) to the output switch OS**1**) and d_2 (=p×d) incoming links for each of

$$\frac{N_1}{d}$$

output switches OS1-OS(N_1/d) (for example ML($2\times\text{Log}_d N_1-2$,1)-ML($2\times\text{Log}_d N_1-2$, d_2) to the output switch OS1).

Each of the

$$\frac{N_1}{d}$$

input switches IS1-IS(N_1/d) are connected to exactly d switches in middle stage 130 through d links.

Each of the

$$\frac{N_1}{d}$$

middle switches MS(1,1)-MS(1,N_1/d) in the middle stage 130 are connected from exactly d input switches through d links and also are connected to exactly d switches in middle stage 140 through d links.

Similarly each of the

$$\frac{N_1}{d}$$

middle switches

$$MS(\text{Log}_d N_1-1,\ 1)-MS\left(\text{Log}_d N_1-1,\ \frac{N_1}{d}\right)$$

in the middle stage 130+10*($\text{Log}_d N_1-2$) are connected from exactly d switches in middle stage 130+10*($\text{Log}_d N_1-3$) through d links and also are connected to exactly d switches in middle stage 130+10*($\text{Log}_d N_1-1$) through d links.

Similarly each of the

$$\frac{N_1}{d}$$

middle switches

$$MS(2\times\text{Log}_d N_1-3,\ 1)-MS\left(2\times\text{Log}_d N_1-3,\ \frac{N_1}{d}\right)$$

in the middle stage 130+10*(2*$\text{Log}_d N_1-4$) are connected from exactly d switches in middle stage 130+10*(2*$\text{Log}_d N_1-5$) through d links and also are connected to exactly d output switches in output stage 120 through d_1 links.

Each of the

$$\frac{N_1}{d}$$

output switches OS1-OS(N_1/d) are connected from exactly d switches in middle stage 130+10*(2*Log_d N−4) through d_2 links.

The general symmetrical multi-stage network V(N_1, N_2, d, s) can be operated in rearrangeably nonblocking manner for multicast when s=1 according to the current invention.

Asymmetric RNB ($N_1>N_2$) Unicast Embodiments:

Referring to FIG. 6A2, FIG. 6B2, FIG. 6C2, FIG. 6D2, FIG. 6E2, FIG. 6F2, FIG. 6G2, FIG. 600H2, FIG. 600I2 and FIG. 6J2 with exemplary symmetrical multi-stage networks 600A2, 600B2, 600C2, 600D2, 600E2, 600F2, 600G2, 600H2, 600I2, and 600J2 respectively with five stages of twenty switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, and 150 is shown where input stage 110 consists of four, six by six switches IS1-IS4 and output stage 120 consists of four, two by two switches OS1-OS4. And all the middle stages namely middle stage 130 consists of four, six by two switches MS(1,1)-MS(1,4), middle stage 140 consists of four, two by two switches MS(2,1)-MS(2,4), and middle stage 150 consists of four, two by two switches MS(3,1)-MS(3,4).

Such networks can be operated in rearrangeably nonblocking manner for unicast connections, because the switches in the input stage 110 are of size six by six, the switches in output stage 120 are of size two by two, and there are four switches in each of middle stage 130, middle stage 140 and middle stage 150.

In all the ten embodiments of FIG. 6A2 to FIG. 6J2 he connection topology is different. That is the way the links ML(1,1)-ML(1,8), ML(2,1)-ML(2,8), ML(3,1)-ML(3,8), and ML(4,1)-ML(4,8) are connected between the respective stages is different. For example, the connection topology of the network 600A2 shown in FIG. 6A2 is known to be back to back inverse Benes connection topology; the connection topology of the network 600B2 shown in FIG. 6B2 is known to be back to back Omega connection topology; and the connection topology of the network 600C2 shown in FIG. 6C2 is hereinafter called nearest neighbor connection topology.

Even though only ten embodiments are illustrated, in general, the network V(N_1, N_2, d, s) can comprise any arbitrary type of connection topology. For example the connection topology of the network V(N_1, N_2, d, s) may be back to back Benes networks, Delta Networks and many more combinations. The applicant notes that the fundamental property of a valid connection topology of the V(N_1, N_2, d, s) network is, when no connections are setup from any input link all the output links should be reachable. Based on this property numerous embodiments of the network V(N_1, N_2, d, s) can be built. The ten embodiments of FIG. 6A2 to FIG. 6J2 are only three examples of network V(N_1, N_2, d, s).

The networks 600A2-600J2 of FIG. 6A2-FIG. 6J2 are also rearrangeably nonblocking for unicast according to the current invention. In one embodiment of these networks each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable

$$\frac{N_2}{d},$$

where N_1 is the total number of inlet links or and N_2 is the total number of outlet links and $N_1>N_2$ and $N_1=p*N_2$ where p>1.

The number of middle switches in each middle stage is denoted by

$$\frac{N_2}{d}.$$

The size of each input switch IS1-IS4 can be denoted in general with the notation d_1*d_1 and each output switch OS1-OS4 can be denoted in general with the notation (d*d), where

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d.$$

The size of each switch in any of the middle stages excepting the first middle stage can be denoted as d*d. The size of each switch in the first middle stage can be denoted as d_1*d. A switch as used herein can be either a crossbar switch, or a network of switches each of which in turn may be a crossbar switch or a network of switches. An asymmetric multi-stage network can be represented with the notation V(N_1, N_2, d, s), where N, represents the total number of inlet links of all input switches (for example the links IL1-IL24), N, represents the total number of outlet links of all output switches (for example the links OL1-OL8), d represents the inlet links of each output switch where N_1>N_2, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

In network **600**A**2** of FIG. **6**A**2**, each of the

$$\frac{N_2}{d}$$

input switches IS**1**-IS**4** are connected to exactly d switches in middle stage **130** through d_1 links (for example input switch IS**1** is connected to middle switch MS(**1**,**1**) through the links ML(**1**,**1**) and ML(**1**,**2**); input switch IS**1** is connected to middle switch MS(**1**,**2**) through the links ML(**1**,**3**) and ML(**1**,**4**); input switch IS**1** is connected to middle switch MS(**1**,**3**) through the link ML(**1**,**5**); and input switch IS**1** is connected to middle switch MS(**1**,**4**) through the links ML(**1**,**6**)).

Each of the

$$\frac{N_2}{d}$$

middle switches MS(**1**,**1**)-MS(**1**,**4**) in the middle stage **130** are connected from exactly d, input switches through d links (for example the links ML(**1**,**1**) and ML(**1**,**2**) are connected to the middle switch MS(**1**,**1**) from input switch IS**1**; the links ML(**1**,**7**) and ML(**1**,**8**) are connected to the middle switch MS(**1**,**1**) from input switch IS**2**; the link ML(**1**,**13**) is connected to the middle switch MS(**1**,**1**) from input switch IS**3**; and the link ML(**1**,**19**) is connected to the middle switch MS(**1**,**1**) from input switch IS**4**), and also are connected to exactly d switches in middle stage **140** through d links (for example the links ML(**2**,**1**) and ML(**2**,**2**) are connected from middle switch MS(**1**,**1**) to middle switch MS(**2**,**1**) and MS(**2**,**3**) respectively).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**2**,**1**)-MS(**2**,**4**) in the middle stage **140** are connected from exactly d switches in middle stage **130** through d links (for example the links ML(**2**,**1**) and ML(**2**,**6**) are connected to the middle switch MS(**2**,**1**) from middle switches MS(**1**,**1**) and MS(**1**,**3**) respectively) and also are connected to exactly d switches in middle stage **150** through d links (for example the links ML(**3**,**1**) and ML(**3**,**2**) are connected from middle switch MS(**2**,**1**) to middle switch MS(**3**,**1**) and MS(**3**,**3**) respectively).

Similarly each of the

$$\frac{N_1}{d}$$

middle switches MS(**3**,**1**)-MS(**3**,**4**) in the middle stage **150** are connected from exactly d switches in middle stage **140** through d links (for example the links ML(**3**,**1**) and ML(**3**,**6**) are connected to the middle switch MS(**3**,**1**) from middle switches MS(**2**,**1**) and MS(**2**,**3**) respectively) and also are connected to exactly d output switches in output stage **120** through d_1 links (for example the links ML(**4**,**1**) and ML(**4**,**2**) are connected to output switches OS**1** and OS**2** respectively from middle switch MS(**3**,**1**)).

Each of the

$$\frac{N_1}{d}$$

output switches OS**1**-OS**4** are connected from exactly d switches in middle stage **150** through d_2 links (for example output switch OS**1** is connected from middle switches MS(**3**,**1**) and MS(**3**,**2**) through the links ML(**4**,**1**) and ML(**4**,**4**) respectively).

Generalized Asymmetric RNB (N_1>N_2) Unicast Embodiments:

Network **600**K**2** of FIG. **6**K**2** is an example of general asymmetrical multi-stage network V(N_1, N_2, d, s) with ($2\times\log_d N$)−1 stages where N_1>N_2 and N_1=p*N_2 where p>1. In network **400**K**2** of FIG. **4**K**2**, N_2=N and N_1=p*N. The general symmetrical multi-stage network V(N_1, N_2, d, s) can be operated in rearrangeably nonblocking manner for unicast when s≧1 according to the current invention (and in the example of FIG. **6**K**2**, s=1). The general asymmetrical multi-stage network V(N_1, N_2, d, s) with ($2\times\log_d N$)−1 stages has d_1 (where

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d$$

inlet links for each of

$$\frac{N_2}{d}$$

input switches IS1-IS(N_2/d) (for example the links IL1-IL(p*d) to the input switch IS1) and d, (=p×d) outgoing links for each of

$$\frac{N_2}{d}$$

input switches IS1-IS(N_2/d) (for example the links ML(1,1)-ML(1,(d+p*d)) to the input switch IS1). There are d outlet links for each of

$$\frac{N_2}{d}$$

output switches OS1-OS(N_2/d) (for example the links OL1-OL(d) to the output switch OS1) and d incoming links for each of

$$\frac{N_2}{d}$$

output switches OS1-OS(N_2/d) (for example ML(2×Log_d N_2−2,1)-ML(2×Log_d N_2−2, d) to the output switch OS1).

Each of the

$$\frac{N_2}{d}$$

input switches IS1-IS(N_2/d) are connected to exactly d switches in middle stage **130** through d_1 links.

Each of the

$$\frac{N_2}{d}$$

middle switches MS(1,1)-MS(1,N_2/d) in the middle stage **130** are connected from exactly d input switches through d_1 links and also are connected to exactly d switches in middle stage **140** through d links.

Similarly each of the

$$\frac{N_2}{d}$$

middle switches

$$MS(\text{Log}_d N_2 - 1, 1) - MS\left(\text{Log}_d N_2 - 1, \frac{N_2}{d}\right)$$

in the middle stage **130**+10*(Log_d N_1−2) are connected from exactly d switches in middle stage **130**+10*($\text{Log}_d N_1$−3) through d links and also are connected to exactly d switches in middle stage **130**+10*(Log_d N_1−1) through d links.

Similarly each of the

$$\frac{N_2}{d}$$

middle switches

$$MS(2\times\text{Log}_d N_2 - 3, 1) - MS\left(2\times\text{Log}_d N_2 - 3, \frac{N_2}{d}\right)$$

in the middle stage **130**+10*(2*Log_d N_1−4) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N_1−5) through d links and also are connected to exactly d output switches in output stage **120** through d links.

Each of the

$$\frac{N_2}{d}$$

output switches OS1-OS(N_2/d) are connected from exactly d switches in middle stage **130**+10*(2*Log_d N_1−4) through d links.

The general symmetrical multi-stage network V(N_1, N_2, d, s) can be operated in rearrangeably nonblocking manner for unicast when s≧1 according to the current invention.

Scheduling Method Embodiments:

FIG. **7**A shows a high-level flowchart of a scheduling method **1000**, in one embodiment executed to setup multicast and unicast connections in network **100**A of FIG. **1**A (or any of the networks V_{mlink}(N_1, N_2, d, s) and the networks V(N_1, N_2, d, s) disclosed in this invention). According to this embodiment, a multicast connection request is received in act **1010**. Then the control goes to act **1020**.

In act **1020**, based on the inlet link and input switch of the multicast connection received in act **1010**, from each available outgoing middle link of the input switch of the multicast connection, by traveling forward from middle stage **130** to middle stage **130**+10*(Log_d N−2), the lists of all reachable middle switches in each middle stage are derived recursively. That is, first, by following each available outgoing middle link of the input switch all the reachable middle switches in middle stage **130** are derived. Next, starting from the selected middle switches in middle stage **130** traveling through all of their available out going middle links to middle stage **140** all the available middle switches in middle stage **140** are derived. This process is repeated recursively until all the reachable middle switches, starting from the outgoing middle link of input switch, in middle stage **130**+10*(Log_d N−2) are derived. This process is repeated for each available outgoing middle link from the input switch of the multicast connection and separate reachable lists are derived in each middle stage from middle stage **130** to middle stage **130**+10*(Log_d N−2) for all the available outgoing middle links from the input switch. Then the control goes to act **1030**.

In act **1030**, based on the destinations of the multicast connection received in act **1010**, from the output switch of each destination, by traveling backward from output stage **120** to middle stage **130**+10*(Log_d N−2), the lists of all middle switches in each middle stage from which each destination output switch (and hence the destination outlet links) is reachable, are derived recursively. That is, first, by following each available incoming middle link of the output switch of each destination link of the multicast connection, all the middle switches in middle stage **130**+10*(2*Log_d N−4) from which the output switch is reachable, are derived. Next, starting from the selected middle switches in middle stage **130**+10*(2*Log_d N−4) traveling backward through all of their available incoming middle links from middle stage **130**+10*(2*Log_d N−5) all the available middle switches in middle stage **130**+10*(2*Log_d N−5) from which the output switch is reachable, are derived. This process is repeated recursively until all the middle switches in middle stage **130**+10*(Log_d N−2) from which the output switch is reachable, are derived. This process is repeated for each output switch of each destination link of the multicast connection and separate lists in each middle stage from middle stage **130**+10*(2*Log_d N−4) to middle stage **130**+10*(Log_d N−2) for all the output switches of each destination link of the connection are derived. Then the control goes to act **1040**.

In act **1040**, using the lists generated in acts **1020** and **1030**, particularly list of middle switches derived in middle stage **130**+10*(Log_d N−2) corresponding to each outgoing link of the input switch of the multicast connection, and the list of middle switches derived in middle stage **130**+10*(Log_d N−2) corresponding to each output switch of the destination links, the list of all the reachable destination links from each outgoing link of the input switch are derived. Specifically if a middle switch in middle stage **130**+10*(Log_d N−2) is reachable from an outgoing link of the input switch, say "x", and also from the same middle switch in middle stage **130**+10*(Log_d N−2) if the output switch of a destination link, say "y", is reachable then using the outgoing link of the input switch x, destination link y is reachable. Accordingly, the list of all the reachable destination links from each outgoing link of the input switch is derived. The control then goes to act **1050**.

In act **1050**, among all the outgoing links of the input switch, it is checked if all the destinations are reachable using only one outgoing link of the input switch. If one outgoing link is available through which all the destinations of the multicast connection are reachable (i.e., act **1050** results in "yes"), the control goes to act **1070**. And in act **1070**, the multicast connection is setup by traversing from the selected only one outgoing middle link of the input switch in act **1050**, to all the destinations. Then the control transfers to act **1090**.

If act **1050** results "no", that is one outgoing link is not available through which all the destinations of the multicast connection are reachable, then the control goes to act **1060**. In act **1060**, it is checked if all destination links of the multicast connection are reachable using two outgoing middle links from the input switch. According to the current invention, it is always possible to find at most two outgoing middle links from the input switch through which all the destinations of a multicast connection are reachable. So act **1060** always results in "yes", and then the control transfers to act **1080**. In act **1080**, the multicast connection is setup by traversing from the selected only two outgoing middle links of the input switch in act **1060**, to all the destinations. Then the control transfers to act **1090**.

In act **1090**, all the middle links between any two stages of the network used to setup the connection in either act **1070** or act **1080** are marked unavailable so that these middle links will be made unavailable to other multicast connections. The control then returns to act **1010**, so that acts **1010**, **1020**, **1030**, **1040**, **1050**, **1060**, **1070**, **1080**, and **1090** are executed in a loop, for each connection request until the connections are set up.

In the example illustrated in FIG. **1**A, four outgoing middle links are available to satisfy a multicast connection request if input switch is IS**2**, but only at most two outgoing middle links of the input switch will be used in accordance with this method. Similarly, although three outgoing middle links is available for a multicast connection request if the input switch is IS**1**, again only at most two outgoing middle links is used. The specific outgoing middle links of the input switch that are chosen when selecting two outgoing middle links of the input switch is irrelevant to the method of FIG. **7**A so long as at most two outgoing middle links of the input switch are selected to ensure that the connection request is satisfied, i.e. the destination switches identified by the connection request can be reached from the outgoing middle links of the input switch that are selected. In essence, limiting the outgoing middle links of the input switch to no more than two permits the network $V_{mlink}(N_1, N_2, d, s)$ and the network $V(N_1, N_2, d, s)$ to be operated in nonblocking manner in accordance with the invention.

According to the current invention, using the method **1040** of FIG. **7**A, the network $V_{mlink}(N_1, N_2, d, s)$ and the networks $V(N_1, N_2, d, s)$ are operated in rearrangeably nonblocking for unicast connections when $s \geqq 1$, are operated in strictly nonblocking for unicast connections when $s \geqq 2$, and are operated in rearrangeably nonblocking for multicast connections when $s \geqq 2$.

The connection request of the type described above in reference to method **1000** of FIG. **7**A can be unicast connection request, a multicast connection request or a broadcast connection request, depending on the example. In case of a unicast connection request, only one outgoing middle link of the input switch is used to satisfy the request. Moreover, in method **1000** described above in reference to FIG. **7**A any number of middle links may be used between any two stages excepting between the input stage and middle stage **130**, and also any arbitrary fan-out may be used within each output stage switch, to satisfy the connection request.

As noted above method **1000** of FIG. **7**A can be used to setup multicast connections, unicast connections, or broadcast connection of all the networks $V_{mlink}(N, d, s)$, $V_{mlink}(N_1, N_2, d, s)$, $V(N, d, s)$ and $V(N_1, N_2, d, s)$ disclosed in this invention.

Applications Embodiments:

All the embodiments disclosed in the current invention are useful in many varieties of applications. FIG. **8A1** illustrates the diagram of **800A1** which is a typical two by two switch with two inlet links namely IL**1** and IL**2**, and two outlet links namely OL**1** and OL**2**. The two by two switch also implements four crosspoints namely CP(**1**,**1**), CP(**1**,**2**), CP(**2**,**1**) and CP(**2**,**2**) as illustrated in FIG. **8A1**. For example the diagram of **800A1** may the implementation of middle switch MS(**1**,**1**) of the diagram **400**A of FIG. **4**A where inlet link IL**1** of diagram **800A1** corresponds to middle link ML(**1**,**1**) of diagram **400**A, inlet link IL**2** of diagram **800A1** corresponds to middle link ML(**1**,**5**) of diagram **400**A, outlet link OL**1** of diagram **800A1** corresponds to middle link ML(**2**,**1**) of diagram **400**A, outlet link OL**2** of diagram **800A1** corresponds to middle link ML(**2**,**2**) of diagram **400**A.

1) Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in programmable integrated circuit applications. FIG. **8A2** illustrates the detailed diagram **800A2** for the implementation of the diagram **800A1** in programmable integrated circuit embodiments. Each crosspoint is implemented by a transistor coupled between the corresponding inlet link and outlet link, and a programmable cell in programmable integrated circuit embodiments. Specifically crosspoint CP(**1**,**1**) is implemented by transistor C(**1**,**1**) coupled between inlet link IL**1** and outlet link OL**1**, and programmable cell P(**1**,**1**); crosspoint CP(**1**,**2**) is implemented by transistor C(**1**,**2**) coupled between inlet link IL**1** and outlet link OL**2**, and programmable cell P(**1**,**2**); crosspoint CP(**2**,**1**) is implemented by transistor C(**2**,**1**) coupled between inlet link IL**2** and outlet link OL**1**, and programmable cell P(**2**,**1**); and crosspoint CP(**2**,**2**) is implemented by transistor C(**2**,**2**) coupled between inlet link IL**2** and outlet link OL**2**, and programmable cell P(**2**,**2**).

If the programmable cell is programmed ON, the corresponding transistor couples the corresponding inlet link and outlet link. If the programmable cell is programmed OFF, the corresponding inlet link and outlet link are not connected. For example if the programmable cell P(**1**,**1**) is programmed ON, the corresponding transistor C(**1**,**1**) couples the corresponding inlet link IL**1** and outlet link OL**1**. If the programmable cell P(**1**,**1**) is programmed OFF, the corresponding inlet link IL**1** and outlet link OL**1** are not connected. In volatile programmable integrated circuit embodiments the programmable cell may be an SRAM (Static Random Address Memory) cell. In non-volatile programmable integrated circuit embodiments the programmable cell may be a Flash memory cell. Also the programmable integrated circuit embodiments may implement field programmable logic arrays (FPGA) devices, or programmable Logic devices (PLD), or Application Specific Integrated Circuits (ASIC) embedded with programmable logic circuits or 3D-FPGAs.

2) One-time Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in one-time programmable integrated circuit applications. FIG. **8A3** illustrates the detailed diagram **800A3** for the implementation of the diagram **800A1** in one-time programmable integrated circuit embodiments. Each crosspoint is implemented by a via coupled between the corresponding inlet link and outlet link in one-time programmable integrated circuit embodiments. Specifically crosspoint CP(**1**,**1**) is implemented by via V(**1**,**1**) coupled between inlet link IL**1** and outlet link OL**1**; crosspoint CP(**1**,**2**) is implemented by via V(**1**,**2**) coupled between inlet link IL**1** and outlet link OL**2**; crosspoint CP(**2**,**1**) is implemented by via V(**2**,**1**) coupled between inlet link IL**2** and outlet link OL**1**; and crosspoint CP(**2**,**2**) is implemented by via V(**2**,**2**) coupled between inlet link IL**2** and outlet link OL**2**.

If the via is programmed ON, the corresponding inlet link and outlet link are permanently connected which is denoted by thick circle at the intersection of inlet link and outlet link. If the via is programmed OFF, the corresponding inlet link and outlet link are not connected which is denoted by the absence of thick circle at the intersection of inlet link and outlet link. For example in the diagram **800A3** the via V(**1**,**1**) is programmed ON, and the corresponding inlet link IL**1** and outlet link OL**1** are connected as denoted by thick circle at the intersection of inlet link IL**1** and outlet link OL**1**; the via V(**2**,**2**) is programmed ON, and the corresponding inlet link IL**2** and outlet link OL**2** are connected as denoted by thick circle at the intersection of inlet link IL**2** and outlet link OL**2**; the via V(**1**,**2**) is programmed OFF, and the corresponding inlet link IL**1** and outlet link OL**2** are not connected as denoted by the absence of thick circle at the intersection of inlet link IL**1** and outlet link OL**2**; the via V(**2**,**1**) is programmed OFF, and the corresponding inlet link IL**2** and outlet link OL**1** are not connected as denoted by the absence of thick circle at the intersection of inlet link IL**2** and outlet link OL**1**. One-time programmable integrated circuit embodiments may be anti-fuse based programmable integrated circuit devices or mask programmable structured ASIC devices.

3) Integrated Circuit Placement and Route Embodiments:

All the embodiments disclosed in the current invention are useful in Integrated Circuit Placement and Route applications, for example in ASIC backend Placement and Route tools. FIG. **8A4** illustrates the detailed diagram **800A4** for the implementation of the diagram **800A1** in Integrated Circuit Placement and Route embodiments. In an integrated circuit since the connections are known a-priori, the switch and crosspoints are actually virtual. However the concept of virtual switch and virtal crosspoint using the embodiments disclosed in the current invention reduces the number of required wires, wire length needed to connect the inputs and outputs of different netlists and the time required by the tool for placement and route of netlists in the integrated circuit.

Each virtual crosspoint is used to either to hardwire or provide no connectivity between the corresponding inlet link and outlet link. Specifically crosspoint CP(**1**,**1**) is implemented by direct connect point DCP(**1**,**1**) to hardwire (i.e., to permanently connect) inlet link IL**1** and outlet link OL**1** which is denoted by the thick circle at the intersection of inlet link IL**1** and outlet link OL**1**; crosspoint CP(**2**,**2**) is implemented by direct connect point DCP(**2**,**2**) to hardwire inlet link IL**2** and outlet link OL**2** which is denoted by the thick circle at the intersection of inlet link IL**2** and outlet link OL**2**. The diagram **800A4** does not show direct connect point DCP (**1**,**2**) and direct connect point DCP(**1**,**3**) since they are not needed and in the hardware implementation they are eliminated. Alternatively inlet link IL**1** needs to be connected to outlet link OL**1** and inlet link IL**1** does not need to be connected to outlet link OL**2**. Also inlet link IL**2** needs to be connected to outlet link OL**2** and inlet link IL**2** does not need to be connected to outlet link OL**1**. Furthermore in the example of the diagram **800A4**, there is no need to drive the signal of inlet link IL**1** horizontally beyond outlet link OL**1** and hence the inlet link IL**1** is not even extended horizontally until the outlet link OL**2**. Also the absence of direct connect point DCP(**2**,**1**) illustrates there is no need to connect inlet link IL**2** and outlet link OL**1**.

In summary in integrated circuit placement and route tools, the concept of virtual switches and virtual cross points is used during the implementation of the placement & routing algorithmically in software, however during the hardware implementation cross points in the cross state are implemented as hardwired connections between the corresponding inlet link and outlet link, and in the bar state are implemented as no connection between inlet link and outlet link

3) More Application Embodiments:

All the embodiments disclosed in the current invention are also useful in the design of SoC interconnects, Field programmable interconnect chips, parallel computer systems and in time-space-time switches.

Numerous modifications and adaptations of the embodiments, implementations, and examples described herein will be apparent to the skilled artisan in view of the disclosure.

What is claimed is:

1. A network having a plurality of multicast connections, said network comprising:

N_1 inlet links and N_2 outlet links, where $N_1>1$, $N_2>1$ and when $N_2>N_1$ and $N_2=p*N_1$ where $p>1$ then $N_1=N$, $d_1=d$, and

$$d_2 = N_2 \times \frac{d}{N_1} = p \times d;$$

where $N>1$, $d_1>1$, $d_2>1$, $d>1$ and an input stage comprising

$$\frac{N_1}{d}$$

input switches, and said each input switch comprising d inlet links and each said input switch further comprising x×d outgoing links connecting to switches in a second stage where x>0; and

an output stage comprising

$$\frac{N_1}{d}$$

output switches, and said each output switch comprising d_2 outlet links and each said output switch further comprising

$$x \times \frac{(d + d_2)}{2}$$

incoming links connecting from switches in a penultimate stage; and

a plurality of y middle stages comprising N/d middle switches in each of said y middle stages wherein said second stage and said penultimate stage are one of said middle stages where y>3, and

said each middle switch in all said middle stages excepting said penultimate stage comprising x×d incoming links (hereinafter "incoming middle links") connecting from switches in its immediate preceding stage, and said each middle switch further comprising x×d outgoing links (hereinafter "outgoing middle links") connecting to switches in its immediate succeeding stage; and

said each middle switch in said penultimate stage comprising x×d incoming links connecting from switches in its said immediate preceding stage, and said each middle switch further comprising

$$x \times \frac{(d + d_2)}{2}$$

outgoing links connecting to switches in its said immediate succeeding stage i.e., said output stage; or

when $N_1>N_2$ and $N_1=p*N_2$ where p>1 then $N_2=N$, $d_2=d$ and

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d$$

and

an input stage comprising

$$\frac{N_2}{d}$$

input switches, and said each input switch comprising d_1 inlet links and said each input switch further comprising

$$x \times \frac{(d + d_1)}{2}$$

outgoing links connecting to switches in a second stage where x>0; and

an output stage comprising

$$\frac{N_2}{d}$$

output switches, and said each output switch comprising d outlet links and said each output switch further comprising x×d incoming links connecting from switches in a penultimate stage; and

a plurality of y middle stages comprising N/d middle switches in each of said y middle stages wherein said second stage and said penultimate stage are one of said middle stages where y>3, and

said each middle switch in said second stage comprising

$$x \times \frac{(d + d_1)}{2}$$

incoming links connecting from switches in its immediate preceding stage i.e., said input stage, and said each middle switch further comprising x×d outgoing links connecting to switches in its immediate succeeding stage; and

said each middle switch in all said middle stages excepting said second stage comprising x×d incoming links (hereinafter "incoming middle links") connecting from switches in its immediate preceding stage, and said each middle switch further comprising x×d outgoing links (hereinafter "outgoing middle links") connecting to switches in its said immediate succeeding stage; and

wherein said each multicast connection from an inlet link passes through at most two outgoing links in said input switch, and said multicast connection further passes through a plurality of outgoing links in a plurality switches in each said middle stage and in said output stage.

2. The network of claim **1**, wherein all said incoming middle links and outgoing middle links are connected in any arbitrary topology such that when no connections are setup in said network, a connection from any said inlet link to any said outlet link can be setup.

3. The network of claim **2**, wherein $y \geqq (2\times\log_d N)-3$ when $N_2>N_1$, and $y \geqq (2\times\log_d N_2)-3$ when $N_1>N_2$.

4. The network of claim **3**, wherein $x \geqq 1$, wherein said each multicast connection comprises only one destination link, and

said each multicast connection from an inlet link passes through only one outgoing link in input switch, and said multicast connection further passes through only one outgoing link in one of the switches in each said middle stage and in said output stage, and

further is always capable of setting up said multicast connection by changing the path, defined by passage of an existing multicast connection, thereby to change only one outgoing link of the input switch used by said existing multicast connection, and said network is hereinafter "rearrangeably nonblocking network for unicast".

5. The network of claim **3**, wherein $x \geqq 2$, wherein said each multicast connection comprises only one destination link, and

said each multicast connection from an inlet link passes through only one outgoing link in input switch, and said multicast connection further passes through only one outgoing link in one of the switches in each said middle stage and in said output stage, and

further is always capable of setting up said multicast connection by never changing path of an existing multicast connection, wherein said each multicast connection comprises only one destination link and the network is hereinafter "strictly nonblocking network for unicast".

6. The network of claim **3**, wherein $x \geqq 2$,

further is always capable of setting up said multicast connection by changing the path, defined by passage of an existing multicast connection, thereby to change one or two outgoing links of the input switch used by said existing multicast connection, and said network is hereinafter "rearrangeably nonblocking network".

7. The network of claim **3**, wherein $x \geqq 3$,

further is always capable of setting up said multicast connection by never changing path of an existing multicast connection, and the network is hereinafter "strictly nonblocking network".

8. The network of claim **1**, further comprising a controller coupled to each of said input, output and middle stages to set up said multicast connection.

9. The network of claim **1**, wherein said N_1 inlet links and N_2 outlet links are the same number of links, i.e., $N_1=N_2=N$, and $d_1=d_2=d$.

10. The network of claim **1**, wherein said each input switch, said each output switch and said each middle switch is either fully populated or partially populated.

11. The network of claim **1**,

wherein each of said input switches, or each of said output switches, or each of said middle switches further recursively comprise one or more networks.

12. A method for setting up one or more multicast connections in a network having N_1 inlet links and N_2 outlet links, where $N_1>1$, $N_2>1$ and

when $N_2>N_1$ and $N_2=p*N_1$ where $p>1$ then $N_1=N$, $d_1=d$, and

$$d_2 = N_2 \times \frac{d}{N_1} = p \times d;$$

where $N>1$, $d_1>1$, $d_2>1$, $d>1$ and having

an input stage having

$$\frac{N_1}{d}$$

input switches, and said each input switch having d inlet links and said each input switch further having $x \times d$ outgoing links connected to switches in a second stage where $x>0$; and

an output stage having

$$\frac{N_1}{d}$$

output switches, and said each output switch having d_2 outlet links and said each output switch further having

$$x \times \frac{(d + d_2)}{2}$$

incoming links connected from switches in a penultimate stage; and

a plurality of y middle stages having N/d middle switches in each of said y middle stages wherein said second stage and said penultimate stage being one of said middle stages where $y>3$, and

said each middle switch in all said middle stages excepting said penultimate stage having $x \times d$ incoming links connected from switches in its immediate preceding stage, and said each middle switch further having $x \times d$ outgoing links connected to switches in its immediate succeeding stage; and

said each middle switch in said penultimate stage having $x \times d$ incoming links connected from switches in its said immediate preceding stage, and said each middle switch further having

$$x \times \frac{(d + d_2)}{2}$$

outgoing links connected to switches in its said immediate succeeding stage; or

when $N_1>N_2$ and $N_1=p*N_2$ where $p>1$ then $N_2=N$, $d_2=d$ and

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d;$$

and having

an input stage having

$$\frac{N_2}{d}$$

input switches, and said each input switch having d_1 inlet links and said each input switch further having

$$x \times \frac{(d + d_1)}{2}$$

outgoing links connected to switches in a second stage where $x>0$; and

an output stage having output

$$\frac{N_2}{d}$$

switches, and said each output switch having d outlet links and said each output switch further having $x \times d$ incoming links connected from switches in a penultimate stage; and

a plurality of y middle stages having N/d middle switches in each of said y middle stages wherein said second stage and said penultimate stage being one of said middle stages where $y>3$, and

said each middle switch in said second stage having

$$x \times \frac{(d + d_1)}{2}$$

incoming links connected from switches in its immediate preceding stage, and said each middle switch further having x×d outgoing links connected to switches in its said immediate succeeding stage; and

said each middle switch in all said middle stages excepting said second stage having x×d incoming links connected from switches in its immediate preceding stage, and said each middle switch further having x×d outgoing links connected to switches in its immediate succeeding stage; and said method comprising:

receiving a multicast connection at said input stage;

fanning out said multicast connection through at most two outgoing links in said input switch and a plurality of outgoing links in a plurality of middle switches in each said middle stage to set up said multicast connection to a plurality of output switches among said

$$\frac{N_2}{d}$$

output switches, wherein said plurality of output switches are specified as destinations of said multicast connection, wherein said at most two outgoing links in input switch and said plurality of outgoing links in said plurality of middle switches in each said middle stage are available.

13. A method of claim **12** wherein said act of fanning out is performed without changing any existing connection to pass through another set of plurality of middle switches in each said middle stage.

14. A method of claim **12** wherein said act of fanning out is performed recursively.

15. A method of claim **12** wherein a connection exists through said network and passes through a plurality of middle switches in each said middle stage and said method further comprises:

if necessary, changing said connection to pass through another set of plurality of middle switches in each said middle stage, act hereinafter "rearranging connection".

16. A method of claim **12** wherein said acts of fanning out and rearranging are performed recursively.

17. A method for setting up one or more multicast connections in a network having N_1 inlet links and N_2 outlet links, where $N_1>1$, $N_2>1$ and

when $N_2>N_1$ and $N_2=p*N_1$ where $p>1$ then $N_1=N$, $d_1=d$, and

$$d_2 = N_2 \times \frac{d}{N_1} = p \times d;$$

where $N>1$, $d_1>1$, $d_2>1$, $d>1$ and having

an input stage having

$$\frac{N_1}{d}$$

input switches, and said each input switch having d inlet links and said each input switch further having x×d outgoing links connected to switches in a second stage where x>0; and

an output stage having

$$\frac{N_1}{d}$$

output switches, and said each output switch having d_2 outlet links and said each output switch further having

$$x \times \frac{(d + d_2)}{2}$$

incoming links connected from switches in a penultimate stage; and

a plurality of y middle stages having N/d middle switches in each of said y middle stages wherein said second stage and said penultimate stage being one of said middle stages where y>3, and

said each middle switch in all said middle stages excepting said penultimate stage having x×d incoming links connected from switches in its immediate preceding stage, and said each middle switch further having x×d outgoing links connected to switches in its immediate succeeding stage; and

said each middle switch in said penultimate stage having x×d incoming links connected from switches in its said immediate preceding stage, and said each middle switch further having

$$x \times \frac{(d + d_2)}{2}$$

outgoing links connected to switches in its said immediate succeeding stage; or

when $N_1>N_2$ and $N_1=p*N_2$ where $p>1$ then $N_2=N$, $d_2=d$ and

$$d_1 = N_1 \times \frac{d}{N_2} = p \times d;$$

and having

an input stage having

$$\frac{N_2}{d}$$

input switches, and said each input switch having d_1 inlet links and said each input switch further having

$$x \times \frac{(d + d_1)}{2}$$

outgoing links connected to switches in a second stage where x>0; and

an output stage having

$$\frac{N_2}{d}$$

output switches, and said each output switch having d outlet links and said each output switch further having x×d incoming links connected from switches in a penultimate stage; and a plurality of y middle stages having N/d middle switches in each of said y middle stages wherein said second stage and said penultimate stage being one of said middle stages where y>3, and

said each middle switch in said second stage having

$$x \times \frac{(d + d_1)}{2}$$

incoming links connected from switches in its immediate preceding stage, and said each middle switch further having x×d outgoing links connected to switches in its immediate succeeding stage; and

said each middle switch in all said middle stages excepting said second stage having x×d incoming links connected from switches in its immediate preceding stage, and said each middle switch further having x×d outgoing links connected to switches in its immediate succeeding stage; and said method comprising:

checking if a first outgoing link in input switch and a first plurality of outgoing links in plurality of middle switches in each said middle stage are available to at least a first subset of destination output switches of said multicast connection; and

checking if a second outgoing link in input switch and second plurality of outgoing links in plurality of middle switches in each said middle stage are available to a second subset of destination output switches of said multicast connection,

wherein each destination output switch of said multicast connection is one of said first subset of destination output switches and said second subset of destination output switches.

18. The method of claim **17** further comprising:

prior to said checkings, checking if all the destination output switches of said multicast connection are available through said first outgoing link in input switch and said first plurality of outgoing links in plurality of middle switches in each said middle stage.

19. The method of claim **17** further comprising:

repeating said checkings of available second outgoing link in input switch and second plurality of outgoing links in plurality of middle switches in each said middle stage to a second subset of destination output switches of said multicast connection to each outgoing link in input switch other than said first and said second outgoing links in input switch,

wherein each destination output switch of said multicast connection is one of said first subset of destination output switches and said second subset of destination output switches.

20. The method of claim **17** further comprising:

repeating said checkings of available first outgoing link in input switch and first plurality of outgoing links in plurality of middle switches in each said middle stage to a first subset of destination output switches of said multicast connection to each outgoing link in input switch other than said first outgoing link in input switch.

21. The method of claim **17** further comprising:

setting up each of said multicast connection from its said input switch to its said output switches through not more than two outgoing links, selected by said checkings, by fanning out said multicast connection in its said input switch into not more than said two outgoing links.

22. The method of claim **17** wherein any of said acts of checking and setting up are performed recursively.

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