

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Application Number	16/562,450 -- GAU: 2464
		Filing Date	09-06-2019
		First Named Inventor	Venkat Konda
		Art Unit	
		Examiner Name	
		Attorney Docket Number	V-0060US
Sheet	1	of	1

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	1	US- 8269523-b2	09-18-2012	Venkat Konda	all FIGs
	2	US- 8898611-b2	11-25-2014	Venkat Konda	all FIGs
	3	US- 9529958-b2	12-27-2016	Venkat Konda	all FIGs
	4	US- 8270400-b2	09-18-2012	Venkat Konda	all FIGs
	5	US- 8170040-b2	05-01-2012	Venkat Konda	all FIGs
	6	US- 8363649-b2	01-29-2013	Venkat Konda	all FIGs
	7	US- 6185220-b1	02-06-2001	Muthukrishnan et. al.	layout FIGs
	8	US- 6940308-b2	09-06-2005	Wong	layout FIGs
	9	US- 5451936	09-19-1995	Yang et. al.	layout FIGs
Change(s) applied to document, /C.C.B./ 1/26/2021	10	US- 5153843 10/1992	10-00-1992	Kenneth E. Batchner	layout FIGs
	11	US- 6018523	01-25-2000	Shimon Even	layout FIGs
	12	US-			
	13	US-			
	14	US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				

Examiner Signature	/RASHEED GIDADO/	Date Considered	08/03/2020
--------------------	------------------	-----------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.
 This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
 If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.G/

FLEX LOGIX EXHIBIT 1055 (Part 1 of 2)
 Flex Logix Technologies v. Venkat Konda
 IPR2020-00260

PART B – FEE(S) TRANSMITTAL

Complete and send this form, together with the applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

By fax, send to: (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Konda Technologies Inc
6278 Grand Oak Way
San Jose, CA 95135

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
16/562,450	09-06-2019	Venkat Konda	V-0060US	6438

TITLE OF INVENTION:

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
Nonprovisional	SMALL	\$600	\$0	\$0	\$600	02/18/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363)

Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

"Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1.

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2.

3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE or COUNTRY)

Konda Technologies Inc.

San Jose, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): Individual Corporation or other private group entity Government

4a. Fees Submitted: Issue Fee Publication Fee (if required) Advance Order - # of Copies _____

4b. Method of Payment (Please first reapply any previously paid fee shown above):

Electronic Payment via EFS-Web Enclosed check Non-electronic payment by credit card (Attach form PTO-2038)

The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change of Entity Status (from status indicated above)

Applicant certifying micro entity status. See 37 CFR 1.29.

NOTE: Absent a valid Certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

Applicant asserting small entity status. See 37 CFR 1.27.

NOTE: If the application was previously under micro entity status, checking this box will be taken as a notification of loss of entitlement to micro entity status.

Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken as a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature **/Venkat Konda/**

Date **02-14-2021**

Typed or printed name **Venkat Konda**

Registration No.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	16562450			
Filing Date:	06-Sep-2019			
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS			
First Named Inventor/Applicant Name:	Venkat Konda			
Filer:	Venkat Konda			
Attorney Docket Number:	V-0060US			
Filed as Small Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	2501	1	600	600

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				600

Electronic Acknowledgement Receipt

EFS ID:	41920445
Application Number:	16562450
International Application Number:	
Confirmation Number:	6438
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkat Konda
Filer Authorized By:	
Attorney Docket Number:	V-0060US
Receipt Date:	14-FEB-2021
Filing Date:	06-SEP-2019
Time Stamp:	15:24:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$600
RAM confirmation Number	E20212DF26053442
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

--	--	--	--	--	--

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	ptol85b-V0060.pdf	269957	no	2
			8b63080f2fb5c95ff0e83f8fc38b2f439531ffa2		

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30057	no	2
			22d81dbfc8bf6d0257b493545f421511639c37d99		

Warnings:

Information:

Total Files Size (in bytes):	300014
-------------------------------------	--------

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO. Includes details for application 16/562,450 filed 09/06/2019 by Venkat Konda.

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

venkat@kondatech.com
vkonda@gmail.com

Response to Rule 312 Communication	Application No. 16/562,450	Applicant(s) Konda, Venkat	
	Examiner RASHEED GIDADO	Art Unit 2464	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. The amendment filed on 21 January 2021 under 37 CFR 1.312 has been considered, and has been:
- a) entered.
 - b) entered as directed to matters of form not affecting the scope of the invention.
 - c) disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.
 - d) disapproved. See explanation below.
 - e) entered in part. See explanation below.

/RASHEED GIDADO/
Primary Examiner, Art Unit 2464

Electronic Acknowledgement Receipt

EFS ID:	41819578
Application Number:	16562450
International Application Number:	
Confirmation Number:	6438
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkat Konda
Filer Authorized By:	
Attorney Docket Number:	V-0060US
Receipt Date:	03-FEB-2021
Filing Date:	06-SEP-2019
Time Stamp:	01:08:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment after Notice of Allowance (Rule 312)	Amnd-after-allow-V_0060.pdf	217256 <small>ebcd7129754161ef49e2db6ee539308b8ae4b846</small>	no	20

Warnings:

Information:	
Total Files Size (in bytes):	217256
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>	

Application Number: 16/562,450

Art Unit: 2464

AMENDMENT AFTER ALLOWANCE UNDER RULE 312

In The United States Patent And Trademark Office

Application Number: 16/562,450

Application Filed: 9/6/2019

5 Applicant(s): Venkat Konda

Title: Fast Scheduling and Optimization of Multi-stage Hierarchical Networks

Examiner/Art Unit: Rasheed Gidado / 2464

San Jose, 2020 February 3, Wed

10 **AMENDMENT AFTER ALLOWANCE UNDER RULE 312**

Mail Stop Amendment

Commissioner for Patents

P.O. Box 1450

15 Alexandria, Virginia, 22313-1450

Dear Sir/Madam:

This replies to the Notice of Allowance and Fee(s) Due from the United States
Patent and Trademark Office mailed on November 18, 2020 in connection with the
20 above-identified patent application. Pursuant to Rule 312, applicant respectfully requests
that the above application be amended as follows:

Application Number: 16/562,450

Art Unit: 2464

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Amendments to the Claims:

Applicant sincerely acknowledges the allowance of claims 1 - 20 with appreciation.

Claims: Claims 1 – 20 are amended to clarify and they do not change the scope of the
5 previously allowed claims:

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Claims

What is claimed is:

1. (Currently Amended): A multi-stage hierarchical network comprising:

a plurality of partial multi-stage networks, ~~each partial multi-stage network of said~~
 5 ~~plurality of partial multi-stage networks comprising a plurality of inlet links and a~~
~~plurality of outlet links, and said plurality of partial multi-stage networks arranged in a~~
~~two-dimensional grid of having a plurality of rows and a plurality of columns; and~~
~~each partial multi-stage network of said plurality of partial multi-stage networks further~~
~~comprising one or more slices, each slice of said one or more slices further comprising~~
 10 ~~one or more rings, each ring of said one or more rings further comprising y stages, where~~
 ~~$y \geq 2$; and~~

each stage of said y stages comprising at least one switch of size $d_i \times d_o$, where $d_i \geq 2$
 and $d_o \geq 2$, ~~and each switch of said at least one switch of size $d_i \times d_o$ having d_i~~
~~incoming links and d_o outgoing links; and, each switch of said at least one switch of size~~
 15 ~~$d_i \times d_o$ further comprising a plurality of multiplexers of size $d \geq 2$ with each multiplexer~~
~~of said plurality of multiplexers comprising d inputs and one output; and~~

wherein said at least one switch of size $d_i \times d_o$ comprises ~~either only one of a) a forward~~
~~switch, or only a backward switch, or b) both a forward switch and a backward U-turn~~
~~switch, or c) a forward switch, a backward switch and a U-turn switch, or a forward~~
 20 ~~switch, a backward switch and a U-turn switch without 180 degree turn paths or d) a~~
~~forward switch, a backward switch, a U-turn switch and a reverse U-turn switch or e) a~~
~~forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without~~
~~180 180-degree turn paths, or an integrated switch of a forward switch, a backward~~
~~switch and U-turn switch, or an integrated switch of a forward switch, a backward switch~~
 25 ~~and a U-turn switch without 180 degree turn paths or an integrated switch of a forward~~
~~switch, a backward switch, a U-turn switch and a reverse U-turn switch or and f) an~~

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

integrated switch ~~of comprising~~ a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without ~~180~~ 180-degree turn paths; and

wherein said d_i incoming links and said d_o outgoing links comprise ~~comprises a~~ plurality of one or more internal connections and a plurality of one or more hop wires; and where said plurality of one or more hop wires ~~further comprising~~ comprise a plurality of one or more internal hop wires or a plurality of one or more external hop wires; and

wherein each outlet link of said plurality of outlet links is connected to the output of a first multiplexer ~~one~~ of said plurality of multiplexers of a first ~~one~~ switch of said at least one switch of size $d_i \times d_o$ of a first ~~one~~ stage of said y stages of a first ~~one~~ partial multi-stage network of said plurality of partial multi-stage networks, and each inlet link of said plurality of inlet links is connected to ~~one of the~~ a first input of said d_i inputs of one or more multiplexers of said plurality of multiplexers of one or more ~~said~~ switches of said at least one switch of size $d_i \times d_o$ of one or more ~~said~~ stages of said y stages of one or more partial multi-stage networks of said plurality of partial multi-stage networks; and

wherein a first partial multi-stage network of said plurality of partial multi-stage networks ~~comprising~~ comprises one of a) a the same number of and b) a different number of said plurality of inlet links as a second partial multi-stage network of said plurality of partial multi-stage networks; and a first partial multi-stage network of said plurality of partial multi-stage networks ~~comprising~~ comprises one of a) a the same number of and b) a different number of said plurality of outlet links as a second partial multi-stage network of said plurality of partial multi-stage networks; a first partial multi-stage network of said plurality of partial multi-stage networks ~~comprising~~ comprises one of a) a the same number of and b) a different number of said one or more slices as a second partial multi-stage network of said plurality of partial multi-stage networks; a first slice of said one or more slices ~~comprising~~ comprises one of a) a the same number of and b) a different number of said one or more rings as a second slice of said one or more slices; a first ring of said one or more rings ~~comprising~~ comprises one of a) a the same number of and b) a different number of said y stages as a second ring of said one or more rings; and a first stage of said y stages ~~comprising~~ comprises one of a) a the same number of and b) a

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

different number of said at least one switch of size $d_i \times d_0$ as a second stage of said y stages; a first switch of said at least one switch of size $d_i \times d_0$ is one of a) a the same size ~~or~~ and b) a different size as a second switch of said at least one switch of size $d_i \times d_0$; and a first multiplexer in said plurality of multiplexers of size $d \geq 2$ is one of a) a the same
 5 size or and b) a different size as a second multiplexer in said plurality of multiplexers of size $d \geq 2$; and

wherein each internal connection of said ~~plurality of one or more~~ internal connections connected from the output of a first multiplexer of said plurality of multiplexers of a first switch of said at least one switch of size $d_i \times d_0$ of a first stage of said y stages of a first
 10 ring of said one or more rings to a first input of said d inputs of a second multiplexer of said plurality of multiplexers of a second switch of said at least one switch of size $d_i \times d_0$ of a second stage of said y stages of the first ring of said one or more rings; and

wherein each internal hop wire of said ~~plurality of one or more~~ internal hop wires is connected from the output of a multiplexer of said plurality of multiplexers of a switch of
 15 said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a first ring of said one or more rings of a first slice of said one or more slices to a first input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_0$ of one or more stages of said y stages of one or more rings different from the first ring of said one or more rings of the ~~same~~ first slice of
 20 said one or more slices; and

wherein each external hop wire of said ~~plurality of one or more~~ external hop wires is connected from the output a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a ring of said one or more rings of a slice of said one or more slices of a first partial multi-stage network of
 25 said plurality of partial multi-stage networks to an input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_0$ of one or more stages of said y stages of said one or more rings of a slice of said one or more slices of one or more partial multi-stage networks different

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

from the first partial multi-stage network of said plurality of partial multi-stage networks;
and

wherein one or more external hop wires of said ~~plurality of one or more~~ external hop wires are ~~either~~ one of a) connected between one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_0$ in same ~~numbered~~ stages of said y stages in three or more partial multi-stage networks of said plurality of partial multi-stage networks (hereinafter “multi-drop hop wires”) ~~or~~ and b) connected between one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_0$ in different ~~numbered~~ stages of said y stages; in three or more partial multi-stage networks of said plurality of partial multi-stage networks (hereinafter “multi-drop hop wires”).

2. (Currently Amended): The multi-stage hierarchical network of claim 1, wherein said ~~plurality of one or more~~ external hop wires are connected vertically (hereinafter “vertical wires” or “vertical external hop wires”), or horizontally (hereinafter “horizontal wires” or “horizontal external hop wires”); and

each partial multi-stage network of said plurality of partial multi-stage networks comprising said one or more slices is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or

each partial multi-stage network of said plurality of partial multi-stage networks comprising said horizontal wires and said vertical wires is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or

each partial multi-stage network of said plurality of partial multi-stage networks comprising both said one or more slices, and said horizontal wires and said vertical wires is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid.

3. (Currently Amended): The multi-stage hierarchical network of claim 1, wherein said ~~plurality of one or more~~ external hop wires are ~~cascade~~ interconnected through only

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

one multiplexer of said plurality of multiplexers at each switch of said at least one switch of size $d_i \times d_0$.

4. (Currently Amended): The multi-stage hierarchical network of claim 1, wherein said one or more external hop wires of said ~~plurality of~~ one or more external hop wires are
 5 connected between at least one same ~~numbered~~ stage in all said plurality of partial multi-stage networks, or

one or more external hop wires of said ~~plurality of~~ one or more external hop wires are connected between at least two ~~not same different~~ numbered stages of said y stages in all said plurality of partial multi-stage networks; or

- 10 said ~~plurality of~~ one or more external hop wires are all connected between same ~~numbered~~ stages of said y stages in all stages of said y stages of all said plurality of partial multi-stage networks.

5. (Currently Amended): The multi-stage hierarchical network of claim 1, wherein each multiplexer of said plurality of multiplexers of size $d \geq 2$ is of size $d = 4$ or ~~$d \geq 4$~~ $d \geq 4$.
 15

6. (Currently Amended): The multi-stage hierarchical network of claim 1, wherein ~~one or more of external hop wires of~~ said ~~plurality of~~ one or more external hop wires are implemented in two or more metal layers, or

each multiplexer of said plurality of multiplexers of size $d \geq 2$ is configurable by
 20 Static Random Address Memory SRAM cells or Flash memory Cells, or

said ~~plurality of~~ one or more external hop wires use a plurality of buffers to amplify signals driven through them; and said plurality of buffers are either inverting or non-inverting buffers, or

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

~~one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks comprising a switch of size $(d_i + m) \times (d_o + n)$, where $d_i \geq 2$, $d_o \geq 2$, $m \geq 0$, $n \geq 0$ or~~

one or more of said y stages in ~~one a first~~ partial multi-stage network of said plurality
 5 of partial multi-stage networks ~~comprising~~ comprise one of a) six 2:1 multiplexers, or
b) eight 2:1 multiplexers, or four 3:1 multiplexers, or and c) four 4:1 multiplexers.

7. (Currently Amended): The multi-stage hierarchical network of claim 1, wherein said at least one switch of size $d_i \times d_o$ of said y stages are either fully populated or partially populated, or

10 said plurality of partial multi-stage networks are implemented in a 3D-FPGAs
~~integrated circuit device.~~

8. (Currently Amended): A programmable integrated circuit comprising:

a plurality of programmable logic blocks and a multi-stage hierarchical network, each
 programmable logic block of said plurality of programmable logic blocks comprising a
 15 plurality of inlet links and a plurality of outlet links, ~~and~~ said multi-stage hierarchical
 network comprising a plurality of partial multi-stage networks wherein each
 programmable logic block of said plurality of programmable logic blocks is coupled with
 at least one partial multi-stage network of said plurality of partial multi-stage networks, ~~and~~
 20 ~~and~~ said plurality of programmable logic blocks coupled with said plurality of partial
 multi-stage networks arranged in a two-dimensional grid ~~of~~ having a plurality of rows and
 a plurality of columns; and

each partial multi-stage network of said plurality of partial multi-stage networks ~~further~~
 comprising one or more slices, each slice of said one or more slices ~~further~~ comprising
 one or more rings, each ring of said one or more rings ~~further~~ comprising y stages, where
 25 $y \geq 2$; and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

each stage of said y stages comprising at least one switch of size $d_i \times d_o$, where $d_i \geq 2$ and $d_o \geq 2$, ~~and each switch of said at least one switch of size $d_i \times d_o$ having d_i incoming links and d_o outgoing links;~~ ~~and~~ each switch of said at least one switch of size $d_i \times d_o$ further comprising a plurality of multiplexers of size $d \geq 2$ with each multiplexer of said plurality of multiplexers comprising d inputs and one output; and

wherein said at least one switch of size $d_i \times d_o$ comprises ~~either only one of a) a forward switch, or only a backward switch, or b) both a forward switch and a backward U-turn switch, or c) a forward switch, a backward switch and a U-turn switch, or a forward switch, a backward switch and a U-turn switch without 180 degree turn paths or d) an integrated switch of a forward switch, a backward switch, U-turn switch, and a reverse U-turn switch, or e) a an integrated switch of a forward switch, a backward switch, U-turn switch, and a reverse U-turn switch without 180 180-degree turn paths; or an integrated switch of a forward switch, a backward switch and U-turn switch, or an integrated switch of a forward switch, a backward switch and a U-turn switch without 180 degree turn paths or an integrated switch of a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch or~~ and f) an integrated switch of comprising a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180 180-degree turn paths; and

wherein said d_i incoming links and said d_o outgoing links ~~comprise~~ ~~comprises~~ either a plurality of one or more internal connections, and a plurality of hop wires; and said plurality of hop wires further comprising a plurality of one or more internal hop wires, or a plurality of one or more external hop wires; and

wherein each inlet link of said plurality of inlet links is connected to the output of a first multiplexer ~~one~~ of said plurality of multiplexers of a first ~~one~~ switch of said at least one switch of size $d_i \times d_o$ of a first ~~one~~ stage of said y stages of a first ~~one~~ partial multi-stage network of said plurality of partial multi-stage networks, and each outlet link of said plurality of outlet links is connected to ~~one of the~~ a first input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more ~~said~~ switches of said at

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

least one switch of size $d_i \times d_0$ of one or more ~~said~~ stages of said y stages of one or more partial multi-stage networks of said plurality of partial multi-stage networks; and

wherein a first partial multi-stage network of said plurality of partial multi-stage networks ~~comprising~~ comprises one of a) a the same number ~~or~~ and b) a different number of said plurality of inlet links as a second partial multi-stage network of said plurality of partial multi-stage networks; and a first partial multi-stage network of said plurality of partial multi-stage networks ~~comprising~~ comprises one of a) a the same number ~~or~~ and b) a different number of said plurality of outlet links as a second partial multi-stage network of said plurality of partial multi-stage networks; a first partial multi-stage network of said plurality of partial multi-stage networks ~~comprising~~ comprises one of a) a the same number ~~or~~ and b) a different number of said one or more slices as a second partial multi-stage network of said plurality of partial multi-stage networks; a first slice of said one or more slices ~~comprising~~ comprises one of a) a the same number ~~or~~ and b) a different number of said one or more rings as a second slice of said one or more slices; a first ring of said one or more rings ~~comprising~~ comprises one of a) a the same number ~~or~~ and b) a different number of said y stages as a second ring of said one or more rings; and a first stage of said y stages ~~comprising~~ comprises one of a) a the same number ~~or~~ and b) a different number of said at least one switch of size $d_i \times d_0$ as a second stage of said y stages; a first switch of said at least one switch of size $d_i \times d_0$ is one of a) a the same size ~~or~~ and b) a different size as a second switch of said at least one switch of size $d_i \times d_0$; and a first multiplexer in said plurality of multiplexers of size $d \geq 2$ is one of a) a the same size ~~or~~ and b) a different size as a second multiplexer in said plurality of multiplexers of size $d \geq 2$; and

wherein each internal connection of said ~~plurality of one or more~~ internal connections connected from the output of a first multiplexer of said plurality of multiplexers of a first switch of said at least one switch of size $d_i \times d_0$ of a first stage of said y stages of a first ring of said one or more rings to a first input of said d inputs of a second multiplexer of said plurality of multiplexers of a second switch of said at least one switch of size $d_i \times d_0$ of a second stage of said y stages of the first ring of said one or more rings; and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

~~wherein~~ each internal hop wire of said ~~plurality of one or more~~ internal hop wires is
 connected from the output of a multiplexer of said plurality of multiplexers of a switch of
 said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a first ring of said
 one or more rings of a first slice of said one or more slices to a first input of said d inputs
 5 of one or more multiplexers of said plurality of multiplexers of one or more switches of
 said at least one switch of size $d_i \times d_0$ of one or more stages of said y stages of one or
 more rings different from the first ring of said one or more rings of the ~~same~~ first slice of
 said one or more slices; and

~~wherein~~ each external hop wire of said ~~plurality of one or more~~ external hop wires is
 10 connected from the output a multiplexer of said plurality of multiplexers of a switch of
 said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a ring of said one or
 more rings of a slice of said one or more slices of a first partial multi-stage network of
 said plurality of partial multi-stage networks to an input of said d inputs of one or more
 multiplexers of said plurality of multiplexers of one or more switches of said at least one
 15 switch of size $d_i \times d_0$ of one or more stages of said y stages of said one or more rings of
 a slice of said one or more slices of one or more partial multi-stage networks different
 from the first partial multi-stage network of said plurality of partial multi-stage networks;
 and

~~wherein~~ one or more external hop wires of said ~~plurality of one or more~~ external hop
 20 wires are ~~either one of a)~~ connected between multiplexers of said plurality of multiplexers
 of switches of said at least one switch of size $d_i \times d_0$ in same ~~numbered~~ stages of said y
 stages in three or more partial multi-stage networks of said plurality of partial multi-stage
 networks (hereinafter "multi-drop hop wires") ~~or and b)~~ connected between multiplexers
 of said plurality of multiplexers of switches of said at least one switch of size $d_i \times d_0$ in
 25 different ~~numbered~~ stages of said y stages, ~~when $y \geq 2$~~ , in three or more partial multi-
 stage networks of said plurality of partial multi-stage networks (hereinafter "multi-drop
 hop wires").

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

9. (Currently Amended): The programmable integrated circuit of claim 8 wherein said plurality of one or more external hop wires are connected vertically (hereinafter “vertical wires” or “vertical external hop wires”), or horizontally (hereinafter “horizontal wires” or “horizontal external hop wires”); and
- 5 each partial multi-stage network of said plurality of partial multi-stage networks comprising said one or more slices is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or
- each partial multi-stage network of said plurality of partial multi-stage networks comprising said horizontal wires and said vertical wires is replicated in either said
- 10 plurality of rows or said plurality of columns of the two-dimensional grid, or
- each partial multi-stage network of said plurality of partial multi-stage networks comprising both said one or more slices, and said horizontal wires and said vertical wires is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid.
- 15 10. (Currently Amended): The programmable integrated circuit of claim 8, wherein said plurality of one or more external hop wires are cascaded interconnected through only one multiplexer of said plurality of multiplexers at each switch of said at least one switch of size $d_i \times d_0$.
- 20 11. (Currently Amended): The programmable integrated circuit of claim 8, wherein said one or more external hop wires of said ~~plurality of~~ one or more external hop wires are connected between at least one same ~~numbered~~ stage in all said plurality of partial multi-stage networks, or
- one or more external hop wires of said ~~plurality of~~ one or more external hop wires are connected between at least two ~~not same~~ different ~~numbered~~ stages of said y stages in all
- 25 said plurality of partial multi-stage networks; or

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

said ~~plurality of~~ one or more external hop wires are all connected between same ~~numbered~~ stages of said y stages in all stages of said y stages of all said plurality of partial multi-stage networks.

12. (Currently Amended): The programmable integrated circuit of claim 8, wherein each
5 multiplexer of said plurality of multiplexers of size $d \geq 2$ is of size $d = 4$ or ~~$d \geq 4$~~ $d \geq 4$.

13. (Currently Amended): The programmable integrated circuit of claim 8, wherein one
or more ~~of~~ external hop wires of said ~~plurality of~~ one or more external hop wires are
implemented in two or more metal layers, or

10 each multiplexer of said plurality of multiplexers of size $d \geq 2$ is configurable by
Static Random Address Memory SRAM cells or Flash memory Cells, or

said ~~plurality of~~ one or more external hop wires use a plurality of buffers to amplify
signals driven through them; and said plurality of buffers are either inverting or non-
inverting buffers, or

15 ~~one or more stages of said y stages in one partial multi-stage network of said~~
~~plurality of partial multi-stage networks comprising a switch of size~~
 ~~$(d_i + m) \times (d_o + n)$, where $d_i \geq 2$, $d_o \geq 2$, $m \geq 0$, $n \geq 0$ or~~

one or more of said y stages in ~~one a first~~ partial multi-stage network of said plurality
of partial multi-stage networks ~~comprising~~ comprise one of a) six 2:1 multiplexers, or
20 b) eight 2:1 multiplexers, or four 3:1 multiplexers, or and c) four 4:1 multiplexers.

14. (Currently Amended): The programmable integrated circuit of claim 8, wherein said
at least one switch of size $d_i \times d_o$ of said y stages are either fully populated or
partially populated, or

25 said plurality of partial multi-stage networks are implemented in a 3D-FPGAs
~~integrated circuit device.~~

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

15. (Currently Amended): A programmable integrated circuit comprising:

a plurality of programmable logic blocks and a multi-stage hierarchical network, each programmable logic block of said plurality of programmable logic blocks comprising a plurality of inlet links and a plurality of outlet links; ~~and~~ said multi-stage hierarchical network comprising a plurality of partial multi-stage networks wherein each
 5 programmable logic block of said plurality of programmable logic blocks is coupled with at least one partial multi-stage network of said plurality of partial multi-stage networks; ~~and~~ said plurality of programmable logic blocks coupled with said plurality of partial multi-stage networks arranged in a two-dimensional grid ~~of~~ having a plurality of rows and
 10 a plurality of columns; and

each partial multi-stage network of said plurality of partial multi-stage networks ~~further~~ comprising one or more slices, each slice of said one or more slices ~~further~~ comprising one or more rings, each ring of said one or more rings ~~further~~ comprising y stages, where $y \geq 2$; and

15 each stage of said y stages comprising at least one switch of size $d_i \times d_0$, where $d_i \geq 2$ and $d_0 \geq 2$, ~~and~~ each switch of said at least one switch of size $d_i \times d_0$ having d_i incoming links and d_0 outgoing links; ~~and~~ each switch of said at least one switch of size $d_i \times d_0$ ~~further~~ comprising a plurality of multiplexers of size $d \geq 2$ with each multiplexer of said plurality of multiplexers comprising d inputs and one output; and

20 wherein said d_i incoming links and said d_0 outgoing links comprise ~~comprises a~~ plurality of one or more internal connections and a plurality of one or more hop wires; ~~and~~ where said plurality of one or more hop wires ~~further comprising~~ comprise a plurality of one or more internal hop wires or a plurality of one or more external hop wires; and

wherein each inlet link of ~~S~~ said plurality of inlet links is connected to the output of a first
 25 multiplexer ~~one~~ of said plurality of multiplexers of a first ~~one~~ switch of said at least one switch of size $d_i \times d_0$ of a first ~~one~~ stage of said y stages of a first ~~one~~ partial multi-stage network of said plurality of partial multi-stage networks, and each outlet link of said

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

plurality of outlet links is connected to ~~one of the~~ a first input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more ~~said~~ switches of said at least one switch of size $d_i \times d_0$ of one or more ~~said~~ stages of said y stages of one or more partial multi-stage networks of said plurality of partial multi-stage networks; and

- 5 a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of inlet links as a second programmable logic block of said plurality of programmable logic blocks and a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of outlet links as a second programmable logic
- 10 block of said plurality of programmable logic blocks; a first partial multi-stage network of said plurality of partial multi-stage networks comprising the same or different number of said one or more slices as a second partial multi-stage network of said plurality of partial multi-stage networks; a first slice of said one or more slices comprising the same or different number of said one or more rings as a second slice of said one or more slices; a
- 15 first ring of said one or more rings comprising the same or different number of said y stages as a second ring of said one or more rings; and a first stage of said y stages comprising the same or different number of said at least one switch of size $d_i \times d_0$ as a second stage of said y stages; a first switch of said at least one switch of size $d_i \times d_0$ is the same or different size as a second switch of said at least one switch of size $d_i \times d_0$; a
- 20 first multiplexer in said plurality of multiplexers of size $d \geq 2$ is the same or different size as a second multiplexer in said plurality of multiplexers of size $d \geq 2$; and

wherein each internal connection of said ~~plurality of~~ one or more internal connections connected from the output of a first multiplexer of said plurality of multiplexers of a first switch of said at least one switch of size $d_i \times d_0$ of a first stage of said y stages of a first

25 ring of said one or more rings to a first input of said d inputs of a second multiplexer of said plurality of multiplexers of a second switch of said at least one switch of size $d_i \times d_0$ of a second stage of said y stages of the first ring of said one or more rings; and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

wherein each internal hop wire of said ~~plurality of one or more~~ internal hop wires is connected from the output of a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_o$ of a stage of said y stages of a first ring of said one or more rings of a first slice of said one or more slices to a first input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_o$ of one or more stages of said y stages of one or more rings different from the first ring of said one or more rings of the ~~same~~ first slice of said one or more slices; and

wherein each external hop wire of said ~~plurality of one or more~~ external hop wires is connected from the output a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_o$ of a stage of said y stages of a ring of said one or more rings of a slice of said one or more slices of a first partial multi-stage network of said plurality of partial multi-stage networks to an input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_o$ of one or more stages of said y stages of said one or more rings of a slice of said one or more slices of one or more partial multi-stage networks different from the first partial multi-stage network of said plurality of partial multi-stage networks; and

wherein one or more external hop wires of said ~~plurality of one or more~~ external hop wires are ~~either one of a)~~ connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size $d_i \times d_o$ in same ~~numbered~~ stages of said y stages in three or more partial multi-stage networks of said plurality of partial multi-stage networks (hereinafter "multi-drop hop wires") ~~or~~ and b) connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size $d_i \times d_o$ in different ~~numbered~~ stages of said y stages; in three or more partial multi-stage networks of said plurality of partial multi-stage networks (hereinafter "multi-drop hop wires").

16. (Currently Amended): The programmable integrated circuit of claim 15, The programmable integrated circuit of claim 8 wherein said ~~plurality of one or more~~

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

external hop wires are connected vertically (hereinafter “vertical wires” or “vertical external hop wires”), or horizontally (hereinafter “horizontal wires” or “horizontal external hop wires”); and

each partial multi-stage network of said plurality of partial multi-stage networks
 5 comprising said one or more slices is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or

each partial multi-stage network of said plurality of partial multi-stage networks comprising said horizontal wires and said vertical wires is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or

10 each partial multi-stage network of said plurality of partial multi-stage networks comprising both said one or more slices, and said horizontal wires and said vertical wires is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid.

17. (Currently Amended): The programmable integrated circuit of claim 15, wherein said
 15 ~~plurality of one or more~~ external hop wires are ~~e cascaded~~ interconnected through only one multiplexer of said plurality of multiplexers at each switch of said at least one switch of size $d_i \times d_0$.

18. (Currently Amended): The programmable integrated circuit of claim 15, wherein said
 20 one or more external hop wires of said ~~plurality of one or more~~ external hop wires are connected between at least one same ~~numbered~~ stage in all said plurality of partial multi-stage networks, or

one or more external hop wires of said ~~plurality of one or more~~ external hop wires are connected between at least two ~~not same~~ different ~~numbered~~ stages of said y stages in all said plurality of partial multi-stage networks; or

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

said ~~plurality of~~ one or more external hop wires are all connected between same ~~numbered~~ stages of said y stages in all stages of said y stages of all said plurality of partial multi-stage networks.

19. (Currently Amended): The programmable integrated circuit of claim 15, wherein each
 5 multiplexer of said plurality of multiplexers of size $d \geq 2$ is of size $d = 4$ or ~~$d \geq 4$~~ $d \geq 4$.

20. (Currently Amended): The programmable integrated circuit of claim 15, wherein one
 or more ~~of~~ external hop wires of said ~~plurality of~~ one or more external hop wires are
 implemented in two or more metal layers, or

10 each multiplexer of said plurality of multiplexers of size $d \geq 2$ is configurable by
Static Random Address Memory SRAM cells or Flash memory Cells, or

said ~~plurality of~~ one or more external hop wires use a plurality of buffers to amplify
 signals driven through them; and said plurality of buffers are either inverting or non-
 inverting buffers, or

15 ~~one or more stages of said y stages in one partial multi-stage network of said~~
~~plurality of partial multi-stage networks comprising a switch of size~~
 ~~$(d_i + m) \times (d_o + n)$, where $d_i \geq 2$, $d_o \geq 2$, $m \geq 0$, $n \geq 0$ or~~

one or more of said y stages in ~~one a first~~ partial multi-stage network of said plurality
 of partial multi-stage networks ~~comprising~~ comprise one of a six 2:1 multiplexers, or
 20 b) eight 2:1 multiplexers, or four 3:1 multiplexers, or and c) four 4:1 multiplexers, or

said at least one switch of size $d_i \times d_o$ of said y stages are either fully populated or
 partially populated, or

said plurality of partial multi-stage networks are implemented in a 3D-FPGAs
integrated circuit device.

25

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

REMARKS

Applicant respectfully submits that entry of the foregoing Amendment pursuant to 37 CFR § 1.121 does not raise any new issues.

5 **The amended claims do not change the scope of the previously allowed claims,**
and will not require a further search or substantial additional work on the part of the Office.

Consequently, pursuant to Rule 312, it is requested that the foregoing Amendment be entered.

10

CONCLUSION

For all of the above reasons, applicant submits that the Claims are now in proper form, and that the Claims all define patentably over the prior art. Therefore applicant submits that this application is now in condition for allowance, which action he
15 respectfully solicits.

Conditional request for Constructive Assistance

Applicant has amended the claims of this application so that they are proper, definite, and define novel structure which is also unobvious. If, for any reason this application is not believed to be in full condition for allowance, applicant respectfully request the
20 constructive assistance and suggestions of the Examiner pursuant to M.P.E.P § 2173.02 and § 707.07(j) in order that the undersigned can place this application in allowable condition as soon as possible and without the need for further proceedings.

Respectfully Submitted,

25 /Venkat Konda/

Application Number: 16/562,450

Art Unit: 2464

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Venkat Konda

Konda Technologies, Inc (USPTO Customer Number: 38139)

6278 Grand Oak Way

San Jose, CA 95135

5 Phone: 408-472-3273



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/562,450	09/06/2019	Venkat Konda	V-0060US	6438

38139 7590 01/27/2021
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

EXAMINER

GIDADO, RASHEED

ART UNIT	PAPER NUMBER
----------	--------------

2464

NOTIFICATION DATE	DELIVERY MODE
-------------------	---------------

01/27/2021

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

venkat@kondatech.com
vkonda@gmail.com

Supplemental Notice of Allowability	Application No. 16/562,450	Applicant(s) Konda, Venkat	
	Examiner RASHEED GIDADO	Art Unit 2464	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. This communication is responsive to 01/13/2021.
 A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. The allowed claim(s) is/are 1-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) All b) Some *c) None of the:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|---|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Examiner's Amendment/Comment |
| 2. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____. | 6. <input type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| 3. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material _____. | 7. <input checked="" type="checkbox"/> Other <u>PTO-90C</u> . |
| 4. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date. _____. | |

/RASHEED GIDADO/
Primary Examiner, Art Unit 2464



UNITED STATES DEPARTMENT OF COMMERCE

U.S. Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR/ PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
16/562,450	09/06/2019	Konda, Venkat	V-0060US

Konda Technologies, Inc 6278 GRAND OAK WAY SAN JOSE, CA 95135	EXAMINER	
	RASHEED GIDADO	
	ART UNIT	PAPER
	2464	20210122

DATE MAILED: 21 January 2021

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

<p>Applicant submitted a substitute amendment to the specification on 01/21/2021.</p> <p>Substitute Abstract is in page 3.</p> <p>Substitute of first paragraph of Cross Reference to Related Application is on page 4. Other paragraphs remain unchanged.</p> <p>Background of the invention remain unchanged.</p> <p>Summary of the invention remain unchanged.</p> <p>Brief Description of Drawings remain unchanged.</p> <p>Substitute Detailed Description of the Invention with marked-up are on pages 8-110.</p> <p>Substitute Detailed Description of the Invention clean copy versions are on pages 111-213.</p>	
/RASHEED GIDADO/ Primary Examiner, Art Unit 2464	

Electronic Acknowledgement Receipt

EFS ID:	41710508
Application Number:	16562450
International Application Number:	
Confirmation Number:	6438
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkat Konda
Filer Authorized By:	
Attorney Docket Number:	V-0060US
Receipt Date:	21-JAN-2021
Filing Date:	06-SEP-2019
Time Stamp:	17:25:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment after Notice of Allowance (Rule 312)	Amnd312-V60-1-21-21.pdf	1177451 <small>c3864ecc0367aedaa21bfda42599e542257a3d93</small>	no	214

Warnings:

Information:	
Total Files Size (in bytes):	1177451
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>	

Application Number: 16/562,450

Art Unit: 2464

AMENDMENT AFTER ALLOWANCE UNDER RULE 312

In The United States Patent And Trademark Office

Application Number: 16/562,450

Application Filed: 9/6/2019

Applicant(s): Venkat Konda

5 Title: Fast Scheduling and Optimization of Multi-stage Hierarchical Networks

Examiner/Art Unit: Rasheed Gidado / 2464

San Jose, 2021 January 21, Thu

AMENDMENT AFTER ALLOWANCE UNDER RULE 312

10 **(37 C.F.R. § 1.312)**

Mail Stop Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, Virginia, 22313-1450

15 Dear Sir/Madam:

This replies to the Notice of Allowance and Fee(s) Due from the United States Patent and Trademark Office mailed on November 18, 2020 in connection with the above-identified patent application. Pursuant to Rule 312, applicant respectfully requests that the above application be amended as follows:

20 For the sake of clarity in the amendment to the abstract of disclosure, amendment to Cross Reference to Related applications, amendment to Summary of Invention, and amendments to the specification submitted on November 9, 2020 in response to the office action August 7, 2020, Applicant is further submitting the following:

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

- 1) Unedited and substitute Abstract of Disclosure in page 3.
- 2) Unedited and substitute Cross Reference to Related Applications in page 4.
- 3) Unedited and substitute Summary of Invention in page 6.
- 4) Complete Specification (Detailed Description of the Invention) with the all
5 amendments to specification begin on page 8 and continues to page 110.
- 5) Unedited and complete substitute specification (Detailed Description of the
Invention) begin on page 111 and continues to page 213.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

I. UNEDITED AND SUBSTITUTE ABSTRACT OF THE DISCLOSURE:

An unedited and substitute Abstract of the Disclosure appears below:

Significantly optimized multi-stage networks including scheduling methods for faster scheduling of connections, useful in wide target applications, with VLSI layouts using only horizontal wires and vertical wires to route large scale partial multi-stage hierarchical networks having inlet and outlet links, and laid out in an integrated circuit device in a two-dimensional grid arrangement of blocks are disclosed. The optimized multi-stage networks in each block employ one or more slices of rings of stages of switches with inlet and outlet links of partial multi-stage hierarchical networks connecting to rings from either left-hand side or right-hand side; and employ hop wires or multi-drop hop wires wherein hop wires or multi-drop wires are connected from switches of stages of rings of slices of a first partial multi-stage hierarchical network to switches of stages of rings of slices of the first or a second partial multi-stage hierarchical network.

Applicant submits that the above amended abstract is within 150 words.

15

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

II. UNEDITED AND SUBSTITUTE CROSS REFERENCE TO RELATED APPLICATIONS

An unedited and substitute Cross Reference to Related Applications appears below:

- 5 This application is Continuation Application and claims priority to US Application Serial No. 15/884,911 entitled "FAST SCHEDULING AND OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed January 31, 2018, which is Continuation Application and claims priority to US Application Serial No.
- 10 15/331,855 entitled "FAST SCHEDULING AND OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed October 22, 2016, issued as US Patent No. 9,929,977 on March 27, 2018, which is Continuation Application and claims priority to US Application Serial No. 14/329,876 entitled "FAST SCHEDULING AND OPTIMIZATION OF MULTI-
- 15 STAGE HIERARCHICAL NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed July 11, 2014, issued as US Patent No. 9,509,634 on November 29, 2016, which claims priority to U.S. Provisional Patent Application Serial No. 61/846,083 entitled "FAST SCHEDULING AND OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS" by Venkat Konda assigned to the
- 20 same assignee as the current application, filed July 15, 2013, and also Continuation-in-Part Application and claims priority to US Application Serial No. US14/199,168 entitled "OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS FOR PRACTICAL ROUTING APPLICATIONS" by Venkat Konda assigned to the same assignee as the current application, filed March 6, 2014, issued as US Patent No.
- 25 9,374,322 on June 21, 2016, which in turn is bypass continuation application and claims priority to PCT Application Serial No. PCT/US12/53814 entitled "OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS FOR PRACTICAL ROUTING APPLICATIONS" by Venkat Konda assigned to the same assignee as the current application, filed September 6, 2012, which is Continuation-in-Part application and
- 30 claims priority to U.S. Provisional Patent Application Serial No. 61/531,615 entitled "OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS FOR

Application Number: 16/562,450

Art Unit: 2464

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

"PRACTICAL ROUTING APPLICATIONS" by Venkat Konda assigned to the same assignee as the current application, filed September 7, 2011.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

III. UNEDITED AND SUBSTITUTE SUMMARY OF INVENTION

An unedited and substitute Summary of Invention appears below:

5 Significantly optimized multi-stage networks for faster scheduling of connections, useful in wide target applications, with VLSI layouts (or floor plans) using only horizontal wires and vertical wires to route large scale partial multi-stage hierarchical networks having inlet and outlet links, and laid out in an integrated circuit device in a two-dimensional grid arrangement of blocks, (for example in an FPGA where the partial
10 multi-stage hierarchical networks to route Lookup Tables, or memory blocks, or DSP blocks) are disclosed. The optimized multi-stage networks in each block employ one or more slices of rings of stages of switches with inlet and outlet links of partial multi-stage hierarchical networks connecting to rings from either left-hand side or right-hand side.

 The optimized multi-stage networks employ hop wires or multi-drop hop wires
15 wherein hop wires or multi-drop wires are connected from switches of stages of rings of slices of a first partial multi-stage hierarchical network to switches of stages of rings of slices of a second partial multi-stage hierarchical network or switches of stages of rings of slices of the first partial multi-stage hierarchical network so that said hop wires or multi-drop hop wires are either vertical wires or horizontal wires.

20 The VLSI layouts exploit spatial locality so that partial multi-stage hierarchical networks that are spatially nearer are connected with shorter hop wires compared to the hop wires between spatially farther partial multi-stage hierarchical networks. The optimized multi-stage networks provide high routability for broadcast, unicast and multicast connections, yet with the benefits of significantly lower cross points hence
25 smaller area, lower signal latency, lower power and with significant fast compilation or routing time. Various scheduling methods are also disclosed to schedule a set of multicast connections in the multi-stage hierarchical network.

 The optimized multi-stage networks $V_{Comb}(N_1, N_2, d, s)$ & $V_{D-Comb}(N_1, N_2, d, s)$ according to the current invention inherit the properties of one or more generalized multi-

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

- stage and pyramid networks $V(N_1, N_2, d, s)$ & $V_p(N_1, N_2, d, s)$, generalized folded multi-stage and pyramid networks $V_{fold}(N_1, N_2, d, s)$ & $V_{fold-p}(N_1, N_2, d, s)$, generalized butterfly fat tree and butterfly fat pyramid networks $V_{bft}(N_1, N_2, d, s)$ & $V_{bfp}(N_1, N_2, d, s)$, generalized multi-link multi-stage and pyramid networks
- 5 $V_{mlink}(N_1, N_2, d, s)$ & $V_{mlink-p}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage and pyramid networks $V_{fold-mlink}(N_1, N_2, d, s)$ & $V_{fold-mlink-p}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree and butterfly fat pyramid networks $V_{mlink-bft}(N_1, N_2, d, s)$ & $V_{mlink-bfp}(N_1, N_2, d, s)$, generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$, and
- 10 generalized cube connected cycles networks $V_{CCC}(N_1, N_2, d, s)$ for $s = 1, 2, 3$ or any number in general.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

IV. COMPLETE SPECIFICATION WITH ALL THE AMENDMENTS TO THE SPECIFICATION

Complete Specification with the all amendments to specification appears below:

5 Fully connected multi-stage hierarchical networks are an over kill in every dimension such as area, power, and performance for certain practical routing applications and need to be optimized to significantly improve savings in area, power and performance of the routing network. The present invention discloses several embodiments of the optimized multi-stage hierarchical networks for practical routing applications along with their VLSI layout (floor plan) feasibility and simplicity.

10 The multi-stage hierarchical networks considered for optimization in the current invention include: generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, generalized hypercube networks $V_{cube}(N_1, N_2, d, s)$, and generalized cube connected cycles networks $V_{ccc}(N_1, N_2, d, s)$ for $s = 1, 2, 3$ or any number in general. Alternatively the optimized multi-stage hierarchical networks disclosed in this invention inherit the properties of one or more of these networks, in addition to additional properties that may not be exhibited these networks.

15
20

The optimized multi-stage hierarchical networks disclosed are applicable for practical routing applications, with several goals such as: 1) all the signals in the design starting from an inlet link of the network to an outlet link of the network need to be setup without blocking. These signals may consist of broadcast, unicast and multicast connections; Each routing resource may need to be used by only one signal or connection; 2) physical area consumed by the routing network to setup all the signals needs to be small; 3) power consumption of the network needs to be small, after the signals are setup. Power may be both static power and dynamic power; 4) Delay of the signal or a connection needs to be small after it is setup through a path using several

25

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

routing resources in the path. The smaller the delay of the connections will lead to faster performance of the design. Typically delay of the critical connections determines the performance of the design on a given network; 5) Designs need to be not only routed through the network (i.e., all the signals need to be setup from inlet links of the network to the outlet links of the network.), but also the routing needs to be in faster time using efficient routing algorithms; 6) Efficient VLSI layout of the network is also critical and can greatly influence all the other parameters including the area taken up by the network on the chip, total number of wires, length of the wires, delay through the signal paths and hence the maximum clock speed of operation.

10 The different varieties of multi-stage networks described in various embodiments in the current invention have not been implemented previously on the semiconductor chips. The practical application of these networks includes Field Programmable Gate Array (FPGA) chips. Current commercial FPGA products such as Xilinx's Vertex, Altera's Stratix, Lattice's ECPx implement island-style architecture using mesh and segmented mesh routing interconnects using either full crossbars or sparse crossbars. 15 These routing interconnects consume large silicon area for crosspoints, long wires, large signal propagation delay and hence consume lot of power.

The current invention discloses the optimization and scheduling methods of multi-stage hierarchical networks with fast scheduling of connections, for practical routing applications of numerous types of multi-stage networks also using multi-drop links. The 20 optimizations disclosed in the current invention are applicable to including the numerous generalized multi-stage networks disclosed in the following patent applications:

1) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-stage networks $V(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 25 8,270,400 that is incorporated by reference above.

2) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized butterfly fat tree networks $V_{bt}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent 30 No. 8,170,040 that is incorporated by reference above.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

3) Rearrangeably nonblocking for arbitrary fan-out multicast and unicast, and strictly nonblocking for unicast for generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$ and generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods
5 are described in detail in the US Patent No. 8,363,649 that is incorporated by reference above.

4) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the
10 US Patent No. 8,170,040 that is incorporated by reference above.

5) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,363,649 that is incorporated by reference above.

15 6) Strictly nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$ and generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,363,649 that is incorporated by reference above.

20 7) VLSI layouts of numerous types of multi-stage networks are described in the US Patent No. 8,269,523 entitled "VLSI LAYOUTS OF FULLY CONNECTED NETWORKS" that is incorporated by reference above.

8) VLSI layouts of numerous types of multi-stage networks are described in the US Patent No. 8,898,611 entitled "VLSI LAYOUTS OF FULLY CONNECTED
25 GENERALIZED AND PYRAMID NETWORKS WITH LOCALITY EXPLOITATION" that is incorporated by reference above.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

In addition the optimization with the VLSI layouts disclosed in the current invention are also applicable to generalized multi-stage pyramid networks $V_p(N_1, N_2, d, s)$, generalized folded multi-stage pyramid networks $V_{fold-p}(N_1, N_2, d, s)$, generalized butterfly fat pyramid networks $V_{bfp}(N_1, N_2, d, s)$, generalized multi-link

5 multi-stage pyramid networks $V_{mlink-p}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage pyramid networks $V_{fold-mlink-p}(N_1, N_2, d, s)$, generalized multi-link butterfly fat pyramid networks $V_{mlink-bfp}(N_1, N_2, d, s)$, generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ and generalized cube connected cycles networks $V_{ccc}(N_1, N_2, d, s)$ for $s = 1, 2, 3$ or any number in general.

10 Finally the current invention discloses the optimizations and VLSI layouts of multi-stage hierarchical networks $V_{Comb}(N_1, N_2, d, s)$ and the optimizations and VLSI layouts of multi-stage hierarchical networks $V_{D-Comb}(N_1, N_2, d, s)$ for practical routing applications (particularly to set up broadcast, unicast and multicast connections), where “Comb” denotes the combination of and “D-Comb” denotes the delay optimized

15 combination of any of the generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, generalized multi-stage

20 pyramid networks $V_p(N_1, N_2, d, s)$, generalized folded multi-stage pyramid networks $V_{fold-p}(N_1, N_2, d, s)$, generalized butterfly fat pyramid networks $V_{bfp}(N_1, N_2, d, s)$, generalized multi-link multi-stage pyramid networks $V_{mlink-p}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage pyramid networks $V_{fold-mlink-p}(N_1, N_2, d, s)$, generalized multi-link butterfly fat pyramid networks $V_{mlink-bfp}(N_1, N_2, d, s)$, generalized hypercube

25 networks $V_{hcube}(N_1, N_2, d, s)$, and generalized cube connected cycles networks $V_{ccc}(N_1, N_2, d, s)$ for $s = 1, 2, 3$ or any number in general.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$:

Referring to diagram 100A in FIG. 1A, in one embodiment, an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ where $N_1 = 200$; $N_2 = 400$; $d = 2$; and $s = 1$ corresponding to one computational block, with each computational block
 5 having 4 inlet links namely I1, I2, I3, and I4; and 2 outlet links namely O1 and O2. And for each computational block the corresponding partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists of two rings 110 and 120, where ring 110 consists of “m+1” stages namely (ring 1, stage 0), (ring 1, stage 1), ... (ring 1, stage “m-1”), and (ring 1, stage “m”), and ring 120 consists of “n+1” stages namely (ring 2, stage 0), (ring
 10 2, stage 1), ... (ring 2, stage “n-1”), and (ring 2, stage “n”), where “m” and “n” are positive integers.

Ring 110 has inlet links Ri(1,1) and Ri(1,2), and has outlet links Bo(1,1) and Bo(1,2). Ring 120 has inlet links Fi(2,1) and Fi(2,2), and outlet links Bo(2,1) and Bo(2,2). And hence the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists
 15 of 4 inlet links and 4 outlet links corresponding to the two rings 110 and 120. Outlet link O1 of the computational block is connected to inlet link Ri(1,1) of ring 110 and also inlet link of Fi(2,1) of ring 120. Similarly outlet link O2 of the computational block is connected to inlet link Ri(1,2) of Ring 110 and also inlet link of Fi(2,2) of Ring 120. And outlet link Bo(1,1) of Ring 110 is connected to inlet link I1 of the computational block.
 20 Outlet link Bo(1,2) of Ring 110 is connected to inlet link I2 of the computational block. Similarly outlet link Bo(2,1) of Ring 120 is connected to inlet link I3 of the computational block. Outlet link Bo(2,2) of Ring 120 is connected to inlet link I4 of the computational block. Since in this embodiment outlet link O1 of the computational block is connected to both inlet link Ri(1,1) of ring 110 and inlet link Fi(2,1) of ring 120; and
 25 outlet link O2 of the computational block is connected to both inlet link Ri(1,2) of ring 110 and inlet link Fi(2,2) of ring 120, the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists of 2 inlet links and 4 outlet links.

The two dimensional grid 800 in FIG. 8 illustrates an exemplary arrangement of 100 blocks arranged in 10 rows and 10 columns, in an embodiment. Each row of 2D-grid
 30 consisting of 10 block numbers namely the first row consists of the blocks (1,1), (1,2),

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

(1,3), ... , (1,9), and (1,10). The second row consists of the blocks (2,1), (2,2), (2,3), ... , (2,9), and (2,10). Similarly 2D-grid 800 consists of 10 rows of each with 10 blocks and finally the tenth row consists of the blocks (10,1), (10,2), (10,3), ... , (10,9), and (10,10). Each block of 2D-grid 800, in one embodiment, is part of the die area of a semiconductor integrated circuit (hereinafter alternatively referred to as “integrated circuit device” or “IC device”), so that the complete 2D-grid 800 of 100 blocks represents the complete die of the semiconductor integrated circuit. In one embodiment, each block of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A with 2 inlet links and 4 outlet links and the corresponding computational block with 4 inlet links and 2 outlet links. For example block (1,1) of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A with 2 inlet links and 4 outlet links and the corresponding computational block with 4 inlet links and 2 outlet links. Similarly each of the 100 blocks of 2D-grid 800 has a separate partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A with 2 inlet links and 4 outlet links and the corresponding computational block with 4 inlet links and 2 outlet links. Hence the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to 2D-grid 800 has $N_1 = 200$ inlet links and $N_2 = 400$ outlet links. And there are 100 computational blocks each one corresponding to one of the blocks with each computational block having 4 inlet links and 2 outlet links. Also the 2D-grid 800 is organized in the fourth quadrant of the 2D-Plane. In other embodiments the 2D-grid 800 may be organized as either first quadrant, or second quadrant or third quadrant of the 2D-Plane.

Referring to partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A in FIG. 1A, the stage (ring 1, stage 0) consists of 4 inputs namely $R_i(1,1)$, $R_i(1,2)$, $U_i(1,1)$, and $U_i(1,2)$; and 4 outputs $B_o(1,1)$, $B_o(1,2)$, $F_o(1,1)$, and $F_o(1,2)$. The stage (ring 1, stage 0) also consists of eight 2:1 multiplexers (A multiplexer is hereinafter called a “mux”) namely $R(1,1)$, $R(1,2)$, $F(1,1)$, $F(1,2)$, $U(1,1)$, $U(1,2)$, $B(1,1)$, and $B(1,2)$. The 2:1 Mux $R(1,1)$ has two inputs namely $R_i(1,1)$ and $B_o(1,1)$ and has one output $R_o(1,1)$. The 2:1 Mux $R(1,2)$ has two inputs namely $R_i(1,2)$ and $B_o(1,2)$ and has one output $R_o(1,2)$. The 2:1 Mux $F(1,1)$ has two inputs namely $R_o(1,1)$ and $R_o(1,2)$ and has one output $F_o(1,1)$. The 2:1 Mux $F(1,2)$ has two inputs namely $R_o(1,1)$ and $R_o(1,2)$ and has one output $F_o(1,2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux U(1,1) has two inputs namely $U_i(1,1)$ and $F_o(1,1)$ and has one output $U_o(1,1)$. The 2:1 Mux U(1,2) has two inputs namely $U_i(1,2)$ and $F_o(1,2)$ and has one output $U_o(1,2)$. The 2:1 Mux B(1,1) has two inputs namely $U_o(1,1)$ and $U_o(1,2)$ and has one output $B_o(1,1)$. The 2:1 Mux B(1,2) has two inputs namely $U_o(1,1)$ and $U_o(1,2)$ and has one output $B_o(1,2)$.

The stage (ring 1, stage 1) consists of 4 inputs namely $R_i(1,3)$, $R_i(1,4)$, $U_i(1,3)$, and $U_i(1,4)$; and 4 outputs $B_o(1,3)$, $B_o(1,4)$, $F_o(1,3)$, and $F_o(1,4)$. The stage (ring 1, stage 1) also consists of eight 2:1 Muxes namely R(1,3), R(1,4), F(1,3), F(1,4), U(1,3), U(1,4), B(1,3), and B(1,4). The 2:1 Mux R(1,3) has two inputs namely $R_i(1,3)$ and $B_o(1,3)$ and has one output $R_o(1,3)$. The 2:1 Mux R(1,4) has two inputs namely $R_i(1,4)$ and $B_o(1,4)$ and has one output $R_o(1,4)$. The 2:1 Mux F(1,3) has two inputs namely $R_o(1,3)$ and $R_o(1,4)$ and has one output $F_o(1,3)$. The 2:1 Mux F(1,4) has two inputs namely $R_o(1,3)$ and $R_o(1,4)$ and has one output $F_o(1,4)$.

The 2:1 Mux U(1,3) has two inputs namely $U_i(1,3)$ and $F_o(1,3)$ and has one output $U_o(1,3)$. The 2:1 Mux U(1,4) has two inputs namely $U_i(1,4)$ and $F_o(1,4)$ and has one output $U_o(1,4)$. The 2:1 Mux B(1,3) has two inputs namely $U_o(1,3)$ and $U_o(1,4)$ and has one output $B_o(1,3)$. The 2:1 Mux B(1,4) has two inputs namely $U_o(1,3)$ and $U_o(1,4)$ and has one output $B_o(1,4)$.

The output $F_o(1,1)$ of the stage (ring 1, stage 0) is connected to the input $R_i(1,3)$ of the stage (ring 1, stage 1) which is called hereinafter an internal connection (hereinafter alternatively referred to as "straight link" or "straight middle link") between two successive stages of a ring. And the output $B_o(1,3)$ of the stage (ring 1, stage 1) is connected to the input $U_i(1,1)$ of the stage (ring 1, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1.

The stage (ring 1, stage "m-1") consists of 4 inputs namely $F_i(1,2m-1)$, $F_i(1,2m)$, $U_i(1,2m-1)$, and $U_i(1,2m)$; and 4 outputs $B_o(1,2m-1)$, $B_o(1,2m)$, $F_o(1,2m-1)$, and $F_o(1,2m)$. The stage (ring 1, stage "m-1") also consists of six 2:1 Muxes namely F(1,2m-1), F(1,2m), U(1,2m-1), U(1,2m), B(1,2m-1), and B(1,2m). The 2:1 Mux F(1,2m-1) has two inputs namely $F_i(1,2m-1)$ and $F_i(1,2m)$ and has one output $F_o(1,2m-1)$. The 2:1 Mux F(1,2m) has two inputs namely $F_i(1,2m-1)$ and $F_i(1,2m)$ and has one output $F_o(1,2m)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux $U(1,2m-1)$ has two inputs namely $U_i(1,2m-1)$ and $F_o(1,2m-1)$ and has one output $U_o(1,2m-1)$. The 2:1 Mux $U(1,2m)$ has two inputs namely $U_i(1,2m)$ and $F_o(1,2m)$ and has one output $U_o(1,2m)$. The 2:1 Mux $B(1,2m-1)$ has two inputs namely $U_o(1,2m-1)$ and $U_o(1,2m)$ and has one output $B_o(1,2m-1)$. The 2:1 Mux $B(1,2m)$ has two
5 inputs namely $U_o(1,2m-1)$ and $U_o(1,2m)$ and has one output $B_o(1,2m)$.

The stage (ring 1, stage "m") consists of 4 inputs namely $F_i(1,2m+1)$, $F_i(1,2m+2)$, $U_i(1,2m+1)$, and $U_i(1,2m+2)$; and 4 outputs $B_o(1,2m+1)$, $B_o(1,2m+2)$, $F_o(1,2m+1)$, and $F_o(1,2m+2)$. The stage (ring 1, stage "m") also consists of six 2:1 Muxes namely $F(1,2m+1)$, $F(1,2m+2)$, $U(1,2m+1)$, $U(1,2m+2)$, $B(1,2m+1)$, and $B(1,2m+2)$. The 2:1
10 Mux $F(1,2m+1)$ has two inputs namely $F_i(1,2m+1)$ and $F_i(1,2m+2)$ and has one output $F_o(1,2m+1)$. The 2:1 Mux $F(1,2m+2)$ has two inputs namely $F_i(1,2m+1)$ and $F_i(1,2m+2)$ and has one output $F_o(1,2m+2)$.

The 2:1 Mux $U(1,2m+1)$ has two inputs namely $U_i(1,2m+1)$ and $F_o(1,2m+1)$ and has one output $U_o(1,2m+1)$. The 2:1 Mux $U(1,2m+2)$ has two inputs namely $U_i(1,2m+2)$ and $F_o(1,2m+2)$ and has one output $U_o(1,2m+2)$. The 2:1 Mux $B(1,2m+1)$ has two inputs
15 namely $U_o(1,2m+1)$ and $U_o(1,2m+2)$ and has one output $B_o(1,2m+1)$. The 2:1 Mux $B(1,2m+2)$ has two inputs namely $U_o(1,2m+1)$ and $U_o(1,2m+2)$ and has one output $B_o(1,2m+2)$.

The output $F_o(1,2m-1)$ of the stage (ring 1, stage "m-1") is connected to the input
20 $F_i(1,2m+1)$ of the stage (ring 1, stage "m"), is an internal connection between stage "m-1" and stage "m" of the ring 1. And the output $B_o(1,2m+1)$ of the stage (ring 1, stage "m") is connected to the input $U_i(1,2m-1)$ of the stage (ring 1, stage "m-1"), is another internal connection between stage "m-1" and stage "m" of the ring 1

Just the same way the stages (ring 1, stage 0), (ring 1, stage 1), there are also
25 stages (ring 1, stage 2), (ring 1, stage 3), ... (ring 1, stage "m-1"), (ring 1, stage "m") in that order, where the stages from (ring 1, stage 2), (ring 1, stage 3), ... , (ring 1, stage "m-2") are not shown in the diagram 100A. Just the same way the two successive stages (ring 1, stage 0) and (ring 1, stage 1) have internal connections between them as described before, any two successive stages have similar internal connections. For example (ring 1,

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

stage 1) and (ring 1, stage 2) have similar internal connections and (ring 1, stage “m-2”) and (ring 1, stage “m-1”) have similar internal connections.

Stage (ring 1, stage 0) is also called hereinafter the “entry stage” or “first stage” of ring 1, since inlet links and outlet links of the computational block are directly connected to stage (ring 1, stage 0). Also stage (ring 1, stage “m”) is hereinafter the “last stage” or “root stage” of ring 1.

The stage (ring 2, stage 0) consists of 4 inputs namely $F_i(2,1)$, $F_i(2,2)$, $U_i(2,1)$, and $U_i(2,2)$; and 4 outputs $B_o(2,1)$, $B_o(2,2)$, $F_o(2,1)$, and $F_o(2,2)$. The stage (ring 2, stage 0) also consists of six 2:1 Muxes namely $F(2,1)$, $F(2,2)$, $U(2,1)$, $U(2,2)$, $B(2,1)$, and $B(2,2)$. The 2:1 Mux $F(2,1)$ has two inputs namely $F_i(2,1)$ and $F_i(2,2)$ and has one output $F_o(2,1)$. The 2:1 Mux $F(2,2)$ has two inputs namely $F_i(2,1)$ and $F_i(2,2)$ and has one output $F_o(2,2)$.

The 2:1 Mux $U(2,1)$ has two inputs namely $U_i(2,1)$ and $F_o(2,1)$ and has one output $U_o(2,1)$. The 2:1 Mux $U(2,2)$ has two inputs namely $U_i(2,2)$ and $F_o(2,2)$ and has one output $U_o(2,2)$. The 2:1 Mux $B(2,1)$ has two inputs namely $U_o(2,1)$ and $U_o(2,2)$ and has one output $B_o(2,1)$. The 2:1 Mux $B(2,2)$ has two inputs namely $U_o(2,1)$ and $U_o(2,2)$ and has one output $B_o(2,2)$.

The stage (ring 2, stage 1) consists of 4 inputs namely $F_i(2,3)$, $F_i(2,4)$, $U_i(2,3)$, and $U_i(2,4)$; and 4 outputs $B_o(2,3)$, $B_o(2,4)$, $F_o(2,3)$, and $F_o(2,4)$. The stage (ring 2, stage 1) also consists of six 2:1 Muxes namely $F(2,3)$, $F(2,4)$, $U(2,3)$, $U(2,4)$, $B(2,3)$, and $B(2,4)$. The 2:1 Mux $F(2,3)$ has two inputs namely $F_i(2,3)$ and $F_i(2,4)$ and has one output $F_o(2,3)$. The 2:1 Mux $F(2,4)$ has two inputs namely $F_i(2,3)$ and $F_i(2,4)$ and has one output $F_o(2,4)$.

The 2:1 Mux $U(2,3)$ has two inputs namely $U_i(2,3)$ and $F_o(2,3)$ and has one output $U_o(2,3)$. The 2:1 Mux $U(2,4)$ has two inputs namely $U_i(2,4)$ and $F_o(2,4)$ and has one output $U_o(2,4)$. The 2:1 Mux $B(2,3)$ has two inputs namely $U_o(2,3)$ and $U_o(2,4)$ and has one output $B_o(2,3)$. The 2:1 Mux $B(2,4)$ has two inputs namely $U_o(2,3)$ and $U_o(2,4)$ and has one output $B_o(2,4)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The output $Fo(2,1)$ of the stage (ring 2, stage 0) is connected to the input $Fi(2,3)$ of the stage (ring 2, stage 1), is an internal connection between stage 0 and stage 1 of the ring 2. And the output $Bo(2,3)$ of the stage (ring 2, stage 1) is connected to the input $Ui(2,1)$ of the stage (ring 2, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1..

The stage (ring 2, stage “n-1”) consists of 4 inputs namely $Ri(2,2n-1)$, $Ri(2,2n)$, $Ui(1,2n-1)$, and $Ui(1,2n)$; and 4 outputs $Bo(1,2n-1)$, $Bo(1,2n)$, $Fo(1,2n-1)$, and $Fo(1,2n)$. The stage (ring 2, stage “n-1”) also consists of eight 2:1 Muxes namely $R(2,2n-1)$, $R(2,2n)$, $F(2,2n-1)$, $F(1,2n)$, $U(1,2n-1)$, $U(1,2n)$, $B(1,2n-1)$, and $B(1,2n)$. The 2:1 Mux $R(2,2n-1)$ has two inputs namely $Ri(2,2n-1)$ and $Bo(2,2n-1)$ and has one output $Ro(2,2n-1)$. The 2:1 Mux $R(2,2n)$ has two inputs namely $Ri(2,2n)$ and $Bo(2,2n)$ and has one output $Ro(2,2n)$. The 2:1 Mux $F(2,2n-1)$ has two inputs namely $Ro(2,2n-1)$ and $Ro(2,2n)$ and has one output $Fo(2,2n-1)$. The 2:1 Mux $F(2,2n)$ has two inputs namely $Ro(2,2n-1)$ and $Ro(2,2n)$ and has one output $Fo(2,2n)$.

The 2:1 Mux $U(2,2n-1)$ has two inputs namely $Ui(2,2n-1)$ and $Fo(2,2n-1)$ and has one output $Uo(2,2n-1)$. The 2:1 Mux $U(2,2n)$ has two inputs namely $Ui(2,2n)$ and $Fo(2,2n)$ and has one output $Uo(2,2n)$. The 2:1 Mux $B(2,2n-1)$ has two inputs namely $Uo(2,2n-1)$ and $Uo(2,2n)$ and has one output $Bo(2,2n-1)$. The 2:1 Mux $B(2,2n)$ has two inputs namely $Uo(2,2n-1)$ and $Uo(2,2n)$ and has one output $Bo(2,2n)$.

The stage (ring 2, stage “n”) consists of 4 inputs namely $Ri(2,2n+1)$, $Ri(2,2n+2)$, $Ui(2,2n+1)$, and $Ui(2,2n+2)$; and 4 outputs $Bo(2,2n+1)$, $Bo(2,2n+2)$, $Fo(2,2n+1)$, and $Fo(2,2n+2)$. The stage (ring 2, stage “n”) also consists of eight 2:1 Muxes namely $R(2,2n+1)$, $R(2,2n+2)$, $F(2,2n+1)$, $F(2,2n+2)$, $U(2,2n+1)$, $U(2,2n+2)$, $B(2,2n+1)$, and $B(2,2n+2)$. The 2:1 Mux $R(2,2n+1)$ has two inputs namely $Ri(2,2n+1)$ and $Bo(2,2n+1)$ and has one output $Ro(2,2n+1)$. The 2:1 Mux $R(2,2n+2)$ has two inputs namely $Ri(2,2n+2)$ and $Bo(2,2n+2)$ and has one output $Ro(2,2n+2)$. The 2:1 Mux $F(2,2n+1)$ has two inputs namely $Ro(2,2n+1)$ and $Ro(2,2n+2)$ and has one output $Fo(2,2n+1)$. The 2:1 Mux $F(2,2n+2)$ has two inputs namely $Ro(2,2n+1)$ and $Ro(2,2n+2)$ and has one output $Fo(2,2n+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux U(2,2n+1) has two inputs namely $U_i(2,2n+1)$ and $F_o(2,2n+1)$ and has one output $U_o(2,2n+1)$. The 2:1 Mux U(2,2n+2) has two inputs namely $U_i(2,2n+2)$ and $F_o(2,2n+2)$ and has one output $U_o(2,2n+2)$. The 2:1 Mux B(2,2n+1) has two inputs namely $U_o(2,2n+1)$ and $U_o(2,2n+2)$ and has one output $B_o(2,2n+1)$. The 2:1 Mux
 5 B(2,2n+2) has two inputs namely $U_o(2,2n+1)$ and $U_o(2,2n+2)$ and has one output $B_o(2,2n+2)$.

The output $F_o(2,2n-1)$ of the stage (ring 2, stage "n-1") is connected to the input $R_i(2,2n+1)$ of the stage (ring 2, stage "n"), is an internal connection between stage "n-1" and stage "n" of the ring 1. And the output $B_o(2,2n+1)$ of the stage (ring 2, stage "n") is
 10 connected to the input $U_i(2,2n-1)$ of the stage (ring 2, stage "n-1"), is another internal connection between stage "n-1" and stage "n" of the ring 1.

Each stage of any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists of 4 inputs and $2 * d = 4$ outputs. Even though the stages (ring 1, stage 0), (ring 1, stage 1), (ring 2, stage "n-1"), and (ring 2, stage "n")
 15 each have eight 2:1 muxes, and the stages (ring 2, stage 0), (ring 2, stage 1), (ring 1, stage "m-1"), and (ring 1, stage "m") each have six 2:1 muxes, in other embodiments any of these stages can be one of the four by four switch diagrams namely 200A of FIG. 2A, 200B of FIG. 2B, 200C of FIG. 2C, and one of the eight by four switch diagrams namely 200E of FIG. 2E, 200F of FIG. 2F.

20 Referring to diagram 100B in FIG. 1B, in one embodiment, an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ where $N_1 = 400$; $N_2 = 800$; $d = 2$; and $s = 1$ corresponding to one computational block, with each computational block having 8 inlet links namely I1, I2, I3, I4, I5, I6, I7, and I8; and 4 outlet links namely O1, O2, O3, and O4. And for each computational block the corresponding partial multi-stage
 25 hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of two rings 110 and 120, where ring 110 consists of "m+1" stages namely (ring 1, stage 0), (ring 1, stage 1), ... (ring 1, stage "m-1"), and (ring 1, stage "m"), and ring 120 consists of "n+1" stages namely (ring 2, stage 0), (ring 2, stage 1), ... (ring 2, stage "n-1"), and (ring 2, stage "n"), where "m" and "n" are positive integers.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Ring 110 has inlet links $Ri(1,1)$ and $Ri(1,2)$ from the left-hand side, and has outlet links $Bo(1,1)$ and $Bo(1,2)$ from left-hand side. Ring 110 also has inlet links $Ui(1,2m+1)$ and $Ui(1,2m+2)$ from the right-hand side, and has outlet links $Fo(1,2m+1)$ and $Fo(1,2m+2)$ from right-hand side. Ring 120 has inlet links $Fi(2,1)$ and $Fi(2,2)$ from left-hand side, and outlet links $Bo(2,1)$ and $Bo(2,2)$ from left-hand side. Ring 120 also has inlet links $Ui(2,2n+1)$ and $Ui(2,2n+2)$ from the right-hand side, and has outlet links $Fo(2,2n+1)$ and $Fo(2,2n+2)$ from right-hand side.

And the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of 8 inlet links and 4 outlet links corresponding to the two rings 110 and 120. From left-hand side, outlet link O1 of the computational block is connected to inlet link $Ri(1,1)$ of ring 110 and also inlet link of $Fi(2,1)$ of ring 120. Similarly from left-hand side, outlet link O2 of the computational block is connected to inlet link $Ri(1,2)$ of Ring 110 and also inlet link of $Fi(2,2)$ of Ring 120. And from left-hand side, outlet link $Bo(1,1)$ of Ring 110 is connected to inlet link I1 of the computational block. From left-hand side, Outlet link $Bo(1,2)$ of Ring 110 is connected to inlet link I2 of the computational block. Similarly from left-hand side, outlet link $Bo(2,1)$ of Ring 120 is connected to inlet link I3 of the computational block. From left-hand side, outlet link $Bo(2,2)$ of Ring 120 is connected to inlet link I4 of the computational block.

From right-hand side, outlet link O3 of the computational block is connected to inlet link $Ui(1,2m+1)$ of ring 110 and also inlet link of $Ui(2,2n+1)$ of ring 120. Similarly from right-hand side, outlet link O4 of the computational block is connected to inlet link $Ui(1,2m+2)$ of Ring 110 and also inlet link of $Ui(2,2n+2)$ of Ring 120. And from right-hand side, outlet link $Fo(1,2m+1)$ of Ring 110 is connected to inlet link I5 of the computational block. From right-hand side, outlet link $Fo(1,2m+2)$ of Ring 110 is connected to inlet link I6 of the computational block. Similarly from right-hand side, outlet link $Fo(2,2n+1)$ of Ring 120 is connected to inlet link I7 of the computational block. From right-hand side, outlet link $Fo(2,2n+2)$ of Ring 120 is connected to inlet link I8 of the computational block.

Since in this embodiment outlet link O1 of the computational block is connected to both inlet link $Ri(1,1)$ of ring 110 and inlet link $Fi(2,1)$ of ring 120; outlet link O2 of the computational block is connected to both inlet link $Ri(1,2)$ of ring 110 and inlet link

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Fi(2,2) of ring 120; outlet link O3 of the computational block is connected to both inlet link Ui(1,2m+1) of ring 110 and inlet link Ui(2,2n+1) of ring 120; and outlet link O4 of the computational block is connected to both inlet link Ui(1,2m+2) of ring 110 and inlet link Ui(2,2n+2) of ring 120, the partial multi-stage hierarchical network

5 $V_{Comb}(N_1, N_2, d, s)$ 100B consists of 4 inlet links and 8 outlet links.

Referring to two dimensional grid 800 in FIG. 8 illustrates, in another embodiment, each block of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B with 4 inlet links and 8 outlet links and the corresponding computational block with 8 inlet links and 4 outlet links. For example
 10 block (1,1) of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B with 4 inlet links and 8 outlet links and the corresponding computational block with 8 inlet links and 4 outlet links. Similarly each of the 100 blocks of 2D-grid 800 has a separate partial multi-stage hierarchical network
 $V_{Comb}(N_1, N_2, d, s)$ 100B with 4 inlet links and 8 outlet links and the corresponding
 15 computational block with 8 inlet links and 4 outlet links. Hence the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to 2D-grid 800 has $N_1 = 400$ inlet links and $N_2 = 800$ outlet links. Since there are 100 computational blocks each one corresponding to one of the blocks with each computational block having 8 inlet links and 4 outlet links. Also the 2D-grid 800 is organized in the fourth quadrant of the 2D-Plane.
 20 In other embodiments the 2D-grid 800 may be organized as either first quadrant, or second quadrant or third quadrant of the 2D-Plane.

Referring to partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B in FIG. 1B, the stage (ring 1, stage 0) consists of 4 inputs namely Ri(1,1), Ri(1,2), Ui(1,1), and Ui(1,2); and 4 outputs Bo(1,1), Bo(1,2), Fo(1,1), and Fo(1,2). The stage (ring 1, stage
 25 0) also consists of eight 2:1 multiplexers (A multiplexer is hereinafter called a "mux") namely R(1,1), R(1,2), F(1,1), F(1,2), U(1,1), U(1,2), B(1,1), and B(1,2). The 2:1 Mux R(1,1) has two inputs namely Ri(1,1) and Bo(1,1) and has one output Ro(1,1). The 2:1 Mux R(1,2) has two inputs namely Ri(1,2) and Bo(1,2) and has one output Ro(1,2). The 2:1 Mux F(1,1) has two inputs namely Ro(1,1) and Ro(1,2) and has one output Fo(1,1).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux F(1,2) has two inputs namely Ro(1,1) and Ro(1,2) and has one output Fo(1,2).

The 2:1 Mux U(1,1) has two inputs namely Ui(1,1) and Fo(1,1) and has one output Uo(1,1). The 2:1 Mux U(1,2) has two inputs namely Ui(1,2) and Fo(1,2) and has one output Uo(1,2). The 2:1 Mux B(1,1) has two inputs namely Uo(1,1) and Uo(1,2) and has one output Bo(1,1). The 2:1 Mux B(1,2) has two inputs namely Uo(1,1) and Uo(1,2) and has one output Bo(1,2).

The stage (ring 1, stage 1) consists of 4 inputs namely Ri(1,3), Ri(1,4), Ui(1,3), and Ui(1,4); and 4 outputs Bo(1,3), Bo(1,4), Fo(1,3), and Fo(1,4). The stage (ring 1, stage 1) also consists of eight 2:1 Muxes namely R(1,3), R(1,4), F(1,3), F(1,4), U(1,3), U(1,4), B(1,3), and B(1,4). The 2:1 Mux R(1,3) has two inputs namely Ri(1,3) and Bo(1,3) and has one output Ro(1,3). The 2:1 Mux R(1,4) has two inputs namely Ri(1,4) and Bo(1,4) and has one output Ro(1,4). The 2:1 Mux F(1,3) has two inputs namely Ro(1,3) and Ro(1,4) and has one output Fo(1,3). The 2:1 Mux F(1,4) has two inputs namely Ro(1,3) and Ro(1,4) and has one output Fo(1,4).

The 2:1 Mux U(1,3) has two inputs namely Ui(1,3) and Fo(1,3) and has one output Uo(1,3). The 2:1 Mux U(1,4) has two inputs namely Ui(1,4) and Fo(1,4) and has one output Uo(1,4). The 2:1 Mux B(1,3) has two inputs namely Uo(1,3) and Uo(1,4) and has one output Bo(1,3). The 2:1 Mux B(1,4) has two inputs namely Uo(1,3) and Uo(1,4) and has one output Bo(1,4).

The output Fo(1,1) of the stage (ring 1, stage 0) is connected to the input Ri(1,3) of the stage (ring 1, stage 1) which is called hereinafter an internal connection between two successive stages of a ring. And the output Bo(1,3) of the stage (ring 1, stage 1) is connected to the input Ui(1,1) of the stage (ring 1, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1.

The stage (ring 1, stage "m-1") consists of 4 inputs namely Fi(1,2m-1), Fi(1,2m), Ui(1,2m-1), and Ui(1,2m); and 4 outputs Bo(1,2m-1), Bo(1,2m), Fo(1,2m-1), and Fo(1,2m). The stage (ring 1, stage "m-1") also consists of six 2:1 Muxes namely F(1,2m-1), F(1,2m), U(1,2m-1), U(1,2m), B(1,2m-1), and B(1,2m). The 2:1 Mux F(1,2m-1) has

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

two inputs namely $F_i(1,2m-1)$ and $F_i(1,2m)$ and has one output $F_o(1,2m-1)$. The 2:1 Mux $F(1,2m)$ has two inputs namely $F_i(1,2m-1)$ and $F_i(1,2m)$ and has one output $F_o(1,2m)$.

The 2:1 Mux $U(1,2m-1)$ has two inputs namely $U_i(1,2m-1)$ and $F_o(1,2m-1)$ and has one output $U_o(1,2m-1)$. The 2:1 Mux $U(1,2m)$ has two inputs namely $U_i(1,2m)$ and $F_o(1,2m)$ and has one output $U_o(1,2m)$. The 2:1 Mux $B(1,2m-1)$ has two inputs namely $U_o(1,2m-1)$ and $U_o(1,2m)$ and has one output $B_o(1,2m-1)$. The 2:1 Mux $B(1,2m)$ has two inputs namely $U_o(1,2m-1)$ and $U_o(1,2m)$ and has one output $B_o(1,2m)$.

The stage (ring 1, stage "m") consists of 4 inputs namely $F_i(1,2m+1)$, $F_i(1,2m+2)$, $U_i(1,2m+1)$, and $U_i(1,2m+2)$; and 4 outputs $B_o(1,2m+1)$, $B_o(1,2m+2)$, $F_o(1,2m+1)$, and $F_o(1,2m+2)$. The stage (ring 1, stage "m") also consists of six 2:1 Muxes namely $F(1,2m+1)$, $F(1,2m+2)$, $U(1,2m+1)$, $U(1,2m+2)$, $B(1,2m+1)$, and $B(1,2m+2)$. The 2:1 Mux $F(1,2m+1)$ has two inputs namely $F_i(1,2m+1)$ and $F_i(1,2m+2)$ and has one output $F_o(1,2m+1)$. The 2:1 Mux $F(1,2m+2)$ has two inputs namely $F_i(1,2m+1)$ and $F_i(1,2m+2)$ and has one output $F_o(1,2m+2)$.

The 2:1 Mux $U(1,2m+1)$ has two inputs namely $U_i(1,2m+1)$ and $F_o(1,2m+1)$ and has one output $U_o(1,2m+1)$. The 2:1 Mux $U(1,2m+2)$ has two inputs namely $U_i(1,2m+2)$ and $F_o(1,2m+2)$ and has one output $U_o(1,2m+2)$. The 2:1 Mux $B(1,2m+1)$ has two inputs namely $U_o(1,2m+1)$ and $U_o(1,2m+2)$ and has one output $B_o(1,2m+1)$. The 2:1 Mux $B(1,2m+2)$ has two inputs namely $U_o(1,2m+1)$ and $U_o(1,2m+2)$ and has one output $B_o(1,2m+2)$.

The output $F_o(1,2m-1)$ of the stage (ring 1, stage "m-1") is connected to the input $F_i(1,2m+1)$ of the stage (ring 1, stage "m"), is an internal connection between stage "m-1" and stage "m" of the ring 1. And the output $B_o(1,2m+1)$ of the stage (ring 1, stage "m") is connected to the input $U_i(1,2m-1)$ of the stage (ring 1, stage "m-1"), is another internal connection between stage "m-1" and stage "m" of the ring 1

Just the same way the stages (ring 1, stage 0), (ring 1, stage 1), there are also stages (ring 1, stage 2), (ring 1, stage 3), ... (ring 1, stage "m-1"), (ring 1, stage "m") in that order, where the stages from (ring 1, stage 2), (ring 1, stage 3), ... , (ring 1, stage "m-2") are not shown in the diagram 100B. Just the same way the two successive stages (ring 1, stage 0) and (ring 1, stage 1) have internal connections between them as described

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

before, any two successive stages have similar internal connections. For example (ring 1, stage 1) and (ring 1, stage 2) have similar internal connections and (ring 1, stage “m-2”) and (ring 1, stage “m-1”) have similar internal connections.

Stage (ring 1, stage 0) is also called hereinafter the “entry stage” or “first stage” of ring 1, since inlet links and outlet links of the computational block are directly connected to stage (ring 1, stage 0). Also stage (ring 1, stage “m”) is hereinafter the “last stage” or “root stage” of ring 1.

The stage (ring 2, stage 0) consists of 4 inputs namely $F_i(2,1)$, $F_i(2,2)$, $U_i(2,1)$, and $U_i(2,2)$; and 4 outputs $B_o(2,1)$, $B_o(2,2)$, $F_o(2,1)$, and $F_o(2,2)$. The stage (ring 2, stage 0) also consists of six 2:1 Muxes namely $F(2,1)$, $F(2,2)$, $U(2,1)$, $U(2,2)$, $B(2,1)$, and $B(2,2)$. The 2:1 Mux $F(2,1)$ has two inputs namely $F_i(2,1)$ and $F_i(2,2)$ and has one output $F_o(2,1)$. The 2:1 Mux $F(2,2)$ has two inputs namely $F_i(2,1)$ and $F_i(2,2)$ and has one output $F_o(2,2)$.

The 2:1 Mux $U(2,1)$ has two inputs namely $U_i(2,1)$ and $F_o(2,1)$ and has one output $U_o(2,1)$. The 2:1 Mux $U(2,2)$ has two inputs namely $U_i(2,2)$ and $F_o(2,2)$ and has one output $U_o(2,2)$. The 2:1 Mux $B(2,1)$ has two inputs namely $U_o(2,1)$ and $U_o(2,2)$ and has one output $B_o(2,1)$. The 2:1 Mux $B(2,2)$ has two inputs namely $U_o(2,1)$ and $U_o(2,2)$ and has one output $B_o(2,2)$.

The stage (ring 2, stage 1) consists of 4 inputs namely $F_i(2,3)$, $F_i(2,4)$, $U_i(2,3)$, and $U_i(2,4)$; and 4 outputs $B_o(2,3)$, $B_o(2,4)$, $F_o(2,3)$, and $F_o(2,4)$. The stage (ring 2, stage 1) also consists of six 2:1 Muxes namely $F(2,3)$, $F(2,4)$, $U(2,3)$, $U(2,4)$, $B(2,3)$, and $B(2,4)$. The 2:1 Mux $F(2,3)$ has two inputs namely $F_i(2,3)$ and $F_i(2,4)$ and has one output $F_o(2,3)$. The 2:1 Mux $F(2,4)$ has two inputs namely $F_i(2,3)$ and $F_i(2,4)$ and has one output $F_o(2,4)$.

The 2:1 Mux $U(2,3)$ has two inputs namely $U_i(2,3)$ and $F_o(2,3)$ and has one output $U_o(2,3)$. The 2:1 Mux $U(2,4)$ has two inputs namely $U_i(2,4)$ and $F_o(2,4)$ and has one output $U_o(2,4)$. The 2:1 Mux $B(2,3)$ has two inputs namely $U_o(2,3)$ and $U_o(2,4)$ and has one output $B_o(2,3)$. The 2:1 Mux $B(2,4)$ has two inputs namely $U_o(2,3)$ and $U_o(2,4)$ and has one output $B_o(2,4)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The output $Fo(2,1)$ of the stage (ring 2, stage 0) is connected to the input $Fi(2,3)$ of the stage (ring 2, stage 1), is an internal connection between stage 0 and stage 1 of the ring 2. And the output $Bo(2,3)$ of the stage (ring 2, stage 1) is connected to the input $Ui(2,1)$ of the stage (ring 2, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1..

The stage (ring 2, stage “n-1”) consists of 4 inputs namely $Ri(2,2n-1)$, $Ri(2,2n)$, $Ui(1,2n-1)$, and $Ui(1,2n)$; and 4 outputs $Bo(1,2n-1)$, $Bo(1,2n)$, $Fo(1,2n-1)$, and $Fo(1,2n)$. The stage (ring 2, stage “n-1”) also consists of eight 2:1 Muxes namely $R(2,2n-1)$, $R(2,2n)$, $F(2,2n-1)$, $F(1,2n)$, $U(1,2n-1)$, $U(1,2n)$, $B(1,2n-1)$, and $B(1,2n)$. The 2:1 Mux $R(2,2n-1)$ has two inputs namely $Ri(2,2n-1)$ and $Bo(2,2n-1)$ and has one output $Ro(2,2n-1)$. The 2:1 Mux $R(2,2n)$ has two inputs namely $Ri(2,2n)$ and $Bo(2,2n)$ and has one output $Ro(2,2n)$. The 2:1 Mux $F(2,2n-1)$ has two inputs namely $Ro(2,2n-1)$ and $Ro(2,2n)$ and has one output $Fo(2,2n-1)$. The 2:1 Mux $F(2,2n)$ has two inputs namely $Ro(2,2n-1)$ and $Ro(2,2n)$ and has one output $Fo(2,2n)$.

The 2:1 Mux $U(2,2n-1)$ has two inputs namely $Ui(2,2n-1)$ and $Fo(2,2n-1)$ and has one output $Uo(2,2n-1)$. The 2:1 Mux $U(2,2n)$ has two inputs namely $Ui(2,2n)$ and $Fo(2,2n)$ and has one output $Uo(2,2n)$. The 2:1 Mux $B(2,2n-1)$ has two inputs namely $Uo(2,2n-1)$ and $Uo(2,2n)$ and has one output $Bo(2,2n-1)$. The 2:1 Mux $B(2,2n)$ has two inputs namely $Uo(2,2n-1)$ and $Uo(2,2n)$ and has one output $Bo(2,2n)$.

The stage (ring 2, stage “n”) consists of 4 inputs namely $Ri(2,2n+1)$, $Ri(2,2n+2)$, $Ui(2,2n+1)$, and $Ui(2,2n+2)$; and 4 outputs $Bo(2,2n+1)$, $Bo(2,2n+2)$, $Fo(2,2n+1)$, and $Fo(2,2n+2)$. The stage (ring 2, stage “n”) also consists of eight 2:1 Muxes namely $R(2,2n+1)$, $R(2,2n+2)$, $F(2,2n+1)$, $F(2,2n+2)$, $U(2,2n+1)$, $U(2,2n+2)$, $B(2,2n+1)$, and $B(2,2n+2)$. The 2:1 Mux $R(2,2n+1)$ has two inputs namely $Ri(2,2n+1)$ and $Bo(2,2n+1)$ and has one output $Ro(2,2n+1)$. The 2:1 Mux $R(2,2n+2)$ has two inputs namely $Ri(2,2n+2)$ and $Bo(2,2n+2)$ and has one output $Ro(2,2n+2)$. The 2:1 Mux $F(2,2n+1)$ has two inputs namely $Ro(2,2n+1)$ and $Ro(2,2n+2)$ and has one output $Fo(2,2n+1)$. The 2:1 Mux $F(2,2n+2)$ has two inputs namely $Ro(2,2n+1)$ and $Ro(2,2n+2)$ and has one output $Fo(2,2n+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux U(2,2n+1) has two inputs namely $U_i(2,2n+1)$ and $F_o(2,2n+1)$ and has one output $U_o(2,2n+1)$. The 2:1 Mux U(2,2n+2) has two inputs namely $U_i(2,2n+2)$ and $F_o(2,2n+2)$ and has one output $U_o(2,2n+2)$. The 2:1 Mux B(2,2n+1) has two inputs namely $U_o(2,2n+1)$ and $U_o(2,2n+2)$ and has one output $B_o(2,2n+1)$. The 2:1 Mux
 5 B(2,2n+2) has two inputs namely $U_o(2,2n+1)$ and $U_o(2,2n+2)$ and has one output $B_o(2,2n+2)$.

The output $F_o(2,2n-1)$ of the stage (ring 2, stage "n-1") is connected to the input $R_i(2,2n+1)$ of the stage (ring 2, stage "n"), is an internal connection between stage "n-1" and stage "n" of the ring 1. And the output $B_o(2,2n+1)$ of the stage (ring 2, stage "n") is connected to the input $U_i(2,2n-1)$ of the stage (ring 2, stage "n-1"), is another internal
 10 connection between stage "n-1" and stage "n" of the ring 1.

Each stage of any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of $2 * d = 4$ outputs. Even though each stage has four 4:1 muxes, in other embodiments any of these stages can be one of the four by four
 15 switch diagrams namely 200A of FIG. 2A, 200B of FIG. 2B, 200C of FIG. 2C, and one of the eight by four switch diagrams namely 200E of FIG. 2E, 200F of FIG. 2F.

In general, any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ may have inputs and outputs connected from computational block from either only from left-hand side as in the partial multi-stage hierarchical network
 20 $V_{Comb}(N_1, N_2, d, s)$ 100A; or only from right-hand side; or from both left-hand and right-hand sides as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B.

Referring to diagram 100C in FIG. 1C, in one embodiment, an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ where $N_1 = 400$; $N_2 = 1600$; $d = 2$; and $s = 1$ corresponding to one computational block, with each computational block
 25 having 16 inlet links namely I1, I2, I3, I4, I5, I6, I7, I8, I9, I10, I11, I12, I13, I14, I15, and I16; and 4 outlet links namely O1, O2, O3, and O4. And for each computational block the corresponding partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C consists of two slices namely slice 1 and slice 2. Slice 1 consists of two rings namely

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

(slice 1, ring 1) and (slice 1, ring 2). Similarly slice 2 consists of two rings namely (slice 2, ring 1) and (slice 2, ring 2).

The ring (slice 1, ring 1) consists of “ $m+1$ ” stages namely (slice 1, ring 1, stage 0), (slice 1, ring 1, stage 1), ... (slice 1, ring 1, stage “ $m-1$ ”), and (slice 1, ring 1, stage “ m ”).
 5 And the ring (slice 1, ring 2) consists of “ $n+1$ ” stages namely (slice 1, ring 2, stage 0), (slice 1, ring 2, stage 1), ... (slice 1, ring 2, stage “ $n-1$ ”), and (slice 1, ring 2, stage “ n ”), where “ m ” and “ n ” are positive integers.

Similarly the ring (slice 2, ring 1) consists of “ $x+1$ ” stages namely (slice 2, ring 1, stage 0), (slice 2, ring 1, stage 1), ... (slice 2, ring 1, stage “ $x-1$ ”), and (slice 2, ring 1, stage “ x ”).
 10 And the ring (slice 2, ring 2) consists of “ $y+1$ ” stages namely (slice 2, ring 2, stage 0), (slice 2, ring 2, stage 1), ... (slice 2, ring 2, stage “ $y-1$ ”), and (slice 2, ring 2, stage “ y ”), where “ x ” and “ y ” are positive integers.

In general “ m ” may be or may not be equal to “ x ” and “ n ” may be or may not be equal to “ y ”. Also in general, “ m ” may be or may not be equal to “ n ” and “ x ” may be or
 15 may not be equal to “ y ”.

Ring (slice 1, ring 1) has inlet links $Ri(1,1,1)$ and $Ri(1,1,2)$ from the left-hand side, and has outlet links $Bo(1,1,1)$ and $Bo(1,1,2)$ from left-hand side. Ring (slice 1, ring 1) also has inlet links $Ui(1,1,2m+1)$ and $Ui(1,1,2m+2)$ from the right-hand side, and has outlet links $Fo(1,1,2m+1)$ and $Fo(1,1,2m+2)$ from right-hand side. Ring (slice 1, ring 2)
 20 has inlet links $Ri(1,2,1)$ and $Ri(1,2,2)$ from left-hand side, and outlet links $Bo(1,2,1)$ and $Bo(1,2,2)$ from left-hand side. Ring (slice 1, ring 2) also has inlet links $Ui(1,2,2n+1)$ and $Ui(1,2,2n+2)$ from the right-hand side, and has outlet links $Fo(1,2,2n+1)$ and $Fo(1,2,2n+2)$ from right-hand side.

Ring (slice 2, ring 1) has inlet links $Ri(2,1,1)$ and $Ri(2,1,2)$ from the left-hand side, and has outlet links $Bo(2,1,1)$ and $Bo(2,1,2)$ from left-hand side. Ring (slice 2, ring 1) also has inlet links $Ui(2,1,2x+1)$ and $Ui(2,1,2x+2)$ from the right-hand side, and has outlet links $Fo(2,1,2x+1)$ and $Fo(2,1,2x+2)$ from right-hand side. Ring (slice 2, ring 2)
 25 has inlet links $Ri(2,2,1)$ and $Ri(2,2,2)$ from left-hand side, and outlet links $Bo(2,2,1)$ and $Bo(2,2,2)$ from left-hand side. Ring (slice 2, ring 2) also has inlet links $Ui(2,2,2y+1)$ and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$U_i(2,2,2y+2)$ from the right-hand side, and has outlet links $F_o(2,2,2y+1)$ and $F_o(2,2,2y+2)$ from right-hand side.

And the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C consists of 16 inlet links and 4 outlet links corresponding to the two slices slice 1 and slice 2.

5 From left-hand side, outlet link O1 of the computational block is connected to inlet link $R_i(1,1,1)$ of ring (slice 1, ring 1) and also inlet link of $R_i(1,2,1)$ of ring (slice 1, ring 2). Similarly from left-hand side, outlet link O2 of the computational block is connected to inlet link $R_i(1,1,2)$ of Ring (slice 1, ring 1) and also inlet link of $R_i(1,2,2)$ of Ring (slice 1, ring 2). And from left-hand side, outlet link $B_o(1,1,1)$ of Ring (slice 1, ring 1) is
 10 connected to inlet link I1 of the computational block. From left-hand side, Outlet link $B_o(1,1,2)$ of Ring (slice 1, ring 1) is connected to inlet link I2 of the computational block. Similarly from left-hand side, outlet link $B_o(1,2,1)$ of Ring (slice 1, ring 2) is connected to inlet link I3 of the computational block. From left-hand side, outlet link $B_o(1,2,2)$ of Ring (slice 1, ring 2) is connected to inlet link I4 of the computational block.

15 From right-hand side, outlet link O1 of the computational block is connected to inlet link $U_i(1,1,2m+1)$ of ring (slice 1, ring 1) and also inlet link of $U_i(1,2,2n+1)$ of ring (slice 1, ring 2). Similarly from right-hand side, outlet link O2 of the computational block is connected to inlet link $U_i(1,1,2m+2)$ of Ring (slice 1, ring 1) and also inlet link of $U_i(1,2,2n+2)$ of Ring (slice 1, ring 2). And from right-hand side, outlet link $F_o(1,1,2m+1)$
 20 of Ring (slice 1, ring 1) is connected to inlet link I5 of the computational block. From right-hand side, outlet link $F_o(1,1,2m+2)$ of Ring (slice 1, ring 1) is connected to inlet link I6 of the computational block. Similarly from right-hand side, outlet link $F_o(1,2,2n+1)$ of Ring (slice 1, ring 2) is connected to inlet link I7 of the computational block. From right-hand side, outlet link $F_o(1,2,2n+2)$ of Ring (slice 1, ring 2) is
 25 connected to inlet link I8 of the computational block.

From left-hand side, outlet link O3 of the computational block is connected to inlet link $R_i(2,1,1)$ of ring (slice 2, ring 1) and also inlet link of $R_i(2,2,1)$ of ring (slice 2, ring 2). Similarly from left-hand side, outlet link O4 of the computational block is connected to inlet link $R_i(2,1,2)$ of Ring (slice 2, ring 1) and also inlet link of $R_i(2,2,2)$ of
 30 Ring (slice 2, ring 2). And from left-hand side, outlet link $B_o(2,1,1)$ of Ring (slice 2, ring 1) is connected to inlet link I9 of the computational block. From left-hand side, Outlet

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

link Bo(2,1,2) of Ring (slice 2, ring 1) is connected to inlet link I10 of the computational block. Similarly from left-hand side, outlet link Bo(2,2,1) of Ring (slice 2, ring 2) is connected to inlet link I11 of the computational block. From left-hand side, outlet link Bo(2,2,2) of Ring (slice 2, ring 2) is connected to inlet link I12 of the computational
5 block.

From right-hand side, outlet link O3 of the computational block is connected to inlet link Ui(2,1,2x+1) of ring (slice 2, ring 1) and also inlet link of Ui(2,2,2y+1) of ring (slice 2, ring 2). Similarly from right-hand side, outlet link O4 of the computational block is connected to inlet link Ui(2,1,2x+2) of Ring (slice 2, ring 1) and also inlet link of
10 Ui(2,2,2y+2) of Ring (slice 2, ring 2). And from right-hand side, outlet link Fo(2,1,2x+1) of Ring (slice 2, ring 1) is connected to inlet link I13 of the computational block. From right-hand side, outlet link Fo(2,1,2x+2) of Ring (slice 2, ring 1) is connected to inlet link I14 of the computational block. Similarly from right-hand side, outlet link Fo(2,2,2y+1) of Ring (slice 2, ring 2) is connected to inlet link I15 of the computational block. From
15 right-hand side, outlet link Fo(2,2,2y+2) of Ring (slice 2, ring 2) is connected to inlet link I16 of the computational block.

In this embodiment outlet links O1 and O2 of the computational block are connected only to slice 1. Similarly outlet links O3 and O4 of the computational block are connected only to slice 2.

Referring to two dimensional grid 800 in FIG. 8 illustrates, in another
20 embodiment, each block of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C with 4 inlet links and 16 outlet links and the corresponding computational block with 16 inlet links and 4 outlet links. For example block (1,1) of 2D-grid 800 consists of one of the partial multi-stage hierarchical network
25 $V_{Comb}(N_1, N_2, d, s)$ 100C with 4 inlet links and 16 outlet links and the corresponding computational block with 16 inlet links and 4 outlet links. Similarly each of the 100 blocks of 2D-grid 800 has a separate partial multi-stage hierarchical network
 $V_{Comb}(N_1, N_2, d, s)$ 100C with 4 inlet links and 16 outlet links and the corresponding
computational block with 16 inlet links and 4 outlet links. Hence the complete multi-stage
30 hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to 2D-grid 800 has $N_1 = 400$ inlet

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

links and $N_2 = 1600$ outlet links. Since there are 100 computational blocks each one corresponding to one of the blocks with each computational block having 16 inlet links and 4 outlet links. Also the 2D-grid 800 is organized in the fourth quadrant of the 2D-Plane. In other embodiments the 2D-grid 800 may be organized as either first quadrant, or
 5 second quadrant or third quadrant of the 2D-Plane.

Referring to partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C, the stage (slice 1, ring 1, stage 0) consists of 8 inputs namely $Ri(1,1,1)$, $Ri(1,1,2)$, $Ui(1,1,1)$, $Ui(1,1,2)$, $J(1,1,1)$, $K(1,1,1)$, $L(1,1,1)$, and $M(1,1,1)$; and 4 outputs $Bo(1,1,1)$, $Bo(1,1,2)$, $Fo(1,1,1)$, and $Fo(1,1,2)$. The stage (slice 1, ring "1", stage "0") also
 10 consists of four 4:1 Muxes namely $F(1,1,1)$, $F(1,1,2)$, $B(1,1,1)$, and $B(1,1,2)$. The 4:1 Mux $F(1,1,1)$ has four inputs namely $Ri(1,1,1)$, $Ri(1,1,2)$, $Ui(1,1,2)$, and $J(1,1,1)$, and has one output $Fo(1,1,1)$. The 4:1 Mux $F(1,1,2)$ has four inputs namely $Ri(1,1,1)$, $Ri(1,1,2)$, $Ui(1,1,1)$, and $K(1,1,1)$, and has one output $Fo(1,1,2)$.

The 4:1 Mux $B(1,1,1)$ has four inputs namely $Ui(1,1,1)$, $Ui(1,1,2)$, $Ri(1,1,2)$, and
 15 $L(1,1,1)$, and has one output $Bo(1,1,1)$. The 4:1 Mux $B(1,1,2)$ has four inputs namely $Ui(1,1,1)$, $Ui(1,1,2)$, $Ri(1,1,1)$ and $M(1,1,1)$, and has one output $Bo(1,1,2)$. In different embodiments the inputs $J(1,1,1)$, $K(1,1,1)$, $L(1,1,1)$, and $M(1,1,1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 1, ring 1, stage "m") consists of 8 inputs namely $Ri(1,1,2m+1)$,
 20 $Ri(1,1,2m+2)$, $Ui(1,1,2m+1)$, $Ui(1,1,2m+2)$, $J(1,1,m+1)$, $K(1,1,m+1)$, $L(1,1,m+1)$, and $M(1,1,m+1)$; and 4 outputs $Bo(1,1,2m+1)$, $Bo(1,1,2m+2)$, $Fo(1,1,2m+1)$, and $Fo(1,1,2m+2)$. The stage (slice 1, ring 1, stage "m") also consists of four 4:1 Muxes namely $F(1,1,2m+1)$, $F(1,1,2m+2)$, $B(1,1,2m+1)$, and $B(1,1,2m+2)$. The 4:1 Mux
 25 $F(1,1,2m+1)$ has four inputs namely $Ri(1,1,2m+1)$, $Ri(1,1,2m+2)$, $Ui(1,1,2m+2)$, and $J(1,1,m+1)$, and has one output $Fo(1,1,2m+1)$. The 4:1 Mux $F(1,1,2m+2)$ has four inputs namely $Ri(1,1,2m+1)$, $Ri(1,1,2m+2)$, $Ui(1,1,2m+1)$, and $K(1,1,m+1)$, and has one output $Fo(1,1,2m+2)$.

The 4:1 Mux $B(1,1,2m+1)$ has four inputs namely $Ui(1,1,2m+1)$, $Ui(1,1,2m+2)$,
 30 $Ri(1,1,2m+2)$, and $L(1,1,m+1)$, and has one output $Bo(1,1,2m+1)$. The 4:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

B(1,1,2m+2) has four inputs namely $U_i(1,1,2m+1)$, $U_i(1,1,2m+2)$, $R_i(1,1,2m+1)$ and $M(1,1,m+1)$, and has one output $Bo(1,1,2m+2)$. In different embodiments the inputs $J(1,1,m+1)$, $K(1,1,m+1)$, $L(1,1,m+1)$, and $M(1,1,m+1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical
 5 network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 1, ring 1, stage 0), there are also stages (slice 1, ring 1, stage 1), (slice 1, ring 1, stage 2), (slice 1, ring 1, stage 3), ... (slice 1, ring 1, stage "m-1"), (slice 1, ring 1, stage "m") in that order, where the stages from (slice 1, ring 1, stage 1), (slice 1, ring 1, stage 2), ... , (slice 1, ring 1, stage "m-1") are not shown in the
 10 diagram 100C.

Referring to diagram 100C5 in FIG. 1C5 illustrates specific details of partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C, particularly the internal connections between two successive stages of any ring of any slice, in one embodiment. The stage (slice "c", ring "d", stage "e") consists of 8 inputs namely
 15 $R_i(c,d,2e+1)$, $R_i(c,d,2e+2)$, $U_i(c,d,2e+1)$, $U_i(c,d,2e+2)$, $J(c,d,e+1)$, $K(c,d,e+1)$, $L(c,d,e+1)$, and $M(c,d,e+1)$; and 4 outputs $Bo(c,d,2e+1)$, $Bo(c,d,2e+2)$, $Fo(c,d,2e+1)$, and $Fo(c,d,2e+2)$. The stage (slice "c", ring "d", stage "e") also consists of four 4:1 Muxes namely $F(c,d,2e+1)$, $F(c,d,2e+2)$, $B(c,d,2e+1)$, and $B(c,d,2e+2)$. The 4:1 Mux $F(c,d,2e+1)$ has four inputs namely $R_i(c,d,2e+1)$, $R_i(c,d,2e+2)$, $U_i(c,d,2e+2)$, and $J(c,d,e+1)$, and has
 20 one output $Fo(c,d,2e+1)$. The 4:1 Mux $F(c,d,2e+2)$ has four inputs namely $R_i(c,d,2e+1)$, $R_i(c,d,2e+2)$, $U_i(c,d,2e+1)$, and $K(c,d,e+1)$, and has one output $Fo(c,d,2e+2)$.

The 4:1 Mux $B(c,d,2e+1)$ has four inputs namely $U_i(c,d,2e+1)$, $U_i(c,d,2e+2)$, $R_i(c,d,2e+2)$, and $L(c,d,e+1)$, and has one output $Bo(c,d,2e+1)$. The 4:1 Mux $B(c,d,2e+2)$ has four inputs namely $U_i(c,d,2e+1)$, $U_i(c,d,2e+2)$, $R_i(c,d,2e+1)$ and $M(c,d,e+1)$, and has
 25 one output $Bo(c,d,2e+2)$. In different embodiments the inputs $J(c,d,e+1)$, $K(c,d,e+1)$, $L(c,d,e+1)$, and $M(c,d,e+1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice "c", ring "d", stage "e+1") consists of 8 inputs namely
 30 $R_i(c,d,2e+3)$, $R_i(c,d,2e+4)$, $U_i(c,d,2e+3)$, $U_i(c,d,2e+4)$, $J(c,d,e+2)$, $K(c,d,e+2)$, $L(c,d,e+2)$, and $M(c,d,e+2)$; and 4 outputs $Bo(c,d,2e+3)$, $Bo(c,d,2e+4)$, $Fo(c,d,2e+3)$, and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Fo(c,d,2e+4). The stage (slice “c”, ring “d”, stage “e+1”) also consists of four 4:1 Muxes namely F(c,d,2e+3), F(c,d,2e+4), B(c,d,2e+3), and B(c,d,2e+4). The 4:1 Mux F(c,d,2e+3) has four inputs namely Ri(c,d,2e+3), Ri(c,d,2e+4), Ui(c,d,2e+4), and J(c,d,e+2), and has one output Fo(c,d,2e+3). The 4:1 Mux F(c,d,2e+4) has four inputs namely Ri(c,d,2e+3),
 5 Ri(c,d,2e+4), Ui(c,d,2e+3), and K(c,d,e+2), and has one output Fo(c,d,2e+4).

The 4:1 Mux B(c,d,2e+3) has four inputs namely Ui(c,d,2e+3), Ui(c,d,2e+4), Ri(c,d,2e+4), and L(c,d,e+2), and has one output Bo(c,d,2e+3). The 4:1 Mux B(c,d,2e+4) has four inputs namely Ui(c,d,2e+3), Ui(c,d,2e+4), Ri(c,d,2e+3) and M(c,d,e+2), and has one output Bo(c,d,2e+4). In different embodiments the inputs J(c,d,e+2), K(c,d,e+2),
 10 L(c,d,e+2), and M(c,d,e+2) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The output Fo(c,d,2e+1) of the stage (slice “c”, ring “d”, stage “e”) is connected to the input Ri(c,d,2e+3) of the stage (slice “c”, ring “d”, stage “e+1”) which is called hereinafter an internal connection between two successive stages of a ring. And the
 15 output Bo(c,d,2e+3) of the stage (slice “c”, ring “d”, stage “e+1”) is connected to the input Ui(c,d,2e+1) of the stage (slice “c”, ring “d”, stage “e”), is another internal connection between stage “e” and stage “e+1” of the ring (slice “c”, ring “d”).

Just the same way the two successive stages (slice “c”, ring “d”, stage “e”) and (slice “c”, ring “d”, stage “e+1”) have internal connections between them as described
 20 above, any two successive stages have similar internal connections for any values of “c”, “d”, “e” of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C belonging to any block of the two dimensional grid 800 in FIG. 8, in some embodiments. For example stage (slice 1, ring 1, stage 0) and stage (slice 1, ring 1, stage 1) have similar internal connections; and stage (slice 1, ring 1, stage “m-1”) and stage
 25 (slice 1, ring 1, stage “m”) have similar internal connections.

Stage (slice 1, ring 1, stage 0) is also called hereinafter the “entry stage” or “first stage” of (slice 1, ring 1), since inlet links and outlet links of the computational block are directly connected to stage (slice 1, ring 1, stage 0). Also stage (slice 1, ring 1, stage “m”) is hereinafter the “last stage” or “root stage” of (slice 1, ring 1).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The stage (slice 1, ring 2, stage 0) consists of 8 inputs namely $Ri(1,2,1)$, $Ri(1,2,2)$, $Ui(1,2,1)$, $Ui(1,2,2)$, $J(1,2,1)$, $K(1,2,1)$, $L(1,2,1)$, and $M(1,2,1)$; and 4 outputs $Bo(1,2,1)$, $Bo(1,2,2)$, $Fo(1,2,1)$, and $Fo(1,2,2)$. The stage (slice 1, ring “2”, stage “0”) also consists of four 4:1 Muxes namely $F(1,2,1)$, $F(1,2,2)$, $B(1,2,1)$, and $B(1,2,2)$. The 4:1 Mux

5 $F(1,2,1)$ has four inputs namely $Ri(1,2,1)$, $Ri(1,2,2)$, $Ui(1,2,2)$, and $J(1,2,1)$, and has one output $Fo(1,2,1)$. The 4:1 Mux $F(1,2,2)$ has four inputs namely $Ri(1,2,1)$, $Ri(1,2,2)$, $Ui(1,2,1)$, and $K(1,2,1)$, and has one output $Fo(1,2,2)$.

The 4:1 Mux $B(1,2,1)$ has four inputs namely $Ui(1,2,1)$, $Ui(1,2,2)$, $Ri(1,2,2)$, and $L(1,2,1)$, and has one output $Bo(1,2,1)$. The 4:1 Mux $B(1,2,2)$ has four inputs namely

10 $Ui(1,2,1)$, $Ui(1,2,2)$, $Ri(1,2,1)$ and $M(1,2,1)$, and has one output $Bo(1,2,2)$. In different embodiments the inputs $J(1,2,1)$, $K(1,2,1)$, $L(1,2,1)$, and $M(1,2,1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 1, ring 2, stage “n”) consists of 8 inputs namely $Ri(1,2,2n+1)$,

15 $Ri(1,2,2n+2)$, $Ui(1,2,2n+1)$, $Ui(1,2,2n+2)$, $J(1,2,n+1)$, $K(1,2,n+1)$, $L(1,2,n+1)$, and $M(1,2,n+1)$; and 4 outputs $Bo(1,2,2n+1)$, $Bo(1,2,2n+2)$, $Fo(1,2,2n+1)$, and $Fo(1,2,2n+2)$. The stage (slice 1, ring 2, stage “n”) also consists of four 4:1 Muxes namely $F(1,2,2n+1)$, $F(1,2,2n+2)$, $B(1,2,2n+1)$, and $B(1,2,2n+2)$. The 4:1 Mux $F(1,2,2n+1)$ has four inputs namely $Ri(1,2,2n+1)$, $Ri(1,2,2n+2)$, $Ui(1,2,2n+2)$, and $J(1,2,n+1)$, and has one output

20 $Fo(1,2,2n+1)$. The 4:1 Mux $F(1,2,2n+2)$ has four inputs namely $Ri(1,2,2n+1)$, $Ri(1,2,2n+2)$, $Ui(1,2,2n+1)$, and $K(1,2,n+1)$, and has one output $Fo(1,2,2n+2)$.

The 4:1 Mux $B(1,2,2n+1)$ has four inputs namely $Ui(1,2,n+1)$, $Ui(1,2,2n+2)$, $Ri(1,2,2n+2)$, and $L(1,2,n+1)$, and has one output $Bo(1,2,2n+1)$. The 4:1 Mux

25 $B(1,2,2n+2)$ has four inputs namely $Ui(1,2,2n+1)$, $Ui(1,2,2n+2)$, $Ri(1,2,2n+1)$ and $M(1,2,n+1)$, and has one output $Bo(1,2,2n+2)$. In different embodiments the inputs $J(1,2,n+1)$, $K(1,2,n+1)$, $L(1,2,n+1)$, and $M(1,2,n+1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 1, ring 2, stage 0), there are also stages (slice 1,

30 ring 2, stage 1), (slice 1, ring 2, stage 2), (slice 1, ring 2, stage 3), ... (slice 1, ring 2, stage

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

“n-1”), (slice 1, ring 2, stage “n”) in that order, where the stages from (slice 1, ring 2, stage 1), (slice 1, ring 2, stage 2), ... , (slice 1, ring 2, stage “n-1”) are not shown in the diagram 100C.

The stage (slice 2, ring 1, stage 0) consists of 8 inputs namely $R_i(2,1,1)$, $R_i(2,1,2)$,
 5 $U_i(2,1,1)$, $U_i(2,1,2)$, $J(2,1,1)$, $K(2,1,1)$, $L(2,1,1)$, and $M(2,1,1)$; and 4 outputs $B_o(2,1,1)$,
 $B_o(2,1,2)$, $F_o(2,1,1)$, and $F_o(2,1,2)$. The stage (slice 2, ring “1”, stage “0”) also consists
 of four 4:1 Muxes namely $F(2,1,1)$, $F(2,1,2)$, $B(2,1,1)$, and $B(2,1,2)$. The 4:1 Mux
 $F(2,1,1)$ has four inputs namely $R_i(2,1,1)$, $R_i(2,1,2)$, $U_i(2,1,2)$, and $J(2,1,1)$, and has one
 output $F_o(2,1,1)$. The 4:1 Mux $F(2,1,2)$ has four inputs namely $R_i(2,1,1)$, $R_i(2,1,2)$,
 10 $U_i(2,1,1)$, and $K(2,1,1)$, and has one output $F_o(2,1,2)$.

The 4:1 Mux $B(2,1,1)$ has four inputs namely $U_i(2,1,1)$, $U_i(2,1,2)$, $R_i(2,1,2)$, and
 $L(2,1,1)$, and has one output $B_o(2,1,1)$. The 4:1 Mux $B(2,1,2)$ has four inputs namely
 $U_i(2,1,1)$, $U_i(2,1,2)$, $R_i(2,1,1)$ and $M(2,1,1)$, and has one output $B_o(2,1,2)$. In different
 embodiments the inputs $J(2,1,1)$, $K(2,1,1)$, $L(2,1,1)$, and $M(2,1,1)$ are connected from any
 15 of the outputs of any other stages of any ring of any block of the multi-stage hierarchical
 network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 2, ring 1, stage “x”) consists of 8 inputs namely $R_i(2,1,2x+1)$,
 $R_i(2,1,2x+2)$, $U_i(2,1,2x+1)$, $U_i(2,1,2x+2)$, $J(2,1,x+1)$, $K(2,1,x+1)$, $L(2,1,x+1)$, and
 $M(2,1,x+1)$; and 4 outputs $B_o(2,1,2x+1)$, $B_o(2,1,2x+2)$, $F_o(2,1,2x+1)$, and $F_o(2,1,2x+2)$.
 20 The stage (slice 2, ring 1, stage “x”) also consists of four 4:1 Muxes namely $F(2,1,2x+1)$,
 $F(2,1,2x+2)$, $B(2,1,2x+1)$, and $B(2,1,2x+2)$. The 4:1 Mux $F(2,1,2x+1)$ has four inputs
 namely $R_i(2,1,2x+1)$, $R_i(2,1,2x+2)$, $U_i(2,1,2x+2)$, and $J(2,1,x+1)$, and has one output
 $F_o(2,1,2x+1)$. The 4:1 Mux $F(2,1,2x+2)$ has four inputs namely $R_i(2,1,2x+1)$,
 $R_i(2,1,2x+2)$, $U_i(2,1,2x+1)$, and $K(2,1,x+1)$, and has one output $F_o(2,1,2x+2)$.

25 The 4:1 Mux $B(2,1,2x+1)$ has four inputs namely $U_i(2,1,2x+1)$, $U_i(2,1,2x+2)$,
 $R_i(2,1,2x+2)$, and $L(2,1,x+1)$, and has one output $B_o(2,1,2x+1)$. The 4:1 Mux
 $B(2,1,2x+2)$ has four inputs namely $U_i(2,1,2x+1)$, $U_i(2,1,2x+2)$, $R_i(2,1,2x+1)$ and
 $M(2,1,x+1)$, and has one output $B_o(2,1,2x+2)$. In different embodiments the inputs
 $J(2,1,x+1)$, $K(2,1,x+1)$, $L(2,1,x+1)$, and $M(2,1,x+1)$ are connected from any of the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

5 Just the same way the stage (slice 2, ring 1, stage 0), there are also stages (slice 2, ring 1, stage 1), (slice 2, ring 1, stage 2), (slice 2, ring 1, stage 3), ... (slice 2, ring 1, stage "m-1"), (slice 2, ring 1, stage "x") in that order, where the stages from (slice 2, ring 1, stage 1), (slice 2, ring 1, stage 2), ... , (slice 2, ring 1, stage "x-1") are not shown in the diagram 100C.

The stage (slice 2, ring 2, stage 0) consists of 8 inputs namely $Ri(2,2,1)$, $Ri(2,2,2)$, $Ui(2,2,1)$, $Ui(2,2,2)$, $J(2,2,1)$, $K(2,2,1)$, $L(2,2,1)$, and $M(2,2,1)$; and 4 outputs $Bo(2,2,1)$, $Bo(2,2,2)$, $Fo(2,2,1)$, and $Fo(2,2,2)$. The stage (slice 2, ring "2", stage "0") also consists of four 4:1 Muxes namely $F(2,2,1)$, $F(2,2,2)$, $B(2,2,1)$, and $B(2,2,2)$. The 4:1 Mux $F(2,2,1)$ has four inputs namely $Ri(2,2,1)$, $Ri(2,2,2)$, $Ui(2,2,2)$, and $J(2,2,1)$, and has one output $Fo(2,2,1)$. The 4:1 Mux $F(2,2,2)$ has four inputs namely $Ri(2,2,1)$, $Ri(2,2,2)$, $Ui(2,2,1)$, and $K(2,2,1)$, and has one output $Fo(2,2,2)$.

15 The 4:1 Mux $B(2,2,1)$ has four inputs namely $Ui(2,2,1)$, $Ui(2,2,2)$, $Ri(2,2,2)$, and $L(2,2,1)$, and has one output $Bo(2,2,1)$. The 4:1 Mux $B(2,2,2)$ has four inputs namely $Ui(2,2,1)$, $Ui(2,2,2)$, $Ri(2,2,1)$ and $M(2,2,1)$, and has one output $Bo(2,2,2)$. In different embodiments the inputs $J(2,2,1)$, $K(2,2,1)$, $L(2,2,1)$, and $M(2,2,1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

25 The stage (slice 2, ring 2, stage "x") consists of 8 inputs namely $Ri(2,2,2x+1)$, $Ri(2,2,2x+2)$, $Ui(2,2,2x+1)$, $Ui(2,2,2x+2)$, $J(2,2,x+1)$, $K(2,2,x+1)$, $L(2,2,x+1)$, and $M(2,2,x+1)$; and 4 outputs $Bo(2,2,2x+1)$, $Bo(2,2,2x+2)$, $Fo(2,2,2x+1)$, and $Fo(2,2,2x+2)$. The stage (slice 2, ring 2, stage "y") also consists of four 4:1 Muxes namely $F(2,2,2y+1)$, $F(2,2,2y+2)$, $B(2,2,2y+1)$, and $B(2,2,2y+2)$. The 4:1 Mux $F(2,2,2y+1)$ has four inputs namely $Ri(2,2,2y+1)$, $Ri(2,2,2y+2)$, $Ui(2,2,2y+2)$, and $J(2,2,y+1)$, and has one output $Fo(2,2,2y+1)$. The 4:1 Mux $F(2,2,2y+2)$ has four inputs namely $Ri(2,2,2y+1)$, $Ri(2,2,2y+2)$, $Ui(2,2,2y+1)$, and $K(2,2,y+1)$, and has one output $Fo(2,2,2y+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 4:1 Mux B(2,2,2y+1) has four inputs namely $U_i(2,2,2y+1)$, $U_i(2,2,2y+2)$, $R_i(2,2,2y+2)$, and $L(2,2,y+1)$, and has one output $Bo(2,2,2y+1)$. The 4:1 Mux B(2,2,2y+2) has four inputs namely $U_i(2,2,2y+1)$, $U_i(2,2,2y+2)$, $R_i(2,2,2y+1)$ and $M(2,2,y+1)$, and has one output $Bo(2,2,2y+2)$. In different embodiments the inputs
 5 J(2,2,y+1), K(2,2,y+1), L(2,2,y+1), and M(2,2,y+1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 2, ring 2, stage 0), there are also stages (slice 2, ring 2, stage 1), (slice 2, ring 2, stage 2), (slice 2, ring 2, stage 3), ... (slice 2, ring 2, stage
 10 "y-1"), (slice 2, ring 2, stage "y") in that order, where the stages from (slice 2, ring 2, stage 1), (slice 2, ring 2, stage 2), ... , (slice 2, ring 2, stage "y-1") are not shown in the diagram 100C.

As illustrated in diagram 100C5 in FIG. 1C5, the similar internal connections between two successive stages of any ring of any slice of partial multi-stage hierarchical
 15 network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C, in some embodiments are provided for all the slices $c = 1, 2$; for all the rings in each of the slices $d = 1, 2$; and for all the stages namely when $c = 1, d = 1, e = [1, m]$; when $c=1, d=2, e=[1, n]$; when $c=2, d=1, e=[1, x]$; and when $c=2, d=2; e=[1, y]$.

Each stage of any ring of the partial multi-stage hierarchical network
 20 $V_{Comb}(N_1, N_2, d, s)$ 100B consists of $2 * d = 4$ outputs. Even though each stage has four 4:1 muxes, in other embodiments any of these stages can be one of the four by four switch diagrams namely 200A of FIG. 2A, 200B of FIG. 2B, 200C of FIG. 2C, and one of the eight by four switch diagrams namely 200E of FIG. 2E, 200F of FIG. 2F.

In general, any ring of the partial multi-stage hierarchical network
 25 $V_{Comb}(N_1, N_2, d, s)$ illustrated in 100C also may have inputs and outputs connected from computational block from either only from left-hand side as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A; or only from right-hand side; or from both left-hand and right-hand sides as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Applicant now notes a few aspects of the diagram 100C in FIG. 1C an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to one computational block, with each computational block having 16 inlet links and 4 outlet links as follows: (Also these aspects are helpful in more optimization of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ as well as faster scheduling of the connections between outlet links of the computational blocks and the inlet links of the computational blocks.)

1) The partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C is divided into two slices namely slice 1 and slice 2. The outlet links of the computational block namely O1 and O2 are connected to only one slice i.e. slice 1. In other words outlet links O1 and O2 are absolutely not connected to slice 2. Similarly the outlet links of the computational block namely O3 and O4 are connected to only one slice i.e. slice 2. In other words outlet links O3 and O4 are absolutely not connected to slice 1.

2) The second aspect is all the hop wires and multi-drop hop wires originating from slice 1 from any block will be terminating only in the slice 1 of any other block. Similarly all the hop wires and multi-drop hop wires originating from slice 2 from any block will be terminating only in the slice 2 of any other block.

3) The third aspect is the mux whose output is directly connected to each inlet link of the computational block must have at least one input connected from each slice of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C. That is for example since the 4:1 mux B(1,1,1), belonging to slice 1, and having its output Bo(1,1,1) directly connected to inlet link I1 must have at least one of its inputs connecting from an output of a mux of a stage of a ring of slice 2 as well. This property must be satisfied for all the inlet links of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C.

Referring to diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 illustrate the details of the foregoing third aspect of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C. Applicant notes that diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 are all actually part of the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C and these separate diagrams are necessary only to avoid the clutter in the diagram 100C of FIG. 1C.

The connections illustrated between different slices in diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 are the only connections between different slices, in some exemplary embodiments. In general the connections between different slices are given only at the terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block.

Referring to diagram 100C1 in FIG. 1C1 illustrate the connections between the stage (slice 1, ring 1, stage 0) and between the stage (slice 2, ring 1, stage 0). The same connection that is given to the input $U_i(1,1,1)$ is also connected to the input $L(2,1,1)$. The same connection that is given to the input $U_i(1,1,2)$ is also connected to the input $M(2,1,1)$. Similarly the same connection that is given to the input $U_i(2,1,1)$ is also connected to the input $L(1,1,1)$. The same connection that is given to the input $U_i(2,1,2)$ is also connected to the input $M(1,1,1)$.

Therefore inlet link I1 can be essentially connected through the 4:1 mux $B(1,1,1)$ with three of its inputs connecting from slice 1 namely $U_i(1,1,1)$, $U_i(1,1,2)$, $R_i(1,1,2)$ and one input $L(1,1,1)$ connecting from slice 2. The inlet link I2 can be essentially connected through the 4:1 mux $B(1,1,2)$ with three of its inputs connecting from slice 1 namely $U_i(1,1,1)$, $U_i(1,1,2)$, $R_i(1,1,1)$ and one input $M(1,1,1)$ connecting from slice 2. The inlet link I9 can be essentially connected through the 4:1 mux $B(1,2,1)$ with three of its inputs connecting from slice 2 namely $U_i(2,1,1)$, $U_i(2,1,2)$, $R_i(2,1,2)$ and one input $L(2,1,1)$ connecting from slice 1. The inlet link I10 can be essentially connected through the 4:1 mux $B(2,1,2)$ with three of its inputs connecting from slice 2 namely $U_i(2,1,1)$, $U_i(2,1,2)$, $R_i(2,1,1)$ and one input $M(2,1,1)$ connecting from slice 1. Hence all the inlet links I1, I2, I9 and I10 are all independently reachable from both slice 1 and slice2.

Referring to diagram 100C2 in FIG. 1C2 illustrate the connections between the stage (slice 1, ring 2, stage 0) and between the stage (slice 2, ring 2, stage 0). The same connection that is given to the input $U_i(1,2,1)$ is also connected to the input $M(2,2,1)$. The same connection that is given to the input $U_i(1,2,2)$ is also connected to the input

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

L(2,2,1). Similarly the same connection that is given to the input $U_i(2,2,1)$ is also connected to the input $M(1,2,1)$. The same connection that is given to the input $U_i(2,2,2)$ is also connected to the input $L(1,2,1)$.

Therefore inlet link I3 can be essentially connected through the 4:1 mux B(1,2,1) with three of its inputs connecting from slice 1 namely $U_i(1,2,1)$, $U_i(1,2,2)$, $R_i(1,2,2)$ and one input $M(2,2,1)$ connecting from slice 2. The inlet link I4 can be essentially connected through the 4:1 mux B(1,2,2) with three of its inputs connecting from slice 1 namely $U_i(1,2,1)$, $U_i(1,2,2)$, $R_i(1,2,1)$ and one input $M(1,2,1)$ connecting from slice 2. The inlet link I11 can be essentially connected through the 4:1 mux B(2,2,1) with three of its inputs connecting from slice 2 namely $U_i(2,2,1)$, $U_i(2,2,2)$, $R_i(2,2,2)$ and one input $L(2,2,1)$ connecting from slice 1. The inlet link I12 can be essentially connected through the 4:1 mux B(2,2,2) with three of its inputs connecting from slice 2 namely $U_i(2,2,1)$, $U_i(2,2,2)$, $R_i(2,2,1)$ and one input $M(2,2,1)$ connecting from slice 1. Hence all the inlet links I3, I4, I11 and I12 are all independently reachable from both slice 1 and slice2.

Referring to diagram 100C3 in FIG. 1C3 illustrate the connections between the stage (slice 1, ring 1, stage "m") and between the stage (slice 2, ring 2, stage "y"). The same connection that is given to the input $R_i(1,1,2m+1)$ is also connected to the input $J(2,2,y+1)$. The same connection that is given to the input $R_i(1,1,2m+2)$ is also connected to the input $K(2,2,y+1)$. Similarly the same connection that is given to the input $R_i(2,2,2y+1)$ is also connected to the input $J(1,1,m+1)$. The same connection that is given to the input $R_i(2,2,2y+2)$ is also connected to the input $K(1,1,m+1)$.

Therefore inlet link I5 can be essentially connected through the 4:1 mux F(1,1,2m+1) with three of its inputs connecting from slice 1 namely $R_i(1,1,2m+1)$, $R_i(1,1,2m+2)$, $U_i(1,1,2m+2)$ and one input $J(1,1,m+1)$ connecting from slice 2. The inlet link I6 can be essentially connected through the 4:1 mux F(1,1,2m+2) with three of its inputs connecting from slice 1 namely $R_i(1,1,2m+1)$, $R_i(1,1,2m+2)$, $U_i(1,1,2m+1)$ and one input $K(1,1,m+1)$ connecting from slice 2. The inlet link I15 can be essentially connected through the 4:1 mux F(2,2,2y+1) with three of its inputs connecting from slice 2 namely $R_i(2,2,2y+1)$, $R_i(2,2,2y+2)$, $U_i(2,2,2y+2)$ and one input $J(2,2,y+1)$ connecting from slice 1. The inlet link I16 can be essentially connected through the 4:1 mux F(2,2,2y+2) with three of its inputs connecting from slice 2 namely $R_i(2,2,2y+1)$,

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$R_i(2,2,2y+2)$, $U_i(2,2,2y+1)$ and one input $K(2,2,y+1)$ connecting from slice 1. Hence all the inlet links I5, I6, I15 and I16 are all independently reachable from both slice 1 and slice2.

Referring to diagram 100C4 in FIG. 1C4 illustrate the connections between the stage (slice 1, ring 2, stage "n") and between the stage (slice 2, ring 1, stage "x"). The same connection that is given to the input $R_i(1,2,2n+1)$ is also connected to the input $K(2,1,x+1)$. The same connection that is given to the input $R_i(1,2,2n+2)$ is also connected to the input $J(2,1,x+1)$. Similarly the same connection that is given to the input $R_i(2,1,2x+1)$ is also connected to the input $K(1,2,n+1)$. The same connection that is given to the input $R_i(2,1,2x+2)$ is also connected to the input $J(1,2,n+1)$.

Therefore inlet link I7 can be essentially connected through the 4:1 mux $F(1,2,2n+1)$ with three of its inputs connecting from slice 1 namely $R_i(1,2,2n+1)$, $R_i(1,2,2n+2)$, $U_i(1,2,2n+2)$ and one input $J(1,2,n+1)$ connecting from slice 2. The inlet link I8 can be essentially connected through the 4:1 mux $F(1,2,2n+2)$ with three of its inputs connecting from slice 1 namely $R_i(1,2,2n+1)$, $R_i(1,2,2n+2)$, $U_i(1,2,2n+1)$ and one input $K(1,2,n+1)$ connecting from slice 2. The inlet link I13 can be essentially connected through the 4:1 mux $F(2,1,2x+1)$ with three of its inputs connecting from slice 2 namely $R_i(2,1,2x+1)$, $R_i(2,1,2x+2)$, $U_i(2,1,2x+2)$ and one input $J(2,1,x+1)$ connecting from slice 1. The inlet link I14 can be essentially connected through the 4:1 mux $F(2,1,2x+2)$ with three of its inputs connecting from slice 2 namely $R_i(2,1,2x+1)$, $R_i(2,1,2x+2)$, $U_i(2,1,2x+1)$ and one input $K(2,1,x+1)$ connecting from slice 1. Hence all the inlet links I7, I8, I13 and I14 are all independently reachable from both slice 1 and slice2.

The connections illustrated between different slices, in several embodiments, in diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 are the only connections between different slices. And also the terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block have three inputs coming from one slice and one input coming from another slice. In other embodiments it is also possible so that the terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block have two inputs coming from one slice and two inputs coming from another slice.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Also in general the number of slices in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C may be more than or equal to two. In such a case terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block will have at least one input coming from each slice. And the outlet links of the computational block will be divided and connected to each slice; however each outlet link of the computational block will be connected to only one slice. Also in general the hop wires and multi-drop hop wires are connected to only between the corresponding slices of different blocks, in some embodiments some of the hop wires and multi-drop hop wires may be connected between different slices of different blocks even if it is done partially.

FIG. 2A illustrates a stage (ring "k", stage "m") 200A consists of 4 inputs namely $F_i(k, 2m+1)$, $F_i(k, 2m+2)$, $U_i(k, 2m+1)$, and $U_i(k, 2m+2)$; and 4 outputs $B_o(k, 2m+1)$, $B_o(k, 2m+2)$, $F_o(k, 2m+1)$, and $F_o(k, 2m+2)$. The stage (ring "k", stage "m") also consists of six 2:1 Muxes namely $F(k, 2m+1)$, $F(k, 2m+2)$ (comprising in combination a forward switch), $U(k, 2m+1)$, $U(k, 2m+2)$ (comprising in combination a U-turn switch), $B(k, 2m+1)$, and $B(k, 2m+2)$ (comprising in combination a backward switch). The 2:1 Mux $F(k, 2m+1)$ has two inputs namely $F_i(k, 2m+1)$ and $F_i(k, 2m+2)$ and has one output $F_o(k, 2m+1)$. The 2:1 Mux $F(k, 2m+2)$ has two inputs namely $F_i(k, 2m+1)$ and $F_i(k, 2m+2)$ and has one output $F_o(k, 2m+2)$.

The 2:1 Mux $U(k, 2m+1)$ has two inputs namely $U_i(k, 2m+1)$ and $F_o(k, 2m+1)$ and has one output $U_o(k, 2m+1)$. The 2:1 Mux $U(k, 2m+2)$ has two inputs namely $U_i(k, 2m+2)$ and $F_o(k, 2m+2)$ and has one output $U_o(k, 2m+2)$. The 2:1 Mux $B(k, 2m+1)$ has two inputs namely $U_o(k, 2m+1)$ and $U_o(k, 2m+2)$ and has one output $B_o(k, 2m+1)$. The 2:1 Mux $B(k, 2m+2)$ has two inputs namely $U_o(k, 2m+1)$ and $U_o(k, 2m+2)$ and has one output $B_o(k, 2m+2)$.

FIG. 2B illustrates a stage (ring "k", stage "m") 200B consists of 4 inputs namely $R_i(k, 2m+1)$, $R_i(k, 2m+2)$, $U_i(k, 2m+1)$, and $U_i(k, 2m+2)$; and 4 outputs $B_o(k, 2m+1)$, $B_o(k, 2m+2)$, $F_o(k, 2m+1)$, and $F_o(k, 2m+2)$. The stage (ring "k", stage "m") also consists of eight 2:1 Muxes namely $R(k, 2m+1)$, $R(k, 2m+2)$ (comprising in combination a Reverse U-turn switch), $F(k, 2m+1)$, $F(k, 2m+2)$ (comprising in combination a forward switch), $U(k, 2m+1)$, $U(k, 2m+2)$ (comprising in combination a U-turn switch), $B(k, 2m+1)$, and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

B(k,2m+2) (comprising in combination a backward switch). The 2:1 Mux R(k,2m+1) has two inputs namely Ri(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and
 5 Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs
 10 namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 2C illustrates a stage (ring “k”, stage “m”) 200C consists of 4 inputs namely Fi(k,2m+1), Fi(k,2m+2), $\underline{U}i(k,2m+1)$, and $\underline{U}i(k,2m+2)$; and 4 outputs
 15 $\underline{U}o(k,2m+1)$, $\underline{U}o(k,2m+2)$, Fo(k,2m+1), and Fo(k,2m+2). The stage (ring “k”, stage “m”) also consists of four 2:1 Muxes namely F(k,2m+1), F(k,2m+2) (comprising in combination a forward switch), $\underline{U}B(k,2m+1)$, and $\underline{U}B(k,2m+2)$ (comprising in combination a U-turn switch). The 2:1 Mux F(k,2m+1) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1
 20 Mux F(k,2m+2) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux $\underline{U}B(k,2m+1)$ has two inputs namely $\underline{U}Bi(k,2m+1)$ and $\underline{U}Bi(k,2m+2)$ and has one output $\underline{U}Bo(k,2m+1)$. The 2:1 Mux $\underline{U}B(k,2m+2)$ has two inputs namely $\underline{U}Bi(k,2m+1)$ and $\underline{U}Bi(k,2m+2)$ and has one output $\underline{U}Bo(k,2m+2)$.

However the stage “ $\underline{m+1m}$ ” of ring “k” with “ $\underline{m+1m}$ ” stages of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 2 inputs and 2 outputs as shown in diagram 200D in FIG. 2D. FIG. 2D illustrates a stage (ring “k”, stage “m”) 200D consists of 2 inputs namely Fi(k,2m+1) and Fi(k,2m+2); and 2 outputs
 25 Fo(k,2m+1) and Fo(k,2m+2). The stage (ring “k”, stage “m”) also consists of two 2:1 Muxes namely F(k,2m+1), F(k,2m+2) (comprising in combination a forward switch). The
 30

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

2:1 Mux $F(k,2m+1)$ has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+2)$. A stage with 2 inputs and 2 outputs is, in one embodiment, the “last stage” or “root stage” of ring.

5 The stage “m” of ring “k” with “m” stages of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 8 inputs and 4 outputs as shown in diagram 200E in FIG. 2E. FIG. 2E illustrates a stage (ring “k”, stage “m”) 200E consists of 8 inputs namely $F_{Ri}(k,2m+1)$, $F_{Ri}(k,2m+2)$, $F_{Ui}(k,2m+1)$, $F_{Ui}(k,2m+2)$, J, K, L, and M; and 4 outputs $F_{Ro}(k,2m+1)$, $F_{Ro}(k,2m+2)$, $F_{Fo}(k,2m+1)$, and $F_{Fo}(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of eight 2:1 Muxes namely $F_R(k,2m+1)$, $F_R(k,2m+2)$ (comprising in combination a forward switch), $F_F(k,2m+1)$, $F_F(k,2m+2)$ (comprising in combination a Reverse U-turn switch), $F_U(k,2m+1)$, $F_U(k,2m+2)$ (comprising in combination a backward switch), $F_B(k,2m+1)$, and $F_B(k,2m+2)$ (comprising in combination a U-turn switch). The 2:1 Mux $R(k,2m+1)$ has two inputs namely $F_{Ri}(k,2m+1)$ and J, and has one output $F_{Ro}(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $F_{Ri}(k,2m+2)$ and K, and has one output $F_{Ro}(k,2m+2)$. The 2:1 Mux $F_F(k,2m+1)$ has two inputs namely $F_{Fo}(k,2m+1)$ and $F_{Uo}(k,2m+2)$, and has one output $F_{Fo}(k,2m+1)$. The 2:1 Mux $F_F(k,2m+2)$ has two inputs namely $F_{Fo}(k,2m+2)$ and $F_{Uo}(k,2m+1)$, and has one output $F_{Fo}(k,2m+2)$.

15 The 2:1 Mux $F_U(k,2m+1)$ has two inputs namely $F_{Ui}(k,2m+1)$ and L, and has one output $F_{Uo}(k,2m+1)$. The 2:1 Mux $F_U(k,2m+2)$ has two inputs namely $F_{Ui}(k,2m+2)$ and M, and has one output $F_{Uo}(k,2m+2)$. The 2:1 Mux $F_B(k,2m+1)$ has two inputs namely $F_{Bo}(k,2m+1)$ and $F_{Ro}(k,2m+2)$, and has one output $F_{Bo}(k,2m+1)$. The 2:1 Mux $F_B(k,2m+2)$ has two inputs namely $F_{Bo}(k,2m+2)$ and $F_{Ro}(k,2m+1)$, and has one output $F_{Bo}(k,2m+2)$. In different embodiments the inputs J, K, L, and M are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

25 The diagram 200E of FIG 2E eliminates the 180-degree turn paths from the internal connection $F_i(k,2m+1)$ to the internal connection $F_o(k,2m+1)$. Similarly the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

5 diagram 200E of FIG 2E eliminates the 180-degree turn paths from the connection $F_i(k,2m+2)$ to the connection $U_o(k,2m+2)$. The diagram 200E of FIG 2E eliminates the 180-degree turn paths from the internal connection $B_i(k,2m+1)$ to the internal connection $R_o(k,2m+1)$. Similarly the diagram 200E of FIG 2E eliminates the 180-degree turn paths from the connection $B_i(k,2m+2)$ to the connection $R_o(k,2m+2)$. Hence diagram 200E of FIG. 2E comprises a forward switch, a backward switch, U-turn switch and reverse U-turn switch without 180-degree U-turn paths.

10 In contrast to diagram 200E of FIG. 2E, the diagram 200A of FIG. 2A, diagram 200B of FIG. 2B, and diagram 200C of FIG. 2C provide 180-degree U-turn paths. Two exemplary 180-degree U-turn paths in diagram 200A of FIG. 2A are shown (by two types of dotted lines) in the attached replacement diagram of FIG. 2A. One of the 180-degree turn path shown in the replacement diagram of FIG. 2A starts at the internal connection $F_i(k,2m+1)$ through the Mux $F(k,2m+1)$ to $F_o(k,2m+1)$ through the Mux $U(k,2m+1)$ to $U_o(k,2m+1)$ through the Mux $B(k,2m+1)$ to the internal connection $B_o(k,2m+1)$. The second of the 180-degree turn path shown in the replacement diagram of FIG. 2A starts at the hop wire $F_i(k,2m+2)$ through the Mux $F(k,2m+2)$ to $F_o(k,2m+2)$ through the Mux $U(k,2m+2)$ to $U_o(k,2m+2)$ through the Mux $B(k,2m+2)$ to the hop wire $B_o(k,2m+2)$.

20 The stage "m" of ring "k" with "m" stages of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 8 inputs and 4 outputs as shown in diagram 200F in FIG. 2F. FIG. 2F illustrates a stage (ring "k", stage "m") 200F consists of 8 inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, J, K, L, and M; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring "k", stage "m") also consists of four 4:1 Muxes namely $F(k,2m+1)$, $F(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The 4:1 Mux $F(k,2m+1)$ has four inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $U_i(k,2m+2)$, and J, and has one output $F_o(k,2m+1)$. The 4:1 Mux $F(k,2m+2)$ has four inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $U_i(k,2m+1)$, and K, and has one output $F_o(k,2m+2)$.

30 The 4:1 Mux $B(k,2m+1)$ has four inputs namely $U_i(k,2m+1)$, $U_i(k,2m+2)$, $R_i(k,2m+2)$, and L, and has one output $B_o(k,2m+1)$. The 4:1 Mux $B(k,2m+2)$ has four inputs namely $U_i(k,2m+1)$, $U_i(k,2m+2)$, $R_i(k,2m+1)$ and M, and has one output $B_o(k,2m+2)$. In different embodiments the inputs J, K, L, and M are connected from any

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

5 The diagram 200F of FIG 2F eliminates the 180-degree turn paths from the internal connection Ri(k,2m+1) to the internal connection Bo(k,2m+1). Similarly the diagram 200F of FIG 2F eliminates the 180-degree turn paths from the connection Ri(k,2m+2) to the connection Bo(k,2m+2). The diagram 200F of FIG 2F eliminates the 180-degree turn paths from the internal connection Ui(k,2m+1) to the internal connection Fo(k,2m+1). Similarly the diagram 200F of FIG 2F eliminates the 180-degree turn paths from the connection Ui(k,2m+2) to the connection Fo(k,2m+2). Hence diagram 200F of
 10 FIG. 2F comprises an integrated switch of a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180-degree U-turn paths.

The number of stages in a ring of any block may not be equal to the number of stages in any other ring of the same of block or any ring of any other block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. For example the number of stages in ring
 15 1 of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A or of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B or of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C is denoted by “m” and the number of stages in ring 2 of the partial multi-stage hierarchical network is denoted by “n”, and so “m” may or may not be equal to “n”. Similarly the number of stages in ring 2 corresponding to
 20 block (3,3) of 2D-grid 800 may not be equal to the number of stages in ring 2 corresponding to block (6,9) of 2D-grid 800. Similarly in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C the number of stages in (slice 1, ring 2) corresponding to block (3,3) of 2D-grid 800 may not be equal to the number of stages in (slice 1, ring 2) corresponding to block (6,9) of 2D-grid 800.

25 Even though the number of inlet links to the computational block is four and the number of outlet links to the computational block is two in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A, the number of inlet links to the computational block is eight and the number of outlet links to the computational block is four in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B, and the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

number of inlet links to the computational block is sixteen and the number of outlet links to the computational block is four in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C, in other embodiments the number of inlet links to the computational block may be any arbitrary number and the number of outlet links to the computational block may also be another arbitrary number. However the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of inlet links to the computational block divided by $d = 2$ if the inputs and outputs are connected either only from left-hand side or only from right-hand side, if the number of inlet links to the computational block is greater than or equal to the number of outlet links to the computational block. In such a case one or more of the outlet links to the computational block are connected to more than one inlet links of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to a block. Similarly the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of inlet links to the computational block divided by $2 * d = 4$ if the inputs and outputs are connected from both left-hand side and from right-hand side, if the number of inlet links to the computational block is greater than or equal to the number of outlet links to the computational block.

Otherwise the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of outlet links to the computational block divided by $d = 2$ if the inputs and outputs are connected either only from left-hand side or only from right-hand side, if the number of outlet links to the computational block is greater than the number of inlet links to the computational block. In such a case one or more of the outlet links of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to a block are connected to more than one inlet link of the computational block. Similarly the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of outlet links to the computational block divided by $2 * d = 4$ if the inputs and outputs are connected from

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

both left-hand side and from right-hand side, if the number of outlet links to the computational block is greater than or equal to the number of inlet links to the computational block.

In another embodiment, the number of inlet links to the computational block
 5 corresponding to a block of 2D-grid of blocks may or may not be equal to the number of
 inlet links to the computational block corresponding to another block. Similarly the
 number of outlet links to the computational block corresponding to a block of 2D-grid of
 blocks may or may not be equal to the number of outlet links to the computational block
 corresponding to another block. Hence the total number of rings of the partial multi-stage
 10 hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to a block of 2D-grid of blocks
 may or may not be equal to the partial multi-stage hierarchical network
 $V_{Comb}(N_1, N_2, d, s)$ corresponding to another block. For example the total number of rings
 corresponding to block (4,5) of 2D-grid 800 may be two and the total number of rings in
 block (5,4) of 2D-grid 800 may be three.

15 A multi-stage hierarchical network can be represented with the notation
 $V_{Comb}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of the complete
 multi-stage hierarchical network and N_2 represents the total number of outlet links of the
 complete multi-stage hierarchical network, d represents the number of inlet links of any
 ring in any block of the complete multi-stage hierarchical network either from only left-
 20 hand side or only right-hand side, or equivalently the number of outlet links of any ring in
 any block of the complete multi-stage hierarchical network either from only left-hand
 side or only right-hand side, and when the inputs and outputs are connected from left-
 hand side, s is the ratio of number of outgoing links from each stage 0 of any ring in any
 block to the number of inlet links of any ring in any block of the complete multi-stage
 25 hierarchical network (for example the complete multi-stage hierarchical network
 corresponding to $V_{Comb}(N_1, N_2, d, s)$ 100A in FIG. 1A, $N_1 = 200$, $N_2 = 400$, $d = 2$,
 $s = 1$). Also a multi-stage hierarchical network where $N_1 = N_2 = N$ is represented as
 $V_{Comb}(N, d, s)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The diagram 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, and 300E of FIG. 3E are different embodiments of all the connections between two arbitrary successive stages in two different rings of the same block or two different rings of different blocks of 2D-grid 800. Referring to diagram 300A in FIG. 3A illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 4 inputs namely $R_i(x, 2p+1)$, $R_i(x, 2p+2)$, $U_i(x, 2p+1)$, and $U_i(x, 2p+2)$; and 4 outputs $B_o(x, 2p+1)$, $B_o(x, 2p+2)$, $F_o(x, 2p+1)$, and $F_o(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely $R(x, 2p+1)$, $R(x, 2p+2)$, $F(x, 2p+1)$, $F(x, 2p+2)$, $U(x, 2p+1)$, $U(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 2:1 Mux $R(x, 2p+1)$ has two inputs namely $R_i(x, 2p+1)$ and $B_o(x, 2p+1)$ and has one output $R_o(x, 2p+1)$. The 2:1 Mux $R(x, 2p+2)$ has two inputs namely $R_i(x, 2p+2)$ and $B_o(x, 2p+2)$ and has one output $R_o(x, 2p+2)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $R_o(x, 2p+1)$ and $R_o(x, 2p+2)$ and has one output $F_o(x, 2p+1)$. The 2:1 Mux $F(x, 2p+2)$ has two inputs namely $R_o(x, 2p+1)$ and $R_o(x, 2p+2)$ and has one output $F_o(x, 2p+2)$.

The 2:1 Mux $U(x, 2p+1)$ has two inputs namely $U_i(x, 2p+1)$ and $F_o(x, 2p+1)$ and has one output $U_o(x, 2p+1)$. The 2:1 Mux $U(x, 2p+2)$ has two inputs namely $U_i(x, 2p+2)$ and $F_o(x, 2p+2)$ and has one output $U_o(x, 2p+2)$. The 2:1 Mux $B(x, 2p+1)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $B_o(x, 2p+1)$. The 2:1 Mux $B(x, 2p+2)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $B_o(x, 2p+2)$.

The stage (ring “x”, stage “p+1”) consists of 4 inputs namely $R_i(x, 2p+3)$, $R_i(x, 2p+4)$, $U_i(x, 2p+3)$, and $U_i(x, 2p+4)$; and 4 outputs $B_o(x, 2p+3)$, $B_o(x, 2p+4)$, $F_o(x, 2p+3)$, and $F_o(x, 2p+4)$. The stage (ring “x”, stage “p+1”) also consists of eight 2:1 Muxes namely $R(x, 2p+3)$, $R(x, 2p+4)$, $F(x, 2p+3)$, $F(x, 2p+4)$, $U(x, 2p+3)$, $U(x, 2p+4)$, $B(x, 2p+3)$, and $B(x, 2p+4)$. The 2:1 Mux $R(x, 2p+3)$ has two inputs namely $R_i(x, 2p+3)$ and $B_o(x, 2p+3)$ and has one output $R_o(x, 2p+3)$. The 2:1 Mux $R(x, 2p+4)$ has two inputs namely $R_i(x, 2p+4)$ and $B_o(x, 2p+4)$ and has one output $R_o(x, 2p+4)$. The 2:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$F(x, 2p+3)$ has two inputs namely $Ro(x, 2p+3)$ and $Ro(x, 2p+4)$ and has one output $Fo(x, 2p+3)$. The 2:1 Mux $F(x, 2p+4)$ has two inputs namely $Ro(x, 2p+3)$ and $Ro(x, 2p+4)$ and has one output $Fo(x, 2p+4)$.

The 2:1 Mux $U(x, 2p+3)$ has two inputs namely $Ui(x, 2p+3)$ and $Fo(x, 2p+3)$ and
 5 has one output $Uo(x, 2p+3)$. The 2:1 Mux $U(x, 2p+4)$ has two inputs namely $Ui(x, 2p+4)$
 and $Fo(x, 2p+4)$ and has one output $Uo(x, 2p+4)$. The 2:1 Mux $B(x, 2p+3)$ has two inputs
 namely $Uo(x, 2p+3)$ and $Uo(x, 2p+4)$ and has one output $Bo(x, 2p+3)$. The 2:1 Mux
 $B(x, 2p+4)$ has two inputs namely $Uo(x, 2p+3)$ and $Uo(x, 2p+4)$ and has one output
 $Bo(x, 2p+4)$.

10 The output $Fo(x, 2p+1)$ of the stage (ring "x", stage "p") is connected to the input
 $Ri(x, 2p+3)$ of the stage (ring "x", stage "p+1"). And the output $Bo(x, 2p+3)$ of the stage
 (ring "x", stage "p+1") is connected to the input $Ui(x, 2p+1)$ of the stage (ring "x", stage
 "p").

The stage (ring "y", stage "q") consists of 4 inputs namely $Ri(y, 2q+1)$,
 15 $Ri(y, 2q+2)$, $Ui(y, 2q+1)$, and $Ui(y, 2q+2)$; and 4 outputs $Bo(y, 2q+1)$, $Bo(y, 2q+2)$,
 $Fo(y, 2q+1)$, and $Fo(y, 2q+2)$. The stage (ring "y", stage "q") also consists of eight 2:1
 Muxes namely $R(y, 2q+1)$, $R(y, 2q+2)$, $F(y, 2q+1)$, $F(y, 2q+2)$, $U(y, 2q+1)$, $U(y, 2q+2)$,
 $B(y, 2q+1)$, and $B(y, 2q+2)$. The 2:1 Mux $R(y, 2q+1)$ has two inputs namely $Ri(y, 2q+1)$
 and $Bo(y, 2q+1)$ and has one output $Ro(y, 2q+1)$. The 2:1 Mux $R(y, 2q+2)$ has two inputs
 20 namely $Ri(y, 2q+2)$ and $Bo(y, 2q+2)$ and has one output $Ro(y, 2q+2)$. The 2:1 Mux
 $F(y, 2q+1)$ has two inputs namely $Ro(y, 2q+1)$ and $Ro(y, 2q+2)$ and has one output
 $Fo(y, 2q+1)$. The 2:1 Mux $F(y, 2q+2)$ has two inputs namely $Ro(y, 2q+1)$ and $Ro(y, 2q+2)$
 and has one output $Fo(y, 2q+2)$.

The 2:1 Mux $U(y, 2q+1)$ has two inputs namely $Ui(y, 2q+1)$ and $Fo(y, 2q+1)$ and
 25 has one output $Uo(y, 2q+1)$. The 2:1 Mux $U(y, 2q+2)$ has two inputs namely $Ui(y, 2q+2)$
 and $Fo(y, 2q+2)$ and has one output $Uo(y, 2q+2)$. The 2:1 Mux $B(y, 2q+1)$ has two inputs
 namely $Uo(y, 2q+1)$ and $Uo(y, 2q+2)$ and has one output $Bo(y, 2q+1)$. The 2:1 Mux
 $B(y, 2q+2)$ has two inputs namely $Uo(y, 2q+1)$ and $Uo(y, 2q+2)$ and has one output
 $Bo(y, 2q+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The stage (ring “y”, stage “q+1”) consists of 4 inputs namely $R_i(y,2q+3)$, $R_i(y,2q+4)$, $U_i(y,2q+3)$, and $U_i(y,2q+4)$; and 4 outputs $B_o(y,2q+3)$, $B_o(y,2q+4)$, $F_o(y,2q+3)$, and $F_o(y,2q+4)$. The stage (ring “y”, stage “q+1”) also consists of eight 2:1 Muxes namely $R(y,2q+3)$, $R(y,2q+4)$, $F(y,2q+3)$, $F(y,2q+4)$, $U(y,2q+3)$, $U(y,2q+4)$, $B(y,2q+3)$, and $B(y,2q+4)$. The 2:1 Mux $R(y,2q+3)$ has two inputs namely $R_i(y,2q+3)$ and $B_o(y,2q+3)$ and has one output $R_o(y,2q+3)$. The 2:1 Mux $R(y,2q+4)$ has two inputs namely $R_i(y,2q+4)$ and $B_o(y,2q+4)$ and has one output $R_o(y,2q+4)$. The 2:1 Mux $F(y,2q+3)$ has two inputs namely $R_o(y,2q+3)$ and $R_o(y,2q+4)$ and has one output $F_o(y,2q+3)$. The 2:1 Mux $F(y,2q+4)$ has two inputs namely $R_o(y,2q+3)$ and $R_o(y,2q+4)$ and has one output $F_o(y,2q+4)$.

The 2:1 Mux $U(y,2q+3)$ has two inputs namely $U_i(y,2q+3)$ and $F_o(y,2q+3)$ and has one output $U_o(y,2q+3)$. The 2:1 Mux $U(y,2q+4)$ has two inputs namely $U_i(y,2q+4)$ and $F_o(y,2q+4)$ and has one output $U_o(y,2q+4)$. The 2:1 Mux $B(y,2q+3)$ has two inputs namely $U_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output $B_o(y,2q+3)$. The 2:1 Mux $B(y,2q+4)$ has two inputs namely $U_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output $B_o(y,2q+4)$.

The output $F_o(y,2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $R_i(y,2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $B_o(y,2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $U_i(y,2q+1)$ of the stage (ring “y”, stage “q”).

The output $F_o(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input $R_i(y,2q+4)$ of the stage (ring “y”, stage “q+1”). The output $B_o(x,2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire Hop(1,2) to the input $U_i(y,2q+2)$ of the stage (ring “y”, stage “q”).

The output $F_o(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire Hop(2,1) to the input $R_i(x,2p+4)$ of the stage (ring “x”, stage “p+1”). The output $B_o(y,2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to the input $U_i(x,2p+2)$ of the stage (ring “x”, stage “p”).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Ring “x” and ring “y” may or may not belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. If ring “x” and ring “y” belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are hereinafter called “internal hop wires”. For example if “x = 2” and “y = 3” and both the ring 2 and ring 3 belong to the same block (9,9) of 2D-grid 800, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are “internal hop wires”.

If ring “x” and ring “y” belong to the different blocks of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are hereinafter called “external hop wires”. The external hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) may be horizontal wires or vertical wires. The length of the external hop wires is manhattan distance between the corresponding blocks, hereinafter “hop length”. For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (1,6) of 2D-grid 800 then the external hop wires are hereinafter called “horizontal external hop wires”. And the hop length of the horizontal hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) is given by $6 - 1 = 5$. Similarly if ring “x” and ring “y” belong to two blocks in the same horizontal row of 2D-grid 800, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are horizontal external hop wires.

For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (9,1) of 2D-grid 800 then the external hop wires are hereinafter called “vertical external hop wires”. And the hop length of the vertical hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) is given by $9 - 1 = 8$. Similarly if ring “x” and ring “y” belong to two blocks in the same vertical column of 2D-grid 800, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are vertical external hop wires. External hop wires are typically horizontal or vertical according to the current invention.

Referring to diagram 300B in FIG. 3B illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The stage (ring “x”, stage “p”) consists of 8 inputs namely $\mathbb{F}Ri(x,2p+1)$, $\mathbb{F}Ri(x,2p+2)$, $\mathbb{B}Ui(x,2p+1)$, $\mathbb{B}Ui(x,2p+2)$, J1, K1, L1, and M1; and 4 outputs $\mathbb{U}Bo(x,2p+1)$, $\mathbb{U}Bo(x,2p+2)$, $\mathbb{R}Fo(x,2p+1)$, and $\mathbb{R}Fo(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely $\mathbb{F}R(x,2p+1)$, $\mathbb{F}R(x,2p+2)$, $\mathbb{R}F(x,2p+1)$, $\mathbb{R}F(x,2p+2)$, $\mathbb{B}U(x,2p+1)$, $\mathbb{B}U(x,2p+2)$, $\mathbb{U}B(x,2p+1)$, and $\mathbb{U}B(x,2p+2)$. The 2:1 Mux $\mathbb{F}R(x,2p+1)$ has two inputs namely $\mathbb{F}Ri(x,2p+1)$ and J1, and has one output $\mathbb{F}Ro(x,2p+1)$. The 2:1 Mux $\mathbb{F}R(x,2p+2)$ has two inputs namely $\mathbb{F}Ri(x,2p+2)$ and K1, and has one output $\mathbb{F}Ro(x,2p+2)$. The 2:1 Mux $\mathbb{R}F(x,2p+1)$ has two inputs namely $\mathbb{F}Ro(x,2p+1)$ and $\mathbb{B}Uo(x,2p+2)$, and has one output $\mathbb{R}Fo(x,2p+1)$. The 2:1 Mux $\mathbb{R}F(x,2p+2)$ has two inputs namely $\mathbb{F}Ro(x,2p+2)$ and $\mathbb{B}Uo(x,2p+1)$, and has one output $\mathbb{R}Fo(x,2p+2)$.

The 2:1 Mux $\mathbb{B}U(x,2p+1)$ has two inputs namely $\mathbb{B}Ui(x,2p+1)$ and L1, and has one output $\mathbb{B}Uo(x,2p+1)$. The 2:1 Mux $\mathbb{B}U(x,2p+2)$ has two inputs namely $\mathbb{B}Ui(x,2p+2)$ and M1, and has one output $\mathbb{B}Uo(x,2p+2)$. The 2:1 Mux $\mathbb{U}B(x,2p+1)$ has two inputs namely $\mathbb{B}Uo(x,2p+1)$ and $\mathbb{F}Ro(x,2p+2)$, and has one output $\mathbb{U}Bo(x,2p+1)$. The 2:1 Mux $\mathbb{U}B(x,2p+2)$ has two inputs namely $\mathbb{B}Uo(x,2p+2)$ and $\mathbb{F}Ro(x,2p+1)$, and has one output $\mathbb{U}Bo(x,2p+2)$.

The stage (ring “x”, stage “p+1”) consists of 8 inputs namely $\mathbb{F}Ri(x,2p+3)$, $\mathbb{F}Ri(x,2p+4)$, $\mathbb{B}Ui(x,2p+3)$, $\mathbb{B}Ui(x,2p+4)$, J2, K2, L2, and M2; and 4 outputs $\mathbb{U}Bo(x,2p+3)$, $\mathbb{U}Bo(x,2p+4)$, $\mathbb{R}Fo(x,2p+3)$, and $\mathbb{R}Fo(x,2p+4)$. The stage (ring “x”, stage “p+1”) also consists of eight 2:1 Muxes namely $\mathbb{F}R(x,2p+3)$, $\mathbb{F}R(x,2p+4)$, $\mathbb{R}F(x,2p+3)$, $\mathbb{R}F(x,2p+4)$, $\mathbb{B}U(x,2p+3)$, $\mathbb{B}U(x,2p+4)$, $\mathbb{U}B(x,2p+3)$, and $\mathbb{U}B(x,2p+4)$. The 2:1 Mux $\mathbb{F}R(x,2p+3)$ has two inputs namely $\mathbb{F}Ri(x,2p+3)$ and J2, and has one output $\mathbb{F}Ro(x,2p+3)$. The 2:1 Mux $\mathbb{F}R(x,2p+4)$ has two inputs namely $\mathbb{F}Ri(x,2p+4)$ and K2, and has one output $\mathbb{F}Ro(x,2p+4)$. The 2:1 Mux $\mathbb{R}F(x,2p+3)$ has two inputs namely $\mathbb{F}Ro(x,2p+3)$ and $\mathbb{B}Uo(x,2p+4)$, and has one output $\mathbb{R}Fo(x,2p+3)$. The 2:1 Mux $\mathbb{R}F(x,2p+4)$ has two inputs namely $\mathbb{F}Ro(x,2p+4)$ and $\mathbb{B}Uo(x,2p+3)$, and has one output $\mathbb{R}Fo(x,2p+4)$.

The 2:1 Mux $\mathbb{B}U(x,2p+3)$ has two inputs namely $\mathbb{B}Ui(x,2p+3)$ and L2, and has one output $\mathbb{B}Uo(x,2p+3)$. The 2:1 Mux $\mathbb{B}U(x,2p+4)$ has two inputs namely $\mathbb{B}Ui(x,2p+4)$ and M2, and has one output $\mathbb{B}Uo(x,2p+4)$. The 2:1 Mux $\mathbb{U}B(x,2p+3)$

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

has two inputs namely $\text{BUo}(x,2p+3)$ and $\text{FRo}(x,2p+4)$, and has one output $\text{UBo}(x,2p+3)$. The 2:1 Mux $\text{UB}(x,2p+4)$ has two inputs namely $\text{BUo}(x,2p+4)$ and $\text{FRo}(x,2p+3)$, and has one output $\text{UBo}(x,2p+4)$.

5 The output $\text{Rfo}(x,2p+1)$ of the stage (ring "x", stage "p") is connected to the input $\text{Ffi}(x,2p+3)$ of the stage (ring "x", stage "p+1"). And the output $\text{UBo}(x,2p+3)$ of the stage (ring "x", stage "p+1") is connected to the input $\text{Bfi}(x,2p+1)$ of the stage (ring "x", stage "p").

10 The stage (ring "y", stage "q") consists of 8 inputs namely $\text{Ffi}(y,2q+1)$, $\text{Ffi}(y,2q+2)$, $\text{Bfi}(y,2q+1)$, $\text{Bfi}(y,2q+2)$, J3, K3, L3, and M3; and 4 outputs $\text{UBo}(y,2q+1)$, $\text{UBo}(y,2q+2)$, $\text{Rfo}(y,2q+1)$, and $\text{Rfo}(y,2q+2)$. The stage (ring "y", stage "q") also consists of eight 2:1 Muxes namely $\text{FR}(y,2q+1)$, $\text{FR}(y,2q+2)$, $\text{RF}(y,2q+1)$, $\text{RF}(y,2q+2)$, $\text{BU}(y,2q+1)$, $\text{BU}(y,2q+2)$, $\text{UB}(y,2q+1)$, and $\text{UB}(y,2q+2)$. The 2:1 Mux $\text{FR}(y,2q+1)$ has two inputs namely $\text{Ffi}(y,2q+1)$ and J3, and has one output $\text{Rfo}(y,2q+1)$. The 2:1 Mux $\text{FR}(y,2q+2)$ has two inputs namely $\text{Ffi}(y,2q+2)$ and K3, and has one output $\text{Rfo}(y,2q+2)$. The 2:1 Mux $\text{RF}(y,2q+1)$ has two inputs namely $\text{FRo}(y,2q+1)$ and $\text{BUo}(y,2q+2)$, and has one output $\text{Rfo}(y,2q+1)$. The 2:1 Mux $\text{RF}(y,2q+2)$ has two inputs namely $\text{FRo}(y,2q+2)$ and $\text{BUo}(y,2q+1)$ and has one output $\text{Rfo}(y,2q+2)$.

20 The 2:1 Mux $\text{BU}(y,2q+1)$ has two inputs namely $\text{Bfi}(y,2q+1)$ and L3, and has one output $\text{BUo}(y,2q+1)$. The 2:1 Mux $\text{BU}(y,2q+2)$ has two inputs namely $\text{Bfi}(y,2q+2)$ and M3, and has one output $\text{BUo}(y,2q+2)$. The 2:1 Mux $\text{UB}(y,2q+1)$ has two inputs namely $\text{BUo}(y,2q+1)$ and $\text{FRo}(y,2q+2)$, and has one output $\text{UBo}(y,2q+1)$. The 2:1 Mux $\text{UB}(y,2q+2)$ has two inputs namely $\text{BUo}(y,2q+2)$ and $\text{FRo}(y,2q+1)$, and has one output $\text{UBo}(y,2q+2)$.

25 The stage (ring "y", stage "q+1") consists of 8 inputs namely $\text{Ffi}(y,2q+3)$, $\text{Ffi}(y,2q+4)$, $\text{Bfi}(y,2q+3)$, $\text{Bfi}(y,2q+4)$, J4, K4, L4, and M4; and 4 outputs $\text{UBo}(y,2q+3)$, $\text{UBo}(y,2q+4)$, $\text{Rfo}(y,2q+3)$, and $\text{Rfo}(y,2q+4)$. The stage (ring "y", stage "q+1") also consists of eight 2:1 Muxes namely $\text{FR}(y,2q+3)$, $\text{FR}(y,2q+4)$, $\text{RF}(y,2q+3)$, $\text{RF}(y,2q+4)$, $\text{BU}(y,2q+3)$, $\text{BU}(y,2q+4)$, $\text{UB}(y,2q+3)$, and $\text{UB}(y,2q+4)$. The 2:1 Mux $\text{FR}(y,2q+3)$ has two inputs namely $\text{Ffi}(y,2q+3)$ and J4, and has one

30

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

5 output $R_{o}(y,2q+3)$. The 2:1 Mux $R(y,2q+4)$ has two inputs namely $R_{i}(y,2q+4)$ and K4, and has one output $R_{o}(y,2q+4)$. The 2:1 Mux $RF(y,2q+3)$ has two inputs namely $R_{o}(y,2q+3)$ and $BU_{o}(y,2q+4)$, and has one output $RF_{o}(y,2q+3)$. The 2:1 Mux $RF(y,2q+4)$ has two inputs namely $R_{o}(y,2q+4)$ and $BU_{o}(y,2q+3)$, and has one output $RF_{o}(y,2q+4)$.

The 2:1 Mux $BU(y,2q+3)$ has two inputs namely $BU_{i}(y,2q+3)$ and L4, and has one output $BU_{o}(y,2q+3)$. The 2:1 Mux $BU(y,2q+4)$ has two inputs namely $BU_{i}(y,2q+4)$ and M4, and has one output $BU_{o}(y,2q+4)$. The 2:1 Mux $UB(y,2q+3)$ has two inputs namely $BU_{o}(y,2q+3)$ and $R_{o}(y,2q+4)$, and has one output $UB_{o}(y,2q+3)$. The 2:1 Mux $UB(y,2q+4)$ has two inputs namely $BU_{o}(y,2q+4)$ and $R_{o}(y,2q+3)$, and has one output $UB_{o}(y,2q+4)$.

10

The output $RF_{o}(y,2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $R_{i}(y,2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $UB_{o}(y,2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $BU_{i}(y,2q+1)$ of the stage (ring “y”, stage “q”).

15

The output $UF_{o}(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input $BR_{i}(y,2q+2)$ of the stage (ring “y”, stage “q+1”). The output $RF_{o}(y,2q+2)$ of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(1,2) to the input $BU_{i}(x,2p+2)$ of the stage (ring “x”, stage “p”).

20

The output $UF_{o}(x,2p+1)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(2,1) to the input $BR_{i}(y,2q+4)$ of the stage (ring “y”, stage “q+1”). The output $UB_{o}(y,2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to the input $BU_{i}(x,2p+1)$ of the stage (ring “x”, stage “p”).

In various embodiments, the inputs J1, K1, L1, and M1 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J2, K2, L2, and M2 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J3, K3, L3, and M3 are connected from any of the outputs of any other stages of any ring of any block of the

25

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Finally the inputs J4, K4, L4, and M4 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Referring to diagram 300C in FIG. 3C, illustrates all the connections between two
 5 arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 4 inputs namely $F_i(x, 2p+1)$, $F_i(x, 2p+2)$,
 10 $U_i(x, 2p+1)$, and $U_i(x, 2p+2)$; and 4 outputs $B_o(x, 2p+1)$, $B_o(x, 2p+2)$, $F_o(x, 2p+1)$, and $F_o(x, 2p+2)$. The stage (ring "x", stage "p") also consists of six 2:1 Muxes namely $F(x, 2p+1)$, $F(x, 2p+2)$, $U(x, 2p+1)$, $U(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $F_i(x, 2p+1)$ and $F_i(x, 2p+2)$ and has one output $F_o(x, 2p+1)$. The 2:1 Mux $F(x, 2p+2)$ has two inputs namely $F_i(x, 2p+1)$ and $F_i(x, 2p+2)$
 15 and has one output $F_o(x, 2p+2)$.

The 2:1 Mux $U(x, 2p+1)$ has two inputs namely $U_i(x, 2p+1)$ and $F_o(x, 2p+1)$ and has one output $U_o(x, 2p+1)$. The 2:1 Mux $U(x, 2p+2)$ has two inputs namely $U_i(x, 2p+2)$ and $F_o(x, 2p+2)$ and has one output $U_o(x, 2p+2)$. The 2:1 Mux $B(x, 2p+1)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $B_o(x, 2p+1)$. The 2:1 Mux
 20 $B(x, 2p+2)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $B_o(x, 2p+2)$.

The stage (ring "x", stage "p+1") consists of 4 inputs namely $F_i(x, 2p+3)$, $F_i(x, 2p+4)$, $U_i(x, 2p+3)$, and $U_i(x, 2p+4)$; and 4 outputs $B_o(x, 2p+3)$, $B_o(x, 2p+4)$, $F_o(x, 2p+3)$, and $F_o(x, 2p+4)$. The stage (ring "x", stage "p+1") also consists of six 2:1
 25 Muxes namely $F(x, 2p+3)$, $F(x, 2p+4)$, $U(x, 2p+3)$, $U(x, 2p+4)$, $B(x, 2p+3)$, and $B(x, 2p+4)$. The 2:1 Mux $F(x, 2p+3)$ has two inputs namely $F_i(x, 2p+3)$ and $F_i(x, 2p+4)$ and has one output $F_o(x, 2p+3)$. The 2:1 Mux $F(x, 2p+4)$ has two inputs namely $F_i(x, 2p+3)$ and $F_i(x, 2p+4)$ and has one output $F_o(x, 2p+4)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux $U(x,2p+3)$ has two inputs namely $U_i(x,2p+3)$ and $F_o(x,2p+3)$ and has one output $U_o(x,2p+3)$. The 2:1 Mux $U(x,2p+4)$ has two inputs namely $U_i(x,2p+4)$ and $F_o(x,2p+4)$ and has one output $U_o(x,2p+4)$. The 2:1 Mux $B(x,2p+3)$ has two inputs namely $U_o(x,2p+3)$ and $U_o(x,2p+4)$ and has one output $B_o(x,2p+3)$. The 2:1 Mux
 5 $B(x,2p+4)$ has two inputs namely $U_o(x,2p+3)$ and $U_o(x,2p+4)$ and has one output $B_o(x,2p+4)$.

The output $F_o(x,2p+1)$ of the stage (ring "x", stage "p") is connected to the input $F_i(x,2p+3)$ of the stage (ring "x", stage "p+1"). And the output $B_o(x,2p+3)$ of the stage (ring "x", stage "p+1") is connected to the input $U_i(x,2p+1)$ of the stage (ring "x", stage
 10 "p").

The stage (ring "y", stage "q") consists of 4 inputs namely $F_i(y,2q+1)$, $F_i(y,2q+2)$, $U_i(y,2q+1)$, and $U_i(y,2q+2)$; and 4 outputs $B_o(y,2q+1)$, $B_o(y,2q+2)$, $F_o(y,2q+1)$, and $F_o(y,2q+2)$. The stage (ring "y", stage "q") also consists of six 2:1 Muxes namely $F(y,2q+1)$, $F(y,2q+2)$, $U(y,2q+1)$, $U(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The 2:1 Mux
 15 $F(y,2q+1)$ has two inputs namely $F_i(y,2q+1)$ and $F_i(y,2q+2)$ and has one output $F_o(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $F_i(y,2q+1)$ and $F_i(y,2q+2)$ and has one output $F_o(y,2q+2)$.

The 2:1 Mux $U(y,2q+1)$ has two inputs namely $U_i(y,2q+1)$ and $F_o(y,2q+1)$ and has one output $U_o(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $U_i(y,2q+2)$ and $F_o(y,2q+2)$ and has one output $U_o(y,2q+2)$. The 2:1 Mux $B(y,2q+1)$ has two inputs namely $U_o(y,2q+1)$ and $U_o(y,2q+2)$ and has one output $B_o(y,2q+1)$. The 2:1 Mux
 20 $B(y,2q+2)$ has two inputs namely $U_o(y,2q+1)$ and $U_o(y,2q+2)$ and has one output $B_o(y,2q+2)$.

The stage (ring "y", stage "q+1") consists of 4 inputs namely $F_i(y,2q+3)$, $F_i(y,2q+4)$, $U_i(y,2q+3)$, and $U_i(y,2q+4)$; and 4 outputs $B_o(y,2q+3)$, $B_o(y,2q+4)$, $F_o(y,2q+3)$, and $F_o(y,2q+4)$. The stage (ring "y", stage "q+1") also consists of six 2:1 Muxes namely $F(y,2q+3)$, $F(y,2q+4)$, $U(y,2q+3)$, $U(y,2q+4)$, $B(y,2q+3)$, and $B(y,2q+4)$. The 2:1 Mux $F(y,2q+3)$ has two inputs namely $F_i(y,2q+3)$ and $F_i(y,2q+4)$ and has one
 25 output $F_o(y,2q+3)$. The 2:1 Mux $F(y,2q+4)$ has two inputs namely $F_i(y,2q+3)$ and
 30 $F_i(y,2q+4)$ and has one output $F_o(y,2q+4)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux $U(y,2q+3)$ has two inputs namely $U_i(y,2q+3)$ and $F_o(y,2q+3)$ and has one output $U_o(y,2q+3)$. The 2:1 Mux $U(y,2q+4)$ has two inputs namely $U_i(y,2q+4)$ and $F_o(y,2q+4)$ and has one output $U_o(y,2q+4)$. The 2:1 Mux $B(y,2q+3)$ has two inputs namely $U_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output $B_o(y,2q+3)$. The 2:1 Mux
 5 $B(y,2q+4)$ has two inputs namely $U_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output $B_o(y,2q+4)$.

The output $F_o(y,2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $F_i(y,2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $B_o(y,2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $U_i(y,2q+1)$ of the stage (ring “y”, stage
 10 “q”).

The output $F_o(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire $Hop(1,1)$ to the input $F_i(y,2q+4)$ of the stage (ring “y”, stage “q+1”). The output $B_o(x,2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire $Hop(1,2)$ to the input $U_i(y,2q+2)$ of the stage (ring “y”, stage “q”).

15 The output $F_o(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire $Hop(2,1)$ to the input $F_i(x,2p+4)$ of the stage (ring “x”, stage “p+1”). The output $B_o(y,2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire $Hop(2,2)$ to the input $U_i(x,2p+2)$ of the stage (ring “x”, stage “p”).

20 Referring to diagram 300D in FIG. 3D, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 4 inputs namely $F_i(x,2p+1)$, $F_i(x,2p+2)$, $U_i(x,2p+1)$, and $U_i(x,2p+2)$; and 4 outputs $B_o(x,2p+1)$, $B_o(x,2p+2)$, $F_o(x,2p+1)$, and $F_o(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of six 2:1 Muxes namely $F(x,2p+1)$, $F(x,2p+2)$, $U(x,2p+1)$, $U(x,2p+2)$, $B(x,2p+1)$, and $B(x,2p+2)$. The 2:1 Mux $F(x,2p+1)$ has two inputs namely $F_i(x,2p+1)$ and $F_i(x,2p+2)$ and has one output
 25

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$Fo(x,2p+1)$. The 2:1 Mux $F(x,2p+2)$ has two inputs namely $Fi(x,2p+1)$ and $Fi(x,2p+2)$ and has one output $Fo(x,2p+2)$.

The 2:1 Mux $U(x,2p+1)$ has two inputs namely $Ui(x,2p+1)$ and $Fo(x,2p+1)$ and has one output $Uo(x,2p+1)$. The 2:1 Mux $U(x,2p+2)$ has two inputs namely $Ui(x,2p+2)$ and $Fo(x,2p+2)$ and has one output $Uo(x,2p+2)$. The 2:1 Mux $B(x,2p+1)$ has two inputs namely $Uo(x,2p+1)$ and $Uo(x,2p+2)$ and has one output $Bo(x,2p+1)$. The 2:1 Mux $B(x,2p+2)$ has two inputs namely $Uo(x,2p+1)$ and $Uo(x,2p+2)$ and has one output $Bo(x,2p+2)$.

The stage (ring "x", stage "p+1") consists of 2 inputs namely $Fi(x,2p+3)$, $Fi(x,2p+4)$; and 2 outputs $Fo(x,2p+3)$, and $Fo(x,2p+4)$. The stage (ring "x", stage "p+1") also consists of two 2:1 Muxes namely $F(x,2p+3)$ and $F(x,2p+4)$. The 2:1 Mux $F(x,2p+3)$ has two inputs namely $Fi(x,2p+3)$ and $Fi(x,2p+4)$ and has one output $Fo(x,2p+3)$. The 2:1 Mux $F(x,2p+4)$ has two inputs namely $Fi(x,2p+3)$ and $Fi(x,2p+4)$ and has one output $Fo(x,2p+4)$.

The output $Fo(x,2p+1)$ of the stage (ring "x", stage "p") is connected to the input $Fi(x,2p+3)$ of the stage (ring "x", stage "p+1"). And the output $Fo(x,2p+3)$ of the stage (ring "x", stage "p+1") is connected to the input $Ui(x,2p+1)$ of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 4 inputs namely $Fi(y,2q+1)$, $Fi(y,2q+2)$, $Ui(y,2q+1)$, and $Ui(y,2q+2)$; and 4 outputs $Bo(y,2q+1)$, $Bo(y,2q+2)$, $Fo(y,2q+1)$, and $Fo(y,2q+2)$. The stage (ring "y", stage "q") also consists of six 2:1 Muxes namely $F(y,2q+1)$, $F(y,2q+2)$, $U(y,2q+1)$, $U(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The 2:1 Mux $F(y,2q+1)$ has two inputs namely $Fi(y,2q+1)$ and $Fi(y,2q+2)$ and has one output $Fo(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $Fi(y,2q+1)$ and $Fi(y,2q+2)$ and has one output $Fo(y,2q+2)$.

The 2:1 Mux $U(y,2q+1)$ has two inputs namely $Ui(y,2q+1)$ and $Fo(y,2q+1)$ and has one output $Uo(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $Ui(y,2q+2)$ and $Fo(y,2q+2)$ and has one output $Uo(y,2q+2)$. The 2:1 Mux $B(y,2q+1)$ has two inputs namely $Uo(y,2q+1)$ and $Uo(y,2q+2)$ and has one output $Bo(y,2q+1)$. The 2:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$B(y, 2q+2)$ has two inputs namely $U_o(y, 2q+1)$ and $U_o(y, 2q+2)$ and has one output $Bo(y, 2q+2)$.

The stage (ring “y”, stage “q+1”) consists of 4 inputs namely $Fi(y, 2q+3)$, $Fi(y, 2q+4)$, $Ui(y, 2q+3)$, and $Ui(y, 2q+4)$; and 4 outputs $Bo(y, 2q+3)$, $Bo(y, 2q+4)$, $Fo(y, 2q+3)$, and $Fo(y, 2q+4)$. The stage (ring “y”, stage “q+1”) also consists of six 2:1 Muxes namely $F(y, 2q+3)$, $F(y, 2q+4)$, $U(y, 2q+3)$, $U(y, 2q+4)$, $B(y, 2q+3)$, and $B(y, 2q+4)$. The 2:1 Mux $F(y, 2q+3)$ has two inputs namely $Fi(y, 2q+3)$ and $Fi(y, 2q+4)$ and has one output $Fo(y, 2q+3)$. The 2:1 Mux $F(y, 2q+4)$ has two inputs namely $Fi(y, 2q+3)$ and $Fi(y, 2q+4)$ and has one output $Fo(y, 2q+4)$.

10 The 2:1 Mux $U(y, 2q+3)$ has two inputs namely $Ui(y, 2q+3)$ and $Fo(y, 2q+3)$ and has one output $Uo(y, 2q+3)$. The 2:1 Mux $U(y, 2q+4)$ has two inputs namely $Ui(y, 2q+4)$ and $Fo(y, 2q+4)$ and has one output $Uo(y, 2q+4)$. The 2:1 Mux $B(y, 2q+3)$ has two inputs namely $Uo(y, 2q+3)$ and $Uo(y, 2q+4)$ and has one output $Bo(y, 2q+3)$. The 2:1 Mux $B(y, 2q+4)$ has two inputs namely $Uo(y, 2q+3)$ and $Uo(y, 2q+4)$ and has one output
15 $Bo(y, 2q+4)$.

The output $Fo(y, 2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $Fi(y, 2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $Bo(y, 2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $Ui(y, 2q+1)$ of the stage (ring “y”, stage “q”).

20 The output $Fo(x, 2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire $Hop(1, 1)$ to the input $Fi(y, 2q+4)$ of the stage (ring “y”, stage “q+1”). The output $Fo(x, 2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire $Hop(1, 2)$ to the input $Ui(y, 2q+2)$ of the stage (ring “y”, stage “q”).

The output $Fo(y, 2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire
25 $Hop(2, 1)$ to the input $Fi(x, 2p+4)$ of the stage (ring “x”, stage “p+1”). The output $Bo(y, 2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire $Hop(2, 2)$ to the input $Ui(x, 2p+2)$ of the stage (ring “x”, stage “p”).

Referring to diagram 300E in FIG. 3E, illustrates all the connections between root stage of a ring namely the stage (ring “x”, stage “p”) and two other arbitrary successive

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 4 inputs namely $F_i(x, 2p+1)$, $F_i(x, 2p+2)$, $U_i(x, 2p+1)$, and $U_i(x, 2p+2)$; and 4 outputs $B_o(x, 2p+1)$, $B_o(x, 2p+2)$, $F_o(x, 2p+1)$, and $F_o(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of six 2:1 Muxes namely $F(x, 2p+1)$, $F(x, 2p+2)$, $U(x, 2p+1)$, $U(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $F_i(x, 2p+1)$ and $F_i(x, 2p+2)$ and has one output $F_o(x, 2p+1)$. The 2:1 Mux $F(x, 2p+2)$ has two inputs namely $F_i(x, 2p+1)$ and $F_i(x, 2p+2)$ and has one output $F_o(x, 2p+2)$.

The 2:1 Mux $U(x, 2p+1)$ has two inputs namely $U_i(x, 2p+1)$ and $F_o(x, 2p+1)$ and has one output $U_o(x, 2p+1)$. The 2:1 Mux $U(x, 2p+2)$ has two inputs namely $U_i(x, 2p+2)$ and $F_o(x, 2p+2)$ and has one output $U_o(x, 2p+2)$. The 2:1 Mux $B(x, 2p+1)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $B_o(x, 2p+1)$. The 2:1 Mux $B(x, 2p+2)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $B_o(x, 2p+2)$.

The stage (ring “y”, stage “q”) consists of 4 inputs namely $F_i(y, 2q+1)$, $F_i(y, 2q+2)$, $U_i(y, 2q+1)$, and $U_i(y, 2q+2)$; and 4 outputs $B_o(y, 2q+1)$, $B_o(y, 2q+2)$, $F_o(y, 2q+1)$, and $F_o(y, 2q+2)$. The stage (ring “y”, stage “q”) also consists of six 2:1 Muxes namely $F(y, 2q+1)$, $F(y, 2q+2)$, $U(y, 2q+1)$, $U(y, 2q+2)$, $B(y, 2q+1)$, and $B(y, 2q+2)$. The 2:1 Mux $F(y, 2q+1)$ has two inputs namely $F_i(y, 2q+1)$ and $F_i(y, 2q+2)$ and has one output $F_o(y, 2q+1)$. The 2:1 Mux $F(y, 2q+2)$ has two inputs namely $F_i(y, 2q+1)$ and $F_i(y, 2q+2)$ and has one output $F_o(y, 2q+2)$.

The 2:1 Mux $U(y, 2q+1)$ has two inputs namely $U_i(y, 2q+1)$ and $F_o(y, 2q+1)$ and has one output $U_o(y, 2q+1)$. The 2:1 Mux $U(y, 2q+2)$ has two inputs namely $U_i(y, 2q+2)$ and $F_o(y, 2q+2)$ and has one output $U_o(y, 2q+2)$. The 2:1 Mux $B(y, 2q+1)$ has two inputs namely $U_o(y, 2q+1)$ and $U_o(y, 2q+2)$ and has one output $B_o(y, 2q+1)$. The 2:1 Mux $B(y, 2q+2)$ has two inputs namely $U_o(y, 2q+1)$ and $U_o(y, 2q+2)$ and has one output $B_o(y, 2q+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The stage (ring “y”, stage “q+1”) consists of 4 inputs namely $F_i(y,2q+3)$, $F_i(y,2q+4)$, $U_i(y,2q+3)$, and $U_i(y,2q+4)$; and 4 outputs $B_o(y,2q+3)$, $B_o(y,2q+4)$, $F_o(y,2q+3)$, and $F_o(y,2q+4)$. The stage (ring “y”, stage “q+1”) also consists of six 2:1 Muxes namely $F(y,2q+3)$, $F(y,2q+4)$, $U(y,2q+3)$, $U(y,2q+4)$, $B(y,2q+3)$, and $B(y,2q+4)$.
 5 The 2:1 Mux $F(y,2q+3)$ has two inputs namely $F_i(y,2q+3)$ and $F_i(y,2q+4)$ and has one output $F_o(y,2q+3)$. The 2:1 Mux $F(y,2q+4)$ has two inputs namely $F_i(y,2q+3)$ and $F_i(y,2q+4)$ and has one output $F_o(y,2q+4)$.

The 2:1 Mux $U(y,2q+3)$ has two inputs namely $U_i(y,2q+3)$ and $F_o(y,2q+3)$ and has one output $U_o(y,2q+3)$. The 2:1 Mux $U(y,2q+4)$ has two inputs namely $U_i(y,2q+4)$ and $F_o(y,2q+4)$ and has one output $U_o(y,2q+4)$. The 2:1 Mux $B(y,2q+3)$ has two inputs namely $U_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output $B_o(y,2q+3)$. The 2:1 Mux $B(y,2q+4)$ has two inputs namely $U_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output $B_o(y,2q+4)$.
 10

The output $F_o(y,2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $F_i(y,2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $B_o(y,2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $U_i(y,2q+1)$ of the stage (ring “y”, stage “q”).
 15

The output $F_o(x,2p+1)$ of the stage (ring “x”, stage “p”) is connected via the wire $Hop(1,2)$ to the input $U_i(y,2q+2)$ of the stage (ring “y”, stage “q”). The output $F_o(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire $Hop(1,1)$ to the input $F_i(y,2q+4)$ of the stage (ring “y”, stage “q+1”).
 20

The output $F_o(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire $Hop(2,1)$ to the input $U_i(x,2p+1)$ of the stage (ring “x”, stage “p”). The output $B_o(y,2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire $Hop(2,2)$ to the input $U_i(x,2p+2)$ of the stage (ring “x”, stage “p”).
 25

Just like in diagram 300A of FIG. 3A, in diagram 300B of FIG. 3B, in diagram 300C of FIG. 3C, diagram 300D of FIG. 3D, and in diagram 300E of FIG. 3E, the wires $Hop(1,1)$, $Hop(1,2)$, $Hop(2,1)$, and $Hop(2,2)$ are either internal hop wires or horizontal external hop wires or vertical external hop wires (hereinafter alternatively referred to as
 30 “cross links” or “cross middle links”).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The diagram 400A of FIG. 4A and 400B of FIG. 4B are different embodiments of all the connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks of 2D-grid 800. Referring to diagram 400A in FIG. 4A illustrates all the connections between an arbitrary stage of a ring namely the stages (ring “x”, stage “p”), and another arbitrary stage of any other ring namely the stages (ring “y”, stage “q”) of the complete multi-stage hierarchical network

5 $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 8 inputs namely $R_i(x, 2p+1)$, $R_i(x, 2p+2)$, $U_i(x, 2p+1)$, $U_i(x, 2p+2)$, J_1 , K_1 , L_1 , and M_1 ; and 4 outputs $B_o(x, 2p+1)$, $B_o(x, 2p+2)$, $F_o(x, 2p+1)$, and $F_o(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely $R(x, 2p+1)$, $R(x, 2p+2)$, $F(x, 2p+1)$, $F(x, 2p+2)$, $U(x, 2p+1)$, $U(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 2:1 Mux $R(x, 2p+1)$ has two inputs namely $R_i(x, 2p+1)$ and J_1 and has one output $R_o(x, 2p+1)$. The 2:1 Mux $R(x, 2p+2)$ has two inputs namely $R_i(x, 2p+2)$ and K_1 and has one output $R_o(x, 2p+2)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $R_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $F_o(x, 2p+1)$. The 2:1 Mux $F(x, 2p+2)$ has two inputs namely $R_o(x, 2p+2)$ and $U_o(x, 2p+1)$ and has one output $F_o(x, 2p+2)$.

10

15

The 2:1 Mux $U(x, 2p+1)$ has two inputs namely $U_i(x, 2p+1)$ and L_1 and has one output $U_o(x, 2p+1)$. The 2:1 Mux $U(x, 2p+2)$ has two inputs namely $U_i(x, 2p+2)$ and M_1 and has one output $U_o(x, 2p+2)$. The 2:1 Mux $B(x, 2p+1)$ has two inputs namely $U_o(x, 2p+1)$ and $R_o(x, 2p+2)$ and has one output $B_o(x, 2p+1)$. The 2:1 Mux $B(x, 2p+2)$ has two inputs namely $U_o(x, 2p+2)$ and $R_o(x, 2p+1)$ and has one output $B_o(x, 2p+2)$.

20

The stage (ring “y”, stage “q”) consists of 8 inputs namely $R_i(y, 2q+1)$, $R_i(y, 2q+2)$, $U_i(y, 2q+1)$, $U_i(y, 2q+2)$, J_3 , K_3 , L_3 , and M_3 ; and 4 outputs $B_o(y, 2q+1)$, $B_o(y, 2q+2)$, $F_o(y, 2q+1)$, and $F_o(y, 2q+2)$. The stage (ring “y”, stage “q”) also consists of eight 2:1 Muxes namely $R(y, 2q+1)$, $R(y, 2q+2)$, $F(y, 2q+1)$, $F(y, 2q+2)$, $U(y, 2q+1)$, $U(y, 2q+2)$, $B(y, 2q+1)$, and $B(y, 2q+2)$. The 2:1 Mux $R(y, 2q+1)$ has two inputs namely $R_i(y, 2q+1)$ and J_3 and has one output $R_o(y, 2q+1)$. The 2:1 Mux $R(y, 2q+2)$ has two inputs namely $R_i(y, 2q+2)$ and K_3 and has one output $R_o(y, 2q+2)$. The 2:1 Mux $F(y, 2q+1)$ has two inputs namely $R_o(y, 2q+1)$ and $U_o(y, 2q+2)$ and has one output

25

30

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Ro(y,2q+2) and Uo(y,2q+1) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and L3, and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and M3,
5 and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Ro(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+2) and Ro(y,2q+1) and has one output Bo(y,2q+2).

The output Fo(x,2p+2) of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input Ri(y,2q+2) of the stage (ring “y”, stage “q”). The output
10 Bo(y,2q+2) of the stage (ring “y”, stage “q”) is connected via the wire Hop(1,2) to the input Ui(x,2p+2) of the stage (ring “x”, stage “p”).

Ring “x” and ring “y” may or may not belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. If ring “x” and ring “y” belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then
15 the wires Hop(1,1) and Hop(1,2) are hereinafter called “internal hop wires”. For example if “x = 2” and “y = 3” and both the ring 2 and ring 3 belong to the same block (9,9) of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are “internal hop wires”.

If ring “x” and ring “y” belong to the different blocks of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1) and Hop(1,2) are
20 hereinafter called “external hop wires”. The external hop wires Hop(1,1) and Hop(1,2) may be horizontal wires or vertical wires. The length of the external hop wires is Manhattan distance between the corresponding blocks, hereinafter “hop length”. For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (1,6) of 2D-grid 800 then the external hop wires are hereinafter called “horizontal external hop wires”.
25 And the hop length of the horizontal hop wires Hop(1,1) and Hop(1,2) is given by $6 - 1 = 5$. Similarly if ring “x” and ring “y” belong to two blocks in the same horizontal row of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are horizontal external hop wires.

For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (9,1) of 2D-grid 800 then the external hop wires are hereinafter called “vertical external hop

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

wires". And the hop length of the vertical hop wires Hop(1,1) and Hop(1,2) is given by $9 - 1 = 8$. Similarly if ring "x" and ring "y" belong to two blocks in the same vertical column of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are vertical external hop wires. External hop wires are typically horizontal or vertical according to the current
5 invention.

Referring to diagram 400B in FIG. 4B illustrates all the connections between an arbitrary stage of a ring namely the stages (ring "x", stage "p"), and another arbitrary stage of any other ring namely the stages (ring "y", stage "q") of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

10 The stage (ring "x", stage "p") consists of 8 inputs namely $Ri(x, 2p+1)$, $Ri(x, 2p+2)$, $Ui(x, 2p+1)$, $Ui(x, 2p+2)$, J1, K1, L1, and M1; and 4 outputs $Bo(x, 2p+1)$, $Bo(x, 2p+2)$, $Fo(x, 2p+1)$, and $Fo(x, 2p+2)$. The stage (ring "x", stage "p") also consists of four 4:1 Muxes namely $F(x, 2p+1)$, $F(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 4:1 Mux $F(x, 2p+1)$ has four inputs namely $Ri(x, 2p+1)$, $Ri(x, 2p+2)$, $Ui(x, 2p+2)$, and J1 and has one
15 output $Fo(x, 2p+1)$. The 4:1 Mux $F(x, 2p+2)$ has four inputs namely $Ri(x, 2p+1)$, $Ri(x, 2p+2)$, $Ui(x, 2p+1)$, and K1 and has one output $Fo(x, 2p+2)$.

The 4:1 Mux $B(x, 2p+1)$ has four inputs namely $Ui(x, 2p+1)$, $Ui(x, 2p+2)$, $Ri(x, 2p+2)$, and L1 and has one output $Bo(x, 2p+1)$. The 2:1 Mux $B(x, 2p+2)$ has two inputs namely $Ui(x, 2p+1)$, $Ui(x, 2p+2)$, $Ri(x, 2p+1)$, and M1 and has one output
20 $Bo(x, 2p+2)$.

The stage (ring "y", stage "q") consists of 8 inputs namely $Ri(y, 2q+1)$, $Ri(y, 2q+2)$, $Ui(y, 2q+1)$, $Ui(y, 2q+2)$, J3, K3, L3, and M3; and 4 outputs $Bo(y, 2q+1)$, $Bo(y, 2q+2)$, $Fo(y, 2q+1)$, and $Fo(y, 2q+2)$. The stage (ring "y", stage "q") also consists of four 4:1 Muxes namely $F(y, 2q+1)$, $F(y, 2q+2)$, $B(y, 2q+1)$, and $B(y, 2q+2)$. The 4:1 Mux
25 $F(y, 2q+1)$ has four inputs namely $Ri(y, 2q+1)$, $Ri(y, 2q+2)$, $Ui(y, 2q+2)$, and J3 and has one output $Fo(y, 2q+1)$. The 4:1 Mux $F(y, 2q+2)$ has four inputs namely $Ri(y, 2q+1)$, $Ri(y, 2q+2)$, $Ui(y, 2q+1)$, and K3 and has one output $Fo(y, 2q+2)$.

The 4:1 Mux $B(y, 2q+1)$ has four inputs namely $Ui(y, 2q+1)$, $Ui(y, 2q+2)$, $Ri(y, 2q+2)$, and L3, and has one output $Bo(y, 2q+1)$. The 4:1 Mux $B(y, 2q+2)$ has four

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

inputs namely $U_i(y, 2q+1)$, $U_i(y, 2q+2)$, $R_i(y, 2q+1)$, and M3, and has one output $B_o(y, 2q+2)$.

The output $F_o(x, 2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input $R_i(y, 2q+2)$ of the stage (ring “y”, stage “q”). The output
 5 $B_o(y, 2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire Hop(1,2) to the input $U_i(x, 2p+2)$ of the stage (ring “x”, stage “p”).

Ring “x” and ring “y” may or may not belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. If ring “x” and ring “y” belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then
 10 the wires Hop(1,1) and Hop(1,2) are hereinafter called “internal hop wires”. For example if “x = 2” and “y = 3” and both the ring 2 and ring 3 belong to the same block (9,9) of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are “internal hop wires”.

If ring “x” and ring “y” belong to the different blocks of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1) and Hop(1,2) are
 15 hereinafter called “external hop wires”. The external hop wires Hop(1,1) and Hop(1,2) may be horizontal wires or vertical wires. The length of the external hop wires is Manhattan distance between the corresponding blocks, hereinafter “hop length”. For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (1,6) of 2D-grid 800 then the external hop wires are hereinafter called “horizontal external hop wires”.
 20 And the hop length of the horizontal hop wires Hop(1,1) and Hop(1,2) is given by $6 - 1 = 5$. Similarly if ring “x” and ring “y” belong to two blocks in the same horizontal row of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are horizontal external hop wires.

For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (9,1) of 2D-grid 800 then the external hop wires are hereinafter called “vertical external hop
 25 wires”. And the hop length of the vertical hop wires Hop(1,1) and Hop(1,2) is given by $9 - 1 = 8$. Similarly if ring “x” and ring “y” belong to two blocks in the same vertical column of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are vertical external hop wires. External hop wires are typically horizontal or vertical according to the current invention.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The diagram 500A of FIG. 5A is an embodiment of all the connections with multi-drop hop wires, between two arbitrary successive stages in two different rings of different blocks of 2D-grid 800. Referring to diagram 500A in FIG. 5A illustrates all the connections with multi-drop hop wires, between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. The multi-drop hop wires are also connected to two other stages (ring “a”, stage “s”) and (ring “b”, stage “t”) belonging to a third block.

10 The stage (ring “x”, stage “p”) consists of 8 inputs namely $R_i(x, 2p+1)$, $R_i(x, 2p+2)$, $U_i(x, 2p+1)$, $U_i(x, 2p+2)$, J_1 , K_1 , L_1 , and M_1 ; and 4 outputs $B_o(x, 2p+1)$, $B_o(x, 2p+2)$, $F_o(x, 2p+1)$, and $F_o(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely $R(x, 2p+1)$, $R(x, 2p+2)$, $F(x, 2p+1)$, $F(x, 2p+2)$, $U(x, 2p+1)$, $U(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 2:1 Mux $R(x, 2p+1)$ has two inputs namely
15 $R_i(x, 2p+1)$ and J_1 , and has one output $R_o(x, 2p+1)$. The 2:1 Mux $R(x, 2p+2)$ has two inputs namely $R_i(x, 2p+2)$ and K_1 , and has one output $R_o(x, 2p+2)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $R_o(x, 2p+1)$ and $U_o(x, 2p+2)$, and has one output $F_o(x, 2p+1)$. The 2:1 Mux $F(x, 2p+2)$ has two inputs namely $R_o(x, 2p+2)$ and $U_o(x, 2p+1)$, and has one output $F_o(x, 2p+2)$.

20 The 2:1 Mux $U(x, 2p+1)$ has two inputs namely $U_i(x, 2p+1)$ and L_1 , and has one output $U_o(x, 2p+1)$. The 2:1 Mux $U(x, 2p+2)$ has two inputs namely $U_i(x, 2p+2)$ and M_1 , and has one output $U_o(x, 2p+2)$. The 2:1 Mux $B(x, 2p+1)$ has two inputs namely $U_o(x, 2p+1)$ and $R_o(x, 2p+2)$, and has one output $B_o(x, 2p+1)$. The 2:1 Mux $B(x, 2p+2)$ has two inputs namely $U_o(x, 2p+2)$ and $R_o(x, 2p+1)$, and has one output $B_o(x, 2p+2)$.

25 The stage (ring “x”, stage “p+1”) consists of 8 inputs namely $R_i(x, 2p+3)$, $R_i(x, 2p+4)$, $U_i(x, 2p+3)$, $U_i(x, 2p+4)$, J_2 , K_2 , L_2 , and M_2 ; and 4 outputs $B_o(x, 2p+3)$, $B_o(x, 2p+4)$, $F_o(x, 2p+3)$, and $F_o(x, 2p+4)$. The stage (ring “x”, stage “p+1”) also consists of eight 2:1 Muxes namely $R(x, 2p+3)$, $R(x, 2p+4)$, $F(x, 2p+3)$, $F(x, 2p+4)$, $U(x, 2p+3)$, $U(x, 2p+4)$, $B(x, 2p+3)$, and $B(x, 2p+4)$. The 2:1 Mux $R(x, 2p+3)$ has two inputs namely
30 $R_i(x, 2p+3)$ and J_2 , and has one output $R_o(x, 2p+3)$. The 2:1 Mux $R(x, 2p+4)$ has two inputs namely $R_i(x, 2p+4)$ and K_2 , and has one output $R_o(x, 2p+4)$. The 2:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$F(x,2p+3)$ has two inputs namely $Ro(x,2p+3)$ and $Uo(x,2p+4)$, and has one output $Fo(x,2p+3)$. The 2:1 Mux $F(x,2p+4)$ has two inputs namely $Ro(x,2p+4)$ and $Uo(x,2p+3)$, and has one output $Fo(x,2p+4)$.

The 2:1 Mux $U(x,2p+3)$ has two inputs namely $Ui(x,2p+3)$ and $L2$, and has one
5 output $Uo(x,2p+3)$. The 2:1 Mux $U(x,2p+4)$ has two inputs namely $Ui(x,2p+4)$ and $M2$, and has one output $Uo(x,2p+4)$. The 2:1 Mux $B(x,2p+3)$ has two inputs namely $Uo(x,2p+3)$ and $Ro(x,2p+4)$, and has one output $Bo(x,2p+3)$. The 2:1 Mux $B(x,2p+4)$ has two inputs namely $Uo(x,2p+4)$ and $Ro(x,2p+3)$, and has one output $Bo(x,2p+4)$.

The output $Fo(x,2p+1)$ of the stage (ring "x", stage "p") is connected to the input
10 $Ri(x,2p+3)$ of the stage (ring "x", stage "p+1"). And the output $Bo(x,2p+3)$ of the stage (ring "x", stage "p+1") is connected to the input $Ui(x,2p+1)$ of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 8 inputs namely $Ri(y,2q+1)$,
 $Ri(y,2q+2)$, $Ui(y,2q+1)$, $Ui(y,2q+2)$, $J3$, $K3$, $L3$, and $M3$; and 4 outputs $Bo(y,2q+1)$,
15 $Bo(y,2q+2)$, $Fo(y,2q+1)$, and $Fo(y,2q+2)$. The stage (ring "y", stage "q") also consists of eight 2:1 Muxes namely $R(y,2q+1)$, $R(y,2q+2)$, $F(y,2q+1)$, $F(y,2q+2)$, $U(y,2q+1)$, $U(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The 2:1 Mux $R(y,2q+1)$ has two inputs namely $Ri(y,2q+1)$ and $J3$, and has one output $Ro(y,2q+1)$. The 2:1 Mux $R(y,2q+2)$ has two inputs namely $Ri(y,2q+2)$ and $K3$, and has one output $Ro(y,2q+2)$. The 2:1 Mux
20 $F(y,2q+1)$ has two inputs namely $Ro(y,2q+1)$ and $Uo(y,2q+2)$, and has one output $Fo(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $Ro(y,2q+2)$ and $Uo(y,2q+1)$ and has one output $Fo(y,2q+2)$.

The 2:1 Mux $U(y,2q+1)$ has two inputs namely $Ui(y,2q+1)$ and $L3$, and has one
output $Uo(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $Ui(y,2q+2)$ and $M3$,
25 and has one output $Uo(y,2q+2)$. The 2:1 Mux $B(y,2q+1)$ has two inputs namely $Uo(y,2q+1)$ and $Ro(y,2q+2)$, and has one output $Bo(y,2q+1)$. The 2:1 Mux $B(y,2q+2)$ has two inputs namely $Uo(y,2q+2)$ and $Ro(y,2q+1)$, and has one output $Bo(y,2q+2)$.

The stage (ring "y", stage "q+1") consists of 8 inputs namely $Ri(y,2q+3)$,
 $Ri(y,2q+4)$, $Ui(y,2q+3)$, $Ui(y,2q+4)$, $J4$, $K4$, $L4$, and $M4$; and 4 outputs $Bo(y,2q+3)$,
30 $Bo(y,2q+4)$, $Fo(y,2q+3)$, and $Fo(y,2q+4)$. The stage (ring "y", stage "q+1") also consists

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

of eight 2:1 Muxes namely $R(y,2q+3)$, $R(y,2q+4)$, $F(y,2q+3)$, $F(y,2q+4)$, $U(y,2q+3)$,
 $U(y,2q+4)$, $B(y,2q+3)$, and $B(y,2q+4)$. The 2:1 Mux $R(y,2q+3)$ has two inputs namely
 $Ri(y,2q+3)$ and $J4$, and has one output $Ro(y,2q+3)$. The 2:1 Mux $R(y,2q+4)$ has two
inputs namely $Ri(y,2q+4)$ and $K4$, and has one output $Ro(y,2q+4)$. The 2:1 Mux
5 $F(y,2q+3)$ has two inputs namely $Ro(y,2q+3)$ and $Uo(y,2q+4)$, and has one output
 $Fo(y,2q+3)$. The 2:1 Mux $F(y,2q+4)$ has two inputs namely $Ro(y,2q+4)$ and $Uo(y,2q+3)$,
and has one output $Fo(y,2q+4)$.

The 2:1 Mux $U(y,2q+3)$ has two inputs namely $Ui(y,2q+3)$ and $L4$, and has one
output $Uo(y,2q+3)$. The 2:1 Mux $U(y,2q+4)$ has two inputs namely $Ui(y,2q+4)$ and $M4$,
10 and has one output $Uo(y,2q+4)$. The 2:1 Mux $B(y,2q+3)$ has two inputs namely
 $Uo(y,2q+3)$ and $Ro(y,2q+4)$, and has one output $Bo(y,2q+3)$. The 2:1 Mux $B(y,2q+4)$ has
two inputs namely $Uo(y,2q+4)$ and $Ro(y,2q+3)$, and has one output $Bo(y,2q+4)$.

The output $Fo(y,2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input
 $Ri(y,2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $Bo(y,2q+3)$ of the stage
15 (ring “y”, stage “q+1”) is connected to the input $Ui(y,2q+1)$ of the stage (ring “y”, stage
“q”).

The output $Fo(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire
Hop(1,1) to the input $Ri(y,2q+4)$ of the stage (ring “y”, stage “q+1”). The output
 $Bo(x,2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire Hop(1,2) to the
20 input $Ui(y,2q+2)$ of the stage (ring “y”, stage “q”).

The output $Fo(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire
Hop(2,1) to the input $Ri(x,2p+4)$ of the stage (ring “x”, stage “p+1”). The output
 $Bo(y,2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to the
input $Ui(x,2p+2)$ of the stage (ring “x”, stage “p”).

25 In various embodiments, the inputs $J1$, $K1$, $L1$, and $M1$ are connected from any of
the outputs of any other stages of any ring of any block of the multi-stage hierarchical
network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs $J2$, $K2$, $L2$, and $M2$ are connected from
any of the outputs of any other stages of any ring of any block of the multi-stage
hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs $J3$, $K3$, $L3$, and $M3$ are

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Finally the inputs J4, K4, L4, and M4 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

5 The stage (ring "a", stage "s") consists of 8 inputs namely $R_i(a, 2s+1)$, $R_i(a, 2s+2)$, $U_i(a, 2s+1)$, $U_i(a, 2s+2)$, J5, K5, L5, and M5; and 4 outputs $B_o(a, 2s+1)$, $B_o(a, 2s+2)$, $F_o(a, 2s+1)$, and $F_o(a, 2s+2)$. The stage (ring "a", stage "s") also consists of eight 2:1 Muxes namely $R(a, 2s+1)$, $R(a, 2s+2)$, $F(a, 2s+1)$, $F(a, 2s+2)$, $U(a, 2s+1)$, $U(a, 2s+2)$, $B(a, 2s+1)$, and $B(a, 2s+2)$. The 2:1 Mux $R(a, 2s+1)$ has two inputs namely $R_i(a, 2s+1)$ and
10 J5, and has one output $R_o(a, 2s+1)$. The 2:1 Mux $R(a, 2s+2)$ has two inputs namely $R_i(a, 2s+2)$ and K5, and has one output $R_o(a, 2s+2)$. The 2:1 Mux $F(a, 2s+1)$ has two inputs namely $R_o(a, 2s+1)$ and $U_o(a, 2s+2)$, and has one output $F_o(a, 2s+1)$. The 2:1 Mux $F(a, 2s+2)$ has two inputs namely $R_o(a, 2s+2)$ and $U_o(a, 2s+1)$, and has one output $F_o(a, 2s+2)$.

15 The 2:1 Mux $U(a, 2s+1)$ has two inputs namely $U_i(a, 2s+1)$ and L5, and has one output $U_o(a, 2s+1)$. The 2:1 Mux $U(a, 2s+2)$ has two inputs namely $U_i(a, 2s+2)$ and M5, and has one output $U_o(a, 2s+2)$. The 2:1 Mux $B(a, 2s+1)$ has two inputs namely $U_o(a, 2s+1)$ and $R_o(a, 2s+2)$, and has one output $B_o(a, 2s+1)$. The 2:1 Mux $B(a, 2s+2)$ has two inputs namely $U_o(a, 2s+2)$ and $R_o(a, 2s+1)$, and has one output $B_o(a, 2s+2)$.

20 The stage (ring "b", stage "t") consists of 8 inputs namely $R_i(b, 2t+1)$, $R_i(b, 2t+2)$, $U_i(b, 2t+1)$, $U_i(b, 2t+2)$, J6, K6, L6, and M6; and 4 outputs $B_o(b, 2t+1)$, $B_o(b, 2t+2)$, $F_o(b, 2t+1)$, and $F_o(b, 2t+2)$. The stage (ring "b", stage "t") also consists of eight 2:1 Muxes namely $R(b, 2t+1)$, $R(b, 2t+2)$, $F(b, 2t+1)$, $F(b, 2t+2)$, $U(b, 2t+1)$, $U(b, 2t+2)$, $B(b, 2t+1)$, and $B(b, 2t+2)$. The 2:1 Mux $R(b, 2t+1)$ has two inputs namely $R_i(b, 2t+1)$ and
25 J6, and has one output $R_o(b, 2t+1)$. The 2:1 Mux $R(b, 2t+2)$ has two inputs namely $R_i(b, 2t+2)$ and K6, and has one output $R_o(b, 2t+2)$. The 2:1 Mux $F(b, 2t+1)$ has two inputs namely $R_o(b, 2t+1)$ and $U_o(b, 2t+2)$, and has one output $F_o(b, 2t+1)$. The 2:1 Mux $F(b, 2t+2)$ has two inputs namely $R_o(b, 2t+2)$ and $U_o(b, 2t+1)$, and has one output $F_o(b, 2t+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux U(b,2t+1) has two inputs namely $U_i(b,2t+1)$ and L6, and has one output $U_o(b,2t+1)$. The 2:1 Mux U(b,2t+2) has two inputs namely $U_i(b,2t+2)$ and M6, and has one output $U_o(b,2t+2)$. The 2:1 Mux B(b,2t+1) has two inputs namely $U_o(b,2t+1)$ and $R_o(b,2t+2)$, and has one output $B_o(b,2t+1)$. The 2:1 Mux B(b,2t+2) has
 5 two inputs namely $U_o(b,2t+2)$ and $R_o(b,2t+1)$, and has one output $B_o(b,2t+2)$.

The wire Hop(1,1) starting from the output $F_o(x,2p+2)$ of the stage (ring "x", stage "p") is also connected to L5 of the stage (ring "a", stage "s"), in addition to the input $R_i(y,2q+4)$ of the stage (ring "y", stage "q+1"). The stage (ring "x", stage "p"), the stage (ring "a", stage "s"), and the stage (ring "y", stage "q+1") may belong to three
 10 different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Therefore the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may not be equal to the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "y", stage "q+1"). For example the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring
 15 "a", stage "s") may be one where as the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y+1") may be two. In such a case the wire Hop(1,1) is called hereinafter a "multi-drop hop wire". The wire Hop(1,1) may be either horizontal hop wire or vertical hop wire. Also multi-drop hop wires are either horizontal external hop wires or vertical external hop wires. Similarly the hop
 20 length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be any number greater than or equal to one, and also the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y+1") may be any number greater or equal to one.

In general a multi-drop hop wire may be dropping or terminating in more than one
 25 different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. For example a multi-drop hop wire starting from one block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ may be terminating at three different blocks or four different blocks, etc.

The wire Hop(1,2) starting from the output $B_o(x,2p+4)$ of the stage (ring "x", stage "p+1") is also connected to J6 of the stage (ring "b", stage "t"), in addition to the
 30

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

input $U_i(y, 2q+2)$ of the stage (ring “y”, stage “q”). The wire Hop(1,2) is also an example of multi-drop hop wire when the stage (ring “x”, stage “p+1”), the stage (ring “b”, stage “t”) and the stage (ring “y”, stage “q”) belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

5 The wire Hop(2,1) starting from the output $F_o(y, 2q+2)$ of the stage (ring “y”, stage “q”) is also connected to M5 of the stage (ring “a”, stage “s”), in addition to the input $R_i(x, 2p+4)$ of the stage (ring “x”, stage “p+1”). The wire Hop(2,1) is also an example of multi-drop hop wire when the stage (ring “x”, stage “p+1”), the stage (ring “a”, stage “s”) and the stage (ring “y”, stage “q”) belong to three different blocks of the
10 multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The wire Hop(2,2) starting from the output $B_o(y, 2q+4)$ of the stage (ring “y”, stage “q+1”) is also connected to K6 of the stage (ring “b”, stage “t”), in addition to the input $U_i(x, 2p+2)$ of the stage (ring “x”, stage “p”). The wire Hop(2,2) is also an example of multi-drop hop wire when the stage (ring “x”, stage “p”), the stage (ring “b”, stage “t”) and the stage (ring “y”, stage “q+1”) belong to three different blocks of the multi-stage
15 hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

In various embodiments, the inputs J5, K5, L5, and M5 are connected from any of the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Also the inputs J6, K6, L6, and M6
20 are connected from any of the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The diagram 600A of FIG. 6A and 600B of FIG. 6B are different embodiments of all the connections with multi-drop hop wires, between two arbitrary stages in two different rings of different blocks of 2D-grid 800. Referring to diagram 600A in FIG. 6A
25 illustrates all the connections with multi-drop hop wires, between an arbitrary stage of a ring namely the stages (ring “x”, stage “p”), and another arbitrary stage of any other ring namely the stages (ring “y”, stage “q”) of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. The multi-drop hop wires are also connected to another stage (ring “a”, stage “s”) belonging to a third block.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The stage (ring “x”, stage “p”) consists of 8 inputs namely $R_i(x,2p+1)$, $R_i(x,2p+2)$, $U_i(x,2p+1)$, $U_i(x,2p+2)$, J_1 , K_1 , L_1 , and M_1 ; and 4 outputs $B_o(x,2p+1)$, $B_o(x,2p+2)$, $F_o(x,2p+1)$, and $F_o(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely $R(x,2p+1)$, $R(x,2p+2)$, $F(x,2p+1)$, $F(x,2p+2)$, $U(x,2p+1)$, $U(x,2p+2)$, $B(x,2p+1)$, and $B(x,2p+2)$. The 2:1 Mux $R(x,2p+1)$ has two inputs namely $R_i(x,2p+1)$ and J_1 and has one output $R_o(x,2p+1)$. The 2:1 Mux $R(x,2p+2)$ has two inputs namely $R_i(x,2p+2)$ and K_1 and has one output $R_o(x,2p+2)$. The 2:1 Mux $F(x,2p+1)$ has two inputs namely $R_o(x,2p+1)$ and $U_o(x,2p+2)$ and has one output $F_o(x,2p+1)$. The 2:1 Mux $F(x,2p+2)$ has two inputs namely $R_o(x,2p+2)$ and $U_o(x,2p+1)$ and has one output $F_o(x,2p+2)$.

The 2:1 Mux $U(x,2p+1)$ has two inputs namely $U_i(x,2p+1)$ and L_1 and has one output $U_o(x,2p+1)$. The 2:1 Mux $U(x,2p+2)$ has two inputs namely $U_i(x,2p+2)$ and M_1 and has one output $U_o(x,2p+2)$. The 2:1 Mux $B(x,2p+1)$ has two inputs namely $U_o(x,2p+1)$ and $R_o(x,2p+2)$ and has one output $B_o(x,2p+1)$. The 2:1 Mux $B(x,2p+2)$ has two inputs namely $U_o(x,2p+2)$ and $R_o(x,2p+1)$ and has one output $B_o(x,2p+2)$.

The stage (ring “y”, stage “q”) consists of 8 inputs namely $R_i(y,2q+1)$, $R_i(y,2q+2)$, $U_i(y,2q+1)$, $U_i(y,2q+2)$, J_3 , K_3 , L_3 , and M_3 ; and 4 outputs $B_o(y,2q+1)$, $B_o(y,2q+2)$, $F_o(y,2q+1)$, and $F_o(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of eight 2:1 Muxes namely $R(y,2q+1)$, $R(y,2q+2)$, $F(y,2q+1)$, $F(y,2q+2)$, $U(y,2q+1)$, $U(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The 2:1 Mux $R(y,2q+1)$ has two inputs namely $R_i(y,2q+1)$ and J_3 and has one output $R_o(y,2q+1)$. The 2:1 Mux $R(y,2q+2)$ has two inputs namely $R_i(y,2q+2)$ and K_3 and has one output $R_o(y,2q+2)$. The 2:1 Mux $F(y,2q+1)$ has two inputs namely $R_o(y,2q+1)$ and $U_o(y,2q+2)$ and has one output $F_o(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $R_o(y,2q+2)$ and $U_o(y,2q+1)$ and has one output $F_o(y,2q+2)$.

The 2:1 Mux $U(y,2q+1)$ has two inputs namely $U_i(y,2q+1)$ and L_3 , and has one output $U_o(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $U_i(y,2q+2)$ and M_3 , and has one output $U_o(y,2q+2)$. The 2:1 Mux $B(y,2q+1)$ has two inputs namely $U_o(y,2q+1)$ and $R_o(y,2q+2)$ and has one output $B_o(y,2q+1)$. The 2:1 Mux $B(y,2q+2)$ has two inputs namely $U_o(y,2q+2)$ and $R_o(y,2q+1)$ and has one output $B_o(y,2q+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The output $Fo(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input $Ri(y,2q+2)$ of the stage (ring “y”, stage “q”). The output $Bo(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire Hop(1,2) to the input $Ui(x,2p+2)$ of the stage (ring “x”, stage “p”).

5 The wire Hop(1,1) starting from the output $Fo(x,2p+2)$ of the stage (ring “x”, stage “p”) is also connected to L2 of the stage (ring “a”, stage “s”), in addition to the input $Ri(y,2q+2)$ of the stage (ring “y”, stage “q”). The stage (ring “x”, stage “p”), the stage (ring “a”, stage “s”), and the stage (ring “y”, stage “q”) may belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Therefore the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “a”, stage “s”) may not be equal to the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “y”, stage “q”). For example the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “a”, stage “s”) may be one where as the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “q”, stage “y”) may be two. Hence the wire Hop(1,1) is a multi-drop hop wire. Also the wire Hop(1,1) is either horizontal external hop wire or vertical external hop wire. Similarly the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “a”, stage “s”) may be any number greater than or equal to one, and also the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “q”, stage “y”) may be any number greater or equal to one.

25 The wire Hop(1,2) starting from the output $Bo(y,2q+2)$ of the stage (ring “y”, stage “q”) is also connected to K2 of the stage (ring “a”, stage “s”), in addition to the input $Ui(x,2p+2)$ of the stage (ring “x”, stage “p”). The wire Hop(1,2) is also an example of multi-drop hop wire when the stage (ring “x”, stage “p”), the stage (ring “a”, stage “s”) and the stage (ring “y”, stage “q”) belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

30 In various embodiments, the inputs J2, K2, L2, and M2 are connected from any of the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Referring to diagram 600B in FIG. 6B illustrates all the connections with multi-drop hop wires, between an arbitrary stage of a ring namely the stages (ring “x”, stage “p”), and another arbitrary stage of any other ring namely the stages (ring “y”, stage “q”) of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. The multi-drop hop wires are also connected to another stage (ring “a”, stage “s”) belonging to a third block.

The stage (ring “x”, stage “p”) consists of 8 inputs namely $Ri(x, 2p+1)$, $Ri(x, 2p+2)$, $Ui(x, 2p+1)$, $Ui(x, 2p+2)$, J1, K1, L1, and M1; and 4 outputs $Bo(x, 2p+1)$, $Bo(x, 2p+2)$, $Fo(x, 2p+1)$, and $Fo(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of four 4:1 Muxes namely $F(x, 2p+1)$, $F(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 4:1 Mux $F(x, 2p+1)$ has four inputs namely $Ri(x, 2p+1)$, $Ri(x, 2p+2)$, $Ui(x, 2p+2)$, and J1 and has one output $Fo(x, 2p+1)$. The 4:1 Mux $F(x, 2p+2)$ has four inputs namely $Ri(x, 2p+1)$, $Ri(x, 2p+2)$, $Ui(x, 2p+1)$, and K1 and has one output $Fo(x, 2p+2)$.

The 4:1 Mux $B(x, 2p+1)$ has four inputs namely $Ui(x, 2p+1)$, $Ui(x, 2p+2)$, $Ri(x, 2p+2)$, and L1 and has one output $Bo(x, 2p+1)$. The 2:1 Mux $B(x, 2p+2)$ has two inputs namely $Ui(x, 2p+1)$, $Ui(x, 2p+2)$, $Ri(x, 2p+1)$, and M1 and has one output $Bo(x, 2p+2)$.

The stage (ring “y”, stage “q”) consists of 8 inputs namely $Ri(y, 2q+1)$, $Ri(y, 2q+2)$, $Ui(y, 2q+1)$, $Ui(y, 2q+2)$, J3, K3, L3, and M3; and 4 outputs $Bo(y, 2q+1)$, $Bo(y, 2q+2)$, $Fo(y, 2q+1)$, and $Fo(y, 2q+2)$. The stage (ring “y”, stage “q”) also consists of four 4:1 Muxes namely $F(y, 2q+1)$, $F(y, 2q+2)$, $B(y, 2q+1)$, and $B(y, 2q+2)$. The 4:1 Mux $F(y, 2q+1)$ has four inputs namely $Ri(y, 2q+1)$, $Ri(y, 2q+2)$, $Ui(y, 2q+2)$, and J3 and has one output $Fo(y, 2q+1)$. The 4:1 Mux $F(y, 2q+2)$ has four inputs namely $Ri(y, 2q+1)$, $Ri(y, 2q+2)$, $Ui(y, 2q+1)$, and K3 and has one output $Fo(y, 2q+2)$.

The 4:1 Mux $B(y, 2q+1)$ has four inputs namely $Ui(y, 2q+1)$, $Ui(y, 2q+2)$, $Ri(y, 2q+2)$, and L3, and has one output $Bo(y, 2q+1)$. The 4:1 Mux $B(y, 2q+2)$ has four inputs namely $Ui(y, 2q+1)$, $Ui(y, 2q+2)$, $Ri(y, 2q+1)$, and M3, and has one output $Bo(y, 2q+2)$.

The output $Fo(x, 2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input $Ri(y, 2q+2)$ of the stage (ring “y”, stage “q”). The output

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Bo(y,2q+2) of the stage (ring “y”, stage “q”) is connected via the wire Hop(1,2) to the input Ui(x,2p+2) of the stage (ring “x”, stage “p”).

The wire Hop(1,1) starting from the output Fo(x,2p+2) of the stage (ring “x”, stage “p”) is also connected to L2 and J2 of the stage (ring “a”, stage “s”), in addition to the input Ri(y,2q+2) of the stage (ring “y”, stage “q”). The stage (ring “x”, stage “p”), the stage (ring “a”, stage “s”), and the stage (ring “y”, stage “q”) may belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Therefore the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “a”, stage “s”) may not be equal to the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “y”, stage “q”). For example the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “a”, stage “s”) may be one where as the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “q”, stage “y”) may be two. Hence the wire Hop(1,1) is a multi-drop hop wire. Also the wire Hop(1,1) is either horizontal external hop wire or vertical external hop wire. Similarly the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “a”, stage “s”) may be any number greater than or equal to one, and also the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “q”, stage “y”) may be any number greater or equal to one.

The wire Hop(1,2) starting from the output Bo(y,2q+2) of the stage (ring “y”, stage “q”) is also connected to K2 and M2 of the stage (ring “a”, stage “s”), in addition to the input Ui(x,2p+2) of the stage (ring “x”, stage “p”). The wire Hop(1,2) is also an example of multi-drop hop wire when the stage (ring “x”, stage “p”), the stage (ring “a”, stage “s”) and the stage (ring “y”, stage “q”) belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

In various embodiments, the inputs J2, K2, L2, and M2 are connected from any of the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Referring to diagram 700A in FIG. 7A, illustrates, in one embodiment, the hop wire connections chart of a partial multi-stage hierarchical network

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$V_{Comb}(N_1, N_2, d, s)$ 100A or a partial multi-stage hierarchical network

$V_{Comb}(N_1, N_2, d, s)$ 100B, or a partial multi-stage hierarchical network

$V_{Comb}(N_1, N_2, d, s)$ 100C, with $m = 6$ and $n = 7$. The hop wire connections chart shows two rings namely ring 1 and ring 2. And there are $m+1 = 7$ stages in ring 1 and $n+1 = 8$ stages in ring 2.

The hop wire connections chart 700A illustrates how the hop wires are connected between any two successive stages of all the rings corresponding to a block of 2D-grid 800. "Lx" denotes an internal hop wire connection, where symbol "L" denotes internal hop wire and "x" is an integer. For example "L1" between the stages (ring 1, stage 0) and (ring 1, stage 1) denotes that the corresponding hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are connected to two successive stages of another ring in the same block or alternatively hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are internal hop wires. Since there is also "L1" between the stages (ring 2, stage 0) and (ring 2, stage 1), there are internal hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected between the stages (ring 1, stage 0) and (ring 1, stage 1) and the stages (ring 2, stage 0) and (ring 2, stage 1). Hence there can be only two "L1" labels in the hop wire connection chart 700A.

Similarly there are two "L2" labels in the hop wire connections chart 700A. Since the label "L2" is given between the stages (ring 1, stage 5) and (ring 1, stage 6) and also the label "L2" is given between the stages (ring 2, stage 3) and (ring 2, stage 4), there are corresponding internal hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected between the stages (ring 1, stage 5) and (ring 1, stage 6) and the stages (ring 2, stage 3) and (ring 2, stage 4).

"Vx" denotes an external vertical hop wire, where symbol "V" denotes vertical external hop wire connections from blocks of the topmost row of 2D-grid 800 (i.e., row of blocks consisting of block (1,1), block (1,2), ..., and block (1,10)) to the same corresponding stages of the same numbered ring of another block that is directly down south, with "x" vertical hop length, where "x" is a positive integer. For example "V1" between the stages (ring 1, stage 1) and (ring 1, stage 2) denote that from block (1,1) of 2D-grid 800 to another block directly below it, which is block (2,1), since "V1" denotes

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 1) and (ring 1, stage 2) of block (1,1) to (ring 1, stage 1) and (ring 1, stage 2) of block (2,1). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 1) and (ring 1, stage 2) of block (3,1) to (ring 1, stage 1) and (ring 1, stage 2) of block (4,1). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 1) and (ring 1, stage 2) of block (9,1) to (ring 1, stage 1) and (ring 1, stage 2) of block (10,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

Similarly “V3” between the stages (ring 2, stage 1) and (ring 2, stage 2) denote that from block (1,1) of 2D-grid 800 to another block below it and at a hop length of 3 which is block (4,1), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 1) and (ring 2, stage 2) of block (1,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (4,1). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 1) and (ring 2, stage 2) of block (2,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (5,1). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 1) and (ring 2, stage 2) of block (7,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (10,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

If there is no block that is directly below a block with hop length equal to 3 then there is no vertical external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (8,1) does not have any block that is directly below and with hop length equal to 3 then none of the vertical external hop wires are connected from (ring 2, stage 1) and (ring 2, stage 2) of block (8,1). Similarly from (ring 2, stage 1) and (ring 2, stage 2) of block (9,1) and from (ring 2, stage 1) and (ring 2, stage 2) of block (10,1), none of the vertical external hop wires are connected. Similarly vertical external hop wires are connected corresponding to “V5”, “V7” etc., labels given in the hop wire connections chart 700A.

“Ux” denotes an external vertical hop wire, where symbol “U” denotes vertical external hop wire connections starting from blocks that are “x” hop length below the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

topmost row of 2D-grid 800 (i.e., row of blocks consisting of block $(1+x,1)$, block $(1+x,2)$, ..., and block $(1+x,10)$) to the same corresponding stages of the same numbered ring of another block that is directly down below, with "x" vertical hop length, where "x" is a positive integer. For example "U1" between the stages (ring 1, stage 2) and (ring 1, stage 3) denote that from block $(2,1)$ of 2D-grid 800 to another block directly below it, which is block $(3,1)$, since "U1" denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 2) and (ring 1, stage 3) of block $(2,1)$ to (ring 1, stage 2) and (ring 1, stage 3) of block $(3,1)$. It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 2) and (ring 1, stage 3) of block $(4,1)$ to (ring 1, stage 2) and (ring 1, stage 3) of block $(5,1)$. This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 2) and (ring 1, stage 3) of block $(8,1)$ to (ring 1, stage 2) and (ring 1, stage 3) of block $(9,1)$. The same pattern continues for all the columns starting from the block in the topmost row of each column.

If there is no block that is directly below a block with hop length equal to 1 then no vertical external hop wire connections is given corresponding to those two successive stages of the blocks. For example block $(10,1)$ does not have any block that is directly below and with hop length equal to 1 then none of the vertical external hop wires are connected from (ring 1, stage 2) and (ring 1, stage 3) of block $(10,1)$. Similarly for all the blocks in each column from the topmost row up to the row "x", no vertical external hop wires are connected to the corresponding (ring 1, stage 2) and (ring 1, stage 3).

Similarly "U3" between the stages (ring 2, stage 2) and (ring 2, stage 3) denote that starting from blocks that are 3 hop length below the topmost row of 2D-grid 800 (i.e., row of blocks consisting of block $(4,1)$, block $(4,2)$, ..., and block $(4,10)$) to the same corresponding stages of the same numbered ring of another block that is directly down below, with vertical hop length of 3, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected. For example from block $(4,1)$ of 2D-grid 800 to another block below it and at a hop length of 3 which is block $(7,1)$, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 2) and (ring 2, stage 3) of block $(4,1)$ to (ring 2, stage 1) and (ring 2, stage 2) of

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

block (7,1). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 2) and (ring 2, stage 3) of block (5,1) to (ring 2, stage 2) and (ring 2, stage 3) of block (8,1). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 2) and (ring 2, stage 3) of block (7,1) to (ring 2, stage 2) and (ring 2, stage 3) of block (10,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

If there is no block that is directly below a block with hop length equal to 3 then no vertical external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (8,1) does not have any block that is directly below and with hop length equal to 3 then none of the vertical external hop wires are connected from (ring 2, stage 2) and (ring 2, stage 3) of block (8,1). Similarly from (ring 2, stage 2) and (ring 2, stage 3) of block (9,1) and from (ring 2, stage 2) and (ring 2, stage 3) of block (10,1), none of the vertical external hop wires are connected. Similarly vertical external hop wires are connected corresponding to "U5", "U7" etc. labels given in the hop wire connections chart 700A.

"Hx" denotes an external horizontal hop wire, where symbol "H" denotes horizontal external hop wire connections from blocks of the leftmost column of 2D-grid 800 (i.e., column of blocks consisting of block (1,1), block (2,1), ..., and block (10,1)) to the same corresponding stages of the same numbered ring of another block that is directly to the right, with "x" horizontal hop length, where "x" is a positive integer. For example "H1" between the stages (ring 1, stage 3) and (ring 1, stage 4) denote that from block (1,1) of 2D-grid 800 to another block directly to the right, which is block (1,2), since "H1" denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 3) and (ring 1, stage 4) of block (1,1) to (ring 1, stage 3) and (ring 1, stage 4) of block (1,2). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 3) and (ring 1, stage 4) of block (1,3) to (ring 1, stage 3) and (ring 1, stage 4) of block (1,4). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 3) and (ring 1, stage 4) of

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

block (9,1) to (ring 1, stage 3) and (ring 1, stage 4) of block (10,1). The same pattern continues for all the rows starting from the block in the leftmost block of each row.

Similarly “H3” between the stages (ring 2, stage 4) and (ring 2, stage 5) denote that from block (1,1) of 2D-grid 800 to another block to the right and at a hop length of 3
 5 which is block (1,4), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 4) and (ring 2, stage 5) of block (1,1) to (ring 2, stage 4) and (ring 2, stage 5) of block (1,4). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 4) and (ring 2, stage 5) of block (1,2) to (ring 2, stage 4) and (ring 2, stage 5) of block (1,5). This
 10 pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 4) and (ring 2, stage 5) of block (1,7) to (ring 2, stage 4) and (ring 2, stage 5) of block (1,10). The same pattern continues for all the columns starting from the block in the leftmost column of each row.

If there is no block that is directly to the right with hop length equal to 3 then
 15 there is no horizontal external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (1,8) does not have any block that is directly to the right and with hop length equal to 3 then none of the horizontal external hop wires are connected from (ring 2, stage 4) and (ring 2, stage 5) of block (1,8). Similarly from (ring 2, stage 4) and (ring 2, stage 5) of block (1,9) and from (ring 2, stage
 20 4) and (ring 2, stage 5) of block (1,10), none of the horizontal external hop wires are connected. Similarly horizontal external hop wires are connected corresponding to “H5”, “H7” etc., labels given in the hop wire connections chart 700A.

“Kx” denotes an external horizontal hop wire, where symbol “K” denotes horizontal external hop wire connections starting from blocks that are “x” hop length
 25 below the leftmost column of 2D-grid 800 (i.e., column of blocks consisting of block (1, 1+x), block (2, 1+x), ..., and block (10, 1+x)) to the same corresponding stages of the same numbered ring of another block that is directly to the right, with “x” horizontal hop length, where “x” is a positive integer. For example “K1” between the stages (ring 1, stage 4) and (ring 1, stage 5) denote that from block (1,2) of 2D-grid 800 to another block
 30 directly to the right, which is block (1,3), since “K1” denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1,

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

stage 4) and (ring 1, stage 5) of block (1,2) to (ring 1, stage 4) and (ring 1, stage 5) of block (1,3). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 4) and (ring 1, stage 4) of block (1,4) to (ring 1, stage 4) and (ring 1, stage 5) of block (1,5). This pattern continues and finally there are
 5 external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 4) and (ring 1, stage 5) of block (1,8) to (ring 1, stage 4) and (ring 1, stage 5) of block (1,9). The same pattern continues for all the rows starting from the block in the leftmost column of each row.

If there is no block that is directly to the right of a block with hop length equal to
 10 1 then no horizontal external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (1,10) does not have any block that is directly to the right and with hop length equal to 1 then none of the horizontal external hop wires are connected from (ring 1, stage 4) and (ring 1, stage 5) of block (1,10). Similarly for all the blocks in each row from the leftmost column up to the column "x",
 15 no horizontal external hop wires are connected to the corresponding (ring 1, stage 4) and (ring 1, stage 5).

Similarly "K3" between the stages (ring 2, stage 5) and (ring 2, stage 6) denote that starting from blocks that are 3 hop length to the right of the leftmost column of 2D-grid 800 (i.e., column of blocks consisting of block (1,4), block (2,4), ..., and block
 20 (10,4)) to the same corresponding stages of the same numbered ring of another block that is directly to the right, with horizontal hop length of 3, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected. For example from block (1,4) of 2D-grid 800 to another block to the right and at a hop length of 3 which is block (1,7), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and
 25 Hop(2,2) from (ring 2, stage 5) and (ring 2, stage 6) of block (1,4) to (ring 2, stage 5) and (ring 2, stage 6) of block (1,7). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 5) and (ring 2, stage 6) of block (1,5) to (ring 2, stage 5) and (ring 2, stage 6) of block (1,8). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and
 30 Hop(2,2) from (ring 2, stage 5) and (ring 2, stage 6) of block (1,7) to (ring 2, stage 5) and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

(ring 2, stage 6) of block (1,10). The same pattern continues for all the rows starting from the block in the leftmost block of each row.

If there is no block that is directly to the right of a block with hop length equal to 3 then no horizontal external hop wire connections is given corresponding to those two
 5 successive stages of the blocks. For example block (1,8) does not have any block that is directly to the right and with hop length equal to 3 then none of the horizontal external hop wires are connected from (ring 2, stage 5) and (ring 2, stage 6) of block (1,8). Similarly from (ring 2, stage 5) and (ring 2, stage 6) of block (1,9) and from (ring 2, stage 5) and (ring 2, stage 6) of block (1,10), none of the horizontal external hop wires are
 10 connected. Similarly horizontal external hop wires are connected corresponding to “K5”, “K7” etc. labels given in the hop wire connections chart 700A.

In general the hop length of an external vertical hop wire can be any positive number. Similarly the hop length of an external horizontal hop wire can be any positive number. The hop wire connections between two arbitrary successive stages in two
 15 different rings of the same block or two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, and 300E of FIG. 3E. Similarly the multi-drop hop wire connections between two arbitrary successive stages in two different rings of different blocks described in diagram 700A of FIG. 7A
 20 may be any one of the embodiments of either the diagrams 500A of FIG. 5A.

In accordance with the invention, the hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may also be any one of the embodiments of either the diagrams 400A of FIG. 4A and 400B of FIG. 4B. Similarly the multi-drop hop wire connections between two arbitrary
 25 stages in two different rings of different blocks may also be any one of the embodiments of either the diagrams 600A of FIG. 6A or 600B of FIG. 6B.

In accordance with the current invention, either partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A of FIG. 1A or partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B of FIG. 1B, or partial multi-stage hierarchical network
 30 $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C, corresponding to a block of 2D-grid of blocks 800

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

of FIG. 8, using any one of the embodiments of 200A-200E of FIGs. 2A-2E to implement a stage of a ring of the multi-stage hierarchical network, either by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, 300E of FIG. 3E, 500A of FIG. 5A, or by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may be any one of the embodiments of either the diagrams 400A of FIG. 4A, 400B of FIG. 4B, 600A of FIG. 6A, or 600B of FIG. 6B is very efficient in the reduction of the die size, power consumption, and for lower wire/path delay for higher performance for practical routing applications to particularly to set up broadcast, unicast and multicast connections. In general in accordance with the current invention, where N_1 and N_2 of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ may be arbitrarily large in size and also the 2D-grid size 800 may also be arbitrarily large in size in terms of both the number of rows and number of columns.

Delay Optimizations in Multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$:

The multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ according to the current invention can further be optimized to reduce the delay in the routed path of the connection. The delay optimized multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ is hereinafter denoted by $V_{D-Comb}(N_1, N_2, d, s)$. The delay optimizing embodiments of the stages of a ring are one of the diagrams namely 900A-900E of FIGs. 9A-9D, 1000A-1000F of FIGs. 10A-10F, and 1100A-1100C of FIGs. 11A-11C. The diagram 1200 of FIG. 12, 1300 of FIG. 13, 1400 of FIG. 14, and 1500 of FIG. 15 are different embodiments for the implementation of delay optimizations with all the connections between two arbitrary successive stages in two different rings of the same block or two different rings of different blocks of 2D-grid 800.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

FIG. 9A illustrates a stage (ring “k”, stage “m”) 900A consists of 5 inputs namely $F_i(k,2m+1)$, $F_i(k,2m+2)$, $YF_i(k,2m+1)$, $U_i(k,2m+1)$, and $U_i(k,2m+2)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of seven 2:1 Muxes namely $YF(k,2m+1)$, $F(k,2m+1)$, $F(k,2m+2)$, $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The 2:1 Mux $YF(k,2m+1)$ has two inputs namely $F_i(k,2m+1)$ and $YF_i(k,2m+1)$ and has one output $YF_o(k,2m+1)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $YF_o(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $YF_o(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 2:1 Mux $U(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

FIG. 9B illustrates a stage (ring “k”, stage “m”) 900B consists of 5 inputs namely $F_i(k,2m+1)$, $F_i(k,2m+2)$, $YU_i(k,2m+1)$, $U_i(k,2m+1)$, and $U_i(k,2m+2)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of seven 2:1 Muxes namely $F(k,2m+1)$, $F(k,2m+2)$, $YF(k,2m+1)$, $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 2:1 Mux $YU(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $YU_i(k,2m+1)$ and has one output $YU_o(k,2m+1)$. The 2:1 Mux $U(k,2m+1)$ has two inputs namely $YU_o(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

FIG. 9C illustrates a stage (ring “k”, stage “m”) 900C consists of 5 inputs namely $F_i(k,2m+1)$, $F_i(k,2m+2)$, $UY_i(k,2m+1)$, $U_i(k,2m+1)$, and $U_i(k,2m+2)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of five 2:1 Muxes namely $F(k,2m+1)$, $F(k,2m+2)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of one 3:1 Mux namely $UY(k,2m+1)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 3:1 Mux $UY(k,2m+1)$ has three inputs namely $U_i(k,2m+1)$, $UY_i(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $UY_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $UY_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $UY_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

FIG. 9D illustrates a stage (ring “k”, stage “m”) 900D consists of 6 inputs namely $F_i(k,2m+1)$, $F_i(k,2m+2)$, $YF_i(k,2m+1)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $YU_i(k,2m+1)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of eight 2:1 Muxes namely $F(k,2m+1)$, $F(k,2m+2)$, $YF(k,2m+1)$, $U(k,2m+1)$, $U(k,2m+2)$, $YU(k,2m+1)$, $B(k,2m+1)$, and $B(k,2m+2)$. The 2:1 Mux $YF(k,2m+1)$ has two inputs namely $F_i(k,2m+1)$ and $YF_i(k,2m+1)$ and has one output $YF_o(k,2m+1)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $YF_o(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $YF_o(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 2:1 Mux $YU(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $YU_i(k,2m+1)$ and has one output $YU_o(k,2m+1)$. The 2:1 Mux $U(k,2m+1)$ has two inputs namely $YU_o(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

FIG. 9E illustrates a stage (ring “k”, stage “m”) 900E consists of 6 inputs namely $F_i(k,2m+1)$, $F_i(k,2m+2)$, $YF_i(k,2m+1)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $UY_i(k,2m+1)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of six 2:1 Muxes namely $F(k,2m+1)$, $F(k,2m+2)$, $YF(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of one 3:1 Mux namely $UY(k,2m+1)$. The 2:1 Mux $YF(k,2m+1)$ has two inputs namely $F_i(k,2m+1)$ and $YF_i(k,2m+1)$ and has one output $YF_o(k,2m+1)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $YF_o(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $YF_o(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 3:1 Mux $UY(k,2m+1)$ has three inputs namely $U_i(k,2m+1)$, $UY_i(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $UY_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $UY_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $UY_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

FIG. 10A illustrates a stage (ring “k”, stage “m”) 1000A consists of 5 inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $YR_i(k,2m+1)$, $U_i(k,2m+1)$, and $U_i(k,2m+2)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of nine 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $YR(k,2m+1)$, $F(k,2m+1)$, $F(k,2m+2)$, $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The 2:1 Mux $YR(k,2m+1)$ has two inputs namely $R_i(k,2m+1)$ and $YR_i(k,2m+1)$ and has one output $YR_o(k,2m+1)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $YR_o(k,2m+1)$ and $B_o(k,2m+1)$ and has one output $R_o(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and $B_o(k,2m+2)$ and has one output $R_o(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $R_o(k,2m+1)$ and $R_o(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $R_o(k,2m+1)$ and $R_o(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 2:1 Mux $U(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

FIG. 10B illustrates a stage (ring “k”, stage “m”) 1000B consists of 5 inputs
 5 namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $RY_i(k,2m+1)$, $U_i(k,2m+1)$, and $U_i(k,2m+2)$; and 4
 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring “k”,
 stage “m”) also consists of seven 2:1 Muxes namely $R(k,2m+2)$, $F(k,2m+1)$, $F(k,2m+2)$,
 $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The stage (ring “k”, stage “m”) also
 consists of one 3:1 Mux namely $RY(k,2m+1)$. The 3:1 Mux $RY(k,2m+1)$ has three inputs
 10 namely $R_i(k,2m+1)$, $RY_i(k,2m+1)$, and $B_o(k,2m+1)$, and has one output $RY_o(k,2m+1)$.
 The 2:1 Mux $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and $B_o(k,2m+2)$ and has one
 output $Ro(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $RY_o(k,2m+1)$ and
 $Ro(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs
 namely $RY_o(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $F_o(k,2m+2)$.

15 The 2:1 Mux $U(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $F_o(k,2m+1)$ and
 has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$
 and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs
 namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux
 $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output
 20 $B_o(k,2m+2)$.

FIG. 10C illustrates a stage (ring “k”, stage “m”) 1000C consists of 5 inputs
 namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $YU_i(k,2m+1)$; and 4
 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring “k”,
 stage “m”) also consists of nine 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$,
 25 $F(k,2m+2)$, $YU(k,2m+1)$, $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The 2:1
 Mux $R(k,2m+1)$ has two inputs namely $R_i(k,2m+1)$ and $B_o(k,2m+1)$ and has one output
 $Ro(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and
 $B_o(k,2m+2)$ and has one output $Ro(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs
 namely $Ro(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux
 30 $F(k,2m+2)$ has two inputs namely $Ro(k,2m+1)$ and $Ro(k,2m+2)$ and has one output
 $F_o(k,2m+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux $YU(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $YU_i(k,2m+1)$ and has one output $YU_o(k,2m+1)$. The 2:1 Mux $U(k,2m+1)$ has two inputs namely $YU_o(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

FIG. 10D illustrates a stage (ring "k", stage "m") 1000D consists of 5 inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $UY_i(k,2m+1)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring "k", stage "m") also consists of seven 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$, $F(k,2m+2)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The stage (ring "k", stage "m") also consists of one 3:1 Mux namely $UY(k,2m+1)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $R_i(k,2m+1)$ and $B_o(k,2m+1)$ and has one output $R_o(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and $B_o(k,2m+2)$ and has one output $R_o(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $R_o(k,2m+1)$ and $R_o(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $R_o(k,2m+1)$ and $R_o(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 3:1 Mux $UY(k,2m+1)$ has three inputs namely $U_i(k,2m+1)$, $UY_i(k,2m+1)$, and $F_o(k,2m+1)$, and has one output $UY_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $UY_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $UY_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

FIG. 10E illustrates a stage (ring "k", stage "m") 1000E consists of 6 inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $YR_i(k,2m+1)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $YU_i(k,2m+1)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring "k", stage "m") also consists of ten 2:1 Muxes namely $YR(k,2m+1)$, $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$, $F(k,2m+2)$, $YU(k,2m+1)$, $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The 2:1 Mux $YR(k,2m+1)$ has two inputs namely $R_i(k,2m+1)$ and $YR_i(k,2m+1)$ and has one output $YR_o(k,2m+1)$. The 2:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

R(k,2m+1) has two inputs namely YRo(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux
 5 F(k,2m+2) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux YU(k,2m+1) has two inputs namely Ui(k,2m+1) and YUi(k,2m+1) and has one output YUo(k,2m+1). The 2:1 Mux U(k,2m+1) has two inputs namely YUo(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2)
 10 has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 10F illustrates a stage (ring "k", stage "m") 1000F consists of 6 inputs
 15 namely Ri(k,2m+1), Ri(k,2m+2), RYi(k,2m+1), Ui(k,2m+1), Ui(k,2m+2), and YUi(k,2m+1); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of six 2:1 Muxes namely R(k,2m+2), F(k,2m+1), F(k,2m+2), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The stage (ring "k", stage "m") also consists of two 3:1 Mux namely RY(k,2m+1) and UY(k,2m+1). The 3:1
 20 Mux RY(k,2m+1) has three inputs namely Ri(k,2m+1), RYi(k,2m+1), and Bo(k,2m+1) and has one output RYo(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely RYo(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely RYo(k,2m+1) and Ro(k,2m+2) and has
 25 one output Fo(k,2m+2).

The 3:1 Mux UY(k,2m+1) has three inputs namely Ui(k,2m+1), YUi(k,2m+1), and Fo(k,2m+1), and has one output UYo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one
 30 output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

FIG. 11A illustrates a stage (ring “k”, stage “m”) 1100A consists of 5 inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $FY_i(k,2m+2)$, $U_i(k,2m+1)$, and $U_i(k,2m+2)$; and 4 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of seven 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$, $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of one 3:1 Mux namely $FY(k,2m+2)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $R_i(k,2m+1)$ and $Bo(k,2m+1)$ and has one output $Ro(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and $Bo(k,2m+2)$ and has one output $Ro(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $Ro(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+1)$. The 3:1 Mux $FY(k,2m+2)$ has three inputs namely $Ro(k,2m+1)$, $Ro(k,2m+2)$, and $FY_i(k,2m+2)$, and has one output $FY_o(k,2m+2)$.

The 2:1 Mux $U(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $Fo(k,2m+1)$ and has one output $Uo(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $FY_o(k,2m+2)$ and has one output $Uo(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $Uo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output $Bo(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $Uo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output $Bo(k,2m+2)$.

FIG. 11B illustrates a stage (ring “k”, stage “m”) 1100B consists of 5 inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $BY_i(k,2m+2)$; and 4 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of seven 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$, $F(k,2m+2)$, $U(k,2m+1)$, $U(k,2m+2)$, and $B(k,2m+1)$. The stage (ring “k”, stage “m”) also consists of one 3:1 Mux namely $BY(k,2m+2)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $R_i(k,2m+1)$ and $Bo(k,2m+1)$ and has one output $Ro(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and $Bo(k,2m+2)$ and has one output $Ro(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $Ro(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $Ro(k,2m+1)$, and $Ro(k,2m+2)$, and has one output $Fo(k,2m+2)$.

The 2:1 Mux $U(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $Fo(k,2m+1)$ and has one output $Uo(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $Fo(k,2m+2)$ and has one output $Uo(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 3:1 Mux $BY(k,2m+2)$ has three inputs namely $U_o(k,2m+1)$, $U_o(k,2m+2)$, and $BY_i(k,2m+2)$, and has one output $BY_o(k,2m+2)$.

FIG. 11C illustrates a stage (ring “k”, stage “m”) 1100C consists of 6 inputs
 5 namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $FY_i(k,2m+2)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $BY_i(k,2m+2)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$.
 The stage (ring “k”, stage “m”) also consists of six 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$, $U(k,2m+1)$, $U(k,2m+2)$, and $B(k,2m+1)$. The stage (ring “k”,
 stage “m”) also consists of two 3:1 Muxes namely $FY(k,2m+2)$ and $BY(k,2m+2)$. The 2:1
 10 Mux $R(k,2m+1)$ has two inputs namely $R_i(k,2m+1)$ and $B_o(k,2m+1)$ and has one output $R_o(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and $B_o(k,2m+2)$ and has one output $R_o(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs
 namely $R_o(k,2m+1)$ and $R_o(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 3:1 Mux
 $FY(k,2m+2)$ has three inputs namely $R_o(k,2m+1)$, $R_o(k,2m+2)$, and $FY_i(k,2m+2)$, and
 15 has one output $FY_o(k,2m+2)$.

The 2:1 Mux $U(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $F_o(k,2m+1)$ and
 has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$
 and $FY_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two
 inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 3:1
 20 Mux $BY(k,2m+2)$ has three inputs namely $U_o(k,2m+1)$, $U_o(k,2m+2)$, and $BY_i(k,2m+2)$
 and has one output $BY_o(k,2m+2)$.

Referring to diagram 1200 in FIG. 12, illustrates all the connections between two
 arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”,
 stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages
 25 (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical
 network $V_{D-Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 5 inputs namely $R_i(x,2p+1)$,
 $R_i(x,2p+2)$, $U_i(x,2p+1)$, $U_i(x,2p+2)$, and $UY_i(x,2p+1)$; and 4 outputs $B_o(x,2p+1)$,
 $B_o(x,2p+2)$, $F_o(x,2p+1)$, and $F_o(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of
 30 seven 2:1 Muxes namely $R(x,2p+1)$, $R(x,2p+2)$, $F(x,2p+1)$, $F(x,2p+2)$, $U(x,2p+1)$,

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$B(x,2p+1)$, and $B(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of one 3:1 Mux namely $UY(x,2p+1)$. The 2:1 Mux $R(x,2p+1)$ has two inputs namely $Ri(x,2p+1)$ and $Bo(x,2p+1)$ and has one output $Ro(x,2p+1)$. The 2:1 Mux $R(x,2p+2)$ has two inputs namely $Ri(x,2p+2)$ and $Bo(x,2p+2)$ and has one output $Ro(x,2p+2)$. The 2:1 Mux

5 $F(x,2p+1)$ has two inputs namely $Ro(x,2p+1)$ and $Ro(x,2p+2)$ and has one output $Fo(x,2p+1)$. The 2:1 Mux $F(x,2p+2)$ has two inputs namely $Ro(x,2p+1)$ and $Ro(x,2p+2)$ and has one output $Fo(x,2p+2)$.

The 3:1 Mux $UY(x,2p+1)$ has three inputs namely $Ui(x,2p+1)$, $UYi(x,2p+1)$, and $Fo(x,2p+1)$, and has one output $UYo(x,2p+1)$. The 2:1 Mux $U(x,2p+2)$ has two inputs

10 namely $Ui(x,2p+2)$ and $Fo(x,2p+2)$ and has one output $Uo(x,2p+2)$. The 2:1 Mux $B(x,2p+1)$ has two inputs namely $UYo(x,2p+1)$ and $Uo(x,2p+2)$ and has one output $Bo(x,2p+1)$. The 2:1 Mux $B(x,2p+2)$ has two inputs namely $UYo(x,2p+1)$ and $Uo(x,2p+2)$ and has one output $Bo(x,2p+2)$.

The stage (ring “x”, stage “p+1”) consists of 5 inputs namely $Ri(x,2p+3)$,

15 $Ri(x,2p+4)$, $RYi(x,2p+3)$, $Ui(x,2p+3)$, and $Ui(x,2p+4)$; and 4 outputs $Bo(x,2p+3)$, $Bo(x,2p+4)$, $Fo(x,2p+3)$, and $Fo(x,2p+4)$. The stage (ring “x”, stage “p+1”) also consists of seven 2:1 Muxes namely $R(x,2p+4)$, $F(x,2p+3)$, $F(x,2p+4)$, $U(x,2p+3)$, $U(x,2p+4)$, $B(x,2p+3)$, and $B(x,2p+4)$. The stage (ring “x”, stage “p+1”) also consists of one 3:1 Mux namely $RY(x,2p+3)$. The 3:1 Mux $RY(x,2p+3)$ has three inputs namely $Ri(x,2p+3)$,

20 $RYi(x,2p+3)$, and $Bo(x,2p+3)$, and has one output $RYo(x,2p+3)$. The 2:1 Mux $R(x,2p+4)$ has two inputs namely $Ri(x,2p+4)$ and $Bo(x,2p+4)$ and has one output $Ro(x,2p+4)$. The 2:1 Mux $F(x,2p+3)$ has two inputs namely $RYo(x,2p+3)$ and $Ro(x,2p+4)$ and has one output $Fo(x,2p+3)$. The 2:1 Mux $F(x,2p+4)$ has two inputs namely $RYo(x,2p+3)$ and $Ro(x,2p+4)$ and has one output $Fo(x,2p+4)$.

25 The 2:1 Mux $U(x,2p+3)$ has two inputs namely $Ui(x,2p+3)$ and $Fo(x,2p+3)$ and has one output $Uo(x,2p+3)$. The 2:1 Mux $U(x,2p+4)$ has two inputs namely $Ui(x,2p+4)$ and $Fo(x,2p+4)$ and has one output $Uo(x,2p+4)$. The 2:1 Mux $B(x,2p+3)$ has two inputs namely $Uo(x,2p+3)$ and $Uo(x,2p+4)$ and has one output $Bo(x,2p+3)$. The 2:1 Mux $B(x,2p+4)$ has two inputs namely $Uo(x,2p+3)$ and $Uo(x,2p+4)$ and has one output

30 $Bo(x,2p+4)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The output $Fo(x,2p+1)$ of the stage (ring “x”, stage “p”) is connected to the input $Ri(x,2p+3)$ of the stage (ring “x”, stage “p+1”). And the output $Bo(x,2p+3)$ of the stage (ring “x”, stage “p+1”) is connected to the input $Ui(x,2p+1)$ of the stage (ring “x”, stage “p”).

5 The stage (ring “y”, stage “q”) consists of 5 inputs namely $Ri(y,2q+1)$, $Ri(y,2q+2)$, $Ui(y,2q+1)$, $Ui(y,2q+2)$, and $YUi(y,2q+1)$; and 4 outputs $Bo(y,2q+1)$, $Bo(y,2q+2)$, $Fo(y,2q+1)$, and $Fo(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of nine 2:1 Muxes namely $R(y,2q+1)$, $R(y,2q+2)$, $F(y,2q+1)$, $F(y,2q+2)$, $YU(y,2q+1)$, $U(y,2q+1)$, $U(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The 2:1 Mux $R(y,2q+1)$ has two inputs
10 namely $Ri(y,2q+1)$ and $Bo(y,2q+1)$ and has one output $Ro(y,2q+1)$. The 2:1 Mux $R(y,2q+2)$ has two inputs namely $Ri(y,2q+2)$ and $Bo(y,2q+2)$ and has one output $Ro(y,2q+2)$. The 2:1 Mux $F(y,2q+1)$ has two inputs namely $Ro(y,2q+1)$ and $Ro(y,2q+2)$ and has one output $Fo(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $Ro(y,2q+1)$ and $Ro(y,2q+2)$ and has one output $Fo(y,2q+2)$.

15 The 2:1 Mux $YU(y,2q+1)$ has two inputs namely $Ui(y,2q+1)$ and $YUi(y,2q+1)$ and has one output $YUo(y,2q+1)$. The 2:1 Mux $U(y,2q+1)$ has two inputs namely $YUo(y,2q+1)$ and $Fo(y,2q+1)$ and has one output $Uo(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $Ui(y,2q+2)$ and $Fo(y,2q+2)$ and has one output $Uo(y,2q+2)$. The 2:1 Mux $B(y,2q+1)$ has two inputs namely $Uo(y,2q+1)$ and $Uo(y,2q+2)$ and has one
20 output $Bo(y,2q+1)$. The 2:1 Mux $B(y,2q+2)$ has two inputs namely $Uo(y,2q+1)$ and $Uo(y,2q+2)$ and has one output $Bo(y,2q+2)$.

 The stage (ring “y”, stage “q+1”) consists of 5 inputs namely $Ri(y,2q+3)$, $Ri(y,2q+4)$, $YRi(y,2q+3)$, $Ui(y,2q+3)$, and $Ui(y,2q+4)$; and 4 outputs $Bo(y,2q+3)$, $Bo(y,2q+4)$, $Fo(y,2q+3)$, and $Fo(y,2q+4)$. The stage (ring “y”, stage “q+1”) also consists
25 of nine 2:1 Muxes namely $R(y,2q+3)$, $R(y,2q+4)$, $YR(y,2q+3)$, $F(y,2q+3)$, $F(y,2q+4)$, $U(y,2q+3)$, $U(y,2q+4)$, $B(y,2q+3)$, and $B(y,2q+4)$. The 2:1 Mux $YR(y,2q+3)$ has two inputs namely $Ri(y,2q+3)$ and $YRi(y,2q+3)$ and has one output $YRo(y,2q+3)$. The 2:1 Mux $R(y,2q+3)$ has two inputs namely $YRo(y,2q+3)$ and $Bo(y,2q+3)$ and has one output $Ro(y,2q+3)$. The 2:1 Mux $R(y,2q+4)$ has two inputs namely $Ri(y,2q+4)$ and $Bo(y,2q+4)$
30 and has one output $Ro(y,2q+4)$. The 2:1 Mux $F(y,2q+3)$ has two inputs namely

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Ro(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Ro(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Ri(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to two inputs namely input Ri(y,2q+4) of the stage (ring "y", stage "q+1") and input YUi(y,2q+1) of the stage (ring "y", stage "q"). The output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to two inputs namely input Ui(y,2q+2) of the stage (ring "y", stage "q") and input YRi(y,2q+3) of the stage (ring "y", stage "q+1").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to two inputs namely input Ri(x,2p+4) of the stage (ring "x", stage "p+1") and input UYi(x,2p+1) of the stage (ring "x", stage "p"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to two inputs namely input Ui(x,2p+2) of the stage (ring "x", stage "p") and input RYi(x,2p+3) of the stage (ring "x", stage "p+1").

Referring to diagram 1300 in FIG. 13, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The stage (ring “x”, stage “p”) consists of 6 inputs namely $F_i(x,2p+1)$, $F_i(x,2p+2)$, $YF_i(x,2p+1)$, $U_i(x,2p+1)$, $U_i(x,2p+2)$, and $YU_i(x,2p+1)$; and 4 outputs $B_o(x,2p+1)$, $B_o(x,2p+2)$, $F_o(x,2p+1)$, and $F_o(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely $F(x,2p+1)$, $F(x,2p+2)$, $YF(x,2p+1)$, $U(x,2p+1)$, $U(x,2p+2)$, $YU(x,2p+1)$, $B(x,2p+1)$, and $B(x,2p+2)$. The 2:1 Mux $YF(x,2p+1)$ has two inputs namely $F_i(x,2p+1)$ and $YF_i(x,2p+1)$ and has one output $YF_o(x,2p+1)$. The 2:1 Mux $F(x,2p+1)$ has two inputs namely $YF_o(x,2p+1)$ and $F_i(x,2p+2)$ and has one output $F_o(x,2p+1)$. The 2:1 Mux $F(x,2p+2)$ has two inputs namely $YF_o(x,2p+1)$ and $F_i(x,2p+2)$ and has one output $F_o(x,2p+2)$.

10 The 2:1 Mux $YU(x,2p+1)$ has two inputs namely $U_i(x,2p+1)$ and $YU_i(x,2p+1)$ and has one output $YU_o(x,2p+1)$. The 2:1 Mux $U(x,2p+1)$ has two inputs namely $YU_o(x,2p+1)$ and $F_o(x,2p+1)$ and has one output $U_o(x,2p+1)$. The 2:1 Mux $U(x,2p+2)$ has two inputs namely $U_i(x,2p+2)$ and $F_o(x,2p+2)$ and has one output $U_o(x,2p+2)$. The 2:1 Mux $B(x,2p+1)$ has two inputs namely $U_o(x,2p+1)$ and $U_o(x,2p+2)$ and has one output $B_o(x,2p+1)$. The 2:1 Mux $B(x,2p+2)$ has two inputs namely $U_o(x,2p+1)$ and $U_o(x,2p+2)$ and has one output $B_o(x,2p+2)$.

The stage (ring “x”, stage “p+1”) consists of 6 inputs namely $R_i(x,2p+3)$, $R_i(x,2p+4)$, $YR_i(x,2p+3)$, $U_i(x,2p+3)$, $U_i(x,2p+4)$, and $YU_i(x,2p+3)$; and 4 outputs $B_o(x,2p+3)$, $B_o(x,2p+4)$, $F_o(x,2p+3)$, and $F_o(x,2p+4)$. The stage (ring “x”, stage “p+1”) also consists of ten 2:1 Muxes namely $YR(x,2p+3)$, $R(x,2p+3)$, $R(x,2p+4)$, $F(x,2p+3)$, $F(x,2p+4)$, $YU(x,2p+3)$, $U(x,2p+3)$, $U(x,2p+4)$, $B(x,2p+3)$, and $B(x,2p+4)$. The 2:1 Mux $YR(x,2p+3)$ has two inputs namely $R_i(x,2p+3)$ and $YR_i(x,2p+3)$ and has one output $YR_o(x,2p+3)$. The 2:1 Mux $R(x,2p+3)$ has two inputs namely $YR_o(x,2p+3)$ and $B_o(x,2p+3)$ and has one output $R_o(x,2p+3)$. The 2:1 Mux $R(x,2p+4)$ has two inputs namely $R_i(x,2p+4)$ and $B_o(x,2p+4)$ and has one output $R_o(x,2p+4)$. The 2:1 Mux $F(x,2p+3)$ has two inputs namely $R_o(x,2p+3)$ and $R_o(x,2p+4)$ and has one output $F_o(x,2p+3)$. The 2:1 Mux $F(x,2p+4)$ has two inputs namely $R_o(x,2p+3)$ and $R_o(x,2p+4)$ and has one output $F_o(x,2p+4)$.

25 The 2:1 Mux $YU(x,2p+3)$ has two inputs namely $U_i(x,2p+3)$ and $YU_i(x,2p+3)$ and has one output $YU_o(x,2p+3)$. The 2:1 Mux $U(x,2p+3)$ has two inputs namely $YU_o(x,2p+3)$ and $F_o(x,2p+3)$ and has one output $U_o(x,2p+3)$. The 2:1 Mux $U(x,2p+4)$

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

has two inputs namely $U_{i(x,2p+4)}$ and $F_{o(x,2p+4)}$ and has one output $U_{o(x,2p+4)}$. The 2:1 Mux $B_{(x,2p+3)}$ has two inputs namely $U_{o(x,2p+3)}$ and $U_{o(x,2p+4)}$ and has one output $B_{o(x,2p+3)}$. The 2:1 Mux $B_{(x,2p+4)}$ has two inputs namely $U_{o(x,2p+3)}$ and $U_{o(x,2p+4)}$ and has one output $B_{o(x,2p+4)}$.

5 The output $F_{o(x,2p+1)}$ of the stage (ring "x", stage "p") is connected to the input $R_{i(x,2p+3)}$ of the stage (ring "x", stage "p+1"). And the output $B_{o(x,2p+3)}$ of the stage (ring "x", stage "p+1") is connected to the input $U_{i(x,2p+1)}$ of the stage (ring "x", stage "p").

 The stage (ring "y", stage "q") consists of 6 inputs namely $F_{i(y,2q+1)}$, $F_{i(y,2q+2)}$, $YF_{i(y,2q+1)}$, $U_{i(y,2q+1)}$, $U_{i(y,2q+2)}$, and $UY_{i(y,2q+1)}$; and 4 outputs $B_{o(y,2q+1)}$, $B_{o(y,2q+2)}$, $F_{o(y,2q+1)}$, and $F_{o(y,2q+2)}$. The stage (ring "y", stage "q") also consists of six 2:1 Muxes namely $F_{(y,2q+1)}$, $F_{(y,2q+2)}$, $YF_{(y,2q+1)}$, $U_{(y,2q+2)}$, $B_{(y,2q+1)}$, and $B_{(y,2q+2)}$. The stage (ring "y", stage "q") also consists of one 3:1 Mux namely $UY_{(y,2q+1)}$. The 2:1 Mux $YF_{(y,2q+1)}$ has two inputs namely $F_{i(y,2q+1)}$ and $YF_{i(y,2q+1)}$ and has one output $YF_{o(y,2q+1)}$. The 2:1 Mux $F_{(y,2q+1)}$ has two inputs namely $YF_{o(y,2q+1)}$ and $F_{i(y,2q+2)}$ and has one output $F_{o(y,2q+1)}$. The 2:1 Mux $F_{(y,2q+2)}$ has two inputs namely $YF_{o(y,2q+1)}$ and $F_{i(y,2q+2)}$ and has one output $F_{o(y,2q+2)}$.

 The 3:1 Mux $UY_{(y,2q+1)}$ has three inputs namely $U_{i(y,2q+1)}$, $UY_{i(y,2q+1)}$ and $F_{o(y,2q+1)}$ and has one output $UY_{o(y,2q+1)}$. The 2:1 Mux $U_{(y,2q+2)}$ has two inputs namely $U_{i(y,2q+2)}$ and $F_{o(y,2q+2)}$ and has one output $U_{o(y,2q+2)}$. The 2:1 Mux $B_{(y,2q+1)}$ has two inputs namely $UY_{o(y,2q+1)}$ and $U_{o(y,2q+2)}$ and has one output $B_{o(y,2q+1)}$. The 2:1 Mux $B_{(y,2q+2)}$ has two inputs namely $UY_{o(y,2q+1)}$ and $U_{o(y,2q+2)}$ and has one output $B_{o(y,2q+2)}$.

25 The stage (ring "y", stage "q+1") consists of 6 inputs namely $R_{i(y,2q+3)}$, $R_{i(y,2q+4)}$, $RY_{i(y,2q+3)}$, $U_{i(y,2q+3)}$, $U_{i(y,2q+4)}$, and $UY_{i(y,2q+3)}$; and 4 outputs $B_{o(y,2q+3)}$, $B_{o(y,2q+4)}$, $F_{o(y,2q+3)}$, and $F_{o(y,2q+4)}$. The stage (ring "y", stage "2q+1") also consists of six 2:1 Muxes namely $R_{(y,2q+4)}$, $F_{(y,2q+3)}$, $F_{(y,2q+4)}$, $U_{(y,2q+4)}$, $B_{(y,2q+3)}$, and $B_{(y,2q+4)}$. The stage (ring "y", stage "2q+1") also consists of two 3:1 Mux namely $RY_{(y,2q+3)}$ and $UY_{(y,2q+3)}$. The 3:1 Mux $RY_{(y,2q+3)}$ has three inputs

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

namely $R_i(y, 2q+3)$, $RY_i(y, 2q+3)$, and $Bo(y, 2q+3)$ and has one output $RY_o(y, 2q+3)$. The 2:1 Mux $R(y, 2q+4)$ has two inputs namely $R_i(y, 2q+4)$ and $Bo(y, 2q+4)$ and has one output $Ro(y, 2q+4)$. The 2:1 Mux $F(y, 2q+3)$ has two inputs namely $RY_o(y, 2q+3)$ and $Ro(y, 2q+4)$ and has one output $Fo(y, 2q+3)$. The 2:1 Mux $F(y, 2q+4)$ has two inputs
 5 namely $RY_o(y, 2q+3)$ and $Ro(y, 2q+4)$ and has one output $Fo(y, 2q+4)$.

The 3:1 Mux $UY(y, 2q+3)$ has three inputs namely $U_i(y, 2q+3)$, $UY_i(y, 2q+3)$, and $Fo(y, 2q+3)$, and has one output $UY_o(y, 2q+3)$. The 2:1 Mux $U(y, 2q+4)$ has two inputs namely $U_i(y, 2q+4)$ and $Fo(y, 2q+4)$ and has one output $U_o(y, 2q+4)$. The 2:1 Mux $B(y, 2q+3)$ has two inputs namely $UY_o(y, 2q+3)$ and $U_o(y, 2q+4)$ and has one output
 10 $Bo(y, 2q+3)$. The 2:1 Mux $B(y, 2q+4)$ has two inputs namely $UY_o(y, 2q+3)$ and $U_o(y, 2q+4)$ and has one output $Bo(y, 2q+4)$.

The output $Fo(y, 2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $R_i(y, 2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $Bo(y, 2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $U_i(y, 2q+1)$ of the stage (ring “y”, stage
 15 “q”).

The output $Fo(x, 2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire $Hop(1,1)$ to two inputs namely input $R_i(y, 2q+4)$ of the stage (ring “y”, stage “q+1”) and input $UY_i(y, 2q+1)$ of the stage (ring “y”, stage “q”). The output $Bo(x, 2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire $Hop(1,2)$ to two inputs namely input
 20 $U_i(y, 2q+2)$ of the stage (ring “y”, stage “q”) and input $RY_i(y, 2q+3)$ of the stage (ring “y”, stage “q+1”).

The output $Fo(y, 2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire $Hop(2,1)$ to two inputs namely input $R_i(x, 2p+4)$ of the stage (ring “x”, stage “p+1”) and input $YU_i(x, 2p+1)$ of the stage (ring “x”, stage “p”). The output $Bo(y, 2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire $Hop(2,2)$ to two inputs namely input
 25 $U_i(x, 2p+2)$ of the stage (ring “x”, stage “p”) and input $YR_i(x, 2p+3)$ of the stage (ring “x”, stage “p+1”).

Referring to diagram 1400 in FIG. 14, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages
 30

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

(ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 5 inputs namely $F_i(x, 2p+1)$, $F_i(x, 2p+2)$, $YU_i(x, 2p+1)$, $U_i(x, 2p+1)$, and $U_i(x, 2p+2)$; and 4 outputs $B_o(x, 2p+1)$, $B_o(x, 2p+2)$, $F_o(x, 2p+1)$, and $F_o(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of seven 2:1 Muxes namely $F(x, 2p+1)$, $F(x, 2p+2)$, $YF(x, 2p+1)$, $U(x, 2p+1)$, $U(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $F_i(x, 2p+1)$ and $F_i(x, 2p+2)$ and has one output $F_o(x, 2p+1)$. The 2:1 Mux $F(x, 2p+2)$ has two inputs namely $F_i(x, 2p+1)$ and $F_i(x, 2p+2)$ and has one output $F_o(x, 2p+2)$.

The 2:1 Mux $YU(x, 2p+1)$ has two inputs namely $U_i(x, 2p+1)$ and $YU_i(x, 2p+1)$ and has one output $YU_o(x, 2p+1)$. The 2:1 Mux $U(x, 2p+1)$ has two inputs namely $YU_o(x, 2p+1)$ and $F_o(x, 2p+1)$ and has one output $U_o(x, 2p+1)$. The 2:1 Mux $U(x, 2p+2)$ has two inputs namely $U_i(x, 2p+2)$ and $F_o(x, 2p+2)$ and has one output $U_o(x, 2p+2)$. The 2:1 Mux $B(x, 2p+1)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $B_o(x, 2p+1)$. The 2:1 Mux $B(x, 2p+2)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $B_o(x, 2p+2)$.

The stage (ring “x”, stage “p+1”) consists of 5 inputs namely $F_i(x, 2p+3)$, $F_i(x, 2p+4)$, $YF_i(x, 2p+3)$, $U_i(x, 2p+3)$, and $U_i(x, 2p+4)$; and 4 outputs $B_o(x, 2p+3)$, $B_o(x, 2p+4)$, $F_o(x, 2p+3)$, and $F_o(x, 2p+4)$. The stage (ring “x”, stage “p+1”) also consists of seven 2:1 Muxes namely $YF(x, 2p+3)$, $F(x, 2p+3)$, $F(x, 2p+4)$, $U(x, 2p+3)$, $U(x, 2p+4)$, $B(x, 2p+3)$, and $B(x, 2p+4)$. The 2:1 Mux $YF(x, 2p+3)$ has two inputs namely $F_i(x, 2p+3)$ and $YF_i(x, 2p+3)$ and has one output $YF_o(x, 2p+3)$. The 2:1 Mux $F(x, 2p+3)$ has two inputs namely $YF_o(x, 2p+3)$ and $F_i(x, 2p+4)$ and has one output $F_o(x, 2p+3)$. The 2:1 Mux $F(x, 2p+4)$ has two inputs namely $YF_o(x, 2p+3)$ and $F_i(x, 2p+4)$ and has one output $F_o(x, 2p+4)$.

The 2:1 Mux $U(x, 2p+3)$ has two inputs namely $U_i(x, 2p+3)$ and $F_o(x, 2p+3)$ and has one output $U_o(x, 2p+3)$. The 2:1 Mux $U(x, 2p+4)$ has two inputs namely $U_i(x, 2p+4)$ and $F_o(x, 2p+4)$ and has one output $U_o(x, 2p+4)$. The 2:1 Mux $B(x, 2p+3)$ has two inputs namely $U_o(x, 2p+3)$ and $U_o(x, 2p+4)$ and has one output $B_o(x, 2p+3)$. The 2:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$B(x,2p+4)$ has two inputs namely $U_o(x,2p+3)$ and $U_o(x,2p+4)$ and has one output $Bo(x,2p+4)$.

The output $Fo(x,2p+1)$ of the stage (ring “x”, stage “p”) is connected to the input $Fi(x,2p+3)$ of the stage (ring “x”, stage “p+1”). And the output $Bo(x,2p+3)$ of the stage
5 (ring “x”, stage “p+1”) is connected to the input $Ui(x,2p+1)$ of the stage (ring “x”, stage “p”).

The stage (ring “y”, stage “q”) consists of 5 inputs namely $Fi(y,2q+1)$, $Fi(y,2q+2)$, $UYi(y,2q+1)$, $Ui(y,2q+1)$, and $Ui(y,2q+2)$; and 4 outputs $Bo(y,2q+1)$, $Bo(y,2q+2)$, $Fo(y,2q+1)$, and $Fo(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of five 2:1
10 Muxes namely $F(y,2q+1)$, $F(y,2q+2)$, $U(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of one 3:1 Mux namely $UY(y,2q+1)$. The 2:1 Mux $F(y,2q+1)$ has two inputs namely $Fi(y,2q+1)$ and $Fi(y,2q+2)$ and has one output $Fo(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $Fi(y,2q+1)$ and $Fi(y,2q+2)$ and has one output $Fo(y,2q+2)$.

15 The 3:1 Mux $UY(y,2q+1)$ has three inputs namely $Ui(y,2q+1)$, $UYi(y,2q+1)$ and $Fo(y,2q+1)$ and has one output $UYo(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $Ui(y,2q+2)$ and $Fo(y,2q+2)$ and has one output $Uo(y,2q+2)$. The 2:1 Mux $B(y,2q+1)$ has two inputs namely $UYo(y,2q+1)$ and $Uo(y,2q+2)$ and has one output $Bo(y,2q+1)$. The 2:1 Mux $B(y,2q+2)$ has two inputs namely $UYo(y,2q+1)$ and
20 $Uo(y,2q+2)$ and has one output $Bo(y,2q+2)$.

The stage (ring “y”, stage “q+1”) consists of 5 inputs namely $Fi(y,2q+3)$, $Fi(y,2q+4)$, $YFi(y,2q+3)$, $Ui(y,2q+3)$, and $Ui(y,2q+4)$; and 4 outputs $Bo(y,2q+3)$, $Bo(y,2q+4)$, $Fo(y,2q+3)$, and $Fo(y,2q+4)$. The stage (ring “y”, stage “q+1”) also consists of seven 2:1 Muxes namely $YF(y,2q+3)$, $F(y,2q+3)$, $F(y,2q+4)$, $U(y,2q+3)$, $U(y,2q+4)$,
25 $B(y,2q+3)$, and $B(y,2q+4)$. The 2:1 Mux $YF(y,2q+3)$ has two inputs namely $Fi(y,2q+3)$ and $YFi(y,2q+3)$ and has one output $YFo(y,2q+3)$. The 2:1 Mux $F(y,2q+3)$ has two inputs namely $YFo(y,2q+3)$ and $Fi(y,2q+4)$ and has one output $Fo(y,2q+3)$. The 2:1 Mux $F(y,2q+4)$ has two inputs namely $YFo(y,2q+3)$ and $Fi(y,2q+4)$ and has one output $Fo(y,2q+4)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux $U(y,2q+3)$ has two inputs namely $U_i(y,2q+3)$ and $F_o(y,2q+3)$ and has one output $U_o(y,2q+3)$. The 2:1 Mux $U(y,2q+4)$ has two inputs namely $U_i(y,2q+4)$ and $F_o(y,2q+4)$ and has one output $U_o(y,2q+4)$. The 2:1 Mux $B(y,2q+3)$ has two inputs namely $U_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output $B_o(y,2q+3)$. The 2:1 Mux

5 $B(y,2q+4)$ has two inputs namely $U_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output $B_o(y,2q+4)$.

The output $F_o(y,2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $F_i(y,2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $B_o(y,2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $U_i(y,2q+1)$ of the stage (ring “y”, stage

10 “q”).

The output $F_o(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire $Hop(1,1)$ to two inputs namely input $F_i(y,2q+4)$ of the stage (ring “y”, stage “q+1”) and input $UY_i(y,2q+1)$ of the stage (ring “y”, stage “q”). The output $B_o(x,2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire $Hop(1,2)$ to two inputs namely input

15 $U_i(y,2q+2)$ of the stage (ring “y”, stage “q”) and input $YF_i(y,2q+3)$ of the stage (ring “y”, stage “q+1”).

The output $F_o(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire $Hop(2,1)$ to two inputs namely input $F_i(x,2p+4)$ of the stage (ring “x”, stage “p+1”) and input $YU_i(x,2p+1)$ of the stage (ring “x”, stage “p”). The output $B_o(y,2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire $Hop(2,2)$ to two inputs namely input

20 $U_i(x,2p+2)$ of the stage (ring “x”, stage “p”) and input $YF_i(x,2p+3)$ of the stage (ring “x”, stage “p+1”).

Referring to diagram 1500 in FIG. 15, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

25

The stage (ring “x”, stage “p”) consists of 5 inputs namely $R_i(x,2p+1)$, $R_i(x,2p+2)$, $U_i(x,2p+1)$, $U_i(x,2p+2)$, and $BY_i(x,2p+2)$; and 4 outputs $B_o(x,2p+1)$,

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p") also consists of seven 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), and B(x,2p+1). The stage (ring "x", stage "p") also consists of one 3:1 Mux namely BY(x,2p+2). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and Bo(x,2p+1) and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and Bo(x,2p+2) and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Ro(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+1), and Ro(x,2p+2), and has one output Fo(x,2p+2).

10 The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 3:1 Mux BY(x,2p+2) has three inputs namely Uo(x,2p+1), Uo(x,2p+2), and BYi(x,2p+2), and has
15 one output BYo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 5 inputs namely Ri(x,2p+3), Ri(x,2p+4), FYi(x,2p+4), Ui(x,2p+3), and Ui(x,2p+4); and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of seven 2:1 Muxes namely R(x,2p+3), R(x,2p+4), F(x,2p+3), U(x,2p+3), U(x,2p+4),
20 B(x,2p+3), and B(x,2p+4). The stage (ring "x", stage "p+1") also consists of one 3:1 Mux namely FY(x,2p+4). The 2:1 Mux R(x,2p+3) has two inputs namely Ri(x,2p+3) and Bo(x,2p+3) and has one output Ro(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs namely Ri(x,2p+4) and Bo(x,2p+4) and has one output Ro(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely Ro(x,2p+3) and Ro(x,2p+4) and has one output
25 Fo(x,2p+3). The 3:1 Mux FY(x,2p+4) has three inputs namely Ro(x,2p+3), Ro(x,2p+4), and FYi(x,2p+4), and has one output FYo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and Fo(x,2p+3) and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and FYo(x,2p+4) and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs
30 namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+3). The 2:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$B(x,2p+4)$ has two inputs namely $Uo(x,2p+3)$ and $Uo(x,2p+4)$ and has one output $Bo(x,2p+4)$.

The output $Fo(x,2p+1)$ of the stage (ring “x”, stage “p”) is connected to the input $Ri(x,2p+3)$ of the stage (ring “x”, stage “p+1”). And the output $Bo(x,2p+3)$ of the stage
5 (ring “x”, stage “p+1”) is connected to the input $Ui(x,2p+1)$ of the stage (ring “x”, stage “p”).

The stage (ring “y”, stage “q”) consists of 6 inputs namely $Ri(y,2q+1)$, $Ri(y,2q+2)$, $FYi(y,2q+2)$, $Ui(y,2q+1)$, $Ui(y,2q+2)$, and $BYi(y,2q+2)$; and 4 outputs $Bo(y,2q+1)$, $Bo(y,2q+2)$, $Fo(y,2q+1)$, and $Fo(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of six 2:1 Muxes namely $R(y,2q+1)$, $R(y,2q+2)$, $F(y,2q+1)$, $U(y,2q+1)$, $U(y,2q+2)$, and $B(y,2q+1)$. The stage (ring “y”, stage “q”) also consists of two 3:1 Muxes
10 namely $FY(y,2q+2)$ and $BY(y,2q+2)$. The 2:1 Mux $R(y,2q+1)$ has two inputs namely $Ri(y,2q+1)$ and $Bo(y,2q+1)$ and has one output $Ro(y,2q+1)$. The 2:1 Mux $R(y,2q+2)$ has two inputs namely $Ri(y,2q+2)$ and $Bo(y,2q+2)$ and has one output $Ro(y,2q+2)$. The 2:1
15 Mux $F(y,2q+1)$ has two inputs namely $Ro(y,2q+1)$ and $Ro(y,2q+2)$ and has one output $Fo(y,2q+1)$. The 3:1 Mux $FY(y,2q+2)$ has three inputs namely $Ro(y,2q+1)$, $Ro(y,2q+2)$, and $FYi(y,2q+2)$, and has one output $FYo(y,2q+2)$.

The 2:1 Mux $U(y,2q+1)$ has two inputs namely $Ui(y,2q+1)$ and $Fo(y,2q+1)$ and has one output $Uo(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $Ui(y,2q+2)$
20 and $FYo(y,2q+2)$ and has one output $Uo(y,2q+2)$. The 2:1 Mux $B(y,2q+1)$ has two inputs namely $Uo(y,2q+1)$ and $Uo(y,2q+2)$ and has one output $Bo(y,2q+1)$. The 3:1 Mux $BY(y,2q+2)$ has three inputs namely $Uo(y,2q+1)$, $Uo(y,2q+2)$, and $BYi(y,2q+2)$ and has one output $BYo(y,2q+2)$.

The stage (ring “y”, stage “q+1”) consists of 5 inputs namely $Fi(y,2q+3)$,
25 $Fi(y,2q+4)$, $YFi(y,2q+3)$, $Ui(y,2q+3)$, and $Ui(y,2q+4)$; and 4 outputs $Bo(y,2q+3)$, $Bo(y,2q+4)$, $Fo(y,2q+3)$, and $Fo(y,2q+4)$. The stage (ring “y”, stage “q+1”) also consists of seven 2:1 Muxes namely $YF(y,2q+3)$, $F(y,2q+3)$, $F(y,2q+4)$, $U(y,2q+3)$, $U(y,2q+4)$, $B(y,2q+3)$, and $B(y,2q+4)$. The 2:1 Mux $YF(y,2q+3)$ has two inputs namely $Fi(y,2q+3)$ and $YFi(y,2q+3)$ and has one output $YFo(y,2q+3)$. The 2:1 Mux $F(y,2q+3)$ has two inputs
30 namely $YFo(y,2q+3)$ and $Fi(y,2q+4)$ and has one output $Fo(y,2q+3)$. The 2:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

F(y,2q+4) has two inputs namely YFo(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Fi(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to two inputs namely input Fi(y,2q+4) of the stage (ring "y", stage "q+1") and input BYi(y,2q+1) of the stage (ring "y", stage "q"). The output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to two inputs namely input Ui(y,2q+2) of the stage (ring "y", stage "q") and input YFi(y,2q+3) of the stage (ring "y", stage "q+1").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to two inputs namely input Ri(x,2p+4) of the stage (ring "x", stage "p+1") and input BYi(x,2p+1) of the stage (ring "x", stage "p"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to two inputs namely input Ui(x,2p+2) of the stage (ring "x", stage "p") and input YFi(x,2p+4) of the stage (ring "x", stage "p+1").

In accordance with the current invention, either partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100A of FIG. 1A, or partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100B of FIG. 1B, or partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C, corresponding to a block of 2D-grid of blocks 800 of FIG. 8, using any one of the embodiments of 200A-200F of FIGs. 2A-2F,

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

900A-900E of FIGs. 9A-9E, 1000A-1000F of FIGs. 10A-10F, 1100A-1100C of FIGs. 11A-11C to implement a stage of a ring of the multi-stage hierarchical network, either by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, 300E of FIG. 3E, 500A of FIG. 5A, 1200 of FIG. 12, 1300 of FIG. 13, 1400 of FIG. 14, and 1500 of FIG. 15 or by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may be any one of the embodiments of either the diagrams 400A of FIG. 4A, 400B of FIG. 4B, 600A of FIG. 6A, or 600B of FIG. 6B is very efficient in the reduction of the die size, power consumption, and highly optimized for lower wire/path delay for higher performance for practical routing applications to particularly to set up broadcast, unicast and multicast connections. In general in accordance with the current invention, where N_1 and N_2 of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ may be arbitrarily large in size and also the 2D-grid size 800 may also be arbitrarily large in size in terms of both the number of rows and number of columns.

1) Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in programmable integrated circuit applications. FIG. 16A2 illustrates the detailed diagram 1600A2 for the implementation of the diagram 1600A1 in programmable integrated circuit embodiments. Each crosspoint is implemented by a transistor coupled between the corresponding inlet link and outlet link, and a programmable cell in programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by transistor C(1,1) coupled between inlet link IL1 and outlet link OL1, and programmable cell P(1,1); crosspoint CP(1,2) is implemented by transistor C(1,2) coupled between inlet link IL1 and outlet link OL2, and programmable cell P(1,2); crosspoint CP(2,1) is implemented by transistor C(2,1) coupled between inlet link IL2 and outlet link OL1, and programmable cell P(2,1); and crosspoint CP(2,2) is implemented by transistor C(2,2) coupled between inlet link IL2 and outlet link OL2, and programmable cell P(2,2).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

If the programmable cell is programmed ON, the corresponding transistor couples the corresponding inlet link and outlet link. If the programmable cell is programmed OFF, the corresponding inlet link and outlet link are not connected. For example if the programmable cell P(1,1) is programmed ON, the corresponding transistor C(1,1) couples the corresponding inlet link IL1 and outlet link OL1. If the programmable cell P(1,1) is programmed OFF, the corresponding inlet link IL1 and outlet link OL1 are not connected. In volatile programmable integrated circuit embodiments the programmable cell may be an SRAM (Static Random Address Memory) cell. In non-volatile programmable integrated circuit embodiments the programmable cell may be a Flash memory cell. Also the programmable integrated circuit embodiments may implement field programmable logic arrays (FPGA) devices, or programmable Logic devices (PLD), or Application Specific Integrated Circuits (ASIC) embedded with programmable logic circuits or 3D-FPGAs.

FIG. 16A2 also illustrates a buffer B1 on inlet link IL2. The signals driven along inlet link IL2 are amplified by buffer B1. Buffer B1 can be inverting or non-inverting buffer. Buffers such as B1 are used to amplify the signal in links which are usually long.

In other embodiments all the $d * d$ switches described in the current invention are also implemented using muxes of different sizes controlled by SRAM cells or flash cells etc.

2) One-time Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in one-time programmable integrated circuit applications. FIG. 16A3 illustrates the detailed diagram 1600A3 for the implementation of the diagram 1600A1 in one-time programmable integrated circuit embodiments. Each crosspoint is implemented by a via coupled between the corresponding inlet link and outlet link in one-time programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by via V(1,1) coupled between inlet link IL1 and outlet link OL1; crosspoint CP(1,2) is implemented by via V(1,2) coupled between inlet link IL1 and outlet link OL2; crosspoint CP(2,1) is implemented by via V(2,1) coupled between inlet link IL2 and outlet link OL1; and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

crosspoint CP(2,2) is implemented by via V(2,2) coupled between inlet link IL2 and outlet link OL2.

If the via is programmed ON, the corresponding inlet link and outlet link are permanently connected which is denoted by thick circle at the intersection of inlet link and outlet link. If the via is programmed OFF, the corresponding inlet link and outlet link are not connected which is denoted by the absence of thick circle at the intersection of inlet link and outlet link. For example in the diagram 1600A3 the via V(1,1) is programmed ON, and the corresponding inlet link IL1 and outlet link OL1 are connected as denoted by thick circle at the intersection of inlet link IL1 and outlet link OL1; the via V(2,2) is programmed ON, and the corresponding inlet link IL2 and outlet link OL2 are connected as denoted by thick circle at the intersection of inlet link IL2 and outlet link OL2; the via V(1,2) is programmed OFF, and the corresponding inlet link IL1 and outlet link OL2 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL1 and outlet link OL2; the via V(2,1) is programmed OFF, and the corresponding inlet link IL2 and outlet link OL1 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL2 and outlet link OL1. One-time programmable integrated circuit embodiments may be anti-fuse based programmable integrated circuit devices or mask programmable structured ASIC devices.

3) Integrated Circuit Placement and Route Embodiments:

All the embodiments disclosed in the current invention are useful in Integrated Circuit Placement and Route applications, for example in ASIC backend Placement and Route tools. FIG. 16A4 illustrates the detailed diagram 1600A4 for the implementation of the diagram 1600A1 in Integrated Circuit Placement and Route embodiments. In an integrated circuit since the connections are known a-priori, the switch and crosspoints are actually virtual. However the concept of virtual switch and virtual crosspoint using the embodiments disclosed in the current invention reduces the number of required wires, wire length needed to connect the inputs and outputs of different netlists and the time required by the tool for placement and route of netlists in the integrated circuit.

Each virtual crosspoint is used to either to hardwire or provide no connectivity between the corresponding inlet link and outlet link. Specifically crosspoint CP(1,1) is

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

implemented by direct connect point DCP(1,1) to hardwire (i.e., to permanently connect) inlet link IL1 and outlet link OL1 which is denoted by the thick circle at the intersection of inlet link IL1 and outlet link OL1; crosspoint CP(2,2) is implemented by direct connect point DCP(2,2) to hardwire inlet link IL2 and outlet link OL2 which is denoted
5 by the thick circle at the intersection of inlet link IL2 and outlet link OL2. The diagram 1600A4 does not show direct connect point DCP(1,2) and direct connect point DCP(1,3) since they are not needed and in the hardware implementation they are eliminated. Alternatively inlet link IL1 needs to be connected to outlet link OL1 and inlet link IL1 does not need to be connected to outlet link OL2. Also inlet link IL2 needs to be
10 connected to outlet link OL2 and inlet link IL2 does not need to be connected to outlet link OL1. Furthermore in the example of the diagram 1600A4, there is no need to drive the signal of inlet link IL1 horizontally beyond outlet link OL1 and hence the inlet link IL1 is not even extended horizontally until the outlet link OL2. Also the absence of direct connect point DCP(2,1) illustrates there is no need to connect inlet link IL2 and outlet
15 link OL1.

In summary in integrated circuit placement and route tools, the concept of virtual switches and virtual cross points is used during the implementation of the placement & routing algorithmically in software, however during the hardware implementation cross points in the cross state are implemented as hardwired connections between the
20 corresponding inlet link and outlet link, and in the bar state are implemented as no connection between inlet link and outlet link.

3) More Application Embodiments:

25 All the embodiments disclosed in the current invention are also useful in the design of SoC interconnects, Field programmable interconnect chips, parallel computer systems and in time-space-time switches.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Scheduling Method Embodiments the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$:

FIG. 17 shows a high-level flowchart of a scheduling method 1700, in one embodiment executed to setup multicast and unicast connections in the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ disclosed in this invention. According to this embodiment, the set of multicast connections are initialized to the beginning of the set in act 1710. Then the control goes to act 1720. In act 1720, next multicast connection is selected in sequence form the set of multicast connections. Then the control goes to act 1730.

In act 1730 it is checked if this is the next multicast connection in sequence is NULL or i.e. all the multicast connections are scheduled. If act 1730 results “no”, that is there are more multicast connections to be scheduled the control goes to act 1740. In act 1740 it is checked if this multicast connection is being scheduled for the first time. Or if it is not scheduled for the first time, it is checked if any one of the links taken by this multicast connection is oversubscribed by any other multicast connection is checked. If either the multicast connection is being scheduled for the first time or if any one of the links taken by this multicast connection is oversubscribed the control goes to act 1750. Otherwise control goes to act 1720 where the next multicast connection will be selected. So act 1720, act 1730, and act 1740 are executed in a loop.

In act 1750 the multicast connection is not being scheduled for the first time and since at least one of the links taken by this multicast connection is oversubscribed, the complete path taken this multicast connection is cleared or the multicast connection's path is ripped. Then the control goes to act 1760. In act 1760, using the well-known A* search algorithm the least cost path from its source outlet link of the computational block to all the target inlet links of the corresponding computational blocks are found out one after another target inlet links. The cost function used is based on the Manhattan distance between the target inlet link's block and source outlet link's block by taking the delays on each wire is considered in the cost function and also that longest wires are chosen first in the A* search algorithm.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

According to the current invention, before scheduling the set of multicast connections in the scheduling method 1700, first a set of static cost tables will be prepared with the least cost paths from each link of the partial multistage network $V_{Comb}(N_1, N_2, d, s)$ to each outgoing hop wire from that partial multistage network as well as to each inlet link of the computational block connected form that partial multistage network. So there will be as many cost tables created equal to the sum of the total number of outgoing hop wires from the partial multistage network and the inlet links of the computational block connected form that partial multistage network. Each cost table will also have as many entries as there are internal links of that partial multistage network.

5

10 And the value at each entry of these cost tables is equal to the total delay from the corresponding internal link to the corresponding outgoing hop wire or to the inlet link of the computational block.

In act 1760, according to the current invention, for the look-ahead cost computation during the A* search algorithm both the cost from the static cost tables from the current internal link in the current partial multistage network and the cost value computed based on the Manhattan distance between the target inlet link's block and the current link's corresponding block by taking the delays on each wire into consideration are added. Also the least of the cost values from all the cost tables corresponding to the current link and all the outgoing wires in the right direction of the target block, is selected before it is added to the Manhattan distance based cost. Finally in act 1760, the multicast connection is scheduled as for the A* search algorithm. Then the control goes to act 1770.

15

20

In act 1770, the demand cost and history cost of each link used by the current multicast connection are updated. And the control goes to act 1720. Thus act 1720, act 1730, act 1740, act 1750, act 1760, and act 1770 are executed in a loop to schedule the multicast connections by going through the list of all multicast connections which will be one pass or iteration.

25

In act 1730 results "yes", i.e. all the required multicast connections in the list are scheduled in this pass or iteration, then the control goes to act 1780. In act 1780, the total number of links in the complete multistage network that are taken by more than one multicast connection are counted, hereinafter "OSN" or "Over Subscription nodes". Then the control goes to act 1790. In act 1790 it will be checked and if OSN is not equal to zero

30

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

then the act 1790 results in “no” and the control goes to act 1710 to start the next iteration or pass to schedule all the required multicast connections in the list of all multicast connections. Thus act 1710, act 1720, act 1730, act 1740, act 1750, act 1760, act 1770, act 1780, and act 1790 are executed in a loop to implement different passes or iterations
 5 of scheduling the set of all multicast connections. If the act 1790 results in “yes”, that means no link in the complete multistage network is taken by more than one multicast connection and hence the scheduling is successfully completed.

Each multicast connection of the type described above in reference to method 1700 of FIG. 17 can be unicast connection, a multicast connection or a broadcast
 10 connection, depending on the example.

Inter-block and Intra-block Scheduling Method Embodiments the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$:

FIG. 18 shows a high-level flowchart of a scheduling method 1800, in one
 15 embodiment executed to setup multicast connections in the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ disclosed in this invention in two steps (one for each act 1810 and act 1820 as shown in FIG. 18) namely: 1) scheduling the set of multicast connections outside the blocks of 2D-grid of blocks with each block corresponding to a partial multi-stage network, or in between the blocks of the complete multi-stage network, or
 20 alternatively on the external wires of the complete multi-stage network hereinafter “inter-block scheduling”. Inter-block scheduling is implemented in act 1810 so that there are no OSN nodes. During inter-block scheduling the partial multi-stage hierarchical network corresponding to each block is considered as a single stage network or alternatively each internal wire of the partial multi-stage hierarchical network is directly connected to each
 25 outgoing wire or external wire of the partial multi-stage hierarchical network, and 2) scheduling the set of multicast connections inside the blocks of 2D-grid of blocks with each block corresponding to a partial multi-stage network or alternatively on the internal wires of the complete multi-stage network hereinafter “intra-block scheduling”. The act 1820 implements intra-block scheduling for each block so that there are no OSN nodes.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The act 1810 may be implemented by the scheduling method 1700 of FIG. 17. Similarly in act 1820 for each block of the multi-stage hierarchical network, the inter-block scheduling may be implemented by the scheduling method 1700 of FIG. 17.

In accordance with the current invention, the scheduling method 1700 of FIG. 17
5 and the scheduling method 1800 of FIG. 18 are applicable to either partial multi-stage
hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100A of FIG. 1A, or partial multi-stage
hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100B of FIG. 1B, or partial multi-stage
hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C, corresponding to a block of
2D-grid of blocks 800 of FIG. 8, using any one of the embodiments of 200A-200F of
10 FIGs. 2A-2F, 900A-900E of FIGs. 9A-9E, 1000A-1000F of FIGs. 10A-10F, 1100A-
1100C of FIGs. 11A-11C to implement a stage of a ring of the multi-stage hierarchical
network, either by using the hop wire connections or multi-drop hop wire connections
between two arbitrary stages in two different rings of the same block or two different
rings of different blocks described in diagram 700A of FIG. 7A may be any one of the
15 embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG.
3C, 300D of FIG. 3D, 300E of FIG. 3E, 500A of FIG. 5A, 1200 of FIG. 12, 1300 of FIG.
13, 1400 of FIG. 14, and 1500 of FIG. 15 or by using the hop wire connections or multi-
drop hop wire connections between two arbitrary stages in two different rings of the same
block or two different rings of different blocks may be any one of the embodiments of
20 either the diagrams 400A of FIG. 4A, 400B of FIG. 4B, 600A of FIG. 6A, or 600B of
FIG. 6B is very efficient in the reduction of the die size, power consumption, and highly
optimized for lower wire/path delay for higher performance for practical routing
applications to particularly to set up broadcast, unicast and multicast connections.

Numerous modifications and adaptations of the embodiments, implementations,
25 and examples described herein will be apparent to the skilled artisan in view of the
disclosure.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

V. UNEDITED AND COMPLETE SUBSTITUTE SPECIFICATION

Unedited and complete substitute specification appears below:

5 Fully connected multi-stage hierarchical networks are an over kill in every dimension such as area, power, and performance for certain practical routing applications and need to be optimized to significantly improve savings in area, power and performance of the routing network. The present invention discloses several embodiments of the optimized multi-stage hierarchical networks for practical routing applications along with their VLSI layout (floor plan) feasibility and simplicity.

10 The multi-stage hierarchical networks considered for optimization in the current invention include: generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, generalized hypercube networks $V_{cube}(N_1, N_2, d, s)$, and generalized cube connected cycles networks $V_{ccc}(N_1, N_2, d, s)$ for $s = 1, 2, 3$ or any number in general. Alternatively the optimized multi-stage hierarchical networks disclosed in this invention inherit the properties of one or more of these networks, in addition to additional properties that may not be exhibited these networks.

15
20

The optimized multi-stage hierarchical networks disclosed are applicable for practical routing applications, with several goals such as: 1) all the signals in the design starting from an inlet link of the network to an outlet link of the network need to be setup without blocking. These signals may consist of broadcast, unicast and multicast connections; Each routing resource may need to be used by only one signal or connection; 2) physical area consumed by the routing network to setup all the signals needs to be small; 3) power consumption of the network needs to be small, after the signals are setup. Power may be both static power and dynamic power; 4) Delay of the

25

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

signal or a connection needs to be small after it is setup through a path using several routing resources in the path. The smaller the delay of the connections will lead to faster performance of the design. Typically delay of the critical connections determines the performance of the design on a given network; 5) Designs need to be not only routed
5 through the network (i.e., all the signals need to be setup from inlet links of the network to the outlet links of the network.), but also the routing needs to be in faster time using efficient routing algorithms; 6) Efficient VLSI layout of the network is also critical and can greatly influence all the other parameters including the area taken up by the network on the chip, total number of wires, length of the wires, delay through the signal paths and
10 hence the maximum clock speed of operation.

The different varieties of multi-stage networks described in various embodiments in the current invention have not been implemented previously on the semiconductor chips. The practical application of these networks includes Field Programmable Gate Array (FPGA) chips. Current commercial FPGA products such as Xilinx's Vertex,
15 Altera's Stratix, Lattice's ECPx implement island-style architecture using mesh and segmented mesh routing interconnects using either full crossbars or sparse crossbars. These routing interconnects consume large silicon area for crosspoints, long wires, large signal propagation delay and hence consume lot of power.

The current invention discloses the optimization and scheduling methods of multi-
20 stage hierarchical networks with fast scheduling of connections, for practical routing applications of numerous types of multi-stage networks also using multi-drop links. The optimizations disclosed in the current invention are applicable to including the numerous generalized multi-stage networks disclosed in the following patent applications:

1) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and
25 unicast for generalized multi-stage networks $V(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,270,400 that is incorporated by reference above.

2) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized butterfly fat tree networks $V_{bt}(N_1, N_2, d, s)$ with numerous

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

connection topologies and the scheduling methods are described in detail in the US Patent No. 8,170,040 that is incorporated by reference above.

3) Rearrangeably nonblocking for arbitrary fan-out multicast and unicast, and strictly nonblocking for unicast for generalized multi-link multi-stage networks

5 $V_{m\text{link}}(N_1, N_2, d, s)$ and generalized folded multi-link multi-stage networks

$V_{\text{fold-mlink}}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,363,649 that is incorporated by reference above.

4) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and

10 unicast for generalized multi-link butterfly fat tree networks $V_{\text{mlink-bft}}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,170,040 that is incorporated by reference above.

5) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized folded multi-stage networks $V_{\text{fold}}(N_1, N_2, d, s)$ with numerous

15 connection topologies and the scheduling methods are described in detail in the US Patent No. 8,363,649 that is incorporated by reference above.

6) Strictly nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link multi-stage networks $V_{\text{mlink}}(N_1, N_2, d, s)$ and generalized folded multi-link

20 multi-stage networks $V_{\text{fold-mlink}}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,363,649 that is incorporated by reference above.

7) VLSI layouts of numerous types of multi-stage networks are described in the US Patent No. 8,269,523 entitled "VLSI LAYOUTS OF FULLY CONNECTED NETWORKS" that is incorporated by reference above.

25 8) VLSI layouts of numerous types of multi-stage networks are described in the US Patent No. 8,898,611 entitled "VLSI LAYOUTS OF FULLY CONNECTED

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

GENERALIZED AND PYRAMID NETWORKS WITH LOCALITY EXPLOITATION"
that is incorporated by reference above.

In addition the optimization with the VLSI layouts disclosed in the current invention are also applicable to generalized multi-stage pyramid networks

- 5 $V_p(N_1, N_2, d, s)$, generalized folded multi-stage pyramid networks $V_{fold-p}(N_1, N_2, d, s)$,
generalized butterfly fat pyramid networks $V_{bjf}(N_1, N_2, d, s)$, generalized multi-link
multi-stage pyramid networks $V_{mlink-p}(N_1, N_2, d, s)$, generalized folded multi-link multi-
stage pyramid networks $V_{fold-mlink-p}(N_1, N_2, d, s)$, generalized multi-link butterfly fat
pyramid networks $V_{mlink-bjf}(N_1, N_2, d, s)$, generalized hypercube networks
10 $V_{cube}(N_1, N_2, d, s)$ and generalized cube connected cycles networks $V_{CCC}(N_1, N_2, d, s)$
for $s = 1, 2, 3$ or any number in general.

- Finally the current invention discloses the optimizations and VLSI layouts of
multi-stage hierarchical networks $V_{Comb}(N_1, N_2, d, s)$ and the optimizations and VLSI
layouts of multi-stage hierarchical networks $V_{D-Comb}(N_1, N_2, d, s)$ for practical routing
15 applications (particularly to set up broadcast, unicast and multicast connections), where
"Comb" denotes the combination of and "D-Comb" denotes the delay optimized
combination of any of the generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized
folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks
 $V_{bjf}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$,
20 generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized
multi-link butterfly fat tree networks $V_{mlink-bjf}(N_1, N_2, d, s)$, generalized multi-stage
pyramid networks $V_p(N_1, N_2, d, s)$, generalized folded multi-stage pyramid networks
 $V_{fold-p}(N_1, N_2, d, s)$, generalized butterfly fat pyramid networks $V_{bjf}(N_1, N_2, d, s)$,
generalized multi-link multi-stage pyramid networks $V_{mlink-p}(N_1, N_2, d, s)$, generalized
25 folded multi-link multi-stage pyramid networks $V_{fold-mlink-p}(N_1, N_2, d, s)$, generalized
multi-link butterfly fat pyramid networks $V_{mlink-bjf}(N_1, N_2, d, s)$, generalized hypercube

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

networks $V_{cube}(N_1, N_2, d, s)$, and generalized cube connected cycles networks $V_{ccc}(N_1, N_2, d, s)$ for $s = 1, 2, 3$ or any number in general.

Multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$:

Referring to diagram 100A in FIG. 1A, in one embodiment, an exemplary partial
 5 multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ where $N_1 = 200$; $N_2 = 400$; $d = 2$;
 and $s = 1$ corresponding to one computational block, with each computational block
 having 4 inlet links namely I1, I2, I3, and I4; and 2 outlet links namely O1 and O2. And
 for each computational block the corresponding partial multi-stage hierarchical network
 $V_{Comb}(N_1, N_2, d, s)$ 100A consists of two rings 110 and 120, where ring 110 consists of
 10 “m+1” stages namely (ring 1, stage 0), (ring 1, stage 1), ... (ring 1, stage “m-1”), and
 (ring 1, stage “m”), and ring 120 consists of “n+1” stages namely (ring 2, stage 0), (ring
 2, stage 1), ... (ring 2, stage “n-1”), and (ring 2, stage “n”), where “m” and “n” are
 positive integers.

Ring 110 has inlet links Ri(1,1) and Ri(1,2), and has outlet links Bo(1,1) and
 15 Bo(1,2). Ring 120 has inlet links Fi(2,1) and Fi(2,2), and outlet links Bo(2,1) and Bo(2,2).
 And hence the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists
 of 4 inlet links and 4 outlet links corresponding to the two rings 110 and 120. Outlet link
 O1 of the computational block is connected to inlet link Ri(1,1) of ring 110 and also inlet
 link of Fi(2,1) of ring 120. Similarly outlet link O2 of the computational block is
 20 connected to inlet link Ri(1,2) of Ring 110 and also inlet link of Fi(2,2) of Ring 120. And
 outlet link Bo(1,1) of Ring 110 is connected to inlet link I1 of the computational block.
 Outlet link Bo(1,2) of Ring 110 is connected to inlet link I2 of the computational block.
 Similarly outlet link Bo(2,1) of Ring 120 is connected to inlet link I3 of the
 computational block. Outlet link Bo(2,2) of Ring 120 is connected to inlet link I4 of the
 25 computational block. Since in this embodiment outlet link O1 of the computational block
 is connected to both inlet link Ri(1,1) of ring 110 and inlet link Fi(2,1) of ring 120; and
 outlet link O2 of the computational block is connected to both inlet link Ri(1,2) of ring
 110 and inlet link Fi(2,2) of ring 120, the partial multi-stage hierarchical network
 $V_{Comb}(N_1, N_2, d, s)$ 100A consists of 2 inlet links and 4 outlet links.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The two dimensional grid 800 in FIG. 8 illustrates an exemplary arrangement of 100 blocks arranged in 10 rows and 10 columns, in an embodiment. Each row of 2D-grid consisting of 10 block numbers namely the first row consists of the blocks (1,1), (1,2), (1,3), ... , (1,9), and (1,10). The second row consists of the blocks (2,1), (2,2), (2,3), ... , (2,9), and (2,10). Similarly 2D-grid 800 consists of 10 rows of each with 10 blocks and finally the tenth row consists of the blocks (10,1), (10,2), (10,3), ... , (10,9), and (10,10). Each block of 2D-grid 800, in one embodiment, is part of the die area of a semiconductor integrated circuit (hereinafter alternatively referred to as “integrated circuit device” or “IC device”), so that the complete 2D-grid 800 of 100 blocks represents the complete die of the semiconductor integrated circuit. In one embodiment, each block of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A with 2 inlet links and 4 outlet links and the corresponding computational block with 4 inlet links and 2 outlet links. For example block (1,1) of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A with 2 inlet links and 4 outlet links and the corresponding computational block with 4 inlet links and 2 outlet links. Similarly each of the 100 blocks of 2D-grid 800 has a separate partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A with 2 inlet links and 4 outlet links and the corresponding computational block with 4 inlet links and 2 outlet links. Hence the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to 2D-grid 800 has $N_1 = 200$ inlet links and $N_2 = 400$ outlet links. And there are 100 computational blocks each one corresponding to one of the blocks with each computational block having 4 inlet links and 2 outlet links. Also the 2D-grid 800 is organized in the fourth quadrant of the 2D-Plane. In other embodiments the 2D-grid 800 may be organized as either first quadrant, or second quadrant or third quadrant of the 2D-Plane.

Referring to partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A in FIG. 1A, the stage (ring 1, stage 0) consists of 4 inputs namely $Ri(1,1)$, $Ri(1,2)$, $Ui(1,1)$, and $Ui(1,2)$; and 4 outputs $Bo(1,1)$, $Bo(1,2)$, $Fo(1,1)$, and $Fo(1,2)$. The stage (ring 1, stage 0) also consists of eight 2:1 multiplexers (A multiplexer is hereinafter called a “mux”) namely $R(1,1)$, $R(1,2)$, $F(1,1)$, $F(1,2)$, $U(1,1)$, $U(1,2)$, $B(1,1)$, and $B(1,2)$. The 2:1 Mux $R(1,1)$ has two inputs namely $Ri(1,1)$ and $Bo(1,1)$ and has one output $Ro(1,1)$. The 2:1 Mux $R(1,2)$ has two inputs namely $Ri(1,2)$ and $Bo(1,2)$ and has one output $Ro(1,2)$. The

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

2:1 Mux F(1,1) has two inputs namely Ro(1,1) and Ro(1,2) and has one output Fo(1,1).
The 2:1 Mux F(1,2) has two inputs namely Ro(1,1) and Ro(1,2) and has one output
Fo(1,2).

The 2:1 Mux U(1,1) has two inputs namely Ui(1,1) and Fo(1,1) and has one
5 output Uo(1,1). The 2:1 Mux U(1,2) has two inputs namely Ui(1,2) and Fo(1,2) and has
one output Uo(1,2). The 2:1 Mux B(1,1) has two inputs namely Uo(1,1) and Uo(1,2) and
has one output Bo(1,1). The 2:1 Mux B(1,2) has two inputs namely Uo(1,1) and Uo(1,2)
and has one output Bo(1,2).

The stage (ring 1, stage 1) consists of 4 inputs namely Ri(1,3), Ri(1,4), Ui(1,3),
10 and Ui(1,4); and 4 outputs Bo(1,3), Bo(1,4), Fo(1,3), and Fo(1,4). The stage (ring 1, stage
1) also consists of eight 2:1 Muxes namely R(1,3), R(1,4), F(1,3), F(1,4), U(1,3), U(1,4),
B(1,3), and B(1,4). The 2:1 Mux R(1,3) has two inputs namely Ri(1,3) and Bo(1,3) and
has one output Ro(1,3). The 2:1 Mux R(1,4) has two inputs namely Ri(1,4) and Bo(1,4)
and has one output Ro(1,4). The 2:1 Mux F(1,3) has two inputs namely Ro(1,3) and
15 Ro(1,4) and has one output Fo(1,3). The 2:1 Mux F(1,4) has two inputs namely Ro(1,3)
and Ro(1,4) and has one output Fo(1,4).

The 2:1 Mux U(1,3) has two inputs namely Ui(1,3) and Fo(1,3) and has one
output Uo(1,3). The 2:1 Mux U(1,4) has two inputs namely Ui(1,4) and Fo(1,4) and has
one output Uo(1,4). The 2:1 Mux B(1,3) has two inputs namely Uo(1,3) and Uo(1,4) and
20 has one output Bo(1,3). The 2:1 Mux B(1,4) has two inputs namely Uo(1,3) and Uo(1,4)
and has one output Bo(1,4).

The output Fo(1,1) of the stage (ring 1, stage 0) is connected to the input Ri(1,3)
of the stage (ring 1, stage 1) which is called hereinafter an internal connection (hereinafter
alternatively referred to as "straight link" or "straight middle link") between two
25 successive stages of a ring. And the output Bo(1,3) of the stage (ring 1, stage 1) is
connected to the input Ui(1,1) of the stage (ring 1, stage 0), is another internal connection
between stage 0 and stage 1 of the ring 1.

The stage (ring 1, stage "m-1") consists of 4 inputs namely Fi(1,2m-1), Fi(1,2m),
Ui(1,2m-1), and Ui(1,2m); and 4 outputs Bo(1,2m-1), Bo(1,2m), Fo(1,2m-1), and
30 Fo(1,2m). The stage (ring 1, stage "m-1") also consists of six 2:1 Muxes namely F(1,2m-

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

1), $F(1,2m)$, $U(1,2m-1)$, $U(1,2m)$, $B(1,2m-1)$, and $B(1,2m)$. The 2:1 Mux $F(1,2m-1)$ has two inputs namely $F_i(1,2m-1)$ and $F_i(1,2m)$ and has one output $F_o(1,2m-1)$. The 2:1 Mux $F(1,2m)$ has two inputs namely $F_i(1,2m-1)$ and $F_i(1,2m)$ and has one output $F_o(1,2m)$.

The 2:1 Mux $U(1,2m-1)$ has two inputs namely $U_i(1,2m-1)$ and $F_o(1,2m-1)$ and
 5 has one output $U_o(1,2m-1)$. The 2:1 Mux $U(1,2m)$ has two inputs namely $U_i(1,2m)$ and $F_o(1,2m)$ and has one output $U_o(1,2m)$. The 2:1 Mux $B(1,2m-1)$ has two inputs namely $U_o(1,2m-1)$ and $U_o(1,2m)$ and has one output $B_o(1,2m-1)$. The 2:1 Mux $B(1,2m)$ has two inputs namely $U_o(1,2m-1)$ and $U_o(1,2m)$ and has one output $B_o(1,2m)$.

The stage (ring 1, stage "m") consists of 4 inputs namely $F_i(1,2m+1)$, $F_i(1,2m+2)$,
 10 $U_i(1,2m+1)$, and $U_i(1,2m+2)$; and 4 outputs $B_o(1,2m+1)$, $B_o(1,2m+2)$, $F_o(1,2m+1)$, and $F_o(1,2m+2)$. The stage (ring 1, stage "m") also consists of six 2:1 Muxes namely $F(1,2m+1)$, $F(1,2m+2)$, $U(1,2m+1)$, $U(1,2m+2)$, $B(1,2m+1)$, and $B(1,2m+2)$. The 2:1 Mux $F(1,2m+1)$ has two inputs namely $F_i(1,2m+1)$ and $F_i(1,2m+2)$ and has one output $F_o(1,2m+1)$. The 2:1 Mux $F(1,2m+2)$ has two inputs namely $F_i(1,2m+1)$ and $F_i(1,2m+2)$
 15 and has one output $F_o(1,2m+2)$.

The 2:1 Mux $U(1,2m+1)$ has two inputs namely $U_i(1,2m+1)$ and $F_o(1,2m+1)$ and has one output $U_o(1,2m+1)$. The 2:1 Mux $U(1,2m+2)$ has two inputs namely $U_i(1,2m+2)$ and $F_o(1,2m+2)$ and has one output $U_o(1,2m+2)$. The 2:1 Mux $B(1,2m+1)$ has two inputs namely $U_o(1,2m+1)$ and $U_o(1,2m+2)$ and has one output $B_o(1,2m+1)$. The 2:1 Mux
 20 $B(1,2m+2)$ has two inputs namely $U_o(1,2m+1)$ and $U_o(1,2m+2)$ and has one output $B_o(1,2m+2)$.

The output $F_o(1,2m-1)$ of the stage (ring 1, stage "m-1") is connected to the input $F_i(1,2m+1)$ of the stage (ring 1, stage "m"), is an internal connection between stage "m-1" and stage "m" of the ring 1. And the output $B_o(1,2m+1)$ of the stage (ring 1, stage
 25 "m") is connected to the input $U_i(1,2m-1)$ of the stage (ring 1, stage "m-1"), is another internal connection between stage "m-1" and stage "m" of the ring 1

Just the same way the stages (ring 1, stage 0), (ring 1, stage 1), there are also stages (ring 1, stage 2), (ring 1, stage 3), ... (ring 1, stage "m-1"), (ring 1, stage "m") in that order, where the stages from (ring 1, stage 2), (ring 1, stage 3), ... , (ring 1, stage
 30 "m-2") are not shown in the diagram 100A. Just the same way the two successive stages

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

(ring 1, stage 0) and (ring 1, stage 1) have internal connections between them as described before, any two successive stages have similar internal connections. For example (ring 1, stage 1) and (ring 1, stage 2) have similar internal connections and (ring 1, stage “m-2”) and (ring 1, stage “m-1”) have similar internal connections.

5 Stage (ring 1, stage 0) is also called hereinafter the “entry stage” or “first stage” of ring 1, since inlet links and outlet links of the computational block are directly connected to stage (ring 1, stage 0). Also stage (ring 1, stage “m”) is hereinafter the “last stage” or “root stage” of ring 1.

 The stage (ring 2, stage 0) consists of 4 inputs namely $F_{i(2,1)}$, $F_{i(2,2)}$, $U_{i(2,1)}$,
10 and $U_{i(2,2)}$; and 4 outputs $B_{o(2,1)}$, $B_{o(2,2)}$, $F_{o(2,1)}$, and $F_{o(2,2)}$. The stage (ring 2, stage 0) also consists of six 2:1 Muxes namely $F(2,1)$, $F(2,2)$, $U(2,1)$, $U(2,2)$, $B(2,1)$, and $B(2,2)$. The 2:1 Mux $F(2,1)$ has two inputs namely $F_{i(2,1)}$ and $F_{i(2,2)}$ and has one output $F_{o(2,1)}$. The 2:1 Mux $F(2,2)$ has two inputs namely $F_{i(2,1)}$ and $F_{i(2,2)}$ and has one output $F_{o(2,2)}$.

15 The 2:1 Mux $U(2,1)$ has two inputs namely $U_{i(2,1)}$ and $F_{o(2,1)}$ and has one output $U_{o(2,1)}$. The 2:1 Mux $U(2,2)$ has two inputs namely $U_{i(2,2)}$ and $F_{o(2,2)}$ and has one output $U_{o(2,2)}$. The 2:1 Mux $B(2,1)$ has two inputs namely $U_{o(2,1)}$ and $U_{o(2,2)}$ and has one output $B_{o(2,1)}$. The 2:1 Mux $B(2,2)$ has two inputs namely $U_{o(2,1)}$ and $U_{o(2,2)}$ and has one output $B_{o(2,2)}$.

20 The stage (ring 2, stage 1) consists of 4 inputs namely $F_{i(2,3)}$, $F_{i(2,4)}$, $U_{i(2,3)}$,
and $U_{i(2,4)}$; and 4 outputs $B_{o(2,3)}$, $B_{o(2,4)}$, $F_{o(2,3)}$, and $F_{o(2,4)}$. The stage (ring 2, stage 1) also consists of six 2:1 Muxes namely $F(2,3)$, $F(2,4)$, $U(2,3)$, $U(2,4)$, $B(2,3)$, and $B(2,4)$. The 2:1 Mux $F(2,3)$ has two inputs namely $F_{i(2,3)}$ and $F_{i(2,4)}$ and has one output $F_{o(2,3)}$. The 2:1 Mux $F(2,4)$ has two inputs namely $F_{i(2,3)}$ and $F_{i(2,4)}$ and has one
25 output $F_{o(2,4)}$.

 The 2:1 Mux $U(2,3)$ has two inputs namely $U_{i(2,3)}$ and $F_{o(2,3)}$ and has one
output $U_{o(2,3)}$. The 2:1 Mux $U(2,4)$ has two inputs namely $U_{i(2,4)}$ and $F_{o(2,4)}$ and has
one output $U_{o(2,4)}$. The 2:1 Mux $B(2,3)$ has two inputs namely $U_{o(2,3)}$ and $U_{o(2,4)}$ and
has one output $B_{o(2,3)}$. The 2:1 Mux $B(2,4)$ has two inputs namely $U_{o(2,3)}$ and $U_{o(2,4)}$
30 and has one output $B_{o(2,4)}$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The output $Fo(2,1)$ of the stage (ring 2, stage 0) is connected to the input $Fi(2,3)$ of the stage (ring 2, stage 1), is an internal connection between stage 0 and stage 1 of the ring 2. And the output $Bo(2,3)$ of the stage (ring 2, stage 1) is connected to the input $Ui(2,1)$ of the stage (ring 2, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1..

The stage (ring 2, stage “n-1”) consists of 4 inputs namely $Ri(2,2n-1)$, $Ri(2,2n)$, $Ui(1,2n-1)$, and $Ui(1,2n)$; and 4 outputs $Bo(1,2n-1)$, $Bo(1,2n)$, $Fo(1,2n-1)$, and $Fo(1,2n)$. The stage (ring 2, stage “n-1”) also consists of eight 2:1 Muxes namely $R(2,2n-1)$, $R(2,2n)$, $F(2,2n-1)$, $F(1,2n)$, $U(1,2n-1)$, $U(1,2n)$, $B(1,2n-1)$, and $B(1,2n)$. The 2:1 Mux $R(2,2n-1)$ has two inputs namely $Ri(2,2n-1)$ and $Bo(2,2n-1)$ and has one output $Ro(2,2n-1)$. The 2:1 Mux $R(2,2n)$ has two inputs namely $Ri(2,2n)$ and $Bo(2,2n)$ and has one output $Ro(2,2n)$. The 2:1 Mux $F(2,2n-1)$ has two inputs namely $Ro(2,2n-1)$ and $Ro(2,2n)$ and has one output $Fo(2,2n-1)$. The 2:1 Mux $F(2,2n)$ has two inputs namely $Ro(2,2n-1)$ and $Ro(2,2n)$ and has one output $Fo(2,2n)$.

The 2:1 Mux $U(2,2n-1)$ has two inputs namely $Ui(2,2n-1)$ and $Fo(2,2n-1)$ and has one output $Uo(2,2n-1)$. The 2:1 Mux $U(2,2n)$ has two inputs namely $Ui(2,2n)$ and $Fo(2,2n)$ and has one output $Uo(2,2n)$. The 2:1 Mux $B(2,2n-1)$ has two inputs namely $Uo(2,2n-1)$ and $Uo(2,2n)$ and has one output $Bo(2,2n-1)$. The 2:1 Mux $B(2,2n)$ has two inputs namely $Uo(2,2n-1)$ and $Uo(2,2n)$ and has one output $Bo(2,2n)$.

The stage (ring 2, stage “n”) consists of 4 inputs namely $Ri(2,2n+1)$, $Ri(2,2n+2)$, $Ui(2,2n+1)$, and $Ui(2,2n+2)$; and 4 outputs $Bo(2,2n+1)$, $Bo(2,2n+2)$, $Fo(2,2n+1)$, and $Fo(2,2n+2)$. The stage (ring 2, stage “n”) also consists of eight 2:1 Muxes namely $R(2,2n+1)$, $R(2,2n+2)$, $F(2,2n+1)$, $F(2,2n+2)$, $U(2,2n+1)$, $U(2,2n+2)$, $B(2,2n+1)$, and $B(2,2n+2)$. The 2:1 Mux $R(2,2n+1)$ has two inputs namely $Ri(2,2n+1)$ and $Bo(2,2n+1)$ and has one output $Ro(2,2n+1)$. The 2:1 Mux $R(2,2n+2)$ has two inputs namely $Ri(2,2n+2)$ and $Bo(2,2n+2)$ and has one output $Ro(2,2n+2)$. The 2:1 Mux $F(2,2n+1)$ has two inputs namely $Ro(2,2n+1)$ and $Ro(2,2n+2)$ and has one output $Fo(2,2n+1)$. The 2:1 Mux $F(2,2n+2)$ has two inputs namely $Ro(2,2n+1)$ and $Ro(2,2n+2)$ and has one output $Fo(2,2n+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux U(2,2n+1) has two inputs namely $U_i(2,2n+1)$ and $F_o(2,2n+1)$ and has one output $U_o(2,2n+1)$. The 2:1 Mux U(2,2n+2) has two inputs namely $U_i(2,2n+2)$ and $F_o(2,2n+2)$ and has one output $U_o(2,2n+2)$. The 2:1 Mux B(2,2n+1) has two inputs namely $U_o(2,2n+1)$ and $U_o(2,2n+2)$ and has one output $B_o(2,2n+1)$. The 2:1 Mux
 5 B(2,2n+2) has two inputs namely $U_o(2,2n+1)$ and $U_o(2,2n+2)$ and has one output $B_o(2,2n+2)$.

The output $F_o(2,2n-1)$ of the stage (ring 2, stage "n-1") is connected to the input $R_i(2,2n+1)$ of the stage (ring 2, stage "n"), is an internal connection between stage "n-1" and stage "n" of the ring 1. And the output $B_o(2,2n+1)$ of the stage (ring 2, stage "n") is
 10 connected to the input $U_i(2,2n-1)$ of the stage (ring 2, stage "n-1"), is another internal connection between stage "n-1" and stage "n" of the ring 1.

Each stage of any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists of 4 inputs and $2 * d = 4$ outputs. Even though the stages (ring 1, stage 0), (ring 1, stage 1), (ring 2, stage "n-1"), and (ring 2, stage "n")
 15 each have eight 2:1 muxes, and the stages (ring 2, stage 0), (ring 2, stage 1), (ring 1, stage "m-1"), and (ring 1, stage "m") each have six 2:1 muxes, in other embodiments any of these stages can be one of the four by four switch diagrams namely 200A of FIG. 2A, 200B of FIG. 2B, 200C of FIG. 2C, and one of the eight by four switch diagrams namely 200E of FIG. 2E, 200F of FIG. 2F.

20 Referring to diagram 100B in FIG. 1B, in one embodiment, an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ where $N_1 = 400$; $N_2 = 800$; $d = 2$; and $s = 1$ corresponding to one computational block, with each computational block having 8 inlet links namely I1, I2, I3, I4, I5, I6, I7, and I8; and 4 outlet links namely O1, O2, O3, and O4. And for each computational block the corresponding partial multi-stage
 25 hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of two rings 110 and 120, where ring 110 consists of "m+1" stages namely (ring 1, stage 0), (ring 1, stage 1), ... (ring 1, stage "m-1"), and (ring 1, stage "m"), and ring 120 consists of "n+1" stages namely (ring 2, stage 0), (ring 2, stage 1), ... (ring 2, stage "n-1"), and (ring 2, stage "n"), where "m" and "n" are positive integers.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Ring 110 has inlet links $Ri(1,1)$ and $Ri(1,2)$ from the left-hand side, and has outlet links $Bo(1,1)$ and $Bo(1,2)$ from left-hand side. Ring 110 also has inlet links $Ui(1,2m+1)$ and $Ui(1,2m+2)$ from the right-hand side, and has outlet links $Fo(1,2m+1)$ and $Fo(1,2m+2)$ from right-hand side. Ring 120 has inlet links $Fi(2,1)$ and $Fi(2,2)$ from left-hand side, and outlet links $Bo(2,1)$ and $Bo(2,2)$ from left-hand side. Ring 120 also has inlet links $Ui(2,2n+1)$ and $Ui(2,2n+2)$ from the right-hand side, and has outlet links $Fo(2,2n+1)$ and $Fo(2,2n+2)$ from right-hand side.

And the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of 8 inlet links and 4 outlet links corresponding to the two rings 110 and 120. From left-hand side, outlet link O1 of the computational block is connected to inlet link $Ri(1,1)$ of ring 110 and also inlet link of $Fi(2,1)$ of ring 120. Similarly from left-hand side, outlet link O2 of the computational block is connected to inlet link $Ri(1,2)$ of Ring 110 and also inlet link of $Fi(2,2)$ of Ring 120. And from left-hand side, outlet link $Bo(1,1)$ of Ring 110 is connected to inlet link I1 of the computational block. From left-hand side, Outlet link $Bo(1,2)$ of Ring 110 is connected to inlet link I2 of the computational block. Similarly from left-hand side, outlet link $Bo(2,1)$ of Ring 120 is connected to inlet link I3 of the computational block. From left-hand side, outlet link $Bo(2,2)$ of Ring 120 is connected to inlet link I4 of the computational block.

From right-hand side, outlet link O3 of the computational block is connected to inlet link $Ui(1,2m+1)$ of ring 110 and also inlet link of $Ui(2,2n+1)$ of ring 120. Similarly from right-hand side, outlet link O4 of the computational block is connected to inlet link $Ui(1,2m+2)$ of Ring 110 and also inlet link of $Ui(2,2n+2)$ of Ring 120. And from right-hand side, outlet link $Fo(1,2m+1)$ of Ring 110 is connected to inlet link I5 of the computational block. From right-hand side, outlet link $Fo(1,2m+2)$ of Ring 110 is connected to inlet link I6 of the computational block. Similarly from right-hand side, outlet link $Fo(2,2n+1)$ of Ring 120 is connected to inlet link I7 of the computational block. From right-hand side, outlet link $Fo(2,2n+2)$ of Ring 120 is connected to inlet link I8 of the computational block.

Since in this embodiment outlet link O1 of the computational block is connected to both inlet link $Ri(1,1)$ of ring 110 and inlet link $Fi(2,1)$ of ring 120; outlet link O2 of the computational block is connected to both inlet link $Ri(1,2)$ of ring 110 and inlet link

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Fi(2,2) of ring 120; outlet link O3 of the computational block is connected to both inlet link Ui(1,2m+1) of ring 110 and inlet link Ui(2,2n+1) of ring 120; and outlet link O4 of the computational block is connected to both inlet link Ui(1,2m+2) of ring 110 and inlet link Ui(2,2n+2) of ring 120, the partial multi-stage hierarchical network

5 $V_{Comb}(N_1, N_2, d, s)$ 100B consists of 4 inlet links and 8 outlet links.

Referring to two dimensional grid 800 in FIG. 8 illustrates, in another embodiment, each block of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B with 4 inlet links and 8 outlet links and the corresponding computational block with 8 inlet links and 4 outlet links. For example
 10 block (1,1) of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B with 4 inlet links and 8 outlet links and the corresponding computational block with 8 inlet links and 4 outlet links. Similarly each of the 100 blocks of 2D-grid 800 has a separate partial multi-stage hierarchical network
 $V_{Comb}(N_1, N_2, d, s)$ 100B with 4 inlet links and 8 outlet links and the corresponding
 15 computational block with 8 inlet links and 4 outlet links. Hence the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to 2D-grid 800 has $N_1 = 400$ inlet links and $N_2 = 800$ outlet links. Since there are 100 computational blocks each one corresponding to one of the blocks with each computational block having 8 inlet links and 4 outlet links. Also the 2D-grid 800 is organized in the fourth quadrant of the 2D-Plane.
 20 In other embodiments the 2D-grid 800 may be organized as either first quadrant, or second quadrant or third quadrant of the 2D-Plane.

Referring to partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B in FIG. 1B, the stage (ring 1, stage 0) consists of 4 inputs namely Ri(1,1), Ri(1,2), Ui(1,1), and Ui(1,2); and 4 outputs Bo(1,1), Bo(1,2), Fo(1,1), and Fo(1,2). The stage (ring 1, stage
 25 0) also consists of eight 2:1 multiplexers (A multiplexer is hereinafter called a "mux") namely R(1,1), R(1,2), F(1,1), F(1,2), U(1,1), U(1,2), B(1,1), and B(1,2). The 2:1 Mux R(1,1) has two inputs namely Ri(1,1) and Bo(1,1) and has one output Ro(1,1). The 2:1 Mux R(1,2) has two inputs namely Ri(1,2) and Bo(1,2) and has one output Ro(1,2). The 2:1 Mux F(1,1) has two inputs namely Ro(1,1) and Ro(1,2) and has one output Fo(1,1).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux F(1,2) has two inputs namely Ro(1,1) and Ro(1,2) and has one output Fo(1,2).

The 2:1 Mux U(1,1) has two inputs namely Ui(1,1) and Fo(1,1) and has one output Uo(1,1). The 2:1 Mux U(1,2) has two inputs namely Ui(1,2) and Fo(1,2) and has one output Uo(1,2). The 2:1 Mux B(1,1) has two inputs namely Uo(1,1) and Uo(1,2) and has one output Bo(1,1). The 2:1 Mux B(1,2) has two inputs namely Uo(1,1) and Uo(1,2) and has one output Bo(1,2).

The stage (ring 1, stage 1) consists of 4 inputs namely Ri(1,3), Ri(1,4), Ui(1,3), and Ui(1,4); and 4 outputs Bo(1,3), Bo(1,4), Fo(1,3), and Fo(1,4). The stage (ring 1, stage 1) also consists of eight 2:1 Muxes namely R(1,3), R(1,4), F(1,3), F(1,4), U(1,3), U(1,4), B(1,3), and B(1,4). The 2:1 Mux R(1,3) has two inputs namely Ri(1,3) and Bo(1,3) and has one output Ro(1,3). The 2:1 Mux R(1,4) has two inputs namely Ri(1,4) and Bo(1,4) and has one output Ro(1,4). The 2:1 Mux F(1,3) has two inputs namely Ro(1,3) and Ro(1,4) and has one output Fo(1,3). The 2:1 Mux F(1,4) has two inputs namely Ro(1,3) and Ro(1,4) and has one output Fo(1,4).

The 2:1 Mux U(1,3) has two inputs namely Ui(1,3) and Fo(1,3) and has one output Uo(1,3). The 2:1 Mux U(1,4) has two inputs namely Ui(1,4) and Fo(1,4) and has one output Uo(1,4). The 2:1 Mux B(1,3) has two inputs namely Uo(1,3) and Uo(1,4) and has one output Bo(1,3). The 2:1 Mux B(1,4) has two inputs namely Uo(1,3) and Uo(1,4) and has one output Bo(1,4).

The output Fo(1,1) of the stage (ring 1, stage 0) is connected to the input Ri(1,3) of the stage (ring 1, stage 1) which is called hereinafter an internal connection between two successive stages of a ring. And the output Bo(1,3) of the stage (ring 1, stage 1) is connected to the input Ui(1,1) of the stage (ring 1, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1.

The stage (ring 1, stage "m-1") consists of 4 inputs namely Fi(1,2m-1), Fi(1,2m), Ui(1,2m-1), and Ui(1,2m); and 4 outputs Bo(1,2m-1), Bo(1,2m), Fo(1,2m-1), and Fo(1,2m). The stage (ring 1, stage "m-1") also consists of six 2:1 Muxes namely F(1,2m-1), F(1,2m), U(1,2m-1), U(1,2m), B(1,2m-1), and B(1,2m). The 2:1 Mux F(1,2m-1) has

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

two inputs namely $F_{i(1,2m-1)}$ and $F_{i(1,2m)}$ and has one output $F_{o(1,2m-1)}$. The 2:1 Mux $F(1,2m)$ has two inputs namely $F_{i(1,2m-1)}$ and $F_{i(1,2m)}$ and has one output $F_{o(1,2m)}$.

The 2:1 Mux $U(1,2m-1)$ has two inputs namely $U_{i(1,2m-1)}$ and $F_{o(1,2m-1)}$ and has one output $U_{o(1,2m-1)}$. The 2:1 Mux $U(1,2m)$ has two inputs namely $U_{i(1,2m)}$ and $F_{o(1,2m)}$ and has one output $U_{o(1,2m)}$. The 2:1 Mux $B(1,2m-1)$ has two inputs namely $U_{o(1,2m-1)}$ and $U_{o(1,2m)}$ and has one output $B_{o(1,2m-1)}$. The 2:1 Mux $B(1,2m)$ has two inputs namely $U_{o(1,2m-1)}$ and $U_{o(1,2m)}$ and has one output $B_{o(1,2m)}$.

The stage (ring 1, stage "m") consists of 4 inputs namely $F_{i(1,2m+1)}$, $F_{i(1,2m+2)}$, $U_{i(1,2m+1)}$, and $U_{i(1,2m+2)}$; and 4 outputs $B_{o(1,2m+1)}$, $B_{o(1,2m+2)}$, $F_{o(1,2m+1)}$, and $F_{o(1,2m+2)}$. The stage (ring 1, stage "m") also consists of six 2:1 Muxes namely $F(1,2m+1)$, $F(1,2m+2)$, $U(1,2m+1)$, $U(1,2m+2)$, $B(1,2m+1)$, and $B(1,2m+2)$. The 2:1 Mux $F(1,2m+1)$ has two inputs namely $F_{i(1,2m+1)}$ and $F_{i(1,2m+2)}$ and has one output $F_{o(1,2m+1)}$. The 2:1 Mux $F(1,2m+2)$ has two inputs namely $F_{i(1,2m+1)}$ and $F_{i(1,2m+2)}$ and has one output $F_{o(1,2m+2)}$.

The 2:1 Mux $U(1,2m+1)$ has two inputs namely $U_{i(1,2m+1)}$ and $F_{o(1,2m+1)}$ and has one output $U_{o(1,2m+1)}$. The 2:1 Mux $U(1,2m+2)$ has two inputs namely $U_{i(1,2m+2)}$ and $F_{o(1,2m+2)}$ and has one output $U_{o(1,2m+2)}$. The 2:1 Mux $B(1,2m+1)$ has two inputs namely $U_{o(1,2m+1)}$ and $U_{o(1,2m+2)}$ and has one output $B_{o(1,2m+1)}$. The 2:1 Mux $B(1,2m+2)$ has two inputs namely $U_{o(1,2m+1)}$ and $U_{o(1,2m+2)}$ and has one output $B_{o(1,2m+2)}$.

The output $F_{o(1,2m-1)}$ of the stage (ring 1, stage "m-1") is connected to the input $F_{i(1,2m+1)}$ of the stage (ring 1, stage "m"), is an internal connection between stage "m-1" and stage "m" of the ring 1. And the output $B_{o(1,2m+1)}$ of the stage (ring 1, stage "m") is connected to the input $U_{i(1,2m-1)}$ of the stage (ring 1, stage "m-1"), is another internal connection between stage "m-1" and stage "m" of the ring 1

Just the same way the stages (ring 1, stage 0), (ring 1, stage 1), there are also stages (ring 1, stage 2), (ring 1, stage 3), ... (ring 1, stage "m-1"), (ring 1, stage "m") in that order, where the stages from (ring 1, stage 2), (ring 1, stage 3), ... , (ring 1, stage "m-2") are not shown in the diagram 100B. Just the same way the two successive stages (ring 1, stage 0) and (ring 1, stage 1) have internal connections between them as described

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

before, any two successive stages have similar internal connections. For example (ring 1, stage 1) and (ring 1, stage 2) have similar internal connections and (ring 1, stage “m-2”) and (ring 1, stage “m-1”) have similar internal connections.

Stage (ring 1, stage 0) is also called hereinafter the “entry stage” or “first stage” of ring 1, since inlet links and outlet links of the computational block are directly connected to stage (ring 1, stage 0). Also stage (ring 1, stage “m”) is hereinafter the “last stage” or “root stage” of ring 1.

The stage (ring 2, stage 0) consists of 4 inputs namely $F_i(2,1)$, $F_i(2,2)$, $U_i(2,1)$, and $U_i(2,2)$; and 4 outputs $B_o(2,1)$, $B_o(2,2)$, $F_o(2,1)$, and $F_o(2,2)$. The stage (ring 2, stage 0) also consists of six 2:1 Muxes namely $F(2,1)$, $F(2,2)$, $U(2,1)$, $U(2,2)$, $B(2,1)$, and $B(2,2)$. The 2:1 Mux $F(2,1)$ has two inputs namely $F_i(2,1)$ and $F_i(2,2)$ and has one output $F_o(2,1)$. The 2:1 Mux $F(2,2)$ has two inputs namely $F_i(2,1)$ and $F_i(2,2)$ and has one output $F_o(2,2)$.

The 2:1 Mux $U(2,1)$ has two inputs namely $U_i(2,1)$ and $F_o(2,1)$ and has one output $U_o(2,1)$. The 2:1 Mux $U(2,2)$ has two inputs namely $U_i(2,2)$ and $F_o(2,2)$ and has one output $U_o(2,2)$. The 2:1 Mux $B(2,1)$ has two inputs namely $U_o(2,1)$ and $U_o(2,2)$ and has one output $B_o(2,1)$. The 2:1 Mux $B(2,2)$ has two inputs namely $U_o(2,1)$ and $U_o(2,2)$ and has one output $B_o(2,2)$.

The stage (ring 2, stage 1) consists of 4 inputs namely $F_i(2,3)$, $F_i(2,4)$, $U_i(2,3)$, and $U_i(2,4)$; and 4 outputs $B_o(2,3)$, $B_o(2,4)$, $F_o(2,3)$, and $F_o(2,4)$. The stage (ring 2, stage 1) also consists of six 2:1 Muxes namely $F(2,3)$, $F(2,4)$, $U(2,3)$, $U(2,4)$, $B(2,3)$, and $B(2,4)$. The 2:1 Mux $F(2,3)$ has two inputs namely $F_i(2,3)$ and $F_i(2,4)$ and has one output $F_o(2,3)$. The 2:1 Mux $F(2,4)$ has two inputs namely $F_i(2,3)$ and $F_i(2,4)$ and has one output $F_o(2,4)$.

The 2:1 Mux $U(2,3)$ has two inputs namely $U_i(2,3)$ and $F_o(2,3)$ and has one output $U_o(2,3)$. The 2:1 Mux $U(2,4)$ has two inputs namely $U_i(2,4)$ and $F_o(2,4)$ and has one output $U_o(2,4)$. The 2:1 Mux $B(2,3)$ has two inputs namely $U_o(2,3)$ and $U_o(2,4)$ and has one output $B_o(2,3)$. The 2:1 Mux $B(2,4)$ has two inputs namely $U_o(2,3)$ and $U_o(2,4)$ and has one output $B_o(2,4)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The output $Fo(2,1)$ of the stage (ring 2, stage 0) is connected to the input $Fi(2,3)$ of the stage (ring 2, stage 1), is an internal connection between stage 0 and stage 1 of the ring 2. And the output $Bo(2,3)$ of the stage (ring 2, stage 1) is connected to the input $Ui(2,1)$ of the stage (ring 2, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1..

The stage (ring 2, stage “n-1”) consists of 4 inputs namely $Ri(2,2n-1)$, $Ri(2,2n)$, $Ui(1,2n-1)$, and $Ui(1,2n)$; and 4 outputs $Bo(1,2n-1)$, $Bo(1,2n)$, $Fo(1,2n-1)$, and $Fo(1,2n)$. The stage (ring 2, stage “n-1”) also consists of eight 2:1 Muxes namely $R(2,2n-1)$, $R(2,2n)$, $F(2,2n-1)$, $F(1,2n)$, $U(1,2n-1)$, $U(1,2n)$, $B(1,2n-1)$, and $B(1,2n)$. The 2:1 Mux $R(2,2n-1)$ has two inputs namely $Ri(2,2n-1)$ and $Bo(2,2n-1)$ and has one output $Ro(2,2n-1)$. The 2:1 Mux $R(2,2n)$ has two inputs namely $Ri(2,2n)$ and $Bo(2,2n)$ and has one output $Ro(2,2n)$. The 2:1 Mux $F(2,2n-1)$ has two inputs namely $Ro(2,2n-1)$ and $Ro(2,2n)$ and has one output $Fo(2,2n-1)$. The 2:1 Mux $F(2,2n)$ has two inputs namely $Ro(2,2n-1)$ and $Ro(2,2n)$ and has one output $Fo(2,2n)$.

The 2:1 Mux $U(2,2n-1)$ has two inputs namely $Ui(2,2n-1)$ and $Fo(2,2n-1)$ and has one output $Uo(2,2n-1)$. The 2:1 Mux $U(2,2n)$ has two inputs namely $Ui(2,2n)$ and $Fo(2,2n)$ and has one output $Uo(2,2n)$. The 2:1 Mux $B(2,2n-1)$ has two inputs namely $Uo(2,2n-1)$ and $Uo(2,2n)$ and has one output $Bo(2,2n-1)$. The 2:1 Mux $B(2,2n)$ has two inputs namely $Uo(2,2n-1)$ and $Uo(2,2n)$ and has one output $Bo(2,2n)$.

The stage (ring 2, stage “n”) consists of 4 inputs namely $Ri(2,2n+1)$, $Ri(2,2n+2)$, $Ui(2,2n+1)$, and $Ui(2,2n+2)$; and 4 outputs $Bo(2,2n+1)$, $Bo(2,2n+2)$, $Fo(2,2n+1)$, and $Fo(2,2n+2)$. The stage (ring 2, stage “n”) also consists of eight 2:1 Muxes namely $R(2,2n+1)$, $R(2,2n+2)$, $F(2,2n+1)$, $F(2,2n+2)$, $U(2,2n+1)$, $U(2,2n+2)$, $B(2,2n+1)$, and $B(2,2n+2)$. The 2:1 Mux $R(2,2n+1)$ has two inputs namely $Ri(2,2n+1)$ and $Bo(2,2n+1)$ and has one output $Ro(2,2n+1)$. The 2:1 Mux $R(2,2n+2)$ has two inputs namely $Ri(2,2n+2)$ and $Bo(2,2n+2)$ and has one output $Ro(2,2n+2)$. The 2:1 Mux $F(2,2n+1)$ has two inputs namely $Ro(2,2n+1)$ and $Ro(2,2n+2)$ and has one output $Fo(2,2n+1)$. The 2:1 Mux $F(2,2n+2)$ has two inputs namely $Ro(2,2n+1)$ and $Ro(2,2n+2)$ and has one output $Fo(2,2n+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux U(2,2n+1) has two inputs namely $U_i(2,2n+1)$ and $F_o(2,2n+1)$ and has one output $U_o(2,2n+1)$. The 2:1 Mux U(2,2n+2) has two inputs namely $U_i(2,2n+2)$ and $F_o(2,2n+2)$ and has one output $U_o(2,2n+2)$. The 2:1 Mux B(2,2n+1) has two inputs namely $U_o(2,2n+1)$ and $U_o(2,2n+2)$ and has one output $B_o(2,2n+1)$. The 2:1 Mux
 5 B(2,2n+2) has two inputs namely $U_o(2,2n+1)$ and $U_o(2,2n+2)$ and has one output $B_o(2,2n+2)$.

The output $F_o(2,2n-1)$ of the stage (ring 2, stage “n-1”) is connected to the input $R_i(2,2n+1)$ of the stage (ring 2, stage “n”), is an internal connection between stage “n-1” and stage “n” of the ring 1. And the output $B_o(2,2n+1)$ of the stage (ring 2, stage “n”) is connected to the input $U_i(2,2n-1)$ of the stage (ring 2, stage “n-1”), is another internal
 10 connection between stage “n-1” and stage “n” of the ring 1.

Each stage of any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of $2 * d = 4$ outputs. Even though each stage has four 4:1 muxes, in other embodiments any of these stages can be one of the four by four
 15 switch diagrams namely 200A of FIG. 2A, 200B of FIG. 2B, 200C of FIG. 2C, and one of the eight by four switch diagrams namely 200E of FIG. 2E, 200F of FIG. 2F.

In general, any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ may have inputs and outputs connected from computational block from either only from left-hand side as in the partial multi-stage hierarchical network
 20 $V_{Comb}(N_1, N_2, d, s)$ 100A; or only from right-hand side; or from both left-hand and right-hand sides as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B.

Referring to diagram 100C in FIG. 1C, in one embodiment, an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ where $N_1 = 400$; $N_2 = 1600$; $d = 2$; and $s = 1$ corresponding to one computational block, with each computational block
 25 having 16 inlet links namely I1, I2, I3, I4, I5, I6, I7, I8, I9, I10, I11, I12, I13, I14, I15, and I16; and 4 outlet links namely O1, O2, O3, and O4. And for each computational block the corresponding partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C consists of two slices namely slice 1 and slice 2. Slice 1 consists of two rings namely

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

(slice 1, ring 1) and (slice 1, ring 2). Similarly slice 2 consists of two rings namely (slice 2, ring 1) and (slice 2, ring 2).

The ring (slice 1, ring 1) consists of “ $m+1$ ” stages namely (slice 1, ring 1, stage 0), (slice 1, ring 1, stage 1), ... (slice 1, ring 1, stage “ $m-1$ ”), and (slice 1, ring 1, stage “ m ”).
 5 And the ring (slice 1, ring 2) consists of “ $n+1$ ” stages namely (slice 1, ring 2, stage 0), (slice 1, ring 2, stage 1), ... (slice 1, ring 2, stage “ $n-1$ ”), and (slice 1, ring 2, stage “ n ”), where “ m ” and “ n ” are positive integers.

Similarly the ring (slice 2, ring 1) consists of “ $x+1$ ” stages namely (slice 2, ring 1, stage 0), (slice 2, ring 1, stage 1), ... (slice 2, ring 1, stage “ $x-1$ ”), and (slice 2, ring 1, stage “ x ”).
 10 And the ring (slice 2, ring 2) consists of “ $y+1$ ” stages namely (slice 2, ring 2, stage 0), (slice 2, ring 2, stage 1), ... (slice 2, ring 2, stage “ $y-1$ ”), and (slice 2, ring 2, stage “ y ”), where “ x ” and “ y ” are positive integers.

In general “ m ” may be or may not be equal to “ x ” and “ n ” may be or may not be equal to “ y ”. Also in general, “ m ” may be or may not be equal to “ n ” and “ x ” may be or
 15 may not be equal to “ y ”.

Ring (slice 1, ring 1) has inlet links $Ri(1,1,1)$ and $Ri(1,1,2)$ from the left-hand side, and has outlet links $Bo(1,1,1)$ and $Bo(1,1,2)$ from left-hand side. Ring (slice 1, ring 1) also has inlet links $Ui(1,1,2m+1)$ and $Ui(1,1,2m+2)$ from the right-hand side, and has outlet links $Fo(1,1,2m+1)$ and $Fo(1,1,2m+2)$ from right-hand side. Ring (slice 1, ring 2)
 20 has inlet links $Ri(1,2,1)$ and $Ri(1,2,2)$ from left-hand side, and outlet links $Bo(1,2,1)$ and $Bo(1,2,2)$ from left-hand side. Ring (slice 1, ring 2) also has inlet links $Ui(1,2,2n+1)$ and $Ui(1,2,2n+2)$ from the right-hand side, and has outlet links $Fo(1,2,2n+1)$ and $Fo(1,2,2n+2)$ from right-hand side.

Ring (slice 2, ring 1) has inlet links $Ri(2,1,1)$ and $Ri(2,1,2)$ from the left-hand side, and has outlet links $Bo(2,1,1)$ and $Bo(2,1,2)$ from left-hand side. Ring (slice 2, ring 1) also has inlet links $Ui(2,1,2x+1)$ and $Ui(2,1,2x+2)$ from the right-hand side, and has outlet links $Fo(2,1,2x+1)$ and $Fo(2,1,2x+2)$ from right-hand side. Ring (slice 2, ring 2)
 25 has inlet links $Ri(2,2,1)$ and $Ri(2,2,2)$ from left-hand side, and outlet links $Bo(2,2,1)$ and $Bo(2,2,2)$ from left-hand side. Ring (slice 2, ring 2) also has inlet links $Ui(2,2,2y+1)$ and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$U_i(2,2,2y+2)$ from the right-hand side, and has outlet links $F_o(2,2,2y+1)$ and $F_o(2,2,2y+2)$ from right-hand side.

And the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C consists of 16 inlet links and 4 outlet links corresponding to the two slices slice 1 and slice 2.

5 From left-hand side, outlet link O1 of the computational block is connected to inlet link $R_i(1,1,1)$ of ring (slice 1, ring 1) and also inlet link of $R_i(1,2,1)$ of ring (slice 1, ring 2). Similarly from left-hand side, outlet link O2 of the computational block is connected to inlet link $R_i(1,1,2)$ of Ring (slice 1, ring 1) and also inlet link of $R_i(1,2,2)$ of Ring (slice 1, ring 2). And from left-hand side, outlet link $B_o(1,1,1)$ of Ring (slice 1, ring 1) is
 10 connected to inlet link I1 of the computational block. From left-hand side, Outlet link $B_o(1,1,2)$ of Ring (slice 1, ring 1) is connected to inlet link I2 of the computational block. Similarly from left-hand side, outlet link $B_o(1,2,1)$ of Ring (slice 1, ring 2) is connected to inlet link I3 of the computational block. From left-hand side, outlet link $B_o(1,2,2)$ of Ring (slice 1, ring 2) is connected to inlet link I4 of the computational block.

15 From right-hand side, outlet link O1 of the computational block is connected to inlet link $U_i(1,1,2m+1)$ of ring (slice 1, ring 1) and also inlet link of $U_i(1,2,2n+1)$ of ring (slice 1, ring 2). Similarly from right-hand side, outlet link O2 of the computational block is connected to inlet link $U_i(1,1,2m+2)$ of Ring (slice 1, ring 1) and also inlet link of $U_i(1,2,2n+2)$ of Ring (slice 1, ring 2). And from right-hand side, outlet link $F_o(1,1,2m+1)$
 20 of Ring (slice 1, ring 1) is connected to inlet link I5 of the computational block. From right-hand side, outlet link $F_o(1,1,2m+2)$ of Ring (slice 1, ring 1) is connected to inlet link I6 of the computational block. Similarly from right-hand side, outlet link $F_o(1,2,2n+1)$ of Ring (slice 1, ring 2) is connected to inlet link I7 of the computational block. From right-hand side, outlet link $F_o(1,2,2n+2)$ of Ring (slice 1, ring 2) is
 25 connected to inlet link I8 of the computational block.

From left-hand side, outlet link O3 of the computational block is connected to inlet link $R_i(2,1,1)$ of ring (slice 2, ring 1) and also inlet link of $R_i(2,2,1)$ of ring (slice 2, ring 2). Similarly from left-hand side, outlet link O4 of the computational block is connected to inlet link $R_i(2,1,2)$ of Ring (slice 2, ring 1) and also inlet link of $R_i(2,2,2)$ of
 30 Ring (slice 2, ring 2). And from left-hand side, outlet link $B_o(2,1,1)$ of Ring (slice 2, ring 1) is connected to inlet link I9 of the computational block. From left-hand side, Outlet

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

link Bo(2,1,2) of Ring (slice 2, ring 1) is connected to inlet link I10 of the computational block. Similarly from left-hand side, outlet link Bo(2,2,1) of Ring (slice 2, ring 2) is connected to inlet link I11 of the computational block. From left-hand side, outlet link Bo(2,2,2) of Ring (slice 2, ring 2) is connected to inlet link I12 of the computational
5 block.

From right-hand side, outlet link O3 of the computational block is connected to inlet link Ui(2,1,2x+1) of ring (slice 2, ring 1) and also inlet link of Ui(2,2,2y+1) of ring (slice 2, ring 2). Similarly from right-hand side, outlet link O4 of the computational block is connected to inlet link Ui(2,1,2x+2) of Ring (slice 2, ring 1) and also inlet link of
10 Ui(2,2,2y+2) of Ring (slice 2, ring 2). And from right-hand side, outlet link Fo(2,1,2x+1) of Ring (slice 2, ring 1) is connected to inlet link I13 of the computational block. From right-hand side, outlet link Fo(2,1,2x+2) of Ring (slice 2, ring 1) is connected to inlet link I14 of the computational block. Similarly from right-hand side, outlet link Fo(2,2,2y+1) of Ring (slice 2, ring 2) is connected to inlet link I15 of the computational block. From
15 right-hand side, outlet link Fo(2,2,2y+2) of Ring (slice 2, ring 2) is connected to inlet link I16 of the computational block.

In this embodiment outlet links O1 and O2 of the computational block are connected only to slice 1. Similarly outlet links O3 and O4 of the computational block are connected only to slice 2.

Referring to two dimensional grid 800 in FIG. 8 illustrates, in another
20 embodiment, each block of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C with 4 inlet links and 16 outlet links and the corresponding computational block with 16 inlet links and 4 outlet links. For example block (1,1) of 2D-grid 800 consists of one of the partial multi-stage hierarchical network
25 $V_{Comb}(N_1, N_2, d, s)$ 100C with 4 inlet links and 16 outlet links and the corresponding computational block with 16 inlet links and 4 outlet links. Similarly each of the 100 blocks of 2D-grid 800 has a separate partial multi-stage hierarchical network
 $V_{Comb}(N_1, N_2, d, s)$ 100C with 4 inlet links and 16 outlet links and the corresponding
computational block with 16 inlet links and 4 outlet links. Hence the complete multi-stage
30 hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to 2D-grid 800 has $N_1 = 400$ inlet

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

links and $N_2 = 1600$ outlet links. Since there are 100 computational blocks each one corresponding to one of the blocks with each computational block having 16 inlet links and 4 outlet links. Also the 2D-grid 800 is organized in the fourth quadrant of the 2D-Plane. In other embodiments the 2D-grid 800 may be organized as either first quadrant, or
 5 second quadrant or third quadrant of the 2D-Plane.

Referring to partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C, the stage (slice 1, ring 1, stage 0) consists of 8 inputs namely $Ri(1,1,1)$, $Ri(1,1,2)$, $Ui(1,1,1)$, $Ui(1,1,2)$, $J(1,1,1)$, $K(1,1,1)$, $L(1,1,1)$, and $M(1,1,1)$; and 4 outputs $Bo(1,1,1)$, $Bo(1,1,2)$, $Fo(1,1,1)$, and $Fo(1,1,2)$. The stage (slice 1, ring “1”, stage “0”) also
 10 consists of four 4:1 Muxes namely $F(1,1,1)$, $F(1,1,2)$, $B(1,1,1)$, and $B(1,1,2)$. The 4:1 Mux $F(1,1,1)$ has four inputs namely $Ri(1,1,1)$, $Ri(1,1,2)$, $Ui(1,1,2)$, and $J(1,1,1)$, and has one output $Fo(1,1,1)$. The 4:1 Mux $F(1,1,2)$ has four inputs namely $Ri(1,1,1)$, $Ri(1,1,2)$, $Ui(1,1,1)$, and $K(1,1,1)$, and has one output $Fo(1,1,2)$.

The 4:1 Mux $B(1,1,1)$ has four inputs namely $Ui(1,1,1)$, $Ui(1,1,2)$, $Ri(1,1,2)$, and
 15 $L(1,1,1)$, and has one output $Bo(1,1,1)$. The 4:1 Mux $B(1,1,2)$ has four inputs namely $Ui(1,1,1)$, $Ui(1,1,2)$, $Ri(1,1,1)$ and $M(1,1,1)$, and has one output $Bo(1,1,2)$. In different embodiments the inputs $J(1,1,1)$, $K(1,1,1)$, $L(1,1,1)$, and $M(1,1,1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 1, ring 1, stage “m”) consists of 8 inputs namely $Ri(1,1,2m+1)$,
 20 $Ri(1,1,2m+2)$, $Ui(1,1,2m+1)$, $Ui(1,1,2m+2)$, $J(1,1,m+1)$, $K(1,1,m+1)$, $L(1,1,m+1)$, and $M(1,1,m+1)$; and 4 outputs $Bo(1,1,2m+1)$, $Bo(1,1,2m+2)$, $Fo(1,1,2m+1)$, and $Fo(1,1,2m+2)$. The stage (slice 1, ring 1, stage “m”) also consists of four 4:1 Muxes namely $F(1,1,2m+1)$, $F(1,1,2m+2)$, $B(1,1,2m+1)$, and $B(1,1,2m+2)$. The 4:1 Mux
 25 $F(1,1,2m+1)$ has four inputs namely $Ri(1,1,2m+1)$, $Ri(1,1,2m+2)$, $Ui(1,1,2m+2)$, and $J(1,1,m+1)$, and has one output $Fo(1,1,2m+1)$. The 4:1 Mux $F(1,1,2m+2)$ has four inputs namely $Ri(1,1,2m+1)$, $Ri(1,1,2m+2)$, $Ui(1,1,2m+1)$, and $K(1,1,m+1)$, and has one output $Fo(1,1,2m+2)$.

The 4:1 Mux $B(1,1,2m+1)$ has four inputs namely $Ui(1,1,2m+1)$, $Ui(1,1,2m+2)$,
 30 $Ri(1,1,2m+2)$, and $L(1,1,m+1)$, and has one output $Bo(1,1,2m+1)$. The 4:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

B(1,1,2m+2) has four inputs namely $U_i(1,1,2m+1)$, $U_i(1,1,2m+2)$, $R_i(1,1,2m+1)$ and $M(1,1,m+1)$, and has one output $Bo(1,1,2m+2)$. In different embodiments the inputs $J(1,1,m+1)$, $K(1,1,m+1)$, $L(1,1,m+1)$, and $M(1,1,m+1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical
 5 network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 1, ring 1, stage 0), there are also stages (slice 1, ring 1, stage 1), (slice 1, ring 1, stage 2), (slice 1, ring 1, stage 3), ... (slice 1, ring 1, stage "m-1"), (slice 1, ring 1, stage "m") in that order, where the stages from (slice 1, ring 1, stage 1), (slice 1, ring 1, stage 2), ... , (slice 1, ring 1, stage "m-1") are not shown in the
 10 diagram 100C.

Referring to diagram 100C5 in FIG. 1C5 illustrates specific details of partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C, particularly the internal connections between two successive stages of any ring of any slice, in one embodiment. The stage (slice "c", ring "d", stage "e") consists of 8 inputs namely
 15 $R_i(c,d,2e+1)$, $R_i(c,d,2e+2)$, $U_i(c,d,2e+1)$, $U_i(c,d,2e+2)$, $J(c,d,e+1)$, $K(c,d,e+1)$, $L(c,d,e+1)$, and $M(c,d,e+1)$; and 4 outputs $Bo(c,d,2e+1)$, $Bo(c,d,2e+2)$, $Fo(c,d,2e+1)$, and $Fo(c,d,2e+2)$. The stage (slice "c", ring "d", stage "e") also consists of four 4:1 Muxes namely $F(c,d,2e+1)$, $F(c,d,2e+2)$, $B(c,d,2e+1)$, and $B(c,d,2e+2)$. The 4:1 Mux $F(c,d,2e+1)$ has four inputs namely $R_i(c,d,2e+1)$, $R_i(c,d,2e+2)$, $U_i(c,d,2e+2)$, and $J(c,d,e+1)$, and has
 20 one output $Fo(c,d,2e+1)$. The 4:1 Mux $F(c,d,2e+2)$ has four inputs namely $R_i(c,d,2e+1)$, $R_i(c,d,2e+2)$, $U_i(c,d,2e+1)$, and $K(c,d,e+1)$, and has one output $Fo(c,d,2e+2)$.

The 4:1 Mux $B(c,d,2e+1)$ has four inputs namely $U_i(c,d,2e+1)$, $U_i(c,d,2e+2)$, $R_i(c,d,2e+2)$, and $L(c,d,e+1)$, and has one output $Bo(c,d,2e+1)$. The 4:1 Mux $B(c,d,2e+2)$ has four inputs namely $U_i(c,d,2e+1)$, $U_i(c,d,2e+2)$, $R_i(c,d,2e+1)$ and $M(c,d,e+1)$, and has
 25 one output $Bo(c,d,2e+2)$. In different embodiments the inputs $J(c,d,e+1)$, $K(c,d,e+1)$, $L(c,d,e+1)$, and $M(c,d,e+1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice "c", ring "d", stage "e+1") consists of 8 inputs namely
 30 $R_i(c,d,2e+3)$, $R_i(c,d,2e+4)$, $U_i(c,d,2e+3)$, $U_i(c,d,2e+4)$, $J(c,d,e+2)$, $K(c,d,e+2)$, $L(c,d,e+2)$, and $M(c,d,e+2)$; and 4 outputs $Bo(c,d,2e+3)$, $Bo(c,d,2e+4)$, $Fo(c,d,2e+3)$, and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Fo(c,d,2e+4). The stage (slice “c”, ring “d”, stage “e+1”) also consists of four 4:1 Muxes namely F(c,d,2e+3), F(c,d,2e+4), B(c,d,2e+3), and B(c,d,2e+4). The 4:1 Mux F(c,d,2e+3) has four inputs namely Ri(c,d,2e+3), Ri(c,d,2e+4), Ui(c,d,2e+4), and J(c,d,e+2), and has one output Fo(c,d,2e+3). The 4:1 Mux F(c,d,2e+4) has four inputs namely Ri(c,d,2e+3),
 5 Ri(c,d,2e+4), Ui(c,d,2e+3), and K(c,d,e+2), and has one output Fo(c,d,2e+4).

The 4:1 Mux B(c,d,2e+3) has four inputs namely Ui(c,d,2e+3), Ui(c,d,2e+4), Ri(c,d,2e+4), and L(c,d,e+2), and has one output Bo(c,d,2e+3). The 4:1 Mux B(c,d,2e+4) has four inputs namely Ui(c,d,2e+3), Ui(c,d,2e+4), Ri(c,d,2e+3) and M(c,d,e+2), and has one output Bo(c,d,2e+4). In different embodiments the inputs J(c,d,e+2), K(c,d,e+2),
 10 L(c,d,e+2), and M(c,d,e+2) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The output Fo(c,d,2e+1) of the stage (slice “c”, ring “d”, stage “e”) is connected to the input Ri(c,d,2e+3) of the stage (slice “c”, ring “d”, stage “e+1”) which is called hereinafter an internal connection between two successive stages of a ring. And the
 15 output Bo(c,d,2e+3) of the stage (slice “c”, ring “d”, stage “e+1”) is connected to the input Ui(c,d,2e+1) of the stage (slice “c”, ring “d”, stage “e”), is another internal connection between stage “e” and stage “e+1” of the ring (slice “c”, ring “d”).

Just the same way the two successive stages (slice “c”, ring “d”, stage “e”) and (slice “c”, ring “d”, stage “e+1”) have internal connections between them as described
 20 above, any two successive stages have similar internal connections for any values of “c”, “d”, “e” of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C belonging to any block of the two dimensional grid 800 in FIG. 8, in some embodiments. For example stage (slice 1, ring 1, stage 0) and stage (slice 1, ring 1, stage 1) have similar internal connections; and stage (slice 1, ring 1, stage “m-1”) and stage
 25 (slice 1, ring 1, stage “m”) have similar internal connections.

Stage (slice 1, ring 1, stage 0) is also called hereinafter the “entry stage” or “first stage” of (slice 1, ring 1), since inlet links and outlet links of the computational block are directly connected to stage (slice 1, ring 1, stage 0). Also stage (slice 1, ring 1, stage “m”) is hereinafter the “last stage” or “root stage” of (slice 1, ring 1).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The stage (slice 1, ring 2, stage 0) consists of 8 inputs namely $Ri(1,2,1)$, $Ri(1,2,2)$, $Ui(1,2,1)$, $Ui(1,2,2)$, $J(1,2,1)$, $K(1,2,1)$, $L(1,2,1)$, and $M(1,2,1)$; and 4 outputs $Bo(1,2,1)$, $Bo(1,2,2)$, $Fo(1,2,1)$, and $Fo(1,2,2)$. The stage (slice 1, ring “2”, stage “0”) also consists of four 4:1 Muxes namely $F(1,2,1)$, $F(1,2,2)$, $B(1,2,1)$, and $B(1,2,2)$. The 4:1 Mux

5 $F(1,2,1)$ has four inputs namely $Ri(1,2,1)$, $Ri(1,2,2)$, $Ui(1,2,2)$, and $J(1,2,1)$, and has one output $Fo(1,2,1)$. The 4:1 Mux $F(1,2,2)$ has four inputs namely $Ri(1,2,1)$, $Ri(1,2,2)$, $Ui(1,2,1)$, and $K(1,2,1)$, and has one output $Fo(1,2,2)$.

The 4:1 Mux $B(1,2,1)$ has four inputs namely $Ui(1,2,1)$, $Ui(1,2,2)$, $Ri(1,2,2)$, and $L(1,2,1)$, and has one output $Bo(1,2,1)$. The 4:1 Mux $B(1,2,2)$ has four inputs namely

10 $Ui(1,2,1)$, $Ui(1,2,2)$, $Ri(1,2,1)$ and $M(1,2,1)$, and has one output $Bo(1,2,2)$. In different embodiments the inputs $J(1,2,1)$, $K(1,2,1)$, $L(1,2,1)$, and $M(1,2,1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 1, ring 2, stage “n”) consists of 8 inputs namely $Ri(1,2,2n+1)$,

15 $Ri(1,2,2n+2)$, $Ui(1,2,2n+1)$, $Ui(1,2,2n+2)$, $J(1,2,n+1)$, $K(1,2,n+1)$, $L(1,2,n+1)$, and $M(1,2,n+1)$; and 4 outputs $Bo(1,2,2n+1)$, $Bo(1,2,2n+2)$, $Fo(1,2,2n+1)$, and $Fo(1,2,2n+2)$. The stage (slice 1, ring 2, stage “n”) also consists of four 4:1 Muxes namely $F(1,2,2n+1)$, $F(1,2,2n+2)$, $B(1,2,2n+1)$, and $B(1,2,2n+2)$. The 4:1 Mux $F(1,2,2n+1)$ has four inputs namely $Ri(1,2,2n+1)$, $Ri(1,2,2n+2)$, $Ui(1,2,2n+2)$, and $J(1,2,n+1)$, and has one output

20 $Fo(1,2,2n+1)$. The 4:1 Mux $F(1,2,2n+2)$ has four inputs namely $Ri(1,2,2n+1)$, $Ri(1,2,2n+2)$, $Ui(1,2,2n+1)$, and $K(1,2,n+1)$, and has one output $Fo(1,2,2n+2)$.

The 4:1 Mux $B(1,2,2n+1)$ has four inputs namely $Ui(1,2,n+1)$, $Ui(1,2,2n+2)$, $Ri(1,2,2n+2)$, and $L(1,2,n+1)$, and has one output $Bo(1,2,2n+1)$. The 4:1 Mux

25 $B(1,2,2n+2)$ has four inputs namely $Ui(1,2,2n+1)$, $Ui(1,2,2n+2)$, $Ri(1,2,2n+1)$ and $M(1,2,n+1)$, and has one output $Bo(1,2,2n+2)$. In different embodiments the inputs $J(1,2,n+1)$, $K(1,2,n+1)$, $L(1,2,n+1)$, and $M(1,2,n+1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 1, ring 2, stage 0), there are also stages (slice 1,

30 ring 2, stage 1), (slice 1, ring 2, stage 2), (slice 1, ring 2, stage 3), ... (slice 1, ring 2, stage

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

“n-1”), (slice 1, ring 2, stage “n”) in that order, where the stages from (slice 1, ring 2, stage 1), (slice 1, ring 2, stage 2), ... , (slice 1, ring 2, stage “n-1”) are not shown in the diagram 100C.

The stage (slice 2, ring 1, stage 0) consists of 8 inputs namely $R_i(2,1,1)$, $R_i(2,1,2)$,
 5 $U_i(2,1,1)$, $U_i(2,1,2)$, $J(2,1,1)$, $K(2,1,1)$, $L(2,1,1)$, and $M(2,1,1)$; and 4 outputs $B_o(2,1,1)$,
 $B_o(2,1,2)$, $F_o(2,1,1)$, and $F_o(2,1,2)$. The stage (slice 2, ring “1”, stage “0”) also consists
 of four 4:1 Muxes namely $F(2,1,1)$, $F(2,1,2)$, $B(2,1,1)$, and $B(2,1,2)$. The 4:1 Mux
 $F(2,1,1)$ has four inputs namely $R_i(2,1,1)$, $R_i(2,1,2)$, $U_i(2,1,2)$, and $J(2,1,1)$, and has one
 output $F_o(2,1,1)$. The 4:1 Mux $F(2,1,2)$ has four inputs namely $R_i(2,1,1)$, $R_i(2,1,2)$,
 10 $U_i(2,1,1)$, and $K(2,1,1)$, and has one output $F_o(2,1,2)$.

The 4:1 Mux $B(2,1,1)$ has four inputs namely $U_i(2,1,1)$, $U_i(2,1,2)$, $R_i(2,1,2)$, and
 $L(2,1,1)$, and has one output $B_o(2,1,1)$. The 4:1 Mux $B(2,1,2)$ has four inputs namely
 $U_i(2,1,1)$, $U_i(2,1,2)$, $R_i(2,1,1)$ and $M(2,1,1)$, and has one output $B_o(2,1,2)$. In different
 embodiments the inputs $J(2,1,1)$, $K(2,1,1)$, $L(2,1,1)$, and $M(2,1,1)$ are connected from any
 15 of the outputs of any other stages of any ring of any block of the multi-stage hierarchical
 network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 2, ring 1, stage “x”) consists of 8 inputs namely $R_i(2,1,2x+1)$,
 $R_i(2,1,2x+2)$, $U_i(2,1,2x+1)$, $U_i(2,1,2x+2)$, $J(2,1,x+1)$, $K(2,1,x+1)$, $L(2,1,x+1)$, and
 $M(2,1,x+1)$; and 4 outputs $B_o(2,1,2x+1)$, $B_o(2,1,2x+2)$, $F_o(2,1,2x+1)$, and $F_o(2,1,2x+2)$.
 20 The stage (slice 2, ring 1, stage “x”) also consists of four 4:1 Muxes namely $F(2,1,2x+1)$,
 $F(2,1,2x+2)$, $B(2,1,2x+1)$, and $B(2,1,2x+2)$. The 4:1 Mux $F(2,1,2x+1)$ has four inputs
 namely $R_i(2,1,2x+1)$, $R_i(2,1,2x+2)$, $U_i(2,1,2x+2)$, and $J(2,1,x+1)$, and has one output
 $F_o(2,1,2x+1)$. The 4:1 Mux $F(2,1,2x+2)$ has four inputs namely $R_i(2,1,2x+1)$,
 $R_i(2,1,2x+2)$, $U_i(2,1,2x+1)$, and $K(2,1,x+1)$, and has one output $F_o(2,1,2x+2)$.

25 The 4:1 Mux $B(2,1,2x+1)$ has four inputs namely $U_i(2,1,2x+1)$, $U_i(2,1,2x+2)$,
 $R_i(2,1,2x+2)$, and $L(2,1,x+1)$, and has one output $B_o(2,1,2x+1)$. The 4:1 Mux
 $B(2,1,2x+2)$ has four inputs namely $U_i(2,1,2x+1)$, $U_i(2,1,2x+2)$, $R_i(2,1,2x+1)$ and
 $M(2,1,x+1)$, and has one output $B_o(2,1,2x+2)$. In different embodiments the inputs
 $J(2,1,x+1)$, $K(2,1,x+1)$, $L(2,1,x+1)$, and $M(2,1,x+1)$ are connected from any of the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 2, ring 1, stage 0), there are also stages (slice 2, ring 1, stage 1), (slice 2, ring 1, stage 2), (slice 2, ring 1, stage 3), ... (slice 2, ring 1, stage "m-1"), (slice 2, ring 1, stage "x") in that order, where the stages from (slice 2, ring 1, stage 1), (slice 2, ring 1, stage 2), ... , (slice 2, ring 1, stage "x-1") are not shown in the diagram 100C.

The stage (slice 2, ring 2, stage 0) consists of 8 inputs namely $Ri(2,2,1)$, $Ri(2,2,2)$, $Ui(2,2,1)$, $Ui(2,2,2)$, $J(2,2,1)$, $K(2,2,1)$, $L(2,2,1)$, and $M(2,2,1)$; and 4 outputs $Bo(2,2,1)$, $Bo(2,2,2)$, $Fo(2,2,1)$, and $Fo(2,2,2)$. The stage (slice 2, ring "2", stage "0") also consists of four 4:1 Muxes namely $F(2,2,1)$, $F(2,2,2)$, $B(2,2,1)$, and $B(2,2,2)$. The 4:1 Mux $F(2,2,1)$ has four inputs namely $Ri(2,2,1)$, $Ri(2,2,2)$, $Ui(2,2,2)$, and $J(2,2,1)$, and has one output $Fo(2,2,1)$. The 4:1 Mux $F(2,2,2)$ has four inputs namely $Ri(2,2,1)$, $Ri(2,2,2)$, $Ui(2,2,1)$, and $K(2,2,1)$, and has one output $Fo(2,2,2)$.

The 4:1 Mux $B(2,2,1)$ has four inputs namely $Ui(2,2,1)$, $Ui(2,2,2)$, $Ri(2,2,2)$, and $L(2,2,1)$, and has one output $Bo(2,2,1)$. The 4:1 Mux $B(2,2,2)$ has four inputs namely $Ui(2,2,1)$, $Ui(2,2,2)$, $Ri(2,2,1)$ and $M(2,2,1)$, and has one output $Bo(2,2,2)$. In different embodiments the inputs $J(2,2,1)$, $K(2,2,1)$, $L(2,2,1)$, and $M(2,2,1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 2, ring 2, stage "x") consists of 8 inputs namely $Ri(2,2,2x+1)$, $Ri(2,2,2x+2)$, $Ui(2,2,2x+1)$, $Ui(2,2,2x+2)$, $J(2,2,x+1)$, $K(2,2,x+1)$, $L(2,2,x+1)$, and $M(2,2,x+1)$; and 4 outputs $Bo(2,2,2x+1)$, $Bo(2,2,2x+2)$, $Fo(2,2,2x+1)$, and $Fo(2,2,2x+2)$. The stage (slice 2, ring 2, stage "y") also consists of four 4:1 Muxes namely $F(2,2,2y+1)$, $F(2,2,2y+2)$, $B(2,2,2y+1)$, and $B(2,2,2y+2)$. The 4:1 Mux $F(2,2,2y+1)$ has four inputs namely $Ri(2,2,2y+1)$, $Ri(2,2,2y+2)$, $Ui(2,2,2y+2)$, and $J(2,2,y+1)$, and has one output $Fo(2,2,2y+1)$. The 4:1 Mux $F(2,2,2y+2)$ has four inputs namely $Ri(2,2,2y+1)$, $Ri(2,2,2y+2)$, $Ui(2,2,2y+1)$, and $K(2,2,y+1)$, and has one output $Fo(2,2,2y+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 4:1 Mux B(2,2,2y+1) has four inputs namely $U_i(2,2,2y+1)$, $U_i(2,2,2y+2)$, $R_i(2,2,2y+2)$, and $L(2,2,y+1)$, and has one output $Bo(2,2,2y+1)$. The 4:1 Mux B(2,2,2y+2) has four inputs namely $U_i(2,2,2y+1)$, $U_i(2,2,2y+2)$, $R_i(2,2,2y+1)$ and $M(2,2,y+1)$, and has one output $Bo(2,2,2y+2)$. In different embodiments the inputs
 5 J(2,2,y+1), K(2,2,y+1), L(2,2,y+1), and M(2,2,y+1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 2, ring 2, stage 0), there are also stages (slice 2, ring 2, stage 1), (slice 2, ring 2, stage 2), (slice 2, ring 2, stage 3), ... (slice 2, ring 2, stage
 10 "y-1"), (slice 2, ring 2, stage "y") in that order, where the stages from (slice 2, ring 2, stage 1), (slice 2, ring 2, stage 2), ... , (slice 2, ring 2, stage "y-1") are not shown in the diagram 100C.

As illustrated in diagram 100C5 in FIG. 1C5, the similar internal connections between two successive stages of any ring of any slice of partial multi-stage hierarchical
 15 network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C, in some embodiments are provided for all the slices $c = 1, 2$; for all the rings in each of the slices $d = 1, 2$; and for all the stages namely when $c = 1, d = 1, e = [1, m]$; when $c=1, d=2, e=[1, n]$; when $c=2, d=1, e=[1, x]$; and when $c=2, d=2; e=[1, y]$.

Each stage of any ring of the partial multi-stage hierarchical network
 20 $V_{Comb}(N_1, N_2, d, s)$ 100B consists of $2 * d = 4$ outputs. Even though each stage has four 4:1 muxes, in other embodiments any of these stages can be one of the four by four switch diagrams namely 200A of FIG. 2A, 200B of FIG. 2B, 200C of FIG. 2C, and one of the eight by four switch diagrams namely 200E of FIG. 2E, 200F of FIG. 2F.

In general, any ring of the partial multi-stage hierarchical network
 25 $V_{Comb}(N_1, N_2, d, s)$ illustrated in 100C also may have inputs and outputs connected from computational block from either only from left-hand side as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A; or only from right-hand side; or from both left-hand and right-hand sides as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Applicant now notes a few aspects of the diagram 100C in FIG. 1C an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to one computational block, with each computational block having 16 inlet links and 4 outlet links as follows: (Also these aspects are helpful in more optimization of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ as well as faster scheduling of the connections between outlet links of the computational blocks and the inlet links of the computational blocks.)

1) The partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C is divided into two slices namely slice 1 and slice 2. The outlet links of the computational block namely O1 and O2 are connected to only one slice i.e. slice 1. In other words outlet links O1 and O2 are absolutely not connected to slice 2. Similarly the outlet links of the computational block namely O3 and O4 are connected to only one slice i.e. slice 2. In other words outlet links O3 and O4 are absolutely not connected to slice 1.

2) The second aspect is all the hop wires and multi-drop hop wires originating from slice 1 from any block will be terminating only in the slice 1 of any other block. Similarly all the hop wires and multi-drop hop wires originating from slice 2 from any block will be terminating only in the slice 2 of any other block.

3) The third aspect is the mux whose output is directly connected to each inlet link of the computational block must have at least one input connected from each slice of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C. That is for example since the 4:1 mux B(1,1,1), belonging to slice 1, and having its output Bo(1,1,1) directly connected to inlet link I1 must have at least one of its inputs connecting from an output of a mux of a stage of a ring of slice 2 as well. This property must be satisfied for all the inlet links of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C.

Referring to diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 illustrate the details of the foregoing third aspect of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C. Applicant notes that diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 are all actually part of the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C and these separate diagrams are necessary only to avoid the clutter in the diagram 100C of FIG. 1C.

The connections illustrated between different slices in diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 are the only connections between different slices, in some exemplary embodiments. In general the connections between different slices are given only at the terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block.

Referring to diagram 100C1 in FIG. 1C1 illustrate the connections between the stage (slice 1, ring 1, stage 0) and between the stage (slice 2, ring 1, stage 0). The same connection that is given to the input $U_i(1,1,1)$ is also connected to the input $L(2,1,1)$. The same connection that is given to the input $U_i(1,1,2)$ is also connected to the input $M(2,1,1)$. Similarly the same connection that is given to the input $U_i(2,1,1)$ is also connected to the input $L(1,1,1)$. The same connection that is given to the input $U_i(2,1,2)$ is also connected to the input $M(1,1,1)$.

Therefore inlet link I1 can be essentially connected through the 4:1 mux $B(1,1,1)$ with three of its inputs connecting from slice 1 namely $U_i(1,1,1)$, $U_i(1,1,2)$, $R_i(1,1,2)$ and one input $L(1,1,1)$ connecting from slice 2. The inlet link I2 can be essentially connected through the 4:1 mux $B(1,1,2)$ with three of its inputs connecting from slice 1 namely $U_i(1,1,1)$, $U_i(1,1,2)$, $R_i(1,1,1)$ and one input $M(1,1,1)$ connecting from slice 2. The inlet link I9 can be essentially connected through the 4:1 mux $B(1,2,1)$ with three of its inputs connecting from slice 2 namely $U_i(2,1,1)$, $U_i(2,1,2)$, $R_i(2,1,2)$ and one input $L(2,1,1)$ connecting from slice 1. The inlet link I10 can be essentially connected through the 4:1 mux $B(2,1,2)$ with three of its inputs connecting from slice 2 namely $U_i(2,1,1)$, $U_i(2,1,2)$, $R_i(2,1,1)$ and one input $M(2,1,1)$ connecting from slice 1. Hence all the inlet links I1, I2, I9 and I10 are all independently reachable from both slice 1 and slice2.

Referring to diagram 100C2 in FIG. 1C2 illustrate the connections between the stage (slice 1, ring 2, stage 0) and between the stage (slice 2, ring 2, stage 0). The same connection that is given to the input $U_i(1,2,1)$ is also connected to the input $M(2,2,1)$. The same connection that is given to the input $U_i(1,2,2)$ is also connected to the input

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

L(2,2,1). Similarly the same connection that is given to the input $U_i(2,2,1)$ is also connected to the input $M(1,2,1)$. The same connection that is given to the input $U_i(2,2,2)$ is also connected to the input $L(1,2,1)$.

Therefore inlet link I3 can be essentially connected through the 4:1 mux B(1,2,1) with three of its inputs connecting from slice 1 namely $U_i(1,2,1)$, $U_i(1,2,2)$, $R_i(1,2,2)$ and one input $M(2,2,1)$ connecting from slice 2. The inlet link I4 can be essentially connected through the 4:1 mux B(1,2,2) with three of its inputs connecting from slice 1 namely $U_i(1,2,1)$, $U_i(1,2,2)$, $R_i(1,2,1)$ and one input $M(1,2,1)$ connecting from slice 2. The inlet link I11 can be essentially connected through the 4:1 mux B(2,2,1) with three of its inputs connecting from slice 2 namely $U_i(2,2,1)$, $U_i(2,2,2)$, $R_i(2,2,2)$ and one input $L(2,2,1)$ connecting from slice 1. The inlet link I12 can be essentially connected through the 4:1 mux B(2,2,2) with three of its inputs connecting from slice 2 namely $U_i(2,2,1)$, $U_i(2,2,2)$, $R_i(2,2,1)$ and one input $M(2,2,1)$ connecting from slice 1. Hence all the inlet links I3, I4, I11 and I12 are all independently reachable from both slice 1 and slice2.

Referring to diagram 100C3 in FIG. 1C3 illustrate the connections between the stage (slice 1, ring 1, stage "m") and between the stage (slice 2, ring 2, stage "y"). The same connection that is given to the input $R_i(1,1,2m+1)$ is also connected to the input $J(2,2,y+1)$. The same connection that is given to the input $R_i(1,1,2m+2)$ is also connected to the input $K(2,2,y+1)$. Similarly the same connection that is given to the input $R_i(2,2,2y+1)$ is also connected to the input $J(1,1,m+1)$. The same connection that is given to the input $R_i(2,2,2y+2)$ is also connected to the input $K(1,1,m+1)$.

Therefore inlet link I5 can be essentially connected through the 4:1 mux F(1,1,2m+1) with three of its inputs connecting from slice 1 namely $R_i(1,1,2m+1)$, $R_i(1,1,2m+2)$, $U_i(1,1,2m+2)$ and one input $J(1,1,m+1)$ connecting from slice 2. The inlet link I6 can be essentially connected through the 4:1 mux F(1,1,2m+2) with three of its inputs connecting from slice 1 namely $R_i(1,1,2m+1)$, $R_i(1,1,2m+2)$, $U_i(1,1,2m+1)$ and one input $K(1,1,m+1)$ connecting from slice 2. The inlet link I15 can be essentially connected through the 4:1 mux F(2,2,2y+1) with three of its inputs connecting from slice 2 namely $R_i(2,2,2y+1)$, $R_i(2,2,2y+2)$, $U_i(2,2,2y+2)$ and one input $J(2,2,y+1)$ connecting from slice 1. The inlet link I16 can be essentially connected through the 4:1 mux F(2,2,2y+2) with three of its inputs connecting from slice 2 namely $R_i(2,2,2y+1)$,

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$R_i(2,2,2y+2)$, $U_i(2,2,2y+1)$ and one input $K(2,2,y+1)$ connecting from slice 1. Hence all the inlet links I5, I6, I15 and I16 are all independently reachable from both slice 1 and slice2.

Referring to diagram 100C4 in FIG. 1C4 illustrate the connections between the stage (slice 1, ring 2, stage "n") and between the stage (slice 2, ring 1, stage "x"). The same connection that is given to the input $R_i(1,2,2n+1)$ is also connected to the input $K(2,1,x+1)$. The same connection that is given to the input $R_i(1,2,2n+2)$ is also connected to the input $J(2,1,x+1)$. Similarly the same connection that is given to the input $R_i(2,1,2x+1)$ is also connected to the input $K(1,2,n+1)$. The same connection that is given to the input $R_i(2,1,2x+2)$ is also connected to the input $J(1,2,n+1)$.

Therefore inlet link I7 can be essentially connected through the 4:1 mux $F(1,2,2n+1)$ with three of its inputs connecting from slice 1 namely $R_i(1,2,2n+1)$, $R_i(1,2,2n+2)$, $U_i(1,2,2n+2)$ and one input $J(1,2,n+1)$ connecting from slice 2. The inlet link I8 can be essentially connected through the 4:1 mux $F(1,2,2n+2)$ with three of its inputs connecting from slice 1 namely $R_i(1,2,2n+1)$, $R_i(1,2,2n+2)$, $U_i(1,2,2n+1)$ and one input $K(1,2,n+1)$ connecting from slice 2. The inlet link I13 can be essentially connected through the 4:1 mux $F(2,1,2x+1)$ with three of its inputs connecting from slice 2 namely $R_i(2,1,2x+1)$, $R_i(2,1,2x+2)$, $U_i(2,1,2x+2)$ and one input $J(2,1,x+1)$ connecting from slice 1. The inlet link I14 can be essentially connected through the 4:1 mux $F(2,1,2x+2)$ with three of its inputs connecting from slice 2 namely $R_i(2,1,2x+1)$, $R_i(2,1,2x+2)$, $U_i(2,1,2x+1)$ and one input $K(2,1,x+1)$ connecting from slice 1. Hence all the inlet links I7, I8, I13 and I14 are all independently reachable from both slice 1 and slice2.

The connections illustrated between different slices, in several embodiments, in diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 are the only connections between different slices. And also the terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block have three inputs coming from one slice and one input coming from another slice. In other embodiments it is also possible so that the terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block have two inputs coming from one slice and two inputs coming from another slice.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Also in general the number of slices in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C may be more than or equal to two. In such a case terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block will have at least one input coming from each slice. And the outlet links of the computational block will be divided and connected to each slice; however each outlet link of the computational block will be connected to only one slice. Also in general the hop wires and multi-drop hop wires are connected to only between the corresponding slices of different blocks, in some embodiments some of the hop wires and multi-drop hop wires may be connected between different slices of different blocks even if it is done partially.

FIG. 2A illustrates a stage (ring “k”, stage “m”) 200A consists of 4 inputs namely $F_i(k, 2m+1)$, $F_i(k, 2m+2)$, $U_i(k, 2m+1)$, and $U_i(k, 2m+2)$; and 4 outputs $B_o(k, 2m+1)$, $B_o(k, 2m+2)$, $F_o(k, 2m+1)$, and $F_o(k, 2m+2)$. The stage (ring “k”, stage “m”) also consists of six 2:1 Muxes namely $F(k, 2m+1)$, $F(k, 2m+2)$ (comprising in combination a forward switch), $U(k, 2m+1)$, $U(k, 2m+2)$ (comprising in combination a U-turn switch), $B(k, 2m+1)$, and $B(k, 2m+2)$ (comprising in combination a backward switch). The 2:1 Mux $F(k, 2m+1)$ has two inputs namely $F_i(k, 2m+1)$ and $F_i(k, 2m+2)$ and has one output $F_o(k, 2m+1)$. The 2:1 Mux $F(k, 2m+2)$ has two inputs namely $F_i(k, 2m+1)$ and $F_i(k, 2m+2)$ and has one output $F_o(k, 2m+2)$.

The 2:1 Mux $U(k, 2m+1)$ has two inputs namely $U_i(k, 2m+1)$ and $F_o(k, 2m+1)$ and has one output $U_o(k, 2m+1)$. The 2:1 Mux $U(k, 2m+2)$ has two inputs namely $U_i(k, 2m+2)$ and $F_o(k, 2m+2)$ and has one output $U_o(k, 2m+2)$. The 2:1 Mux $B(k, 2m+1)$ has two inputs namely $U_o(k, 2m+1)$ and $U_o(k, 2m+2)$ and has one output $B_o(k, 2m+1)$. The 2:1 Mux $B(k, 2m+2)$ has two inputs namely $U_o(k, 2m+1)$ and $U_o(k, 2m+2)$ and has one output $B_o(k, 2m+2)$.

FIG. 2B illustrates a stage (ring “k”, stage “m”) 200B consists of 4 inputs namely $R_i(k, 2m+1)$, $R_i(k, 2m+2)$, $U_i(k, 2m+1)$, and $U_i(k, 2m+2)$; and 4 outputs $B_o(k, 2m+1)$, $B_o(k, 2m+2)$, $F_o(k, 2m+1)$, and $F_o(k, 2m+2)$. The stage (ring “k”, stage “m”) also consists of eight 2:1 Muxes namely $R(k, 2m+1)$, $R(k, 2m+2)$ (comprising in combination a Reverse U-turn switch), $F(k, 2m+1)$, $F(k, 2m+2)$ (comprising in combination a forward switch), $U(k, 2m+1)$, $U(k, 2m+2)$ (comprising in combination a U-turn switch), $B(k, 2m+1)$, and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

B(k,2m+2) (comprising in combination a backward switch). The 2:1 Mux R(k,2m+1) has two inputs namely $R_i(k,2m+1)$ and $B_o(k,2m+1)$ and has one output $R_o(k,2m+1)$. The 2:1 Mux R(k,2m+2) has two inputs namely $R_i(k,2m+2)$ and $B_o(k,2m+2)$ and has one output $R_o(k,2m+2)$. The 2:1 Mux F(k,2m+1) has two inputs namely $R_o(k,2m+1)$ and $R_o(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux F(k,2m+2) has two inputs namely $R_o(k,2m+1)$ and $R_o(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 2:1 Mux U(k,2m+1) has two inputs namely $U_i(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux U(k,2m+2) has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux B(k,2m+1) has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux B(k,2m+2) has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

FIG. 2C illustrates a stage (ring “k”, stage “m”) 200C consists of 4 inputs namely $F_i(k,2m+1)$, $F_i(k,2m+2)$, $U_i(k,2m+1)$, and $U_i(k,2m+2)$; and 4 outputs $U_o(k,2m+1)$, $U_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of four 2:1 Muxes namely F(k,2m+1), F(k,2m+2) (comprising in combination a forward switch), U(k,2m+1), and U(k,2m+2) (comprising in combination a U-turn switch). The 2:1 Mux F(k,2m+1) has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux F(k,2m+2) has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 2:1 Mux U(k,2m+1) has two inputs namely $U_i(k,2m+1)$ and $U_i(k,2m+2)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux U(k,2m+2) has two inputs namely $U_i(k,2m+1)$ and $U_i(k,2m+2)$ and has one output $U_o(k,2m+2)$.

However the stage “m” of ring “k” with “m” stages of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 2 inputs and 2 outputs as shown in diagram 200D in FIG. 2D. FIG. 2D illustrates a stage (ring “k”, stage “m”) 200D consists of 2 inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$; and 2 outputs $F_o(k,2m+1)$ and $F_o(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of two 2:1 Muxes namely F(k,2m+1), F(k,2m+2) (comprising in combination a forward switch). The 2:1 Mux F(k,2m+1) has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

output $Fo(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $Fi(k,2m+1)$ and $Fi(k,2m+2)$ and has one output $Fo(k,2m+2)$. A stage with 2 inputs and 2 outputs is, in one embodiment, the “last stage” or “root stage” of ring.

The stage “m” of ring “k” with “m” stages of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 8 inputs and 4 outputs as shown in diagram 200E in FIG. 2E. FIG. 2E illustrates a stage (ring “k”, stage “m”) 200E consists of 8 inputs namely $Fi(k,2m+1)$, $Fi(k,2m+2)$, $Bi(k,2m+1)$, $Bi(k,2m+2)$, J, K, L, and M; and 4 outputs $Uo(k,2m+1)$, $Uo(k,2m+2)$, $Ro(k,2m+1)$, and $Ro(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of eight 2:1 Muxes namely $F(k,2m+1)$, $F(k,2m+2)$ (comprising in combination a forward switch), $R(k,2m+1)$, $R(k,2m+2)$ (comprising in combination a Reverse U-turn switch), $B(k,2m+1)$, $B(k,2m+2)$ (comprising in combination a backward switch), $U(k,2m+1)$, and $U(k,2m+2)$ (comprising in combination a U-turn switch). The 2:1 Mux $R(k,2m+1)$ has two inputs namely $Fi(k,2m+1)$ and J, and has one output $Fo(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $Fi(k,2m+2)$ and K, and has one output $Fo(k,2m+2)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $Fo(k,2m+1)$ and $Bo(k,2m+2)$, and has one output $Ro(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $Fo(k,2m+2)$ and $Bo(k,2m+1)$, and has one output $Ro(k,2m+2)$.

The 2:1 Mux $B(k,2m+1)$ has two inputs namely $Bi(k,2m+1)$ and L, and has one output $Bo(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $Bi(k,2m+2)$ and M, and has one output $Bo(k,2m+2)$. The 2:1 Mux $U(k,2m+1)$ has two inputs namely $Bo(k,2m+1)$ and $Fo(k,2m+2)$, and has one output $Uo(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $Bo(k,2m+2)$ and $Fo(k,2m+1)$, and has one output $Uo(k,2m+2)$. In different embodiments the inputs J, K, L, and M are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The diagram 200E of FIG 2E eliminates the 180-degree turn paths from the internal connection $Fi(k,2m+1)$ to the internal connection $Uo(k,2m+1)$. Similarly the diagram 200E of FIG 2E eliminates the 180-degree turn paths from the connection $Fi(k,2m+2)$ to the connection $Uo(k,2m+2)$. The diagram 200E of FIG 2E eliminates the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

180-degree turn paths from the internal connection $Bi(k,2m+1)$ to the internal connection $Ro(k,2m+1)$. Similarly the diagram 200E of FIG. 2E eliminates the 180-degree turn paths from the connection $Bi(k,2m+2)$ to the connection $Ro(k,2m+2)$. Hence diagram 200E of FIG. 2E comprises a forward switch, a backward switch, U-turn switch and reverse U-
 5 turn switch without 180-degree U-turn paths.

In contrast to diagram 200E of FIG. 2E, the diagram 200A of FIG. 2A, diagram 200B of FIG. 2B, and diagram 200C of FIG. 2C provide 180-degree U-turn paths. Two exemplary 180-degree U-turn paths in diagram 200A of FIG. 2A are shown (by two types of dotted lines) in the attached replacement diagram of FIG. 2A. One of the 180-degree
 10 turn path shown in the replacement diagram of FIG. 2A starts at the internal connection $Fi(k,2m+1)$ through the Mux $F(k,2m+1)$ to $Fo(k,2m+1)$ through the Mux $U(k,2m+1)$ to $Uo(k,2m+1)$ through the Mux $B(k,2m+1)$ to the internal connection $Bo(k,2m+1)$. The second of the 180-degree turn path shown in the replacement diagram of FIG. 2A starts at the hop wire $Fi(k,2m+2)$ through the Mux $F(k,2m+2)$ to $Fo(k,2m+2)$ through the Mux
 15 $U(k,2m+2)$ to $Uo(k,2m+2)$ through the Mux $B(k,2m+2)$ to the hop wire $Bo(k,2m+2)$.

The stage “m” of ring “k” with “m” stages of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 8 inputs and 4 outputs as shown in diagram 200F in FIG. 2F. FIG. 2F illustrates a stage (ring “k”, stage “m”) 200F consists of 8 inputs namely $Ri(k,2m+1)$, $Ri(k,2m+2)$, $Ui(k,2m+1)$, $Ui(k,2m+2)$, J, K, L, and M; and 4 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage
 20 (ring “k”, stage “m”) also consists of four 4:1 Muxes namely $F(k,2m+1)$, $F(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The 4:1 Mux $F(k,2m+1)$ has four inputs namely $Ri(k,2m+1)$, $Ri(k,2m+2)$, $Ui(k,2m+2)$, and J, and has one output $Fo(k,2m+1)$. The 4:1 Mux $F(k,2m+2)$ has four inputs namely $Ri(k,2m+1)$, $Ri(k,2m+2)$, $Ui(k,2m+1)$, and K, and has one output
 25 $Fo(k,2m+2)$.

The 4:1 Mux $B(k,2m+1)$ has four inputs namely $Ui(k,2m+1)$, $Ui(k,2m+2)$, $Ri(k,2m+2)$, and L, and has one output $Bo(k,2m+1)$. The 4:1 Mux $B(k,2m+2)$ has four inputs namely $Ui(k,2m+1)$, $Ui(k,2m+2)$, $Ri(k,2m+1)$ and M, and has one output $Bo(k,2m+2)$. In different embodiments the inputs J, K, L, and M are connected from any

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The diagram 200F of FIG 2F eliminates the 180-degree turn paths from the internal connection $Ri(k, 2m+1)$ to the internal connection $Bo(k, 2m+1)$. Similarly the diagram 200F of FIG 2F eliminates the 180-degree turn paths from the connection $Ri(k, 2m+2)$ to the connection $Bo(k, 2m+2)$. The diagram 200F of FIG 2F eliminates the 180-degree turn paths from the internal connection $Ui(k, 2m+1)$ to the internal connection $Fo(k, 2m+1)$. Similarly the diagram 200F of FIG 2F eliminates the 180-degree turn paths from the connection $Ui(k, 2m+2)$ to the connection $Fo(k, 2m+2)$. Hence diagram 200F of FIG. 2F comprises an integrated switch of a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180-degree U-turn paths.

The number of stages in a ring of any block may not be equal to the number of stages in any other ring of the same of block or any ring of any other block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. For example the number of stages in ring 1 of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A or of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B or of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C is denoted by “m” and the number of stages in ring 2 of the partial multi-stage hierarchical network is denoted by “n”, and so “m” may or may not be equal to “n”. Similarly the number of stages in ring 2 corresponding to block (3,3) of 2D-grid 800 may not be equal to the number of stages in ring 2 corresponding to block (6,9) of 2D-grid 800. Similarly in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C the number of stages in (slice 1, ring 2) corresponding to block (3,3) of 2D-grid 800 may not be equal to the number of stages in (slice 1, ring 2) corresponding to block (6,9) of 2D-grid 800.

Even though the number of inlet links to the computational block is four and the number of outlet links to the computational block is two in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A, the number of inlet links to the computational block is eight and the number of outlet links to the computational block is four in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B, and the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

number of inlet links to the computational block is sixteen and the number of outlet links to the computational block is four in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C, in other embodiments the number of inlet links to the computational block may be any arbitrary number and the number of outlet links to the computational block may also be another arbitrary number. However the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of inlet links to the computational block divided by $d = 2$ if the inputs and outputs are connected either only from left-hand side or only from right-hand side, if the number of inlet links to the computational block is greater than or equal to the number of outlet links to the computational block. In such a case one or more of the outlet links to the computational block are connected to more than one inlet links of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to a block. Similarly the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of inlet links to the computational block divided by $2 * d = 4$ if the inputs and outputs are connected from both left-hand side and from right-hand side, if the number of inlet links to the computational block is greater than or equal to the number of outlet links to the computational block.

Otherwise the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of outlet links to the computational block divided by $d = 2$ if the inputs and outputs are connected either only from left-hand side or only from right-hand side, if the number of outlet links to the computational block is greater than the number of inlet links to the computational block. In such a case one or more of the outlet links of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to a block are connected to more than one inlet link of the computational block. Similarly the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of outlet links to the computational block divided by $2 * d = 4$ if the inputs and outputs are connected from

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

both left-hand side and from right-hand side, if the number of outlet links to the computational block is greater than or equal to the number of inlet links to the computational block.

In another embodiment, the number of inlet links to the computational block
 5 corresponding to a block of 2D-grid of blocks may or may not be equal to the number of inlet links to the computational block corresponding to another block. Similarly the number of outlet links to the computational block corresponding to a block of 2D-grid of blocks may or may not be equal to the number of outlet links to the computational block corresponding to another block. Hence the total number of rings of the partial multi-stage
 10 hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to a block of 2D-grid of blocks may or may not be equal to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to another block. For example the total number of rings corresponding to block (4,5) of 2D-grid 800 may be two and the total number of rings in block (5,4) of 2D-grid 800 may be three.

15 A multi-stage hierarchical network can be represented with the notation $V_{Comb}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of the complete multi-stage hierarchical network and N_2 represents the total number of outlet links of the complete multi-stage hierarchical network, d represents the number of inlet links of any ring in any block of the complete multi-stage hierarchical network either from only left-
 20 hand side or only right-hand side, or equivalently the number of outlet links of any ring in any block of the complete multi-stage hierarchical network either from only left-hand side or only right-hand side, and when the inputs and outputs are connected from left-hand side, s is the ratio of number of outgoing links from each stage 0 of any ring in any block to the number of inlet links of any ring in any block of the complete multi-stage
 25 hierarchical network (for example the complete multi-stage hierarchical network corresponding to $V_{Comb}(N_1, N_2, d, s)$ 100A in FIG. 1A, $N_1 = 200$, $N_2 = 400$, $d = 2$, $s = 1$). Also a multi-stage hierarchical network where $N_1 = N_2 = N$ is represented as $V_{Comb}(N, d, s)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The diagram 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, and 300E of FIG. 3E are different embodiments of all the connections between two arbitrary successive stages in two different rings of the same block or two different rings of different blocks of 2D-grid 800. Referring to diagram 300A in FIG. 3A illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 4 inputs namely $R_i(x, 2p+1)$, $R_i(x, 2p+2)$, $U_i(x, 2p+1)$, and $U_i(x, 2p+2)$; and 4 outputs $B_o(x, 2p+1)$, $B_o(x, 2p+2)$, $F_o(x, 2p+1)$, and $F_o(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely $R(x, 2p+1)$, $R(x, 2p+2)$, $F(x, 2p+1)$, $F(x, 2p+2)$, $U(x, 2p+1)$, $U(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 2:1 Mux $R(x, 2p+1)$ has two inputs namely $R_i(x, 2p+1)$ and $B_o(x, 2p+1)$ and has one output $R_o(x, 2p+1)$. The 2:1 Mux $R(x, 2p+2)$ has two inputs namely $R_i(x, 2p+2)$ and $B_o(x, 2p+2)$ and has one output $R_o(x, 2p+2)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $R_o(x, 2p+1)$ and $R_o(x, 2p+2)$ and has one output $F_o(x, 2p+1)$. The 2:1 Mux $F(x, 2p+2)$ has two inputs namely $R_o(x, 2p+1)$ and $R_o(x, 2p+2)$ and has one output $F_o(x, 2p+2)$.

The 2:1 Mux $U(x, 2p+1)$ has two inputs namely $U_i(x, 2p+1)$ and $F_o(x, 2p+1)$ and has one output $U_o(x, 2p+1)$. The 2:1 Mux $U(x, 2p+2)$ has two inputs namely $U_i(x, 2p+2)$ and $F_o(x, 2p+2)$ and has one output $U_o(x, 2p+2)$. The 2:1 Mux $B(x, 2p+1)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $B_o(x, 2p+1)$. The 2:1 Mux $B(x, 2p+2)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $B_o(x, 2p+2)$.

The stage (ring “x”, stage “p+1”) consists of 4 inputs namely $R_i(x, 2p+3)$, $R_i(x, 2p+4)$, $U_i(x, 2p+3)$, and $U_i(x, 2p+4)$; and 4 outputs $B_o(x, 2p+3)$, $B_o(x, 2p+4)$, $F_o(x, 2p+3)$, and $F_o(x, 2p+4)$. The stage (ring “x”, stage “p+1”) also consists of eight 2:1 Muxes namely $R(x, 2p+3)$, $R(x, 2p+4)$, $F(x, 2p+3)$, $F(x, 2p+4)$, $U(x, 2p+3)$, $U(x, 2p+4)$, $B(x, 2p+3)$, and $B(x, 2p+4)$. The 2:1 Mux $R(x, 2p+3)$ has two inputs namely $R_i(x, 2p+3)$ and $B_o(x, 2p+3)$ and has one output $R_o(x, 2p+3)$. The 2:1 Mux $R(x, 2p+4)$ has two inputs namely $R_i(x, 2p+4)$ and $B_o(x, 2p+4)$ and has one output $R_o(x, 2p+4)$. The 2:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$F(x,2p+3)$ has two inputs namely $Ro(x,2p+3)$ and $Ro(x,2p+4)$ and has one output $Fo(x,2p+3)$. The 2:1 Mux $F(x,2p+4)$ has two inputs namely $Ro(x,2p+3)$ and $Ro(x,2p+4)$ and has one output $Fo(x,2p+4)$.

The 2:1 Mux $U(x,2p+3)$ has two inputs namely $Ui(x,2p+3)$ and $Fo(x,2p+3)$ and
 5 has one output $Uo(x,2p+3)$. The 2:1 Mux $U(x,2p+4)$ has two inputs namely $Ui(x,2p+4)$
 and $Fo(x,2p+4)$ and has one output $Uo(x,2p+4)$. The 2:1 Mux $B(x,2p+3)$ has two inputs
 namely $Uo(x,2p+3)$ and $Uo(x,2p+4)$ and has one output $Bo(x,2p+3)$. The 2:1 Mux
 $B(x,2p+4)$ has two inputs namely $Uo(x,2p+3)$ and $Uo(x,2p+4)$ and has one output
 $Bo(x,2p+4)$.

10 The output $Fo(x,2p+1)$ of the stage (ring "x", stage "p") is connected to the input
 $Ri(x,2p+3)$ of the stage (ring "x", stage "p+1"). And the output $Bo(x,2p+3)$ of the stage
 (ring "x", stage "p+1") is connected to the input $Ui(x,2p+1)$ of the stage (ring "x", stage
 "p").

The stage (ring "y", stage "q") consists of 4 inputs namely $Ri(y,2q+1)$,
 15 $Ri(y,2q+2)$, $Ui(y,2q+1)$, and $Ui(y,2q+2)$; and 4 outputs $Bo(y,2q+1)$, $Bo(y,2q+2)$,
 $Fo(y,2q+1)$, and $Fo(y,2q+2)$. The stage (ring "y", stage "q") also consists of eight 2:1
 Muxes namely $R(y,2q+1)$, $R(y,2q+2)$, $F(y,2q+1)$, $F(y,2q+2)$, $U(y,2q+1)$, $U(y,2q+2)$,
 $B(y,2q+1)$, and $B(y,2q+2)$. The 2:1 Mux $R(y,2q+1)$ has two inputs namely $Ri(y,2q+1)$
 and $Bo(y,2q+1)$ and has one output $Ro(y,2q+1)$. The 2:1 Mux $R(y,2q+2)$ has two inputs
 20 namely $Ri(y,2q+2)$ and $Bo(y,2q+2)$ and has one output $Ro(y,2q+2)$. The 2:1 Mux
 $F(y,2q+1)$ has two inputs namely $Ro(y,2q+1)$ and $Ro(y,2q+2)$ and has one output
 $Fo(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $Ro(y,2q+1)$ and $Ro(y,2q+2)$
 and has one output $Fo(y,2q+2)$.

The 2:1 Mux $U(y,2q+1)$ has two inputs namely $Ui(y,2q+1)$ and $Fo(y,2q+1)$ and
 25 has one output $Uo(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $Ui(y,2q+2)$
 and $Fo(y,2q+2)$ and has one output $Uo(y,2q+2)$. The 2:1 Mux $B(y,2q+1)$ has two inputs
 namely $Uo(y,2q+1)$ and $Uo(y,2q+2)$ and has one output $Bo(y,2q+1)$. The 2:1 Mux
 $B(y,2q+2)$ has two inputs namely $Uo(y,2q+1)$ and $Uo(y,2q+2)$ and has one output
 $Bo(y,2q+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The stage (ring “y”, stage “q+1”) consists of 4 inputs namely $R_i(y,2q+3)$, $R_i(y,2q+4)$, $U_i(y,2q+3)$, and $U_i(y,2q+4)$; and 4 outputs $B_o(y,2q+3)$, $B_o(y,2q+4)$, $F_o(y,2q+3)$, and $F_o(y,2q+4)$. The stage (ring “y”, stage “q+1”) also consists of eight 2:1 Muxes namely $R(y,2q+3)$, $R(y,2q+4)$, $F(y,2q+3)$, $F(y,2q+4)$, $U(y,2q+3)$, $U(y,2q+4)$, $B(y,2q+3)$, and $B(y,2q+4)$. The 2:1 Mux $R(y,2q+3)$ has two inputs namely $R_i(y,2q+3)$ and $B_o(y,2q+3)$ and has one output $R_o(y,2q+3)$. The 2:1 Mux $R(y,2q+4)$ has two inputs namely $R_i(y,2q+4)$ and $B_o(y,2q+4)$ and has one output $R_o(y,2q+4)$. The 2:1 Mux $F(y,2q+3)$ has two inputs namely $R_o(y,2q+3)$ and $R_o(y,2q+4)$ and has one output $F_o(y,2q+3)$. The 2:1 Mux $F(y,2q+4)$ has two inputs namely $R_o(y,2q+3)$ and $R_o(y,2q+4)$ and has one output $F_o(y,2q+4)$.

The 2:1 Mux $U(y,2q+3)$ has two inputs namely $U_i(y,2q+3)$ and $F_o(y,2q+3)$ and has one output $U_o(y,2q+3)$. The 2:1 Mux $U(y,2q+4)$ has two inputs namely $U_i(y,2q+4)$ and $F_o(y,2q+4)$ and has one output $U_o(y,2q+4)$. The 2:1 Mux $B(y,2q+3)$ has two inputs namely $U_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output $B_o(y,2q+3)$. The 2:1 Mux $B(y,2q+4)$ has two inputs namely $U_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output $B_o(y,2q+4)$.

The output $F_o(y,2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $R_i(y,2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $B_o(y,2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $U_i(y,2q+1)$ of the stage (ring “y”, stage “q”).

The output $F_o(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input $R_i(y,2q+4)$ of the stage (ring “y”, stage “q+1”). The output $B_o(x,2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire Hop(1,2) to the input $U_i(y,2q+2)$ of the stage (ring “y”, stage “q”).

The output $F_o(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire Hop(2,1) to the input $R_i(x,2p+4)$ of the stage (ring “x”, stage “p+1”). The output $B_o(y,2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to the input $U_i(x,2p+2)$ of the stage (ring “x”, stage “p”).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Ring “x” and ring “y” may or may not belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. If ring “x” and ring “y” belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are hereinafter called “internal hop wires”. For example if “x = 2” and “y = 3” and both the ring 2 and ring 3 belong to the same block (9,9) of 2D-grid 800, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are “internal hop wires”.

If ring “x” and ring “y” belong to the different blocks of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are hereinafter called “external hop wires”. The external hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) may be horizontal wires or vertical wires. The length of the external hop wires is manhattan distance between the corresponding blocks, hereinafter “hop length”. For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (1,6) of 2D-grid 800 then the external hop wires are hereinafter called “horizontal external hop wires”. And the hop length of the horizontal hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) is given by $6 - 1 = 5$. Similarly if ring “x” and ring “y” belong to two blocks in the same horizontal row of 2D-grid 800, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are horizontal external hop wires.

For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (9,1) of 2D-grid 800 then the external hop wires are hereinafter called “vertical external hop wires”. And the hop length of the vertical hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) is given by $9 - 1 = 8$. Similarly if ring “x” and ring “y” belong to two blocks in the same vertical column of 2D-grid 800, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are vertical external hop wires. External hop wires are typically horizontal or vertical according to the current invention.

Referring to diagram 300B in FIG. 3B illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The stage (ring “x”, stage “p”) consists of 8 inputs namely $F_i(x,2p+1)$, $F_i(x,2p+2)$, $B_i(x,2p+1)$, $B_i(x,2p+2)$, J_1 , K_1 , L_1 , and M_1 ; and 4 outputs $U_o(x,2p+1)$, $U_o(x,2p+2)$, $R_o(x,2p+1)$, and $R_o(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely $F(x,2p+1)$, $F(x,2p+2)$, $R(x,2p+1)$, $R(x,2p+2)$, $B(x,2p+1)$, $B(x,2p+2)$, $U(x,2p+1)$, and $U(x,2p+2)$. The 2:1 Mux $F(x,2p+1)$ has two inputs namely $F_i(x,2p+1)$ and J_1 , and has one output $F_o(x,2p+1)$. The 2:1 Mux $F(x,2p+2)$ has two inputs namely $F_i(x,2p+2)$ and K_1 , and has one output $F_o(x,2p+2)$. The 2:1 Mux $R(x,2p+1)$ has two inputs namely $F_o(x,2p+1)$ and $B_o(x,2p+2)$, and has one output $R_o(x,2p+1)$. The 2:1 Mux $R(x,2p+2)$ has two inputs namely $F_o(x,2p+2)$ and $B_o(x,2p+1)$, and has one output $R_o(x,2p+2)$.

The 2:1 Mux $B(x,2p+1)$ has two inputs namely $B_i(x,2p+1)$ and L_1 , and has one output $B_o(x,2p+1)$. The 2:1 Mux $B(x,2p+2)$ has two inputs namely $B_i(x,2p+2)$ and M_1 , and has one output $B_o(x,2p+2)$. The 2:1 Mux $U(x,2p+1)$ has two inputs namely $B_o(x,2p+1)$ and $F_o(x,2p+2)$, and has one output $U_o(x,2p+1)$. The 2:1 Mux $U(x,2p+2)$ has two inputs namely $B_o(x,2p+2)$ and $F_o(x,2p+1)$, and has one output $U_o(x,2p+2)$.

The stage (ring “x”, stage “p+1”) consists of 8 inputs namely $F_i(x,2p+3)$, $F_i(x,2p+4)$, $B_i(x,2p+3)$, $B_i(x,2p+4)$, J_2 , K_2 , L_2 , and M_2 ; and 4 outputs $U_o(x,2p+3)$, $U_o(x,2p+4)$, $R_o(x,2p+3)$, and $R_o(x,2p+4)$. The stage (ring “x”, stage “p+1”) also consists of eight 2:1 Muxes namely $F(x,2p+3)$, $F(x,2p+4)$, $R(x,2p+3)$, $R(x,2p+4)$, $B(x,2p+3)$, $B(x,2p+4)$, $U(x,2p+3)$, and $U(x,2p+4)$. The 2:1 Mux $F(x,2p+3)$ has two inputs namely $F_i(x,2p+3)$ and J_2 , and has one output $F_o(x,2p+3)$. The 2:1 Mux $F(x,2p+4)$ has two inputs namely $F_i(x,2p+4)$ and K_2 , and has one output $F_o(x,2p+4)$. The 2:1 Mux $R(x,2p+3)$ has two inputs namely $F_o(x,2p+3)$ and $B_o(x,2p+4)$, and has one output $R_o(x,2p+3)$. The 2:1 Mux $R(x,2p+4)$ has two inputs namely $F_o(x,2p+4)$ and $B_o(x,2p+3)$, and has one output $R_o(x,2p+4)$.

The 2:1 Mux $B(x,2p+3)$ has two inputs namely $B_i(x,2p+3)$ and L_2 , and has one output $B_o(x,2p+3)$. The 2:1 Mux $B(x,2p+4)$ has two inputs namely $B_i(x,2p+4)$ and M_2 , and has one output $B_o(x,2p+4)$. The 2:1 Mux $U(x,2p+3)$ has two inputs namely $B_o(x,2p+3)$ and $F_o(x,2p+4)$, and has one output $U_o(x,2p+3)$. The 2:1 Mux $U(x,2p+4)$ has two inputs namely $B_o(x,2p+4)$ and $F_o(x,2p+3)$, and has one output $U_o(x,2p+4)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The output $Ro(x,2p+1)$ of the stage (ring “x”, stage “p”) is connected to the input $Fi(x,2p+3)$ of the stage (ring “x”, stage “p+1”). And the output $Uo(x,2p+3)$ of the stage (ring “x”, stage “p+1”) is connected to the input $Bi(x,2p+1)$ of the stage (ring “x”, stage “p”).

5 The stage (ring “y”, stage “q”) consists of 8 inputs namely $Fi(y,2q+1)$, $Fi(y,2q+2)$, $Bi(y,2q+1)$, $Bi(y,2q+2)$, J3, K3, L3, and M3; and 4 outputs $Uo(y,2q+1)$, $Uo(y,2q+2)$, $Ro(y,2q+1)$, and $Ro(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of eight 2:1 Muxes namely $F(y,2q+1)$, $F(y,2q+2)$, $R(y,2q+1)$, $R(y,2q+2)$, $B(y,2q+1)$, $B(y,2q+2)$, $U(y,2q+1)$, and $U(y,2q+2)$. The 2:1 Mux $F(y,2q+1)$ has two inputs namely $Fi(y,2q+1)$ and J3, and has one output $Fo(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $Fi(y,2q+2)$ and K3, and has one output $Fo(y,2q+2)$. The 2:1 Mux $R(y,2q+1)$ has two inputs namely $Fo(y,2q+1)$ and $Bo(y,2q+2)$, and has one output $Ro(y,2q+1)$. The 2:1 Mux $R(y,2q+2)$ has two inputs namely $Fo(y,2q+2)$ and $Bo(y,2q+1)$ and has one output $Ro(y,2q+2)$.

15 The 2:1 Mux $B(y,2q+1)$ has two inputs namely $Bi(y,2q+1)$ and L3, and has one output $Bo(y,2q+1)$. The 2:1 Mux $B(y,2q+2)$ has two inputs namely $Bi(y,2q+2)$ and M3, and has one output $Bo(y,2q+2)$. The 2:1 Mux $U(y,2q+1)$ has two inputs namely $Bo(y,2q+1)$ and $Fo(y,2q+2)$, and has one output $Uo(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $Bo(y,2q+2)$ and $Fo(y,2q+1)$, and has one output $Uo(y,2q+2)$.

20 The stage (ring “y”, stage “q+1”) consists of 8 inputs namely $Fi(y,2q+3)$, $Fi(y,2q+4)$, $Bi(y,2q+3)$, $Bi(y,2q+4)$, J4, K4, L4, and M4; and 4 outputs $Uo(y,2q+3)$, $Uo(y,2q+4)$, $Ro(y,2q+3)$, and $Ro(y,2q+4)$. The stage (ring “y”, stage “q+1”) also consists of eight 2:1 Muxes namely $F(y,2q+3)$, $F(y,2q+4)$, $R(y,2q+3)$, $R(y,2q+4)$, $B(y,2q+3)$, $B(y,2q+4)$, $U(y,2q+3)$, and $U(y,2q+4)$. The 2:1 Mux $F(y,2q+3)$ has two inputs namely $Fi(y,2q+3)$ and J4, and has one output $Fo(y,2q+3)$. The 2:1 Mux $F(y,2q+4)$ has two inputs namely $Fi(y,2q+4)$ and K4, and has one output $Fo(y,2q+4)$. The 2:1 Mux $R(y,2q+3)$ has two inputs namely $Fo(y,2q+3)$ and $Bo(y,2q+4)$, and has one output $Ro(y,2q+3)$. The 2:1 Mux $R(y,2q+4)$ has two inputs namely $Fo(y,2q+4)$ and $Bo(y,2q+3)$, and has one output $Ro(y,2q+4)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux B(y,2q+3) has two inputs namely Bi(y,2q+3) and L4, and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Bi(y,2q+4) and M4, and has one output Bo(y,2q+4). The 2:1 Mux U(y,2q+3) has two inputs namely Bo(y,2q+3) and Fo(y,2q+4), and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has
5 two inputs namely Bo(y,2q+4) and Fo(y,2q+3), and has one output Uo(y,2q+4).

The output Ro(y,2q+1) of the stage (ring “y”, stage “q”) is connected to the input Fi(y,2q+3) of the stage (ring “y”, stage “q+1”). And the output Uo(y,2q+3) of the stage (ring “y”, stage “q+1”) is connected to the input Bi(y,2q+1) of the stage (ring “y”, stage “q”).

10 The output Uo(x,2p+2) of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input Bi(y,2q+2) of the stage (ring “y”, stage “q”). The output Ro(y,2q+2) of the stage (ring “y”, stage “q”) is connected via the wire Hop(1,2) to the input Fi(x,2p+2) of the stage (ring “x”, stage “p”).

The output Uo(x,2p+4) of the stage (ring “x”, stage “p+1”) is connected via the
15 wire Hop(2,1) to the input Bi(y,2q+4) of the stage (ring “y”, stage “q+1”). The output Ro(y,2q+4) of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to the input Fi(x,2p+4) of the stage (ring “x”, stage “p+1”).

In various embodiments, the inputs J1, K1, L1, and M1 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical
20 network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J2, K2, L2, and M2 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J3, K3, L3, and M3 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Finally the inputs J4, K4, L4, and
25 M4 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Referring to diagram 300C in FIG. 3C, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

(ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 4 inputs namely $F_i(x, 2p+1)$, $F_i(x, 2p+2)$, $U_i(x, 2p+1)$, and $U_i(x, 2p+2)$; and 4 outputs $B_o(x, 2p+1)$, $B_o(x, 2p+2)$, $F_o(x, 2p+1)$, and $F_o(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of six 2:1 Muxes namely $F(x, 2p+1)$, $F(x, 2p+2)$, $U(x, 2p+1)$, $U(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $F_i(x, 2p+1)$ and $F_i(x, 2p+2)$ and has one output $F_o(x, 2p+1)$. The 2:1 Mux $F(x, 2p+2)$ has two inputs namely $F_i(x, 2p+1)$ and $F_i(x, 2p+2)$ and has one output $F_o(x, 2p+2)$.

The 2:1 Mux $U(x, 2p+1)$ has two inputs namely $U_i(x, 2p+1)$ and $F_o(x, 2p+1)$ and has one output $U_o(x, 2p+1)$. The 2:1 Mux $U(x, 2p+2)$ has two inputs namely $U_i(x, 2p+2)$ and $F_o(x, 2p+2)$ and has one output $U_o(x, 2p+2)$. The 2:1 Mux $B(x, 2p+1)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $B_o(x, 2p+1)$. The 2:1 Mux $B(x, 2p+2)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $B_o(x, 2p+2)$.

The stage (ring “x”, stage “p+1”) consists of 4 inputs namely $F_i(x, 2p+3)$, $F_i(x, 2p+4)$, $U_i(x, 2p+3)$, and $U_i(x, 2p+4)$; and 4 outputs $B_o(x, 2p+3)$, $B_o(x, 2p+4)$, $F_o(x, 2p+3)$, and $F_o(x, 2p+4)$. The stage (ring “x”, stage “p+1”) also consists of six 2:1 Muxes namely $F(x, 2p+3)$, $F(x, 2p+4)$, $U(x, 2p+3)$, $U(x, 2p+4)$, $B(x, 2p+3)$, and $B(x, 2p+4)$. The 2:1 Mux $F(x, 2p+3)$ has two inputs namely $F_i(x, 2p+3)$ and $F_i(x, 2p+4)$ and has one output $F_o(x, 2p+3)$. The 2:1 Mux $F(x, 2p+4)$ has two inputs namely $F_i(x, 2p+3)$ and $F_i(x, 2p+4)$ and has one output $F_o(x, 2p+4)$.

The 2:1 Mux $U(x, 2p+3)$ has two inputs namely $U_i(x, 2p+3)$ and $F_o(x, 2p+3)$ and has one output $U_o(x, 2p+3)$. The 2:1 Mux $U(x, 2p+4)$ has two inputs namely $U_i(x, 2p+4)$ and $F_o(x, 2p+4)$ and has one output $U_o(x, 2p+4)$. The 2:1 Mux $B(x, 2p+3)$ has two inputs namely $U_o(x, 2p+3)$ and $U_o(x, 2p+4)$ and has one output $B_o(x, 2p+3)$. The 2:1 Mux $B(x, 2p+4)$ has two inputs namely $U_o(x, 2p+3)$ and $U_o(x, 2p+4)$ and has one output $B_o(x, 2p+4)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The output $Fo(x,2p+1)$ of the stage (ring "x", stage "p") is connected to the input $Fi(x,2p+3)$ of the stage (ring "x", stage "p+1"). And the output $Bo(x,2p+3)$ of the stage (ring "x", stage "p+1") is connected to the input $Ui(x,2p+1)$ of the stage (ring "x", stage "p").

5 The stage (ring "y", stage "q") consists of 4 inputs namely $Fi(y,2q+1)$, $Fi(y,2q+2)$, $Ui(y,2q+1)$, and $Ui(y,2q+2)$; and 4 outputs $Bo(y,2q+1)$, $Bo(y,2q+2)$, $Fo(y,2q+1)$, and $Fo(y,2q+2)$. The stage (ring "y", stage "q") also consists of six 2:1 Muxes namely $F(y,2q+1)$, $F(y,2q+2)$, $U(y,2q+1)$, $U(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The 2:1 Mux $F(y,2q+1)$ has two inputs namely $Fi(y,2q+1)$ and $Fi(y,2q+2)$ and has one output
10 $Fo(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $Fi(y,2q+1)$ and $Fi(y,2q+2)$ and has one output $Fo(y,2q+2)$.

The 2:1 Mux $U(y,2q+1)$ has two inputs namely $Ui(y,2q+1)$ and $Fo(y,2q+1)$ and has one output $Uo(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $Ui(y,2q+2)$ and $Fo(y,2q+2)$ and has one output $Uo(y,2q+2)$. The 2:1 Mux $B(y,2q+1)$ has two inputs
15 namely $Uo(y,2q+1)$ and $Uo(y,2q+2)$ and has one output $Bo(y,2q+1)$. The 2:1 Mux $B(y,2q+2)$ has two inputs namely $Uo(y,2q+1)$ and $Uo(y,2q+2)$ and has one output $Bo(y,2q+2)$.

The stage (ring "y", stage "q+1") consists of 4 inputs namely $Fi(y,2q+3)$, $Fi(y,2q+4)$, $Ui(y,2q+3)$, and $Ui(y,2q+4)$; and 4 outputs $Bo(y,2q+3)$, $Bo(y,2q+4)$,
20 $Fo(y,2q+3)$, and $Fo(y,2q+4)$. The stage (ring "y", stage "q+1") also consists of six 2:1 Muxes namely $F(y,2q+3)$, $F(y,2q+4)$, $U(y,2q+3)$, $U(y,2q+4)$, $B(y,2q+3)$, and $B(y,2q+4)$. The 2:1 Mux $F(y,2q+3)$ has two inputs namely $Fi(y,2q+3)$ and $Fi(y,2q+4)$ and has one output $Fo(y,2q+3)$. The 2:1 Mux $F(y,2q+4)$ has two inputs namely $Fi(y,2q+3)$ and $Fi(y,2q+4)$ and has one output $Fo(y,2q+4)$.

25 The 2:1 Mux $U(y,2q+3)$ has two inputs namely $Ui(y,2q+3)$ and $Fo(y,2q+3)$ and has one output $Uo(y,2q+3)$. The 2:1 Mux $U(y,2q+4)$ has two inputs namely $Ui(y,2q+4)$ and $Fo(y,2q+4)$ and has one output $Uo(y,2q+4)$. The 2:1 Mux $B(y,2q+3)$ has two inputs namely $Uo(y,2q+3)$ and $Uo(y,2q+4)$ and has one output $Bo(y,2q+3)$. The 2:1 Mux $B(y,2q+4)$ has two inputs namely $Uo(y,2q+3)$ and $Uo(y,2q+4)$ and has one output
30 $Bo(y,2q+4)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The output $Fo(y,2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $Fi(y,2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $Bo(y,2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $Ui(y,2q+1)$ of the stage (ring “y”, stage “q”).

5 The output $Fo(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire $Hop(1,1)$ to the input $Fi(y,2q+4)$ of the stage (ring “y”, stage “q+1”). The output $Bo(x,2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire $Hop(1,2)$ to the input $Ui(y,2q+2)$ of the stage (ring “y”, stage “q”).

10 The output $Fo(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire $Hop(2,1)$ to the input $Fi(x,2p+4)$ of the stage (ring “x”, stage “p+1”). The output $Bo(y,2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire $Hop(2,2)$ to the input $Ui(x,2p+2)$ of the stage (ring “x”, stage “p”).

15 Referring to diagram 300D in FIG. 3D, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

20 The stage (ring “x”, stage “p”) consists of 4 inputs namely $Fi(x,2p+1)$, $Fi(x,2p+2)$, $Ui(x,2p+1)$, and $Ui(x,2p+2)$; and 4 outputs $Bo(x,2p+1)$, $Bo(x,2p+2)$, $Fo(x,2p+1)$, and $Fo(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of six 2:1 Muxes namely $F(x,2p+1)$, $F(x,2p+2)$, $U(x,2p+1)$, $U(x,2p+2)$, $B(x,2p+1)$, and $B(x,2p+2)$. The 2:1 Mux $F(x,2p+1)$ has two inputs namely $Fi(x,2p+1)$ and $Fi(x,2p+2)$ and has one output $Fo(x,2p+1)$. The 2:1 Mux $F(x,2p+2)$ has two inputs namely $Fi(x,2p+1)$ and $Fi(x,2p+2)$ and has one output $Fo(x,2p+2)$.

25 The 2:1 Mux $U(x,2p+1)$ has two inputs namely $Ui(x,2p+1)$ and $Fo(x,2p+1)$ and has one output $Uo(x,2p+1)$. The 2:1 Mux $U(x,2p+2)$ has two inputs namely $Ui(x,2p+2)$ and $Fo(x,2p+2)$ and has one output $Uo(x,2p+2)$. The 2:1 Mux $B(x,2p+1)$ has two inputs namely $Uo(x,2p+1)$ and $Uo(x,2p+2)$ and has one output $Bo(x,2p+1)$. The 2:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$B(x,2p+2)$ has two inputs namely $Uo(x,2p+1)$ and $Uo(x,2p+2)$ and has one output $Bo(x,2p+2)$.

The stage (ring “x”, stage “p+1”) consists of 2 inputs namely $Fi(x,2p+3)$, $Fi(x,2p+4)$; and 2 outputs $Fo(x,2p+3)$, and $Fo(x,2p+4)$. The stage (ring “x”, stage “p+1”) also consists of two 2:1 Muxes namely $F(x,2p+3)$ and $F(x,2p+4)$. The 2:1 Mux $F(x,2p+3)$ has two inputs namely $Fi(x,2p+3)$ and $Fi(x,2p+4)$ and has one output $Fo(x,2p+3)$. The 2:1 Mux $F(x,2p+4)$ has two inputs namely $Fi(x,2p+3)$ and $Fi(x,2p+4)$ and has one output $Fo(x,2p+4)$.

The output $Fo(x,2p+1)$ of the stage (ring “x”, stage “p”) is connected to the input $Fi(x,2p+3)$ of the stage (ring “x”, stage “p+1”). And the output $Fo(x,2p+3)$ of the stage (ring “x”, stage “p+1”) is connected to the input $Ui(x,2p+1)$ of the stage (ring “x”, stage “p”).

The stage (ring “y”, stage “q”) consists of 4 inputs namely $Fi(y,2q+1)$, $Fi(y,2q+2)$, $Ui(y,2q+1)$, and $Ui(y,2q+2)$; and 4 outputs $Bo(y,2q+1)$, $Bo(y,2q+2)$, $Fo(y,2q+1)$, and $Fo(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of six 2:1 Muxes namely $F(y,2q+1)$, $F(y,2q+2)$, $U(y,2q+1)$, $U(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The 2:1 Mux $F(y,2q+1)$ has two inputs namely $Fi(y,2q+1)$ and $Fi(y,2q+2)$ and has one output $Fo(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $Fi(y,2q+1)$ and $Fi(y,2q+2)$ and has one output $Fo(y,2q+2)$.

The 2:1 Mux $U(y,2q+1)$ has two inputs namely $Ui(y,2q+1)$ and $Fo(y,2q+1)$ and has one output $Uo(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $Ui(y,2q+2)$ and $Fo(y,2q+2)$ and has one output $Uo(y,2q+2)$. The 2:1 Mux $B(y,2q+1)$ has two inputs namely $Uo(y,2q+1)$ and $Uo(y,2q+2)$ and has one output $Bo(y,2q+1)$. The 2:1 Mux $B(y,2q+2)$ has two inputs namely $Uo(y,2q+1)$ and $Uo(y,2q+2)$ and has one output $Bo(y,2q+2)$.

The stage (ring “y”, stage “q+1”) consists of 4 inputs namely $Fi(y,2q+3)$, $Fi(y,2q+4)$, $Ui(y,2q+3)$, and $Ui(y,2q+4)$; and 4 outputs $Bo(y,2q+3)$, $Bo(y,2q+4)$, $Fo(y,2q+3)$, and $Fo(y,2q+4)$. The stage (ring “y”, stage “q+1”) also consists of six 2:1 Muxes namely $F(y,2q+3)$, $F(y,2q+4)$, $U(y,2q+3)$, $U(y,2q+4)$, $B(y,2q+3)$, and $B(y,2q+4)$. The 2:1 Mux $F(y,2q+3)$ has two inputs namely $Fi(y,2q+3)$ and $Fi(y,2q+4)$ and has one

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

output $Fo(y,2q+3)$. The 2:1 Mux $F(y,2q+4)$ has two inputs namely $Fi(y,2q+3)$ and $Fi(y,2q+4)$ and has one output $Fo(y,2q+4)$.

The 2:1 Mux $U(y,2q+3)$ has two inputs namely $Ui(y,2q+3)$ and $Fo(y,2q+3)$ and has one output $Uo(y,2q+3)$. The 2:1 Mux $U(y,2q+4)$ has two inputs namely $Ui(y,2q+4)$ and $Fo(y,2q+4)$ and has one output $Uo(y,2q+4)$. The 2:1 Mux $B(y,2q+3)$ has two inputs namely $Uo(y,2q+3)$ and $Uo(y,2q+4)$ and has one output $Bo(y,2q+3)$. The 2:1 Mux $B(y,2q+4)$ has two inputs namely $Uo(y,2q+3)$ and $Uo(y,2q+4)$ and has one output $Bo(y,2q+4)$.

The output $Fo(y,2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $Fi(y,2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $Bo(y,2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $Ui(y,2q+1)$ of the stage (ring “y”, stage “q”).

The output $Fo(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire $Hop(1,1)$ to the input $Fi(y,2q+4)$ of the stage (ring “y”, stage “q+1”). The output $Fo(x,2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire $Hop(1,2)$ to the input $Ui(y,2q+2)$ of the stage (ring “y”, stage “q”).

The output $Fo(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire $Hop(2,1)$ to the input $Fi(x,2p+4)$ of the stage (ring “x”, stage “p+1”). The output $Bo(y,2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire $Hop(2,2)$ to the input $Ui(x,2p+2)$ of the stage (ring “x”, stage “p”).

Referring to diagram 300E in FIG. 3E, illustrates all the connections between root stage of a ring namely the stage (ring “x”, stage “p”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 4 inputs namely $Fi(x,2p+1)$, $Fi(x,2p+2)$, $Ui(x,2p+1)$, and $Ui(x,2p+2)$; and 4 outputs $Bo(x,2p+1)$, $Bo(x,2p+2)$, $Fo(x,2p+1)$, and $Fo(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of six 2:1 Muxes namely $F(x,2p+1)$, $F(x,2p+2)$, $U(x,2p+1)$, $U(x,2p+2)$, $B(x,2p+1)$, and $B(x,2p+2)$. The 2:1 Mux $F(x,2p+1)$ has two inputs namely $Fi(x,2p+1)$ and $Fi(x,2p+2)$ and has one output

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$F_o(x,2p+1)$. The 2:1 Mux $F(x,2p+2)$ has two inputs namely $F_i(x,2p+1)$ and $F_i(x,2p+2)$ and has one output $F_o(x,2p+2)$.

The 2:1 Mux $U(x,2p+1)$ has two inputs namely $U_i(x,2p+1)$ and $F_o(x,2p+1)$ and has one output $U_o(x,2p+1)$. The 2:1 Mux $U(x,2p+2)$ has two inputs namely $U_i(x,2p+2)$ and $F_o(x,2p+2)$ and has one output $U_o(x,2p+2)$. The 2:1 Mux $B(x,2p+1)$ has two inputs namely $U_o(x,2p+1)$ and $U_o(x,2p+2)$ and has one output $B_o(x,2p+1)$. The 2:1 Mux $B(x,2p+2)$ has two inputs namely $U_o(x,2p+1)$ and $U_o(x,2p+2)$ and has one output $B_o(x,2p+2)$.

The stage (ring "y", stage "q") consists of 4 inputs namely $F_i(y,2q+1)$, $F_i(y,2q+2)$, $U_i(y,2q+1)$, and $U_i(y,2q+2)$; and 4 outputs $B_o(y,2q+1)$, $B_o(y,2q+2)$, $F_o(y,2q+1)$, and $F_o(y,2q+2)$. The stage (ring "y", stage "q") also consists of six 2:1 Muxes namely $F(y,2q+1)$, $F(y,2q+2)$, $U(y,2q+1)$, $U(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The 2:1 Mux $F(y,2q+1)$ has two inputs namely $F_i(y,2q+1)$ and $F_i(y,2q+2)$ and has one output $F_o(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $F_i(y,2q+1)$ and $F_i(y,2q+2)$ and has one output $F_o(y,2q+2)$.

The 2:1 Mux $U(y,2q+1)$ has two inputs namely $U_i(y,2q+1)$ and $F_o(y,2q+1)$ and has one output $U_o(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $U_i(y,2q+2)$ and $F_o(y,2q+2)$ and has one output $U_o(y,2q+2)$. The 2:1 Mux $B(y,2q+1)$ has two inputs namely $U_o(y,2q+1)$ and $U_o(y,2q+2)$ and has one output $B_o(y,2q+1)$. The 2:1 Mux $B(y,2q+2)$ has two inputs namely $U_o(y,2q+1)$ and $U_o(y,2q+2)$ and has one output $B_o(y,2q+2)$.

The stage (ring "y", stage "q+1") consists of 4 inputs namely $F_i(y,2q+3)$, $F_i(y,2q+4)$, $U_i(y,2q+3)$, and $U_i(y,2q+4)$; and 4 outputs $B_o(y,2q+3)$, $B_o(y,2q+4)$, $F_o(y,2q+3)$, and $F_o(y,2q+4)$. The stage (ring "y", stage "q+1") also consists of six 2:1 Muxes namely $F(y,2q+3)$, $F(y,2q+4)$, $U(y,2q+3)$, $U(y,2q+4)$, $B(y,2q+3)$, and $B(y,2q+4)$. The 2:1 Mux $F(y,2q+3)$ has two inputs namely $F_i(y,2q+3)$ and $F_i(y,2q+4)$ and has one output $F_o(y,2q+3)$. The 2:1 Mux $F(y,2q+4)$ has two inputs namely $F_i(y,2q+3)$ and $F_i(y,2q+4)$ and has one output $F_o(y,2q+4)$.

The 2:1 Mux $U(y,2q+3)$ has two inputs namely $U_i(y,2q+3)$ and $F_o(y,2q+3)$ and has one output $U_o(y,2q+3)$. The 2:1 Mux $U(y,2q+4)$ has two inputs namely $U_i(y,2q+4)$

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

and $Fo(y,2q+4)$ and has one output $Uo(y,2q+4)$. The 2:1 Mux $B(y,2q+3)$ has two inputs namely $Uo(y,2q+3)$ and $Uo(y,2q+4)$ and has one output $Bo(y,2q+3)$. The 2:1 Mux $B(y,2q+4)$ has two inputs namely $Uo(y,2q+3)$ and $Uo(y,2q+4)$ and has one output $Bo(y,2q+4)$.

5 The output $Fo(y,2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $Fi(y,2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $Bo(y,2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $Ui(y,2q+1)$ of the stage (ring “y”, stage “q”).

 The output $Fo(x,2p+1)$ of the stage (ring “x”, stage “p”) is connected via the wire
10 Hop(1,2) to the input $Ui(y,2q+2)$ of the stage (ring “y”, stage “q”). The output $Fo(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input $Fi(y,2q+4)$ of the stage (ring “y”, stage “q+1”).

 The output $Fo(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire
Hop(2,1) to the input $Ui(x,2p+1)$ of the stage (ring “x”, stage “p”). The output
15 $Bo(y,2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to the input $Ui(x,2p+2)$ of the stage (ring “x”, stage “p”).

 Just like in diagram 300A of FIG. 3A, in diagram 300B of FIG. 3B, in diagram
300C of FIG. 3C, diagram 300D of FIG. 3D, and in diagram 300E of FIG. 3E, the wires
Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are either internal hop wires or horizontal
20 external hop wires or vertical external hop wires (hereinafter alternatively referred to as
“cross links” or “cross middle links”).

 The diagram 400A of FIG. 4A and 400B of FIG. 4B are different embodiments of
all the connections between two arbitrary stages in two different rings of the same block
or two different rings of different blocks of 2D-grid 800. Referring to diagram 400A in
25 FIG. 4A illustrates all the connections between an arbitrary stage of a ring namely the
stages (ring “x”, stage “p”), and another arbitrary stage of any other ring namely the
stages (ring “y”, stage “q”) of the complete multi-stage hierarchical network

$$V_{Comb}(N_1, N_2, d, s).$$

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The stage (ring “x”, stage “p”) consists of 8 inputs namely $R_i(x,2p+1)$, $R_i(x,2p+2)$, $U_i(x,2p+1)$, $U_i(x,2p+2)$, J_1 , K_1 , L_1 , and M_1 ; and 4 outputs $B_o(x,2p+1)$, $B_o(x,2p+2)$, $F_o(x,2p+1)$, and $F_o(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely $R(x,2p+1)$, $R(x,2p+2)$, $F(x,2p+1)$, $F(x,2p+2)$, $U(x,2p+1)$, $U(x,2p+2)$, $B(x,2p+1)$, and $B(x,2p+2)$. The 2:1 Mux $R(x,2p+1)$ has two inputs namely $R_i(x,2p+1)$ and J_1 and has one output $R_o(x,2p+1)$. The 2:1 Mux $R(x,2p+2)$ has two inputs namely $R_i(x,2p+2)$ and K_1 and has one output $R_o(x,2p+2)$. The 2:1 Mux $F(x,2p+1)$ has two inputs namely $R_o(x,2p+1)$ and $U_o(x,2p+2)$ and has one output $F_o(x,2p+1)$. The 2:1 Mux $F(x,2p+2)$ has two inputs namely $R_o(x,2p+2)$ and $U_o(x,2p+1)$ and has one output $F_o(x,2p+2)$.

The 2:1 Mux $U(x,2p+1)$ has two inputs namely $U_i(x,2p+1)$ and L_1 and has one output $U_o(x,2p+1)$. The 2:1 Mux $U(x,2p+2)$ has two inputs namely $U_i(x,2p+2)$ and M_1 and has one output $U_o(x,2p+2)$. The 2:1 Mux $B(x,2p+1)$ has two inputs namely $U_o(x,2p+1)$ and $R_o(x,2p+2)$ and has one output $B_o(x,2p+1)$. The 2:1 Mux $B(x,2p+2)$ has two inputs namely $U_o(x,2p+2)$ and $R_o(x,2p+1)$ and has one output $B_o(x,2p+2)$.

The stage (ring “y”, stage “q”) consists of 8 inputs namely $R_i(y,2q+1)$, $R_i(y,2q+2)$, $U_i(y,2q+1)$, $U_i(y,2q+2)$, J_3 , K_3 , L_3 , and M_3 ; and 4 outputs $B_o(y,2q+1)$, $B_o(y,2q+2)$, $F_o(y,2q+1)$, and $F_o(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of eight 2:1 Muxes namely $R(y,2q+1)$, $R(y,2q+2)$, $F(y,2q+1)$, $F(y,2q+2)$, $U(y,2q+1)$, $U(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The 2:1 Mux $R(y,2q+1)$ has two inputs namely $R_i(y,2q+1)$ and J_3 and has one output $R_o(y,2q+1)$. The 2:1 Mux $R(y,2q+2)$ has two inputs namely $R_i(y,2q+2)$ and K_3 and has one output $R_o(y,2q+2)$. The 2:1 Mux $F(y,2q+1)$ has two inputs namely $R_o(y,2q+1)$ and $U_o(y,2q+2)$ and has one output $F_o(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $R_o(y,2q+2)$ and $U_o(y,2q+1)$ and has one output $F_o(y,2q+2)$.

The 2:1 Mux $U(y,2q+1)$ has two inputs namely $U_i(y,2q+1)$ and L_3 , and has one output $U_o(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $U_i(y,2q+2)$ and M_3 , and has one output $U_o(y,2q+2)$. The 2:1 Mux $B(y,2q+1)$ has two inputs namely $U_o(y,2q+1)$ and $R_o(y,2q+2)$ and has one output $B_o(y,2q+1)$. The 2:1 Mux $B(y,2q+2)$ has two inputs namely $U_o(y,2q+2)$ and $R_o(y,2q+1)$ and has one output $B_o(y,2q+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The output $Fo(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input $Ri(y,2q+2)$ of the stage (ring “y”, stage “q”). The output $Bo(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire Hop(1,2) to the input $Ui(x,2p+2)$ of the stage (ring “x”, stage “p”).

5 Ring “x” and ring “y” may or may not belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. If ring “x” and ring “y” belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1) and Hop(1,2) are hereinafter called “internal hop wires”. For example if “x = 2” and “y = 3” and both the ring 2 and ring 3 belong to the same block (9,9) of
10 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are “internal hop wires”.

If ring “x” and ring “y” belong to the different blocks of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1) and Hop(1,2) are hereinafter called “external hop wires”. The external hop wires Hop(1,1) and Hop(1,2) may be horizontal wires or vertical wires. The length of the external hop wires is
15 Manhattan distance between the corresponding blocks, hereinafter “hop length”. For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (1,6) of 2D-grid 800 then the external hop wires are hereinafter called “horizontal external hop wires”. And the hop length of the horizontal hop wires Hop(1,1) and Hop(1,2) is given by $6 - 1 = 5$. Similarly if ring “x” and ring “y” belong to two blocks in the same horizontal row of
20 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are horizontal external hop wires.

For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (9,1) of 2D-grid 800 then the external hop wires are hereinafter called “vertical external hop wires”. And the hop length of the vertical hop wires Hop(1,1) and Hop(1,2) is given by $9 - 1 = 8$. Similarly if ring “x” and ring “y” belong to two blocks in the same vertical
25 column of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are vertical external hop wires. External hop wires are typically horizontal or vertical according to the current invention.

Referring to diagram 400B in FIG. 4B illustrates all the connections between an arbitrary stage of a ring namely the stages (ring “x”, stage “p”), and another arbitrary

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

stage of any other ring namely the stages (ring “y”, stage “q”) of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 8 inputs namely $Ri(x, 2p+1)$, $Ri(x, 2p+2)$, $Ui(x, 2p+1)$, $Ui(x, 2p+2)$, $J1$, $K1$, $L1$, and $M1$; and 4 outputs $Bo(x, 2p+1)$, $Bo(x, 2p+2)$, $Fo(x, 2p+1)$, and $Fo(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of four 4:1 Muxes namely $F(x, 2p+1)$, $F(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 4:1 Mux $F(x, 2p+1)$ has four inputs namely $Ri(x, 2p+1)$, $Ri(x, 2p+2)$, $Ui(x, 2p+2)$, and $J1$ and has one output $Fo(x, 2p+1)$. The 4:1 Mux $F(x, 2p+2)$ has four inputs namely $Ri(x, 2p+1)$, $Ri(x, 2p+2)$, $Ui(x, 2p+1)$, and $K1$ and has one output $Fo(x, 2p+2)$.

10 The 4:1 Mux $B(x, 2p+1)$ has four inputs namely $Ui(x, 2p+1)$, $Ui(x, 2p+2)$, $Ri(x, 2p+2)$, and $L1$ and has one output $Bo(x, 2p+1)$. The 2:1 Mux $B(x, 2p+2)$ has two inputs namely $Ui(x, 2p+1)$, $Ui(x, 2p+2)$, $Ri(x, 2p+1)$, and $M1$ and has one output $Bo(x, 2p+2)$.

The stage (ring “y”, stage “q”) consists of 8 inputs namely $Ri(y, 2q+1)$, $Ri(y, 2q+2)$, $Ui(y, 2q+1)$, $Ui(y, 2q+2)$, $J3$, $K3$, $L3$, and $M3$; and 4 outputs $Bo(y, 2q+1)$, $Bo(y, 2q+2)$, $Fo(y, 2q+1)$, and $Fo(y, 2q+2)$. The stage (ring “y”, stage “q”) also consists of four 4:1 Muxes namely $F(y, 2q+1)$, $F(y, 2q+2)$, $B(y, 2q+1)$, and $B(y, 2q+2)$. The 4:1 Mux $F(y, 2q+1)$ has four inputs namely $Ri(y, 2q+1)$, $Ri(y, 2q+2)$, $Ui(y, 2q+2)$, and $J3$ and has one output $Fo(y, 2q+1)$. The 4:1 Mux $F(y, 2q+2)$ has four inputs namely $Ri(y, 2q+1)$, $Ri(y, 2q+2)$, $Ui(y, 2q+1)$, and $K3$ and has one output $Fo(y, 2q+2)$.

20 The 4:1 Mux $B(y, 2q+1)$ has four inputs namely $Ui(y, 2q+1)$, $Ui(y, 2q+2)$, $Ri(y, 2q+2)$, and $L3$, and has one output $Bo(y, 2q+1)$. The 4:1 Mux $B(y, 2q+2)$ has four inputs namely $Ui(y, 2q+1)$, $Ui(y, 2q+2)$, $Ri(y, 2q+1)$, and $M3$, and has one output $Bo(y, 2q+2)$.

25 The output $Fo(x, 2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input $Ri(y, 2q+2)$ of the stage (ring “y”, stage “q”). The output $Bo(y, 2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire Hop(1,2) to the input $Ui(x, 2p+2)$ of the stage (ring “x”, stage “p”).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Ring “x” and ring “y” may or may not belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. If ring “x” and ring “y” belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1) and Hop(1,2) are hereinafter called “internal hop wires”. For example
 5 if “x = 2” and “y = 3” and both the ring 2 and ring 3 belong to the same block (9,9) of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are “internal hop wires”.

If ring “x” and ring “y” belong to the different blocks of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1) and Hop(1,2) are hereinafter called “external hop wires”. The external hop wires Hop(1,1) and Hop(1,2)
 10 may be horizontal wires or vertical wires. The length of the external hop wires is Manhattan distance between the corresponding blocks, hereinafter “hop length”. For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (1,6) of 2D-grid 800 then the external hop wires are hereinafter called “horizontal external hop wires”. And the hop length of the horizontal hop wires Hop(1,1) and Hop(1,2) is given by $6 - 1 =$
 15 5. Similarly if ring “x” and ring “y” belong to two blocks in the same horizontal row of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are horizontal external hop wires.

For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (9,1) of 2D-grid 800 then the external hop wires are hereinafter called “vertical external hop wires”. And the hop length of the vertical hop wires Hop(1,1) and Hop(1,2) is given by 9
 20 $- 1 = 8$. Similarly if ring “x” and ring “y” belong to two blocks in the same vertical column of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are vertical external hop wires. External hop wires are typically horizontal or vertical according to the current invention.

The diagram 500A of FIG. 5A is an embodiment of all the connections with
 25 multi-drop hop wires, between two arbitrary successive stages in two different rings of different blocks of 2D-grid 800. Referring to diagram 500A in FIG. 5A illustrates all the connections with multi-drop hop wires, between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”,
 30 stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. The

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

multi-drop hop wires are also connected to two other stages (ring “a”, stage “s”) and (ring “b”, stage “t”) belonging to a third block.

The stage (ring “x”, stage “p”) consists of 8 inputs namely $R_i(x, 2p+1)$, $R_i(x, 2p+2)$, $U_i(x, 2p+1)$, $U_i(x, 2p+2)$, J_1 , K_1 , L_1 , and M_1 ; and 4 outputs $B_o(x, 2p+1)$, $B_o(x, 2p+2)$, $F_o(x, 2p+1)$, and $F_o(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely $R(x, 2p+1)$, $R(x, 2p+2)$, $F(x, 2p+1)$, $F(x, 2p+2)$, $U(x, 2p+1)$, $U(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 2:1 Mux $R(x, 2p+1)$ has two inputs namely $R_i(x, 2p+1)$ and J_1 , and has one output $R_o(x, 2p+1)$. The 2:1 Mux $R(x, 2p+2)$ has two inputs namely $R_i(x, 2p+2)$ and K_1 , and has one output $R_o(x, 2p+2)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $R_o(x, 2p+1)$ and $U_o(x, 2p+2)$, and has one output $F_o(x, 2p+1)$. The 2:1 Mux $F(x, 2p+2)$ has two inputs namely $R_o(x, 2p+2)$ and $U_o(x, 2p+1)$, and has one output $F_o(x, 2p+2)$.

The 2:1 Mux $U(x, 2p+1)$ has two inputs namely $U_i(x, 2p+1)$ and L_1 , and has one output $U_o(x, 2p+1)$. The 2:1 Mux $U(x, 2p+2)$ has two inputs namely $U_i(x, 2p+2)$ and M_1 , and has one output $U_o(x, 2p+2)$. The 2:1 Mux $B(x, 2p+1)$ has two inputs namely $U_o(x, 2p+1)$ and $R_o(x, 2p+2)$, and has one output $B_o(x, 2p+1)$. The 2:1 Mux $B(x, 2p+2)$ has two inputs namely $U_o(x, 2p+2)$ and $R_o(x, 2p+1)$, and has one output $B_o(x, 2p+2)$.

The stage (ring “x”, stage “p+1”) consists of 8 inputs namely $R_i(x, 2p+3)$, $R_i(x, 2p+4)$, $U_i(x, 2p+3)$, $U_i(x, 2p+4)$, J_2 , K_2 , L_2 , and M_2 ; and 4 outputs $B_o(x, 2p+3)$, $B_o(x, 2p+4)$, $F_o(x, 2p+3)$, and $F_o(x, 2p+4)$. The stage (ring “x”, stage “p+1”) also consists of eight 2:1 Muxes namely $R(x, 2p+3)$, $R(x, 2p+4)$, $F(x, 2p+3)$, $F(x, 2p+4)$, $U(x, 2p+3)$, $U(x, 2p+4)$, $B(x, 2p+3)$, and $B(x, 2p+4)$. The 2:1 Mux $R(x, 2p+3)$ has two inputs namely $R_i(x, 2p+3)$ and J_2 , and has one output $R_o(x, 2p+3)$. The 2:1 Mux $R(x, 2p+4)$ has two inputs namely $R_i(x, 2p+4)$ and K_2 , and has one output $R_o(x, 2p+4)$. The 2:1 Mux $F(x, 2p+3)$ has two inputs namely $R_o(x, 2p+3)$ and $U_o(x, 2p+4)$, and has one output $F_o(x, 2p+3)$. The 2:1 Mux $F(x, 2p+4)$ has two inputs namely $R_o(x, 2p+4)$ and $U_o(x, 2p+3)$, and has one output $F_o(x, 2p+4)$.

The 2:1 Mux $U(x, 2p+3)$ has two inputs namely $U_i(x, 2p+3)$ and L_2 , and has one output $U_o(x, 2p+3)$. The 2:1 Mux $U(x, 2p+4)$ has two inputs namely $U_i(x, 2p+4)$ and M_2 , and has one output $U_o(x, 2p+4)$. The 2:1 Mux $B(x, 2p+3)$ has two inputs namely

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$Uo(x,2p+3)$ and $Ro(x,2p+4)$, and has one output $Bo(x,2p+3)$. The 2:1 Mux $B(x,2p+4)$ has two inputs namely $Uo(x,2p+4)$ and $Ro(x,2p+3)$, and has one output $Bo(x,2p+4)$.

The output $Fo(x,2p+1)$ of the stage (ring “x”, stage “p”) is connected to the input $Ri(x,2p+3)$ of the stage (ring “x”, stage “p+1”). And the output $Bo(x,2p+3)$ of the stage (ring “x”, stage “p+1”) is connected to the input $Ui(x,2p+1)$ of the stage (ring “x”, stage “p”).

The stage (ring “y”, stage “q”) consists of 8 inputs namely $Ri(y,2q+1)$, $Ri(y,2q+2)$, $Ui(y,2q+1)$, $Ui(y,2q+2)$, $J3$, $K3$, $L3$, and $M3$; and 4 outputs $Bo(y,2q+1)$, $Bo(y,2q+2)$, $Fo(y,2q+1)$, and $Fo(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of eight 2:1 Muxes namely $R(y,2q+1)$, $R(y,2q+2)$, $F(y,2q+1)$, $F(y,2q+2)$, $U(y,2q+1)$, $U(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The 2:1 Mux $R(y,2q+1)$ has two inputs namely $Ri(y,2q+1)$ and $J3$, and has one output $Ro(y,2q+1)$. The 2:1 Mux $R(y,2q+2)$ has two inputs namely $Ri(y,2q+2)$ and $K3$, and has one output $Ro(y,2q+2)$. The 2:1 Mux $F(y,2q+1)$ has two inputs namely $Ro(y,2q+1)$ and $Uo(y,2q+2)$, and has one output $Fo(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $Ro(y,2q+2)$ and $Uo(y,2q+1)$ and has one output $Fo(y,2q+2)$.

The 2:1 Mux $U(y,2q+1)$ has two inputs namely $Ui(y,2q+1)$ and $L3$, and has one output $Uo(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $Ui(y,2q+2)$ and $M3$, and has one output $Uo(y,2q+2)$. The 2:1 Mux $B(y,2q+1)$ has two inputs namely $Uo(y,2q+1)$ and $Ro(y,2q+2)$, and has one output $Bo(y,2q+1)$. The 2:1 Mux $B(y,2q+2)$ has two inputs namely $Uo(y,2q+2)$ and $Ro(y,2q+1)$, and has one output $Bo(y,2q+2)$.

The stage (ring “y”, stage “q+1”) consists of 8 inputs namely $Ri(y,2q+3)$, $Ri(y,2q+4)$, $Ui(y,2q+3)$, $Ui(y,2q+4)$, $J4$, $K4$, $L4$, and $M4$; and 4 outputs $Bo(y,2q+3)$, $Bo(y,2q+4)$, $Fo(y,2q+3)$, and $Fo(y,2q+4)$. The stage (ring “y”, stage “q+1”) also consists of eight 2:1 Muxes namely $R(y,2q+3)$, $R(y,2q+4)$, $F(y,2q+3)$, $F(y,2q+4)$, $U(y,2q+3)$, $U(y,2q+4)$, $B(y,2q+3)$, and $B(y,2q+4)$. The 2:1 Mux $R(y,2q+3)$ has two inputs namely $Ri(y,2q+3)$ and $J4$, and has one output $Ro(y,2q+3)$. The 2:1 Mux $R(y,2q+4)$ has two inputs namely $Ri(y,2q+4)$ and $K4$, and has one output $Ro(y,2q+4)$. The 2:1 Mux $F(y,2q+3)$ has two inputs namely $Ro(y,2q+3)$ and $Uo(y,2q+4)$, and has one output

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Ro(y,2q+4) and Uo(y,2q+3), and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and L4, and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and M4,
5 and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Ro(y,2q+4), and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+4) and Ro(y,2q+3), and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring “y”, stage “q”) is connected to the input Ri(y,2q+3) of the stage (ring “y”, stage “q+1”). And the output Bo(y,2q+3) of the stage
10 (ring “y”, stage “q+1”) is connected to the input Ui(y,2q+1) of the stage (ring “y”, stage “q”).

The output Fo(x,2p+2) of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input Ri(y,2q+4) of the stage (ring “y”, stage “q+1”). The output Bo(x,2p+4) of the stage (ring “x”, stage “p+1”) is connected via the wire Hop(1,2) to the
15 input Ui(y,2q+2) of the stage (ring “y”, stage “q”).

The output Fo(y,2q+2) of the stage (ring “y”, stage “q”) is connected via the wire Hop(2,1) to the input Ri(x,2p+4) of the stage (ring “x”, stage “p+1”). The output Bo(y,2q+4) of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to the input Ui(x,2p+2) of the stage (ring “x”, stage “p”).

20 In various embodiments, the inputs J1, K1, L1, and M1 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J2, K2, L2, and M2 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J3, K3, L3, and M3 are
25 connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Finally the inputs J4, K4, L4, and M4 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The stage (ring "a", stage "s") consists of 8 inputs namely $R_i(a,2s+1)$, $R_i(a,2s+2)$, $U_i(a,2s+1)$, $U_i(a,2s+2)$, J5, K5, L5, and M5; and 4 outputs $B_o(a,2s+1)$, $B_o(a,2s+2)$, $F_o(a,2s+1)$, and $F_o(a,2s+2)$. The stage (ring "a", stage "s") also consists of eight 2:1 Muxes namely $R(a,2s+1)$, $R(a,2s+2)$, $F(a,2s+1)$, $F(a,2s+2)$, $U(a,2s+1)$, $U(a,2s+2)$, $B(a,2s+1)$, and $B(a,2s+2)$. The 2:1 Mux $R(a,2s+1)$ has two inputs namely $R_i(a,2s+1)$ and J5, and has one output $R_o(a,2s+1)$. The 2:1 Mux $R(a,2s+2)$ has two inputs namely $R_i(a,2s+2)$ and K5, and has one output $R_o(a,2s+2)$. The 2:1 Mux $F(a,2s+1)$ has two inputs namely $R_o(a,2s+1)$ and $U_o(a,2s+2)$, and has one output $F_o(a,2s+1)$. The 2:1 Mux $F(a,2s+2)$ has two inputs namely $R_o(a,2s+2)$ and $U_o(a,2s+1)$, and has one output $F_o(a,2s+2)$.

The 2:1 Mux $U(a,2s+1)$ has two inputs namely $U_i(a,2s+1)$ and L5, and has one output $U_o(a,2s+1)$. The 2:1 Mux $U(a,2s+2)$ has two inputs namely $U_i(a,2s+2)$ and M5, and has one output $U_o(a,2s+2)$. The 2:1 Mux $B(a,2s+1)$ has two inputs namely $U_o(a,2s+1)$ and $R_o(a,2s+2)$, and has one output $B_o(a,2s+1)$. The 2:1 Mux $B(a,2s+2)$ has two inputs namely $U_o(a,2s+2)$ and $R_o(a,2s+1)$, and has one output $B_o(a,2s+2)$.

The stage (ring "b", stage "t") consists of 8 inputs namely $R_i(b,2t+1)$, $R_i(b,2t+2)$, $U_i(b,2t+1)$, $U_i(b,2t+2)$, J6, K6, L6, and M6; and 4 outputs $B_o(b,2t+1)$, $B_o(b,2t+2)$, $F_o(b,2t+1)$, and $F_o(b,2t+2)$. The stage (ring "b", stage "t") also consists of eight 2:1 Muxes namely $R(b,2t+1)$, $R(b,2t+2)$, $F(b,2t+1)$, $F(b,2t+2)$, $U(b,2t+1)$, $U(b,2t+2)$, $B(b,2t+1)$, and $B(b,2t+2)$. The 2:1 Mux $R(b,2t+1)$ has two inputs namely $R_i(b,2t+1)$ and J6, and has one output $R_o(b,2t+1)$. The 2:1 Mux $R(b,2t+2)$ has two inputs namely $R_i(b,2t+2)$ and K6, and has one output $R_o(b,2t+2)$. The 2:1 Mux $F(b,2t+1)$ has two inputs namely $R_o(b,2t+1)$ and $U_o(b,2t+2)$, and has one output $F_o(b,2t+1)$. The 2:1 Mux $F(b,2t+2)$ has two inputs namely $R_o(b,2t+2)$ and $U_o(b,2t+1)$, and has one output $F_o(b,2t+2)$.

The 2:1 Mux $U(b,2t+1)$ has two inputs namely $U_i(b,2t+1)$ and L6, and has one output $U_o(b,2t+1)$. The 2:1 Mux $U(b,2t+2)$ has two inputs namely $U_i(b,2t+2)$ and M6, and has one output $U_o(b,2t+2)$. The 2:1 Mux $B(b,2t+1)$ has two inputs namely $U_o(b,2t+1)$ and $R_o(b,2t+2)$, and has one output $B_o(b,2t+1)$. The 2:1 Mux $B(b,2t+2)$ has two inputs namely $U_o(b,2t+2)$ and $R_o(b,2t+1)$, and has one output $B_o(b,2t+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The wire Hop(1,1) starting from the output $Fo(x,2p+2)$ of the stage (ring "x", stage "p") is also connected to L5 of the stage (ring "a", stage "s"), in addition to the input $Ri(y,2q+4)$ of the stage (ring "y", stage "q+1"). The stage (ring "x", stage "p"), the stage (ring "a", stage "s"), and the stage (ring "y", stage "q+1") may belong to three
 5 different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Therefore the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may not be equal to the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "y", stage "q+1"). For example the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring
 10 "a", stage "s") may be one where as the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y+1") may be two. In such a case the wire Hop(1,1) is called hereinafter a "multi-drop hop wire". The wire Hop(1,1) may be either horizontal hop wire or vertical hop wire. Also multi-drop hop wires are either horizontal external hop wires or vertical external hop wires. Similarly the hop
 15 length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be any number greater than or equal to one, and also the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y+1") may be any number greater or equal to one.

In general a multi-drop hop wire may be dropping or terminating in more than one
 20 different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. For example a multi-drop hop wire starting from one block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ may be terminating at three different blocks or four different blocks, etc.

The wire Hop(1,2) starting from the output $Bo(x,2p+4)$ of the stage (ring "x",
 25 stage "p+1") is also connected to J6 of the stage (ring "b", stage "t"), in addition to the input $Ui(y,2q+2)$ of the stage (ring "y", stage "q"). The wire Hop(1,2) is also an example of multi-drop hop wire when the stage (ring "x", stage "p+1"), the stage (ring "b", stage "t") and the stage (ring "y", stage "q") belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The wire Hop(2,1) starting from the output Fo(y,2q+2) of the stage (ring “y”, stage “q”) is also connected to M5 of the stage (ring “a”, stage “s”), in addition to the input Ri(x,2p+4) of the stage (ring “x”, stage “p+1”). The wire Hop(2,1) is also an example of multi-drop hop wire when the stage (ring “x”, stage “p+1”), the stage (ring “a”, stage “s”) and the stage (ring “y”, stage “q”) belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The wire Hop(2,2) starting from the output Bo(y,2q+4) of the stage (ring “y”, stage “q+1”) is also connected to K6 of the stage (ring “b”, stage “t”), in addition to the input Ui(x,2p+2) of the stage (ring “x”, stage “p”). The wire Hop(2,2) is also an example of multi-drop hop wire when the stage (ring “x”, stage “p”), the stage (ring “b”, stage “t”) and the stage (ring “y”, stage “q+1”) belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

In various embodiments, the inputs J5, K5, L5, and M5 are connected from any of the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Also the inputs J6, K6, L6, and M6 are connected from any of the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The diagram 600A of FIG. 6A and 600B of FIG. 6B are different embodiments of all the connections with multi-drop hop wires, between two arbitrary stages in two different rings of different blocks of 2D-grid 800. Referring to diagram 600A in FIG. 6A illustrates all the connections with multi-drop hop wires, between an arbitrary stage of a ring namely the stages (ring “x”, stage “p”), and another arbitrary stage of any other ring namely the stages (ring “y”, stage “q”) of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. The multi-drop hop wires are also connected to another stage (ring “a”, stage “s”) belonging to a third block.

The stage (ring “x”, stage “p”) consists of 8 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), J1, K1, L1, and M1; and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+1),

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and J1 and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and K1 and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Uo(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+2) and Uo(x,2p+1) and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and L1 and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and M1 and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Ro(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+2) and Ro(x,2p+1) and has one output Bo(x,2p+2).

The stage (ring "y", stage "q") consists of 8 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), J3, K3, L3, and M3; and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q") also consists of eight 2:1 Muxes namely R(y,2q+1), R(y,2q+2), F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and J3 and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Ri(y,2q+2) and K3 and has one output Ro(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Ro(y,2q+1) and Uo(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Ro(y,2q+2) and Uo(y,2q+1) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and L3, and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and M3, and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Ro(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+2) and Ro(y,2q+1) and has one output Bo(y,2q+2).

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Ri(y,2q+2) of the stage (ring "y", stage "q"). The output Bo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(1,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The wire Hop(1,1) starting from the output Fo(x,2p+2) of the stage (ring "x", stage "p") is also connected to L2 of the stage (ring "a", stage "s"), in addition to the input Ri(y,2q+2) of the stage (ring "y", stage "q"). The stage (ring "x", stage "p"), the stage (ring "a", stage "s"), and the stage (ring "y", stage "q") may belong to three
 5 different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Therefore the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may not be equal to the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "y", stage "q"). For example the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring
 10 "a", stage "s") may be one where as the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y") may be two. Hence the wire Hop(1,1) is a multi-drop hop wire. Also the wire Hop(1,1) is either horizontal external hop wire or vertical external hop wire. Similarly the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be any
 15 number greater than or equal to one, and also the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y") may be any number greater or equal to one.

The wire Hop(1,2) starting from the output Bo(y,2q+2) of the stage (ring "y", stage "q") is also connected to K2 of the stage (ring "a", stage "s"), in addition to the
 20 input Ui(x,2p+2) of the stage (ring "x", stage "p"). The wire Hop(1,2) is also an example of multi-drop hop wire when the stage (ring "x", stage "p"), the stage (ring "a", stage "s") and the stage (ring "y", stage "q") belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

In various embodiments, the inputs J2, K2, L2, and M2 are connected from any of
 25 the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Referring to diagram 600B in FIG. 6B illustrates all the connections with multi-drop hop wires, between an arbitrary stage of a ring namely the stages (ring "x", stage "p"), and another arbitrary stage of any other ring namely the stages (ring "y", stage "q")

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. The multi-drop hop wires are also connected to another stage (ring “a”, stage “s”) belonging to a third block.

The stage (ring “x”, stage “p”) consists of 8 inputs namely $Ri(x, 2p+1)$, $Ri(x, 2p+2)$, $Ui(x, 2p+1)$, $Ui(x, 2p+2)$, $J1$, $K1$, $L1$, and $M1$; and 4 outputs $Bo(x, 2p+1)$, $Bo(x, 2p+2)$, $Fo(x, 2p+1)$, and $Fo(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of four 4:1 Muxes namely $F(x, 2p+1)$, $F(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 4:1 Mux $F(x, 2p+1)$ has four inputs namely $Ri(x, 2p+1)$, $Ri(x, 2p+2)$, $Ui(x, 2p+2)$, and $J1$ and has one output $Fo(x, 2p+1)$. The 4:1 Mux $F(x, 2p+2)$ has four inputs namely $Ri(x, 2p+1)$, $Ri(x, 2p+2)$, $Ui(x, 2p+1)$, and $K1$ and has one output $Fo(x, 2p+2)$.

10 The 4:1 Mux $B(x, 2p+1)$ has four inputs namely $Ui(x, 2p+1)$, $Ui(x, 2p+2)$, $Ri(x, 2p+2)$, and $L1$ and has one output $Bo(x, 2p+1)$. The 2:1 Mux $B(x, 2p+2)$ has two inputs namely $Ui(x, 2p+1)$, $Ui(x, 2p+2)$, $Ri(x, 2p+1)$, and $M1$ and has one output $Bo(x, 2p+2)$.

The stage (ring “y”, stage “q”) consists of 8 inputs namely $Ri(y, 2q+1)$, $Ri(y, 2q+2)$, $Ui(y, 2q+1)$, $Ui(y, 2q+2)$, $J3$, $K3$, $L3$, and $M3$; and 4 outputs $Bo(y, 2q+1)$, $Bo(y, 2q+2)$, $Fo(y, 2q+1)$, and $Fo(y, 2q+2)$. The stage (ring “y”, stage “q”) also consists of four 4:1 Muxes namely $F(y, 2q+1)$, $F(y, 2q+2)$, $B(y, 2q+1)$, and $B(y, 2q+2)$. The 4:1 Mux $F(y, 2q+1)$ has four inputs namely $Ri(y, 2q+1)$, $Ri(y, 2q+2)$, $Ui(y, 2q+2)$, and $J3$ and has one output $Fo(y, 2q+1)$. The 4:1 Mux $F(y, 2q+2)$ has four inputs namely $Ri(y, 2q+1)$, $Ri(y, 2q+2)$, $Ui(y, 2q+1)$, and $K3$ and has one output $Fo(y, 2q+2)$.

20 The 4:1 Mux $B(y, 2q+1)$ has four inputs namely $Ui(y, 2q+1)$, $Ui(y, 2q+2)$, $Ri(y, 2q+2)$, and $L3$, and has one output $Bo(y, 2q+1)$. The 4:1 Mux $B(y, 2q+2)$ has four inputs namely $Ui(y, 2q+1)$, $Ui(y, 2q+2)$, $Ri(y, 2q+1)$, and $M3$, and has one output $Bo(y, 2q+2)$.

25 The output $Fo(x, 2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input $Ri(y, 2q+2)$ of the stage (ring “y”, stage “q”). The output $Bo(y, 2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire Hop(1,2) to the input $Ui(x, 2p+2)$ of the stage (ring “x”, stage “p”).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The wire Hop(1,1) starting from the output Fo(x,2p+2) of the stage (ring “x”, stage “p”) is also connected to L2 and J2 of the stage (ring “a”, stage “s”), in addition to the input Ri(y,2q+2) of the stage (ring “y”, stage “q”). The stage (ring “x”, stage “p”), the stage (ring “a”, stage “s”), and the stage (ring “y”, stage “q”) may belong to three
 5 different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Therefore the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “a”, stage “s”) may not be equal to the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “y”, stage “q”). For example the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring
 10 “a”, stage “s”) may be one where as the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “q”, stage “y”) may be two. Hence the wire Hop(1,1) is a multi-drop hop wire. Also the wire Hop(1,1) is either horizontal external hop wire or vertical external hop wire. Similarly the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “a”, stage “s”) may be any
 15 number greater than or equal to one, and also the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “q”, stage “y”) may be any number greater or equal to one.

The wire Hop(1,2) starting from the output Bo(y,2q+2) of the stage (ring “y”, stage “q”) is also connected to K2 and M2 of the stage (ring “a”, stage “s”), in addition to
 20 the input Ui(x,2p+2) of the stage (ring “x”, stage “p”). The wire Hop(1,2) is also an example of multi-drop hop wire when the stage (ring “x”, stage “p”), the stage (ring “a”, stage “s”) and the stage (ring “y”, stage “q”) belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

In various embodiments, the inputs J2, K2, L2, and M2 are connected from any of
 25 the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Referring to diagram 700A in FIG. 7A, illustrates, in one embodiment, the hop wire connections chart of a partial multi-stage hierarchical network
 $V_{Comb}(N_1, N_2, d, s)$ 100A or a partial multi-stage hierarchical network
 30 $V_{Comb}(N_1, N_2, d, s)$ 100B, or a partial multi-stage hierarchical network

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$V_{Comb}(N_1, N_2, d, s)$ 100C, with $m = 6$ and $n = 7$. The hop wire connections chart shows two rings namely ring 1 and ring 2. And there are $m+1 = 7$ stages in ring 1 and $n+1 = 8$ stages in ring 2.

The hop wire connections chart 700A illustrates how the hop wires are connected
 5 between any two successive stages of all the rings corresponding to a block of 2D-grid 800. "L_x" denotes an internal hop wire connection, where symbol "L" denotes internal hop wire and "x" is an integer. For example "L1" between the stages (ring 1, stage 0) and (ring 1, stage 1) denotes that the corresponding hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are connected to two successive stages of another ring in the same block or
 10 alternatively hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are internal hop wires. Since there is also "L1" between the stages (ring 2, stage 0) and (ring 2, stage 1), there are internal hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected between the stages (ring 1, stage 0) and (ring 1, stage 1) and the stages (ring 2, stage 0) and (ring 2, stage 1). Hence there can be only two "L1" labels in the hop wire
 15 connection chart 700A.

Similarly there are two "L2" labels in the hop wire connections chart 700A. Since the label "L2" is given between the stages (ring 1, stage 5) and (ring 1, stage 6) and also the label "L2" is given between the stages (ring 2, stage 3) and (ring 2, stage 4), there are corresponding internal hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2)
 20 connected between the stages (ring 1, stage 5) and (ring 1, stage 6) and the stages (ring 2, stage 3) and (ring 2, stage 4).

"V_x" denotes an external vertical hop wire, where symbol "V" denotes vertical external hop wire connections from blocks of the topmost row of 2D-grid 800 (i.e., row of blocks consisting of block (1,1), block (1,2), ..., and block (1,10)) to the same
 25 corresponding stages of the same numbered ring of another block that is directly down south, with "x" vertical hop length, where "x" is a positive integer. For example "V1" between the stages (ring 1, stage 1) and (ring 1, stage 2) denote that from block (1,1) of 2D-grid 800 to another block directly below it, which is block (2,1), since "V1" denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 1) and (ring 1, stage 2) of block (1,1) to (ring 1, stage 1) and (ring 1, stage 2) of block (2,1). It also means there are external hop wire connections
 30

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 1) and (ring 1, stage 2) of block (3,1) to (ring 1, stage 1) and (ring 1, stage 2) of block (4,1). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 1) and (ring 1, stage 2) of block (9,1) to (ring 1, stage 1) and (ring 1, stage 2) of block (10,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

Similarly “V3” between the stages (ring 2, stage 1) and (ring 2, stage 2) denote that from block (1,1) of 2D-grid 800 to another block below it and at a hop length of 3 which is block (4,1), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 1) and (ring 2, stage 2) of block (1,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (4,1). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 1) and (ring 2, stage 2) of block (2,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (5,1). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 1) and (ring 2, stage 2) of block (7,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (10,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

If there is no block that is directly below a block with hop length equal to 3 then there is no vertical external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (8,1) does not have any block that is directly below and with hop length equal to 3 then none of the vertical external hop wires are connected from (ring 2, stage 1) and (ring 2, stage 2) of block (8,1). Similarly from (ring 2, stage 1) and (ring 2, stage 2) of block (9,1) and from (ring 2, stage 1) and (ring 2, stage 2) of block (10,1), none of the vertical external hop wires are connected. Similarly vertical external hop wires are connected corresponding to “V5”, “V7” etc., labels given in the hop wire connections chart 700A.

“U_x” denotes an external vertical hop wire, where symbol “U” denotes vertical external hop wire connections starting from blocks that are “x” hop length below the topmost row of 2D-grid 800 (i.e., row of blocks consisting of block (1+x,1), block (1+x,2), ..., and block (1+x,10)) to the same corresponding stages of the same numbered ring of another block that is directly down below, with “x” vertical hop length, where “x”

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

is a positive integer. For example “U1” between the stages (ring 1, stage 2) and (ring 1, stage 3) denote that from block (2,1) of 2D-grid 800 to another block directly below it, which is block (3,1), since “U1” denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 2) and (ring 1, stage 3) of block (2,1) to (ring 1, stage 2) and (ring 1, stage 3) of block (3,1). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 2) and (ring 1, stage 3) of block (4,1) to (ring 1, stage 2) and (ring 1, stage 3) of block (5,1). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 2) and (ring 1, stage 3) of block (8,1) to (ring 1, stage 2) and (ring 1, stage 3) of block (9,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

If there is no block that is directly below a block with hop length equal to 1 then no vertical external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (10,1) does not have any block that is directly below and with hop length equal to 1 then none of the vertical external hop wires are connected from (ring 1, stage 2) and (ring 1, stage 3) of block (10,1). Similarly for all the blocks in each column from the topmost row up to the row “x”, no vertical external hop wires are connected to the corresponding (ring 1, stage 2) and (ring 1, stage 3).

Similarly “U3” between the stages (ring 2, stage 2) and (ring 2, stage 3) denote that starting from blocks that are 3 hop length below the topmost row of 2D-grid 800 (i.e., row of blocks consisting of block (4,1), block (4,2), ..., and block (4,10)) to the same corresponding stages of the same numbered ring of another block that is directly down below, with vertical hop length of 3, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected. For example from block (4,1) of 2D-grid 800 to another block below it and at a hop length of 3 which is block (7,1), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 2) and (ring 2, stage 3) of block (4,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (7,1). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 2) and (ring 2, stage 3) of block (5,1) to (ring 2, stage 2) and (ring 2, stage 3) of block (8,1). This pattern continues and finally there are

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 2) and (ring 2, stage 3) of block (7,1) to (ring 2, stage 2) and (ring 2, stage 3) of block (10,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

5 If there is no block that is directly below a block with hop length equal to 3 then no vertical external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (8,1) does not have any block that is directly below and with hop length equal to 3 then none of the vertical external hop wires are connected from (ring 2, stage 2) and (ring 2, stage 3) of block (8,1). Similarly from (ring
10 2, stage 2) and (ring 2, stage 3) of block (9,1) and from (ring 2, stage 2) and (ring 2, stage 3) of block (10,1), none of the vertical external hop wires are connected. Similarly vertical external hop wires are connected corresponding to “U5”, “U7” etc. labels given in the hop wire connections chart 700A.

 “Hx” denotes an external horizontal hop wire, where symbol “H” denotes
15 horizontal external hop wire connections from blocks of the leftmost column of 2D-grid 800 (i.e., column of blocks consisting of block (1,1), block (2,1), ..., and block (10,1)) to the same corresponding stages of the same numbered ring of another block that is directly to the right, with “x” horizontal hop length, where “x” is a positive integer. For example
20 “H1” between the stages (ring 1, stage 3) and (ring 1, stage 4) denote that from block (1,1) of 2D-grid 800 to another block directly to the right, which is block (1,2), since “H1” denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 3) and (ring 1, stage 4) of block (1,1) to (ring 1, stage 3) and (ring 1, stage 4) of block (1,2). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1,
25 stage 3) and (ring 1, stage 4) of block (1,3) to (ring 1, stage 3) and (ring 1, stage 4) of block (1,4). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 3) and (ring 1, stage 4) of block (9,1) to (ring 1, stage 3) and (ring 1, stage 4) of block (10,1). The same pattern continues for all the rows starting from the block in the leftmost block of each row.

30 Similarly “H3” between the stages (ring 2, stage 4) and (ring 2, stage 5) denote that from block (1,1) of 2D-grid 800 to another block to the right and at a hop length of 3

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

which is block (1,4), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 4) and (ring 2, stage 5) of block (1,1) to (ring 2, stage 4) and (ring 2, stage 5) of block (1,4). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 4) and (ring 2, stage 5) of block (1,2) to (ring 2, stage 4) and (ring 2, stage 5) of block (1,5). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 4) and (ring 2, stage 5) of block (1,7) to (ring 2, stage 4) and (ring 2, stage 5) of block (1,10). The same pattern continues for all the columns starting from the block in the leftmost column of each row.

10 If there is no block that is directly to the right with hop length equal to 3 then there is no horizontal external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (1,8) does not have any block that is directly to the right and with hop length equal to 3 then none of the horizontal external hop wires are connected from (ring 2, stage 4) and (ring 2, stage 5) of block (1,8).
15 Similarly from (ring 2, stage 4) and (ring 2, stage 5) of block (1,9) and from (ring 2, stage 4) and (ring 2, stage 5) of block (1,10), none of the horizontal external hop wires are connected. Similarly horizontal external hop wires are connected corresponding to "H5", "H7" etc., labels given in the hop wire connections chart 700A.

 "K_x" denotes an external horizontal hop wire, where symbol "K" denotes
20 horizontal external hop wire connections starting from blocks that are "x" hop length below the leftmost column of 2D-grid 800 (i.e., column of blocks consisting of block (1, 1+x), block (2, 1+x), ..., and block (10, 1+x)) to the same corresponding stages of the same numbered ring of another block that is directly to the right, with "x" horizontal hop length, where "x" is a positive integer. For example "K₁" between the stages (ring 1,
25 stage 4) and (ring 1, stage 5) denote that from block (1,2) of 2D-grid 800 to another block directly to the right, which is block (1,3), since "K₁" denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 4) and (ring 1, stage 5) of block (1,2) to (ring 1, stage 4) and (ring 1, stage 5) of block (1,3). It also means there are external hop wire connections Hop(1,1), Hop(1,2),
30 Hop(2,1), and Hop(2,2) from (ring 1, stage 4) and (ring 1, stage 4) of block (1,4) to (ring 1, stage 4) and (ring 1, stage 5) of block (1,5). This pattern continues and finally there are

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 4) and (ring 1, stage 5) of block (1,8) to (ring 1, stage 4) and (ring 1, stage 5) of block (1,9). The same pattern continues for all the rows starting from the block in the leftmost column of each row.

- 5 If there is no block that is directly to the right of a block with hop length equal to 1 then no horizontal external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (1,10) does not have any block that is directly to the right and with hop length equal to 1 then none of the horizontal external hop wires are connected from (ring 1, stage 4) and (ring 1, stage 5) of block (1,10).
- 10 Similarly for all the blocks in each row from the leftmost column up to the column “x”, no horizontal external hop wires are connected to the corresponding (ring 1, stage 4) and (ring 1, stage 5).

 Similarly “K3” between the stages (ring 2, stage 5) and (ring 2, stage 6) denote that starting from blocks that are 3 hop length to the right of the leftmost column of 2D-
 15 grid 800 (i.e., column of blocks consisting of block (1,4), block (2,4), ..., and block (10,4)) to the same corresponding stages of the same numbered ring of another block that is directly to the right, with horizontal hop length of 3, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected. For example from
 20 block (1,4) of 2D-grid 800 to another block to the right and at a hop length of 3 which is block (1,7), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 5) and (ring 2, stage 6) of block (1,4) to (ring 2, stage 5) and (ring 2, stage 6) of block (1,7). It also means there are external hop wire connections
 25 Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 5) and (ring 2, stage 6) of block (1,5) to (ring 2, stage 5) and (ring 2, stage 6) of block (1,8). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and
 Hop(2,2) from (ring 2, stage 5) and (ring 2, stage 6) of block (1,7) to (ring 2, stage 5) and (ring 2, stage 6) of block (1,10). The same pattern continues for all the rows starting from the block in the leftmost block of each row.

- If there is no block that is directly to the right of a block with hop length equal to
 30 3 then no horizontal external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (1,8) does not have any block that is

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

directly to the right and with hop length equal to 3 then none of the horizontal external hop wires are connected from (ring 2, stage 5) and (ring 2, stage 6) of block (1,8). Similarly from (ring 2, stage 5) and (ring 2, stage 6) of block (1,9) and from (ring 2, stage 5) and (ring 2, stage 6) of block (1,10), none of the horizontal external hop wires are
5 connected. Similarly horizontal external hop wires are connected corresponding to “K5”, “K7” etc. labels given in the hop wire connections chart 700A.

In general the hop length of an external vertical hop wire can be any positive number. Similarly the hop length of an external horizontal hop wire can be any positive number. The hop wire connections between two arbitrary successive stages in two
10 different rings of the same block or two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, and 300E of FIG. 3E. Similarly the multi-drop hop wire connections between two arbitrary successive stages in two different rings of different blocks described in diagram 700A of FIG. 7A
15 may be any one of the embodiments of either the diagrams 500A of FIG. 5A.

In accordance with the invention, the hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may also be any one of the embodiments of either the diagrams 400A of FIG. 4A and 400B of FIG. 4B. Similarly the multi-drop hop wire connections between two arbitrary
20 stages in two different rings of different blocks may also be any one of the embodiments of either the diagrams 600A of FIG. 6A or 600B of FIG. 6B.

In accordance with the current invention, either partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A of FIG. 1A or partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B of FIG. 1B, or partial multi-stage hierarchical network
25 $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C, corresponding to a block of 2D-grid of blocks 800 of FIG. 8, using any one of the embodiments of 200A-200E of FIGs. 2A-2E to implement a stage of a ring of the multi-stage hierarchical network, either by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks described in
30 diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, 300E of FIG. 3E, 500A of FIG. 5A, or by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may be any one of the embodiments of either the diagrams 400A of FIG. 4A, 400B of FIG. 4B, 600A of FIG. 6A, or 600B of FIG. 6B is very efficient in the reduction of the die size, power consumption, and for lower wire/path delay for higher performance for practical routing applications to particularly to set up broadcast, unicast and multicast connections. In general in accordance with the current invention, where N_1 and N_2 of the complete multi-stage hierarchical network

5 $V_{Comb}(N_1, N_2, d, s)$ may be arbitrarily large in size and also the 2D-grid size 800 may also be arbitrarily large in size in terms of both the number of rows and number of columns.

Delay Optimizations in Multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$:

The multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ according to the current invention can further be optimized to reduce the delay in the routed path of the connection. The delay optimized multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ is hereinafter denoted by $V_{D-Comb}(N_1, N_2, d, s)$. The delay optimizing embodiments of the stages of a ring are one of the diagrams namely 900A-900E of FIGs. 9A-9D, 1000A-1000F of FIGs. 10A-10F, and 1100A-1100C of FIGs. 11A-11C. The diagram 1200 of

15 FIG. 12, 1300 of FIG. 13, 1400 of FIG. 14, and 1500 of FIG. 15 are different embodiments for the implementation of delay optimizations with all the connections between two arbitrary successive stages in two different rings of the same block or two different rings of different blocks of 2D-grid 800.

FIG. 9A illustrates a stage (ring "k", stage "m") 900A consists of 5 inputs namely

25 $F_i(k, 2m+1)$, $F_i(k, 2m+2)$, $YF_i(k, 2m+1)$, $U_i(k, 2m+1)$, and $U_i(k, 2m+2)$; and 4 outputs $B_o(k, 2m+1)$, $B_o(k, 2m+2)$, $F_o(k, 2m+1)$, and $F_o(k, 2m+2)$. The stage (ring "k", stage "m") also consists of seven 2:1 Muxes namely $YF(k, 2m+1)$, $F(k, 2m+1)$, $F(k, 2m+2)$, $U(k, 2m+1)$, $U(k, 2m+2)$, $B(k, 2m+1)$, and $B(k, 2m+2)$. The 2:1 Mux $YF(k, 2m+1)$ has two inputs namely $F_i(k, 2m+1)$ and $YF_i(k, 2m+1)$ and has one output $YF_o(k, 2m+1)$. The 2:1

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Mux $F(k,2m+1)$ has two inputs namely $YF_o(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $YF_o(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 2:1 Mux $U(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $F_o(k,2m+1)$ and
 5 has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$
 and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs
 namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux
 $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output
 $B_o(k,2m+2)$.

10 FIG. 9B illustrates a stage (ring "k", stage "m") 900B consists of 5 inputs namely
 $F_i(k,2m+1)$, $F_i(k,2m+2)$, $YU_i(k,2m+1)$, $U_i(k,2m+1)$, and $U_i(k,2m+2)$; and 4 outputs
 $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring "k", stage "m")
 also consists of seven 2:1 Muxes namely $F(k,2m+1)$, $F(k,2m+2)$, $YF(k,2m+1)$,
 $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two
 15 inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux
 $F(k,2m+2)$ has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output
 $F_o(k,2m+2)$.

The 2:1 Mux $YU(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $YU_i(k,2m+1)$
 and has one output $YU_o(k,2m+1)$. The 2:1 Mux $U(k,2m+1)$ has two inputs namely
 20 $YU_o(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$
 has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The
 2:1 Mux $B(k,2m+1)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one
 output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and
 $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

25 FIG. 9C illustrates a stage (ring "k", stage "m") 900C consists of 5 inputs namely
 $F_i(k,2m+1)$, $F_i(k,2m+2)$, $UY_i(k,2m+1)$, $U_i(k,2m+1)$, and $U_i(k,2m+2)$; and 4 outputs
 $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring "k", stage "m")
 also consists of five 2:1 Muxes namely $F(k,2m+1)$, $F(k,2m+2)$, $U(k,2m+2)$, $B(k,2m+1)$,
 and $B(k,2m+2)$. The stage (ring "k", stage "m") also consists of one 3:1 Mux namely
 30 $UY(k,2m+1)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $F_i(k,2m+1)$ and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$F_i(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 3:1 Mux $UY(k,2m+1)$ has three inputs namely $U_i(k,2m+1)$, $UY_i(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $UY_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two
 5 inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $UY_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $UY_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

FIG. 9D illustrates a stage (ring "k", stage "m") 900D consists of 6 inputs namely
 10 $F_i(k,2m+1)$, $F_i(k,2m+2)$, $YF_i(k,2m+1)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $YU_i(k,2m+1)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring "k", stage "m") also consists of eight 2:1 Muxes namely $F(k,2m+1)$, $F(k,2m+2)$, $YF(k,2m+1)$, $U(k,2m+1)$, $U(k,2m+2)$, $YU(k,2m+1)$, $B(k,2m+1)$, and $B(k,2m+2)$. The 2:1 Mux $YF(k,2m+1)$ has two inputs namely $F_i(k,2m+1)$ and $YF_i(k,2m+1)$ and has one output
 15 $YF_o(k,2m+1)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $YF_o(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $YF_o(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 2:1 Mux $YU(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $YU_i(k,2m+1)$ and has one output $YU_o(k,2m+1)$. The 2:1 Mux $U(k,2m+1)$ has two inputs namely
 20 $YU_o(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

FIG. 9E illustrates a stage (ring "k", stage "m") 900E consists of 6 inputs namely
 25 $F_i(k,2m+1)$, $F_i(k,2m+2)$, $YF_i(k,2m+1)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $UY_i(k,2m+1)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring "k", stage "m") also consists of six 2:1 Muxes namely $F(k,2m+1)$, $F(k,2m+2)$, $YF(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The stage (ring "k", stage "m") also consists of
 30 one 3:1 Mux namely $UY(k,2m+1)$. The 2:1 Mux $YF(k,2m+1)$ has two inputs namely

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$F_i(k, 2m+1)$ and $YF_i(k, 2m+1)$ and has one output $YF_o(k, 2m+1)$. The 2:1 Mux $F(k, 2m+1)$ has two inputs namely $YF_o(k, 2m+1)$ and $F_i(k, 2m+2)$ and has one output $F_o(k, 2m+1)$. The 2:1 Mux $F(k, 2m+2)$ has two inputs namely $YF_o(k, 2m+1)$ and $F_i(k, 2m+2)$ and has one output $F_o(k, 2m+2)$.

5 The 3:1 Mux $UY(k, 2m+1)$ has three inputs namely $U_i(k, 2m+1)$, $UY_i(k, 2m+1)$ and $F_o(k, 2m+1)$ and has one output $UY_o(k, 2m+1)$. The 2:1 Mux $U(k, 2m+2)$ has two inputs namely $U_i(k, 2m+2)$ and $F_o(k, 2m+2)$ and has one output $U_o(k, 2m+2)$. The 2:1 Mux $B(k, 2m+1)$ has two inputs namely $UY_o(k, 2m+1)$ and $U_o(k, 2m+2)$ and has one output $B_o(k, 2m+1)$. The 2:1 Mux $B(k, 2m+2)$ has two inputs namely $UY_o(k, 2m+1)$ and
10 $U_o(k, 2m+2)$ and has one output $B_o(k, 2m+2)$.

FIG. 10A illustrates a stage (ring "k", stage "m") 1000A consists of 5 inputs namely $R_i(k, 2m+1)$, $R_i(k, 2m+2)$, $YR_i(k, 2m+1)$, $U_i(k, 2m+1)$, and $U_i(k, 2m+2)$; and 4 outputs $B_o(k, 2m+1)$, $B_o(k, 2m+2)$, $F_o(k, 2m+1)$, and $F_o(k, 2m+2)$. The stage (ring "k", stage "m") also consists of nine 2:1 Muxes namely $R(k, 2m+1)$, $R(k, 2m+2)$, $YR(k, 2m+1)$,
15 $F(k, 2m+1)$, $F(k, 2m+2)$, $U(k, 2m+1)$, $U(k, 2m+2)$, $B(k, 2m+1)$, and $B(k, 2m+2)$. The 2:1 Mux $YR(k, 2m+1)$ has two inputs namely $R_i(k, 2m+1)$ and $YR_i(k, 2m+1)$ and has one output $YR_o(k, 2m+1)$. The 2:1 Mux $R(k, 2m+1)$ has two inputs namely $YR_o(k, 2m+1)$ and $B_o(k, 2m+1)$ and has one output $R_o(k, 2m+1)$. The 2:1 Mux $R(k, 2m+2)$ has two inputs namely $R_i(k, 2m+2)$ and $B_o(k, 2m+2)$ and has one output $R_o(k, 2m+2)$. The 2:1 Mux
20 $F(k, 2m+1)$ has two inputs namely $R_o(k, 2m+1)$ and $R_o(k, 2m+2)$ and has one output $F_o(k, 2m+1)$. The 2:1 Mux $F(k, 2m+2)$ has two inputs namely $R_o(k, 2m+1)$ and $R_o(k, 2m+2)$ and has one output $F_o(k, 2m+2)$.

The 2:1 Mux $U(k, 2m+1)$ has two inputs namely $U_i(k, 2m+1)$ and $F_o(k, 2m+1)$ and has one output $U_o(k, 2m+1)$. The 2:1 Mux $U(k, 2m+2)$ has two inputs namely $U_i(k, 2m+2)$ and $F_o(k, 2m+2)$ and has one output $U_o(k, 2m+2)$. The 2:1 Mux $B(k, 2m+1)$ has two inputs namely $U_o(k, 2m+1)$ and $U_o(k, 2m+2)$ and has one output $B_o(k, 2m+1)$. The 2:1 Mux
25 $B(k, 2m+2)$ has two inputs namely $U_o(k, 2m+1)$ and $U_o(k, 2m+2)$ and has one output $B_o(k, 2m+2)$.

FIG. 10B illustrates a stage (ring "k", stage "m") 1000B consists of 5 inputs
30 namely $R_i(k, 2m+1)$, $R_i(k, 2m+2)$, $RY_i(k, 2m+1)$, $U_i(k, 2m+1)$, and $U_i(k, 2m+2)$; and 4

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of seven 2:1 Muxes namely $R(k,2m+2)$, $F(k,2m+1)$, $F(k,2m+2)$, $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of one 3:1 Mux namely $RY(k,2m+1)$. The 3:1 Mux $RY(k,2m+1)$ has three inputs
 5 namely $Ri(k,2m+1)$, $RYi(k,2m+1)$, and $Bo(k,2m+1)$, and has one output $RYo(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $Ri(k,2m+2)$ and $Bo(k,2m+2)$ and has one output $Ro(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $RYo(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $RYo(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+2)$.

10 The 2:1 Mux $U(k,2m+1)$ has two inputs namely $Ui(k,2m+1)$ and $Fo(k,2m+1)$ and has one output $Uo(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $Ui(k,2m+2)$ and $Fo(k,2m+2)$ and has one output $Uo(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $Uo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output $Bo(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $Uo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output
 15 $Bo(k,2m+2)$.

FIG. 10C illustrates a stage (ring “k”, stage “m”) 1000C consists of 5 inputs namely $Ri(k,2m+1)$, $Ri(k,2m+2)$, $Ui(k,2m+1)$, $Ui(k,2m+2)$, and $YUi(k,2m+1)$; and 4 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of nine 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$,
 20 $F(k,2m+2)$, $YU(k,2m+1)$, $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $Ri(k,2m+1)$ and $Bo(k,2m+1)$ and has one output $Ro(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $Ri(k,2m+2)$ and $Bo(k,2m+2)$ and has one output $Ro(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $Ro(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+1)$. The 2:1 Mux
 25 $F(k,2m+2)$ has two inputs namely $Ro(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+2)$.

The 2:1 Mux $YU(k,2m+1)$ has two inputs namely $Ui(k,2m+1)$ and $YUi(k,2m+1)$ and has one output $YUo(k,2m+1)$. The 2:1 Mux $U(k,2m+1)$ has two inputs namely $YUo(k,2m+1)$ and $Fo(k,2m+1)$ and has one output $Uo(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$
 30 has two inputs namely $Ui(k,2m+2)$ and $Fo(k,2m+2)$ and has one output $Uo(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $Uo(k,2m+1)$ and $Uo(k,2m+2)$ and has one

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

output $Bo(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $Uo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output $Bo(k,2m+2)$.

FIG. 10D illustrates a stage (ring “k”, stage “m”) 1000D consists of 5 inputs namely $Ri(k,2m+1)$, $Ri(k,2m+2)$, $Ui(k,2m+1)$, $Ui(k,2m+2)$, and $UYi(k,2m+1)$; and 4
 5 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of seven 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$, $F(k,2m+2)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of one 3:1 Mux namely $UY(k,2m+1)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $Ri(k,2m+1)$ and $Bo(k,2m+1)$ and has one output $Ro(k,2m+1)$. The 2:1 Mux
 10 $R(k,2m+2)$ has two inputs namely $Ri(k,2m+2)$ and $Bo(k,2m+2)$ and has one output $Ro(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $Ro(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $Ro(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+2)$.

The 3:1 Mux $UY(k,2m+1)$ has three inputs namely $Ui(k,2m+1)$, $UYi(k,2m+1)$,
 15 and $Fo(k,2m+1)$, and has one output $UYo(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $Ui(k,2m+2)$ and $Fo(k,2m+2)$ and has one output $Uo(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $UYo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output $Bo(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $UYo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output $Bo(k,2m+2)$.

FIG. 10E illustrates a stage (ring “k”, stage “m”) 1000E consists of 6 inputs namely $Ri(k,2m+1)$, $Ri(k,2m+2)$, $YRi(k,2m+1)$, $Ui(k,2m+1)$, $Ui(k,2m+2)$, and $YUi(k,2m+1)$; and 4 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$.
 The stage (ring “k”, stage “m”) also consists of ten 2:1 Muxes namely $YR(k,2m+1)$, $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$, $F(k,2m+2)$, $YU(k,2m+1)$, $U(k,2m+1)$, $U(k,2m+2)$,
 25 $B(k,2m+1)$, and $B(k,2m+2)$. The 2:1 Mux $YR(k,2m+1)$ has two inputs namely $Ri(k,2m+1)$ and $YRi(k,2m+1)$ and has one output $YRo(k,2m+1)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $YRo(k,2m+1)$ and $Bo(k,2m+1)$ and has one output $Ro(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $Ri(k,2m+2)$ and $Bo(k,2m+2)$ and has one output $Ro(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs
 30 namely $Ro(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+1)$. The 2:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$F(k,2m+2)$ has two inputs namely $Ro(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+2)$.

The 2:1 Mux $YU(k,2m+1)$ has two inputs namely $Ui(k,2m+1)$ and $YUi(k,2m+1)$ and has one output $YUo(k,2m+1)$. The 2:1 Mux $U(k,2m+1)$ has two inputs namely
 5 $YUo(k,2m+1)$ and $Fo(k,2m+1)$ and has one output $Uo(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $Ui(k,2m+2)$ and $Fo(k,2m+2)$ and has one output $Uo(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $Uo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output $Bo(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $Uo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output $Bo(k,2m+2)$.

10 FIG. 10F illustrates a stage (ring “k”, stage “m”) 1000F consists of 6 inputs namely $Ri(k,2m+1)$, $Ri(k,2m+2)$, $RYi(k,2m+1)$, $Ui(k,2m+1)$, $Ui(k,2m+2)$, and $UYi(k,2m+1)$; and 4 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of six 2:1 Muxes namely $R(k,2m+2)$, $F(k,2m+1)$, $F(k,2m+2)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The stage (ring “k”,
 15 stage “m”) also consists of two 3:1 Mux namely $RY(k,2m+1)$ and $UY(k,2m+1)$. The 3:1 Mux $RY(k,2m+1)$ has three inputs namely $Ri(k,2m+1)$, $RYi(k,2m+1)$, and $Bo(k,2m+1)$ and has one output $RYo(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $Ri(k,2m+2)$ and $Bo(k,2m+2)$ and has one output $Ro(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $RYo(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+1)$.
 20 The 2:1 Mux $F(k,2m+2)$ has two inputs namely $RYo(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+2)$.

The 3:1 Mux $UY(k,2m+1)$ has three inputs namely $Ui(k,2m+1)$, $UYi(k,2m+1)$, and $Fo(k,2m+1)$, and has one output $UYo(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $Ui(k,2m+2)$ and $Fo(k,2m+2)$ and has one output $Uo(k,2m+2)$. The 2:1
 25 Mux $B(k,2m+1)$ has two inputs namely $UYo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output $Bo(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $UYo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output $Bo(k,2m+2)$.

FIG. 11A illustrates a stage (ring “k”, stage “m”) 1100A consists of 5 inputs namely $Ri(k,2m+1)$, $Ri(k,2m+2)$, $FYi(k,2m+2)$, $Ui(k,2m+1)$, and $Ui(k,2m+2)$; and 4
 30 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring “k”,

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

stage “m”) also consists of seven 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$, $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of one 3:1 Mux namely $FY(k,2m+2)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $R_i(k,2m+1)$ and $B_o(k,2m+1)$ and has one output $R_o(k,2m+1)$. The 2:1 Mux

5 $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and $B_o(k,2m+2)$ and has one output $R_o(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $R_o(k,2m+1)$ and $R_o(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 3:1 Mux $FY(k,2m+2)$ has three inputs namely $R_o(k,2m+1)$, $R_o(k,2m+2)$, and $FY_i(k,2m+2)$, and has one output $FY_o(k,2m+2)$.

The 2:1 Mux $U(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $F_o(k,2m+1)$ and

10 has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $FY_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

15 FIG. 11B illustrates a stage (ring “k”, stage “m”) 1100B consists of 5 inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $BY_i(k,2m+2)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of seven 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$, $F(k,2m+2)$, $U(k,2m+1)$, $U(k,2m+2)$, and $B(k,2m+1)$. The stage (ring “k”, stage “m”) also

20 consists of one 3:1 Mux namely $BY(k,2m+2)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $R_i(k,2m+1)$ and $B_o(k,2m+1)$ and has one output $R_o(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and $B_o(k,2m+2)$ and has one output $R_o(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $R_o(k,2m+1)$ and $R_o(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs

25 namely $R_o(k,2m+1)$, and $R_o(k,2m+2)$, and has one output $F_o(k,2m+2)$.

The 2:1 Mux $U(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 3:1 Mux

30 $BY(k,2m+2)$ has three inputs namely $U_o(k,2m+1)$, $U_o(k,2m+2)$, and $BY_i(k,2m+2)$, and has one output $BY_o(k,2m+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

FIG. 11C illustrates a stage (ring “k”, stage “m”) 1100C consists of 6 inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $FY_i(k,2m+2)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $BY_i(k,2m+2)$; and 4 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of six 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$, $U(k,2m+1)$, $U(k,2m+2)$, and $B(k,2m+1)$. The stage (ring “k”, stage “m”) also consists of two 3:1 Muxes namely $FY(k,2m+2)$ and $BY(k,2m+2)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $R_i(k,2m+1)$ and $Bo(k,2m+1)$ and has one output $Ro(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and $Bo(k,2m+2)$ and has one output $Ro(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $Ro(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+1)$. The 3:1 Mux $FY(k,2m+2)$ has three inputs namely $Ro(k,2m+1)$, $Ro(k,2m+2)$, and $FY_i(k,2m+2)$, and has one output $FYo(k,2m+2)$.

The 2:1 Mux $U(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $Fo(k,2m+1)$ and has one output $Uo(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $FYo(k,2m+2)$ and has one output $Uo(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $Uo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output $Bo(k,2m+1)$. The 3:1 Mux $BY(k,2m+2)$ has three inputs namely $Uo(k,2m+1)$, $Uo(k,2m+2)$, and $BY_i(k,2m+2)$ and has one output $BYo(k,2m+2)$.

Referring to diagram 1200 in FIG. 12, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 5 inputs namely $R_i(x,2p+1)$, $R_i(x,2p+2)$, $U_i(x,2p+1)$, $U_i(x,2p+2)$, and $UY_i(x,2p+1)$; and 4 outputs $Bo(x,2p+1)$, $Bo(x,2p+2)$, $Fo(x,2p+1)$, and $Fo(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of seven 2:1 Muxes namely $R(x,2p+1)$, $R(x,2p+2)$, $F(x,2p+1)$, $F(x,2p+2)$, $U(x,2p+2)$, $B(x,2p+1)$, and $B(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of one 3:1 Mux namely $UY(x,2p+1)$. The 2:1 Mux $R(x,2p+1)$ has two inputs namely $R_i(x,2p+1)$ and $Bo(x,2p+1)$ and has one output $Ro(x,2p+1)$. The 2:1 Mux $R(x,2p+2)$ has two inputs namely $R_i(x,2p+2)$ and $Bo(x,2p+2)$ and has one output $Ro(x,2p+2)$. The 2:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$F(x,2p+1)$ has two inputs namely $Ro(x,2p+1)$ and $Ro(x,2p+2)$ and has one output $Fo(x,2p+1)$. The 2:1 Mux $F(x,2p+2)$ has two inputs namely $Ro(x,2p+1)$ and $Ro(x,2p+2)$ and has one output $Fo(x,2p+2)$.

The 3:1 Mux $UY(x,2p+1)$ has three inputs namely $Ui(x,2p+1)$, $UYi(x,2p+1)$, and $Fo(x,2p+1)$, and has one output $UYo(x,2p+1)$. The 2:1 Mux $U(x,2p+2)$ has two inputs namely $Ui(x,2p+2)$ and $Fo(x,2p+2)$ and has one output $Uo(x,2p+2)$. The 2:1 Mux $B(x,2p+1)$ has two inputs namely $UYo(x,2p+1)$ and $Uo(x,2p+2)$ and has one output $Bo(x,2p+1)$. The 2:1 Mux $B(x,2p+2)$ has two inputs namely $UYo(x,2p+1)$ and $Uo(x,2p+2)$ and has one output $Bo(x,2p+2)$.

The stage (ring "x", stage "p+1") consists of 5 inputs namely $Ri(x,2p+3)$, $Ri(x,2p+4)$, $RYi(x,2p+3)$, $Ui(x,2p+3)$, and $Ui(x,2p+4)$; and 4 outputs $Bo(x,2p+3)$, $Bo(x,2p+4)$, $Fo(x,2p+3)$, and $Fo(x,2p+4)$. The stage (ring "x", stage "p+1") also consists of seven 2:1 Muxes namely $R(x,2p+4)$, $F(x,2p+3)$, $F(x,2p+4)$, $U(x,2p+3)$, $U(x,2p+4)$, $B(x,2p+3)$, and $B(x,2p+4)$. The stage (ring "x", stage "p+1") also consists of one 3:1 Mux namely $RY(x,2p+3)$. The 3:1 Mux $RY(x,2p+3)$ has three inputs namely $Ri(x,2p+3)$, $RYi(x,2p+3)$, and $Bo(x,2p+3)$, and has one output $RYo(x,2p+3)$. The 2:1 Mux $R(x,2p+4)$ has two inputs namely $Ri(x,2p+4)$ and $Bo(x,2p+4)$ and has one output $Ro(x,2p+4)$. The 2:1 Mux $F(x,2p+3)$ has two inputs namely $RYo(x,2p+3)$ and $Ro(x,2p+4)$ and has one output $Fo(x,2p+3)$. The 2:1 Mux $F(x,2p+4)$ has two inputs namely $RYo(x,2p+3)$ and $Ro(x,2p+4)$ and has one output $Fo(x,2p+4)$.

The 2:1 Mux $U(x,2p+3)$ has two inputs namely $Ui(x,2p+3)$ and $Fo(x,2p+3)$ and has one output $Uo(x,2p+3)$. The 2:1 Mux $U(x,2p+4)$ has two inputs namely $Ui(x,2p+4)$ and $Fo(x,2p+4)$ and has one output $Uo(x,2p+4)$. The 2:1 Mux $B(x,2p+3)$ has two inputs namely $Uo(x,2p+3)$ and $Uo(x,2p+4)$ and has one output $Bo(x,2p+3)$. The 2:1 Mux $B(x,2p+4)$ has two inputs namely $Uo(x,2p+3)$ and $Uo(x,2p+4)$ and has one output $Bo(x,2p+4)$.

The output $Fo(x,2p+1)$ of the stage (ring "x", stage "p") is connected to the input $Ri(x,2p+3)$ of the stage (ring "x", stage "p+1"). And the output $Bo(x,2p+3)$ of the stage (ring "x", stage "p+1") is connected to the input $Ui(x,2p+1)$ of the stage (ring "x", stage "p").

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The stage (ring “y”, stage “q”) consists of 5 inputs namely $R_i(y, 2q+1)$, $R_i(y, 2q+2)$, $U_i(y, 2q+1)$, $U_i(y, 2q+2)$, and $YU_i(y, 2q+1)$; and 4 outputs $Bo(y, 2q+1)$, $Bo(y, 2q+2)$, $Fo(y, 2q+1)$, and $Fo(y, 2q+2)$. The stage (ring “y”, stage “q”) also consists of nine 2:1 Muxes namely $R(y, 2q+1)$, $R(y, 2q+2)$, $F(y, 2q+1)$, $F(y, 2q+2)$, $YU(y, 2q+1)$, $U(y, 2q+1)$, $U(y, 2q+2)$, $B(y, 2q+1)$, and $B(y, 2q+2)$. The 2:1 Mux $R(y, 2q+1)$ has two inputs namely $R_i(y, 2q+1)$ and $Bo(y, 2q+1)$ and has one output $Ro(y, 2q+1)$. The 2:1 Mux $R(y, 2q+2)$ has two inputs namely $R_i(y, 2q+2)$ and $Bo(y, 2q+2)$ and has one output $Ro(y, 2q+2)$. The 2:1 Mux $F(y, 2q+1)$ has two inputs namely $Ro(y, 2q+1)$ and $Ro(y, 2q+2)$ and has one output $Fo(y, 2q+1)$. The 2:1 Mux $F(y, 2q+2)$ has two inputs namely $Ro(y, 2q+1)$ and $Ro(y, 2q+2)$ and has one output $Fo(y, 2q+2)$.

The 2:1 Mux $YU(y, 2q+1)$ has two inputs namely $U_i(y, 2q+1)$ and $YU_i(y, 2q+1)$ and has one output $YUo(y, 2q+1)$. The 2:1 Mux $U(y, 2q+1)$ has two inputs namely $YUo(y, 2q+1)$ and $Fo(y, 2q+1)$ and has one output $Uo(y, 2q+1)$. The 2:1 Mux $U(y, 2q+2)$ has two inputs namely $U_i(y, 2q+2)$ and $Fo(y, 2q+2)$ and has one output $Uo(y, 2q+2)$. The 2:1 Mux $B(y, 2q+1)$ has two inputs namely $Uo(y, 2q+1)$ and $Uo(y, 2q+2)$ and has one output $Bo(y, 2q+1)$. The 2:1 Mux $B(y, 2q+2)$ has two inputs namely $Uo(y, 2q+1)$ and $Uo(y, 2q+2)$ and has one output $Bo(y, 2q+2)$.

The stage (ring “y”, stage “q+1”) consists of 5 inputs namely $R_i(y, 2q+3)$, $R_i(y, 2q+4)$, $YR_i(y, 2q+3)$, $U_i(y, 2q+3)$, and $U_i(y, 2q+4)$; and 4 outputs $Bo(y, 2q+3)$, $Bo(y, 2q+4)$, $Fo(y, 2q+3)$, and $Fo(y, 2q+4)$. The stage (ring “y”, stage “q+1”) also consists of nine 2:1 Muxes namely $R(y, 2q+3)$, $R(y, 2q+4)$, $YR(y, 2q+3)$, $F(y, 2q+3)$, $F(y, 2q+4)$, $U(y, 2q+3)$, $U(y, 2q+4)$, $B(y, 2q+3)$, and $B(y, 2q+4)$. The 2:1 Mux $YR(y, 2q+3)$ has two inputs namely $R_i(y, 2q+3)$ and $YR_i(y, 2q+3)$ and has one output $YRo(y, 2q+3)$. The 2:1 Mux $R(y, 2q+3)$ has two inputs namely $YRo(y, 2q+3)$ and $Bo(y, 2q+3)$ and has one output $Ro(y, 2q+3)$. The 2:1 Mux $R(y, 2q+4)$ has two inputs namely $R_i(y, 2q+4)$ and $Bo(y, 2q+4)$ and has one output $Ro(y, 2q+4)$. The 2:1 Mux $F(y, 2q+3)$ has two inputs namely $Ro(y, 2q+3)$ and $Ro(y, 2q+4)$ and has one output $Fo(y, 2q+3)$. The 2:1 Mux $F(y, 2q+4)$ has two inputs namely $Ro(y, 2q+3)$ and $Ro(y, 2q+4)$ and has one output $Fo(y, 2q+4)$.

The 2:1 Mux $U(y, 2q+3)$ has two inputs namely $U_i(y, 2q+3)$ and $Fo(y, 2q+3)$ and has one output $Uo(y, 2q+3)$. The 2:1 Mux $U(y, 2q+4)$ has two inputs namely $U_i(y, 2q+4)$ and $Fo(y, 2q+4)$ and has one output $Uo(y, 2q+4)$. The 2:1 Mux $B(y, 2q+3)$ has two inputs

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

namely $Uo(y,2q+3)$ and $Uo(y,2q+4)$ and has one output $Bo(y,2q+3)$. The 2:1 Mux $B(y,2q+4)$ has two inputs namely $Uo(y,2q+3)$ and $Uo(y,2q+4)$ and has one output $Bo(y,2q+4)$.

The output $Fo(y,2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $Ri(y,2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $Bo(y,2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $Ui(y,2q+1)$ of the stage (ring “y”, stage “q”).

The output $Fo(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire $Hop(1,1)$ to two inputs namely input $Ri(y,2q+4)$ of the stage (ring “y”, stage “q+1”) and input $YUi(y,2q+1)$ of the stage (ring “y”, stage “q”). The output $Bo(x,2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire $Hop(1,2)$ to two inputs namely input $Ui(y,2q+2)$ of the stage (ring “y”, stage “q”) and input $YRi(y,2q+3)$ of the stage (ring “y”, stage “q+1”).

The output $Fo(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire $Hop(2,1)$ to two inputs namely input $Ri(x,2p+4)$ of the stage (ring “x”, stage “p+1”) and input $UYi(x,2p+1)$ of the stage (ring “x”, stage “p”). The output $Bo(y,2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire $Hop(2,2)$ to two inputs namely input $Ui(x,2p+2)$ of the stage (ring “x”, stage “p”) and input $RYi(x,2p+3)$ of the stage (ring “x”, stage “p+1”).

Referring to diagram 1300 in FIG. 13, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 6 inputs namely $Fi(x,2p+1)$, $Fi(x,2p+2)$, $YFi(x,2p+1)$, $Ui(x,2p+1)$, $Ui(x,2p+2)$, and $YUi(x,2p+1)$; and 4 outputs $Bo(x,2p+1)$, $Bo(x,2p+2)$, $Fo(x,2p+1)$, and $Fo(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely $F(x,2p+1)$, $F(x,2p+2)$, $YF(x,2p+1)$, $U(x,2p+1)$, $U(x,2p+2)$, $YU(x,2p+1)$, $B(x,2p+1)$, and $B(x,2p+2)$. The 2:1 Mux $YF(x,2p+1)$ has two inputs namely

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$F_i(x, 2p+1)$ and $YF_i(x, 2p+1)$ and has one output $YF_o(x, 2p+1)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $YF_o(x, 2p+1)$ and $F_i(x, 2p+2)$ and has one output $F_o(x, 2p+1)$. The 2:1 Mux $F(x, 2p+2)$ has two inputs namely $YF_o(x, 2p+1)$ and $F_i(x, 2p+2)$ and has one output $F_o(x, 2p+2)$.

5 The 2:1 Mux $YU(x, 2p+1)$ has two inputs namely $U_i(x, 2p+1)$ and $YU_i(x, 2p+1)$ and has one output $YU_o(x, 2p+1)$. The 2:1 Mux $U(x, 2p+1)$ has two inputs namely $YU_o(x, 2p+1)$ and $F_o(x, 2p+1)$ and has one output $U_o(x, 2p+1)$. The 2:1 Mux $U(x, 2p+2)$ has two inputs namely $U_i(x, 2p+2)$ and $F_o(x, 2p+2)$ and has one output $U_o(x, 2p+2)$. The 2:1 Mux $B(x, 2p+1)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one
10 output $B_o(x, 2p+1)$. The 2:1 Mux $B(x, 2p+2)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $B_o(x, 2p+2)$.

 The stage (ring "x", stage "p+1") consists of 6 inputs namely $R_i(x, 2p+3)$, $R_i(x, 2p+4)$, $YR_i(x, 2p+3)$, $U_i(x, 2p+3)$, $U_i(x, 2p+4)$, and $YU_i(x, 2p+3)$; and 4 outputs $B_o(x, 2p+3)$, $B_o(x, 2p+4)$, $F_o(x, 2p+3)$, and $F_o(x, 2p+4)$. The stage (ring "x", stage "p+1")
15 also consists of ten 2:1 Muxes namely $YR(x, 2p+3)$, $R(x, 2p+3)$, $R(x, 2p+4)$, $F(x, 2p+3)$, $F(x, 2p+4)$, $YU(x, 2p+3)$, $U(x, 2p+3)$, $U(x, 2p+4)$, $B(x, 2p+3)$, and $B(x, 2p+4)$. The 2:1 Mux $YR(x, 2p+3)$ has two inputs namely $R_i(x, 2p+3)$ and $YR_i(x, 2p+3)$ and has one output $YR_o(x, 2p+3)$. The 2:1 Mux $R(x, 2p+3)$ has two inputs namely $YR_o(x, 2p+3)$ and $B_o(x, 2p+3)$ and has one output $R_o(x, 2p+3)$. The 2:1 Mux $R(x, 2p+4)$ has two inputs
20 namely $R_i(x, 2p+4)$ and $B_o(x, 2p+4)$ and has one output $R_o(x, 2p+4)$. The 2:1 Mux $F(x, 2p+3)$ has two inputs namely $R_o(x, 2p+3)$ and $R_o(x, 2p+4)$ and has one output $F_o(x, 2p+3)$. The 2:1 Mux $F(x, 2p+4)$ has two inputs namely $R_o(x, 2p+3)$ and $R_o(x, 2p+4)$ and has one output $F_o(x, 2p+4)$.

 The 2:1 Mux $YU(x, 2p+3)$ has two inputs namely $U_i(x, 2p+3)$ and $YU_i(x, 2p+3)$
25 and has one output $YU_o(x, 2p+3)$. The 2:1 Mux $U(x, 2p+3)$ has two inputs namely $YU_o(x, 2p+3)$ and $F_o(x, 2p+3)$ and has one output $U_o(x, 2p+3)$. The 2:1 Mux $U(x, 2p+4)$ has two inputs namely $U_i(x, 2p+4)$ and $F_o(x, 2p+4)$ and has one output $U_o(x, 2p+4)$. The 2:1 Mux $B(x, 2p+3)$ has two inputs namely $U_o(x, 2p+3)$ and $U_o(x, 2p+4)$ and has one
30 output $B_o(x, 2p+3)$. The 2:1 Mux $B(x, 2p+4)$ has two inputs namely $U_o(x, 2p+3)$ and $U_o(x, 2p+4)$ and has one output $B_o(x, 2p+4)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The output $Fo(x,2p+1)$ of the stage (ring “x”, stage “p”) is connected to the input $Ri(x,2p+3)$ of the stage (ring “x”, stage “p+1”). And the output $Bo(x,2p+3)$ of the stage (ring “x”, stage “p+1”) is connected to the input $Ui(x,2p+1)$ of the stage (ring “x”, stage “p”).

5 The stage (ring “y”, stage “q”) consists of 6 inputs namely $Fi(y,2q+1)$, $Fi(y,2q+2)$, $YFi(y,2q+1)$, $Ui(y,2q+1)$, $Ui(y,2q+2)$, and $UYi(y,2q+1)$; and 4 outputs $Bo(y,2q+1)$, $Bo(y,2q+2)$, $Fo(y,2q+1)$, and $Fo(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of six 2:1 Muxes namely $F(y,2q+1)$, $F(y,2q+2)$, $YF(y,2q+1)$, $U(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of one 3:1 Mux namely
10 $UY(y,2q+1)$. The 2:1 Mux $YF(y,2q+1)$ has two inputs namely $Fi(y,2q+1)$ and $YFi(y,2q+1)$ and has one output $YFo(y,2q+1)$. The 2:1 Mux $F(y,2q+1)$ has two inputs namely $YFo(y,2q+1)$ and $Fi(y,2q+2)$ and has one output $Fo(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $YFo(y,2q+1)$ and $Fi(y,2q+2)$ and has one output $Fo(y,2q+2)$.

15 The 3:1 Mux $UY(y,2q+1)$ has three inputs namely $Ui(y,2q+1)$, $UYi(y,2q+1)$ and $Fo(y,2q+1)$ and has one output $UYo(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $Ui(y,2q+2)$ and $Fo(y,2q+2)$ and has one output $Uo(y,2q+2)$. The 2:1 Mux $B(y,2q+1)$ has two inputs namely $UYo(y,2q+1)$ and $Uo(y,2q+2)$ and has one output $Bo(y,2q+1)$. The 2:1 Mux $B(y,2q+2)$ has two inputs namely $UYo(y,2q+1)$ and
20 $Uo(y,2q+2)$ and has one output $Bo(y,2q+2)$.

The stage (ring “y”, stage “q+1”) consists of 6 inputs namely $Ri(y,2q+3)$, $Ri(y,2q+4)$, $RYi(y,2q+3)$, $Ui(y,2q+3)$, $Ui(y,2q+4)$, and $UYi(y,2q+3)$; and 4 outputs $Bo(y,2q+3)$, $Bo(y,2q+4)$, $Fo(y,2q+3)$, and $Fo(y,2q+4)$. The stage (ring “y”, stage “2q+1”) also consists of six 2:1 Muxes namely $R(y,2q+4)$, $F(y,2q+3)$, $F(y,2q+4)$, $U(y,2q+4)$,
25 $B(y,2q+3)$, and $B(y,2q+4)$. The stage (ring “y”, stage “2q+1”) also consists of two 3:1 Mux namely $RY(y,2q+3)$ and $UY(y,2q+3)$. The 3:1 Mux $RY(y,2q+3)$ has three inputs namely $Ri(y,2q+3)$, $RYi(y,2q+3)$, and $Bo(y,2q+3)$ and has one output $RYo(y,2q+3)$. The 2:1 Mux $R(y,2q+4)$ has two inputs namely $Ri(y,2q+4)$ and $Bo(y,2q+4)$ and has one output $Ro(y,2q+4)$. The 2:1 Mux $F(y,2q+3)$ has two inputs namely $RYo(y,2q+3)$ and
30 $Ro(y,2q+4)$ and has one output $Fo(y,2q+3)$. The 2:1 Mux $F(y,2q+4)$ has two inputs namely $RYo(y,2q+3)$ and $Ro(y,2q+4)$ and has one output $Fo(y,2q+4)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 3:1 Mux $UY(y,2q+3)$ has three inputs namely $U_i(y,2q+3)$, $UY_i(y,2q+3)$, and $Fo(y,2q+3)$, and has one output $UY_o(y,2q+3)$. The 2:1 Mux $U(y,2q+4)$ has two inputs namely $U_i(y,2q+4)$ and $Fo(y,2q+4)$ and has one output $U_o(y,2q+4)$. The 2:1 Mux $B(y,2q+3)$ has two inputs namely $UY_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output
 5 $Bo(y,2q+3)$. The 2:1 Mux $B(y,2q+4)$ has two inputs namely $UY_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output $Bo(y,2q+4)$.

The output $Fo(y,2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $R_i(y,2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $Bo(y,2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $U_i(y,2q+1)$ of the stage (ring “y”, stage
 10 “q”).

The output $Fo(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire $Hop(1,1)$ to two inputs namely input $R_i(y,2q+4)$ of the stage (ring “y”, stage “q+1”) and input $UY_i(y,2q+1)$ of the stage (ring “y”, stage “q”). The output $Bo(x,2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire $Hop(1,2)$ to two inputs namely input
 15 $U_i(y,2q+2)$ of the stage (ring “y”, stage “q”) and input $RY_i(y,2q+3)$ of the stage (ring “y”, stage “q+1”).

The output $Fo(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire $Hop(2,1)$ to two inputs namely input $R_i(x,2p+4)$ of the stage (ring “x”, stage “p+1”) and input $YU_i(x,2p+1)$ of the stage (ring “x”, stage “p”). The output $Bo(y,2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire $Hop(2,2)$ to two inputs namely input
 20 $U_i(x,2p+2)$ of the stage (ring “x”, stage “p”) and input $YR_i(x,2p+3)$ of the stage (ring “x”, stage “p+1”).

Referring to diagram 1400 in FIG. 14, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.
 25

The stage (ring “x”, stage “p”) consists of 5 inputs namely $Fi(x,2p+1)$, $Fi(x,2p+2)$, $YU_i(x,2p+1)$, $U_i(x,2p+1)$, and $U_i(x,2p+2)$; and 4 outputs $Bo(x,2p+1)$, $Bo(x,2p+2)$,

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$Fo(x,2p+1)$, and $Fo(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of seven 2:1 Muxes namely $F(x,2p+1)$, $F(x,2p+2)$, $YF(x,2p+1)$, $U(x,2p+1)$, $U(x,2p+2)$, $B(x,2p+1)$, and $B(x,2p+2)$. The 2:1 Mux $F(x,2p+1)$ has two inputs namely $Fi(x,2p+1)$ and $Fi(x,2p+2)$ and has one output $Fo(x,2p+1)$. The 2:1 Mux $F(x,2p+2)$ has two inputs namely $Fi(x,2p+1)$ and $Fi(x,2p+2)$ and has one output $Fo(x,2p+2)$.

The 2:1 Mux $YU(x,2p+1)$ has two inputs namely $Ui(x,2p+1)$ and $YUi(x,2p+1)$ and has one output $YUo(x,2p+1)$. The 2:1 Mux $U(x,2p+1)$ has two inputs namely $YUo(x,2p+1)$ and $Fo(x,2p+1)$ and has one output $Uo(x,2p+1)$. The 2:1 Mux $U(x,2p+2)$ has two inputs namely $Ui(x,2p+2)$ and $Fo(x,2p+2)$ and has one output $Uo(x,2p+2)$. The 2:1 Mux $B(x,2p+1)$ has two inputs namely $Uo(x,2p+1)$ and $Uo(x,2p+2)$ and has one output $Bo(x,2p+1)$. The 2:1 Mux $B(x,2p+2)$ has two inputs namely $Uo(x,2p+1)$ and $Uo(x,2p+2)$ and has one output $Bo(x,2p+2)$.

The stage (ring “x”, stage “p+1”) consists of 5 inputs namely $Fi(x,2p+3)$, $Fi(x,2p+4)$, $YFi(x,2p+3)$, $Ui(x,2p+3)$, and $Ui(x,2p+4)$; and 4 outputs $Bo(x,2p+3)$, $Bo(x,2p+4)$, $Fo(x,2p+3)$, and $Fo(x,2p+4)$. The stage (ring “x”, stage “p+1”) also consists of seven 2:1 Muxes namely $YF(x,2p+3)$, $F(x,2p+3)$, $F(x,2p+4)$, $U(x,2p+3)$, $U(x,2p+4)$, $B(x,2p+3)$, and $B(x,2p+4)$. The 2:1 Mux $YF(x,2p+3)$ has two inputs namely $Fi(x,2p+3)$ and $YFi(x,2p+3)$ and has one output $YFo(x,2p+3)$. The 2:1 Mux $F(x,2p+3)$ has two inputs namely $YFo(x,2p+3)$ and $Fi(x,2p+4)$ and has one output $Fo(x,2p+3)$. The 2:1 Mux $F(x,2p+4)$ has two inputs namely $YFo(x,2p+3)$ and $Fi(x,2p+4)$ and has one output $Fo(x,2p+4)$.

The 2:1 Mux $U(x,2p+3)$ has two inputs namely $Ui(x,2p+3)$ and $Fo(x,2p+3)$ and has one output $Uo(x,2p+3)$. The 2:1 Mux $U(x,2p+4)$ has two inputs namely $Ui(x,2p+4)$ and $Fo(x,2p+4)$ and has one output $Uo(x,2p+4)$. The 2:1 Mux $B(x,2p+3)$ has two inputs namely $Uo(x,2p+3)$ and $Uo(x,2p+4)$ and has one output $Bo(x,2p+3)$. The 2:1 Mux $B(x,2p+4)$ has two inputs namely $Uo(x,2p+3)$ and $Uo(x,2p+4)$ and has one output $Bo(x,2p+4)$.

The output $Fo(x,2p+1)$ of the stage (ring “x”, stage “p”) is connected to the input $Fi(x,2p+3)$ of the stage (ring “x”, stage “p+1”). And the output $Bo(x,2p+3)$ of the stage

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

(ring “x”, stage “p+1”) is connected to the input $U_i(x, 2p+1)$ of the stage (ring “x”, stage “p”).

The stage (ring “y”, stage “q”) consists of 5 inputs namely $F_i(y, 2q+1)$, $F_i(y, 2q+2)$, $UY_i(y, 2q+1)$, $U_i(y, 2q+1)$, and $U_i(y, 2q+2)$; and 4 outputs $Bo(y, 2q+1)$, $Bo(y, 2q+2)$, $Fo(y, 2q+1)$, and $Fo(y, 2q+2)$. The stage (ring “y”, stage “q”) also consists of five 2:1 Muxes namely $F(y, 2q+1)$, $F(y, 2q+2)$, $U(y, 2q+2)$, $B(y, 2q+1)$, and $B(y, 2q+2)$. The stage (ring “y”, stage “q”) also consists of one 3:1 Mux namely $UY(y, 2q+1)$. The 2:1 Mux $F(y, 2q+1)$ has two inputs namely $F_i(y, 2q+1)$ and $F_i(y, 2q+2)$ and has one output $Fo(y, 2q+1)$. The 2:1 Mux $F(y, 2q+2)$ has two inputs namely $F_i(y, 2q+1)$ and $F_i(y, 2q+2)$ and has one output $Fo(y, 2q+2)$.

The 3:1 Mux $UY(y, 2q+1)$ has three inputs namely $U_i(y, 2q+1)$, $UY_i(y, 2q+1)$ and $Fo(y, 2q+1)$ and has one output $UYo(y, 2q+1)$. The 2:1 Mux $U(y, 2q+2)$ has two inputs namely $U_i(y, 2q+2)$ and $Fo(y, 2q+2)$ and has one output $Uo(y, 2q+2)$. The 2:1 Mux $B(y, 2q+1)$ has two inputs namely $UYo(y, 2q+1)$ and $Uo(y, 2q+2)$ and has one output $Bo(y, 2q+1)$. The 2:1 Mux $B(y, 2q+2)$ has two inputs namely $UYo(y, 2q+1)$ and $Uo(y, 2q+2)$ and has one output $Bo(y, 2q+2)$.

The stage (ring “y”, stage “q+1”) consists of 5 inputs namely $F_i(y, 2q+3)$, $F_i(y, 2q+4)$, $YF_i(y, 2q+3)$, $U_i(y, 2q+3)$, and $U_i(y, 2q+4)$; and 4 outputs $Bo(y, 2q+3)$, $Bo(y, 2q+4)$, $Fo(y, 2q+3)$, and $Fo(y, 2q+4)$. The stage (ring “y”, stage “q+1”) also consists of seven 2:1 Muxes namely $YF(y, 2q+3)$, $F(y, 2q+3)$, $F(y, 2q+4)$, $U(y, 2q+3)$, $U(y, 2q+4)$, $B(y, 2q+3)$, and $B(y, 2q+4)$. The 2:1 Mux $YF(y, 2q+3)$ has two inputs namely $F_i(y, 2q+3)$ and $YF_i(y, 2q+3)$ and has one output $YFo(y, 2q+3)$. The 2:1 Mux $F(y, 2q+3)$ has two inputs namely $YFo(y, 2q+3)$ and $F_i(y, 2q+4)$ and has one output $Fo(y, 2q+3)$. The 2:1 Mux $F(y, 2q+4)$ has two inputs namely $YFo(y, 2q+3)$ and $F_i(y, 2q+4)$ and has one output $Fo(y, 2q+4)$.

The 2:1 Mux $U(y, 2q+3)$ has two inputs namely $U_i(y, 2q+3)$ and $Fo(y, 2q+3)$ and has one output $Uo(y, 2q+3)$. The 2:1 Mux $U(y, 2q+4)$ has two inputs namely $U_i(y, 2q+4)$ and $Fo(y, 2q+4)$ and has one output $Uo(y, 2q+4)$. The 2:1 Mux $B(y, 2q+3)$ has two inputs namely $Uo(y, 2q+3)$ and $Uo(y, 2q+4)$ and has one output $Bo(y, 2q+3)$. The 2:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$B(y,2q+4)$ has two inputs namely $U_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output $Bo(y,2q+4)$.

The output $Fo(y,2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $Fi(y,2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $Bo(y,2q+3)$ of the stage
5 (ring “y”, stage “q+1”) is connected to the input $Ui(y,2q+1)$ of the stage (ring “y”, stage “q”).

The output $Fo(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire $Hop(1,1)$ to two inputs namely input $Fi(y,2q+4)$ of the stage (ring “y”, stage “q+1”) and input $UYi(y,2q+1)$ of the stage (ring “y”, stage “q”). The output $Bo(x,2p+4)$ of the stage
10 (ring “x”, stage “p+1”) is connected via the wire $Hop(1,2)$ to two inputs namely input $Ui(y,2q+2)$ of the stage (ring “y”, stage “q”) and input $YFi(y,2q+3)$ of the stage (ring “y”, stage “q+1”).

The output $Fo(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire $Hop(2,1)$ to two inputs namely input $Fi(x,2p+4)$ of the stage (ring “x”, stage “p+1”) and
15 input $YUi(x,2p+1)$ of the stage (ring “x”, stage “p”). The output $Bo(y,2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire $Hop(2,2)$ to two inputs namely input $Ui(x,2p+2)$ of the stage (ring “x”, stage “p”) and input $YFi(x,2p+3)$ of the stage (ring “x”, stage “p+1”).

Referring to diagram 1500 in FIG. 15, illustrates all the connections between two
20 arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 5 inputs namely $Ri(x,2p+1)$,
25 $Ri(x,2p+2)$, $Ui(x,2p+1)$, $Ui(x,2p+2)$, and $BYi(x,2p+2)$; and 4 outputs $Bo(x,2p+1)$, $Bo(x,2p+2)$, $Fo(x,2p+1)$, and $Fo(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of seven 2:1 Muxes namely $R(x,2p+1)$, $R(x,2p+2)$, $F(x,2p+1)$, $F(x,2p+2)$, $U(x,2p+1)$, $U(x,2p+2)$, and $B(x,2p+1)$. The stage (ring “x”, stage “p”) also consists of one 3:1 Mux namely $BY(x,2p+2)$. The 2:1 Mux $R(x,2p+1)$ has two inputs namely $Ri(x,2p+1)$ and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Bo(x,2p+1) and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and Bo(x,2p+2) and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Ro(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+1), and Ro(x,2p+2),
5 and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 3:1 Mux
10 BY(x,2p+2) has three inputs namely Uo(x,2p+1), Uo(x,2p+2), and BYi(x,2p+2), and has one output BYo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 5 inputs namely Ri(x,2p+3), Ri(x,2p+4), FYi(x,2p+4), Ui(x,2p+3), and Ui(x,2p+4); and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists
15 of seven 2:1 Muxes namely R(x,2p+3), R(x,2p+4), F(x,2p+3), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The stage (ring "x", stage "p+1") also consists of one 3:1 Mux namely FY(x,2p+4). The 2:1 Mux R(x,2p+3) has two inputs namely Ri(x,2p+3) and Bo(x,2p+3) and has one output Ro(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs namely Ri(x,2p+4) and Bo(x,2p+4) and has one output Ro(x,2p+4). The 2:1 Mux
20 F(x,2p+3) has two inputs namely Ro(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+3). The 3:1 Mux FY(x,2p+4) has three inputs namely Ro(x,2p+3), Ro(x,2p+4), and FYi(x,2p+4), and has one output FYo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and Fo(x,2p+3) and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and FYo(x,2p+4) and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs
25 namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input
30 Ri(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

(ring “x”, stage “p+1”) is connected to the input $U_i(x, 2p+1)$ of the stage (ring “x”, stage “p”).

The stage (ring “y”, stage “q”) consists of 6 inputs namely $R_i(y, 2q+1)$, $R_i(y, 2q+2)$, $FY_i(y, 2q+2)$, $U_i(y, 2q+1)$, $U_i(y, 2q+2)$, and $BY_i(y, 2q+2)$; and 4 outputs
 5 $Bo(y, 2q+1)$, $Bo(y, 2q+2)$, $Fo(y, 2q+1)$, and $Fo(y, 2q+2)$. The stage (ring “y”, stage “q”) also consists of six 2:1 Muxes namely $R(y, 2q+1)$, $R(y, 2q+2)$, $F(y, 2q+1)$, $U(y, 2q+1)$, $U(y, 2q+2)$, and $B(y, 2q+1)$. The stage (ring “y”, stage “q”) also consists of two 3:1 Muxes namely $FY(y, 2q+2)$ and $BY(y, 2q+2)$. The 2:1 Mux $R(y, 2q+1)$ has two inputs namely $R_i(y, 2q+1)$ and $Bo(y, 2q+1)$ and has one output $Ro(y, 2q+1)$. The 2:1 Mux $R(y, 2q+2)$ has
 10 two inputs namely $R_i(y, 2q+2)$ and $Bo(y, 2q+2)$ and has one output $Ro(y, 2q+2)$. The 2:1 Mux $F(y, 2q+1)$ has two inputs namely $Ro(y, 2q+1)$ and $Ro(y, 2q+2)$ and has one output $Fo(y, 2q+1)$. The 3:1 Mux $FY(y, 2q+2)$ has three inputs namely $Ro(y, 2q+1)$, $Ro(y, 2q+2)$, and $FY_i(y, 2q+2)$, and has one output $FY_o(y, 2q+2)$.

The 2:1 Mux $U(y, 2q+1)$ has two inputs namely $U_i(y, 2q+1)$ and $Fo(y, 2q+1)$ and
 15 has one output $U_o(y, 2q+1)$. The 2:1 Mux $U(y, 2q+2)$ has two inputs namely $U_i(y, 2q+2)$ and $FY_o(y, 2q+2)$ and has one output $U_o(y, 2q+2)$. The 2:1 Mux $B(y, 2q+1)$ has two inputs namely $U_o(y, 2q+1)$ and $U_o(y, 2q+2)$ and has one output $Bo(y, 2q+1)$. The 3:1 Mux $BY(y, 2q+2)$ has three inputs namely $U_o(y, 2q+1)$, $U_o(y, 2q+2)$, and $BY_i(y, 2q+2)$ and has one output $BY_o(y, 2q+2)$.

20 The stage (ring “y”, stage “q+1”) consists of 5 inputs namely $Fi(y, 2q+3)$, $Fi(y, 2q+4)$, $YFi(y, 2q+3)$, $U_i(y, 2q+3)$, and $U_i(y, 2q+4)$; and 4 outputs $Bo(y, 2q+3)$, $Bo(y, 2q+4)$, $Fo(y, 2q+3)$, and $Fo(y, 2q+4)$. The stage (ring “y”, stage “q+1”) also consists of seven 2:1 Muxes namely $YF(y, 2q+3)$, $F(y, 2q+3)$, $F(y, 2q+4)$, $U(y, 2q+3)$, $U(y, 2q+4)$, $B(y, 2q+3)$, and $B(y, 2q+4)$. The 2:1 Mux $YF(y, 2q+3)$ has two inputs namely $Fi(y, 2q+3)$
 25 and $YFi(y, 2q+3)$ and has one output $YFo(y, 2q+3)$. The 2:1 Mux $F(y, 2q+3)$ has two inputs namely $YFo(y, 2q+3)$ and $Fi(y, 2q+4)$ and has one output $Fo(y, 2q+3)$. The 2:1 Mux $F(y, 2q+4)$ has two inputs namely $YFo(y, 2q+3)$ and $Fi(y, 2q+4)$ and has one output $Fo(y, 2q+4)$.

The 2:1 Mux $U(y, 2q+3)$ has two inputs namely $U_i(y, 2q+3)$ and $Fo(y, 2q+3)$ and
 30 has one output $U_o(y, 2q+3)$. The 2:1 Mux $U(y, 2q+4)$ has two inputs namely $U_i(y, 2q+4)$

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

and $Fo(y, 2q+4)$ and has one output $Uo(y, 2q+4)$. The 2:1 Mux $B(y, 2q+3)$ has two inputs namely $Uo(y, 2q+3)$ and $Uo(y, 2q+4)$ and has one output $Bo(y, 2q+3)$. The 2:1 Mux $B(y, 2q+4)$ has two inputs namely $Uo(y, 2q+3)$ and $Uo(y, 2q+4)$ and has one output $Bo(y, 2q+4)$.

5 The output $Fo(y, 2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $Fi(y, 2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $Bo(y, 2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $Ui(y, 2q+1)$ of the stage (ring “y”, stage “q”).

 The output $Fo(x, 2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire
10 Hop(1,1) to two inputs namely input $Fi(y, 2q+4)$ of the stage (ring “y”, stage “q+1”) and input $BYi(y, 2q+1)$ of the stage (ring “y”, stage “q”). The output $Bo(x, 2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire Hop(1,2) to two inputs namely input $Ui(y, 2q+2)$ of the stage (ring “y”, stage “q”) and input $YFi(y, 2q+3)$ of the stage (ring “y”, stage “q+1”).

15 The output $Fo(y, 2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire Hop(2,1) to two inputs namely input $Ri(x, 2p+4)$ of the stage (ring “x”, stage “p+1”) and input $BYi(x, 2p+1)$ of the stage (ring “x”, stage “p”). The output $Bo(y, 2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to two inputs namely input $Ui(x, 2p+2)$ of the stage (ring “x”, stage “p”) and input $YFi(x, 2p+4)$ of the stage (ring “x”,
20 stage “p+1”).

 In accordance with the current invention, either partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100A of FIG. 1A, or partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100B of FIG. 1B, or partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C, corresponding to a block of 2D-grid of
25 blocks 800 of FIG. 8, using any one of the embodiments of 200A-200F of FIGS. 2A-2F, 900A-900E of FIGS. 9A-9E, 1000A-1000F of FIGS. 10A-10F, 1100A-1100C of FIGS. 11A-11C to implement a stage of a ring of the multi-stage hierarchical network, either by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks
30 described in diagram 700A of FIG. 7A may be any one of the embodiments of either the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, 300E of FIG. 3E, 500A of FIG. 5A, 1200 of FIG. 12, 1300 of FIG. 13, 1400 of FIG. 14, and 1500 of FIG. 15 or by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may be any one of the embodiments of either the diagrams 400A of FIG. 4A, 400B of FIG. 4B, 600A of FIG. 6A, or 600B of FIG. 6B is very efficient in the reduction of the die size, power consumption, and highly optimized for lower wire/path delay for higher performance for practical routing applications to particularly to set up broadcast, unicast and multicast connections. In general in accordance with the current invention, where N_1 and N_2 of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ may be arbitrarily large in size and also the 2D-grid size 800 may also be arbitrarily large in size in terms of both the number of rows and number of columns.

1) Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in programmable integrated circuit applications. FIG. 16A2 illustrates the detailed diagram 1600A2 for the implementation of the diagram 1600A1 in programmable integrated circuit embodiments. Each crosspoint is implemented by a transistor coupled between the corresponding inlet link and outlet link, and a programmable cell in programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by transistor C(1,1) coupled between inlet link IL1 and outlet link OL1, and programmable cell P(1,1); crosspoint CP(1,2) is implemented by transistor C(1,2) coupled between inlet link IL1 and outlet link OL2, and programmable cell P(1,2); crosspoint CP(2,1) is implemented by transistor C(2,1) coupled between inlet link IL2 and outlet link OL1, and programmable cell P(2,1); and crosspoint CP(2,2) is implemented by transistor C(2,2) coupled between inlet link IL2 and outlet link OL2, and programmable cell P(2,2).

If the programmable cell is programmed ON, the corresponding transistor couples the corresponding inlet link and outlet link. If the programmable cell is programmed OFF, the corresponding inlet link and outlet link are not connected. For example if the programmable cell P(1,1) is programmed ON, the corresponding transistor C(1,1) couples the corresponding inlet link IL1 and outlet link OL1. If the programmable cell P(1,1) is

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

programmed OFF, the corresponding inlet link IL1 and outlet link OL1 are not connected. In volatile programmable integrated circuit embodiments the programmable cell may be an SRAM (Static Random Address Memory) cell. In non-volatile programmable integrated circuit embodiments the programmable cell may be a Flash memory cell. Also
5 the programmable integrated circuit embodiments may implement field programmable logic arrays (FPGA) devices, or programmable Logic devices (PLD), or Application Specific Integrated Circuits (ASIC) embedded with programmable logic circuits or 3D-FPGAs.

FIG. 16A2 also illustrates a buffer B1 on inlet link IL2. The signals driven along
10 inlet link IL2 are amplified by buffer B1. Buffer B1 can be inverting or non-inverting buffer. Buffers such as B1 are used to amplify the signal in links which are usually long.

In other embodiments all the $d * d$ switches described in the current invention are also implemented using muxes of different sizes controlled by SRAM cells or flash cells etc.

15 2) One-time Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in one-time programmable integrated circuit applications. FIG. 16A3 illustrates the detailed diagram 1600A3 for the implementation of the diagram 1600A1 in one-time programmable integrated circuit embodiments. Each crosspoint is implemented by a via coupled
20 between the corresponding inlet link and outlet link in one-time programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by via V(1,1) coupled between inlet link IL1 and outlet link OL1; crosspoint CP(1,2) is implemented by via V(1,2) coupled between inlet link IL1 and outlet link OL2; crosspoint CP(2,1) is implemented by via V(2,1) coupled between inlet link IL2 and outlet link OL1; and
25 crosspoint CP(2,2) is implemented by via V(2,2) coupled between inlet link IL2 and outlet link OL2.

If the via is programmed ON, the corresponding inlet link and outlet link are permanently connected which is denoted by thick circle at the intersection of inlet link and outlet link. If the via is programmed OFF, the corresponding inlet link and outlet link
30 are not connected which is denoted by the absence of thick circle at the intersection of

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

inlet link and outlet link. For example in the diagram 1600A3 the via V(1,1) is programmed ON, and the corresponding inlet link IL1 and outlet link OL1 are connected as denoted by thick circle at the intersection of inlet link IL1 and outlet link OL1; the via V(2,2) is programmed ON, and the corresponding inlet link IL2 and outlet link OL2 are connected as denoted by thick circle at the intersection of inlet link IL2 and outlet link OL2; the via V(1,2) is programmed OFF, and the corresponding inlet link IL1 and outlet link OL2 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL1 and outlet link OL2; the via V(2,1) is programmed OFF, and the corresponding inlet link IL2 and outlet link OL1 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL2 and outlet link OL1. One-time programmable integrated circuit embodiments may be anti-fuse based programmable integrated circuit devices or mask programmable structured ASIC devices.

3) Integrated Circuit Placement and Route Embodiments:

All the embodiments disclosed in the current invention are useful in Integrated Circuit Placement and Route applications, for example in ASIC backend Placement and Route tools. FIG. 16A4 illustrates the detailed diagram 1600A4 for the implementation of the diagram 1600A1 in Integrated Circuit Placement and Route embodiments. In an integrated circuit since the connections are known a-priori, the switch and crosspoints are actually virtual. However the concept of virtual switch and virtual crosspoint using the embodiments disclosed in the current invention reduces the number of required wires, wire length needed to connect the inputs and outputs of different netlists and the time required by the tool for placement and route of netlists in the integrated circuit.

Each virtual crosspoint is used to either to hardwire or provide no connectivity between the corresponding inlet link and outlet link. Specifically crosspoint CP(1,1) is implemented by direct connect point DCP(1,1) to hardwire (i.e., to permanently connect) inlet link IL1 and outlet link OL1 which is denoted by the thick circle at the intersection of inlet link IL1 and outlet link OL1; crosspoint CP(2,2) is implemented by direct connect point DCP(2,2) to hardwire inlet link IL2 and outlet link OL2 which is denoted by the thick circle at the intersection of inlet link IL2 and outlet link OL2. The diagram 1600A4 does not show direct connect point DCP(1,2) and direct connect point DCP(1,3) since they are not needed and in the hardware implementation they are eliminated.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Alternatively inlet link IL1 needs to be connected to outlet link OL1 and inlet link IL1 does not need to be connected to outlet link OL2. Also inlet link IL2 needs to be connected to outlet link OL2 and inlet link IL2 does not need to be connected to outlet link OL1. Furthermore in the example of the diagram 1600A4, there is no need to drive the signal of inlet link IL1 horizontally beyond outlet link OL1 and hence the inlet link IL1 is not even extended horizontally until the outlet link OL2. Also the absence of direct connect point DCP(2,1) illustrates there is no need to connect inlet link IL2 and outlet link OL1.

In summary in integrated circuit placement and route tools, the concept of virtual switches and virtual cross points is used during the implementation of the placement & routing algorithmically in software, however during the hardware implementation cross points in the cross state are implemented as hardwired connections between the corresponding inlet link and outlet link, and in the bar state are implemented as no connection between inlet link and outlet link.

15

3) More Application Embodiments:

All the embodiments disclosed in the current invention are also useful in the design of SoC interconnects, Field programmable interconnect chips, parallel computer systems and in time-space-time switches.

20

Scheduling Method Embodiments the multi-stage hierarchical network

$$V_{Comb}(N_1, N_2, d, s):$$

FIG. 17 shows a high-level flowchart of a scheduling method 1700, in one embodiment executed to setup multicast and unicast connections in the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ disclosed in this invention. According to this embodiment, the set of multicast connections are initialized to the beginning of the set in

25

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

act 1710. Then the control goes to act 1720. In act 1720, next multicast connection is selected in sequence form the set of multicast connections. Then the control goes to act 1730.

In act 1730 it is checked if this is the next multicast connection in sequence is
5 NULL or i.e. all the multicast connections are scheduled. If act 1730 results “no”, that is there are more multicast connections to be scheduled the control goes to act 1740. In act 1740 it is checked if this multicast connection is being scheduled for the first time. Or if it is not scheduled for the first time, it is checked if any one of the links taken by this multicast connection is oversubscribed by any other multicast connection is checked. If
10 either the multicast connection is being scheduled for the first time or if any one of the links taken by this multicast connection is oversubscribed the control goes to act 1750. Otherwise control goes to act 1720 where the next multicast connection will be selected. So act 1720, act 1730, and act 1740 are executed in a loop.

In act 1750 the multicast connection is not being scheduled for the first time and
15 since at least one of the links taken by this multicast connection is oversubscribed, the complete path taken this multicast connection is cleared or the multicast connection’s path is ripped. Then the control goes to act 1760. In act 1760, using the well-known A* search algorithm the least cost path from its source outlet link of the computational block to all the target inlet links of the corresponding computational blocks are found out one
20 after another target inlet links. The cost function used is based on the Manhattan distance between the target inlet link’s block and source outlet link’s block by taking the delays on each wire is considered in the cost function and also that longest wires are chosen first in the A* search algorithm.

According to the current invention, before scheduling the set of multicast
25 connections in the scheduling method 1700, first a set of static cost tables will be prepared with the least cost paths from each link of the partial multistage network $V_{Comb}(N_1, N_2, d, s)$ to each outgoing hop wire from that partial multistage network as well as to each inlet link of the computational block connected form that partial multistage network. So there will be as many cost tables created equal to the sum of the total number
30 of outgoing hop wires from the partial multistage network and the inlet links of the computational block connected form that partial multistage network. Each cost table will

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

also have as many entries as there are internal links of that partial multistage network. And the value at each entry of these cost tables is equal to the total delay from the corresponding internal link to the corresponding outgoing hop wire or to the inlet link of the computational block.

5 In act 1760, according to the current invention, for the look-ahead cost computation during the A* search algorithm both the cost from the static cost tables from the current internal link in the current partial multistage network and the cost value computed based on the Manhattan distance between the target inlet link's block and the current link's corresponding block by taking the delays on each wire into consideration
10 are added. Also the least of the cost values from all the cost tables corresponding to the current link and all the outgoing wires in the right direction of the target block, is selected before it is added to the Manhattan distance based cost. Finally in act 1760, the multicast connection is scheduled as for the A* search algorithm. Then the control goes to act 1770.

 In act 1770, the demand cost and history cost of each link used by the current
15 multicast connection are updated. And the control goes to act 1720. Thus act 1720, act 1730, act 1740, act 1750, act 1760, and act 1770 are executed in a loop to schedule the multicast connections by going through the list of all multicast connections which will be one pass or iteration.

 In act 1730 results "yes", i.e. all the required multicast connections in the list are
20 scheduled in this pass or iteration, then the control goes to act 1780. In act 1780, the total number of links in the complete multistage network that are taken by more than one multicast connection are counted, hereinafter "OSN" or "Over Subscription nodes". Then the control goes to act 1790. In act 1790 it will be checked and if OSN is not equal to zero then the act 1790 results in "no" and the control goes to act 1710 to start the next iteration
25 or pass to schedule all the required multicast connections in the list of all multicast connections. Thus act 1710, act 1720, act 1730, act 1740, act 1750, act 1760, act 1770, act 1780, and act 1790 are executed in a loop to implement different passes or iterations of scheduling the set of all multicast connections. If the act 1790 results in "yes", that means no link in the complete multistage network is taken by more than one multicast
30 connection and hence the scheduling is successfully completed.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Each multicast connection of the type described above in reference to method 1700 of FIG. 17 can be unicast connection, a multicast connection or a broadcast connection, depending on the example.

5 **Inter-block and Intra-block Scheduling Method Embodiments the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$:**

FIG. 18 shows a high-level flowchart of a scheduling method 1800, in one embodiment executed to setup multicast connections in the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ disclosed in this invention in two steps (one for each act 1810 and act 1820 as shown in FIG. 18) namely: 1) scheduling the set of multicast connections
10 outside the blocks of 2D-grid of blocks with each block corresponding to a partial multi-stage network, or in between the blocks of the complete multi-stage network, or alternatively on the external wires of the complete multi-stage network hereinafter “inter-block scheduling”. Inter-block scheduling is implemented in act 1810 so that there are no
15 OSN nodes. During inter-block scheduling the partial multi-stage hierarchical network corresponding to each block is considered as a single stage network or alternatively each internal wire of the partial multi-stage hierarchical network is directly connected to each outgoing wire or external wire of the partial multi-stage hierarchical network, and 2)
20 scheduling the set of multicast connections inside the blocks of 2D-grid of blocks with each block corresponding to a partial multi-stage network or alternatively on the internal wires of the complete multi-stage network hereinafter “intra-block scheduling”. The act 1820 implements intra-block scheduling for each block so that there are no OSN nodes.

The act 1810 may be implemented by the scheduling method 1700 of FIG. 17. Similarly in act 1820 for each block of the multi-stage hierarchical network, the inter-
25 block scheduling may be implemented by the scheduling method 1700 of FIG. 17.

In accordance with the current invention, the scheduling method 1700 of FIG. 17 and the scheduling method 1800 of FIG. 18 are applicable to either partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100A of FIG. 1A, or partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100B of FIG. 1B, or partial multi-stage

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C, corresponding to a block of 2D-grid of blocks 800 of FIG. 8, using any one of the embodiments of 200A-200F of FIGS. 2A-2F, 900A-900E of FIGS. 9A-9E, 1000A-1000F of FIGS. 10A-10F, 1100A-1100C of FIGS. 11A-11C to implement a stage of a ring of the multi-stage hierarchical network, either by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, 300E of FIG. 3E, 500A of FIG. 5A, 1200 of FIG. 12, 1300 of FIG. 13, 1400 of FIG. 14, and 1500 of FIG. 15 or by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may be any one of the embodiments of either the diagrams 400A of FIG. 4A, 400B of FIG. 4B, 600A of FIG. 6A, or 600B of FIG. 6B is very efficient in the reduction of the die size, power consumption, and highly optimized for lower wire/path delay for higher performance for practical routing applications to particularly to set up broadcast, unicast and multicast connections.

Numerous modifications and adaptations of the embodiments, implementations, and examples described herein will be apparent to the skilled artisan in view of the disclosure.

20

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

REMARKS

Applicant respectfully submits that entry of the foregoing Amendment pursuant to Rule 312 (37 C.F.R. § 1.312) does not raise any new issues. Consequently, pursuant to Rule 312, it is requested that the foregoing Amendment be entered.

5

CONCLUSION

For all of the above reasons, applicant submits that the amendments to abstract, cross reference to related applications, summary of invention, and amendments to specification are now in proper form. Therefore applicant submits that this application is now in condition for allowance, which action he respectfully solicits.

10

Conditional request for Constructive Assistance

Applicant has amended the claims of this application so that they are proper, definite, and define novel structure which is also unobvious. If, for any reason this application is not believed to be in full condition for allowance, applicant respectfully request the constructive assistance and suggestions of the Examiner pursuant to M.P.E.P § 2173.02 and § 707.07(j) in order that the undersigned can place this application in allowable condition as soon as possible and without the need for further proceedings.

15

Very respectfully,

/Venkat Konda/

20 Venkat Konda

Konda Technologies, Inc. (USPTO Customer Number: 38139)

6278 Grand Oak Way

San Jose, CA 95135

Phone: 408-472-3273



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Table with columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO., EXAMINER, ART UNIT, PAPER NUMBER, NOTIFICATION DATE, DELIVERY MODE. Includes application details for Venkat Konda and examiner GIDADO, RASHEED.

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

venkat@kondatech.com
vkonda@gmail.com

Response to Rule 312 Communication	Application No. 16/562,450	Applicant(s) Konda, Venkat	
	Examiner RASHEED GIDADO	Art Unit 2464	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. The amendment filed on 28 December 2020 under 37 CFR 1.312 has been considered, and has been:
- a) entered.
 - b) entered as directed to matters of form not affecting the scope of the invention.
 - c) disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.
 - d) disapproved. See explanation below.
 - e) entered in part. See explanation below.

/RASHEED GIDADO/
Primary Examiner, Art Unit 2464

Electronic Acknowledgement Receipt

EFS ID:	41503518
Application Number:	16562450
International Application Number:	
Confirmation Number:	6438
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkat Konda
Filer Authorized By:	
Attorney Docket Number:	V-0060US
Receipt Date:	28-DEC-2020
Filing Date:	06-SEP-2019
Time Stamp:	19:05:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment after Notice of Allowance (Rule 312)	AmndAfterAllow-V0060-12-28-20.pdf	984782 6e69b972072fc19ecdbad4ac117a14cfb08de24	no	211

Warnings:

Information:	
Total Files Size (in bytes):	984782
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>	

Application Number: 16/562,450

Art Unit: 2464

AMENDMENT AFTER ALLOWANCE UNDER RULE 312

In The United States Patent And Trademark Office

Application Number: 16/562,450

Application Filed: 9/6/2019

Applicant(s): Venkat Konda

5 Title: Fast Scheduling and Optimization of Multi-stage Hierarchical Networks

Examiner/Art Unit: Rasheed Gidado / 2464

San Jose, 2020 December 28, Mon

AMENDMENT AFTER ALLOWANCE UNDER RULE 312

10 **(37 C.F.R. § 1.312)**

Mail Stop Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, Virginia, 22313-1450

15 Dear Sir/Madam:

This replies to the Notice of Allowance and Fee(s) Due from the United States Patent and Trademark Office mailed on November 18, 2020 in connection with the above-identified patent application. Pursuant to Rule 312, applicant respectfully requests that the above application be amended as follows:

20 For the sake of clarity in the amendment to the abstract of disclosure, amendment to Cross Reference to Related applications, amendment to Summary of Invention, and amendments to the specification submitted on November 9, 2020 in response to the office action August 7, 2020, Applicant is further submitting the following:

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

- 1) Unedited and substitute Abstract of Disclosure in page 2
- 2) Unedited and substitute Cross Reference to Related Applications in page 3
- 3) Unedited and substitute Summary of Invention in page 4
- 4) Complete Specification (Detailed Description of the Invention) with the all
5 amendments to specification begin on page 5 and continues to page 108
- 5) Unedited and complete substitute specification (Detailed Description of the
Invention) begin on page 108 and continues to page 210

I. UNEDITED AND SUSTITUTE ABSTRACT OF THE DISCLOSURE:

10 An unedited and substitute Abstract of the Disclosure appears below:

Significantly optimized multi-stage networks including scheduling methods for
faster scheduling of connections, useful in wide target applications, with VLSI layouts
using only horizontal wires and vertical wires to route large scale partial multi-stage
hierarchical networks having inlet and outlet links, and laid out in an integrated circuit
15 device in a two-dimensional grid arrangement of blocks are disclosed. The optimized
multi-stage networks in each block employ one or more slices of rings of stages of
switches with inlet and outlet links of partial multi-stage hierarchical networks connecting
to rings from either left-hand side or right-hand side; and employ hop wires or multi-drop
hop wires wherein hop wires or multi-drop wires are connected from switches of stages
20 of rings of slices of a first partial multi-stage hierarchical network to switches of stages of
rings of slices of the first or a second partial multi-stage hierarchical network.

Applicant submits that the above amended abstract is within 150 words.

25

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

II. UNEDITED AND SUBSTITUTE CROSS REFERENCE TO RELATED APPLICATIONS

An unedited and substitute Cross Reference to Related Applications appears below:

5 This application is Continuation Application and claims priority to US
Application Serial No. 15/884,911 entitled "FAST SCHEDULING AND
OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS" by Venkat
Konda assigned to the same assignee as the current application, filed January 31, 2018,
which is Continuation Application and claims priority to US Application Serial No.
10 15/331,855 entitled "FAST SCHEDULING AND OPTIMIZATION OF MULTI-STAGE
HIERARCHICAL NETWORKS" by Venkat Konda assigned to the same assignee as the
current application, filed October 22, 2016, issued as US Patent No. 9,929,977 on March
27, 2018, which is Continuation Application and claims priority to US Application Serial
No. 14/329,876 entitled "FAST SCHEDULING AND OPTIMIZATION OF MULTI-
15 STAGE HIERARCHICAL NETWORKS" by Venkat Konda assigned to the same
assignee as the current application, filed July 11, 2014, issued as US Patent No. 9,509,634
on November 29, 2016, which claims priority to U.S. Provisional Patent Application
Serial No. 61/846,083 entitled "FAST SCHEDULING AND OPTIMIZATION OF
MULTI-STAGE HIERARCHICAL NETWORKS" by Venkat Konda assigned to the
20 same assignee as the current application, filed July 15, 2013, and also Continuation-in-
Part Application and claims priority to US Application Serial No. US14/199,168 entitled
"OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS FOR
PRACTICAL ROUTING APPLICATIONS" by Venkat Konda assigned to the same
assignee as the current application, filed March 6, 2014, issued as US Patent No.
25 9,374,322 on June 21, 2016, which in turn is bypass continuation application and claims
priority to PCT Application Serial No. PCT/US12/53814 entitled "OPTIMIZATION OF
MULTI-STAGE HIERARCHICAL NETWORKS FOR PRACTICAL ROUTING
APPLICATIONS" by Venkat Konda assigned to the same assignee as the current
application, filed September 6, 2012, which is Continuation-in-Part application and
30 claims priority to U.S. Provisional Patent Application Serial No. 61/531,615 entitled
"OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS FOR

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

PRACTICAL ROUTING APPLICATIONS" by Venkat Konda assigned to the same assignee as the current application, filed September 7, 2011.

III. UNEDITED AND SUBSTITUTE SUMMARY OF INVENTION

5

An unedited and substitute Summary of Invention appears below:

Significantly optimized multi-stage networks for faster scheduling of connections, useful in wide target applications, with VLSI layouts (or floor plans) using only
10 horizontal wires and vertical wires to route large scale partial multi-stage hierarchical networks having inlet and outlet links, and laid out in an integrated circuit device in a two-dimensional grid arrangement of blocks, (for example in an FPGA where the partial multi-stage hierarchical networks to route Lookup Tables, or memory blocks, or DSP blocks) are disclosed. The optimized multi-stage networks in each block employ one or
15 more slices of rings of stages of switches with inlet and outlet links of partial multi-stage hierarchical networks connecting to rings from either left-hand side or right-hand side.

The optimized multi-stage networks employ hop wires or multi-drop hop wires wherein hop wires or multi-drop wires are connected from switches of stages of rings of slices of a first partial multi-stage hierarchical network to switches of stages of rings of
20 slices of a second partial multi-stage hierarchical network or switches of stages of rings of slices of the first partial multi-stage hierarchical network so that said hop wires or multi-drop hop wires are either vertical wires or horizontal wires.

The VLSI layouts exploit spatial locality so that partial multi-stage hierarchical networks that are spatially nearer are connected with shorter hop wires compared to the
25 hop wires between spatially farther partial multi-stage hierarchical networks. The optimized multi-stage networks provide high routability for broadcast, unicast and multicast connections, yet with the benefits of significantly lower cross points hence smaller area, lower signal latency, lower power and with significant fast compilation or

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

routing time. Various scheduling methods are also disclosed to schedule a set of multicast connections in the multi-stage hierarchical network.

The optimized multi-stage networks $V_{Comb}(N_1, N_2, d, s)$ & $V_{D-Comb}(N_1, N_2, d, s)$ according to the current invention inherit the properties of one or more generalized multi-stage and pyramid networks $V(N_1, N_2, d, s)$ & $V_P(N_1, N_2, d, s)$, generalized folded multi-stage and pyramid networks $V_{fold}(N_1, N_2, d, s)$ & $V_{fold-p}(N_1, N_2, d, s)$, generalized butterfly fat tree and butterfly fat pyramid networks $V_{bft}(N_1, N_2, d, s)$ & $V_{bfp}(N_1, N_2, d, s)$, generalized multi-link multi-stage and pyramid networks $V_{mlink}(N_1, N_2, d, s)$ & $V_{mlink-p}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage and pyramid networks $V_{fold-mlink}(N_1, N_2, d, s)$ & $V_{fold-mlink-p}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree and butterfly fat pyramid networks $V_{mlink-bft}(N_1, N_2, d, s)$ & $V_{mlink-bfp}(N_1, N_2, d, s)$, generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$, and generalized cube connected cycles networks $V_{CCC}(N_1, N_2, d, s)$ for $s = 1, 2, 3$ or any number in general.

15

IV. COMPLETE SPECIFICATION WITH ALL THE AMENDMENTS TO THE SPECIFICATION

Complete Specification with the all amendments to specification appears below:

Fully connected multi-stage hierarchical networks are an over kill in every dimension such as area, power, and performance for certain practical routing applications and need to be optimized to significantly improve savings in area, power and performance of the routing network. The present invention discloses several embodiments of the optimized multi-stage hierarchical networks for practical routing applications along with their VLSI layout (floor plan) feasibility and simplicity.

The multi-stage hierarchical networks considered for optimization in the current invention include: generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$, and generalized cube connected cycles networks $V_{ccc}(N_1, N_2, d, s)$ for $s = 1, 2, 3$ or any number in general. Alternatively the optimized multi-stage hierarchical networks disclosed in this invention inherit the properties of one or more of these networks, in addition to additional properties that may not be exhibited these networks.

10 The optimized multi-stage hierarchical networks disclosed are applicable for practical routing applications, with several goals such as: 1) all the signals in the design starting from an inlet link of the network to an outlet link of the network need to be setup without blocking. These signals may consist of broadcast, unicast and multicast connections; Each routing resource may need to be used by only one signal or
15 connection; 2) physical area consumed by the routing network to setup all the signals needs to be small; 3) power consumption of the network needs to be small, after the signals are setup. Power may be both static power and dynamic power; 4) Delay of the signal or a connection needs to be small after it is setup through a path using several routing resources in the path. The smaller the delay of the connections will lead to faster
20 performance of the design. Typically delay of the critical connections determines the performance of the design on a given network; 5) Designs need to be not only routed through the network (i.e., all the signals need to be setup from inlet links of the network to the outlet links of the network.), but also the routing needs to be in faster time using efficient routing algorithms; 6) Efficient VLSI layout of the network is also critical and
25 can greatly influence all the other parameters including the area taken up by the network on the chip, total number of wires, length of the wires, delay through the signal paths and hence the maximum clock speed of operation.

 The different varieties of multi-stage networks described in various embodiments in the current invention have not been implemented previously on the semiconductor
30 chips. The practical application of these networks includes Field Programmable Gate

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Array (FPGA) chips. Current commercial FPGA products such as Xilinx's Vertex, Altera's Stratix, Lattice's ECPx implement island-style architecture using mesh and segmented mesh routing interconnects using either full crossbars or sparse crossbars. These routing interconnects consume large silicon area for crosspoints, long wires, large
5 signal propagation delay and hence consume lot of power.

The current invention discloses the optimization and scheduling methods of multi-stage hierarchical networks with fast scheduling of connections, for practical routing applications of numerous types of multi-stage networks also using multi-drop links. The optimizations disclosed in the current invention are applicable to including the numerous
10 generalized multi-stage networks disclosed in the following patent applications:

1) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-stage networks $V(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,270,400 that is incorporated by reference above.

15 2) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,170,040 that is incorporated by reference above.

20 3) Rearrangeably nonblocking for arbitrary fan-out multicast and unicast, and strictly nonblocking for unicast for generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$ and generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,363,649 that is incorporated by reference above.

25 4) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,170,040 that is incorporated by reference above.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

5) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,363,649 that is incorporated by reference above.

5 6) Strictly nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$ and generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,363,649 that is incorporated by reference above.

10 7) VLSI layouts of numerous types of multi-stage networks are described in the US Patent No. 8,269,523 entitled "VLSI LAYOUTS OF FULLY CONNECTED NETWORKS" that is incorporated by reference above.

 8) VLSI layouts of numerous types of multi-stage networks are described in the US Patent No. 8,898,611 entitled "VLSI LAYOUTS OF FULLY CONNECTED
15 GENERALIZED AND PYRAMID NETWORKS WITH LOCALITY EXPLOITATION" that is incorporated by reference above.

In addition the optimization with the VLSI layouts disclosed in the current invention are also applicable to generalized multi-stage pyramid networks $V_p(N_1, N_2, d, s)$, generalized folded multi-stage pyramid networks $V_{fold-p}(N_1, N_2, d, s)$,
20 generalized butterfly fat pyramid networks $V_{bfp}(N_1, N_2, d, s)$, generalized multi-link multi-stage pyramid networks $V_{mlink-p}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage pyramid networks $V_{fold-mlink-p}(N_1, N_2, d, s)$, generalized multi-link butterfly fat pyramid networks $V_{mlink-bfp}(N_1, N_2, d, s)$, generalized hypercube networks $V_{cube}(N_1, N_2, d, s)$ and generalized cube connected cycles networks $V_{CCC}(N_1, N_2, d, s)$
25 for $s = 1, 2, 3$ or any number in general.

Finally the current invention discloses the optimizations and VLSI layouts of multi-stage hierarchical networks $V_{Comb}(N_1, N_2, d, s)$ and the optimizations and VLSI

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

layouts of multi-stage hierarchical networks $V_{D-Comb}(N_1, N_2, d, s)$ for practical routing applications (particularly to set up broadcast, unicast and multicast connections), where “Comb” denotes the combination of and “D-Comb” denotes the delay optimized combination of any of the generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized

5 folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, generalized multi-stage pyramid networks $V_p(N_1, N_2, d, s)$, generalized folded multi-stage pyramid networks

10 $V_{fold-p}(N_1, N_2, d, s)$, generalized butterfly fat pyramid networks $V_{bfp}(N_1, N_2, d, s)$, generalized multi-link multi-stage pyramid networks $V_{mlink-p}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage pyramid networks $V_{fold-mlink-p}(N_1, N_2, d, s)$, generalized multi-link butterfly fat pyramid networks $V_{mlink-bfp}(N_1, N_2, d, s)$, generalized hypercube networks $V_{cube}(N_1, N_2, d, s)$, and generalized cube connected cycles networks

15 $V_{ccc}(N_1, N_2, d, s)$ for $s = 1, 2, 3$ or any number in general.

Multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$:

Referring to diagram 100A in FIG. 1A, in one embodiment, an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ where $N_1 = 200$; $N_2 = 400$; $d = 2$; and $s = 1$ corresponding to one computational block, with each computational block

20 having 4 inlet links namely I1, I2, I3, and I4; and 2 outlet links namely O1 and O2. And for each computational block the corresponding partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists of two rings 110 and 120, where ring 110 consists of “m+1” stages namely (ring 1, stage 0), (ring 1, stage 1), ... (ring 1, stage “m-1”), and (ring 1, stage “m”), and ring 120 consists of “n+1” stages namely (ring 2, stage 0), (ring

25 2, stage 1), ... (ring 2, stage “n-1”), and (ring 2, stage “n”), where “m” and “n” are positive integers.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Ring 110 has inlet links Ri(1,1) and Ri(1,2), and has outlet links Bo(1,1) and Bo(1,2). Ring 120 has inlet links Fi(2,1) and Fi(2,2), and outlet links Bo(2,1) and Bo(2,2). And hence the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists of 4 inlet links and 4 outlet links corresponding to the two rings 110 and 120. Outlet link O1 of the computational block is connected to inlet link Ri(1,1) of ring 110 and also inlet link of Fi(2,1) of ring 120. Similarly outlet link O2 of the computational block is connected to inlet link Ri(1,2) of Ring 110 and also inlet link of Fi(2,2) of Ring 120. And outlet link Bo(1,1) of Ring 110 is connected to inlet link I1 of the computational block. Outlet link Bo(1,2) of Ring 110 is connected to inlet link I2 of the computational block. Similarly outlet link Bo(2,1) of Ring 120 is connected to inlet link I3 of the computational block. Outlet link Bo(2,2) of Ring 120 is connected to inlet link I4 of the computational block. Since in this embodiment outlet link O1 of the computational block is connected to both inlet link Ri(1,1) of ring 110 and inlet link Fi(2,1) of ring 120; and outlet link O2 of the computational block is connected to both inlet link Ri(1,2) of ring 110 and inlet link Fi(2,2) of ring 120, the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists of 2 inlet links and 4 outlet links.

The two dimensional grid 800 in FIG. 8 illustrates an exemplary arrangement of 100 blocks arranged in 10 rows and 10 columns, in an embodiment. Each row of 2D-grid consisting of 10 block numbers namely the first row consists of the blocks (1,1), (1,2), (1,3), ... , (1,9), and (1,10). The second row consists of the blocks (2,1), (2,2), (2,3), ... , (2,9), and (2,10). Similarly 2D-grid 800 consists of 10 rows of each with 10 blocks and finally the tenth row consists of the blocks (10,1), (10,2), (10,3), ... , (10,9), and (10,10). Each block of 2D-grid 800, in one embodiment, is part of the die area of a semiconductor integrated circuit (hereinafter alternatively referred to as "integrated circuit device" or "IC device"), so that the complete 2D-grid 800 of 100 blocks represents the complete die of the semiconductor integrated circuit. In one embodiment, each block of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A with 2 inlet links and 4 outlet links and the corresponding computational block with 4 inlet links and 2 outlet links. For example block (1,1) of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A with 2 inlet links and 4 outlet links and the corresponding computational block with 4 inlet links and 2 outlet

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

links. Similarly each of the 100 blocks of 2D-grid 800 has a separate partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A with 2 inlet links and 4 outlet links and the corresponding computational block with 4 inlet links and 2 outlet links. Hence the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to 2D-grid 800 has $N_1 = 200$ inlet links and $N_2 = 400$ outlet links. And there are 100 computational blocks each one corresponding to one of the blocks with each computational block having 4 inlet links and 2 outlet links. Also the 2D-grid 800 is organized in the fourth quadrant of the 2D-Plane. In other embodiments the 2D-grid 800 may be organized as either first quadrant, or second quadrant or third quadrant of the 2D-Plane.

10 Referring to partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A in FIG. 1A, the stage (ring 1, stage 0) consists of 4 inputs namely $Ri(1,1)$, $Ri(1,2)$, $Ui(1,1)$, and $Ui(1,2)$; and 4 outputs $Bo(1,1)$, $Bo(1,2)$, $Fo(1,1)$, and $Fo(1,2)$. The stage (ring 1, stage 0) also consists of eight 2:1 multiplexers (A multiplexer is hereinafter called a “mux”) namely $R(1,1)$, $R(1,2)$, $F(1,1)$, $F(1,2)$, $U(1,1)$, $U(1,2)$, $B(1,1)$, and $B(1,2)$. The 2:1 Mux $R(1,1)$ has two inputs namely $Ri(1,1)$ and $Bo(1,1)$ and has one output $Ro(1,1)$. The 2:1 Mux $R(1,2)$ has two inputs namely $Ri(1,2)$ and $Bo(1,2)$ and has one output $Ro(1,2)$. The 2:1 Mux $F(1,1)$ has two inputs namely $Ro(1,1)$ and $Ro(1,2)$ and has one output $Fo(1,1)$. The 2:1 Mux $F(1,2)$ has two inputs namely $Ro(1,1)$ and $Ro(1,2)$ and has one output $Fo(1,2)$.

20 The 2:1 Mux $U(1,1)$ has two inputs namely $Ui(1,1)$ and $Fo(1,1)$ and has one output $Uo(1,1)$. The 2:1 Mux $U(1,2)$ has two inputs namely $Ui(1,2)$ and $Fo(1,2)$ and has one output $Uo(1,2)$. The 2:1 Mux $B(1,1)$ has two inputs namely $Uo(1,1)$ and $Uo(1,2)$ and has one output $Bo(1,1)$. The 2:1 Mux $B(1,2)$ has two inputs namely $Uo(1,1)$ and $Uo(1,2)$ and has one output $Bo(1,2)$.

25 The stage (ring 1, stage 1) consists of 4 inputs namely $Ri(1,3)$, $Ri(1,4)$, $Ui(1,3)$, and $Ui(1,4)$; and 4 outputs $Bo(1,3)$, $Bo(1,4)$, $Fo(1,3)$, and $Fo(1,4)$. The stage (ring 1, stage 1) also consists of eight 2:1 Muxes namely $R(1,3)$, $R(1,4)$, $F(1,3)$, $F(1,4)$, $U(1,3)$, $U(1,4)$, $B(1,3)$, and $B(1,4)$. The 2:1 Mux $R(1,3)$ has two inputs namely $Ri(1,3)$ and $Bo(1,3)$ and has one output $Ro(1,3)$. The 2:1 Mux $R(1,4)$ has two inputs namely $Ri(1,4)$ and $Bo(1,4)$ and has one output $Ro(1,4)$. The 2:1 Mux $F(1,3)$ has two inputs namely $Ro(1,3)$ and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Ro(1,4) and has one output Fo(1,3). The 2:1 Mux F(1,4) has two inputs namely Ro(1,3) and Ro(1,4) and has one output Fo(1,4).

The 2:1 Mux U(1,3) has two inputs namely Ui(1,3) and Fo(1,3) and has one output Uo(1,3). The 2:1 Mux U(1,4) has two inputs namely Ui(1,4) and Fo(1,4) and has one output Uo(1,4). The 2:1 Mux B(1,3) has two inputs namely Uo(1,3) and Uo(1,4) and has one output Bo(1,3). The 2:1 Mux B(1,4) has two inputs namely Uo(1,3) and Uo(1,4) and has one output Bo(1,4).

The output Fo(1,1) of the stage (ring 1, stage 0) is connected to the input Ri(1,3) of the stage (ring 1, stage 1) which is called hereinafter an internal connection (hereinafter alternatively referred to as “straight link” or “straight middle link”) between two successive stages of a ring. And the output Bo(1,3) of the stage (ring 1, stage 1) is connected to the input Ui(1,1) of the stage (ring 1, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1.

The stage (ring 1, stage “m-1”) consists of 4 inputs namely Fi(1,2m-1), Fi(1,2m), Ui(1,2m-1), and Ui(1,2m); and 4 outputs Bo(1,2m-1), Bo(1,2m), Fo(1,2m-1), and Fo(1,2m). The stage (ring 1, stage “m-1”) also consists of six 2:1 Muxes namely F(1,2m-1), F(1,2m), U(1,2m-1), U(1,2m), B(1,2m-1), and B(1,2m). The 2:1 Mux F(1,2m-1) has two inputs namely Fi(1,2m-1) and Fi(1,2m) and has one output Fo(1,2m-1). The 2:1 Mux F(1,2m) has two inputs namely Fi(1,2m-1) and Fi(1,2m) and has one output Fo(1,2m).

The 2:1 Mux U(1,2m-1) has two inputs namely Ui(1,2m-1) and Fo(1,2m-1) and has one output Uo(1,2m-1). The 2:1 Mux U(1,2m) has two inputs namely Ui(1,2m) and Fo(1,2m) and has one output Uo(1,2m). The 2:1 Mux B(1,2m-1) has two inputs namely Uo(1,2m-1) and Uo(1,2m) and has one output Bo(1,2m-1). The 2:1 Mux B(1,2m) has two inputs namely Uo(1,2m-1) and Uo(1,2m) and has one output Bo(1,2m).

The stage (ring 1, stage “m”) consists of 4 inputs namely Fi(1,2m+1), Fi(1,2m+2), Ui(1,2m+1), and Ui(1,2m+2); and 4 outputs Bo(1,2m+1), Bo(1,2m+2), Fo(1,2m+1), and Fo(1,2m+2). The stage (ring 1, stage “m”) also consists of six 2:1 Muxes namely F(1,2m+1), F(1,2m+2), U(1,2m+1), U(1,2m+2), B(1,2m+1), and B(1,2m+2). The 2:1 Mux F(1,2m+1) has two inputs namely Fi(1,2m+1) and Fi(1,2m+2) and has one output

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Fo(1,2m+1). The 2:1 Mux F(1,2m+2) has two inputs namely Fi(1,2m+1) and Fi(1,2m+2) and has one output Fo(1,2m+2).

The 2:1 Mux U(1,2m+1) has two inputs namely Ui(1,2m+1) and Fo(1,2m+1) and has one output Uo(1,2m+1). The 2:1 Mux U(1,2m+2) has two inputs namely Ui(1,2m+2) and Fo(1,2m+2) and has one output Uo(1,2m+2). The 2:1 Mux B(1,2m+1) has two inputs namely Uo(1,2m+1) and Uo(1,2m+2) and has one output Bo(1,2m+1). The 2:1 Mux B(1,2m+2) has two inputs namely Uo(1,2m+1) and Uo(1,2m+2) and has one output Bo(1,2m+2).

The output Fo(1,2m-1) of the stage (ring 1, stage "m-1") is connected to the input Fi(1,2m+1) of the stage (ring 1, stage "m"), is an internal connection between stage "m-1" and stage "m" of the ring 1. And the output Bo(1,2m+1) of the stage (ring 1, stage "m") is connected to the input Ui(1,2m-1) of the stage (ring 1, stage "m-1"), is another internal connection between stage "m-1" and stage "m" of the ring 1

Just the same way the stages (ring 1, stage 0), (ring 1, stage 1), there are also stages (ring 1, stage 2), (ring 1, stage 3), ... (ring 1, stage "m-1"), (ring 1, stage "m") in that order, where the stages from (ring 1, stage 2), (ring 1, stage 3), ... , (ring 1, stage "m-2") are not shown in the diagram 100A. Just the same way the two successive stages (ring 1, stage 0) and (ring 1, stage 1) have internal connections between them as described before, any two successive stages have similar internal connections. For example (ring 1, stage 1) and (ring 1, stage 2) have similar internal connections and (ring 1, stage "m-2") and (ring 1, stage "m-1") have similar internal connections.

Stage (ring 1, stage 0) is also called hereinafter the "entry stage" or "first stage" of ring 1, since inlet links and outlet links of the computational block are directly connected to stage (ring 1, stage 0). Also stage (ring 1, stage "m") is hereinafter the "last stage" or "root stage" of ring 1.

The stage (ring 2, stage 0) consists of 4 inputs namely Fi(2,1), Fi(2,2), Ui(2,1), and Ui(2,2); and 4 outputs Bo(2,1), Bo(2,2), Fo(2,1), and Fo(2,2). The stage (ring 2, stage 0) also consists of six 2:1 Muxes namely F(2,1), F(2,2), U(2,1), U(2,2), B(2,1), and B(2,2). The 2:1 Mux F(2,1) has two inputs namely Fi(2,1) and Fi(2,2) and has one output

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Fo(2,1). The 2:1 Mux F(2,2) has two inputs namely Fi(2,1) and Fi(2,2) and has one output Fo(2,2).

The 2:1 Mux U(2,1) has two inputs namely Ui(2,1) and Fo(2,1) and has one output Uo(2,1). The 2:1 Mux U(2,2) has two inputs namely Ui(2,2) and Fo(2,2) and has one output Uo(2,2). The 2:1 Mux B(2,1) has two inputs namely Uo(2,1) and Uo(2,2) and has one output Bo(2,1). The 2:1 Mux B(2,2) has two inputs namely Uo(2,1) and Uo(2,2) and has one output Bo(2,2).

The stage (ring 2, stage 1) consists of 4 inputs namely Fi(2,3), Fi(2,4), Ui(2,3), and Ui(2,4); and 4 outputs Bo(2,3), Bo(2,4), Fo(2,3), and Fo(2,4). The stage (ring 2, stage 1) also consists of six 2:1 Muxes namely F(2,3), F(2,4), U(2,3), U(2,4), B(2,3), and B(2,4). The 2:1 Mux F(2,3) has two inputs namely Fi(2,3) and Fi(2,4) and has one output Fo(2,3). The 2:1 Mux F(2,4) has two inputs namely Fi(2,3) and Fi(2,4) and has one output Fo(2,4).

The 2:1 Mux U(2,3) has two inputs namely Ui(2,3) and Fo(2,3) and has one output Uo(2,3). The 2:1 Mux U(2,4) has two inputs namely Ui(2,4) and Fo(2,4) and has one output Uo(2,4). The 2:1 Mux B(2,3) has two inputs namely Uo(2,3) and Uo(2,4) and has one output Bo(2,3). The 2:1 Mux B(2,4) has two inputs namely Uo(2,3) and Uo(2,4) and has one output Bo(2,4).

The output Fo(2,1) of the stage (ring 2, stage 0) is connected to the input Fi(2,3) of the stage (ring 2, stage 1), is an internal connection between stage 0 and stage 1 of the ring 2. And the output Bo(2,3) of the stage (ring 2, stage 1) is connected to the input Ui(2,1) of the stage (ring 2, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1..

The stage (ring 2, stage "n-1") consists of 4 inputs namely Ri(2,2n-1), Ri(2,2n), Ui(1,2n-1), and Ui(1,2n); and 4 outputs Bo(1,2n-1), Bo(1,2n), Fo(1,2n-1), and Fo(1,2n). The stage (ring 2, stage "n-1") also consists of eight 2:1 Muxes namely R(2,2n-1), R(2,2n), F(2,2n-1), F(1,2n), U(1,2n-1), U(1,2n), B(1,2n-1), and B(1,2n). The 2:1 Mux R(2,2n-1) has two inputs namely Ri(2,2n-1) and Bo(2,2n-1) and has one output Ro(2,2n-1). The 2:1 Mux R(2,2n) has two inputs namely Ri(2,2n) and Bo(2,2n) and has one output Ro(2,2n). The 2:1 Mux F(2,2n-1) has two inputs namely Ro(2,2n-1) and Ro(2,2n) and has

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

one output $Fo(2,2n-1)$. The 2:1 Mux $F(2,2n)$ has two inputs namely $Ro(2,2n-1)$ and $Ro(2,2n)$ and has one output $Fo(2,2n)$.

The 2:1 Mux $U(2,2n-1)$ has two inputs namely $Ui(2,2n-1)$ and $Fo(2,2n-1)$ and has one output $Uo(2,2n-1)$. The 2:1 Mux $U(2,2n)$ has two inputs namely $Ui(2,2n)$ and $Fo(2,2n)$ and has one output $Uo(2,2n)$. The 2:1 Mux $B(2,2n-1)$ has two inputs namely $Uo(2,2n-1)$ and $Uo(2,2n)$ and has one output $Bo(2,2n-1)$. The 2:1 Mux $B(2,2n)$ has two inputs namely $Uo(2,2n-1)$ and $Uo(2,2n)$ and has one output $Bo(2,2n)$.

The stage (ring 2, stage "n") consists of 4 inputs namely $Ri(2,2n+1)$, $Ri(2,2n+2)$, $Ui(2,2n+1)$, and $Ui(2,2n+2)$; and 4 outputs $Bo(2,2n+1)$, $Bo(2,2n+2)$, $Fo(2,2n+1)$, and $Fo(2,2n+2)$. The stage (ring 2, stage "n") also consists of eight 2:1 Muxes namely $R(2,2n+1)$, $R(2,2n+2)$, $F(2,2n+1)$, $F(2,2n+2)$, $U(2,2n+1)$, $U(2,2n+2)$, $B(2,2n+1)$, and $B(2,2n+2)$. The 2:1 Mux $R(2,2n+1)$ has two inputs namely $Ri(2,2n+1)$ and $Bo(2,2n+1)$ and has one output $Ro(2,2n+1)$. The 2:1 Mux $R(2,2n+2)$ has two inputs namely $Ri(2,2n+2)$ and $Bo(2,2n+2)$ and has one output $Ro(2,2n+2)$. The 2:1 Mux $F(2,2n+1)$ has two inputs namely $Ro(2,2n+1)$ and $Ro(2,2n+2)$ and has one output $Fo(2,2n+1)$. The 2:1 Mux $F(2,2n+2)$ has two inputs namely $Ro(2,2n+1)$ and $Ro(2,2n+2)$ and has one output $Fo(2,2n+2)$.

The 2:1 Mux $U(2,2n+1)$ has two inputs namely $Ui(2,2n+1)$ and $Fo(2,2n+1)$ and has one output $Uo(2,2n+1)$. The 2:1 Mux $U(2,2n+2)$ has two inputs namely $Ui(2,2n+2)$ and $Fo(2,2n+2)$ and has one output $Uo(2,2n+2)$. The 2:1 Mux $B(2,2n+1)$ has two inputs namely $Uo(2,2n+1)$ and $Uo(2,2n+2)$ and has one output $Bo(2,2n+1)$. The 2:1 Mux $B(2,2n+2)$ has two inputs namely $Uo(2,2n+1)$ and $Uo(2,2n+2)$ and has one output $Bo(2,2n+2)$.

The output $Fo(2,2n-1)$ of the stage (ring 2, stage "n-1") is connected to the input $Ri(2,2n+1)$ of the stage (ring 2, stage "n"), is an internal connection between stage "n-1" and stage "n" of the ring 1. And the output $Bo(2,2n+1)$ of the stage (ring 2, stage "n") is connected to the input $Ui(2,2n-1)$ of the stage (ring 2, stage "n-1"), is another internal connection between stage "n-1" and stage "n" of the ring 1.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Each stage of any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists of 4 inputs and $2 * d = 4$ outputs. Even though the stages (ring 1, stage 0), (ring 1, stage 1), (ring 2, stage “n-1”), and (ring 2, stage “n”) each have eight 2:1 muxes, and the stages (ring 2, stage 0), (ring 2, stage 1), (ring 1, stage “m-1”), and (ring 1, stage “m”) each have six 2:1 muxes, in other embodiments any of these stages can be one of the four by four switch diagrams namely 200A of FIG. 2A, 200B of FIG. 2B, 200C of FIG. 2C, and one of the eight by four switch diagrams namely 200E of FIG. 2E, 200F of FIG. 2F.

Referring to diagram 100B in FIG. 1B, in one embodiment, an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ where $N_1 = 400$; $N_2 = 800$; $d = 2$; and $s = 1$ corresponding to one computational block, with each computational block having 8 inlet links namely I1, I2, I3, I4, I5, I6, I7, and I8; and 4 outlet links namely O1, O2, O3, and O4. And for each computational block the corresponding partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of two rings 110 and 120, where ring 110 consists of “m+1” stages namely (ring 1, stage 0), (ring 1, stage 1), ... (ring 1, stage “m-1”), and (ring 1, stage “m”), and ring 120 consists of “n+1” stages namely (ring 2, stage 0), (ring 2, stage 1), ... (ring 2, stage “n-1”), and (ring 2, stage “n”), where “m” and “n” are positive integers.

Ring 110 has inlet links $Ri(1,1)$ and $Ri(1,2)$ from the left-hand side, and has outlet links $Bo(1,1)$ and $Bo(1,2)$ from left-hand side. Ring 110 also has inlet links $Ui(1,2m+1)$ and $Ui(1,2m+2)$ from the right-hand side, and has outlet links $Fo(1,2m+1)$ and $Fo(1,2m+2)$ from right-hand side. Ring 120 has inlet links $Fi(2,1)$ and $Fi(2,2)$ from left-hand side, and outlet links $Bo(2,1)$ and $Bo(2,2)$ from left-hand side. Ring 120 also has inlet links $Ui(2,2n+1)$ and $Ui(2,2n+2)$ from the right-hand side, and has outlet links $Fo(2,2n+1)$ and $Fo(2,2n+2)$ from right-hand side.

And the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of 8 inlet links and 4 outlet links corresponding to the two rings 110 and 120. From left-hand side, outlet link O1 of the computational block is connected to inlet link $Ri(1,1)$ of ring 110 and also inlet link of $Fi(2,1)$ of ring 120. Similarly from left-hand side, outlet link O2 of the computational block is connected to inlet link $Ri(1,2)$ of Ring 110 and also

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

inlet link of $F_i(2,2)$ of Ring 120. And from left-hand side, outlet link $B_o(1,1)$ of Ring 110 is connected to inlet link I1 of the computational block. From left-hand side, Outlet link $B_o(1,2)$ of Ring 110 is connected to inlet link I2 of the computational block. Similarly from left-hand side, outlet link $B_o(2,1)$ of Ring 120 is connected to inlet link I3 of the computational block. From left-hand side, outlet link $B_o(2,2)$ of Ring 120 is connected to inlet link I4 of the computational block.

From right-hand side, outlet link O3 of the computational block is connected to inlet link $U_i(1,2m+1)$ of ring 110 and also inlet link of $U_i(2,2n+1)$ of ring 120. Similarly from right-hand side, outlet link O4 of the computational block is connected to inlet link $U_i(1,2m+2)$ of Ring 110 and also inlet link of $U_i(2,2n+2)$ of Ring 120. And from right-hand side, outlet link $F_o(1,2m+1)$ of Ring 110 is connected to inlet link I5 of the computational block. From right-hand side, outlet link $F_o(1,2m+2)$ of Ring 110 is connected to inlet link I6 of the computational block. Similarly from right-hand side, outlet link $F_o(2,2n+1)$ of Ring 120 is connected to inlet link I7 of the computational block. From right-hand side, outlet link $F_o(2,2n+2)$ of Ring 120 is connected to inlet link I8 of the computational block.

Since in this embodiment outlet link O1 of the computational block is connected to both inlet link $R_i(1,1)$ of ring 110 and inlet link $F_i(2,1)$ of ring 120; outlet link O2 of the computational block is connected to both inlet link $R_i(1,2)$ of ring 110 and inlet link $F_i(2,2)$ of ring 120; outlet link O3 of the computational block is connected to both inlet link $U_i(1,2m+1)$ of ring 110 and inlet link $U_i(2,2n+1)$ of ring 120; and outlet link O4 of the computational block is connected to both inlet link $U_i(1,2m+2)$ of ring 110 and inlet link $U_i(2,2n+2)$ of ring 120, the partial multi-stage hierarchical network

$V_{Comb}(N_1, N_2, d, s)$ 100B consists of 4 inlet links and 8 outlet links.

Referring to two dimensional grid 800 in FIG. 8 illustrates, in another embodiment, each block of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B with 4 inlet links and 8 outlet links and the corresponding computational block with 8 inlet links and 4 outlet links. For example block (1,1) of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B with 4 inlet links and 8 outlet links and the corresponding

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

computational block with 8 inlet links and 4 outlet links. Similarly each of the 100 blocks of 2D-grid 800 has a separate partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B with 4 inlet links and 8 outlet links and the corresponding computational block with 8 inlet links and 4 outlet links. Hence the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to 2D-grid 800 has $N_1 = 400$ inlet links and $N_2 = 800$ outlet links. Since there are 100 computational blocks each one corresponding to one of the blocks with each computational block having 8 inlet links and 4 outlet links. Also the 2D-grid 800 is organized in the fourth quadrant of the 2D-Plane. In other embodiments the 2D-grid 800 may be organized as either first quadrant, or second quadrant or third quadrant of the 2D-Plane.

Referring to partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B in FIG. 1B, the stage (ring 1, stage 0) consists of 4 inputs namely $Ri(1,1)$, $Ri(1,2)$, $Ui(1,1)$, and $Ui(1,2)$; and 4 outputs $Bo(1,1)$, $Bo(1,2)$, $Fo(1,1)$, and $Fo(1,2)$. The stage (ring 1, stage 0) also consists of eight 2:1 multiplexers (A multiplexer is hereinafter called a "mux") namely $R(1,1)$, $R(1,2)$, $F(1,1)$, $F(1,2)$, $U(1,1)$, $U(1,2)$, $B(1,1)$, and $B(1,2)$. The 2:1 Mux $R(1,1)$ has two inputs namely $Ri(1,1)$ and $Bo(1,1)$ and has one output $Ro(1,1)$. The 2:1 Mux $R(1,2)$ has two inputs namely $Ri(1,2)$ and $Bo(1,2)$ and has one output $Ro(1,2)$. The 2:1 Mux $F(1,1)$ has two inputs namely $Ro(1,1)$ and $Ro(1,2)$ and has one output $Fo(1,1)$. The 2:1 Mux $F(1,2)$ has two inputs namely $Ro(1,1)$ and $Ro(1,2)$ and has one output $Fo(1,2)$.

The 2:1 Mux $U(1,1)$ has two inputs namely $Ui(1,1)$ and $Fo(1,1)$ and has one output $Uo(1,1)$. The 2:1 Mux $U(1,2)$ has two inputs namely $Ui(1,2)$ and $Fo(1,2)$ and has one output $Uo(1,2)$. The 2:1 Mux $B(1,1)$ has two inputs namely $Uo(1,1)$ and $Uo(1,2)$ and has one output $Bo(1,1)$. The 2:1 Mux $B(1,2)$ has two inputs namely $Uo(1,1)$ and $Uo(1,2)$ and has one output $Bo(1,2)$.

The stage (ring 1, stage 1) consists of 4 inputs namely $Ri(1,3)$, $Ri(1,4)$, $Ui(1,3)$, and $Ui(1,4)$; and 4 outputs $Bo(1,3)$, $Bo(1,4)$, $Fo(1,3)$, and $Fo(1,4)$. The stage (ring 1, stage 1) also consists of eight 2:1 Muxes namely $R(1,3)$, $R(1,4)$, $F(1,3)$, $F(1,4)$, $U(1,3)$, $U(1,4)$, $B(1,3)$, and $B(1,4)$. The 2:1 Mux $R(1,3)$ has two inputs namely $Ri(1,3)$ and $Bo(1,3)$ and has one output $Ro(1,3)$. The 2:1 Mux $R(1,4)$ has two inputs namely $Ri(1,4)$ and $Bo(1,4)$

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

and has one output $Ro(1,4)$. The 2:1 Mux $F(1,3)$ has two inputs namely $Ro(1,3)$ and $Ro(1,4)$ and has one output $Fo(1,3)$. The 2:1 Mux $F(1,4)$ has two inputs namely $Ro(1,3)$ and $Ro(1,4)$ and has one output $Fo(1,4)$.

The 2:1 Mux $U(1,3)$ has two inputs namely $Ui(1,3)$ and $Fo(1,3)$ and has one
 5 output $Uo(1,3)$. The 2:1 Mux $U(1,4)$ has two inputs namely $Ui(1,4)$ and $Fo(1,4)$ and has one output $Uo(1,4)$. The 2:1 Mux $B(1,3)$ has two inputs namely $Uo(1,3)$ and $Uo(1,4)$ and has one output $Bo(1,3)$. The 2:1 Mux $B(1,4)$ has two inputs namely $Uo(1,3)$ and $Uo(1,4)$ and has one output $Bo(1,4)$.

The output $Fo(1,1)$ of the stage (ring 1, stage 0) is connected to the input $Ri(1,3)$
 10 of the stage (ring 1, stage 1) which is called hereinafter an internal connection between two successive stages of a ring. And the output $Bo(1,3)$ of the stage (ring 1, stage 1) is connected to the input $Ui(1,1)$ of the stage (ring 1, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1.

The stage (ring 1, stage "m-1") consists of 4 inputs namely $Fi(1,2m-1)$, $Fi(1,2m)$,
 15 $Ui(1,2m-1)$, and $Ui(1,2m)$; and 4 outputs $Bo(1,2m-1)$, $Bo(1,2m)$, $Fo(1,2m-1)$, and $Fo(1,2m)$. The stage (ring 1, stage "m-1") also consists of six 2:1 Muxes namely $F(1,2m-1)$, $F(1,2m)$, $U(1,2m-1)$, $U(1,2m)$, $B(1,2m-1)$, and $B(1,2m)$. The 2:1 Mux $F(1,2m-1)$ has two inputs namely $Fi(1,2m-1)$ and $Fi(1,2m)$ and has one output $Fo(1,2m-1)$. The 2:1 Mux $F(1,2m)$ has two inputs namely $Fi(1,2m-1)$ and $Fi(1,2m)$ and has one output $Fo(1,2m)$.

20 The 2:1 Mux $U(1,2m-1)$ has two inputs namely $Ui(1,2m-1)$ and $Fo(1,2m-1)$ and has one output $Uo(1,2m-1)$. The 2:1 Mux $U(1,2m)$ has two inputs namely $Ui(1,2m)$ and $Fo(1,2m)$ and has one output $Uo(1,2m)$. The 2:1 Mux $B(1,2m-1)$ has two inputs namely $Uo(1,2m-1)$ and $Uo(1,2m)$ and has one output $Bo(1,2m-1)$. The 2:1 Mux $B(1,2m)$ has two inputs namely $Uo(1,2m-1)$ and $Uo(1,2m)$ and has one output $Bo(1,2m)$.

25 The stage (ring 1, stage "m") consists of 4 inputs namely $Fi(1,2m+1)$, $Fi(1,2m+2)$, $Ui(1,2m+1)$, and $Ui(1,2m+2)$; and 4 outputs $Bo(1,2m+1)$, $Bo(1,2m+2)$, $Fo(1,2m+1)$, and $Fo(1,2m+2)$. The stage (ring 1, stage "m") also consists of six 2:1 Muxes namely $F(1,2m+1)$, $F(1,2m+2)$, $U(1,2m+1)$, $U(1,2m+2)$, $B(1,2m+1)$, and $B(1,2m+2)$. The 2:1 Mux $F(1,2m+1)$ has two inputs namely $Fi(1,2m+1)$ and $Fi(1,2m+2)$ and has one output

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Fo(1,2m+1). The 2:1 Mux F(1,2m+2) has two inputs namely Fi(1,2m+1) and Fi(1,2m+2) and has one output Fo(1,2m+2).

The 2:1 Mux U(1,2m+1) has two inputs namely Ui(1,2m+1) and Fo(1,2m+1) and has one output Uo(1,2m+1). The 2:1 Mux U(1,2m+2) has two inputs namely Ui(1,2m+2) and Fo(1,2m+2) and has one output Uo(1,2m+2). The 2:1 Mux B(1,2m+1) has two inputs namely Uo(1,2m+1) and Uo(1,2m+2) and has one output Bo(1,2m+1). The 2:1 Mux B(1,2m+2) has two inputs namely Uo(1,2m+1) and Uo(1,2m+2) and has one output Bo(1,2m+2).

The output Fo(1,2m-1) of the stage (ring 1, stage "m-1") is connected to the input Fi(1,2m+1) of the stage (ring 1, stage "m"), is an internal connection between stage "m-1" and stage "m" of the ring 1. And the output Bo(1,2m+1) of the stage (ring 1, stage "m") is connected to the input Ui(1,2m-1) of the stage (ring 1, stage "m-1"), is another internal connection between stage "m-1" and stage "m" of the ring 1

Just the same way the stages (ring 1, stage 0), (ring 1, stage 1), there are also stages (ring 1, stage 2), (ring 1, stage 3), ... (ring 1, stage "m-1"), (ring 1, stage "m") in that order, where the stages from (ring 1, stage 2), (ring 1, stage 3), ... , (ring 1, stage "m-2") are not shown in the diagram 100B. Just the same way the two successive stages (ring 1, stage 0) and (ring 1, stage 1) have internal connections between them as described before, any two successive stages have similar internal connections. For example (ring 1, stage 1) and (ring 1, stage 2) have similar internal connections and (ring 1, stage "m-2") and (ring 1, stage "m-1") have similar internal connections.

Stage (ring 1, stage 0) is also called hereinafter the "entry stage" or "first stage" of ring 1, since inlet links and outlet links of the computational block are directly connected to stage (ring 1, stage 0). Also stage (ring 1, stage "m") is hereinafter the "last stage" or "root stage" of ring 1.

The stage (ring 2, stage 0) consists of 4 inputs namely Fi(2,1), Fi(2,2), Ui(2,1), and Ui(2,2); and 4 outputs Bo(2,1), Bo(2,2), Fo(2,1), and Fo(2,2). The stage (ring 2, stage 0) also consists of six 2:1 Muxes namely F(2,1), F(2,2), U(2,1), U(2,2), B(2,1), and B(2,2). The 2:1 Mux F(2,1) has two inputs namely Fi(2,1) and Fi(2,2) and has one output

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Fo(2,1). The 2:1 Mux F(2,2) has two inputs namely Fi(2,1) and Fi(2,2) and has one output Fo(2,2).

The 2:1 Mux U(2,1) has two inputs namely Ui(2,1) and Fo(2,1) and has one output Uo(2,1). The 2:1 Mux U(2,2) has two inputs namely Ui(2,2) and Fo(2,2) and has one output Uo(2,2). The 2:1 Mux B(2,1) has two inputs namely Uo(2,1) and Uo(2,2) and has one output Bo(2,1). The 2:1 Mux B(2,2) has two inputs namely Uo(2,1) and Uo(2,2) and has one output Bo(2,2).

The stage (ring 2, stage 1) consists of 4 inputs namely Fi(2,3), Fi(2,4), Ui(2,3), and Ui(2,4); and 4 outputs Bo(2,3), Bo(2,4), Fo(2,3), and Fo(2,4). The stage (ring 2, stage 1) also consists of six 2:1 Muxes namely F(2,3), F(2,4), U(2,3), U(2,4), B(2,3), and B(2,4). The 2:1 Mux F(2,3) has two inputs namely Fi(2,3) and Fi(2,4) and has one output Fo(2,3). The 2:1 Mux F(2,4) has two inputs namely Fi(2,3) and Fi(2,4) and has one output Fo(2,4).

The 2:1 Mux U(2,3) has two inputs namely Ui(2,3) and Fo(2,3) and has one output Uo(2,3). The 2:1 Mux U(2,4) has two inputs namely Ui(2,4) and Fo(2,4) and has one output Uo(2,4). The 2:1 Mux B(2,3) has two inputs namely Uo(2,3) and Uo(2,4) and has one output Bo(2,3). The 2:1 Mux B(2,4) has two inputs namely Uo(2,3) and Uo(2,4) and has one output Bo(2,4).

The output Fo(2,1) of the stage (ring 2, stage 0) is connected to the input Fi(2,3) of the stage (ring 2, stage 1), is an internal connection between stage 0 and stage 1 of the ring 2. And the output Bo(2,3) of the stage (ring 2, stage 1) is connected to the input Ui(2,1) of the stage (ring 2, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1..

The stage (ring 2, stage "n-1") consists of 4 inputs namely Ri(2,2n-1), Ri(2,2n), Ui(1,2n-1), and Ui(1,2n); and 4 outputs Bo(1,2n-1), Bo(1,2n), Fo(1,2n-1), and Fo(1,2n). The stage (ring 2, stage "n-1") also consists of eight 2:1 Muxes namely R(2,2n-1), R(2,2n), F(2,2n-1), F(1,2n), U(1,2n-1), U(1,2n), B(1,2n-1), and B(1,2n). The 2:1 Mux R(2,2n-1) has two inputs namely Ri(2,2n-1) and Bo(2,2n-1) and has one output Ro(2,2n-1). The 2:1 Mux R(2,2n) has two inputs namely Ri(2,2n) and Bo(2,2n) and has one output Ro(2,2n). The 2:1 Mux F(2,2n-1) has two inputs namely Ro(2,2n-1) and Ro(2,2n) and has

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

one output $Fo(2,2n-1)$. The 2:1 Mux $F(2,2n)$ has two inputs namely $Ro(2,2n-1)$ and $Ro(2,2n)$ and has one output $Fo(2,2n)$.

The 2:1 Mux $U(2,2n-1)$ has two inputs namely $Ui(2,2n-1)$ and $Fo(2,2n-1)$ and has one output $Uo(2,2n-1)$. The 2:1 Mux $U(2,2n)$ has two inputs namely $Ui(2,2n)$ and $Fo(2,2n)$ and has one output $Uo(2,2n)$. The 2:1 Mux $B(2,2n-1)$ has two inputs namely $Uo(2,2n-1)$ and $Uo(2,2n)$ and has one output $Bo(2,2n-1)$. The 2:1 Mux $B(2,2n)$ has two inputs namely $Uo(2,2n-1)$ and $Uo(2,2n)$ and has one output $Bo(2,2n)$.

The stage (ring 2, stage "n") consists of 4 inputs namely $Ri(2,2n+1)$, $Ri(2,2n+2)$, $Ui(2,2n+1)$, and $Ui(2,2n+2)$; and 4 outputs $Bo(2,2n+1)$, $Bo(2,2n+2)$, $Fo(2,2n+1)$, and $Fo(2,2n+2)$. The stage (ring 2, stage "n") also consists of eight 2:1 Muxes namely $R(2,2n+1)$, $R(2,2n+2)$, $F(2,2n+1)$, $F(2,2n+2)$, $U(2,2n+1)$, $U(2,2n+2)$, $B(2,2n+1)$, and $B(2,2n+2)$. The 2:1 Mux $R(2,2n+1)$ has two inputs namely $Ri(2,2n+1)$ and $Bo(2,2n+1)$ and has one output $Ro(2,2n+1)$. The 2:1 Mux $R(2,2n+2)$ has two inputs namely $Ri(2,2n+2)$ and $Bo(2,2n+2)$ and has one output $Ro(2,2n+2)$. The 2:1 Mux $F(2,2n+1)$ has two inputs namely $Ro(2,2n+1)$ and $Ro(2,2n+2)$ and has one output $Fo(2,2n+1)$. The 2:1 Mux $F(2,2n+2)$ has two inputs namely $Ro(2,2n+1)$ and $Ro(2,2n+2)$ and has one output $Fo(2,2n+2)$.

The 2:1 Mux $U(2,2n+1)$ has two inputs namely $Ui(2,2n+1)$ and $Fo(2,2n+1)$ and has one output $Uo(2,2n+1)$. The 2:1 Mux $U(2,2n+2)$ has two inputs namely $Ui(2,2n+2)$ and $Fo(2,2n+2)$ and has one output $Uo(2,2n+2)$. The 2:1 Mux $B(2,2n+1)$ has two inputs namely $Uo(2,2n+1)$ and $Uo(2,2n+2)$ and has one output $Bo(2,2n+1)$. The 2:1 Mux $B(2,2n+2)$ has two inputs namely $Uo(2,2n+1)$ and $Uo(2,2n+2)$ and has one output $Bo(2,2n+2)$.

The output $Fo(2,2n-1)$ of the stage (ring 2, stage "n-1") is connected to the input $Ri(2,2n+1)$ of the stage (ring 2, stage "n"), is an internal connection between stage "n-1" and stage "n" of the ring 1. And the output $Bo(2,2n+1)$ of the stage (ring 2, stage "n") is connected to the input $Ui(2,2n-1)$ of the stage (ring 2, stage "n-1"), is another internal connection between stage "n-1" and stage "n" of the ring 1.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Each stage of any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of $2 * d = 4$ outputs. Even though each stage has four 4:1 muxes, in other embodiments any of these stages can be one of the four by four switch diagrams namely 200A of FIG. 2A, 200B of FIG. 2B, 200C of FIG. 2C, and one
 5 of the eight by four switch diagrams namely 200E of FIG. 2E, 200F of FIG. 2F.

In general, any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ may have inputs and outputs connected from computational block from either only from left-hand side as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A; or only from right-hand side; or from both left-hand and right-
 10 hand sides as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B.

Referring to diagram 100C in FIG. 1C, in one embodiment, an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ where $N_1 = 400$; $N_2 = 1600$; $d = 2$; and $s = 1$ corresponding to one computational block, with each computational block having 16 inlet links namely I1, I2, I3, I4, I5, I6, I7, I8, I9, I10, I11, I12, I13, I14, I15,
 15 and I16 ; and 4 outlet links namely O1, O2, O3, and O4. And for each computational block the corresponding partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C consists of two slices namely slice 1 and slice 2. Slice 1 consists of two rings namely (slice 1, ring 1) and (slice 1, ring 2). Similarly slice 2 consists of two rings namely (slice 2, ring 1) and (slice 2, ring 2).

20 The ring (slice 1, ring 1) consists of “m+1” stages namely (slice 1, ring 1, stage 0), (slice 1, ring 1, stage 1), ... (slice 1, ring 1, stage “m-1”), and (slice 1, ring 1, stage “m”). And the ring (slice 1, ring 2) consists of “n+1” stages namely (slice 1, ring 2, stage 0), (slice 1, ring 2, stage 1), ... (slice 1, ring 2, stage “n-1”), and (slice 1, ring 2, stage “n”), where “m” and “n” are positive integers.

25 Similarly the ring (slice 2, ring 1) consists of “x+1” stages namely (slice 2, ring 1, stage 0), (slice 2, ring 1, stage 1), ... (slice 2, ring 1, stage “x-1”), and (slice 2, ring 1, stage “x”). And the ring (slice 2, ring 2) consists of “y+1” stages namely (slice 2, ring 2, stage 0), (slice 2, ring 2, stage 1), ... (slice 2, ring 2, stage “y-1”), and (slice 2, ring 2, stage “y”), where “x” and “y” are positive integers.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

In general “m” may be or may not be equal to “x” and “n” may be or may not be equal to “y”. Also in general, “m” may be or may not be equal to “n” and “x” may be or may not be equal to “y”.

Ring (slice 1, ring 1) has inlet links $Ri(1,1,1)$ and $Ri(1,1,2)$ from the left-hand side, and has outlet links $Bo(1,1,1)$ and $Bo(1,1,2)$ from left-hand side. Ring (slice 1, ring 1) also has inlet links $Ui(1,1,2m+1)$ and $Ui(1,1,2m+2)$ from the right-hand side, and has outlet links $Fo(1,1,2m+1)$ and $Fo(1,1,2m+2)$ from right-hand side. Ring (slice 1, ring 2) has inlet links $Ri(1,2,1)$ and $Ri(1,2,2)$ from left-hand side, and outlet links $Bo(1,2,1)$ and $Bo(1,2,2)$ from left-hand side. Ring (slice 1, ring 2) also has inlet links $Ui(1,2,2n+1)$ and $Ui(1,2,2n+2)$ from the right-hand side, and has outlet links $Fo(1,2,2n+1)$ and $Fo(1,2,2n+2)$ from right-hand side.

Ring (slice 2, ring 1) has inlet links $Ri(2,1,1)$ and $Ri(2,1,2)$ from the left-hand side, and has outlet links $Bo(2,1,1)$ and $Bo(2,1,2)$ from left-hand side. Ring (slice 2, ring 1) also has inlet links $Ui(2,1,2x+1)$ and $Ui(2,1,2x+2)$ from the right-hand side, and has outlet links $Fo(2,1,2x+1)$ and $Fo(2,1,2x+2)$ from right-hand side. Ring (slice 2, ring 2) has inlet links $Ri(2,2,1)$ and $Ri(2,2,2)$ from left-hand side, and outlet links $Bo(2,2,1)$ and $Bo(2,2,2)$ from left-hand side. Ring (slice 2, ring 2) also has inlet links $Ui(2,2,2y+1)$ and $Ui(2,2,2y+2)$ from the right-hand side, and has outlet links $Fo(2,2,2y+1)$ and $Fo(2,2,2y+2)$ from right-hand side.

And the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C consists of 16 inlet links and 4 outlet links corresponding to the two slices slice 1 and slice 2. From left-hand side, outlet link O1 of the computational block is connected to inlet link $Ri(1,1,1)$ of ring (slice 1, ring 1) and also inlet link of $Ri(1,2,1)$ of ring (slice 1, ring 2). Similarly from left-hand side, outlet link O2 of the computational block is connected to inlet link $Ri(1,1,2)$ of Ring (slice 1, ring 1) and also inlet link of $Ri(1,2,2)$ of Ring (slice 1, ring 2). And from left-hand side, outlet link $Bo(1,1,1)$ of Ring (slice 1, ring 1) is connected to inlet link I1 of the computational block. From left-hand side, Outlet link $Bo(1,1,2)$ of Ring (slice 1, ring 1) is connected to inlet link I2 of the computational block. Similarly from left-hand side, outlet link $Bo(1,2,1)$ of Ring (slice 1, ring 2) is connected to inlet link I3 of the computational block. From left-hand side, outlet link $Bo(1,2,2)$ of Ring (slice 1, ring 2) is connected to inlet link I4 of the computational block.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

From right-hand side, outlet link O1 of the computational block is connected to inlet link $U_i(1,1,2m+1)$ of ring (slice 1, ring 1) and also inlet link of $U_i(1,2,2n+1)$ of ring (slice 1, ring 2). Similarly from right-hand side, outlet link O2 of the computational block is connected to inlet link $U_i(1,1,2m+2)$ of Ring (slice 1, ring 1) and also inlet link of $U_i(1,2,2n+2)$ of Ring (slice 1, ring 2). And from right-hand side, outlet link $F_o(1,1,2m+1)$ of Ring (slice 1, ring 1) is connected to inlet link I5 of the computational block. From right-hand side, outlet link $F_o(1,1,2m+2)$ of Ring (slice 1, ring 1) is connected to inlet link I6 of the computational block. Similarly from right-hand side, outlet link $F_o(1,2,2n+1)$ of Ring (slice 1, ring 2) is connected to inlet link I7 of the computational block. From right-hand side, outlet link $F_o(1,2,2n+2)$ of Ring (slice 1, ring 2) is connected to inlet link I8 of the computational block.

From left-hand side, outlet link O3 of the computational block is connected to inlet link $R_i(2,1,1)$ of ring (slice 2, ring 1) and also inlet link of $R_i(2,2,1)$ of ring (slice 2, ring 2). Similarly from left-hand side, outlet link O4 of the computational block is connected to inlet link $R_i(2,1,2)$ of Ring (slice 2, ring 1) and also inlet link of $R_i(2,2,2)$ of Ring (slice 2, ring 2). And from left-hand side, outlet link $B_o(2,1,1)$ of Ring (slice 2, ring 1) is connected to inlet link I9 of the computational block. From left-hand side, Outlet link $B_o(2,1,2)$ of Ring (slice 2, ring 1) is connected to inlet link I10 of the computational block. Similarly from left-hand side, outlet link $B_o(2,2,1)$ of Ring (slice 2, ring 2) is connected to inlet link I11 of the computational block. From left-hand side, outlet link $B_o(2,2,2)$ of Ring (slice 2, ring 2) is connected to inlet link I12 of the computational block.

From right-hand side, outlet link O3 of the computational block is connected to inlet link $U_i(2,1,2x+1)$ of ring (slice 2, ring 1) and also inlet link of $U_i(2,2,2y+1)$ of ring (slice 2, ring 2). Similarly from right-hand side, outlet link O4 of the computational block is connected to inlet link $U_i(2,1,2x+2)$ of Ring (slice 2, ring 1) and also inlet link of $U_i(2,2,2y+2)$ of Ring (slice 2, ring 2). And from right-hand side, outlet link $F_o(2,1,2x+1)$ of Ring (slice 2, ring 1) is connected to inlet link I13 of the computational block. From right-hand side, outlet link $F_o(2,1,2x+2)$ of Ring (slice 2, ring 1) is connected to inlet link I14 of the computational block. Similarly from right-hand side, outlet link $F_o(2,2,2y+1)$ of Ring (slice 2, ring 2) is connected to inlet link I15 of the computational block. From

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

right-hand side, outlet link $Fo(2,2,2y+2)$ of Ring (slice 2, ring 2) is connected to inlet link I16 of the computational block.

In this embodiment outlet links O1 and O2 of the computational block are connected only to slice 1. Similarly outlet links O3 and O4 of the computational block are
5 connected only to slice 2.

Referring to two dimensional grid 800 in FIG. 8 illustrates, in another embodiment, each block of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C with 4 inlet links and 16 outlet links and the corresponding computational block with 16 inlet links and 4 outlet links. For example
10 block (1,1) of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C with 4 inlet links and 16 outlet links and the corresponding computational block with 16 inlet links and 4 outlet links. Similarly each of the 100 blocks of 2D-grid 800 has a separate partial multi-stage hierarchical network
15 $V_{Comb}(N_1, N_2, d, s)$ 100C with 4 inlet links and 16 outlet links and the corresponding computational block with 16 inlet links and 4 outlet links. Hence the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to 2D-grid 800 has $N_1 = 400$ inlet links and $N_2 = 1600$ outlet links. Since there are 100 computational blocks each one corresponding to one of the blocks with each computational block having 16 inlet links and 4 outlet links. Also the 2D-grid 800 is organized in the fourth quadrant of the 2D-
20 Plane. In other embodiments the 2D-grid 800 may be organized as either first quadrant, or second quadrant or third quadrant of the 2D-Plane.

Referring to partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C, the stage (slice 1, ring 1, stage 0) consists of 8 inputs namely $Ri(1,1,1)$, $Ri(1,1,2)$, $Ui(1,1,1)$, $Ui(1,1,2)$, $J(1,1,1)$, $K(1,1,1)$, $L(1,1,1)$, and $M(1,1,1)$; and 4 outputs
25 $Bo(1,1,1)$, $Bo(1,1,2)$, $Fo(1,1,1)$, and $Fo(1,1,2)$. The stage (slice 1, ring "1", stage "0") also consists of four 4:1 Muxes namely $F(1,1,1)$, $F(1,1,2)$, $B(1,1,1)$, and $B(1,1,2)$. The 4:1 Mux $F(1,1,1)$ has four inputs namely $Ri(1,1,1)$, $Ri(1,1,2)$, $Ui(1,1,2)$, and $J(1,1,1)$, and has one output $Fo(1,1,1)$. The 4:1 Mux $F(1,1,2)$ has four inputs namely $Ri(1,1,1)$, $Ri(1,1,2)$, $Ui(1,1,1)$, and $K(1,1,1)$, and has one output $Fo(1,1,2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 4:1 Mux B(1,1,1) has four inputs namely $U_i(1,1,1)$, $U_i(1,1,2)$, $R_i(1,1,2)$, and $L(1,1,1)$, and has one output $Bo(1,1,1)$. The 4:1 Mux B(1,1,2) has four inputs namely $U_i(1,1,1)$, $U_i(1,1,2)$, $R_i(1,1,1)$ and $M(1,1,1)$, and has one output $Bo(1,1,2)$. In different embodiments the inputs $J(1,1,1)$, $K(1,1,1)$, $L(1,1,1)$, and $M(1,1,1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 1, ring 1, stage "m") consists of 8 inputs namely $R_i(1,1,2m+1)$, $R_i(1,1,2m+2)$, $U_i(1,1,2m+1)$, $U_i(1,1,2m+2)$, $J(1,1,m+1)$, $K(1,1,m+1)$, $L(1,1,m+1)$, and $M(1,1,m+1)$; and 4 outputs $Bo(1,1,2m+1)$, $Bo(1,1,2m+2)$, $Fo(1,1,2m+1)$, and $Fo(1,1,2m+2)$. The stage (slice 1, ring 1, stage "m") also consists of four 4:1 Muxes namely $F(1,1,2m+1)$, $F(1,1,2m+2)$, $B(1,1,2m+1)$, and $B(1,1,2m+2)$. The 4:1 Mux $F(1,1,2m+1)$ has four inputs namely $R_i(1,1,2m+1)$, $R_i(1,1,2m+2)$, $U_i(1,1,2m+2)$, and $J(1,1,m+1)$, and has one output $Fo(1,1,2m+1)$. The 4:1 Mux $F(1,1,2m+2)$ has four inputs namely $R_i(1,1,2m+1)$, $R_i(1,1,2m+2)$, $U_i(1,1,2m+1)$, and $K(1,1,m+1)$, and has one output $Fo(1,1,2m+2)$.

The 4:1 Mux B(1,1,2m+1) has four inputs namely $U_i(1,1,2m+1)$, $U_i(1,1,2m+2)$, $R_i(1,1,2m+2)$, and $L(1,1,m+1)$, and has one output $Bo(1,1,2m+1)$. The 4:1 Mux B(1,1,2m+2) has four inputs namely $U_i(1,1,2m+1)$, $U_i(1,1,2m+2)$, $R_i(1,1,2m+1)$ and $M(1,1,m+1)$, and has one output $Bo(1,1,2m+2)$. In different embodiments the inputs $J(1,1,m+1)$, $K(1,1,m+1)$, $L(1,1,m+1)$, and $M(1,1,m+1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 1, ring 1, stage 0), there are also stages (slice 1, ring 1, stage 1), (slice 1, ring 1, stage 2), (slice 1, ring 1, stage 3), ... (slice 1, ring 1, stage "m-1"), (slice 1, ring 1, stage "m") in that order, where the stages from (slice 1, ring 1, stage 1), (slice 1, ring 1, stage 2), ... , (slice 1, ring 1, stage "m-1") are not shown in the diagram 100C.

Referring to diagram 100C5 in FIG. 1C5 illustrates specific details of partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C, particularly the internal connections between two successive stages of any ring of any slice, in one

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

embodiment. The stage (slice “c”, ring “d”, stage “e”) consists of 8 inputs namely $Ri(c,d,2e+1)$, $Ri(c,d,2e+2)$, $Ui(c,d,2e+1)$, $Ui(c,d,2e+2)$, $J(c,d,e+1)$, $K(c,d,e+1)$, $L(c,d,e+1)$, and $M(c,d,e+1)$; and 4 outputs $Bo(c,d,2e+1)$, $Bo(c,d,2e+2)$, $Fo(c,d,2e+1)$, and $Fo(c,d,2e+2)$. The stage (slice “c”, ring “d”, stage “e”) also consists of four 4:1 Muxes
 5 namely $F(c,d,2e+1)$, $F(c,d,2e+2)$, $B(c,d,2e+1)$, and $B(c,d,2e+2)$. The 4:1 Mux $F(c,d,2e+1)$ has four inputs namely $Ri(c,d,2e+1)$, $Ri(c,d,2e+2)$, $Ui(c,d,2e+2)$, and $J(c,d,e+1)$, and has one output $Fo(c,d,2e+1)$. The 4:1 Mux $F(c,d,2e+2)$ has four inputs namely $Ri(c,d,2e+1)$, $Ri(c,d,2e+2)$, $Ui(c,d,2e+1)$, and $K(c,d,e+1)$, and has one output $Fo(c,d,2e+2)$.

The 4:1 Mux $B(c,d,2e+1)$ has four inputs namely $Ui(c,d,2e+1)$, $Ui(c,d,2e+2)$,
 10 $Ri(c,d,2e+2)$, and $L(c,d,e+1)$, and has one output $Bo(c,d,2e+1)$. The 4:1 Mux $B(c,d,2e+2)$ has four inputs namely $Ui(c,d,2e+1)$, $Ui(c,d,2e+2)$, $Ri(c,d,2e+1)$ and $M(c,d,e+1)$, and has one output $Bo(c,d,2e+2)$. In different embodiments the inputs $J(c,d,e+1)$, $K(c,d,e+1)$, $L(c,d,e+1)$, and $M(c,d,e+1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

15 The stage (slice “c”, ring “d”, stage “e+1”) consists of 8 inputs namely $Ri(c,d,2e+3)$, $Ri(c,d,2e+4)$, $Ui(c,d,2e+3)$, $Ui(c,d,2e+4)$, $J(c,d,e+2)$, $K(c,d,e+2)$, $L(c,d,e+2)$, and $M(c,d,e+2)$; and 4 outputs $Bo(c,d,2e+3)$, $Bo(c,d,2e+4)$, $Fo(c,d,2e+3)$, and $Fo(c,d,2e+4)$. The stage (slice “c”, ring “d”, stage “e+1”) also consists of four 4:1 Muxes
 20 namely $F(c,d,2e+3)$, $F(c,d,2e+4)$, $B(c,d,2e+3)$, and $B(c,d,2e+4)$. The 4:1 Mux $F(c,d,2e+3)$ has four inputs namely $Ri(c,d,2e+3)$, $Ri(c,d,2e+4)$, $Ui(c,d,2e+4)$, and $J(c,d,e+2)$, and has one output $Fo(c,d,2e+3)$. The 4:1 Mux $F(c,d,2e+4)$ has four inputs namely $Ri(c,d,2e+3)$, $Ri(c,d,2e+4)$, $Ui(c,d,2e+3)$, and $K(c,d,e+2)$, and has one output $Fo(c,d,2e+4)$.

The 4:1 Mux $B(c,d,2e+3)$ has four inputs namely $Ui(c,d,2e+3)$, $Ui(c,d,2e+4)$,
 25 $Ri(c,d,2e+4)$, and $L(c,d,e+2)$, and has one output $Bo(c,d,2e+3)$. The 4:1 Mux $B(c,d,2e+4)$ has four inputs namely $Ui(c,d,2e+3)$, $Ui(c,d,2e+4)$, $Ri(c,d,2e+3)$ and $M(c,d,e+2)$, and has one output $Bo(c,d,2e+4)$. In different embodiments the inputs $J(c,d,e+2)$, $K(c,d,e+2)$, $L(c,d,e+2)$, and $M(c,d,e+2)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The output $Fo(c,d,2e+1)$ of the stage (slice “c”, ring “d”, stage “e”) is connected
 30 to the input $Ri(c,d,2e+3)$ of the stage (slice “c”, ring “d”, stage “e+1”) which is called

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

hereinafter an internal connection between two successive stages of a ring. And the output $Bo(c,d,2e+3)$ of the stage (slice “c”, ring “d”, stage “e+1”) is connected to the input $Ui(c,d,2e+1)$ of the stage (slice “c”, ring “d”, stage “e”), is another internal connection between stage “e” and stage “e+1” of the ring (slice “c”, ring “d”).

5 Just the same way the two successive stages (slice “c”, ring “d”, stage “e”) and (slice “c”, ring “d”, stage “e+1”) have internal connections between them as described above, any two successive stages have similar internal connections for any values of “c”, “d”, “e” of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C belonging to any block of the two dimensional grid 800 in FIG. 8, in some
10 embodiments. For example stage (slice 1, ring 1, stage 0) and stage (slice 1, ring 1, stage 1) have similar internal connections; and stage (slice 1, ring 1, stage “m-1”) and stage (slice 1, ring 1, stage “m”) have similar internal connections.

Stage (slice 1, ring 1, stage 0) is also called hereinafter the “entry stage” or “first stage” of (slice 1, ring 1), since inlet links and outlet links of the computational block are
15 directly connected to stage (slice 1, ring 1, stage 0). Also stage (slice 1, ring 1, stage “m”) is hereinafter the “last stage” or “root stage” of (slice 1, ring 1).

The stage (slice 1, ring 2, stage 0) consists of 8 inputs namely $Ri(1,2,1)$, $Ri(1,2,2)$, $Ui(1,2,1)$, $Ui(1,2,2)$, $J(1,2,1)$, $K(1,2,1)$, $L(1,2,1)$, and $M(1,2,1)$; and 4 outputs $Bo(1,2,1)$, $Bo(1,2,2)$, $Fo(1,2,1)$, and $Fo(1,2,2)$. The stage (slice 1, ring “2”, stage “0”) also consists
20 of four 4:1 Muxes namely $F(1,2,1)$, $F(1,2,2)$, $B(1,2,1)$, and $B(1,2,2)$. The 4:1 Mux $F(1,2,1)$ has four inputs namely $Ri(1,2,1)$, $Ri(1,2,2)$, $Ui(1,2,2)$, and $J(1,2,1)$, and has one output $Fo(1,2,1)$. The 4:1 Mux $F(1,2,2)$ has four inputs namely $Ri(1,2,1)$, $Ri(1,2,2)$, $Ui(1,2,1)$, and $K(1,2,1)$, and has one output $Fo(1,2,2)$.

The 4:1 Mux $B(1,2,1)$ has four inputs namely $Ui(1,2,1)$, $Ui(1,2,2)$, $Ri(1,2,2)$, and
25 $L(1,2,1)$, and has one output $Bo(1,2,1)$. The 4:1 Mux $B(1,2,2)$ has four inputs namely $Ui(1,2,1)$, $Ui(1,2,2)$, $Ri(1,2,1)$ and $M(1,2,1)$, and has one output $Bo(1,2,2)$. In different embodiments the inputs $J(1,2,1)$, $K(1,2,1)$, $L(1,2,1)$, and $M(1,2,1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The stage (slice 1, ring 2, stage “n”) consists of 8 inputs namely $R_i(1,2,2n+1)$, $R_i(1,2,2n+2)$, $U_i(1,2,2n+1)$, $U_i(1,2,2n+2)$, $J(1,2,n+1)$, $K(1,2,n+1)$, $L(1,2,n+1)$, and $M(1,2,n+1)$; and 4 outputs $B_o(1,2,2n+1)$, $B_o(1,2,2n+2)$, $F_o(1,2,2n+1)$, and $F_o(1,2,2n+2)$. The stage (slice 1, ring 2, stage “n”) also consists of four 4:1 Muxes namely $F(1,2,2n+1)$, $F(1,2,2n+2)$, $B(1,2,2n+1)$, and $B(1,2,2n+2)$. The 4:1 Mux $F(1,2,2n+1)$ has four inputs namely $R_i(1,2,2n+1)$, $R_i(1,2,2n+2)$, $U_i(1,2,2n+2)$, and $J(1,2,n+1)$, and has one output $F_o(1,2,2n+1)$. The 4:1 Mux $F(1,2,2n+2)$ has four inputs namely $R_i(1,2,2n+1)$, $R_i(1,2,2n+2)$, $U_i(1,2,2n+1)$, and $K(1,2,n+1)$, and has one output $F_o(1,2,2n+2)$.

The 4:1 Mux $B(1,2,2n+1)$ has four inputs namely $U_i(1,2,n+1)$, $U_i(1,2,2n+2)$, $R_i(1,2,2n+2)$, and $L(1,2,n+1)$, and has one output $B_o(1,2,2n+1)$. The 4:1 Mux $B(1,2,2n+2)$ has four inputs namely $U_i(1,2,2n+1)$, $U_i(1,2,2n+2)$, $R_i(1,2,2n+1)$ and $M(1,2,n+1)$, and has one output $B_o(1,2,2n+2)$. In different embodiments the inputs $J(1,2,n+1)$, $K(1,2,n+1)$, $L(1,2,n+1)$, and $M(1,2,n+1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 1, ring 2, stage 0), there are also stages (slice 1, ring 2, stage 1), (slice 1, ring 2, stage 2), (slice 1, ring 2, stage 3), ... (slice 1, ring 2, stage “n-1”), (slice 1, ring 2, stage “n”) in that order, where the stages from (slice 1, ring 2, stage 1), (slice 1, ring 2, stage 2), ... , (slice 1, ring 2, stage “n-1”) are not shown in the diagram 100C.

The stage (slice 2, ring 1, stage 0) consists of 8 inputs namely $R_i(2,1,1)$, $R_i(2,1,2)$, $U_i(2,1,1)$, $U_i(2,1,2)$, $J(2,1,1)$, $K(2,1,1)$, $L(2,1,1)$, and $M(2,1,1)$; and 4 outputs $B_o(2,1,1)$, $B_o(2,1,2)$, $F_o(2,1,1)$, and $F_o(2,1,2)$. The stage (slice 2, ring “1”, stage “0”) also consists of four 4:1 Muxes namely $F(2,1,1)$, $F(2,1,2)$, $B(2,1,1)$, and $B(2,1,2)$. The 4:1 Mux $F(2,1,1)$ has four inputs namely $R_i(2,1,1)$, $R_i(2,1,2)$, $U_i(2,1,2)$, and $J(2,1,1)$, and has one output $F_o(2,1,1)$. The 4:1 Mux $F(2,1,2)$ has four inputs namely $R_i(2,1,1)$, $R_i(2,1,2)$, $U_i(2,1,1)$, and $K(2,1,1)$, and has one output $F_o(2,1,2)$.

The 4:1 Mux $B(2,1,1)$ has four inputs namely $U_i(2,1,1)$, $U_i(2,1,2)$, $R_i(2,1,2)$, and $L(2,1,1)$, and has one output $B_o(2,1,1)$. The 4:1 Mux $B(2,1,2)$ has four inputs namely $U_i(2,1,1)$, $U_i(2,1,2)$, $R_i(2,1,1)$ and $M(2,1,1)$, and has one output $B_o(2,1,2)$. In different

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

embodiments the inputs J(2,1,1), K(2,1,1), L(2,1,1), and M(2,1,1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 2, ring 1, stage "x") consists of 8 inputs namely Ri(2,1,2x+1),
 5 Ri(2,1,2x+2), Ui(2,1,2x+1), Ui(2,1,2x+2), J(2,1,x+1), K(2,1,x+1), L(2,1,x+1), and
 M(2,1,x+1); and 4 outputs Bo(2,1,2x+1), Bo(2,1,2x+2), Fo(2,1,2x+1), and Fo(2,1,2x+2).
 The stage (slice 2, ring 1, stage "x") also consists of four 4:1 Muxes namely F(2,1,2x+1),
 F(2,1,2x+2), B(2,1,2x+1), and B(2,1,2x+2). The 4:1 Mux F(2,1,2x+1) has four inputs
 namely Ri(2,1,2x+1), Ri(2,1,2x+2), Ui(2,1,2x+2), and J(2,1,x+1), and has one output
 10 Fo(2,1,2x+1). The 4:1 Mux F(2,1,2x+2) has four inputs namely Ri(2,1,2x+1),
 Ri(2,1,2x+2), Ui(2,1,2x+1), and K(2,1,x+1), and has one output Fo(2,1,2x+2).

The 4:1 Mux B(2,1,2x+1) has four inputs namely Ui(2,1,2x+1), Ui(2,1,2x+2),
 Ri(2,1,2x+2), and L(2,1,x+1), and has one output Bo(2,1,2x+1). The 4:1 Mux
 B(2,1,2x+2) has four inputs namely Ui(2,1,2x+1), Ui(2,1,2x+2), Ri(2,1,2x+1) and
 15 M(2,1,x+1), and has one output Bo(2,1,2x+2). In different embodiments the inputs
 J(2,1,x+1), K(2,1,x+1), L(2,1,x+1), and M(2,1,x+1) are connected from any of the
 outputs of any other stages of any ring of any block of the multi-stage hierarchical
 network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 2, ring 1, stage 0), there are also stages (slice 2,
 20 ring 1, stage 1), (slice 2, ring 1, stage 2), (slice 2, ring 1, stage 3), ... (slice 2, ring 1, stage
 "m-1"), (slice 2, ring 1, stage "x") in that order, where the stages from (slice 2, ring 1,
 stage 1), (slice 2, ring 1, stage 2), ... , (slice 2, ring 1, stage "x-1") are not shown in the
 diagram 100C.

The stage (slice 2, ring 2, stage 0) consists of 8 inputs namely Ri(2,2,1), Ri(2,2,2),
 25 Ui(2,2,1), Ui(2,2,2), J(2,2,1), K(2,2,1), L(2,2,1), and M(2,2,1); and 4 outputs Bo(2,2,1),
 Bo(2,2,2), Fo(2,2,1), and Fo(2,2,2). The stage (slice 2, ring "2", stage "0") also consists
 of four 4:1 Muxes namely F(2,2,1), F(2,2,2), B(2,2,1), and B(2,2,2). The 4:1 Mux
 F(2,2,1) has four inputs namely Ri(2,2,1), Ri(2,2,2), Ui(2,2,2), and J(2,2,1), and has one
 output Fo(2,2,1). The 4:1 Mux F(2,2,2) has four inputs namely Ri(2,2,1), Ri(2,2,2),
 30 Ui(2,2,1), and K(2,2,1), and has one output Fo(2,2,2).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 4:1 Mux B(2,2,1) has four inputs namely $U_i(2,2,1)$, $U_i(2,2,2)$, $R_i(2,2,2)$, and $L(2,2,1)$, and has one output $Bo(2,2,1)$. The 4:1 Mux B(2,2,2) has four inputs namely $U_i(2,2,1)$, $U_i(2,2,2)$, $R_i(2,2,1)$ and $M(2,2,1)$, and has one output $Bo(2,2,2)$. In different embodiments the inputs $J(2,2,1)$, $K(2,2,1)$, $L(2,2,1)$, and $M(2,2,1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 2, ring 2, stage "x") consists of 8 inputs namely $R_i(2,2,2x+1)$, $R_i(2,2,2x+2)$, $U_i(2,2,2x+1)$, $U_i(2,2,2x+2)$, $J(2,2,x+1)$, $K(2,2,x+1)$, $L(2,2,x+1)$, and $M(2,2,x+1)$; and 4 outputs $Bo(2,2,2x+1)$, $Bo(2,2,2x+2)$, $Fo(2,2,2x+1)$, and $Fo(2,2,2x+2)$. The stage (slice 2, ring 2, stage "y") also consists of four 4:1 Muxes namely $F(2,2,2y+1)$, $F(2,2,2y+2)$, $B(2,2,2y+1)$, and $B(2,2,2y+2)$. The 4:1 Mux $F(2,2,2y+1)$ has four inputs namely $R_i(2,2,2y+1)$, $R_i(2,2,2y+2)$, $U_i(2,2,2y+2)$, and $J(2,2,y+1)$, and has one output $Fo(2,2,2y+1)$. The 4:1 Mux $F(2,2,2y+2)$ has four inputs namely $R_i(2,2,2y+1)$, $R_i(2,2,2y+2)$, $U_i(2,2,2y+1)$, and $K(2,2,y+1)$, and has one output $Fo(2,2,2y+2)$.

The 4:1 Mux B(2,2,2y+1) has four inputs namely $U_i(2,2,2y+1)$, $U_i(2,2,2y+2)$, $R_i(2,2,2y+2)$, and $L(2,2,y+1)$, and has one output $Bo(2,2,2y+1)$. The 4:1 Mux B(2,2,2y+2) has four inputs namely $U_i(2,2,2y+1)$, $U_i(2,2,2y+2)$, $R_i(2,2,2y+1)$ and $M(2,2,y+1)$, and has one output $Bo(2,2,2y+2)$. In different embodiments the inputs $J(2,2,y+1)$, $K(2,2,y+1)$, $L(2,2,y+1)$, and $M(2,2,y+1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 2, ring 2, stage 0), there are also stages (slice 2, ring 2, stage 1), (slice 2, ring 2, stage 2), (slice 2, ring 2, stage 3), ... (slice 2, ring 2, stage "y-1"), (slice 2, ring 2, stage "y") in that order, where the stages from (slice 2, ring 2, stage 1), (slice 2, ring 2, stage 2), ... , (slice 2, ring 2, stage "y-1") are not shown in the diagram 100C.

As illustrated in diagram 100C5 in FIG. 1C5, the similar internal connections between two successive stages of any ring of any slice of partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C, in some embodiments are provided for all the slices $c = 1, 2$; for all the rings in each of the slices $d = 1, 2$; and for all the stages

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

namely when $c = 1, d = 1, e = [1, m]$; when $c=1, d=2, e=[1, n]$; when $c=2, d=1, e=[1, x]$; and when $c=2, d=2; e=[1, y]$.

Each stage of any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of $2 * d = 4$ outputs. Even though each stage has four
 5 4:1 muxes, in other embodiments any of these stages can be one of the four by four switch diagrams namely 200A of FIG. 2A, 200B of FIG. 2B, 200C of FIG. 2C, and one of the eight by four switch diagrams namely 200E of FIG. 2E, 200F of FIG. 2F.

In general, any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ illustrated in 100C also may have inputs and outputs connected from
 10 computational block from either only from left-hand side as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A; or only from right-hand side; or from both left-hand and right-hand sides as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B.

Applicant now notes a few aspects of the diagram 100C in FIG. 1C an exemplary
 15 partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to one computational block, with each computational block having 16 inlet links and 4 outlet links as follows: (Also these aspects are helpful in more optimization of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ as well as faster scheduling of the connections between outlet links of the computational blocks and the inlet links of the
 20 computational blocks.)

1) The partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C is divided into two slices namely slice 1 and slice 2. The outlet links of the computational block namely O1 and O2 are connected to only one slice i.e. slice 1. In other words outlet links O1 and O2 are absolutely not connected to slice 2. Similarly the
 25 outlet links of the computational block namely O3 and O4 are connected to only one slice i.e. slice 2. In other words outlet links O3 and O4 are absolutely not connected to slice 1.
 2) The second aspect is all the hop wires and multi-drop hop wires originating from slice 1 from any block will be terminating only in the slice 1 of any other block. Similarly all the hop wires and multi-drop hop wires originating from slice 2 from any block will be

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

terminating only in the slice 2 of any other block. 3) The third aspect is the mux whose output is directly connected to each inlet link of the computational block must have at least one input connected from each slice of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C. That is for example since the 4:1 mux B(1,1,1), belonging to slice 1, and having its output Bo(1,1,1) directly connected to inlet link I1 must have at least one of its inputs connecting from an output of a mux of a stage of a ring of slice 2 as well. This property must be satisfied for all the inlet links of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C.

Referring to diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 illustrate the details of the foregoing third aspect of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C. Applicant notes that diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 are all actually part of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C and these separate diagrams are necessary only to avoid the clutter in the diagram 100C of FIG. 1C.

The connections illustrated between different slices in diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 are the only connections between different slices, in some exemplary embodiments. In general the connections between different slices are given only at the terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block.

Referring to diagram 100C1 in FIG. 1C1 illustrate the connections between the stage (slice 1, ring 1, stage 0) and between the stage (slice 2, ring 1, stage 0). The same connection that is given to the input $U_i(1,1,1)$ is also connected to the input $L(2,1,1)$. The same connection that is given to the input $U_i(1,1,2)$ is also connected to the input $M(2,1,1)$. Similarly the same connection that is given to the input $U_i(2,1,1)$ is also connected to the input $L(1,1,1)$. The same connection that is given to the input $U_i(2,1,2)$ is also connected to the input $M(1,1,1)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Therefore inlet link I1 can be essentially connected through the 4:1 mux B(1,1,1) with three of its inputs connecting from slice 1 namely $U_i(1,1,1)$, $U_i(1,1,2)$, $R_i(1,1,2)$ and one input $L(1,1,1)$ connecting from slice 2. The inlet link I2 can be essentially connected through the 4:1 mux B(1,1,2) with three of its inputs connecting from slice 1 namely

5 $U_i(1,1,1)$, $U_i(1,1,2)$, $R_i(1,1,1)$ and one input $M(1,1,1)$ connecting from slice 2. The inlet link I9 can be essentially connected through the 4:1 mux B(1,2,1) with three of its inputs connecting from slice 2 namely $U_i(2,1,1)$, $U_i(2,1,2)$, $R_i(2,1,2)$ and one input $L(2,1,1)$ connecting from slice 1. The inlet link I10 can be essentially connected through the 4:1 mux B(2,1,2) with three of its inputs connecting from slice 2 namely $U_i(2,1,1)$, $U_i(2,1,2)$,

10 $R_i(2,1,1)$ and one input $M(2,1,1)$ connecting from slice 1. Hence all the inlet links I1, I2, I9 and I10 are all independently reachable from both slice 1 and slice2.

Referring to diagram 100C2 in FIG. 1C2 illustrate the connections between the stage (slice 1, ring 2, stage 0) and between the stage (slice 2, ring 2, stage 0). The same connection that is given to the input $U_i(1,2,1)$ is also connected to the input $M(2,2,1)$. The

15 same connection that is given to the input $U_i(1,2,2)$ is also connected to the input $L(2,2,1)$. Similarly the same connection that is given to the input $U_i(2,2,1)$ is also connected to the input $M(1,2,1)$. The same connection that is given to the input $U_i(2,2,2)$ is also connected to the input $L(1,2,1)$.

Therefore inlet link I3 can be essentially connected through the 4:1 mux B(1,2,1)

20 with three of its inputs connecting from slice 1 namely $U_i(1,2,1)$, $U_i(1,2,2)$, $R_i(1,2,2)$ and one input $M(2,2,1)$ connecting from slice 2. The inlet link I4 can be essentially connected through the 4:1 mux B(1,2,2) with three of its inputs connecting from slice 1 namely $U_i(1,2,1)$, $U_i(1,2,2)$, $R_i(1,2,1)$ and one input $M(1,2,1)$ connecting from slice 2. The inlet link I11 can be essentially connected through the 4:1 mux B(2,2,1) with three of its inputs

25 connecting from slice 2 namely $U_i(2,2,1)$, $U_i(2,2,2)$, $R_i(2,2,2)$ and one input $L(2,2,1)$ connecting from slice 1. The inlet link I12 can be essentially connected through the 4:1 mux B(2,2,2) with three of its inputs connecting from slice 2 namely $U_i(2,2,1)$, $U_i(2,2,2)$, $R_i(2,2,1)$ and one input $M(2,2,1)$ connecting from slice 1. Hence all the inlet links I3, I4, I11 and I12 are all independently reachable from both slice 1 and slice2.

30 Referring to diagram 100C3 in FIG. 1C3 illustrate the connections between the stage (slice 1, ring 1, stage "m") and between the stage (slice 2, ring 2, stage "y"). The

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

same connection that is given to the input $Ri(1,1,2m+1)$ is also connected to the input $J(2,2,y+1)$. The same connection that is given to the input $Ri(1,1,2m+2)$ is also connected to the input $K(2,2,y+1)$. Similarly the same connection that is given to the input $Ri(2,2,2y+1)$ is also connected to the input $J(1,1,m+1)$. The same connection that is given
 5 to the input $Ri(2,2,2y+2)$ is also connected to the input $K(1,1,m+1)$.

Therefore inlet link I5 can be essentially connected through the 4:1 mux $F(1,1,2m+1)$ with three of its inputs connecting from slice 1 namely $Ri(1,1,2m+1)$, $Ri(1,1,2m+2)$, $Ui(1,1,2m+2)$ and one input $J(1,1,m+1)$ connecting from slice 2. The inlet link I6 can be essentially connected through the 4:1 mux $F(1,1,2m+2)$ with three of its
 10 inputs connecting from slice 1 namely $Ri(1,1,2m+1)$, $Ri(1,1,2m+2)$, $Ui(1,1,2m+1)$ and one input $K(1,1,m+1)$ connecting from slice 2. The inlet link I15 can be essentially connected through the 4:1 mux $F(2,2,2y+1)$ with three of its inputs connecting from slice 2 namely $Ri(2,2,2y+1)$, $Ri(2,2,2y+2)$, $Ui(2,2,2y+2)$ and one input $J(2,2,y+1)$ connecting from slice 1. The inlet link I16 can be essentially connected through the 4:1 mux
 15 $F(2,2,2y+2)$ with three of its inputs connecting from slice 2 namely $Ri(2,2,2y+1)$, $Ri(2,2,2y+2)$, $Ui(2,2,2y+1)$ and one input $K(2,2,y+1)$ connecting from slice 1. Hence all the inlet links I5, I6, I15 and I16 are all independently reachable from both slice 1 and slice2.

Referring to diagram 100C4 in FIG. 1C4 illustrate the connections between the
 20 stage (slice 1, ring 2, stage "n") and between the stage (slice 2, ring 1, stage "x"). The same connection that is given to the input $Ri(1,2,2n+1)$ is also connected to the input $K(2,1,x+1)$. The same connection that is given to the input $Ri(1,2,2n+2)$ is also connected to the input $J(2,1,x+1)$. Similarly the same connection that is given to the input $Ri(2,1,2x+1)$ is also connected to the input $K(1,2,n+1)$. The same connection that is given
 25 to the input $Ri(2,1,2x+2)$ is also connected to the input $J(1,2,n+1)$.

Therefore inlet link I7 can be essentially connected through the 4:1 mux $F(1,2,2n+1)$ with three of its inputs connecting from slice 1 namely $Ri(1,2,2n+1)$, $Ri(1,2,2n+2)$, $Ui(1,2,2n+2)$ and one input $J(1,2,n+1)$ connecting from slice 2. The inlet link I8 can be essentially connected through the 4:1 mux $F(1,2,2n+2)$ with three of its
 30 inputs connecting from slice 1 namely $Ri(1,2,2n+1)$, $Ri(1,2,2n+2)$, $Ui(1,2,2n+1)$ and one input $K(1,2,n+1)$ connecting from slice 2. The inlet link I13 can be essentially connected

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

through the 4:1 mux $F(2,1,2x+1)$ with three of its inputs connecting from slice 2 namely $Ri(2,1,2x+1)$, $Ri(2,1,2x+2)$, $Ui(2,1,2x+2)$ and one input $J(2,1,x+1)$ connecting from slice 1. The inlet link I14 can be essentially connected through the 4:1 mux $F(2,1,2x+2)$ with three of its inputs connecting from slice 2 namely $Ri(2,1,2x+1)$, $Ri(2,1,2x+2)$,
 5 $Ui(2,1,2x+1)$ and one input $K(2,1,x+1)$ connecting from slice 1. Hence all the inlet links I7, I8, I13 and I14 are all independently reachable from both slice 1 and slice2.

The connections illustrated between different slices, in several embodiments, in diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 are the only connections between different slices. And
 10 also the terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block have three inputs coming from one slice and one input coming from another slice. In other embodiments it is also possible so that the terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block have two inputs coming from one slice and two inputs coming from
 15 another slice.

Also in general the number of slices in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C may be more than or equal to two. In such a case terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block will have at least one input coming from each slice. And the outlet
 20 links of the computational block will be divided and connected to each slice; however each outlet link of the computational block will be connected to only one slice. Also in general the hop wires and multi-drop hop wires are connected to only between the corresponding slices of different blocks, in some embodiments some of the hop wires and multi-drop hop wires may be connected between different slices of different blocks
 25 even if it is done partially.

FIG. 2A illustrates a stage (ring "k", stage "m") 200A consists of 4 inputs namely $Fi(k,2m+1)$, $Fi(k,2m+2)$, $Ui(k,2m+1)$, and $Ui(k,2m+2)$; and 4 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring "k", stage "m") also consists of six 2:1 Muxes namely $F(k,2m+1)$, $F(k,2m+2)$ (comprising in combination a forward switch), $U(k,2m+1)$, $U(k,2m+2)$ (comprising in combination a U-turn switch), $B(k,2m+1)$, and $B(k,2m+2)$ (comprising in combination a backward switch). The 2:1
 30

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Mux $F(k,2m+1)$ has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 2:1 Mux $U(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $F_o(k,2m+1)$ and
 5 has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

10 FIG. 2B illustrates a stage (ring “k”, stage “m”) 200B consists of 4 inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $U_i(k,2m+1)$, and $U_i(k,2m+2)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of eight 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$ (comprising in combination a Reverse U-turn switch), $F(k,2m+1)$, $F(k,2m+2)$ (comprising in combination a forward switch),
 15 $U(k,2m+1)$, $U(k,2m+2)$ (comprising in combination a U-turn switch), $B(k,2m+1)$, and $B(k,2m+2)$ (comprising in combination a backward switch). The 2:1 Mux $R(k,2m+1)$ has two inputs namely $R_i(k,2m+1)$ and $B_o(k,2m+1)$ and has one output $R_o(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and $B_o(k,2m+2)$ and has one output $R_o(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $R_o(k,2m+1)$ and
 20 $R_o(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $R_o(k,2m+1)$ and $R_o(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 2:1 Mux $U(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs
 25 namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

30 FIG. 2C illustrates a stage (ring “k”, stage “m”) 200C consists of 4 inputs namely $F_i(k,2m+1)$, $F_i(k,2m+2)$, $U_i(k,2m+1)$, and $U_i(k,2m+2)$; and 4 outputs $U_o(k,2m+1)$, $U_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring “k”,

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

stage “m”) also consists of four 2:1 Muxes namely $F(k, 2m+1)$, $F(k, 2m+2)$ (comprising in combination a forward switch), $UB(k, 2m+1)$, and $UB(k, 2m+2)$ (comprising in combination a U-turn switch). The 2:1 Mux $F(k, 2m+1)$ has two inputs namely $Fi(k, 2m+1)$ and $Fi(k, 2m+2)$ and has one output $Fo(k, 2m+1)$. The 2:1 Mux $F(k, 2m+2)$ has two inputs namely $Fi(k, 2m+1)$ and $Fi(k, 2m+2)$ and has one output $Fo(k, 2m+2)$.

The 2:1 Mux $UB(k, 2m+1)$ has two inputs namely $UBi(k, 2m+1)$ and $UBi(k, 2m+2)$ and has one output $UBo(k, 2m+1)$. The 2:1 Mux $UB(k, 2m+2)$ has two inputs namely $UBi(k, 2m+1)$ and $UBi(k, 2m+2)$ and has one output $UBo(k, 2m+2)$.

However the stage “ $m+1$ ” of ring “k” with “ $m+1$ ” stages of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 2 inputs and 2 outputs as shown in diagram 200D in FIG. 2D. FIG. 2D illustrates a stage (ring “k”, stage “m”) 200D consists of 2 inputs namely $Fi(k, 2m+1)$ and $Fi(k, 2m+2)$; and 2 outputs $Fo(k, 2m+1)$ and $Fo(k, 2m+2)$. The stage (ring “k”, stage “m”) also consists of two 2:1 Muxes namely $F(k, 2m+1)$, $F(k, 2m+2)$ (comprising in combination a forward switch). The 2:1 Mux $F(k, 2m+1)$ has two inputs namely $Fi(k, 2m+1)$ and $Fi(k, 2m+2)$ and has one output $Fo(k, 2m+1)$. The 2:1 Mux $F(k, 2m+2)$ has two inputs namely $Fi(k, 2m+1)$ and $Fi(k, 2m+2)$ and has one output $Fo(k, 2m+2)$. A stage with 2 inputs and 2 outputs is, in one embodiment, the “last stage” or “root stage” of ring.

The stage “m” of ring “k” with “m” stages of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 8 inputs and 4 outputs as shown in diagram 200E in FIG. 2E. FIG. 2E illustrates a stage (ring “k”, stage “m”) 200E consists of 8 inputs namely $EBi(k, 2m+1)$, $EBi(k, 2m+2)$, $UBi(k, 2m+1)$, $UBi(k, 2m+2)$, J, K, L, and M; and 4 outputs $UBo(k, 2m+1)$, $UBo(k, 2m+2)$, $RFo(k, 2m+1)$, and $RFo(k, 2m+2)$. The stage (ring “k”, stage “m”) also consists of eight 2:1 Muxes namely $ER(k, 2m+1)$, $ER(k, 2m+2)$ (comprising in combination a forward switch), $RF(k, 2m+1)$, $RF(k, 2m+2)$ (comprising in combination a Reverse U-turn switch), $BU(k, 2m+1)$, $BU(k, 2m+2)$ (comprising in combination a backward switch), $UB(k, 2m+1)$, and $UB(k, 2m+2)$ (comprising in combination a U-turn switch). The 2:1 Mux $R(k, 2m+1)$ has two

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

inputs namely $F_i(k, 2m+1)$ and J, and has one output $F_o(k, 2m+1)$. The 2:1 Mux $F(k, 2m+2)$ has two inputs namely $F_i(k, 2m+2)$ and K, and has one output $F_o(k, 2m+2)$. The 2:1 Mux $B(k, 2m+1)$ has two inputs namely $F_o(k, 2m+1)$ and $B_i(k, 2m+1)$, and has one output $B_o(k, 2m+1)$. The 2:1 Mux $B(k, 2m+2)$ has two inputs namely $B_o(k, 2m+2)$ and $B_i(k, 2m+1)$, and has one output $B_o(k, 2m+2)$.

The 2:1 Mux $B(k, 2m+1)$ has two inputs namely $B_i(k, 2m+1)$ and L, and has one output $B_o(k, 2m+1)$. The 2:1 Mux $B(k, 2m+2)$ has two inputs namely $B_i(k, 2m+2)$ and M, and has one output $B_o(k, 2m+2)$. The 2:1 Mux $U(k, 2m+1)$ has two inputs namely $B_o(k, 2m+1)$ and $F_o(k, 2m+2)$, and has one output $U_o(k, 2m+1)$. The 2:1 Mux $U(k, 2m+2)$ has two inputs namely $B_o(k, 2m+2)$ and $F_o(k, 2m+1)$, and has one output $U_o(k, 2m+2)$. In different embodiments the inputs J, K, L, and M are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The diagram 200E of FIG 2E eliminates the 180-degree turn paths from the internal connection $F_i(k, 2m+1)$ to the internal connection $U_o(k, 2m+1)$. Similarly the diagram 200E of FIG 2E eliminates the 180-degree turn paths from the connection $F_i(k, 2m+2)$ to the connection $U_o(k, 2m+2)$. The diagram 200E of FIG 2E eliminates the 180-degree turn paths from the internal connection $B_i(k, 2m+1)$ to the internal connection $R_o(k, 2m+1)$. Similarly the diagram 200E of FIG 2E eliminates the 180-degree turn paths from the connection $B_i(k, 2m+2)$ to the connection $R_o(k, 2m+2)$. Hence diagram 200E of FIG. 2E comprises a forward switch, a backward switch, U-turn switch and reverse U-turn switch without 180-degree U-turn paths.

In contrast to diagram 200E of FIG. 2E, the diagram 200A of FIG. 2A, diagram 200B of FIG. 2B, and diagram 200C of FIG. 2C provide 180-degree U-turn paths. Two exemplary 180-degree U-turn paths in diagram 200A of FIG. 2A are shown (by two types of dotted lines) in the attached replacement diagram of FIG. 2A. One of the 180-degree turn path shown in the replacement diagram of FIG. 2A starts at the internal connection $F_i(k, 2m+1)$ through the Mux $F(k, 2m+1)$ to $F_o(k, 2m+1)$ through the Mux $U(k, 2m+1)$ to $U_o(k, 2m+1)$ through the Mux $B(k, 2m+1)$ to the internal connection $B_o(k, 2m+1)$. The second of the 180-degree turn path shown in the replacement diagram of FIG. 2A starts at

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

the hop wire $F_i(k, 2m+2)$ through the Mux $F(k, 2m+2)$ to $F_o(k, 2m+2)$ through the Mux $U(k, 2m+2)$ to $U_o(k, 2m+2)$ through the Mux $B(k, 2m+2)$ to the hop wire $B_o(k, 2m+2)$.

The stage “m” of ring “k” with “m” stages of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 8 inputs and 4 outputs as shown in diagram 200F in FIG. 2F. FIG. 2F illustrates a stage (ring “k”, stage “m”) 200F consists of 8 inputs namely $R_i(k, 2m+1)$, $R_i(k, 2m+2)$, $U_i(k, 2m+1)$, $U_i(k, 2m+2)$, J, K, L, and M; and 4 outputs $B_o(k, 2m+1)$, $B_o(k, 2m+2)$, $F_o(k, 2m+1)$, and $F_o(k, 2m+2)$. The stage (ring “k”, stage “m”) also consists of four 4:1 Muxes namely $F(k, 2m+1)$, $F(k, 2m+2)$, $B(k, 2m+1)$, and $B(k, 2m+2)$. The 4:1 Mux $F(k, 2m+1)$ has four inputs namely $R_i(k, 2m+1)$, $R_i(k, 2m+2)$, $U_i(k, 2m+2)$, and J, and has one output $F_o(k, 2m+1)$. The 4:1 Mux $F(k, 2m+2)$ has four inputs namely $R_i(k, 2m+1)$, $R_i(k, 2m+2)$, $U_i(k, 2m+1)$, and K, and has one output $F_o(k, 2m+2)$.

The 4:1 Mux $B(k, 2m+1)$ has four inputs namely $U_i(k, 2m+1)$, $U_i(k, 2m+2)$, $R_i(k, 2m+2)$, and L, and has one output $B_o(k, 2m+1)$. The 4:1 Mux $B(k, 2m+2)$ has four inputs namely $U_i(k, 2m+1)$, $U_i(k, 2m+2)$, $R_i(k, 2m+1)$ and M, and has one output $B_o(k, 2m+2)$. In different embodiments the inputs J, K, L, and M are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The diagram 200F of FIG 2F eliminates the 180-degree turn paths from the internal connection $R_i(k, 2m+1)$ to the internal connection $B_o(k, 2m+1)$. Similarly the diagram 200F of FIG 2F eliminates the 180-degree turn paths from the connection $R_i(k, 2m+2)$ to the connection $B_o(k, 2m+2)$. The diagram 200F of FIG 2F eliminates the 180-degree turn paths from the internal connection $U_i(k, 2m+1)$ to the internal connection $F_o(k, 2m+1)$. Similarly the diagram 200F of FIG 2F eliminates the 180-degree turn paths from the connection $U_i(k, 2m+2)$ to the connection $F_o(k, 2m+2)$. Hence diagram 200F of FIG. 2F comprises an integrated switch of a backward switch, U-turn switch and reverse U-turn switch without 180-degree U-turn paths.

The number of stages in a ring of any block may not be equal to the number of stages in any other ring of the same of block or any ring of any other block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. For example the number of stages in ring

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

1 of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A or of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B or of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C is denoted by “m” and the number of stages in ring 2 of the partial multi-stage hierarchical network is denoted by “n”, and so “m”
 5 may or may not be equal to “n”. Similarly the number of stages in ring 2 corresponding to block (3,3) of 2D-grid 800 may not be equal to the number of stages in ring 2 corresponding to block (6,9) of 2D-grid 800. Similarly in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C the number of stages in (slice 1, ring 2) corresponding to block (3,3) of 2D-grid 800 may not be equal to the number of stages in
 10 (slice 1, ring 2) corresponding to block (6,9) of 2D-grid 800.

Even though the number of inlet links to the computational block is four and the number of outlet links to the computational block is two in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A, the number of inlet links to the computational block is eight and the number of outlet links to the computational block is
 15 four in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B, and the number of inlet links to the computational block is sixteen and the number of outlet links to the computational block is four in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C, in other embodiments the number of inlet links to the computational block may be any arbitrary number and the number of outlet links to the
 20 computational block may also be another arbitrary number. However the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of inlet links to the computational block divided by $d = 2$ if the inputs and outputs are connected either only from left-hand side or only from right-hand side, if the number of inlet links to the
 25 computational block is greater than or equal to the number of outlet links to the computational block. In such a case one or more of the outlet links to the computational block are connected to more than one inlet links of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to a block. Similarly the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network
 30 $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of inlet links to the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

computational block divided by $2 * d = 4$ if the inputs and outputs are connected from both left-hand side and from right-hand side, if the number of inlet links to the computational block is greater than or equal to the number of outlet links to the computational block.

5 Otherwise the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of outlet links to the computational block divided by $d = 2$ if the inputs and outputs are connected either only from left-hand side or only from right-hand side, if the number of outlet links to the computational block is greater than the number of inlet links
10 to the computational block. In such a case one or more of the outlet links of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to a block are connected to more than one inlet link of the computational block. Similarly the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of outlet links to
15 the computational block divided by $2 * d = 4$ if the inputs and outputs are connected from both left-hand side and from right-hand side, if the number of outlet links to the computational block is greater than or equal to the number of inlet links to the computational block.

In another embodiment, the number of inlet links to the computational block
20 corresponding to a block of 2D-grid of blocks may or may not be equal to the number of inlet links to the computational block corresponding to another block. Similarly the number of outlet links to the computational block corresponding to a block of 2D-grid of blocks may or may not be equal to the number of outlet links to the computational block corresponding to another block. Hence the total number of rings of the partial multi-stage
25 hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to a block of 2D-grid of blocks may or may not be equal to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to another block. For example the total number of rings corresponding to block (4,5) of 2D-grid 800 may be two and the total number of rings in block (5,4) of 2D-grid 800 may be three.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

A multi-stage hierarchical network can be represented with the notation $V_{Comb}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of the complete multi-stage hierarchical network and N_2 represents the total number of outlet links of the complete multi-stage hierarchical network, d represents the number of inlet links of any ring in any block of the complete multi-stage hierarchical network either from only left-hand side or only right-hand side, or equivalently the number of outlet links of any ring in any block of the complete multi-stage hierarchical network either from only left-hand side or only right-hand side, and when the inputs and outputs are connected from left-hand side, s is the ratio of number of outgoing links from each stage 0 of any ring in any block to the number of inlet links of any ring in any block of the complete multi-stage hierarchical network (for example the complete multi-stage hierarchical network corresponding to $V_{Comb}(N_1, N_2, d, s)$ 100A in FIG. 1A, $N_1 = 200$, $N_2 = 400$, $d = 2$, $s = 1$). Also a multi-stage hierarchical network where $N_1 = N_2 = N$ is represented as $V_{Comb}(N, d, s)$.

The diagram 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, and 300E of FIG. 3E are different embodiments of all the connections between two arbitrary successive stages in two different rings of the same block or two different rings of different blocks of 2D-grid 800. Referring to diagram 300A in FIG. 3A illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 4 inputs namely $Ri(x, 2p+1)$, $Ri(x, 2p+2)$, $Ui(x, 2p+1)$, and $Ui(x, 2p+2)$; and 4 outputs $Bo(x, 2p+1)$, $Bo(x, 2p+2)$, $Fo(x, 2p+1)$, and $Fo(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely $R(x, 2p+1)$, $R(x, 2p+2)$, $F(x, 2p+1)$, $F(x, 2p+2)$, $U(x, 2p+1)$, $U(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 2:1 Mux $R(x, 2p+1)$ has two inputs namely $Ri(x, 2p+1)$ and $Bo(x, 2p+1)$ and has one output $Ro(x, 2p+1)$. The 2:1 Mux $R(x, 2p+2)$ has two inputs namely $Ri(x, 2p+2)$ and $Bo(x, 2p+2)$ and has one output $Ro(x, 2p+2)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $Ro(x, 2p+1)$ and $Ro(x, 2p+2)$ and has one output

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+1) and Ro(x,2p+2) and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 4 inputs namely Ri(x,2p+3), Ri(x,2p+4), Ui(x,2p+3), and Ui(x,2p+4); and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of eight 2:1 Muxes namely R(x,2p+3), R(x,2p+4), F(x,2p+3), F(x,2p+4), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The 2:1 Mux R(x,2p+3) has two inputs namely Ri(x,2p+3) and Bo(x,2p+3) and has one output Ro(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs namely Ri(x,2p+4) and Bo(x,2p+4) and has one output Ro(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely Ro(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely Ro(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and Fo(x,2p+3) and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and Fo(x,2p+4) and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Ri(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 4 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), and Ui(y,2q+2); and 4 outputs Bo(y,2q+1), Bo(y,2q+2),

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Fo(y,2q+1), and Fo(y,2q+2). The stage (ring “y”, stage “q”) also consists of eight 2:1 Muxes namely R(y,2q+1), R(y,2q+2), F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and Bo(y,2q+1) and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs
 5 namely Ri(y,2q+2) and Bo(y,2q+2) and has one output Ro(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Ro(y,2q+1) and Ro(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Ro(y,2q+1) and Ro(y,2q+2) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and Fo(y,2q+1) and
 10 has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

15 The stage (ring “y”, stage “q+1”) consists of 4 inputs namely Ri(y,2q+3), Ri(y,2q+4), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring “y”, stage “q+1”) also consists of eight 2:1 Muxes namely R(y,2q+3), R(y,2q+4), F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux R(y,2q+3) has two inputs namely Ri(y,2q+3)
 20 and Bo(y,2q+3) and has one output Ro(y,2q+3). The 2:1 Mux R(y,2q+4) has two inputs namely Ri(y,2q+4) and Bo(y,2q+4) and has one output Ro(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely Ro(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Ro(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+4).

25 The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output
 30 Bo(y,2q+4).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The output $Fo(y,2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $Ri(y,2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $Bo(y,2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $Ui(y,2q+1)$ of the stage (ring “y”, stage “q”).

5 The output $Fo(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire $Hop(1,1)$ to the input $Ri(y,2q+4)$ of the stage (ring “y”, stage “q+1”). The output $Bo(x,2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire $Hop(1,2)$ to the input $Ui(y,2q+2)$ of the stage (ring “y”, stage “q”).

10 The output $Fo(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire $Hop(2,1)$ to the input $Ri(x,2p+4)$ of the stage (ring “x”, stage “p+1”). The output $Bo(y,2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire $Hop(2,2)$ to the input $Ui(x,2p+2)$ of the stage (ring “x”, stage “p”).

15 Ring “x” and ring “y” may or may not belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. If ring “x” and ring “y” belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires $Hop(1,1)$, $Hop(1,2)$, $Hop(2,1)$, and $Hop(2,2)$ are hereinafter called “internal hop wires”. For example if “x = 2” and “y = 3” and both the ring 2 and ring 3 belong to the same block (9,9) of 2D-grid 800, then the wires $Hop(1,1)$, $Hop(1,2)$, $Hop(2,1)$, and $Hop(2,2)$ are “internal hop wires”.

20 If ring “x” and ring “y” belong to the different blocks of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires $Hop(1,1)$, $Hop(1,2)$, $Hop(2,1)$, and $Hop(2,2)$ are hereinafter called “external hop wires”. The external hop wires $Hop(1,1)$, $Hop(1,2)$, $Hop(2,1)$, and $Hop(2,2)$ may be horizontal wires or vertical wires. The length of the external hop wires is manhattan distance between the corresponding
25 blocks, hereinafter “hop length”. For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (1,6) of 2D-grid 800 then the external hop wires are hereinafter called “horizontal external hop wires”. And the hop length of the horizontal hop wires $Hop(1,1)$, $Hop(1,2)$, $Hop(2,1)$, and $Hop(2,2)$ is given by $6 - 1 = 5$. Similarly if ring “x” and ring “y” belong to two blocks in the same horizontal row of 2D-grid 800, then the
30 wires $Hop(1,1)$, $Hop(1,2)$, $Hop(2,1)$, and $Hop(2,2)$ are horizontal external hop wires.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (9,1) of 2D-grid 800 then the external hop wires are hereinafter called “vertical external hop wires”. And the hop length of the vertical hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) is given by $9 - 1 = 8$. Similarly if ring “x” and ring “y” belong to two blocks in the same vertical column of 2D-grid 800, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are vertical external hop wires. External hop wires are typically horizontal or vertical according to the current invention.

Referring to diagram 300B in FIG. 3B illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 8 inputs namely $\mathbb{R}i(x, 2p+1)$, $\mathbb{R}i(x, 2p+2)$, $\mathbb{U}i(x, 2p+1)$, $\mathbb{U}i(x, 2p+2)$, J1, K1, L1, and M1; and 4 outputs $\mathbb{U}o(x, 2p+1)$, $\mathbb{U}o(x, 2p+2)$, $\mathbb{R}o(x, 2p+1)$, and $\mathbb{R}o(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely $\mathbb{R}(x, 2p+1)$, $\mathbb{R}(x, 2p+2)$, $\mathbb{R}^f(x, 2p+1)$, $\mathbb{R}^f(x, 2p+2)$, $\mathbb{U}(x, 2p+1)$, $\mathbb{U}(x, 2p+2)$, $\mathbb{U}^b(x, 2p+1)$, and $\mathbb{U}^b(x, 2p+2)$. The 2:1 Mux $\mathbb{R}(x, 2p+1)$ has two inputs namely $\mathbb{R}i(x, 2p+1)$ and J1, and has one output $\mathbb{R}o(x, 2p+1)$. The 2:1 Mux $\mathbb{R}(x, 2p+2)$ has two inputs namely $\mathbb{R}i(x, 2p+2)$ and K1, and has one output $\mathbb{R}o(x, 2p+2)$. The 2:1 Mux $\mathbb{R}^f(x, 2p+1)$ has two inputs namely $\mathbb{R}o(x, 2p+1)$ and $\mathbb{U}o(x, 2p+2)$, and has one output $\mathbb{R}^fo(x, 2p+1)$. The 2:1 Mux $\mathbb{R}^f(x, 2p+2)$ has two inputs namely $\mathbb{R}o(x, 2p+2)$ and $\mathbb{U}o(x, 2p+1)$, and has one output $\mathbb{R}^fo(x, 2p+2)$.

The 2:1 Mux $\mathbb{U}(x, 2p+1)$ has two inputs namely $\mathbb{U}i(x, 2p+1)$ and L1, and has one output $\mathbb{U}o(x, 2p+1)$. The 2:1 Mux $\mathbb{U}(x, 2p+2)$ has two inputs namely $\mathbb{U}i(x, 2p+2)$ and M1, and has one output $\mathbb{U}o(x, 2p+2)$. The 2:1 Mux $\mathbb{U}^b(x, 2p+1)$ has two inputs namely $\mathbb{U}o(x, 2p+1)$ and $\mathbb{R}o(x, 2p+2)$, and has one output $\mathbb{U}^bo(x, 2p+1)$. The 2:1 Mux $\mathbb{U}^b(x, 2p+2)$ has two inputs namely $\mathbb{U}o(x, 2p+2)$ and $\mathbb{R}o(x, 2p+1)$, and has one output $\mathbb{U}^bo(x, 2p+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The stage (ring “x”, stage “p+1”) consists of 8 inputs namely $\mathbb{E}R_i(x,2p+3)$, $\mathbb{E}R_i(x,2p+4)$, $\mathbb{B}U_i(x,2p+3)$, $\mathbb{B}U_i(x,2p+4)$, J2, K2, L2, and M2; and 4 outputs $\mathbb{U}B_o(x,2p+3)$, $\mathbb{U}B_o(x,2p+4)$, $\mathbb{R}F_o(x,2p+3)$, and $\mathbb{R}F_o(x,2p+4)$. The stage (ring “x”, stage “p+1”) also consists of eight 2:1 Muxes namely $\mathbb{E}R(x,2p+3)$, $\mathbb{E}R(x,2p+4)$, $\mathbb{R}F(x,2p+3)$, $\mathbb{R}F(x,2p+4)$, $\mathbb{B}U(x,2p+3)$, $\mathbb{B}U(x,2p+4)$, $\mathbb{U}B(x,2p+3)$, and $\mathbb{U}B(x,2p+4)$. The 2:1 Mux $\mathbb{E}R(x,2p+3)$ has two inputs namely $\mathbb{E}R_i(x,2p+3)$ and J2, and has one output $\mathbb{E}R_o(x,2p+3)$. The 2:1 Mux $\mathbb{E}R(x,2p+4)$ has two inputs namely $\mathbb{E}R_i(x,2p+4)$ and K2, and has one output $\mathbb{E}R_o(x,2p+4)$. The 2:1 Mux $\mathbb{R}F(x,2p+3)$ has two inputs namely $\mathbb{E}R_o(x,2p+3)$ and $\mathbb{B}U_o(x,2p+4)$, and has one output $\mathbb{R}F_o(x,2p+3)$. The 2:1 Mux $\mathbb{R}F(x,2p+4)$ has two inputs namely $\mathbb{E}R_o(x,2p+4)$ and $\mathbb{B}U_o(x,2p+3)$, and has one output $\mathbb{R}F_o(x,2p+4)$.

The 2:1 Mux $\mathbb{B}U(x,2p+3)$ has two inputs namely $\mathbb{B}U_i(x,2p+3)$ and L2, and has one output $\mathbb{B}U_o(x,2p+3)$. The 2:1 Mux $\mathbb{B}U(x,2p+4)$ has two inputs namely $\mathbb{B}U_i(x,2p+4)$ and M2, and has one output $\mathbb{B}U_o(x,2p+4)$. The 2:1 Mux $\mathbb{U}B(x,2p+3)$ has two inputs namely $\mathbb{B}U_o(x,2p+3)$ and $\mathbb{E}R_o(x,2p+4)$, and has one output $\mathbb{U}B_o(x,2p+3)$. The 2:1 Mux $\mathbb{U}B(x,2p+4)$ has two inputs namely $\mathbb{B}U_o(x,2p+4)$ and $\mathbb{E}R_o(x,2p+3)$, and has one output $\mathbb{U}B_o(x,2p+4)$.

The output $\mathbb{R}F_o(x,2p+1)$ of the stage (ring “x”, stage “p”) is connected to the input $\mathbb{E}R_i(x,2p+3)$ of the stage (ring “x”, stage “p+1”). And the output $\mathbb{U}B_o(x,2p+3)$ of the stage (ring “x”, stage “p+1”) is connected to the input $\mathbb{B}U_i(x,2p+1)$ of the stage (ring “x”, stage “p”).

The stage (ring “y”, stage “q”) consists of 8 inputs namely $\mathbb{E}R_i(y,2q+1)$, $\mathbb{E}R_i(y,2q+2)$, $\mathbb{B}U_i(y,2q+1)$, $\mathbb{B}U_i(y,2q+2)$, J3, K3, L3, and M3; and 4 outputs $\mathbb{U}B_o(y,2q+1)$, $\mathbb{U}B_o(y,2q+2)$, $\mathbb{R}F_o(y,2q+1)$, and $\mathbb{R}F_o(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of eight 2:1 Muxes namely $\mathbb{E}R(y,2q+1)$, $\mathbb{E}R(y,2q+2)$, $\mathbb{R}F(y,2q+1)$, $\mathbb{R}F(y,2q+2)$, $\mathbb{B}U(y,2q+1)$, $\mathbb{B}U(y,2q+2)$, $\mathbb{U}B(y,2q+1)$, and $\mathbb{U}B(y,2q+2)$. The 2:1 Mux $\mathbb{E}R(y,2q+1)$ has two inputs namely $\mathbb{E}R_i(y,2q+1)$ and J3, and has one output $\mathbb{E}R_o(y,2q+1)$. The 2:1 Mux $\mathbb{E}R(y,2q+2)$ has two inputs namely $\mathbb{E}R_i(y,2q+2)$ and K3, and has one output $\mathbb{E}R_o(y,2q+2)$. The 2:1 Mux $\mathbb{R}F(y,2q+1)$ has two inputs namely $\mathbb{E}R_o(y,2q+1)$ and $\mathbb{B}U_o(y,2q+2)$, and has one output $\mathbb{R}F_o(y,2q+1)$. The 2:1

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Mux $R_F(y, 2q+2)$ has two inputs namely $R_o(y, 2q+2)$ and $B_uo(y, 2q+1)$ and has one output $R_Fo(y, 2q+2)$.

The 2:1 Mux $B_U(y, 2q+1)$ has two inputs namely $B_{Ui}(y, 2q+1)$ and L3, and has one output $B_Uo(y, 2q+1)$. The 2:1 Mux $B_U(y, 2q+2)$ has two inputs namely $B_{Ui}(y, 2q+2)$ and M3, and has one output $B_Uo(y, 2q+2)$. The 2:1 Mux $U_B(y, 2q+1)$ has two inputs namely $B_Uo(y, 2q+1)$ and $R_o(y, 2q+2)$, and has one output $U_Bo(y, 2q+1)$. The 2:1 Mux $U_B(y, 2q+2)$ has two inputs namely $B_Uo(y, 2q+2)$ and $R_o(y, 2q+1)$, and has one output $U_Bo(y, 2q+2)$.

The stage (ring “y”, stage “q+1”) consists of 8 inputs namely $R_i(y, 2q+3)$, $R_i(y, 2q+4)$, $B_{Ui}(y, 2q+3)$, $B_{Ui}(y, 2q+4)$, J4, K4, L4, and M4; and 4 outputs $U_Bo(y, 2q+3)$, $U_Bo(y, 2q+4)$, $R_Fo(y, 2q+3)$, and $R_Fo(y, 2q+4)$. The stage (ring “y”, stage “q+1”) also consists of eight 2:1 Muxes namely $R(y, 2q+3)$, $R(y, 2q+4)$, $R_F(y, 2q+3)$, $R_F(y, 2q+4)$, $B_U(y, 2q+3)$, $B_U(y, 2q+4)$, $U_B(y, 2q+3)$, and $U_B(y, 2q+4)$. The 2:1 Mux $R(y, 2q+3)$ has two inputs namely $R_i(y, 2q+3)$ and J4, and has one output $R_o(y, 2q+3)$. The 2:1 Mux $R(y, 2q+4)$ has two inputs namely $R_i(y, 2q+4)$ and K4, and has one output $R_o(y, 2q+4)$. The 2:1 Mux $R_F(y, 2q+3)$ has two inputs namely $R_o(y, 2q+3)$ and $B_Uo(y, 2q+4)$, and has one output $R_Fo(y, 2q+3)$. The 2:1 Mux $R_F(y, 2q+4)$ has two inputs namely $R_o(y, 2q+4)$ and $B_Uo(y, 2q+3)$, and has one output $R_Fo(y, 2q+4)$.

The 2:1 Mux $B_U(y, 2q+3)$ has two inputs namely $B_{Ui}(y, 2q+3)$ and L4, and has one output $B_Uo(y, 2q+3)$. The 2:1 Mux $B_U(y, 2q+4)$ has two inputs namely $B_{Ui}(y, 2q+4)$ and M4, and has one output $B_Uo(y, 2q+4)$. The 2:1 Mux $U_B(y, 2q+3)$ has two inputs namely $B_Uo(y, 2q+3)$ and $R_o(y, 2q+4)$, and has one output $U_Bo(y, 2q+3)$. The 2:1 Mux $U_B(y, 2q+4)$ has two inputs namely $B_Uo(y, 2q+4)$ and $R_o(y, 2q+3)$, and has one output $U_Bo(y, 2q+4)$.

The output $R_Fo(y, 2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $R_i(y, 2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $U_Bo(y, 2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $B_{Ui}(y, 2q+1)$ of the stage (ring “y”, stage “q”).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The output $U_{Fo}(x, 2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input $B_{Ri}(y, 2q+2)$ of the stage (ring “y”, stage “q”). The output $B_{Bo}(y, 2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire Hop(1,2) to the input $F_{Fi}(x, 2p+2)$ of the stage (ring “x”, stage “p”).

5 The output $U_{Fo}(xy, 2pq+4)$ of the stage (ring “xy”, stage “pq”) is connected via the wire Hop(2,1) to the input $B_{Ri}(yx, 2qp+4)$ of the stage (ring “yx”, stage “qp”). The output $B_{Bo}(y, 2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to the input $F_{Fi}(x, 2p+4)$ of the stage (ring “x”, stage “p+1”).

In various embodiments, the inputs J1, K1, L1, and M1 are connected from any of
10 the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J2, K2, L2, and M2 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J3, K3, L3, and M3 are
15 connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Finally the inputs J4, K4, L4, and M4 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Referring to diagram 300C in FIG. 3C, illustrates all the connections between two
20 arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 4 inputs namely $F_i(x, 2p+1)$, $F_i(x, 2p+2)$, $U_i(x, 2p+1)$, and $U_i(x, 2p+2)$; and 4 outputs $B_o(x, 2p+1)$, $B_o(x, 2p+2)$, $F_o(x, 2p+1)$, and
25 $F_o(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of six 2:1 Muxes namely $F(x, 2p+1)$, $F(x, 2p+2)$, $U(x, 2p+1)$, $U(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $F_i(x, 2p+1)$ and $F_i(x, 2p+2)$ and has one output $F_o(x, 2p+1)$. The 2:1 Mux $F(x, 2p+2)$ has two inputs namely $F_i(x, 2p+1)$ and $F_i(x, 2p+2)$ and has one output $F_o(x, 2p+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux $U(x,2p+1)$ has two inputs namely $U_i(x,2p+1)$ and $F_o(x,2p+1)$ and has one output $U_o(x,2p+1)$. The 2:1 Mux $U(x,2p+2)$ has two inputs namely $U_i(x,2p+2)$ and $F_o(x,2p+2)$ and has one output $U_o(x,2p+2)$. The 2:1 Mux $B(x,2p+1)$ has two inputs namely $U_o(x,2p+1)$ and $U_o(x,2p+2)$ and has one output $B_o(x,2p+1)$. The 2:1 Mux
 5 $B(x,2p+2)$ has two inputs namely $U_o(x,2p+1)$ and $U_o(x,2p+2)$ and has one output $B_o(x,2p+2)$.

The stage (ring "x", stage "p+1") consists of 4 inputs namely $F_i(x,2p+3)$, $F_i(x,2p+4)$, $U_i(x,2p+3)$, and $U_i(x,2p+4)$; and 4 outputs $B_o(x,2p+3)$, $B_o(x,2p+4)$, $F_o(x,2p+3)$, and $F_o(x,2p+4)$. The stage (ring "x", stage "p+1") also consists of six 2:1
 10 Muxes namely $F(x,2p+3)$, $F(x,2p+4)$, $U(x,2p+3)$, $U(x,2p+4)$, $B(x,2p+3)$, and $B(x,2p+4)$. The 2:1 Mux $F(x,2p+3)$ has two inputs namely $F_i(x,2p+3)$ and $F_i(x,2p+4)$ and has one output $F_o(x,2p+3)$. The 2:1 Mux $F(x,2p+4)$ has two inputs namely $F_i(x,2p+3)$ and $F_i(x,2p+4)$ and has one output $F_o(x,2p+4)$.

The 2:1 Mux $U(x,2p+3)$ has two inputs namely $U_i(x,2p+3)$ and $F_o(x,2p+3)$ and
 15 has one output $U_o(x,2p+3)$. The 2:1 Mux $U(x,2p+4)$ has two inputs namely $U_i(x,2p+4)$ and $F_o(x,2p+4)$ and has one output $U_o(x,2p+4)$. The 2:1 Mux $B(x,2p+3)$ has two inputs namely $U_o(x,2p+3)$ and $U_o(x,2p+4)$ and has one output $B_o(x,2p+3)$. The 2:1 Mux $B(x,2p+4)$ has two inputs namely $U_o(x,2p+3)$ and $U_o(x,2p+4)$ and has one output $B_o(x,2p+4)$.

20 The output $F_o(x,2p+1)$ of the stage (ring "x", stage "p") is connected to the input $F_i(x,2p+3)$ of the stage (ring "x", stage "p+1"). And the output $B_o(x,2p+3)$ of the stage (ring "x", stage "p+1") is connected to the input $U_i(x,2p+1)$ of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 4 inputs namely $F_i(y,2q+1)$, $F_i(y,2q+2)$,
 25 $U_i(y,2q+1)$, and $U_i(y,2q+2)$; and 4 outputs $B_o(y,2q+1)$, $B_o(y,2q+2)$, $F_o(y,2q+1)$, and $F_o(y,2q+2)$. The stage (ring "y", stage "q") also consists of six 2:1 Muxes namely $F(y,2q+1)$, $F(y,2q+2)$, $U(y,2q+1)$, $U(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The 2:1 Mux $F(y,2q+1)$ has two inputs namely $F_i(y,2q+1)$ and $F_i(y,2q+2)$ and has one output $F_o(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $F_i(y,2q+1)$ and $F_i(y,2q+2)$
 30 and has one output $F_o(y,2q+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux $U(y,2q+1)$ has two inputs namely $U_i(y,2q+1)$ and $F_o(y,2q+1)$ and has one output $U_o(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $U_i(y,2q+2)$ and $F_o(y,2q+2)$ and has one output $U_o(y,2q+2)$. The 2:1 Mux $B(y,2q+1)$ has two inputs namely $U_o(y,2q+1)$ and $U_o(y,2q+2)$ and has one output $B_o(y,2q+1)$. The 2:1 Mux $B(y,2q+2)$ has two inputs namely $U_o(y,2q+1)$ and $U_o(y,2q+2)$ and has one output $B_o(y,2q+2)$.

The stage (ring “y”, stage “q+1”) consists of 4 inputs namely $F_i(y,2q+3)$, $F_i(y,2q+4)$, $U_i(y,2q+3)$, and $U_i(y,2q+4)$; and 4 outputs $B_o(y,2q+3)$, $B_o(y,2q+4)$, $F_o(y,2q+3)$, and $F_o(y,2q+4)$. The stage (ring “y”, stage “q+1”) also consists of six 2:1 Muxes namely $F(y,2q+3)$, $F(y,2q+4)$, $U(y,2q+3)$, $U(y,2q+4)$, $B(y,2q+3)$, and $B(y,2q+4)$. The 2:1 Mux $F(y,2q+3)$ has two inputs namely $F_i(y,2q+3)$ and $F_i(y,2q+4)$ and has one output $F_o(y,2q+3)$. The 2:1 Mux $F(y,2q+4)$ has two inputs namely $F_i(y,2q+3)$ and $F_i(y,2q+4)$ and has one output $F_o(y,2q+4)$.

The 2:1 Mux $U(y,2q+3)$ has two inputs namely $U_i(y,2q+3)$ and $F_o(y,2q+3)$ and has one output $U_o(y,2q+3)$. The 2:1 Mux $U(y,2q+4)$ has two inputs namely $U_i(y,2q+4)$ and $F_o(y,2q+4)$ and has one output $U_o(y,2q+4)$. The 2:1 Mux $B(y,2q+3)$ has two inputs namely $U_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output $B_o(y,2q+3)$. The 2:1 Mux $B(y,2q+4)$ has two inputs namely $U_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output $B_o(y,2q+4)$.

The output $F_o(y,2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $F_i(y,2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $B_o(y,2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $U_i(y,2q+1)$ of the stage (ring “y”, stage “q”).

The output $F_o(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input $F_i(y,2q+4)$ of the stage (ring “y”, stage “q+1”). The output $B_o(x,2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire Hop(1,2) to the input $U_i(y,2q+2)$ of the stage (ring “y”, stage “q”).

The output $F_o(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire Hop(2,1) to the input $F_i(x,2p+4)$ of the stage (ring “x”, stage “p+1”). The output

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$Bo(y,2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to the input $Ui(x,2p+2)$ of the stage (ring “x”, stage “p”).

Referring to diagram 300D in FIG. 3D, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages
 5 (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 4 inputs namely $Fi(x,2p+1)$, $Fi(x,2p+2)$, $Ui(x,2p+1)$, and $Ui(x,2p+2)$; and 4 outputs $Bo(x,2p+1)$, $Bo(x,2p+2)$, $Fo(x,2p+1)$, and
 10 $Fo(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of six 2:1 Muxes namely $F(x,2p+1)$, $F(x,2p+2)$, $U(x,2p+1)$, $U(x,2p+2)$, $B(x,2p+1)$, and $B(x,2p+2)$. The 2:1 Mux $F(x,2p+1)$ has two inputs namely $Fi(x,2p+1)$ and $Fi(x,2p+2)$ and has one output $Fo(x,2p+1)$. The 2:1 Mux $F(x,2p+2)$ has two inputs namely $Fi(x,2p+1)$ and $Fi(x,2p+2)$ and has one output $Fo(x,2p+2)$.

15 The 2:1 Mux $U(x,2p+1)$ has two inputs namely $Ui(x,2p+1)$ and $Fo(x,2p+1)$ and has one output $Uo(x,2p+1)$. The 2:1 Mux $U(x,2p+2)$ has two inputs namely $Ui(x,2p+2)$ and $Fo(x,2p+2)$ and has one output $Uo(x,2p+2)$. The 2:1 Mux $B(x,2p+1)$ has two inputs namely $Uo(x,2p+1)$ and $Uo(x,2p+2)$ and has one output $Bo(x,2p+1)$. The 2:1 Mux $B(x,2p+2)$ has two inputs namely $Uo(x,2p+1)$ and $Uo(x,2p+2)$ and has one output
 20 $Bo(x,2p+2)$.

The stage (ring “x”, stage “p+1”) consists of 2 inputs namely $Fi(x,2p+3)$, $Fi(x,2p+4)$; and 2 outputs $Fo(x,2p+3)$, and $Fo(x,2p+4)$. The stage (ring “x”, stage “p+1”) also consists of two 2:1 Muxes namely $F(x,2p+3)$ and $F(x,2p+4)$. The 2:1 Mux $F(x,2p+3)$ has two inputs namely $Fi(x,2p+3)$ and $Fi(x,2p+4)$ and has one output $Fo(x,2p+3)$. The 2:1
 25 Mux $F(x,2p+4)$ has two inputs namely $Fi(x,2p+3)$ and $Fi(x,2p+4)$ and has one output $Fo(x,2p+4)$.

The output $Fo(x,2p+1)$ of the stage (ring “x”, stage “p”) is connected to the input $Fi(x,2p+3)$ of the stage (ring “x”, stage “p+1”). And the output $Fo(x,2p+3)$ of the stage

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

(ring “x”, stage “p+1”) is connected to the input $U_i(x, 2p+1)$ of the stage (ring “x”, stage “p”).

The stage (ring “y”, stage “q”) consists of 4 inputs namely $F_i(y, 2q+1)$, $F_i(y, 2q+2)$, $U_i(y, 2q+1)$, and $U_i(y, 2q+2)$; and 4 outputs $B_o(y, 2q+1)$, $B_o(y, 2q+2)$, $F_o(y, 2q+1)$, and $F_o(y, 2q+2)$. The stage (ring “y”, stage “q”) also consists of six 2:1 Muxes namely $F(y, 2q+1)$, $F(y, 2q+2)$, $U(y, 2q+1)$, $U(y, 2q+2)$, $B(y, 2q+1)$, and $B(y, 2q+2)$. The 2:1 Mux $F(y, 2q+1)$ has two inputs namely $F_i(y, 2q+1)$ and $F_i(y, 2q+2)$ and has one output $F_o(y, 2q+1)$. The 2:1 Mux $F(y, 2q+2)$ has two inputs namely $F_i(y, 2q+1)$ and $F_i(y, 2q+2)$ and has one output $F_o(y, 2q+2)$.

The 2:1 Mux $U(y, 2q+1)$ has two inputs namely $U_i(y, 2q+1)$ and $F_o(y, 2q+1)$ and has one output $U_o(y, 2q+1)$. The 2:1 Mux $U(y, 2q+2)$ has two inputs namely $U_i(y, 2q+2)$ and $F_o(y, 2q+2)$ and has one output $U_o(y, 2q+2)$. The 2:1 Mux $B(y, 2q+1)$ has two inputs namely $U_o(y, 2q+1)$ and $U_o(y, 2q+2)$ and has one output $B_o(y, 2q+1)$. The 2:1 Mux $B(y, 2q+2)$ has two inputs namely $U_o(y, 2q+1)$ and $U_o(y, 2q+2)$ and has one output $B_o(y, 2q+2)$.

The stage (ring “y”, stage “q+1”) consists of 4 inputs namely $F_i(y, 2q+3)$, $F_i(y, 2q+4)$, $U_i(y, 2q+3)$, and $U_i(y, 2q+4)$; and 4 outputs $B_o(y, 2q+3)$, $B_o(y, 2q+4)$, $F_o(y, 2q+3)$, and $F_o(y, 2q+4)$. The stage (ring “y”, stage “q+1”) also consists of six 2:1 Muxes namely $F(y, 2q+3)$, $F(y, 2q+4)$, $U(y, 2q+3)$, $U(y, 2q+4)$, $B(y, 2q+3)$, and $B(y, 2q+4)$. The 2:1 Mux $F(y, 2q+3)$ has two inputs namely $F_i(y, 2q+3)$ and $F_i(y, 2q+4)$ and has one output $F_o(y, 2q+3)$. The 2:1 Mux $F(y, 2q+4)$ has two inputs namely $F_i(y, 2q+3)$ and $F_i(y, 2q+4)$ and has one output $F_o(y, 2q+4)$.

The 2:1 Mux $U(y, 2q+3)$ has two inputs namely $U_i(y, 2q+3)$ and $F_o(y, 2q+3)$ and has one output $U_o(y, 2q+3)$. The 2:1 Mux $U(y, 2q+4)$ has two inputs namely $U_i(y, 2q+4)$ and $F_o(y, 2q+4)$ and has one output $U_o(y, 2q+4)$. The 2:1 Mux $B(y, 2q+3)$ has two inputs namely $U_o(y, 2q+3)$ and $U_o(y, 2q+4)$ and has one output $B_o(y, 2q+3)$. The 2:1 Mux $B(y, 2q+4)$ has two inputs namely $U_o(y, 2q+3)$ and $U_o(y, 2q+4)$ and has one output $B_o(y, 2q+4)$.

The output $F_o(y, 2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $F_i(y, 2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $B_o(y, 2q+3)$ of the stage

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

(ring “y”, stage “q+1”) is connected to the input $U_i(y,2q+1)$ of the stage (ring “y”, stage “q”).

The output $F_o(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input $F_i(y,2q+4)$ of the stage (ring “y”, stage “q+1”). The output
 5 $F_o(x,2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire Hop(1,2) to the input $U_i(y,2q+2)$ of the stage (ring “y”, stage “q”).

The output $F_o(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire Hop(2,1) to the input $F_i(x,2p+4)$ of the stage (ring “x”, stage “p+1”). The output
 10 $B_o(y,2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to the input $U_i(x,2p+2)$ of the stage (ring “x”, stage “p”).

Referring to diagram 300E in FIG. 3E, illustrates all the connections between root stage of a ring namely the stage (ring “x”, stage “p”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

15 The stage (ring “x”, stage “p”) consists of 4 inputs namely $F_i(x,2p+1)$, $F_i(x,2p+2)$, $U_i(x,2p+1)$, and $U_i(x,2p+2)$; and 4 outputs $B_o(x,2p+1)$, $B_o(x,2p+2)$, $F_o(x,2p+1)$, and $F_o(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of six 2:1 Muxes namely $F(x,2p+1)$, $F(x,2p+2)$, $U(x,2p+1)$, $U(x,2p+2)$, $B(x,2p+1)$, and $B(x,2p+2)$. The 2:1 Mux $F(x,2p+1)$ has two inputs namely $F_i(x,2p+1)$ and $F_i(x,2p+2)$ and has one output
 20 $F_o(x,2p+1)$. The 2:1 Mux $F(x,2p+2)$ has two inputs namely $F_i(x,2p+1)$ and $F_i(x,2p+2)$ and has one output $F_o(x,2p+2)$.

The 2:1 Mux $U(x,2p+1)$ has two inputs namely $U_i(x,2p+1)$ and $F_o(x,2p+1)$ and has one output $U_o(x,2p+1)$. The 2:1 Mux $U(x,2p+2)$ has two inputs namely $U_i(x,2p+2)$ and $F_o(x,2p+2)$ and has one output $U_o(x,2p+2)$. The 2:1 Mux $B(x,2p+1)$ has two inputs
 25 namely $U_o(x,2p+1)$ and $U_o(x,2p+2)$ and has one output $B_o(x,2p+1)$. The 2:1 Mux $B(x,2p+2)$ has two inputs namely $U_o(x,2p+1)$ and $U_o(x,2p+2)$ and has one output $B_o(x,2p+2)$.

The stage (ring “y”, stage “q”) consists of 4 inputs namely $F_i(y,2q+1)$, $F_i(y,2q+2)$, $U_i(y,2q+1)$, and $U_i(y,2q+2)$; and 4 outputs $B_o(y,2q+1)$, $B_o(y,2q+2)$, $F_o(y,2q+1)$, and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Fo(y,2q+2). The stage (ring “y”, stage “q”) also consists of six 2:1 Muxes namely F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and Fo(y,2q+1) and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring “y”, stage “q+1”) consists of 4 inputs namely Fi(y,2q+3), Fi(y,2q+4), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring “y”, stage “q+1”) also consists of six 2:1 Muxes namely F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely Fi(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Fi(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring “y”, stage “q”) is connected to the input Fi(y,2q+3) of the stage (ring “y”, stage “q+1”). And the output Bo(y,2q+3) of the stage (ring “y”, stage “q+1”) is connected to the input Ui(y,2q+1) of the stage (ring “y”, stage “q”).

The output Fo(x,2p+1) of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,2) to the input Ui(y,2q+2) of the stage (ring “y”, stage “q”). The output Fo(x,2p+2)

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input Fi(y,2q+4) of the stage (ring “y”, stage “q+1”).

The output Fo(y,2q+2) of the stage (ring “y”, stage “q”) is connected via the wire Hop(2,1) to the input Ui(x,2p+1) of the stage (ring “x”, stage “p”). The output
5 Bo(y,2q+4) of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to the input Ui(x,2p+2) of the stage (ring “x”, stage “p”).

Just like in diagram 300A of FIG. 3A, in diagram 300B of FIG. 3B, in diagram 300C of FIG. 3C, diagram 300D of FIG. 3D, and in diagram 300E of FIG. 3E, the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are either internal hop wires or horizontal
10 external hop wires or vertical external hop wires (hereinafter alternatively referred to as “cross links” or “cross middle links”).

The diagram 400A of FIG. 4A and 400B of FIG. 4B are different embodiments of all the connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks of 2D-grid 800. Referring to diagram 400A in
15 FIG. 4A illustrates all the connections between an arbitrary stage of a ring namely the stages (ring “x”, stage “p”), and another arbitrary stage of any other ring namely the stages (ring “y”, stage “q”) of the complete multi-stage hierarchical network

$$V_{Comb}(N_1, N_2, d, s).$$

The stage (ring “x”, stage “p”) consists of 8 inputs namely Ri(x,2p+1),
20 Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), J1, K1, L1, and M1; and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and J1 and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two
25 inputs namely Ri(x,2p+2) and K1 and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Uo(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+2) and Uo(x,2p+1) and has one output Fo(x,2p+2).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux $U(x,2p+1)$ has two inputs namely $U_i(x,2p+1)$ and $L1$ and has one output $U_o(x,2p+1)$. The 2:1 Mux $U(x,2p+2)$ has two inputs namely $U_i(x,2p+2)$ and $M1$ and has one output $U_o(x,2p+2)$. The 2:1 Mux $B(x,2p+1)$ has two inputs namely $U_o(x,2p+1)$ and $R_o(x,2p+2)$ and has one output $B_o(x,2p+1)$. The 2:1 Mux $B(x,2p+2)$ has
 5 two inputs namely $U_o(x,2p+2)$ and $R_o(x,2p+1)$ and has one output $B_o(x,2p+2)$.

The stage (ring “y”, stage “q”) consists of 8 inputs namely $R_i(y,2q+1)$, $R_i(y,2q+2)$, $U_i(y,2q+1)$, $U_i(y,2q+2)$, $J3$, $K3$, $L3$, and $M3$; and 4 outputs $B_o(y,2q+1)$, $B_o(y,2q+2)$, $F_o(y,2q+1)$, and $F_o(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of eight 2:1 Muxes namely $R(y,2q+1)$, $R(y,2q+2)$, $F(y,2q+1)$, $F(y,2q+2)$, $U(y,2q+1)$,
 10 $U(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The 2:1 Mux $R(y,2q+1)$ has two inputs namely $R_i(y,2q+1)$ and $J3$ and has one output $R_o(y,2q+1)$. The 2:1 Mux $R(y,2q+2)$ has two inputs namely $R_i(y,2q+2)$ and $K3$ and has one output $R_o(y,2q+2)$. The 2:1 Mux $F(y,2q+1)$ has two inputs namely $R_o(y,2q+1)$ and $U_o(y,2q+2)$ and has one output $F_o(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $R_o(y,2q+2)$ and $U_o(y,2q+1)$
 15 and has one output $F_o(y,2q+2)$.

The 2:1 Mux $U(y,2q+1)$ has two inputs namely $U_i(y,2q+1)$ and $L3$, and has one output $U_o(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $U_i(y,2q+2)$ and $M3$, and has one output $U_o(y,2q+2)$. The 2:1 Mux $B(y,2q+1)$ has two inputs namely $U_o(y,2q+1)$ and $R_o(y,2q+2)$ and has one output $B_o(y,2q+1)$. The 2:1 Mux $B(y,2q+2)$ has
 20 two inputs namely $U_o(y,2q+2)$ and $R_o(y,2q+1)$ and has one output $B_o(y,2q+2)$.

The output $F_o(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire $Hop(1,1)$ to the input $R_i(y,2q+2)$ of the stage (ring “y”, stage “q”). The output $B_o(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire $Hop(1,2)$ to the input $U_i(x,2p+2)$ of the stage (ring “x”, stage “p”).

25 Ring “x” and ring “y” may or may not belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. If ring “x” and ring “y” belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires $Hop(1,1)$ and $Hop(1,2)$ are hereinafter called “internal hop wires”. For example if “x = 2” and “y = 3” and both the ring 2 and ring 3 belong to the same block (9,9) of
 30 2D-grid 800, then the wires $Hop(1,1)$ and $Hop(1,2)$ are “internal hop wires”.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

If ring “x” and ring “y” belong to the different blocks of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1) and Hop(1,2) are hereinafter called “external hop wires”. The external hop wires Hop(1,1) and Hop(1,2) may be horizontal wires or vertical wires. The length of the external hop wires is

5 Manhattan distance between the corresponding blocks, hereinafter “hop length”. For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (1,6) of 2D-grid 800 then the external hop wires are hereinafter called “horizontal external hop wires”. And the hop length of the horizontal hop wires Hop(1,1) and Hop(1,2) is given by $6 - 1 =$

10 5. Similarly if ring “x” and ring “y” belong to two blocks in the same horizontal row of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are horizontal external hop wires.

For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (9,1) of 2D-grid 800 then the external hop wires are hereinafter called “vertical external hop wires”. And the hop length of the vertical hop wires Hop(1,1) and Hop(1,2) is given by $9 - 1 = 8$. Similarly if ring “x” and ring “y” belong to two blocks in the same vertical

15 column of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are vertical external hop wires. External hop wires are typically horizontal or vertical according to the current invention.

Referring to diagram 400B in FIG. 4B illustrates all the connections between an arbitrary stage of a ring namely the stages (ring “x”, stage “p”), and another arbitrary

20 stage of any other ring namely the stages (ring “y”, stage “q”) of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 8 inputs namely $Ri(x, 2p+1)$, $Ri(x, 2p+2)$, $Ui(x, 2p+1)$, $Ui(x, 2p+2)$, J1, K1, L1, and M1; and 4 outputs $Bo(x, 2p+1)$, $Bo(x, 2p+2)$, $Fo(x, 2p+1)$, and $Fo(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of

25 four 4:1 Muxes namely $F(x, 2p+1)$, $F(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 4:1 Mux $F(x, 2p+1)$ has four inputs namely $Ri(x, 2p+1)$, $Ri(x, 2p+2)$, $Ui(x, 2p+2)$, and J1 and has one output $Fo(x, 2p+1)$. The 4:1 Mux $F(x, 2p+2)$ has four inputs namely $Ri(x, 2p+1)$, $Ri(x, 2p+2)$, $Ui(x, 2p+1)$, and K1 and has one output $Fo(x, 2p+2)$.

The 4:1 Mux $B(x, 2p+1)$ has four inputs namely $Ui(x, 2p+1)$, $Ui(x, 2p+2)$,

30 $Ri(x, 2p+2)$, and L1 and has one output $Bo(x, 2p+1)$. The 2:1 Mux $B(x, 2p+2)$ has two

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

inputs namely $U_i(x, 2p+1)$, $U_i(x, 2p+2)$, $R_i(x, 2p+1)$, and $M1$ and has one output $B_o(x, 2p+2)$.

The stage (ring “y”, stage “q”) consists of 8 inputs namely $R_i(y, 2q+1)$, $R_i(y, 2q+2)$, $U_i(y, 2q+1)$, $U_i(y, 2q+2)$, $J3$, $K3$, $L3$, and $M3$; and 4 outputs $B_o(y, 2q+1)$, $B_o(y, 2q+2)$, $F_o(y, 2q+1)$, and $F_o(y, 2q+2)$. The stage (ring “y”, stage “q”) also consists of four 4:1 Muxes namely $F(y, 2q+1)$, $F(y, 2q+2)$, $B(y, 2q+1)$, and $B(y, 2q+2)$. The 4:1 Mux $F(y, 2q+1)$ has four inputs namely $R_i(y, 2q+1)$, $R_i(y, 2q+2)$, $U_i(y, 2q+2)$, and $J3$ and has one output $F_o(y, 2q+1)$. The 4:1 Mux $F(y, 2q+2)$ has four inputs namely $R_i(y, 2q+1)$, $R_i(y, 2q+2)$, $U_i(y, 2q+1)$, and $K3$ and has one output $F_o(y, 2q+2)$.

The 4:1 Mux $B(y, 2q+1)$ has four inputs namely $U_i(y, 2q+1)$, $U_i(y, 2q+2)$, $R_i(y, 2q+2)$, and $L3$, and has one output $B_o(y, 2q+1)$. The 4:1 Mux $B(y, 2q+2)$ has four inputs namely $U_i(y, 2q+1)$, $U_i(y, 2q+2)$, $R_i(y, 2q+1)$, and $M3$, and has one output $B_o(y, 2q+2)$.

The output $F_o(x, 2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire $Hop(1, 1)$ to the input $R_i(y, 2q+2)$ of the stage (ring “y”, stage “q”). The output $B_o(y, 2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire $Hop(1, 2)$ to the input $U_i(x, 2p+2)$ of the stage (ring “x”, stage “p”).

Ring “x” and ring “y” may or may not belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. If ring “x” and ring “y” belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires $Hop(1, 1)$ and $Hop(1, 2)$ are hereinafter called “internal hop wires”. For example if “x = 2” and “y = 3” and both the ring 2 and ring 3 belong to the same block (9,9) of 2D-grid 800, then the wires $Hop(1, 1)$ and $Hop(1, 2)$ are “internal hop wires”.

If ring “x” and ring “y” belong to the different blocks of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires $Hop(1, 1)$ and $Hop(1, 2)$ are hereinafter called “external hop wires”. The external hop wires $Hop(1, 1)$ and $Hop(1, 2)$ may be horizontal wires or vertical wires. The length of the external hop wires is Manhattan distance between the corresponding blocks, hereinafter “hop length”. For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (1,6) of 2D-grid

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

800 then the external hop wires are hereinafter called “horizontal external hop wires”. And the hop length of the horizontal hop wires Hop(1,1) and Hop(1,2) is given by $6 - 1 = 5$. Similarly if ring “x” and ring “y” belong to two blocks in the same horizontal row of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are horizontal external hop wires.

5 For example if ring “x” belongs to block (1,1) and ring “y” belongs to block (9,1) of 2D-grid 800 then the external hop wires are hereinafter called “vertical external hop wires”. And the hop length of the vertical hop wires Hop(1,1) and Hop(1,2) is given by $9 - 1 = 8$. Similarly if ring “x” and ring “y” belong to two blocks in the same vertical column of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are vertical external hop wires. External hop wires are typically horizontal or vertical according to the current
10 invention.

The diagram 500A of FIG. 5A is an embodiment of all the connections with multi-drop hop wires, between two arbitrary successive stages in two different rings of different blocks of 2D-grid 800. Referring to diagram 500A in FIG. 5A illustrates all the
15 connections with multi-drop hop wires, between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. The multi-drop hop wires are also connected to two other stages (ring “a”, stage “s”) and (ring
20 “b”, stage “t”) belonging to a third block.

The stage (ring “x”, stage “p”) consists of 8 inputs namely $R_i(x, 2p+1)$, $R_i(x, 2p+2)$, $U_i(x, 2p+1)$, $U_i(x, 2p+2)$, J1, K1, L1, and M1; and 4 outputs $B_o(x, 2p+1)$, $B_o(x, 2p+2)$, $F_o(x, 2p+1)$, and $F_o(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely $R(x, 2p+1)$, $R(x, 2p+2)$, $F(x, 2p+1)$, $F(x, 2p+2)$, $U(x, 2p+1)$,
25 $U(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 2:1 Mux $R(x, 2p+1)$ has two inputs namely $R_i(x, 2p+1)$ and J1, and has one output $R_o(x, 2p+1)$. The 2:1 Mux $R(x, 2p+2)$ has two inputs namely $R_i(x, 2p+2)$ and K1, and has one output $R_o(x, 2p+2)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $R_o(x, 2p+1)$ and $U_o(x, 2p+2)$, and has one output $F_o(x, 2p+1)$. The 2:1 Mux $F(x, 2p+2)$ has two inputs namely $R_o(x, 2p+2)$ and $U_o(x, 2p+1)$,
30 and has one output $F_o(x, 2p+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux $U(x,2p+1)$ has two inputs namely $U_i(x,2p+1)$ and $L1$, and has one output $U_o(x,2p+1)$. The 2:1 Mux $U(x,2p+2)$ has two inputs namely $U_i(x,2p+2)$ and $M1$, and has one output $U_o(x,2p+2)$. The 2:1 Mux $B(x,2p+1)$ has two inputs namely $U_o(x,2p+1)$ and $R_o(x,2p+2)$, and has one output $B_o(x,2p+1)$. The 2:1 Mux $B(x,2p+2)$ has two inputs namely $U_o(x,2p+2)$ and $R_o(x,2p+1)$, and has one output $B_o(x,2p+2)$.

The stage (ring “x”, stage “p+1”) consists of 8 inputs namely $R_i(x,2p+3)$, $R_i(x,2p+4)$, $U_i(x,2p+3)$, $U_i(x,2p+4)$, $J2$, $K2$, $L2$, and $M2$; and 4 outputs $B_o(x,2p+3)$, $B_o(x,2p+4)$, $F_o(x,2p+3)$, and $F_o(x,2p+4)$. The stage (ring “x”, stage “p+1”) also consists of eight 2:1 Muxes namely $R(x,2p+3)$, $R(x,2p+4)$, $F(x,2p+3)$, $F(x,2p+4)$, $U(x,2p+3)$, $U(x,2p+4)$, $B(x,2p+3)$, and $B(x,2p+4)$. The 2:1 Mux $R(x,2p+3)$ has two inputs namely $R_i(x,2p+3)$ and $J2$, and has one output $R_o(x,2p+3)$. The 2:1 Mux $R(x,2p+4)$ has two inputs namely $R_i(x,2p+4)$ and $K2$, and has one output $R_o(x,2p+4)$. The 2:1 Mux $F(x,2p+3)$ has two inputs namely $R_o(x,2p+3)$ and $U_o(x,2p+4)$, and has one output $F_o(x,2p+3)$. The 2:1 Mux $F(x,2p+4)$ has two inputs namely $R_o(x,2p+4)$ and $U_o(x,2p+3)$, and has one output $F_o(x,2p+4)$.

The 2:1 Mux $U(x,2p+3)$ has two inputs namely $U_i(x,2p+3)$ and $L2$, and has one output $U_o(x,2p+3)$. The 2:1 Mux $U(x,2p+4)$ has two inputs namely $U_i(x,2p+4)$ and $M2$, and has one output $U_o(x,2p+4)$. The 2:1 Mux $B(x,2p+3)$ has two inputs namely $U_o(x,2p+3)$ and $R_o(x,2p+4)$, and has one output $B_o(x,2p+3)$. The 2:1 Mux $B(x,2p+4)$ has two inputs namely $U_o(x,2p+4)$ and $R_o(x,2p+3)$, and has one output $B_o(x,2p+4)$.

The output $F_o(x,2p+1)$ of the stage (ring “x”, stage “p”) is connected to the input $R_i(x,2p+3)$ of the stage (ring “x”, stage “p+1”). And the output $B_o(x,2p+3)$ of the stage (ring “x”, stage “p+1”) is connected to the input $U_i(x,2p+1)$ of the stage (ring “x”, stage “p”).

The stage (ring “y”, stage “q”) consists of 8 inputs namely $R_i(y,2q+1)$, $R_i(y,2q+2)$, $U_i(y,2q+1)$, $U_i(y,2q+2)$, $J3$, $K3$, $L3$, and $M3$; and 4 outputs $B_o(y,2q+1)$, $B_o(y,2q+2)$, $F_o(y,2q+1)$, and $F_o(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of eight 2:1 Muxes namely $R(y,2q+1)$, $R(y,2q+2)$, $F(y,2q+1)$, $F(y,2q+2)$, $U(y,2q+1)$, $U(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The 2:1 Mux $R(y,2q+1)$ has two inputs namely $R_i(y,2q+1)$ and $J3$, and has one output $R_o(y,2q+1)$. The 2:1 Mux $R(y,2q+2)$ has two

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

inputs namely $R_i(y, 2q+2)$ and K_3 , and has one output $R_o(y, 2q+2)$. The 2:1 Mux $F(y, 2q+1)$ has two inputs namely $R_o(y, 2q+1)$ and $U_o(y, 2q+2)$, and has one output $F_o(y, 2q+1)$. The 2:1 Mux $F(y, 2q+2)$ has two inputs namely $R_o(y, 2q+2)$ and $U_o(y, 2q+1)$ and has one output $F_o(y, 2q+2)$.

5 The 2:1 Mux $U(y, 2q+1)$ has two inputs namely $U_i(y, 2q+1)$ and L_3 , and has one output $U_o(y, 2q+1)$. The 2:1 Mux $U(y, 2q+2)$ has two inputs namely $U_i(y, 2q+2)$ and M_3 , and has one output $U_o(y, 2q+2)$. The 2:1 Mux $B(y, 2q+1)$ has two inputs namely $U_o(y, 2q+1)$ and $R_o(y, 2q+2)$, and has one output $B_o(y, 2q+1)$. The 2:1 Mux $B(y, 2q+2)$ has two inputs namely $U_o(y, 2q+2)$ and $R_o(y, 2q+1)$, and has one output $B_o(y, 2q+2)$.

10 The stage (ring “y”, stage “q+1”) consists of 8 inputs namely $R_i(y, 2q+3)$, $R_i(y, 2q+4)$, $U_i(y, 2q+3)$, $U_i(y, 2q+4)$, J_4 , K_4 , L_4 , and M_4 ; and 4 outputs $B_o(y, 2q+3)$, $B_o(y, 2q+4)$, $F_o(y, 2q+3)$, and $F_o(y, 2q+4)$. The stage (ring “y”, stage “q+1”) also consists of eight 2:1 Muxes namely $R(y, 2q+3)$, $R(y, 2q+4)$, $F(y, 2q+3)$, $F(y, 2q+4)$, $U(y, 2q+3)$, $U(y, 2q+4)$, $B(y, 2q+3)$, and $B(y, 2q+4)$. The 2:1 Mux $R(y, 2q+3)$ has two inputs namely
 15 $R_i(y, 2q+3)$ and J_4 , and has one output $R_o(y, 2q+3)$. The 2:1 Mux $R(y, 2q+4)$ has two inputs namely $R_i(y, 2q+4)$ and K_4 , and has one output $R_o(y, 2q+4)$. The 2:1 Mux $F(y, 2q+3)$ has two inputs namely $R_o(y, 2q+3)$ and $U_o(y, 2q+4)$, and has one output $F_o(y, 2q+3)$. The 2:1 Mux $F(y, 2q+4)$ has two inputs namely $R_o(y, 2q+4)$ and $U_o(y, 2q+3)$, and has one output $F_o(y, 2q+4)$.

20 The 2:1 Mux $U(y, 2q+3)$ has two inputs namely $U_i(y, 2q+3)$ and L_4 , and has one output $U_o(y, 2q+3)$. The 2:1 Mux $U(y, 2q+4)$ has two inputs namely $U_i(y, 2q+4)$ and M_4 , and has one output $U_o(y, 2q+4)$. The 2:1 Mux $B(y, 2q+3)$ has two inputs namely $U_o(y, 2q+3)$ and $R_o(y, 2q+4)$, and has one output $B_o(y, 2q+3)$. The 2:1 Mux $B(y, 2q+4)$ has two inputs namely $U_o(y, 2q+4)$ and $R_o(y, 2q+3)$, and has one output $B_o(y, 2q+4)$.

25 The output $F_o(y, 2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $R_i(y, 2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $B_o(y, 2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $U_i(y, 2q+1)$ of the stage (ring “y”, stage “q”).

30 The output $F_o(x, 2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to the input $R_i(y, 2q+4)$ of the stage (ring “y”, stage “q+1”). The output

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Bo(x,2p+4) of the stage (ring “x”, stage “p+1”) is connected via the wire Hop(1,2) to the input Ui(y,2q+2) of the stage (ring “y”, stage “q”).

The output Fo(y,2q+2) of the stage (ring “y”, stage “q”) is connected via the wire Hop(2,1) to the input Ri(x,2p+4) of the stage (ring “x”, stage “p+1”). The output
 5 Bo(y,2q+4) of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to the input Ui(x,2p+2) of the stage (ring “x”, stage “p”).

In various embodiments, the inputs J1, K1, L1, and M1 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J2, K2, L2, and M2 are connected from
 10 any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J3, K3, L3, and M3 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Finally the inputs J4, K4, L4, and M4 are connected from any of the outputs of any other stages of any ring of any block of
 15 the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring “a”, stage “s”) consists of 8 inputs namely Ri(a,2s+1), Ri(a,2s+2), Ui(a,2s+1), Ui(a,2s+2), J5, K5, L5, and M5; and 4 outputs Bo(a,2s+1), Bo(a,2s+2), Fo(a,2s+1), and Fo(a,2s+2). The stage (ring “a”, stage “s”) also consists of eight 2:1
 20 Muxes namely R(a,2s+1), R(a,2s+2), F(a,2s+1), F(a,2s+2), U(a,2s+1), U(a,2s+2), B(a,2s+1), and B(a,2s+2). The 2:1 Mux R(a,2s+1) has two inputs namely Ri(a,2s+1) and J5, and has one output Ro(a,2s+1). The 2:1 Mux R(a,2s+2) has two inputs namely Ri(a,2s+2) and K5, and has one output Ro(a,2s+2). The 2:1 Mux F(a,2s+1) has two inputs namely Ro(a,2s+1) and Uo(a,2s+2), and has one output Fo(a,2s+1). The 2:1 Mux F(a,2s+2) has two inputs namely Ro(a,2s+2) and Uo(a,2s+1), and has one output
 25 Fo(a,2s+2).

The 2:1 Mux U(a,2s+1) has two inputs namely Ui(a,2s+1) and L5, and has one output Uo(a,2s+1). The 2:1 Mux U(a,2s+2) has two inputs namely Ui(a,2s+2) and M5, and has one output Uo(a,2s+2). The 2:1 Mux B(a,2s+1) has two inputs namely

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$Uo(a,2s+1)$ and $Ro(a,2s+2)$, and has one output $Bo(a,2s+1)$. The 2:1 Mux $B(a,2s+2)$ has two inputs namely $Uo(a,2s+2)$ and $Ro(a,2s+1)$, and has one output $Bo(a,2s+2)$.

The stage (ring “b”, stage “t”) consists of 8 inputs namely $Ri(b,2t+1)$, $Ri(b,2t+2)$, $Ui(b,2t+1)$, $Ui(b,2t+2)$, $J6$, $K6$, $L6$, and $M6$; and 4 outputs $Bo(b,2t+1)$, $Bo(b,2t+2)$, $Fo(b,2t+1)$, and $Fo(b,2t+2)$. The stage (ring “b”, stage “t”) also consists of eight 2:1 Muxes namely $R(b,2t+1)$, $R(b,2t+2)$, $F(b,2t+1)$, $F(b,2t+2)$, $U(b,2t+1)$, $U(b,2t+2)$, $B(b,2t+1)$, and $B(b,2t+2)$. The 2:1 Mux $R(b,2t+1)$ has two inputs namely $Ri(b,2t+1)$ and $J6$, and has one output $Ro(b,2t+1)$. The 2:1 Mux $R(b,2t+2)$ has two inputs namely $Ri(b,2t+2)$ and $K6$, and has one output $Ro(b,2t+2)$. The 2:1 Mux $F(b,2t+1)$ has two inputs namely $Ro(b,2t+1)$ and $Uo(b,2t+2)$, and has one output $Fo(b,2t+1)$. The 2:1 Mux $F(b,2t+2)$ has two inputs namely $Ro(b,2t+2)$ and $Uo(b,2t+1)$, and has one output $Fo(b,2t+2)$.

The 2:1 Mux $U(b,2t+1)$ has two inputs namely $Ui(b,2t+1)$ and $L6$, and has one output $Uo(b,2t+1)$. The 2:1 Mux $U(b,2t+2)$ has two inputs namely $Ui(b,2t+2)$ and $M6$, and has one output $Uo(b,2t+2)$. The 2:1 Mux $B(b,2t+1)$ has two inputs namely $Uo(b,2t+1)$ and $Ro(b,2t+2)$, and has one output $Bo(b,2t+1)$. The 2:1 Mux $B(b,2t+2)$ has two inputs namely $Uo(b,2t+2)$ and $Ro(b,2t+1)$, and has one output $Bo(b,2t+2)$.

The wire $Hop(1,1)$ starting from the output $Fo(x,2p+2)$ of the stage (ring “x”, stage “p”) is also connected to $L5$ of the stage (ring “a”, stage “s”), in addition to the input $Ri(y,2q+4)$ of the stage (ring “y”, stage “q+1”). The stage (ring “x”, stage “p”), the stage (ring “a”, stage “s”), and the stage (ring “y”, stage “q+1”) may belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Therefore the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “a”, stage “s”) may not be equal to the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “y”, stage “q+1”). For example the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “a”, stage “s”) may be one where as the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “q”, stage “y+1”) may be two. In such a case the wire $Hop(1,1)$ is called hereinafter a “multi-drop hop wire”. The wire $Hop(1,1)$ may be either horizontal hop wire or vertical hop wire. Also multi-drop hop wires are either horizontal external hop wires or vertical external hop wires. Similarly the hop

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “a”, stage “s”) may be any number greater than or equal to one, and also the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “q”, stage “y+1”) may be any number greater than or equal to one.

5 In general a multi-drop hop wire may be dropping or terminating in more than one different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. For example a multi-drop hop wire starting from one block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ may be terminating at three different blocks or four different blocks, etc.

10 The wire Hop(1,2) starting from the output Bo(x,2p+4) of the stage (ring “x”, stage “p+1”) is also connected to J6 of the stage (ring “b”, stage “t”), in addition to the input Ui(y,2q+2) of the stage (ring “y”, stage “q”). The wire Hop(1,2) is also an example of multi-drop hop wire when the stage (ring “x”, stage “p+1”), the stage (ring “b”, stage “t”) and the stage (ring “y”, stage “q”) belong to three different blocks of the multi-stage
15 hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The wire Hop(2,1) starting from the output Fo(y,2q+2) of the stage (ring “y”, stage “q”) is also connected to M5 of the stage (ring “a”, stage “s”), in addition to the input Ri(x,2p+4) of the stage (ring “x”, stage “p+1”). The wire Hop(2,1) is also an example of multi-drop hop wire when the stage (ring “x”, stage “p+1”), the stage (ring
20 “a”, stage “s”) and the stage (ring “y”, stage “q”) belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The wire Hop(2,2) starting from the output Bo(y,2q+4) of the stage (ring “y”, stage “q+1”) is also connected to K6 of the stage (ring “b”, stage “t”), in addition to the input Ui(x,2p+2) of the stage (ring “x”, stage “p”). The wire Hop(2,2) is also an example
25 of multi-drop hop wire when the stage (ring “x”, stage “p”), the stage (ring “b”, stage “t”) and the stage (ring “y”, stage “q+1”) belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

In various embodiments, the inputs J5, K5, L5, and M5 are connected from any of the multi-drop hop wires starting from any other stages of any ring of any block of the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Also the inputs J6, K6, L6, and M6 are connected from any of the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The diagram 600A of FIG. 6A and 600B of FIG. 6B are different embodiments of
 5 all the connections with multi-drop hop wires, between two arbitrary stages in two different rings of different blocks of 2D-grid 800. Referring to diagram 600A in FIG. 6A illustrates all the connections with multi-drop hop wires, between an arbitrary stage of a ring namely the stages (ring “x”, stage “p”), and another arbitrary stage of any other ring namely the stages (ring “y”, stage “q”) of the complete multi-stage hierarchical network
 10 $V_{Comb}(N_1, N_2, d, s)$. The multi-drop hop wires are also connected to another stage (ring “a”, stage “s”) belonging to a third block.

The stage (ring “x”, stage “p”) consists of 8 inputs namely $R_i(x, 2p+1)$, $R_i(x, 2p+2)$, $U_i(x, 2p+1)$, $U_i(x, 2p+2)$, J1, K1, L1, and M1; and 4 outputs $B_o(x, 2p+1)$, $B_o(x, 2p+2)$, $F_o(x, 2p+1)$, and $F_o(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of
 15 eight 2:1 Muxes namely $R(x, 2p+1)$, $R(x, 2p+2)$, $F(x, 2p+1)$, $F(x, 2p+2)$, $U(x, 2p+1)$, $U(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 2:1 Mux $R(x, 2p+1)$ has two inputs namely $R_i(x, 2p+1)$ and J1 and has one output $R_o(x, 2p+1)$. The 2:1 Mux $R(x, 2p+2)$ has two inputs namely $R_i(x, 2p+2)$ and K1 and has one output $R_o(x, 2p+2)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $R_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output
 20 $F_o(x, 2p+1)$. The 2:1 Mux $F(x, 2p+2)$ has two inputs namely $R_o(x, 2p+2)$ and $U_o(x, 2p+1)$ and has one output $F_o(x, 2p+2)$.

The 2:1 Mux $U(x, 2p+1)$ has two inputs namely $U_i(x, 2p+1)$ and L1 and has one output $U_o(x, 2p+1)$. The 2:1 Mux $U(x, 2p+2)$ has two inputs namely $U_i(x, 2p+2)$ and M1 and has one output $U_o(x, 2p+2)$. The 2:1 Mux $B(x, 2p+1)$ has two inputs namely
 25 $U_o(x, 2p+1)$ and $R_o(x, 2p+2)$ and has one output $B_o(x, 2p+1)$. The 2:1 Mux $B(x, 2p+2)$ has two inputs namely $U_o(x, 2p+2)$ and $R_o(x, 2p+1)$ and has one output $B_o(x, 2p+2)$.

The stage (ring “y”, stage “q”) consists of 8 inputs namely $R_i(y, 2q+1)$, $R_i(y, 2q+2)$, $U_i(y, 2q+1)$, $U_i(y, 2q+2)$, J3, K3, L3, and M3; and 4 outputs $B_o(y, 2q+1)$, $B_o(y, 2q+2)$, $F_o(y, 2q+1)$, and $F_o(y, 2q+2)$. The stage (ring “y”, stage “q”) also consists of
 30 eight 2:1 Muxes namely $R(y, 2q+1)$, $R(y, 2q+2)$, $F(y, 2q+1)$, $F(y, 2q+2)$, $U(y, 2q+1)$,

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and J3 and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Ri(y,2q+2) and K3 and has one output Ro(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Ro(y,2q+1) and Uo(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Ro(y,2q+2) and Uo(y,2q+1) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and L3, and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and M3, and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Ro(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+2) and Ro(y,2q+1) and has one output Bo(y,2q+2).

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Ri(y,2q+2) of the stage (ring "y", stage "q"). The output Bo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(1,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

The wire Hop(1,1) starting from the output Fo(x,2p+2) of the stage (ring "x", stage "p") is also connected to L2 of the stage (ring "a", stage "s"), in addition to the input Ri(y,2q+2) of the stage (ring "y", stage "q"). The stage (ring "x", stage "p"), the stage (ring "a", stage "s"), and the stage (ring "y", stage "q") may belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Therefore the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may not be equal to the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "y", stage "q"). For example the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be one where as the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y") may be two. Hence the wire Hop(1,1) is a multi-drop hop wire. Also the wire Hop(1,1) is either horizontal external hop wire or vertical external hop wire. Similarly the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be any number greater than or equal to one, and also the hop length between the blocks

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

consisting of the stage (ring “x”, stage “p”) and the stage (ring “q”, stage “y”) may be any number greater or equal to one.

The wire Hop(1,2) starting from the output $Bo(y,2q+2)$ of the stage (ring “y”, stage “q”) is also connected to K2 of the stage (ring “a”, stage “s”), in addition to the
 5 input $Ui(x,2p+2)$ of the stage (ring “x”, stage “p”). The wire Hop(1,2) is also an example of multi-drop hop wire when the stage (ring “x”, stage “p”), the stage (ring “a”, stage “s”) and the stage (ring “y”, stage “q”) belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

In various embodiments, the inputs J2, K2, L2, and M2 are connected from any of
 10 the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Referring to diagram 600B in FIG. 6B illustrates all the connections with multi-drop hop wires, between an arbitrary stage of a ring namely the stages (ring “x”, stage “p”), and another arbitrary stage of any other ring namely the stages (ring “y”, stage “q”) of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. The multi-drop hop
 15 wires are also connected to another stage (ring “a”, stage “s”) belonging to a third block.

The stage (ring “x”, stage “p”) consists of 8 inputs namely $Ri(x,2p+1)$, $Ri(x,2p+2)$, $Ui(x,2p+1)$, $Ui(x,2p+2)$, J1, K1, L1, and M1; and 4 outputs $Bo(x,2p+1)$, $Bo(x,2p+2)$, $Fo(x,2p+1)$, and $Fo(x,2p+2)$. The stage (ring “x”, stage “p”) also consists of
 20 four 4:1 Muxes namely $F(x,2p+1)$, $F(x,2p+2)$, $B(x,2p+1)$, and $B(x,2p+2)$. The 4:1 Mux $F(x,2p+1)$ has four inputs namely $Ri(x,2p+1)$, $Ri(x,2p+2)$, $Ui(x,2p+2)$, and J1 and has one output $Fo(x,2p+1)$. The 4:1 Mux $F(x,2p+2)$ has four inputs namely $Ri(x,2p+1)$, $Ri(x,2p+2)$, $Ui(x,2p+1)$, and K1 and has one output $Fo(x,2p+2)$.

The 4:1 Mux $B(x,2p+1)$ has four inputs namely $Ui(x,2p+1)$, $Ui(x,2p+2)$,
 25 $Ri(x,2p+2)$, and L1 and has one output $Bo(x,2p+1)$. The 2:1 Mux $B(x,2p+2)$ has two inputs namely $Ui(x,2p+1)$, $Ui(x,2p+2)$, $Ri(x,2p+1)$, and M1 and has one output $Bo(x,2p+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The stage (ring “y”, stage “q”) consists of 8 inputs namely $Ri(y,2q+1)$, $Ri(y,2q+2)$, $Ui(y,2q+1)$, $Ui(y,2q+2)$, $J3$, $K3$, $L3$, and $M3$; and 4 outputs $Bo(y,2q+1)$, $Bo(y,2q+2)$, $Fo(y,2q+1)$, and $Fo(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of four 4:1 Muxes namely $F(y,2q+1)$, $F(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The 4:1 Mux $F(y,2q+1)$ has four inputs namely $Ri(y,2q+1)$, $Ri(y,2q+2)$, $Ui(y,2q+2)$, and $J3$ and has one output $Fo(y,2q+1)$. The 4:1 Mux $F(y,2q+2)$ has four inputs namely $Ri(y,2q+1)$, $Ri(y,2q+2)$, $Ui(y,2q+1)$, and $K3$ and has one output $Fo(y,2q+2)$.

The 4:1 Mux $B(y,2q+1)$ has four inputs namely $Ui(y,2q+1)$, $Ui(y,2q+2)$, $Ri(y,2q+2)$, and $L3$, and has one output $Bo(y,2q+1)$. The 4:1 Mux $B(y,2q+2)$ has four inputs namely $Ui(y,2q+1)$, $Ui(y,2q+2)$, $Ri(y,2q+1)$, and $M3$, and has one output $Bo(y,2q+2)$.

The output $Fo(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire $Hop(1,1)$ to the input $Ri(y,2q+2)$ of the stage (ring “y”, stage “q”). The output $Bo(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire $Hop(1,2)$ to the input $Ui(x,2p+2)$ of the stage (ring “x”, stage “p”).

The wire $Hop(1,1)$ starting from the output $Fo(x,2p+2)$ of the stage (ring “x”, stage “p”) is also connected to $L2$ and $J2$ of the stage (ring “a”, stage “s”), in addition to the input $Ri(y,2q+2)$ of the stage (ring “y”, stage “q”). The stage (ring “x”, stage “p”), the stage (ring “a”, stage “s”), and the stage (ring “y”, stage “q”) may belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Therefore the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “a”, stage “s”) may not be equal to the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “y”, stage “q”). For example the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “a”, stage “s”) may be one where as the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “q”, stage “y”) may be two. Hence the wire $Hop(1,1)$ is a multi-drop hop wire. Also the wire $Hop(1,1)$ is either horizontal external hop wire or vertical external hop wire. Similarly the hop length between the blocks consisting of the stage (ring “x”, stage “p”) and the stage (ring “a”, stage “s”) may be any number greater than or equal to one, and also the hop length between the blocks

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

consisting of the stage (ring “x”, stage “p”) and the stage (ring “q”, stage “y”) may be any number greater or equal to one.

The wire Hop(1,2) starting from the output Bo(y,2q+2) of the stage (ring “y”, stage “q”) is also connected to K2 and M2 of the stage (ring “a”, stage “s”), in addition to
 5 the input Ui(x,2p+2) of the stage (ring “x”, stage “p”). The wire Hop(1,2) is also an example of multi-drop hop wire when the stage (ring “x”, stage “p”), the stage (ring “a”, stage “s”) and the stage (ring “y”, stage “q”) belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

In various embodiments, the inputs J2, K2, L2, and M2 are connected from any of
 10 the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Referring to diagram 700A in FIG. 7A, illustrates, in one embodiment, the hop wire connections chart of a partial multi-stage hierarchical network
 $V_{Comb}(N_1, N_2, d, s)$ 100A or a partial multi-stage hierarchical network
 15 $V_{Comb}(N_1, N_2, d, s)$ 100B, or a partial multi-stage hierarchical network
 $V_{Comb}(N_1, N_2, d, s)$ 100C, with $m = 6$ and $n = 7$. The hop wire connections chart shows two rings namely ring 1 and ring 2. And there are $m+1 = 7$ stages in ring 1 and $n+1 = 8$ stages in ring 2.

The hop wire connections chart 700A illustrates how the hop wires are connected
 20 between any two successive stages of all the rings corresponding to a block of 2D-grid 800. “Lx” denotes an internal hop wire connection, where symbol “L” denotes internal hop wire and “x” is an integer. For example “L1” between the stages (ring 1, stage 0) and (ring 1, stage 1) denotes that the corresponding hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are connected to two successive stages of another ring in the same block or
 25 alternatively hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are internal hop wires. Since there is also “L1” between the stages (ring 2, stage 0) and (ring 2, stage 1), there are internal hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected between the stages (ring 1, stage 0) and (ring 1, stage 1) and the stages (ring 2,

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

stage 0) and (ring 2, stage 1). Hence there can be only two “L1” labels in the hop wire connection chart 700A.

Similarly there are two “L2” labels in the hop wire connections chart 700A. Since the label “L2” is given between the stages (ring 1, stage 5) and (ring 1, stage 6) and also
 5 the label “L2” is given between the stages (ring 2, stage 3) and (ring 2, stage 4), there are corresponding internal hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected between the stages (ring 1, stage 5) and (ring 1, stage 6) and the stages (ring 2, stage 3) and (ring 2, stage 4).

“V_x” denotes an external vertical hop wire, where symbol “V” denotes vertical
 10 external hop wire connections from blocks of the topmost row of 2D-grid 800 (i.e., row of blocks consisting of block (1,1), block (1,2), ..., and block (1,10)) to the same corresponding stages of the same numbered ring of another block that is directly down south, with “x” vertical hop length, where “x” is a positive integer. For example “V1”
 15 between the stages (ring 1, stage 1) and (ring 1, stage 2) denote that from block (1,1) of 2D-grid 800 to another block directly below it, which is block (2,1), since “V1” denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 1) and (ring 1, stage 2) of block (1,1) to (ring 1, stage 1) and (ring 1, stage 2) of block (2,1). It also means there are external hop wire connections
 20 Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 1) and (ring 1, stage 2) of block (3,1) to (ring 1, stage 1) and (ring 1, stage 2) of block (4,1). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 1) and (ring 1, stage 2) of block (9,1) to (ring 1, stage 1) and (ring 1, stage 2) of block (10,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

25 Similarly “V3” between the stages (ring 2, stage 1) and (ring 2, stage 2) denote that from block (1,1) of 2D-grid 800 to another block below it and at a hop length of 3 which is block (4,1), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 1) and (ring 2, stage 2) of block (1,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (4,1). It also means there are external hop wire
 30 connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 1) and (ring 2, stage 2) of block (2,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (5,1). This

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 1) and (ring 2, stage 2) of block (7,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (10,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

5 If there is no block that is directly below a block with hop length equal to 3 then there is no vertical external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (8,1) does not have any block that is directly below and with hop length equal to 3 then none of the vertical external hop wires are connected from (ring 2, stage 1) and (ring 2, stage 2) of block (8,1). Similarly from
10 (ring 2, stage 1) and (ring 2, stage 2) of block (9,1) and from (ring 2, stage 1) and (ring 2, stage 2) of block (10,1), none of the vertical external hop wires are connected. Similarly vertical external hop wires are connected corresponding to “V5”, “V7” etc., labels given in the hop wire connections chart 700A.

 “U_x” denotes an external vertical hop wire, where symbol “U” denotes vertical
15 external hop wire connections starting from blocks that are “x” hop length below the topmost row of 2D-grid 800 (i.e., row of blocks consisting of block (1+x,1), block (1+x,2), ..., and block (1+x,10)) to the same corresponding stages of the same numbered ring of another block that is directly down below, with “x” vertical hop length, where “x” is a positive integer. For example “U1” between the stages (ring 1, stage 2) and (ring 1,
20 stage 3) denote that from block (2,1) of 2D-grid 800 to another block directly below it, which is block (3,1), since “U1” denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 2) and (ring 1, stage 3) of block (2,1) to (ring 1, stage 2) and (ring 1, stage 3) of block (3,1). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and
25 Hop(2,2) from (ring 1, stage 2) and (ring 1, stage 3) of block (4,1) to (ring 1, stage 2) and (ring 1, stage 3) of block (5,1). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 2) and (ring 1, stage 3) of block (8,1) to (ring 1, stage 2) and (ring 1, stage 3) of block (9,1). The same pattern continues for all the columns starting from the block in the topmost row of
30 each column.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

If there is no block that is directly below a block with hop length equal to 1 then no vertical external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (10,1) does not have any block that is directly below and with hop length equal to 1 then none of the vertical external hop wires are
 5 connected from (ring 1, stage 2) and (ring 1, stage 3) of block (10,1). Similarly for all the blocks in each column from the topmost row up to the row "x", no vertical external hop wires are connected to the corresponding (ring 1, stage 2) and (ring 1, stage 3).

Similarly "U3" between the stages (ring 2, stage 2) and (ring 2, stage 3) denote that starting from blocks that are 3 hop length below the topmost row of 2D-grid 800 (i.e.,
 10 row of blocks consisting of block (4,1), block (4,2), ..., and block (4,10)) to the same corresponding stages of the same numbered ring of another block that is directly down below, with vertical hop length of 3, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected. For example from block (4,1) of 2D-grid 800 to another block below it and at a hop length of 3 which is block (7,1), there are
 15 external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 2) and (ring 2, stage 3) of block (4,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (7,1). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 2) and (ring 2, stage 3) of block (5,1) to (ring 2, stage 2) and (ring 2, stage 3) of block (8,1). This pattern continues and finally there are
 20 external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 2) and (ring 2, stage 3) of block (7,1) to (ring 2, stage 2) and (ring 2, stage 3) of block (10,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

If there is no block that is directly below a block with hop length equal to 3 then
 25 no vertical external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (8,1) does not have any block that is directly below and with hop length equal to 3 then none of the vertical external hop wires are connected from (ring 2, stage 2) and (ring 2, stage 3) of block (8,1). Similarly from (ring 2, stage 2) and (ring 2, stage 3) of block (9,1) and from (ring 2, stage 2) and (ring 2, stage
 30 3) of block (10,1), none of the vertical external hop wires are connected. Similarly

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

vertical external hop wires are connected corresponding to “U5”, “U7” etc. labels given in the hop wire connections chart 700A.

“H_x” denotes an external horizontal hop wire, where symbol “H” denotes horizontal external hop wire connections from blocks of the leftmost column of 2D-grid 800 (i.e., column of blocks consisting of block (1,1), block (2,1), ..., and block (10,1)) to the same corresponding stages of the same numbered ring of another block that is directly to the right, with “x” horizontal hop length, where “x” is a positive integer. For example “H1” between the stages (ring 1, stage 3) and (ring 1, stage 4) denote that from block (1,1) of 2D-grid 800 to another block directly to the right, which is block (1,2), since “H1” denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 3) and (ring 1, stage 4) of block (1,1) to (ring 1, stage 3) and (ring 1, stage 4) of block (1,2). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 3) and (ring 1, stage 4) of block (1,3) to (ring 1, stage 3) and (ring 1, stage 4) of block (1,4). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 3) and (ring 1, stage 4) of block (9,1) to (ring 1, stage 3) and (ring 1, stage 4) of block (10,1). The same pattern continues for all the rows starting from the block in the leftmost block of each row.

Similarly “H3” between the stages (ring 2, stage 4) and (ring 2, stage 5) denote that from block (1,1) of 2D-grid 800 to another block to the right and at a hop length of 3 which is block (1,4), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 4) and (ring 2, stage 5) of block (1,1) to (ring 2, stage 4) and (ring 2, stage 5) of block (1,4). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 4) and (ring 2, stage 5) of block (1,2) to (ring 2, stage 4) and (ring 2, stage 5) of block (1,5). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 4) and (ring 2, stage 5) of block (1,7) to (ring 2, stage 4) and (ring 2, stage 5) of block (1,10). The same pattern continues for all the columns starting from the block in the leftmost column of each row.

If there is no block that is directly to the right with hop length equal to 3 then there is no horizontal external hop wire connections is given corresponding to those two

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

successive stages of the blocks. For example block (1,8) does not have any block that is directly to the right and with hop length equal to 3 then none of the horizontal external hop wires are connected from (ring 2, stage 4) and (ring 2, stage 5) of block (1,8).

Similarly from (ring 2, stage 4) and (ring 2, stage 5) of block (1,9) and from (ring 2, stage 4) and (ring 2, stage 5) of block (1,10), none of the horizontal external hop wires are connected. Similarly horizontal external hop wires are connected corresponding to "H5", "H7" etc., labels given in the hop wire connections chart 700A.

"Kx" denotes an external horizontal hop wire, where symbol "K" denotes horizontal external hop wire connections starting from blocks that are "x" hop length below the leftmost column of 2D-grid 800 (i.e., column of blocks consisting of block (1, 1+x), block (2, 1+x), ..., and block (10, 1+x)) to the same corresponding stages of the same numbered ring of another block that is directly to the right, with "x" horizontal hop length, where "x" is a positive integer. For example "K1" between the stages (ring 1, stage 4) and (ring 1, stage 5) denote that from block (1,2) of 2D-grid 800 to another block directly to the right, which is block (1,3), since "K1" denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 4) and (ring 1, stage 5) of block (1,2) to (ring 1, stage 4) and (ring 1, stage 5) of block (1,3). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 4) and (ring 1, stage 4) of block (1,4) to (ring 1, stage 4) and (ring 1, stage 5) of block (1,5). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 4) and (ring 1, stage 5) of block (1,8) to (ring 1, stage 4) and (ring 1, stage 5) of block (1,9). The same pattern continues for all the rows starting from the block in the leftmost column of each row.

If there is no block that is directly to the right of a block with hop length equal to 1 then no horizontal external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (1,10) does not have any block that is directly to the right and with hop length equal to 1 then none of the horizontal external hop wires are connected from (ring 1, stage 4) and (ring 1, stage 5) of block (1,10). Similarly for all the blocks in each row from the leftmost column up to the column "x",

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

no horizontal external hop wires are connected to the corresponding (ring 1, stage 4) and (ring 1, stage 5).

Similarly “K3” between the stages (ring 2, stage 5) and (ring 2, stage 6) denote that starting from blocks that are 3 hop length to the right of the leftmost column of 2D-
5 grid 800 (i.e., column of blocks consisting of block (1,4), block (2,4), . . . , and block (10,4)) to the same corresponding stages of the same numbered ring of another block that is directly to the right, with horizontal hop length of 3, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected. For example from
10 block (1,4) of 2D-grid 800 to another block to the right and at a hop length of 3 which is block (1,7), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 5) and (ring 2, stage 6) of block (1,4) to (ring 2, stage 5) and (ring 2, stage 6) of block (1,7). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 5) and (ring 2, stage 6) of
15 block (1,5) to (ring 2, stage 5) and (ring 2, stage 6) of block (1,8). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 5) and (ring 2, stage 6) of block (1,7) to (ring 2, stage 5) and (ring 2, stage 6) of block (1,10). The same pattern continues for all the rows starting from the block in the leftmost block of each row.

If there is no block that is directly to the right of a block with hop length equal to
20 3 then no horizontal external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (1,8) does not have any block that is directly to the right and with hop length equal to 3 then none of the horizontal external hop wires are connected from (ring 2, stage 5) and (ring 2, stage 6) of block (1,8). Similarly from (ring 2, stage 5) and (ring 2, stage 6) of block (1,9) and from (ring 2, stage
25 5) and (ring 2, stage 6) of block (1,10), none of the horizontal external hop wires are connected. Similarly horizontal external hop wires are connected corresponding to “K5”, “K7” etc. labels given in the hop wire connections chart 700A.

In general the hop length of an external vertical hop wire can be any positive number. Similarly the hop length of an external horizontal hop wire can be any positive
30 number. The hop wire connections between two arbitrary successive stages in two different rings of the same block or two different rings of different blocks described in

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, and 300E of FIG. 3E. Similarly the multi-drop hop wire connections between two arbitrary successive stages in two different rings of different blocks described in diagram 700A of FIG. 7A
5 may be any one of the embodiments of either the diagrams 500A of FIG. 5A.

In accordance with the invention, the hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may also be any one of the embodiments of either the diagrams 400A of FIG. 4A and 400B of FIG. 4B. Similarly the multi-drop hop wire connections between two arbitrary
10 stages in two different rings of different blocks may also be any one of the embodiments of either the diagrams 600A of FIG. 6A or 600B of FIG. 6B.

In accordance with the current invention, either partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A of FIG. 1A or partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B of FIG. 1B, or partial multi-stage hierarchical network
15 $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C, corresponding to a block of 2D-grid of blocks 800 of FIG. 8, using any one of the embodiments of 200A-200E of FIGs. 2A-2E to implement a stage of a ring of the multi-stage hierarchical network, either by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks described in
20 diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, 300E of FIG. 3E, 500A of FIG. 5A, or by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may be any one of the embodiments of either the
25 diagrams 400A of FIG. 4A, 400B of FIG. 4B, 600A of FIG. 6A, or 600B of FIG. 6B is very efficient in the reduction of the die size, power consumption, and for lower wire/path delay for higher performance for practical routing applications to particularly to set up broadcast, unicast and multicast connections. In general in accordance with the current invention, where N_1 and N_2 of the complete multi-stage hierarchical network

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$V_{Comb}(N_1, N_2, d, s)$ may be arbitrarily large in size and also the 2D-grid size 800 may also be arbitrarily large in size in terms of both the number of rows and number of columns.

Delay Optimizations in Multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$:

5 The multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ according to the current invention can further be optimized to reduce the delay in the routed path of the connection. The delay optimized multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ is hereinafter denoted by $V_{D-Comb}(N_1, N_2, d, s)$. The delay optimizing embodiments of the stages of a ring are one of the diagrams namely 900A-900E of FIGs. 9A-9D, 1000A-1000F of FIGs. 10A-10F, and 1100A-1100C of FIGs. 11A-11C. The diagram 1200 of
10 FIG. 12, 1300 of FIG. 13, 1400 of FIG. 14, and 1500 of FIG. 15 are different embodiments for the implementation of delay optimizations with all the connections between two arbitrary successive stages in two different rings of the same block or two different rings of different blocks of 2D-grid 800.

15 FIG. 9A illustrates a stage (ring "k", stage "m") 900A consists of 5 inputs namely $F_i(k, 2m+1)$, $F_i(k, 2m+2)$, $YF_i(k, 2m+1)$, $U_i(k, 2m+1)$, and $U_i(k, 2m+2)$; and 4 outputs $B_o(k, 2m+1)$, $B_o(k, 2m+2)$, $F_o(k, 2m+1)$, and $F_o(k, 2m+2)$. The stage (ring "k", stage "m") also consists of seven 2:1 Muxes namely $YF(k, 2m+1)$, $F(k, 2m+1)$, $F(k, 2m+2)$, $U(k, 2m+1)$, $U(k, 2m+2)$, $B(k, 2m+1)$, and $B(k, 2m+2)$. The 2:1 Mux $YF(k, 2m+1)$ has two
20 inputs namely $F_i(k, 2m+1)$ and $YF_i(k, 2m+1)$ and has one output $YF_o(k, 2m+1)$. The 2:1 Mux $F(k, 2m+1)$ has two inputs namely $YF_o(k, 2m+1)$ and $F_i(k, 2m+2)$ and has one output $F_o(k, 2m+1)$. The 2:1 Mux $F(k, 2m+2)$ has two inputs namely $YF_o(k, 2m+1)$ and $F_i(k, 2m+2)$ and has one output $F_o(k, 2m+2)$.

 The 2:1 Mux $U(k, 2m+1)$ has two inputs namely $U_i(k, 2m+1)$ and $F_o(k, 2m+1)$ and
25 has one output $U_o(k, 2m+1)$. The 2:1 Mux $U(k, 2m+2)$ has two inputs namely $U_i(k, 2m+2)$ and $F_o(k, 2m+2)$ and has one output $U_o(k, 2m+2)$. The 2:1 Mux $B(k, 2m+1)$ has two inputs namely $U_o(k, 2m+1)$ and $U_o(k, 2m+2)$ and has one output $B_o(k, 2m+1)$. The 2:1 Mux $B(k, 2m+2)$ has two inputs namely $U_o(k, 2m+1)$ and $U_o(k, 2m+2)$ and has one output $B_o(k, 2m+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

FIG. 9B illustrates a stage (ring “k”, stage “m”) 900B consists of 5 inputs namely $F_i(k,2m+1)$, $F_i(k,2m+2)$, $YU_i(k,2m+1)$, $U_i(k,2m+1)$, and $U_i(k,2m+2)$; and 4 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of seven 2:1 Muxes namely $F(k,2m+1)$, $F(k,2m+2)$, $YF(k,2m+1)$,
 5 $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $Fo(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $Fo(k,2m+2)$.

The 2:1 Mux $YU(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $YU_i(k,2m+1)$
 10 and has one output $YUo(k,2m+1)$. The 2:1 Mux $U(k,2m+1)$ has two inputs namely $YUo(k,2m+1)$ and $Fo(k,2m+1)$ and has one output $Uo(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $Fo(k,2m+2)$ and has one output $Uo(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $Uo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output $Bo(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $Uo(k,2m+1)$ and
 15 $Uo(k,2m+2)$ and has one output $Bo(k,2m+2)$.

FIG. 9C illustrates a stage (ring “k”, stage “m”) 900C consists of 5 inputs namely $F_i(k,2m+1)$, $F_i(k,2m+2)$, $UY_i(k,2m+1)$, $U_i(k,2m+1)$, and $U_i(k,2m+2)$; and 4 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of five 2:1 Muxes namely $F(k,2m+1)$, $F(k,2m+2)$, $U(k,2m+2)$, $B(k,2m+1)$,
 20 and $B(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of one 3:1 Mux namely $UY(k,2m+1)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $Fo(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $F_i(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $Fo(k,2m+2)$.

The 3:1 Mux $UY(k,2m+1)$ has three inputs namely $U_i(k,2m+1)$, $UY_i(k,2m+1)$
 25 and $Fo(k,2m+1)$ and has one output $UYo(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $Fo(k,2m+2)$ and has one output $Uo(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $UYo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output $Bo(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $UYo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output $Bo(k,2m+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

FIG. 9D illustrates a stage (ring “k”, stage “m”) 900D consists of 6 inputs namely $F_i(k,2m+1)$, $F_i(k,2m+2)$, $YF_i(k,2m+1)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $YU_i(k,2m+1)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of eight 2:1 Muxes namely $F(k,2m+1)$, $F(k,2m+2)$, $YF(k,2m+1)$,
 5 $U(k,2m+1)$, $U(k,2m+2)$, $YU(k,2m+1)$, $B(k,2m+1)$, and $B(k,2m+2)$. The 2:1 Mux $YF(k,2m+1)$ has two inputs namely $F_i(k,2m+1)$ and $YF_i(k,2m+1)$ and has one output $YF_o(k,2m+1)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $YF_o(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $YF_o(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+2)$.

10 The 2:1 Mux $YU(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $YU_i(k,2m+1)$ and has one output $YU_o(k,2m+1)$. The 2:1 Mux $U(k,2m+1)$ has two inputs namely $YU_o(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one
 15 output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

FIG. 9E illustrates a stage (ring “k”, stage “m”) 900E consists of 6 inputs namely $F_i(k,2m+1)$, $F_i(k,2m+2)$, $YF_i(k,2m+1)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $UY_i(k,2m+1)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of six 2:1 Muxes namely $F(k,2m+1)$, $F(k,2m+2)$, $YF(k,2m+1)$,
 20 $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of one 3:1 Mux namely $UY(k,2m+1)$. The 2:1 Mux $YF(k,2m+1)$ has two inputs namely $F_i(k,2m+1)$ and $YF_i(k,2m+1)$ and has one output $YF_o(k,2m+1)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $YF_o(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+1)$.
 25 The 2:1 Mux $F(k,2m+2)$ has two inputs namely $YF_o(k,2m+1)$ and $F_i(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 3:1 Mux $UY(k,2m+1)$ has three inputs namely $U_i(k,2m+1)$, $UY_i(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $UY_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1
 30 Mux $B(k,2m+1)$ has two inputs namely $UY_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

output $Bo(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $UYo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output $Bo(k,2m+2)$.

FIG. 10A illustrates a stage (ring “k”, stage “m”) 1000A consists of 5 inputs namely $Ri(k,2m+1)$, $Ri(k,2m+2)$, $YRi(k,2m+1)$, $Ui(k,2m+1)$, and $Ui(k,2m+2)$; and 4
 5 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of nine 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $YR(k,2m+1)$, $F(k,2m+1)$, $F(k,2m+2)$, $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The 2:1 Mux $YR(k,2m+1)$ has two inputs namely $Ri(k,2m+1)$ and $YRi(k,2m+1)$ and has one output $YRo(k,2m+1)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $YRo(k,2m+1)$ and
 10 $Bo(k,2m+1)$ and has one output $Ro(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $Ri(k,2m+2)$ and $Bo(k,2m+2)$ and has one output $Ro(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $Ro(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $Ro(k,2m+1)$ and
 $Ro(k,2m+2)$ and has one output $Fo(k,2m+2)$.

15 The 2:1 Mux $U(k,2m+1)$ has two inputs namely $Ui(k,2m+1)$ and $Fo(k,2m+1)$ and has one output $Uo(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $Ui(k,2m+2)$ and $Fo(k,2m+2)$ and has one output $Uo(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $Uo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output $Bo(k,2m+1)$. The 2:1 Mux
 $B(k,2m+2)$ has two inputs namely $Uo(k,2m+1)$ and $Uo(k,2m+2)$ and has one output
 20 $Bo(k,2m+2)$.

FIG. 10B illustrates a stage (ring “k”, stage “m”) 1000B consists of 5 inputs namely $Ri(k,2m+1)$, $Ri(k,2m+2)$, $RYi(k,2m+1)$, $Ui(k,2m+1)$, and $Ui(k,2m+2)$; and 4
 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of seven 2:1 Muxes namely $R(k,2m+2)$, $F(k,2m+1)$, $F(k,2m+2)$,
 25 $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of one 3:1 Mux namely $RY(k,2m+1)$. The 3:1 Mux $RY(k,2m+1)$ has three inputs namely $Ri(k,2m+1)$, $RYi(k,2m+1)$, and $Bo(k,2m+1)$, and has one output $RYo(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $Ri(k,2m+2)$ and $Bo(k,2m+2)$ and has one output $Ro(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $RYo(k,2m+1)$ and
 30 $Ro(k,2m+2)$ and has one output $Fo(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $RYo(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux $U(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux
 5 $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

FIG. 10C illustrates a stage (ring “k”, stage “m”) 1000C consists of 5 inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $YU_i(k,2m+1)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring “k”,
 10 stage “m”) also consists of nine 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$, $F(k,2m+2)$, $YU(k,2m+1)$, $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $R_i(k,2m+1)$ and $B_o(k,2m+1)$ and has one output $R_o(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and $B_o(k,2m+2)$ and has one output $R_o(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs
 15 namely $R_o(k,2m+1)$ and $R_o(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $R_o(k,2m+1)$ and $R_o(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 2:1 Mux $YU(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $YU_i(k,2m+1)$ and has one output $YU_o(k,2m+1)$. The 2:1 Mux $U(k,2m+1)$ has two inputs namely
 20 $YU_o(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

FIG. 10D illustrates a stage (ring “k”, stage “m”) 1000D consists of 5 inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $UY_i(k,2m+1)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring “k”,
 25 stage “m”) also consists of seven 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$, $F(k,2m+2)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The stage (ring “k”, stage “m”) also
 30 consists of one 3:1 Mux namely $UY(k,2m+1)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $R_i(k,2m+1)$ and $B_o(k,2m+1)$ and has one output $R_o(k,2m+1)$. The 2:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and $B_o(k,2m+2)$ and has one output $R_o(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $R_o(k,2m+1)$ and $R_o(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $R_o(k,2m+1)$ and $R_o(k,2m+2)$ and has one output $F_o(k,2m+2)$.

5 The 3:1 Mux $UY(k,2m+1)$ has three inputs namely $U_i(k,2m+1)$, $UY_i(k,2m+1)$, and $F_o(k,2m+1)$, and has one output $UY_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $UY_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $UY_o(k,2m+1)$ and
10 $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

FIG. 10E illustrates a stage (ring "k", stage "m") 1000E consists of 6 inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $YR_i(k,2m+1)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $YU_i(k,2m+1)$; and 4 outputs $B_o(k,2m+1)$, $B_o(k,2m+2)$, $F_o(k,2m+1)$, and $F_o(k,2m+2)$. The stage (ring "k", stage "m") also consists of ten 2:1 Muxes namely $YR(k,2m+1)$,
15 $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$, $F(k,2m+2)$, $YU(k,2m+1)$, $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The 2:1 Mux $YR(k,2m+1)$ has two inputs namely $R_i(k,2m+1)$ and $YR_i(k,2m+1)$ and has one output $YR_o(k,2m+1)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $YR_o(k,2m+1)$ and $B_o(k,2m+1)$ and has one output $R_o(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and
20 $B_o(k,2m+2)$ and has one output $R_o(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $R_o(k,2m+1)$ and $R_o(k,2m+2)$ and has one output $F_o(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $R_o(k,2m+1)$ and $R_o(k,2m+2)$ and has one output $F_o(k,2m+2)$.

The 2:1 Mux $YU(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $YU_i(k,2m+1)$
25 and has one output $YU_o(k,2m+1)$. The 2:1 Mux $U(k,2m+1)$ has two inputs namely $YU_o(k,2m+1)$ and $F_o(k,2m+1)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $F_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $B_o(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and
30 $U_o(k,2m+2)$ and has one output $B_o(k,2m+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

FIG. 10F illustrates a stage (ring “k”, stage “m”) 1000F consists of 6 inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $RY_i(k,2m+1)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $UY_i(k,2m+1)$; and 4 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of six 2:1 Muxes namely $R(k,2m+2)$, $F(k,2m+1)$, $F(k,2m+2)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of two 3:1 Mux namely $RY(k,2m+1)$ and $UY(k,2m+1)$. The 3:1 Mux $RY(k,2m+1)$ has three inputs namely $R_i(k,2m+1)$, $RY_i(k,2m+1)$, and $Bo(k,2m+1)$ and has one output $RY_o(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and $Bo(k,2m+2)$ and has one output $Ro(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $RY_o(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs namely $RY_o(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+2)$.

The 3:1 Mux $UY(k,2m+1)$ has three inputs namely $U_i(k,2m+1)$, $UY_i(k,2m+1)$, and $Fo(k,2m+1)$, and has one output $UY_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $Fo(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $UY_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $Bo(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $UY_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $Bo(k,2m+2)$.

FIG. 11A illustrates a stage (ring “k”, stage “m”) 1100A consists of 5 inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $FY_i(k,2m+2)$, $U_i(k,2m+1)$, and $U_i(k,2m+2)$; and 4 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of seven 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$, $U(k,2m+1)$, $U(k,2m+2)$, $B(k,2m+1)$, and $B(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of one 3:1 Mux namely $FY(k,2m+2)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $R_i(k,2m+1)$ and $Bo(k,2m+1)$ and has one output $Ro(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and $Bo(k,2m+2)$ and has one output $Ro(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $Ro(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+1)$. The 3:1 Mux $FY(k,2m+2)$ has three inputs namely $Ro(k,2m+1)$, $Ro(k,2m+2)$, and $FY_i(k,2m+2)$, and has one output $FY_o(k,2m+2)$.

The 2:1 Mux $U(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $Fo(k,2m+1)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

and $FY_o(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $Bo(k,2m+1)$. The 2:1 Mux $B(k,2m+2)$ has two inputs namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $Bo(k,2m+2)$.

5 FIG. 11B illustrates a stage (ring “k”, stage “m”) 1100B consists of 5 inputs namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $BY_i(k,2m+2)$; and 4 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of seven 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$, $F(k,2m+2)$, $U(k,2m+1)$, $U(k,2m+2)$, and $B(k,2m+1)$. The stage (ring “k”, stage “m”) also consists of one 3:1 Mux namely $BY(k,2m+2)$. The 2:1 Mux $R(k,2m+1)$ has two inputs
10 namely $R_i(k,2m+1)$ and $Bo(k,2m+1)$ and has one output $Ro(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and $Bo(k,2m+2)$ and has one output $Ro(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $Ro(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+1)$. The 2:1 Mux $F(k,2m+2)$ has two inputs
15 namely $Ro(k,2m+1)$, and $Ro(k,2m+2)$, and has one output $Fo(k,2m+2)$.

The 2:1 Mux $U(k,2m+1)$ has two inputs namely $U_i(k,2m+1)$ and $Fo(k,2m+1)$ and has one output $U_o(k,2m+1)$. The 2:1 Mux $U(k,2m+2)$ has two inputs namely $U_i(k,2m+2)$ and $Fo(k,2m+2)$ and has one output $U_o(k,2m+2)$. The 2:1 Mux $B(k,2m+1)$ has two inputs
20 namely $U_o(k,2m+1)$ and $U_o(k,2m+2)$ and has one output $Bo(k,2m+1)$. The 3:1 Mux $BY(k,2m+2)$ has three inputs namely $U_o(k,2m+1)$, $U_o(k,2m+2)$, and $BY_i(k,2m+2)$, and has one output $BY_o(k,2m+2)$.

FIG. 11C illustrates a stage (ring “k”, stage “m”) 1100C consists of 6 inputs
25 namely $R_i(k,2m+1)$, $R_i(k,2m+2)$, $FY_i(k,2m+2)$, $U_i(k,2m+1)$, $U_i(k,2m+2)$, and $BY_i(k,2m+2)$; and 4 outputs $Bo(k,2m+1)$, $Bo(k,2m+2)$, $Fo(k,2m+1)$, and $Fo(k,2m+2)$. The stage (ring “k”, stage “m”) also consists of six 2:1 Muxes namely $R(k,2m+1)$, $R(k,2m+2)$, $F(k,2m+1)$, $U(k,2m+1)$, $U(k,2m+2)$, and $B(k,2m+1)$. The stage (ring “k”, stage “m”) also consists of two 3:1 Muxes namely $FY(k,2m+2)$ and $BY(k,2m+2)$. The 2:1 Mux $R(k,2m+1)$ has two inputs namely $R_i(k,2m+1)$ and $Bo(k,2m+1)$ and has one output
30 $Ro(k,2m+1)$. The 2:1 Mux $R(k,2m+2)$ has two inputs namely $R_i(k,2m+2)$ and $Bo(k,2m+2)$ and has one output $Ro(k,2m+2)$. The 2:1 Mux $F(k,2m+1)$ has two inputs namely $Ro(k,2m+1)$ and $Ro(k,2m+2)$ and has one output $Fo(k,2m+1)$. The 3:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

FY(k,2m+2) has three inputs namely Ro(k,2m+1), Ro(k,2m+2), and FYi(k,2m+2), and has one output FYo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and FYo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 3:1 Mux BY(k,2m+2) has three inputs namely Uo(k,2m+1), Uo(k,2m+2), and BYi(k,2m+2) and has one output BYo(k,2m+2).

Referring to diagram 1200 in FIG. 12, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 5 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), and UYi(x,2p+1); and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring “x”, stage “p”) also consists of seven 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The stage (ring “x”, stage “p”) also consists of one 3:1 Mux namely UY(x,2p+1). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and Bo(x,2p+1) and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and Bo(x,2p+2) and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Ro(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+1) and Ro(x,2p+2) and has one output Fo(x,2p+2).

The 3:1 Mux UY(x,2p+1) has three inputs namely Ui(x,2p+1), UYi(x,2p+1), and Fo(x,2p+1), and has one output UYo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely UYo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely UYo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+2).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The stage (ring “x”, stage “p+1”) consists of 5 inputs namely $R_i(x,2p+3)$, $R_i(x,2p+4)$, $RY_i(x,2p+3)$, $U_i(x,2p+3)$, and $U_i(x,2p+4)$; and 4 outputs $Bo(x,2p+3)$, $Bo(x,2p+4)$, $Fo(x,2p+3)$, and $Fo(x,2p+4)$. The stage (ring “x”, stage “p+1”) also consists of seven 2:1 Muxes namely $R(x,2p+4)$, $F(x,2p+3)$, $F(x,2p+4)$, $U(x,2p+3)$, $U(x,2p+4)$, $B(x,2p+3)$, and $B(x,2p+4)$. The stage (ring “x”, stage “p+1”) also consists of one 3:1 Mux namely $RY(x,2p+3)$. The 3:1 Mux $RY(x,2p+3)$ has three inputs namely $R_i(x,2p+3)$, $RY_i(x,2p+3)$, and $Bo(x,2p+3)$, and has one output $RY_o(x,2p+3)$. The 2:1 Mux $R(x,2p+4)$ has two inputs namely $R_i(x,2p+4)$ and $Bo(x,2p+4)$ and has one output $Ro(x,2p+4)$. The 2:1 Mux $F(x,2p+3)$ has two inputs namely $RY_o(x,2p+3)$ and $Ro(x,2p+4)$ and has one output $Fo(x,2p+3)$. The 2:1 Mux $F(x,2p+4)$ has two inputs namely $RY_o(x,2p+3)$ and $Ro(x,2p+4)$ and has one output $Fo(x,2p+4)$.

The 2:1 Mux $U(x,2p+3)$ has two inputs namely $U_i(x,2p+3)$ and $Fo(x,2p+3)$ and has one output $U_o(x,2p+3)$. The 2:1 Mux $U(x,2p+4)$ has two inputs namely $U_i(x,2p+4)$ and $Fo(x,2p+4)$ and has one output $U_o(x,2p+4)$. The 2:1 Mux $B(x,2p+3)$ has two inputs namely $U_o(x,2p+3)$ and $U_o(x,2p+4)$ and has one output $Bo(x,2p+3)$. The 2:1 Mux $B(x,2p+4)$ has two inputs namely $U_o(x,2p+3)$ and $U_o(x,2p+4)$ and has one output $Bo(x,2p+4)$.

The output $Fo(x,2p+1)$ of the stage (ring “x”, stage “p”) is connected to the input $R_i(x,2p+3)$ of the stage (ring “x”, stage “p+1”). And the output $Bo(x,2p+3)$ of the stage (ring “x”, stage “p+1”) is connected to the input $U_i(x,2p+1)$ of the stage (ring “x”, stage “p”).

The stage (ring “y”, stage “q”) consists of 5 inputs namely $R_i(y,2q+1)$, $R_i(y,2q+2)$, $U_i(y,2q+1)$, $U_i(y,2q+2)$, and $YU_i(y,2q+1)$; and 4 outputs $Bo(y,2q+1)$, $Bo(y,2q+2)$, $Fo(y,2q+1)$, and $Fo(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of nine 2:1 Muxes namely $R(y,2q+1)$, $R(y,2q+2)$, $F(y,2q+1)$, $F(y,2q+2)$, $YU(y,2q+1)$, $U(y,2q+1)$, $U(y,2q+2)$, $B(y,2q+1)$, and $B(y,2q+2)$. The 2:1 Mux $R(y,2q+1)$ has two inputs namely $R_i(y,2q+1)$ and $Bo(y,2q+1)$ and has one output $Ro(y,2q+1)$. The 2:1 Mux $R(y,2q+2)$ has two inputs namely $R_i(y,2q+2)$ and $Bo(y,2q+2)$ and has one output $Ro(y,2q+2)$. The 2:1 Mux $F(y,2q+1)$ has two inputs namely $Ro(y,2q+1)$ and $Ro(y,2q+2)$ and has one output $Fo(y,2q+1)$. The 2:1 Mux $F(y,2q+2)$ has two inputs namely $Ro(y,2q+1)$ and $Ro(y,2q+2)$ and has one output $Fo(y,2q+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux $YU(y,2q+1)$ has two inputs namely $U_i(y,2q+1)$ and $YU_i(y,2q+1)$ and has one output $YU_o(y,2q+1)$. The 2:1 Mux $U(y,2q+1)$ has two inputs namely $YU_o(y,2q+1)$ and $F_o(y,2q+1)$ and has one output $U_o(y,2q+1)$. The 2:1 Mux $U(y,2q+2)$ has two inputs namely $U_i(y,2q+2)$ and $F_o(y,2q+2)$ and has one output $U_o(y,2q+2)$. The
 5 2:1 Mux $B(y,2q+1)$ has two inputs namely $U_o(y,2q+1)$ and $U_o(y,2q+2)$ and has one output $B_o(y,2q+1)$. The 2:1 Mux $B(y,2q+2)$ has two inputs namely $U_o(y,2q+1)$ and $U_o(y,2q+2)$ and has one output $B_o(y,2q+2)$.

The stage (ring "y", stage "q+1") consists of 5 inputs namely $R_i(y,2q+3)$, $R_i(y,2q+4)$, $YR_i(y,2q+3)$, $U_i(y,2q+3)$, and $U_i(y,2q+4)$; and 4 outputs $B_o(y,2q+3)$,
 10 $B_o(y,2q+4)$, $F_o(y,2q+3)$, and $F_o(y,2q+4)$. The stage (ring "y", stage "q+1") also consists of nine 2:1 Muxes namely $R(y,2q+3)$, $R(y,2q+4)$, $YR(y,2q+3)$, $F(y,2q+3)$, $F(y,2q+4)$, $U(y,2q+3)$, $U(y,2q+4)$, $B(y,2q+3)$, and $B(y,2q+4)$. The 2:1 Mux $YR(y,2q+3)$ has two inputs namely $R_i(y,2q+3)$ and $YR_i(y,2q+3)$ and has one output $YR_o(y,2q+3)$. The 2:1 Mux $R(y,2q+3)$ has two inputs namely $YR_o(y,2q+3)$ and $B_o(y,2q+3)$ and has one output
 15 $R_o(y,2q+3)$. The 2:1 Mux $R(y,2q+4)$ has two inputs namely $R_i(y,2q+4)$ and $B_o(y,2q+4)$ and has one output $R_o(y,2q+4)$. The 2:1 Mux $F(y,2q+3)$ has two inputs namely $R_o(y,2q+3)$ and $R_o(y,2q+4)$ and has one output $F_o(y,2q+3)$. The 2:1 Mux $F(y,2q+4)$ has two inputs namely $R_o(y,2q+3)$ and $R_o(y,2q+4)$ and has one output $F_o(y,2q+4)$.

The 2:1 Mux $U(y,2q+3)$ has two inputs namely $U_i(y,2q+3)$ and $F_o(y,2q+3)$ and
 20 has one output $U_o(y,2q+3)$. The 2:1 Mux $U(y,2q+4)$ has two inputs namely $U_i(y,2q+4)$ and $F_o(y,2q+4)$ and has one output $U_o(y,2q+4)$. The 2:1 Mux $B(y,2q+3)$ has two inputs namely $U_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output $B_o(y,2q+3)$. The 2:1 Mux $B(y,2q+4)$ has two inputs namely $U_o(y,2q+3)$ and $U_o(y,2q+4)$ and has one output $B_o(y,2q+4)$.

25 The output $F_o(y,2q+1)$ of the stage (ring "y", stage "q") is connected to the input $R_i(y,2q+3)$ of the stage (ring "y", stage "q+1"). And the output $B_o(y,2q+3)$ of the stage (ring "y", stage "q+1") is connected to the input $U_i(y,2q+1)$ of the stage (ring "y", stage "q").

The output $F_o(x,2p+2)$ of the stage (ring "x", stage "p") is connected via the wire
 30 Hop(1,1) to two inputs namely input $R_i(y,2q+4)$ of the stage (ring "y", stage "q+1") and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

input $YU_i(y, 2q+1)$ of the stage (ring “y”, stage “q”). The output $Bo(x, 2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire $Hop(1,2)$ to two inputs namely input $U_i(y, 2q+2)$ of the stage (ring “y”, stage “q”) and input $YR_i(y, 2q+3)$ of the stage (ring “y”, stage “q+1”).

5 The output $Fo(y, 2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire $Hop(2,1)$ to two inputs namely input $R_i(x, 2p+4)$ of the stage (ring “x”, stage “p+1”) and input $UY_i(x, 2p+1)$ of the stage (ring “x”, stage “p”). The output $Bo(y, 2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire $Hop(2,2)$ to two inputs namely input $U_i(x, 2p+2)$ of the stage (ring “x”, stage “p”) and input $RY_i(x, 2p+3)$ of the stage (ring “x”,
10 stage “p+1”).

Referring to diagram 1300 in FIG. 13, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical
15 network $V_{D-Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 6 inputs namely $Fi(x, 2p+1)$, $Fi(x, 2p+2)$, $YFi(x, 2p+1)$, $U_i(x, 2p+1)$, $U_i(x, 2p+2)$, and $YU_i(x, 2p+1)$; and 4 outputs $Bo(x, 2p+1)$, $Bo(x, 2p+2)$, $Fo(x, 2p+1)$, and $Fo(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of eight 2:1 Muxes namely $F(x, 2p+1)$, $F(x, 2p+2)$, $YF(x, 2p+1)$, $U(x, 2p+1)$, $U(x, 2p+2)$,
20 $YU(x, 2p+1)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 2:1 Mux $YF(x, 2p+1)$ has two inputs namely $Fi(x, 2p+1)$ and $YFi(x, 2p+1)$ and has one output $YFo(x, 2p+1)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $YFo(x, 2p+1)$ and $Fi(x, 2p+2)$ and has one output $Fo(x, 2p+1)$. The 2:1 Mux $F(x, 2p+2)$ has two inputs namely $YFo(x, 2p+1)$ and $Fi(x, 2p+2)$ and has one output $Fo(x, 2p+2)$.

25 The 2:1 Mux $YU(x, 2p+1)$ has two inputs namely $U_i(x, 2p+1)$ and $YU_i(x, 2p+1)$ and has one output $YUo(x, 2p+1)$. The 2:1 Mux $U(x, 2p+1)$ has two inputs namely $YUo(x, 2p+1)$ and $Fo(x, 2p+1)$ and has one output $Uo(x, 2p+1)$. The 2:1 Mux $U(x, 2p+2)$ has two inputs namely $U_i(x, 2p+2)$ and $Fo(x, 2p+2)$ and has one output $Uo(x, 2p+2)$. The 2:1 Mux $B(x, 2p+1)$ has two inputs namely $Uo(x, 2p+1)$ and $Uo(x, 2p+2)$ and has one

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

output $Bo(x,2p+1)$. The 2:1 Mux $B(x,2p+2)$ has two inputs namely $Uo(x,2p+1)$ and $Uo(x,2p+2)$ and has one output $Bo(x,2p+2)$.

The stage (ring “x”, stage “p+1”) consists of 6 inputs namely $Ri(x,2p+3)$, $Ri(x,2p+4)$, $YRi(x,2p+3)$, $Ui(x,2p+3)$, $Ui(x,2p+4)$, and $YUi(x,2p+3)$; and 4 outputs
 5 $Bo(x,2p+3)$, $Bo(x,2p+4)$, $Fo(x,2p+3)$, and $Fo(x,2p+4)$. The stage (ring “x”, stage “p+1”) also consists of ten 2:1 Muxes namely $YR(x,2p+3)$, $R(x,2p+3)$, $R(x,2p+4)$, $F(x,2p+3)$, $F(x,2p+4)$, $YU(x,2p+3)$, $U(x,2p+3)$, $U(x,2p+4)$, $B(x,2p+3)$, and $B(x,2p+4)$. The 2:1 Mux $YR(x,2p+3)$ has two inputs namely $Ri(x,2p+3)$ and $YRi(x,2p+3)$ and has one output $YRo(x,2p+3)$. The 2:1 Mux $R(x,2p+3)$ has two inputs namely $YRo(x,2p+3)$ and
 10 $Bo(x,2p+3)$ and has one output $Ro(x,2p+3)$. The 2:1 Mux $R(x,2p+4)$ has two inputs namely $Ri(x,2p+4)$ and $Bo(x,2p+4)$ and has one output $Ro(x,2p+4)$. The 2:1 Mux $F(x,2p+3)$ has two inputs namely $Ro(x,2p+3)$ and $Ro(x,2p+4)$ and has one output $Fo(x,2p+3)$. The 2:1 Mux $F(x,2p+4)$ has two inputs namely $Ro(x,2p+3)$ and $Ro(x,2p+4)$ and has one output $Fo(x,2p+4)$.

15 The 2:1 Mux $YU(x,2p+3)$ has two inputs namely $Ui(x,2p+3)$ and $YUi(x,2p+3)$ and has one output $YUo(x,2p+3)$. The 2:1 Mux $U(x,2p+3)$ has two inputs namely $YUo(x,2p+3)$ and $Fo(x,2p+3)$ and has one output $Uo(x,2p+3)$. The 2:1 Mux $U(x,2p+4)$ has two inputs namely $Ui(x,2p+4)$ and $Fo(x,2p+4)$ and has one output $Uo(x,2p+4)$. The 2:1 Mux $B(x,2p+3)$ has two inputs namely $Uo(x,2p+3)$ and $Uo(x,2p+4)$ and has one
 20 output $Bo(x,2p+3)$. The 2:1 Mux $B(x,2p+4)$ has two inputs namely $Uo(x,2p+3)$ and $Uo(x,2p+4)$ and has one output $Bo(x,2p+4)$.

The output $Fo(x,2p+1)$ of the stage (ring “x”, stage “p”) is connected to the input $Ri(x,2p+3)$ of the stage (ring “x”, stage “p+1”). And the output $Bo(x,2p+3)$ of the stage (ring “x”, stage “p+1”) is connected to the input $Ui(x,2p+1)$ of the stage (ring “x”, stage
 25 “p”).

The stage (ring “y”, stage “q”) consists of 6 inputs namely $Fi(y,2q+1)$, $Fi(y,2q+2)$, $YFi(y,2q+1)$, $Ui(y,2q+1)$, $Ui(y,2q+2)$, and $YUi(y,2q+1)$; and 4 outputs $Bo(y,2q+1)$, $Bo(y,2q+2)$, $Fo(y,2q+1)$, and $Fo(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of six 2:1 Muxes namely $F(y,2q+1)$, $F(y,2q+2)$, $YF(y,2q+1)$, $U(y,2q+2)$, $B(y,2q+1)$, and
 30 $B(y,2q+2)$. The stage (ring “y”, stage “q”) also consists of one 3:1 Mux namely

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

UY(y,2q+1). The 2:1 Mux YF(y,2q+1) has two inputs namely Fi(y,2q+1) and YFi(y,2q+1) and has one output YFo(y,2q+1). The 2:1 Mux F(y,2q+1) has two inputs namely YFo(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely YFo(y,2q+1) and Fi(y,2q+2) and has one output
5 Fo(y,2q+2).

The 3:1 Mux UY(y,2q+1) has three inputs namely Ui(y,2q+1), UYi(y,2q+1) and Fo(y,2q+1) and has one output UYo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely UYo(y,2q+1) and Uo(y,2q+2) and has one output
10 Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely UYo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring “y”, stage “q+1”) consists of 6 inputs namely Ri(y,2q+3), Ri(y,2q+4), RYi(y,2q+3), Ui(y,2q+3), Ui(y,2q+4), and UYi(y,2q+3); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring “y”, stage “2q+1”) also consists of six 2:1 Muxes namely R(y,2q+4), F(y,2q+3), F(y,2q+4), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The stage (ring “y”, stage “2q+1”) also consists of two 3:1 Mux namely RY(y,2q+3) and UY(y,2q+3). The 3:1 Mux RY(y,2q+3) has three inputs namely Ri(y,2q+3), RYi(y,2q+3), and Bo(y,2q+3) and has one output RYo(y,2q+3). The 2:1 Mux R(y,2q+4) has two inputs namely Ri(y,2q+4) and Bo(y,2q+4) and has one
20 output Ro(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely RYo(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely RYo(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+4).

The 3:1 Mux UY(y,2q+3) has three inputs namely Ui(y,2q+3), UYi(y,2q+3), and Fo(y,2q+3), and has one output UYo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs
25 namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely UYo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely UYo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring “y”, stage “q”) is connected to the input
30 Ri(y,2q+3) of the stage (ring “y”, stage “q+1”). And the output Bo(y,2q+3) of the stage

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

(ring “y”, stage “q+1”) is connected to the input $U_i(y, 2q+1)$ of the stage (ring “y”, stage “q”).

The output $F_o(x, 2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to two inputs namely input $R_i(y, 2q+4)$ of the stage (ring “y”, stage “q+1”) and
 5 input $YU_i(y, 2q+1)$ of the stage (ring “y”, stage “q”). The output $B_o(x, 2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire Hop(1,2) to two inputs namely input $U_i(y, 2q+2)$ of the stage (ring “y”, stage “q”) and input $RY_i(y, 2q+3)$ of the stage (ring “y”, stage “q+1”).

The output $F_o(y, 2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire
 10 Hop(2,1) to two inputs namely input $R_i(x, 2p+4)$ of the stage (ring “x”, stage “p+1”) and input $YU_i(x, 2p+1)$ of the stage (ring “x”, stage “p”). The output $B_o(y, 2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to two inputs namely input $U_i(x, 2p+2)$ of the stage (ring “x”, stage “p”) and input $YR_i(x, 2p+3)$ of the stage (ring “x”, stage “p+1”).

15 Referring to diagram 1400 in FIG. 14, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

20 The stage (ring “x”, stage “p”) consists of 5 inputs namely $F_i(x, 2p+1)$, $F_i(x, 2p+2)$, $YU_i(x, 2p+1)$, $U_i(x, 2p+1)$, and $U_i(x, 2p+2)$; and 4 outputs $B_o(x, 2p+1)$, $B_o(x, 2p+2)$, $F_o(x, 2p+1)$, and $F_o(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of seven 2:1 Muxes namely $F(x, 2p+1)$, $F(x, 2p+2)$, $YF(x, 2p+1)$, $U(x, 2p+1)$, $U(x, 2p+2)$, $B(x, 2p+1)$, and $B(x, 2p+2)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $F_i(x, 2p+1)$ and $F_i(x, 2p+2)$ and
 25 has one output $F_o(x, 2p+1)$. The 2:1 Mux $F(x, 2p+2)$ has two inputs namely $F_i(x, 2p+1)$ and $F_i(x, 2p+2)$ and has one output $F_o(x, 2p+2)$.

The 2:1 Mux $YU(x, 2p+1)$ has two inputs namely $U_i(x, 2p+1)$ and $YU_i(x, 2p+1)$ and has one output $YU_o(x, 2p+1)$. The 2:1 Mux $U(x, 2p+1)$ has two inputs namely $YU_o(x, 2p+1)$ and $F_o(x, 2p+1)$ and has one output $U_o(x, 2p+1)$. The 2:1 Mux $U(x, 2p+2)$

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

has two inputs namely $U_i(x, 2p+2)$ and $F_o(x, 2p+2)$ and has one output $U_o(x, 2p+2)$. The 2:1 Mux $B(x, 2p+1)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $B_o(x, 2p+1)$. The 2:1 Mux $B(x, 2p+2)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $B_o(x, 2p+2)$.

5 The stage (ring "x", stage "p+1") consists of 5 inputs namely $F_i(x, 2p+3)$, $F_i(x, 2p+4)$, $YF_i(x, 2p+3)$, $U_i(x, 2p+3)$, and $U_i(x, 2p+4)$; and 4 outputs $B_o(x, 2p+3)$, $B_o(x, 2p+4)$, $F_o(x, 2p+3)$, and $F_o(x, 2p+4)$. The stage (ring "x", stage "p+1") also consists of seven 2:1 Muxes namely $YF(x, 2p+3)$, $F(x, 2p+3)$, $F(x, 2p+4)$, $U(x, 2p+3)$, $U(x, 2p+4)$, $B(x, 2p+3)$, and $B(x, 2p+4)$. The 2:1 Mux $YF(x, 2p+3)$ has two inputs namely $F_i(x, 2p+3)$ and $YF_i(x, 2p+3)$ and has one output $YF_o(x, 2p+3)$. The 2:1 Mux $F(x, 2p+3)$ has two inputs namely $YF_o(x, 2p+3)$ and $F_i(x, 2p+4)$ and has one output $F_o(x, 2p+3)$. The 2:1 Mux $F(x, 2p+4)$ has two inputs namely $YF_o(x, 2p+3)$ and $F_i(x, 2p+4)$ and has one output $F_o(x, 2p+4)$.

15 The 2:1 Mux $U(x, 2p+3)$ has two inputs namely $U_i(x, 2p+3)$ and $F_o(x, 2p+3)$ and has one output $U_o(x, 2p+3)$. The 2:1 Mux $U(x, 2p+4)$ has two inputs namely $U_i(x, 2p+4)$ and $F_o(x, 2p+4)$ and has one output $U_o(x, 2p+4)$. The 2:1 Mux $B(x, 2p+3)$ has two inputs namely $U_o(x, 2p+3)$ and $U_o(x, 2p+4)$ and has one output $B_o(x, 2p+3)$. The 2:1 Mux $B(x, 2p+4)$ has two inputs namely $U_o(x, 2p+3)$ and $U_o(x, 2p+4)$ and has one output $B_o(x, 2p+4)$.

20 The output $F_o(x, 2p+1)$ of the stage (ring "x", stage "p") is connected to the input $F_i(x, 2p+3)$ of the stage (ring "x", stage "p+1"). And the output $B_o(x, 2p+3)$ of the stage (ring "x", stage "p+1") is connected to the input $U_i(x, 2p+1)$ of the stage (ring "x", stage "p").

25 The stage (ring "y", stage "q") consists of 5 inputs namely $F_i(y, 2q+1)$, $F_i(y, 2q+2)$, $UY_i(y, 2q+1)$, $U_i(y, 2q+1)$, and $U_i(y, 2q+2)$; and 4 outputs $B_o(y, 2q+1)$, $B_o(y, 2q+2)$, $F_o(y, 2q+1)$, and $F_o(y, 2q+2)$. The stage (ring "y", stage "q") also consists of five 2:1 Muxes namely $F(y, 2q+1)$, $F(y, 2q+2)$, $U(y, 2q+2)$, $B(y, 2q+1)$, and $B(y, 2q+2)$. The stage (ring "y", stage "q") also consists of one 3:1 Mux namely $UY(y, 2q+1)$. The 2:1 Mux $F(y, 2q+1)$ has two inputs namely $F_i(y, 2q+1)$ and $F_i(y, 2q+2)$ and has one output

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+2).

The 3:1 Mux UY(y,2q+1) has three inputs namely Ui(y,2q+1), UYi(y,2q+1) and Fo(y,2q+1) and has one output UYo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs
 5 namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely UYo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely UYo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 5 inputs namely Fi(y,2q+3),
 10 Fi(y,2q+4), YFi(y,2q+3), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of seven 2:1 Muxes namely YF(y,2q+3), F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux YF(y,2q+3) has two inputs namely Fi(y,2q+3) and YFi(y,2q+3) and has one output YFo(y,2q+3). The 2:1 Mux F(y,2q+3) has two inputs
 15 namely YFo(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely YFo(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4)
 20 and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input
 25 Fi(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to two inputs namely input Fi(y,2q+4) of the stage (ring "y", stage "q+1") and
 30 input UYi(y,2q+1) of the stage (ring "y", stage "q"). The output Bo(x,2p+4) of the stage

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

(ring “x”, stage “p+1”) is connected via the wire Hop(1,2) to two inputs namely input $U_i(y, 2q+2)$ of the stage (ring “y”, stage “q”) and input $YF_i(y, 2q+3)$ of the stage (ring “y”, stage “q+1”).

The output $F_o(y, 2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire Hop(2,1) to two inputs namely input $F_i(x, 2p+4)$ of the stage (ring “x”, stage “p+1”) and input $YU_i(x, 2p+1)$ of the stage (ring “x”, stage “p”). The output $B_o(y, 2q+4)$ of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to two inputs namely input $U_i(x, 2p+2)$ of the stage (ring “x”, stage “p”) and input $YF_i(x, 2p+3)$ of the stage (ring “x”, stage “p+1”).

Referring to diagram 1500 in FIG. 15, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring “x”, stage “p”) and (ring “x”, stage “p+1”) and two other arbitrary successive stages of any other ring namely the stages (ring “y”, stage “q”) and (ring “y”, stage “q+1”), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

The stage (ring “x”, stage “p”) consists of 5 inputs namely $R_i(x, 2p+1)$, $R_i(x, 2p+2)$, $U_i(x, 2p+1)$, $U_i(x, 2p+2)$, and $BY_i(x, 2p+2)$; and 4 outputs $B_o(x, 2p+1)$, $B_o(x, 2p+2)$, $F_o(x, 2p+1)$, and $F_o(x, 2p+2)$. The stage (ring “x”, stage “p”) also consists of seven 2:1 Muxes namely $R(x, 2p+1)$, $R(x, 2p+2)$, $F(x, 2p+1)$, $F(x, 2p+2)$, $U(x, 2p+1)$, $U(x, 2p+2)$, and $B(x, 2p+1)$. The stage (ring “x”, stage “p”) also consists of one 3:1 Mux namely $BY(x, 2p+2)$. The 2:1 Mux $R(x, 2p+1)$ has two inputs namely $R_i(x, 2p+1)$ and $B_o(x, 2p+1)$ and has one output $R_o(x, 2p+1)$. The 2:1 Mux $R(x, 2p+2)$ has two inputs namely $R_i(x, 2p+2)$ and $B_o(x, 2p+2)$ and has one output $R_o(x, 2p+2)$. The 2:1 Mux $F(x, 2p+1)$ has two inputs namely $R_o(x, 2p+1)$ and $R_o(x, 2p+2)$ and has one output $F_o(x, 2p+1)$. The 2:1 Mux $F(x, 2p+2)$ has two inputs namely $R_o(x, 2p+1)$, and $R_o(x, 2p+2)$, and has one output $F_o(x, 2p+2)$.

The 2:1 Mux $U(x, 2p+1)$ has two inputs namely $U_i(x, 2p+1)$ and $F_o(x, 2p+1)$ and has one output $U_o(x, 2p+1)$. The 2:1 Mux $U(x, 2p+2)$ has two inputs namely $U_i(x, 2p+2)$ and $F_o(x, 2p+2)$ and has one output $U_o(x, 2p+2)$. The 2:1 Mux $B(x, 2p+1)$ has two inputs namely $U_o(x, 2p+1)$ and $U_o(x, 2p+2)$ and has one output $B_o(x, 2p+1)$. The 3:1 Mux

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

BY(x,2p+2) has three inputs namely Uo(x,2p+1), Uo(x,2p+2), and BYi(x,2p+2), and has one output BYo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 5 inputs namely Ri(x,2p+3), Ri(x,2p+4), FYi(x,2p+4), Ui(x,2p+3), and Ui(x,2p+4); and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of seven 2:1 Muxes namely R(x,2p+3), R(x,2p+4), F(x,2p+3), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The stage (ring "x", stage "p+1") also consists of one 3:1 Mux namely FY(x,2p+4). The 2:1 Mux R(x,2p+3) has two inputs namely Ri(x,2p+3) and Bo(x,2p+3) and has one output Ro(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs namely Ri(x,2p+4) and Bo(x,2p+4) and has one output Ro(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely Ro(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+3). The 3:1 Mux FY(x,2p+4) has three inputs namely Ro(x,2p+3), Ro(x,2p+4), and FYi(x,2p+4), and has one output FYo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and Fo(x,2p+3) and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and FYo(x,2p+4) and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Ri(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 6 inputs namely Ri(y,2q+1), Ri(y,2q+2), FYi(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), and BYi(y,2q+2); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q") also consists of six 2:1 Muxes namely R(y,2q+1), R(y,2q+2), F(y,2q+1), U(y,2q+1), U(y,2q+2), and B(y,2q+1). The stage (ring "y", stage "q") also consists of two 3:1 Muxes namely FY(y,2q+2) and BY(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and Bo(y,2q+1) and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

two inputs namely $R_i(y, 2q+2)$ and $B_o(y, 2q+2)$ and has one output $R_o(y, 2q+2)$. The 2:1 Mux $F(y, 2q+1)$ has two inputs namely $R_o(y, 2q+1)$ and $R_o(y, 2q+2)$ and has one output $F_o(y, 2q+1)$. The 3:1 Mux $F_Y(y, 2q+2)$ has three inputs namely $R_o(y, 2q+1)$, $R_o(y, 2q+2)$, and $F_Yi(y, 2q+2)$, and has one output $F_Yo(y, 2q+2)$.

5 The 2:1 Mux $U(y, 2q+1)$ has two inputs namely $U_i(y, 2q+1)$ and $F_o(y, 2q+1)$ and has one output $U_o(y, 2q+1)$. The 2:1 Mux $U(y, 2q+2)$ has two inputs namely $U_i(y, 2q+2)$ and $F_Yo(y, 2q+2)$ and has one output $U_o(y, 2q+2)$. The 2:1 Mux $B(y, 2q+1)$ has two inputs namely $U_o(y, 2q+1)$ and $U_o(y, 2q+2)$ and has one output $B_o(y, 2q+1)$. The 3:1 Mux $B_Y(y, 2q+2)$ has three inputs namely $U_o(y, 2q+1)$, $U_o(y, 2q+2)$, and $B_Yi(y, 2q+2)$ and has
10 one output $B_Yo(y, 2q+2)$.

The stage (ring “y”, stage “q+1”) consists of 5 inputs namely $F_i(y, 2q+3)$, $F_i(y, 2q+4)$, $YF_i(y, 2q+3)$, $U_i(y, 2q+3)$, and $U_i(y, 2q+4)$; and 4 outputs $B_o(y, 2q+3)$, $B_o(y, 2q+4)$, $F_o(y, 2q+3)$, and $F_o(y, 2q+4)$. The stage (ring “y”, stage “q+1”) also consists of seven 2:1 Muxes namely $YF(y, 2q+3)$, $F(y, 2q+3)$, $F(y, 2q+4)$, $U(y, 2q+3)$, $U(y, 2q+4)$,
15 $B(y, 2q+3)$, and $B(y, 2q+4)$. The 2:1 Mux $YF(y, 2q+3)$ has two inputs namely $F_i(y, 2q+3)$ and $YF_i(y, 2q+3)$ and has one output $YF_o(y, 2q+3)$. The 2:1 Mux $F(y, 2q+3)$ has two inputs namely $YF_o(y, 2q+3)$ and $F_i(y, 2q+4)$ and has one output $F_o(y, 2q+3)$. The 2:1 Mux $F(y, 2q+4)$ has two inputs namely $YF_o(y, 2q+3)$ and $F_i(y, 2q+4)$ and has one output $F_o(y, 2q+4)$.

20 The 2:1 Mux $U(y, 2q+3)$ has two inputs namely $U_i(y, 2q+3)$ and $F_o(y, 2q+3)$ and has one output $U_o(y, 2q+3)$. The 2:1 Mux $U(y, 2q+4)$ has two inputs namely $U_i(y, 2q+4)$ and $F_o(y, 2q+4)$ and has one output $U_o(y, 2q+4)$. The 2:1 Mux $B(y, 2q+3)$ has two inputs namely $U_o(y, 2q+3)$ and $U_o(y, 2q+4)$ and has one output $B_o(y, 2q+3)$. The 2:1 Mux $B(y, 2q+4)$ has two inputs namely $U_o(y, 2q+3)$ and $U_o(y, 2q+4)$ and has one output
25 $B_o(y, 2q+4)$.

The output $F_o(y, 2q+1)$ of the stage (ring “y”, stage “q”) is connected to the input $F_i(y, 2q+3)$ of the stage (ring “y”, stage “q+1”). And the output $B_o(y, 2q+3)$ of the stage (ring “y”, stage “q+1”) is connected to the input $U_i(y, 2q+1)$ of the stage (ring “y”, stage “q”).

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The output $Fo(x,2p+2)$ of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to two inputs namely input $Fi(y,2q+4)$ of the stage (ring “y”, stage “q+1”) and input $BYi(y,2q+1)$ of the stage (ring “y”, stage “q”). The output $Bo(x,2p+4)$ of the stage (ring “x”, stage “p+1”) is connected via the wire Hop(1,2) to two inputs namely input
 5 $Ui(y,2q+2)$ of the stage (ring “y”, stage “q”) and input $YFi(y,2q+3)$ of the stage (ring “y”, stage “q+1”).

The output $Fo(y,2q+2)$ of the stage (ring “y”, stage “q”) is connected via the wire Hop(2,1) to two inputs namely input $Ri(x,2p+4)$ of the stage (ring “x”, stage “p+1”) and input $BYi(x,2p+1)$ of the stage (ring “x”, stage “p”). The output $Bo(y,2q+4)$ of the stage
 10 (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to two inputs namely input $Ui(x,2p+2)$ of the stage (ring “x”, stage “p”) and input $YFi(x,2p+4)$ of the stage (ring “x”, stage “p+1”).

In accordance with the current invention, either partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100A of FIG. 1A, or partial multi-stage hierarchical
 15 network $V_{D-Comb}(N_1, N_2, d, s)$ 100B of FIG. 1B, or partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C, corresponding to a block of 2D-grid of blocks 800 of FIG. 8, using any one of the embodiments of 200A-200F of FIGs. 2A-2F, 900A-900E of FIGs. 9A-9E, 1000A-1000F of FIGs. 10A-10F, 1100A-1100C of FIGs. 11A-11C to implement a stage of a ring of the multi-stage hierarchical network, either by
 20 using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, 300E of FIG. 3E, 500A of FIG. 5A, 1200 of FIG. 12, 1300 of FIG. 13, 1400 of FIG. 14, and
 25 1500 of FIG. 15 or by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may be any one of the embodiments of either the diagrams 400A of FIG. 4A, 400B of FIG. 4B, 600A of FIG. 6A, or 600B of FIG. 6B is very efficient in the reduction of the die size, power consumption, and highly optimized for lower
 30 wire/path delay for higher performance for practical routing applications to particularly to set up broadcast, unicast and multicast connections. In general in accordance with the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

current invention, where N_1 and N_2 of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ may be arbitrarily large in size and also the 2D-grid size 800 may also be arbitrarily large in size in terms of both the number of rows and number of columns.

5 1) Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in programmable integrated circuit applications. FIG. 16A2 illustrates the detailed diagram 1600A2 for the implementation of the diagram 1600A1 in programmable integrated circuit embodiments. Each crosspoint is implemented by a transistor coupled between the
10 corresponding inlet link and outlet link, and a programmable cell in programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by transistor C(1,1) coupled between inlet link IL1 and outlet link OL1, and programmable cell P(1,1); crosspoint CP(1,2) is implemented by transistor C(1,2) coupled between inlet link IL1 and outlet link OL2, and programmable cell P(1,2); crosspoint CP(2,1) is
15 implemented by transistor C(2,1) coupled between inlet link IL2 and outlet link OL1, and programmable cell P(2,1); and crosspoint CP(2,2) is implemented by transistor C(2,2) coupled between inlet link IL2 and outlet link OL2, and programmable cell P(2,2).

If the programmable cell is programmed ON, the corresponding transistor couples the corresponding inlet link and outlet link. If the programmable cell is programmed
20 OFF, the corresponding inlet link and outlet link are not connected. For example if the programmable cell P(1,1) is programmed ON, the corresponding transistor C(1,1) couples the corresponding inlet link IL1 and outlet link OL1. If the programmable cell P(1,1) is programmed OFF, the corresponding inlet link IL1 and outlet link OL1 are not connected. In volatile programmable integrated circuit embodiments the programmable cell may be
25 an SRAM (Static Random Address Memory) cell. In non-volatile programmable integrated circuit embodiments the programmable cell may be a Flash memory cell. Also the programmable integrated circuit embodiments may implement field programmable logic arrays (FPGA) devices, or programmable Logic devices (PLD), or Application Specific Integrated Circuits (ASIC) embedded with programmable logic circuits or 3D-
30 FPGAs.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

FIG. 16A2 also illustrates a buffer B1 on inlet link IL2. The signals driven along inlet link IL2 are amplified by buffer B1. Buffer B1 can be inverting or non-inverting buffer. Buffers such as B1 are used to amplify the signal in links which are usually long.

In other embodiments all the $d * d$ switches described in the current invention are also implemented using muxes of different sizes controlled by SRAM cells or flash cells etc.

2) One-time Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in one-time programmable integrated circuit applications. FIG. 16A3 illustrates the detailed diagram 1600A3 for the implementation of the diagram 1600A1 in one-time programmable integrated circuit embodiments. Each crosspoint is implemented by a via coupled between the corresponding inlet link and outlet link in one-time programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by via V(1,1) coupled between inlet link IL1 and outlet link OL1; crosspoint CP(1,2) is implemented by via V(1,2) coupled between inlet link IL1 and outlet link OL2; crosspoint CP(2,1) is implemented by via V(2,1) coupled between inlet link IL2 and outlet link OL1; and crosspoint CP(2,2) is implemented by via V(2,2) coupled between inlet link IL2 and outlet link OL2.

If the via is programmed ON, the corresponding inlet link and outlet link are permanently connected which is denoted by thick circle at the intersection of inlet link and outlet link. If the via is programmed OFF, the corresponding inlet link and outlet link are not connected which is denoted by the absence of thick circle at the intersection of inlet link and outlet link. For example in the diagram 1600A3 the via V(1,1) is programmed ON, and the corresponding inlet link IL1 and outlet link OL1 are connected as denoted by thick circle at the intersection of inlet link IL1 and outlet link OL1; the via V(2,2) is programmed ON, and the corresponding inlet link IL2 and outlet link OL2 are connected as denoted by thick circle at the intersection of inlet link IL2 and outlet link OL2; the via V(1,2) is programmed OFF, and the corresponding inlet link IL1 and outlet link OL2 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL1 and outlet link OL2; the via V(2,1) is programmed OFF, and the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

corresponding inlet link IL2 and outlet link OL1 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL2 and outlet link OL1. One-time programmable integrated circuit embodiments may be anti-fuse based programmable integrated circuit devices or mask programmable structured ASIC devices.

5 **3) Integrated Circuit Placement and Route Embodiments:**

All the embodiments disclosed in the current invention are useful in Integrated Circuit Placement and Route applications, for example in ASIC backend Placement and Route tools. FIG. 16A4 illustrates the detailed diagram 1600A4 for the implementation of the diagram 1600A1 in Integrated Circuit Placement and Route embodiments. In an
10 integrated circuit since the connections are known a-priori, the switch and crosspoints are actually virtual. However the concept of virtual switch and virtual crosspoint using the embodiments disclosed in the current invention reduces the number of required wires, wire length needed to connect the inputs and outputs of different netlists and the time required by the tool for placement and route of netlists in the integrated circuit.

15 Each virtual crosspoint is used to either to hardwire or provide no connectivity between the corresponding inlet link and outlet link. Specifically crosspoint CP(1,1) is implemented by direct connect point DCP(1,1) to hardwire (i.e., to permanently connect) inlet link IL1 and outlet link OL1 which is denoted by the thick circle at the intersection of inlet link IL1 and outlet link OL1; crosspoint CP(2,2) is implemented by direct
20 connect point DCP(2,2) to hardwire inlet link IL2 and outlet link OL2 which is denoted by the thick circle at the intersection of inlet link IL2 and outlet link OL2. The diagram 1600A4 does not show direct connect point DCP(1,2) and direct connect point DCP(1,3) since they are not needed and in the hardware implementation they are eliminated. Alternatively inlet link IL1 needs to be connected to outlet link OL1 and inlet link IL1
25 does not need to be connected to outlet link OL2. Also inlet link IL2 needs to be connected to outlet link OL2 and inlet link IL2 does not need to be connected to outlet link OL1. Furthermore in the example of the diagram 1600A4, there is no need to drive the signal of inlet link IL1 horizontally beyond outlet link OL1 and hence the inlet link IL1 is not even extended horizontally until the outlet link OL2. Also the absence of direct
30 connect point DCP(2,1) illustrates there is no need to connect inlet link IL2 and outlet link OL1.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

In summary in integrated circuit placement and route tools, the concept of virtual switches and virtual cross points is used during the implementation of the placement & routing algorithmically in software, however during the hardware implementation cross points in the cross state are implemented as hardwired connections between the
5 corresponding inlet link and outlet link, and in the bar state are implemented as no connection between inlet link and outlet link.

3) More Application Embodiments:

10 All the embodiments disclosed in the current invention are also useful in the design of SoC interconnects, Field programmable interconnect chips, parallel computer systems and in time-space-time switches.

Scheduling Method Embodiments the multi-stage hierarchical network

15 $V_{Comb}(N_1, N_2, d, s)$:

FIG. 17 shows a high-level flowchart of a scheduling method 1700, in one embodiment executed to setup multicast and unicast connections in the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ disclosed in this invention. According to this embodiment, the set of multicast connections are initialized to the beginning of the set in
20 act 1710. Then the control goes to act 1720. In act 1720, next multicast connection is selected in sequence form the set of multicast connections. Then the control goes to act 1730.

In act 1730 it is checked if this is the next multicast connection in sequence is NULL or i.e. all the multicast connections are scheduled. If act 1730 results “no”, that is
25 there are more multicast connections to be scheduled the control goes to act 1740. In act 1740 it is checked if this multicast connection is being scheduled for the first time. Or if it is not scheduled for the first time, it is checked if any one of the links taken by this

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

multicast connection is oversubscribed by any other multicast connection is checked. If either the multicast connection is being scheduled for the first time or if any one of the links taken by this multicast connection is oversubscribed the control goes to act 1750. Otherwise control goes to act 1720 where the next multicast connection will be selected.
5 So act 1720, act 1730, and act 1740 are executed in a loop.

In act 1750 the multicast connection is not being scheduled for the first time and since at least one of the links taken by this multicast connection is oversubscribed, the complete path taken this multicast connection is cleared or the multicast connection's path is ripped. Then the control goes to act 1760. In act 1760, using the well-known A*
10 search algorithm the least cost path from its source outlet link of the computational block to all the target inlet links of the corresponding computational blocks are found out one after another target inlet links. The cost function used is based on the Manhattan distance between the target inlet link's block and source outlet link's block by taking the delays on each wire is considered in the cost function and also that longest wires are chosen first in
15 the A* search algorithm.

According to the current invention, before scheduling the set of multicast connections in the scheduling method 1700, first a set of static cost tables will be prepared with the least cost paths from each link of the partial multistage network $V_{Comb}(N_1, N_2, d, s)$ to each outgoing hop wire from that partial multistage network as well
20 as to each inlet link of the computational block connected form that partial multistage network. So there will be as many cost tables created equal to the sum of the total number of outgoing hop wires from the partial multistage network and the inlet links of the computational block connected form that partial multistage network. Each cost table will also have as many entries as there are internal links of that partial multistage network.
25 And the value at each entry of these cost tables is equal to the total delay from the corresponding internal link to the corresponding outgoing hop wire or to the inlet link of the computational block.

In act 1760, according to the current invention, for the look-ahead cost computation during the A* search algorithm both the cost from the static cost tables from
30 the current internal link in the current partial multistage network and the cost value computed based on the Manhattan distance between the target inlet link's block and the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

current link's corresponding block by taking the delays on each wire into consideration are added. Also the least of the cost values from all the cost tables corresponding to the current link and all the outgoing wires in the right direction of the target block, is selected before it is added to the Manhattan distance based cost. Finally in act 1760, the multicast
 5 connection is scheduled as for the A* search algorithm. Then the control goes to act 1770.

In act 1770, the demand cost and history cost of each link used by the current multicast connection are updated. And the control goes to act 1720. Thus act 1720, act 1730, act 1740, act 1750, act 1760, and act 1770 are executed in a loop to schedule the multicast connections by going through the list of all multicast connections which will be
 10 one pass or iteration.

In act 1730 results "yes", i.e. all the required multicast connections in the list are scheduled in this pass or iteration, then the control goes to act 1780. In act 1780, the total number of links in the complete multistage network that are taken by more than one multicast connection are counted, hereinafter "OSN" or "Over Subscription nodes". Then
 15 the control goes to act 1790. In act 1790 it will be checked and if OSN is not equal to zero then the act 1790 results in "no" and the control goes to act 1710 to start the next iteration or pass to schedule all the required multicast connections in the list of all multicast connections. Thus act 1710, act 1720, act 1730, act 1740, act 1750, act 1760, act 1770,
 20 act 1780, and act 1790 are executed in a loop to implement different passes or iterations of scheduling the set of all multicast connections. If the act 1790 results in "yes", that means no link in the complete multistage network is taken by more than one multicast connection and hence the scheduling is successfully completed.

Each multicast connection of the type described above in reference to method 1700 of FIG. 17 can be unicast connection, a multicast connection or a broadcast
 25 connection, depending on the example.

Inter-block and Intra-block Scheduling Method Embodiments the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$:

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

FIG. 18 shows a high-level flowchart of a scheduling method 1800, in one embodiment executed to setup multicast connections in the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ disclosed in this invention in two steps (one for each act 1810 and act 1820 as shown in FIG. 18) namely: 1) scheduling the set of multicast connections outside the blocks of 2D-grid of blocks with each block corresponding to a partial multi-stage network, or in between the blocks of the complete multi-stage network, or alternatively on the external wires of the complete multi-stage network hereinafter “inter-block scheduling”. Inter-block scheduling is implemented in act 1810 so that there are no OSN nodes. During inter-block scheduling the partial multi-stage hierarchical network corresponding to each block is considered as a single stage network or alternatively each internal wire of the partial multi-stage hierarchical network is directly connected to each outgoing wire or external wire of the partial multi-stage hierarchical network, and 2) scheduling the set of multicast connections inside the blocks of 2D-grid of blocks with each block corresponding to a partial multi-stage network or alternatively on the internal wires of the complete multi-stage network hereinafter “intra-block scheduling”. The act 1820 implements intra-block scheduling for each block so that there are no OSN nodes.

The act 1810 may be implemented by the scheduling method 1700 of FIG. 17. Similarly in act 1820 for each block of the multi-stage hierarchical network, the inter-block scheduling may be implemented by the scheduling method 1700 of FIG. 17.

In accordance with the current invention, the scheduling method 1700 of FIG. 17 and the scheduling method 1800 of FIG. 18 are applicable to either partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100A of FIG. 1A, or partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100B of FIG. 1B, or partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C, corresponding to a block of 2D-grid of blocks 800 of FIG. 8, using any one of the embodiments of 200A-200F of FIGs. 2A-2F, 900A-900E of FIGs. 9A-9E, 1000A-1000F of FIGs. 10A-10F, 1100A-1100C of FIGs. 11A-11C to implement a stage of a ring of the multi-stage hierarchical network, either by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, 300E of FIG. 3E, 500A of FIG. 5A, 1200 of FIG. 12, 1300 of FIG. 13, 1400 of FIG. 14, and 1500 of FIG. 15 or by using the hop wire connections or multi-hop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may be any one of the embodiments of
 5 either the diagrams 400A of FIG. 4A, 400B of FIG. 4B, 600A of FIG. 6A, or 600B of FIG. 6B is very efficient in the reduction of the die size, power consumption, and highly optimized for lower wire/path delay for higher performance for practical routing applications to particularly to set up broadcast, unicast and multicast connections.

10 Numerous modifications and adaptations of the embodiments, implementations, and examples described herein will be apparent to the skilled artisan in view of the disclosure.

V. UNEDITED AND COMPLETE SUBSTITUTE SPECIFICATION

15 Unedited and complete substitute specification appears below:

Fully connected multi-stage hierarchical networks are an over kill in every dimension such as area, power, and performance for certain practical routing applications and need to be optimized to significantly improve savings in area, power and
 20 performance of the routing network. The present invention discloses several embodiments of the optimized multi-stage hierarchical networks for practical routing applications along with their VLSI layout (floor plan) feasibility and simplicity.

The multi-stage hierarchical networks considered for optimization in the current invention include: generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded
 25 multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, generalized hypercube networks $V_{cube}(N_1, N_2, d, s)$, and generalized cube connected cycles networks $V_{ccc}(N_1, N_2, d, s)$ for $s = 1, 2, 3$ or any number in general. Alternatively the optimized multi-stage hierarchical networks disclosed in this invention inherit the properties of one or more of these networks, in addition to additional properties that may not be exhibited these networks.

The optimized multi-stage hierarchical networks disclosed are applicable for practical routing applications, with several goals such as: 1) all the signals in the design starting from an inlet link of the network to an outlet link of the network need to be setup without blocking. These signals may consist of broadcast, unicast and multicast connections; Each routing resource may need to be used by only one signal or connection; 2) physical area consumed by the routing network to setup all the signals needs to be small; 3) power consumption of the network needs to be small, after the signals are setup. Power may be both static power and dynamic power; 4) Delay of the signal or a connection needs to be small after it is setup through a path using several routing resources in the path. The smaller the delay of the connections will lead to faster performance of the design. Typically delay of the critical connections determines the performance of the design on a given network; 5) Designs need to be not only routed through the network (i.e., all the signals need to be setup from inlet links of the network to the outlet links of the network.), but also the routing needs to be in faster time using efficient routing algorithms; 6) Efficient VLSI layout of the network is also critical and can greatly influence all the other parameters including the area taken up by the network on the chip, total number of wires, length of the wires, delay through the signal paths and hence the maximum clock speed of operation.

The different varieties of multi-stage networks described in various embodiments in the current invention have not been implemented previously on the semiconductor chips. The practical application of these networks includes Field Programmable Gate Array (FPGA) chips. Current commercial FPGA products such as Xilinx's Vertex, Altera's Stratix, Lattice's ECPx implement island-style architecture using mesh and segmented mesh routing interconnects using either full crossbars or sparse crossbars.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

These routing interconnects consume large silicon area for crosspoints, long wires, large signal propagation delay and hence consume lot of power.

The current invention discloses the optimization and scheduling methods of multi-stage hierarchical networks with fast scheduling of connections, for practical routing applications of numerous types of multi-stage networks also using multi-drop links. The optimizations disclosed in the current invention are applicable to including the numerous generalized multi-stage networks disclosed in the following patent applications:

1) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-stage networks $V(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,270,400 that is incorporated by reference above.

2) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,170,040 that is incorporated by reference above.

3) Rearrangeably nonblocking for arbitrary fan-out multicast and unicast, and strictly nonblocking for unicast for generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$ and generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,363,649 that is incorporated by reference above.

4) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,170,040 that is incorporated by reference above.

5) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$ with numerous

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

connection topologies and the scheduling methods are described in detail in the US Patent No. 8,363,649 that is incorporated by reference above.

6) Strictly nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$ and generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,363,649 that is incorporated by reference above.

7) VLSI layouts of numerous types of multi-stage networks are described in the US Patent No. 8,269,523 entitled "VLSI LAYOUTS OF FULLY CONNECTED NETWORKS" that is incorporated by reference above.

8) VLSI layouts of numerous types of multi-stage networks are described in the US Patent No. 8,898,611 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED AND PYRAMID NETWORKS WITH LOCALITY EXPLOITATION" that is incorporated by reference above.

In addition the optimization with the VLSI layouts disclosed in the current invention are also applicable to generalized multi-stage pyramid networks $V_p(N_1, N_2, d, s)$, generalized folded multi-stage pyramid networks $V_{fold-p}(N_1, N_2, d, s)$, generalized butterfly fat pyramid networks $V_{bfp}(N_1, N_2, d, s)$, generalized multi-link multi-stage pyramid networks $V_{mlink-p}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage pyramid networks $V_{fold-mlink-p}(N_1, N_2, d, s)$, generalized multi-link butterfly fat pyramid networks $V_{mlink-bfp}(N_1, N_2, d, s)$, generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ and generalized cube connected cycles networks $V_{CCC}(N_1, N_2, d, s)$ for $s = 1, 2, 3$ or any number in general.

Finally the current invention discloses the optimizations and VLSI layouts of multi-stage hierarchical networks $V_{Comb}(N_1, N_2, d, s)$ and the optimizations and VLSI layouts of multi-stage hierarchical networks $V_{D-Comb}(N_1, N_2, d, s)$ for practical routing applications (particularly to set up broadcast, unicast and multicast connections), where

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

“Comb” denotes the combination of and “D-Comb” denotes the delay optimized combination of any of the generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$,
 5 generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, generalized multi-stage pyramid networks $V_p(N_1, N_2, d, s)$, generalized folded multi-stage pyramid networks $V_{fold-p}(N_1, N_2, d, s)$, generalized butterfly fat pyramid networks $V_{bfp}(N_1, N_2, d, s)$, generalized multi-link multi-stage pyramid networks $V_{mlink-p}(N_1, N_2, d, s)$, generalized
 10 folded multi-link multi-stage pyramid networks $V_{fold-mlink-p}(N_1, N_2, d, s)$, generalized multi-link butterfly fat pyramid networks $V_{mlink-bfp}(N_1, N_2, d, s)$, generalized hypercube networks $V_{cube}(N_1, N_2, d, s)$, and generalized cube connected cycles networks $V_{ccc}(N_1, N_2, d, s)$ for $s = 1, 2, 3$ or any number in general.

Multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$:

15 Referring to diagram 100A in FIG. 1A, in one embodiment, an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ where $N_1 = 200$; $N_2 = 400$; $d = 2$; and $s = 1$ corresponding to one computational block, with each computational block having 4 inlet links namely I1, I2, I3, and I4; and 2 outlet links namely O1 and O2. And for each computational block the corresponding partial multi-stage hierarchical network
 20 $V_{Comb}(N_1, N_2, d, s)$ 100A consists of two rings 110 and 120, where ring 110 consists of “m+1” stages namely (ring 1, stage 0), (ring 1, stage 1), ... (ring 1, stage “m-1”), and (ring 1, stage “m”), and ring 120 consists of “n+1” stages namely (ring 2, stage 0), (ring 2, stage 1), ... (ring 2, stage “n-1”), and (ring 2, stage “n”), where “m” and “n” are positive integers.

25 Ring 110 has inlet links $Ri(1,1)$ and $Ri(1,2)$, and has outlet links $Bo(1,1)$ and $Bo(1,2)$. Ring 120 has inlet links $Fi(2,1)$ and $Fi(2,2)$, and outlet links $Bo(2,1)$ and $Bo(2,2)$. And hence the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

of 4 inlet links and 4 outlet links corresponding to the two rings 110 and 120. Outlet link O1 of the computational block is connected to inlet link Ri(1,1) of ring 110 and also inlet link of Fi(2,1) of ring 120. Similarly outlet link O2 of the computational block is connected to inlet link Ri(1,2) of Ring 110 and also inlet link of Fi(2,2) of Ring 120. And outlet link Bo(1,1) of Ring 110 is connected to inlet link I1 of the computational block. Outlet link Bo(1,2) of Ring 110 is connected to inlet link I2 of the computational block. Similarly outlet link Bo(2,1) of Ring 120 is connected to inlet link I3 of the computational block. Outlet link Bo(2,2) of Ring 120 is connected to inlet link I4 of the computational block. Since in this embodiment outlet link O1 of the computational block is connected to both inlet link Ri(1,1) of ring 110 and inlet link Fi(2,1) of ring 120; and outlet link O2 of the computational block is connected to both inlet link Ri(1,2) of ring 110 and inlet link Fi(2,2) of ring 120, the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists of 2 inlet links and 4 outlet links.

The two dimensional grid 800 in FIG. 8 illustrates an exemplary arrangement of 100 blocks arranged in 10 rows and 10 columns, in an embodiment. Each row of 2D-grid consisting of 10 block numbers namely the first row consists of the blocks (1,1), (1,2), (1,3), ... , (1,9), and (1,10). The second row consists of the blocks (2,1), (2,2), (2,3), ... , (2,9), and (2,10). Similarly 2D-grid 800 consists of 10 rows of each with 10 blocks and finally the tenth row consists of the blocks (10,1), (10,2), (10,3), ... , (10,9), and (10,10). Each block of 2D-grid 800, in one embodiment, is part of the die area of a semiconductor integrated circuit (hereinafter alternatively referred to as "integrated circuit device" or "IC device"), so that the complete 2D-grid 800 of 100 blocks represents the complete die of the semiconductor integrated circuit. In one embodiment, each block of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A with 2 inlet links and 4 outlet links and the corresponding computational block with 4 inlet links and 2 outlet links. For example block (1,1) of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A with 2 inlet links and 4 outlet links and the corresponding computational block with 4 inlet links and 2 outlet links. Similarly each of the 100 blocks of 2D-grid 800 has a separate partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A with 2 inlet links and 4 outlet links and the corresponding computational block with 4 inlet links and 2 outlet links. Hence the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to 2D-grid 800 has $N_1 = 200$ inlet links and $N_2 = 400$ outlet links. And there are 100 computational blocks each one corresponding to one of the blocks with each computational block having 4 inlet links and 2 outlet links. Also the 2D-grid 800 is organized in the fourth quadrant of the 2D-Plane. In other embodiments the 2D-grid 800 may be organized as either first
 5 quadrant, or second quadrant or third quadrant of the 2D-Plane.

Referring to partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A in FIG. 1A, the stage (ring 1, stage 0) consists of 4 inputs namely $Ri(1,1)$, $Ri(1,2)$, $Ui(1,1)$, and $Ui(1,2)$; and 4 outputs $Bo(1,1)$, $Bo(1,2)$, $Fo(1,1)$, and $Fo(1,2)$. The stage (ring 1, stage
 10 0) also consists of eight 2:1 multiplexers (A multiplexer is hereinafter called a "mux") namely $R(1,1)$, $R(1,2)$, $F(1,1)$, $F(1,2)$, $U(1,1)$, $U(1,2)$, $B(1,1)$, and $B(1,2)$. The 2:1 Mux $R(1,1)$ has two inputs namely $Ri(1,1)$ and $Bo(1,1)$ and has one output $Ro(1,1)$. The 2:1 Mux $R(1,2)$ has two inputs namely $Ri(1,2)$ and $Bo(1,2)$ and has one output $Ro(1,2)$. The 2:1 Mux $F(1,1)$ has two inputs namely $Ro(1,1)$ and $Ro(1,2)$ and has one output $Fo(1,1)$.
 15 The 2:1 Mux $F(1,2)$ has two inputs namely $Ro(1,1)$ and $Ro(1,2)$ and has one output $Fo(1,2)$.

The 2:1 Mux $U(1,1)$ has two inputs namely $Ui(1,1)$ and $Fo(1,1)$ and has one output $Uo(1,1)$. The 2:1 Mux $U(1,2)$ has two inputs namely $Ui(1,2)$ and $Fo(1,2)$ and has one output $Uo(1,2)$. The 2:1 Mux $B(1,1)$ has two inputs namely $Uo(1,1)$ and $Uo(1,2)$ and
 20 has one output $Bo(1,1)$. The 2:1 Mux $B(1,2)$ has two inputs namely $Uo(1,1)$ and $Uo(1,2)$ and has one output $Bo(1,2)$.

The stage (ring 1, stage 1) consists of 4 inputs namely $Ri(1,3)$, $Ri(1,4)$, $Ui(1,3)$, and $Ui(1,4)$; and 4 outputs $Bo(1,3)$, $Bo(1,4)$, $Fo(1,3)$, and $Fo(1,4)$. The stage (ring 1, stage
 1) also consists of eight 2:1 Muxes namely $R(1,3)$, $R(1,4)$, $F(1,3)$, $F(1,4)$, $U(1,3)$, $U(1,4)$,
 25 $B(1,3)$, and $B(1,4)$. The 2:1 Mux $R(1,3)$ has two inputs namely $Ri(1,3)$ and $Bo(1,3)$ and has one output $Ro(1,3)$. The 2:1 Mux $R(1,4)$ has two inputs namely $Ri(1,4)$ and $Bo(1,4)$ and has one output $Ro(1,4)$. The 2:1 Mux $F(1,3)$ has two inputs namely $Ro(1,3)$ and $Ro(1,4)$ and has one output $Fo(1,3)$. The 2:1 Mux $F(1,4)$ has two inputs namely $Ro(1,3)$ and $Ro(1,4)$ and has one output $Fo(1,4)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux U(1,3) has two inputs namely $U_i(1,3)$ and $F_o(1,3)$ and has one output $U_o(1,3)$. The 2:1 Mux U(1,4) has two inputs namely $U_i(1,4)$ and $F_o(1,4)$ and has one output $U_o(1,4)$. The 2:1 Mux B(1,3) has two inputs namely $U_o(1,3)$ and $U_o(1,4)$ and has one output $B_o(1,3)$. The 2:1 Mux B(1,4) has two inputs namely $U_o(1,3)$ and $U_o(1,4)$ and has one output $B_o(1,4)$.

The output $F_o(1,1)$ of the stage (ring 1, stage 0) is connected to the input $R_i(1,3)$ of the stage (ring 1, stage 1) which is called hereinafter an internal connection (hereinafter alternatively referred to as “straight link” or “straight middle link”) between two successive stages of a ring. And the output $B_o(1,3)$ of the stage (ring 1, stage 1) is connected to the input $U_i(1,1)$ of the stage (ring 1, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1.

The stage (ring 1, stage “m-1”) consists of 4 inputs namely $F_i(1,2m-1)$, $F_i(1,2m)$, $U_i(1,2m-1)$, and $U_i(1,2m)$; and 4 outputs $B_o(1,2m-1)$, $B_o(1,2m)$, $F_o(1,2m-1)$, and $F_o(1,2m)$. The stage (ring 1, stage “m-1”) also consists of six 2:1 Muxes namely $F(1,2m-1)$, $F(1,2m)$, $U(1,2m-1)$, $U(1,2m)$, $B(1,2m-1)$, and $B(1,2m)$. The 2:1 Mux $F(1,2m-1)$ has two inputs namely $F_i(1,2m-1)$ and $F_i(1,2m)$ and has one output $F_o(1,2m-1)$. The 2:1 Mux $F(1,2m)$ has two inputs namely $F_i(1,2m-1)$ and $F_i(1,2m)$ and has one output $F_o(1,2m)$.

The 2:1 Mux U(1,2m-1) has two inputs namely $U_i(1,2m-1)$ and $F_o(1,2m-1)$ and has one output $U_o(1,2m-1)$. The 2:1 Mux U(1,2m) has two inputs namely $U_i(1,2m)$ and $F_o(1,2m)$ and has one output $U_o(1,2m)$. The 2:1 Mux B(1,2m-1) has two inputs namely $U_o(1,2m-1)$ and $U_o(1,2m)$ and has one output $B_o(1,2m-1)$. The 2:1 Mux B(1,2m) has two inputs namely $U_o(1,2m-1)$ and $U_o(1,2m)$ and has one output $B_o(1,2m)$.

The stage (ring 1, stage “m”) consists of 4 inputs namely $F_i(1,2m+1)$, $F_i(1,2m+2)$, $U_i(1,2m+1)$, and $U_i(1,2m+2)$; and 4 outputs $B_o(1,2m+1)$, $B_o(1,2m+2)$, $F_o(1,2m+1)$, and $F_o(1,2m+2)$. The stage (ring 1, stage “m”) also consists of six 2:1 Muxes namely $F(1,2m+1)$, $F(1,2m+2)$, $U(1,2m+1)$, $U(1,2m+2)$, $B(1,2m+1)$, and $B(1,2m+2)$. The 2:1 Mux $F(1,2m+1)$ has two inputs namely $F_i(1,2m+1)$ and $F_i(1,2m+2)$ and has one output $F_o(1,2m+1)$. The 2:1 Mux $F(1,2m+2)$ has two inputs namely $F_i(1,2m+1)$ and $F_i(1,2m+2)$ and has one output $F_o(1,2m+2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux $U(1,2m+1)$ has two inputs namely $U_i(1,2m+1)$ and $F_o(1,2m+1)$ and has one output $U_o(1,2m+1)$. The 2:1 Mux $U(1,2m+2)$ has two inputs namely $U_i(1,2m+2)$ and $F_o(1,2m+2)$ and has one output $U_o(1,2m+2)$. The 2:1 Mux $B(1,2m+1)$ has two inputs namely $U_o(1,2m+1)$ and $U_o(1,2m+2)$ and has one output $B_o(1,2m+1)$. The 2:1 Mux
 5 $B(1,2m+2)$ has two inputs namely $U_o(1,2m+1)$ and $U_o(1,2m+2)$ and has one output $B_o(1,2m+2)$.

The output $F_o(1,2m-1)$ of the stage (ring 1, stage "m-1") is connected to the input $F_i(1,2m+1)$ of the stage (ring 1, stage "m"), is an internal connection between stage "m-1" and stage "m" of the ring 1. And the output $B_o(1,2m+1)$ of the stage (ring 1, stage
 10 "m") is connected to the input $U_i(1,2m-1)$ of the stage (ring 1, stage "m-1"), is another internal connection between stage "m-1" and stage "m" of the ring 1

Just the same way the stages (ring 1, stage 0), (ring 1, stage 1), there are also stages (ring 1, stage 2), (ring 1, stage 3), ... (ring 1, stage "m-1"), (ring 1, stage "m") in that order, where the stages from (ring 1, stage 2), (ring 1, stage 3), ... , (ring 1, stage
 15 "m-2") are not shown in the diagram 100A. Just the same way the two successive stages (ring 1, stage 0) and (ring 1, stage 1) have internal connections between them as described before, any two successive stages have similar internal connections. For example (ring 1, stage 1) and (ring 1, stage 2) have similar internal connections and (ring 1, stage "m-2") and (ring 1, stage "m-1") have similar internal connections.

20 Stage (ring 1, stage 0) is also called hereinafter the "entry stage" or "first stage" of ring 1, since inlet links and outlet links of the computational block are directly connected to stage (ring 1, stage 0). Also stage (ring 1, stage "m") is hereinafter the "last stage" or "root stage" of ring 1.

The stage (ring 2, stage 0) consists of 4 inputs namely $F_i(2,1)$, $F_i(2,2)$, $U_i(2,1)$,
 25 and $U_i(2,2)$; and 4 outputs $B_o(2,1)$, $B_o(2,2)$, $F_o(2,1)$, and $F_o(2,2)$. The stage (ring 2, stage 0) also consists of six 2:1 Muxes namely $F(2,1)$, $F(2,2)$, $U(2,1)$, $U(2,2)$, $B(2,1)$, and $B(2,2)$. The 2:1 Mux $F(2,1)$ has two inputs namely $F_i(2,1)$ and $F_i(2,2)$ and has one output $F_o(2,1)$. The 2:1 Mux $F(2,2)$ has two inputs namely $F_i(2,1)$ and $F_i(2,2)$ and has one output $F_o(2,2)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux U(2,1) has two inputs namely $U_i(2,1)$ and $F_o(2,1)$ and has one output $U_o(2,1)$. The 2:1 Mux U(2,2) has two inputs namely $U_i(2,2)$ and $F_o(2,2)$ and has one output $U_o(2,2)$. The 2:1 Mux B(2,1) has two inputs namely $U_o(2,1)$ and $U_o(2,2)$ and has one output $B_o(2,1)$. The 2:1 Mux B(2,2) has two inputs namely $U_o(2,1)$ and $U_o(2,2)$ and has one output $B_o(2,2)$.

The stage (ring 2, stage 1) consists of 4 inputs namely $F_i(2,3)$, $F_i(2,4)$, $U_i(2,3)$, and $U_i(2,4)$; and 4 outputs $B_o(2,3)$, $B_o(2,4)$, $F_o(2,3)$, and $F_o(2,4)$. The stage (ring 2, stage 1) also consists of six 2:1 Muxes namely F(2,3), F(2,4), U(2,3), U(2,4), B(2,3), and B(2,4). The 2:1 Mux F(2,3) has two inputs namely $F_i(2,3)$ and $F_i(2,4)$ and has one output $F_o(2,3)$. The 2:1 Mux F(2,4) has two inputs namely $F_i(2,3)$ and $F_i(2,4)$ and has one output $F_o(2,4)$.

The 2:1 Mux U(2,3) has two inputs namely $U_i(2,3)$ and $F_o(2,3)$ and has one output $U_o(2,3)$. The 2:1 Mux U(2,4) has two inputs namely $U_i(2,4)$ and $F_o(2,4)$ and has one output $U_o(2,4)$. The 2:1 Mux B(2,3) has two inputs namely $U_o(2,3)$ and $U_o(2,4)$ and has one output $B_o(2,3)$. The 2:1 Mux B(2,4) has two inputs namely $U_o(2,3)$ and $U_o(2,4)$ and has one output $B_o(2,4)$.

The output $F_o(2,1)$ of the stage (ring 2, stage 0) is connected to the input $F_i(2,3)$ of the stage (ring 2, stage 1), is an internal connection between stage 0 and stage 1 of the ring 2. And the output $B_o(2,3)$ of the stage (ring 2, stage 1) is connected to the input $U_i(2,1)$ of the stage (ring 2, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1.

The stage (ring 2, stage "n-1") consists of 4 inputs namely $R_i(2,2n-1)$, $R_i(2,2n)$, $U_i(1,2n-1)$, and $U_i(1,2n)$; and 4 outputs $B_o(1,2n-1)$, $B_o(1,2n)$, $F_o(1,2n-1)$, and $F_o(1,2n)$. The stage (ring 2, stage "n-1") also consists of eight 2:1 Muxes namely R(2,2n-1), R(2,2n), F(2,2n-1), F(1,2n), U(1,2n-1), U(1,2n), B(1,2n-1), and B(1,2n). The 2:1 Mux R(2,2n-1) has two inputs namely $R_i(2,2n-1)$ and $B_o(2,2n-1)$ and has one output $R_o(2,2n-1)$. The 2:1 Mux R(2,2n) has two inputs namely $R_i(2,2n)$ and $B_o(2,2n)$ and has one output $R_o(2,2n)$. The 2:1 Mux F(2,2n-1) has two inputs namely $R_o(2,2n-1)$ and $R_o(2,2n)$ and has one output $F_o(2,2n-1)$. The 2:1 Mux F(2,2n) has two inputs namely $R_o(2,2n-1)$ and $R_o(2,2n)$ and has one output $F_o(2,2n)$.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux $U(2,2n-1)$ has two inputs namely $U_i(2,2n-1)$ and $F_o(2,2n-1)$ and has one output $U_o(2,2n-1)$. The 2:1 Mux $U(2,2n)$ has two inputs namely $U_i(2,2n)$ and $F_o(2,2n)$ and has one output $U_o(2,2n)$. The 2:1 Mux $B(2,2n-1)$ has two inputs namely $U_o(2,2n-1)$ and $U_o(2,2n)$ and has one output $B_o(2,2n-1)$. The 2:1 Mux $B(2,2n)$ has two
5 inputs namely $U_o(2,2n-1)$ and $U_o(2,2n)$ and has one output $B_o(2,2n)$.

The stage (ring 2, stage “n”) consists of 4 inputs namely $R_i(2,2n+1)$, $R_i(2,2n+2)$, $U_i(2,2n+1)$, and $U_i(2,2n+2)$; and 4 outputs $B_o(2,2n+1)$, $B_o(2,2n+2)$, $F_o(2,2n+1)$, and $F_o(2,2n+2)$. The stage (ring 2, stage “n”) also consists of eight 2:1 Muxes namely $R(2,2n+1)$, $R(2,2n+2)$, $F(2,2n+1)$, $F(2,2n+2)$, $U(2,2n+1)$, $U(2,2n+2)$, $B(2,2n+1)$, and
10 $B(2,2n+2)$. The 2:1 Mux $R(2,2n+1)$ has two inputs namely $R_i(2,2n+1)$ and $B_o(2,2n+1)$ and has one output $R_o(2,2n+1)$. The 2:1 Mux $R(2,2n+2)$ has two inputs namely $R_i(2,2n+2)$ and $B_o(2,2n+2)$ and has one output $R_o(2,2n+2)$. The 2:1 Mux $F(2,2n+1)$ has two inputs namely $R_o(2,2n+1)$ and $R_o(2,2n+2)$ and has one output $F_o(2,2n+1)$. The 2:1 Mux $F(2,2n+2)$ has two inputs namely $R_o(2,2n+1)$ and $R_o(2,2n+2)$ and has one output
15 $F_o(2,2n+2)$.

The 2:1 Mux $U(2,2n+1)$ has two inputs namely $U_i(2,2n+1)$ and $F_o(2,2n+1)$ and has one output $U_o(2,2n+1)$. The 2:1 Mux $U(2,2n+2)$ has two inputs namely $U_i(2,2n+2)$ and $F_o(2,2n+2)$ and has one output $U_o(2,2n+2)$. The 2:1 Mux $B(2,2n+1)$ has two inputs namely $U_o(2,2n+1)$ and $U_o(2,2n+2)$ and has one output $B_o(2,2n+1)$. The 2:1 Mux
20 $B(2,2n+2)$ has two inputs namely $U_o(2,2n+1)$ and $U_o(2,2n+2)$ and has one output $B_o(2,2n+2)$.

The output $F_o(2,2n-1)$ of the stage (ring 2, stage “n-1”) is connected to the input $R_i(2,2n+1)$ of the stage (ring 2, stage “n”), is an internal connection between stage “n-1” and stage “n” of the ring 1. And the output $B_o(2,2n+1)$ of the stage (ring 2, stage “n”) is
25 connected to the input $U_i(2,2n-1)$ of the stage (ring 2, stage “n-1”), is another internal connection between stage “n-1” and stage “n” of the ring 1.

Each stage of any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists of 4 inputs and $2 * d = 4$ outputs. Even though the stages (ring 1, stage 0), (ring 1, stage 1), (ring 2, stage “n-1”), and (ring 2, stage “n”) each have eight 2:1 muxes, and the stages (ring 2, stage 0), (ring 2, stage 1), (ring 1,
30

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

stage “m-1”), and (ring 1, stage “m”) each have six 2:1 muxes, in other embodiments any of these stages can be one of the four by four switch diagrams namely 200A of FIG. 2A, 200B of FIG. 2B, 200C of FIG. 2C, and one of the eight by four switch diagrams namely 200E of FIG. 2E, 200F of FIG. 2F.

5 Referring to diagram 100B in FIG. 1B, in one embodiment, an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ where $N_1 = 400$; $N_2 = 800$; $d = 2$; and $s = 1$ corresponding to one computational block, with each computational block having 8 inlet links namely I1, I2, I3, I4, I5, I6, I7, and I8; and 4 outlet links namely O1, O2, O3, and O4. And for each computational block the corresponding partial multi-stage
 10 hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of two rings 110 and 120, where ring 110 consists of “m+1” stages namely (ring 1, stage 0), (ring 1, stage 1), ... (ring 1, stage “m-1”), and (ring 1, stage “m”), and ring 120 consists of “n+1” stages namely (ring 2, stage 0), (ring 2, stage 1), ... (ring 2, stage “n-1”), and (ring 2, stage “n”), where “m” and “n” are positive integers.

15 Ring 110 has inlet links $Ri(1,1)$ and $Ri(1,2)$ from the left-hand side, and has outlet links $Bo(1,1)$ and $Bo(1,2)$ from left-hand side. Ring 110 also has inlet links $Ui(1,2m+1)$ and $Ui(1,2m+2)$ from the right-hand side, and has outlet links $Fo(1,2m+1)$ and $Fo(1,2m+2)$ from right-hand side. Ring 120 has inlet links $Fi(2,1)$ and $Fi(2,2)$ from left-hand side, and outlet links $Bo(2,1)$ and $Bo(2,2)$ from left-hand side. Ring 120 also has
 20 inlet links $Ui(2,2n+1)$ and $Ui(2,2n+2)$ from the right-hand side, and has outlet links $Fo(2,2n+1)$ and $Fo(2,2n+2)$ from right-hand side.

And the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of 8 inlet links and 4 outlet links corresponding to the two rings 110 and 120. From left-hand side, outlet link O1 of the computational block is connected to inlet link $Ri(1,1)$ of
 25 ring 110 and also inlet link of $Fi(2,1)$ of ring 120. Similarly from left-hand side, outlet link O2 of the computational block is connected to inlet link $Ri(1,2)$ of Ring 110 and also inlet link of $Fi(2,2)$ of Ring 120. And from left-hand side, outlet link $Bo(1,1)$ of Ring 110 is connected to inlet link I1 of the computational block. From left-hand side, Outlet link $Bo(1,2)$ of Ring 110 is connected to inlet link I2 of the computational block. Similarly
 30 from left-hand side, outlet link $Bo(2,1)$ of Ring 120 is connected to inlet link I3 of the

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

computational block. From left-hand side, outlet link $Bo(2,2)$ of Ring 120 is connected to inlet link I4 of the computational block.

From right-hand side, outlet link O3 of the computational block is connected to inlet link $Ui(1,2m+1)$ of ring 110 and also inlet link of $Ui(2,2n+1)$ of ring 120. Similarly
 5 from right-hand side, outlet link O4 of the computational block is connected to inlet link $Ui(1,2m+2)$ of Ring 110 and also inlet link of $Ui(2,2n+2)$ of Ring 120. And from right-hand side, outlet link $Fo(1,2m+1)$ of Ring 110 is connected to inlet link I5 of the computational block. From right-hand side, outlet link $Fo(1,2m+2)$ of Ring 110 is connected to inlet link I6 of the computational block. Similarly from right-hand side,
 10 outlet link $Fo(2,2n+1)$ of Ring 120 is connected to inlet link I7 of the computational block. From right-hand side, outlet link $Fo(2,2n+2)$ of Ring 120 is connected to inlet link I8 of the computational block.

Since in this embodiment outlet link O1 of the computational block is connected to both inlet link $Ri(1,1)$ of ring 110 and inlet link $Fi(2,1)$ of ring 120; outlet link O2 of
 15 the computational block is connected to both inlet link $Ri(1,2)$ of ring 110 and inlet link $Fi(2,2)$ of ring 120; outlet link O3 of the computational block is connected to both inlet link $Ui(1,2m+1)$ of ring 110 and inlet link $Ui(2,2n+1)$ of ring 120; and outlet link O4 of the computational block is connected to both inlet link $Ui(1,2m+2)$ of ring 110 and inlet link $Ui(2,2n+2)$ of ring 120, the partial multi-stage hierarchical network
 20 $V_{Comb}(N_1, N_2, d, s)$ 100B consists of 4 inlet links and 8 outlet links.

Referring to two dimensional grid 800 in FIG. 8 illustrates, in another embodiment, each block of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B with 4 inlet links and 8 outlet links and the corresponding computational block with 8 inlet links and 4 outlet links. For example
 25 block (1,1) of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B with 4 inlet links and 8 outlet links and the corresponding computational block with 8 inlet links and 4 outlet links. Similarly each of the 100 blocks of 2D-grid 800 has a separate partial multi-stage hierarchical network
 30 $V_{Comb}(N_1, N_2, d, s)$ 100B with 4 inlet links and 8 outlet links and the corresponding computational block with 8 inlet links and 4 outlet links. Hence the complete multi-stage

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to 2D-grid 800 has $N_1 = 400$ inlet links and $N_2 = 800$ outlet links. Since there are 100 computational blocks each one corresponding to one of the blocks with each computational block having 8 inlet links and 4 outlet links. Also the 2D-grid 800 is organized in the fourth quadrant of the 2D-Plane.

- 5 In other embodiments the 2D-grid 800 may be organized as either first quadrant, or second quadrant or third quadrant of the 2D-Plane.

Referring to partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B in FIG. 1B, the stage (ring 1, stage 0) consists of 4 inputs namely $R_i(1,1)$, $R_i(1,2)$, $U_i(1,1)$, and $U_i(1,2)$; and 4 outputs $B_o(1,1)$, $B_o(1,2)$, $F_o(1,1)$, and $F_o(1,2)$. The stage (ring 1, stage 0) also consists of eight 2:1 multiplexers (A multiplexer is hereinafter called a “mux”) namely $R(1,1)$, $R(1,2)$, $F(1,1)$, $F(1,2)$, $U(1,1)$, $U(1,2)$, $B(1,1)$, and $B(1,2)$. The 2:1 Mux $R(1,1)$ has two inputs namely $R_i(1,1)$ and $B_o(1,1)$ and has one output $R_o(1,1)$. The 2:1 Mux $R(1,2)$ has two inputs namely $R_i(1,2)$ and $B_o(1,2)$ and has one output $R_o(1,2)$. The 2:1 Mux $F(1,1)$ has two inputs namely $R_o(1,1)$ and $R_o(1,2)$ and has one output $F_o(1,1)$.
15 The 2:1 Mux $F(1,2)$ has two inputs namely $R_o(1,1)$ and $R_o(1,2)$ and has one output $F_o(1,2)$.

The 2:1 Mux $U(1,1)$ has two inputs namely $U_i(1,1)$ and $F_o(1,1)$ and has one output $U_o(1,1)$. The 2:1 Mux $U(1,2)$ has two inputs namely $U_i(1,2)$ and $F_o(1,2)$ and has one output $U_o(1,2)$. The 2:1 Mux $B(1,1)$ has two inputs namely $U_o(1,1)$ and $U_o(1,2)$ and has one output $B_o(1,1)$. The 2:1 Mux $B(1,2)$ has two inputs namely $U_o(1,1)$ and $U_o(1,2)$ and has one output $B_o(1,2)$.
20

The stage (ring 1, stage 1) consists of 4 inputs namely $R_i(1,3)$, $R_i(1,4)$, $U_i(1,3)$, and $U_i(1,4)$; and 4 outputs $B_o(1,3)$, $B_o(1,4)$, $F_o(1,3)$, and $F_o(1,4)$. The stage (ring 1, stage 1) also consists of eight 2:1 Muxes namely $R(1,3)$, $R(1,4)$, $F(1,3)$, $F(1,4)$, $U(1,3)$, $U(1,4)$, $B(1,3)$, and $B(1,4)$. The 2:1 Mux $R(1,3)$ has two inputs namely $R_i(1,3)$ and $B_o(1,3)$ and has one output $R_o(1,3)$. The 2:1 Mux $R(1,4)$ has two inputs namely $R_i(1,4)$ and $B_o(1,4)$ and has one output $R_o(1,4)$. The 2:1 Mux $F(1,3)$ has two inputs namely $R_o(1,3)$ and $R_o(1,4)$ and has one output $F_o(1,3)$. The 2:1 Mux $F(1,4)$ has two inputs namely $R_o(1,3)$ and $R_o(1,4)$ and has one output $F_o(1,4)$.
25

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

The 2:1 Mux U(1,3) has two inputs namely $U_i(1,3)$ and $F_o(1,3)$ and has one output $U_o(1,3)$. The 2:1 Mux U(1,4) has two inputs namely $U_i(1,4)$ and $F_o(1,4)$ and has one output $U_o(1,4)$. The 2:1 Mux B(1,3) has two inputs namely $U_o(1,3)$ and $U_o(1,4)$ and has one output $B_o(1,3)$. The 2:1 Mux B(1,4) has two inputs namely $U_o(1,3)$ and $U_o(1,4)$ and has one output $B_o(1,4)$.

The output $F_o(1,1)$ of the stage (ring 1, stage 0) is connected to the input $R_i(1,3)$ of the stage (ring 1, stage 1) which is called hereinafter an internal connection between two successive stages of a ring. And the output $B_o(1,3)$ of the stage (ring 1, stage 1) is connected to the input $U_i(1,1)$ of the stage (ring 1, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1.

The stage (ring 1, stage "m-1") consists of 4 inputs namely $F_i(1,2m-1)$, $F_i(1,2m)$, $U_i(1,2m-1)$, and $U_i(1,2m)$; and 4 outputs $B_o(1,2m-1)$, $B_o(1,2m)$, $F_o(1,2m-1)$, and $F_o(1,2m)$. The stage (ring 1, stage "m-1") also consists of six 2:1 Muxes namely $F(1,2m-1)$, $F(1,2m)$, $U(1,2m-1)$, $U(1,2m)$, $B(1,2m-1)$, and $B(1,2m)$. The 2:1 Mux $F(1,2m-1)$ has two inputs namely $F_i(1,2m-1)$ and $F_i(1,2m)$ and has one output $F_o(1,2m-1)$. The 2:1 Mux $F(1,2m)$ has two inputs namely $F_i(1,2m-1)$ and $F_i(1,2m)$ and has one output $F_o(1,2m)$.

The 2:1 Mux U(1,2m-1) has two inputs namely $U_i(1,2m-1)$ and $F_o(1,2m-1)$ and has one output $U_o(1,2m-1)$. The 2:1 Mux U(1,2m) has two inputs namely $U_i(1,2m)$ and $F_o(1,2m)$ and has one output $U_o(1,2m)$. The 2:1 Mux B(1,2m-1) has two inputs namely $U_o(1,2m-1)$ and $U_o(1,2m)$ and has one output $B_o(1,2m-1)$. The 2:1 Mux B(1,2m) has two inputs namely $U_o(1,2m-1)$ and $U_o(1,2m)$ and has one output $B_o(1,2m)$.

The stage (ring 1, stage "m") consists of 4 inputs namely $F_i(1,2m+1)$, $F_i(1,2m+2)$, $U_i(1,2m+1)$, and $U_i(1,2m+2)$; and 4 outputs $B_o(1,2m+1)$, $B_o(1,2m+2)$, $F_o(1,2m+1)$, and $F_o(1,2m+2)$. The stage (ring 1, stage "m") also consists of six 2:1 Muxes namely $F(1,2m+1)$, $F(1,2m+2)$, $U(1,2m+1)$, $U(1,2m+2)$, $B(1,2m+1)$, and $B(1,2m+2)$. The 2:1 Mux $F(1,2m+1)$ has two inputs namely $F_i(1,2m+1)$ and $F_i(1,2m+2)$ and has one output $F_o(1,2m+1)$. The 2:1 Mux $F(1,2m+2)$ has two inputs namely $F_i(1,2m+1)$ and $F_i(1,2m+2)$ and has one output $F_o(1,2m+2)$.

The 2:1 Mux U(1,2m+1) has two inputs namely $U_i(1,2m+1)$ and $F_o(1,2m+1)$ and has one output $U_o(1,2m+1)$. The 2:1 Mux U(1,2m+2) has two inputs namely $U_i(1,2m+2)$

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

and $Fo(1,2m+2)$ and has one output $Uo(1,2m+2)$. The 2:1 Mux $B(1,2m+1)$ has two inputs namely $Uo(1,2m+1)$ and $Uo(1,2m+2)$ and has one output $Bo(1,2m+1)$. The 2:1 Mux $B(1,2m+2)$ has two inputs namely $Uo(1,2m+1)$ and $Uo(1,2m+2)$ and has one output $Bo(1,2m+2)$.

5 The output $Fo(1,2m-1)$ of the stage (ring 1, stage "m-1") is connected to the input $Fi(1,2m+1)$ of the stage (ring 1, stage "m"), is an internal connection between stage "m-1" and stage "m" of the ring 1. And the output $Bo(1,2m+1)$ of the stage (ring 1, stage "m") is connected to the input $Ui(1,2m-1)$ of the stage (ring 1, stage "m-1"), is another internal connection between stage "m-1" and stage "m" of the ring 1

10 Just the same way the stages (ring 1, stage 0), (ring 1, stage 1), there are also stages (ring 1, stage 2), (ring 1, stage 3), ... (ring 1, stage "m-1"), (ring 1, stage "m") in that order, where the stages from (ring 1, stage 2), (ring 1, stage 3), ... , (ring 1, stage "m-2") are not shown in the diagram 100B. Just the same way the two successive stages (ring 1, stage 0) and (ring 1, stage 1) have internal connections between them as described
15 before, any two successive stages have similar internal connections. For example (ring 1, stage 1) and (ring 1, stage 2) have similar internal connections and (ring 1, stage "m-2") and (ring 1, stage "m-1") have similar internal connections.

Stage (ring 1, stage 0) is also called hereinafter the "entry stage" or "first stage" of ring 1, since inlet links and outlet links of the computational block are directly connected
20 to stage (ring 1, stage 0). Also stage (ring 1, stage "m") is hereinafter the "last stage" or "root stage" of ring 1.

The stage (ring 2, stage 0) consists of 4 inputs namely $Fi(2,1)$, $Fi(2,2)$, $Ui(2,1)$, and $Ui(2,2)$; and 4 outputs $Bo(2,1)$, $Bo(2,2)$, $Fo(2,1)$, and $Fo(2,2)$. The stage (ring 2, stage 0) also consists of six 2:1 Muxes namely $F(2,1)$, $F(2,2)$, $U(2,1)$, $U(2,2)$, $B(2,1)$, and
25 $B(2,2)$. The 2:1 Mux $F(2,1)$ has two inputs namely $Fi(2,1)$ and $Fi(2,2)$ and has one output $Fo(2,1)$. The 2:1 Mux $F(2,2)$ has two inputs namely $Fi(2,1)$ and $Fi(2,2)$ and has one output $Fo(2,2)$.

The 2:1 Mux $U(2,1)$ has two inputs namely $Ui(2,1)$ and $Fo(2,1)$ and has one output $Uo(2,1)$. The 2:1 Mux $U(2,2)$ has two inputs namely $Ui(2,2)$ and $Fo(2,2)$ and has
30 one output $Uo(2,2)$. The 2:1 Mux $B(2,1)$ has two inputs namely $Uo(2,1)$ and $Uo(2,2)$ and

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

has one output $Bo(2,1)$. The 2:1 Mux $B(2,2)$ has two inputs namely $Uo(2,1)$ and $Uo(2,2)$ and has one output $Bo(2,2)$.

The stage (ring 2, stage 1) consists of 4 inputs namely $Fi(2,3)$, $Fi(2,4)$, $Ui(2,3)$, and $Ui(2,4)$; and 4 outputs $Bo(2,3)$, $Bo(2,4)$, $Fo(2,3)$, and $Fo(2,4)$. The stage (ring 2, stage 5 1) also consists of six 2:1 Muxes namely $F(2,3)$, $F(2,4)$, $U(2,3)$, $U(2,4)$, $B(2,3)$, and $B(2,4)$. The 2:1 Mux $F(2,3)$ has two inputs namely $Fi(2,3)$ and $Fi(2,4)$ and has one output $Fo(2,3)$. The 2:1 Mux $F(2,4)$ has two inputs namely $Fi(2,3)$ and $Fi(2,4)$ and has one output $Fo(2,4)$.

The 2:1 Mux $U(2,3)$ has two inputs namely $Ui(2,3)$ and $Fo(2,3)$ and has one 10 output $Uo(2,3)$. The 2:1 Mux $U(2,4)$ has two inputs namely $Ui(2,4)$ and $Fo(2,4)$ and has one output $Uo(2,4)$. The 2:1 Mux $B(2,3)$ has two inputs namely $Uo(2,3)$ and $Uo(2,4)$ and has one output $Bo(2,3)$. The 2:1 Mux $B(2,4)$ has two inputs namely $Uo(2,3)$ and $Uo(2,4)$ and has one output $Bo(2,4)$.

The output $Fo(2,1)$ of the stage (ring 2, stage 0) is connected to the input $Fi(2,3)$ 15 of the stage (ring 2, stage 1), is an internal connection between stage 0 and stage 1 of the ring 2. And the output $Bo(2,3)$ of the stage (ring 2, stage 1) is connected to the input $Ui(2,1)$ of the stage (ring 2, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1..

The stage (ring 2, stage "n-1") consists of 4 inputs namely $Ri(2,2n-1)$, $Ri(2,2n)$, 20 $Ui(1,2n-1)$, and $Ui(1,2n)$; and 4 outputs $Bo(1,2n-1)$, $Bo(1,2n)$, $Fo(1,2n-1)$, and $Fo(1,2n)$. The stage (ring 2, stage "n-1") also consists of eight 2:1 Muxes namely $R(2,2n-1)$, $R(2,2n)$, $F(2,2n-1)$, $F(1,2n)$, $U(1,2n-1)$, $U(1,2n)$, $B(1,2n-1)$, and $B(1,2n)$. The 2:1 Mux $R(2,2n-1)$ has two inputs namely $Ri(2,2n-1)$ and $Bo(2,2n-1)$ and has one output $Ro(2,2n-1)$. The 2:1 Mux $R(2,2n)$ has two inputs namely $Ri(2,2n)$ and $Bo(2,2n)$ and has one output 25 $Ro(2,2n)$. The 2:1 Mux $F(2,2n-1)$ has two inputs namely $Ro(2,2n-1)$ and $Ro(2,2n)$ and has one output $Fo(2,2n-1)$. The 2:1 Mux $F(2,2n)$ has two inputs namely $Ro(2,2n-1)$ and $Ro(2,2n)$ and has one output $Fo(2,2n)$.

The 2:1 Mux $U(2,2n-1)$ has two inputs namely $Ui(2,2n-1)$ and $Fo(2,2n-1)$ and has one output $Uo(2,2n-1)$. The 2:1 Mux $U(2,2n)$ has two inputs namely $Ui(2,2n)$ and 30 $Fo(2,2n)$ and has one output $Uo(2,2n)$. The 2:1 Mux $B(2,2n-1)$ has two inputs namely

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

$U_o(2,2n-1)$ and $U_o(2,2n)$ and has one output $B_o(2,2n-1)$. The 2:1 Mux $B(2,2n)$ has two inputs namely $U_o(2,2n-1)$ and $U_o(2,2n)$ and has one output $B_o(2,2n)$.

The stage (ring 2, stage “n”) consists of 4 inputs namely $R_i(2,2n+1)$, $R_i(2,2n+2)$, $U_i(2,2n+1)$, and $U_i(2,2n+2)$; and 4 outputs $B_o(2,2n+1)$, $B_o(2,2n+2)$, $F_o(2,2n+1)$, and $F_o(2,2n+2)$. The stage (ring 2, stage “n”) also consists of eight 2:1 Muxes namely
 5 $R(2,2n+1)$, $R(2,2n+2)$, $F(2,2n+1)$, $F(2,2n+2)$, $U(2,2n+1)$, $U(2,2n+2)$, $B(2,2n+1)$, and $B(2,2n+2)$. The 2:1 Mux $R(2,2n+1)$ has two inputs namely $R_i(2,2n+1)$ and $B_o(2,2n+1)$ and has one output $R_o(2,2n+1)$. The 2:1 Mux $R(2,2n+2)$ has two inputs namely $R_i(2,2n+2)$ and $B_o(2,2n+2)$ and has one output $R_o(2,2n+2)$. The 2:1 Mux $F(2,2n+1)$ has
 10 two inputs namely $R_o(2,2n+1)$ and $R_o(2,2n+2)$ and has one output $F_o(2,2n+1)$. The 2:1 Mux $F(2,2n+2)$ has two inputs namely $R_o(2,2n+1)$ and $R_o(2,2n+2)$ and has one output $F_o(2,2n+2)$.

The 2:1 Mux $U(2,2n+1)$ has two inputs namely $U_i(2,2n+1)$ and $F_o(2,2n+1)$ and has one output $U_o(2,2n+1)$. The 2:1 Mux $U(2,2n+2)$ has two inputs namely $U_i(2,2n+2)$ and $F_o(2,2n+2)$ and has one output $U_o(2,2n+2)$. The 2:1 Mux $B(2,2n+1)$ has two inputs
 15 namely $U_o(2,2n+1)$ and $U_o(2,2n+2)$ and has one output $B_o(2,2n+1)$. The 2:1 Mux $B(2,2n+2)$ has two inputs namely $U_o(2,2n+1)$ and $U_o(2,2n+2)$ and has one output $B_o(2,2n+2)$.

The output $F_o(2,2n-1)$ of the stage (ring 2, stage “n-1”) is connected to the input
 20 $R_i(2,2n+1)$ of the stage (ring 2, stage “n”), is an internal connection between stage “n-1” and stage “n” of the ring 1. And the output $B_o(2,2n+1)$ of the stage (ring 2, stage “n”) is connected to the input $U_i(2,2n-1)$ of the stage (ring 2, stage “n-1”), is another internal connection between stage “n-1” and stage “n” of the ring 1.

Each stage of any ring of the partial multi-stage hierarchical network
 25 $V_{Comb}(N_1, N_2, d, s)$ 100B consists of $2 * d = 4$ outputs. Even though each stage has four 4:1 muxes, in other embodiments any of these stages can be one of the four by four switch diagrams namely 200A of FIG. 2A, 200B of FIG. 2B, 200C of FIG. 2C, and one of the eight by four switch diagrams namely 200E of FIG. 2E, 200F of FIG. 2F.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

In general, any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ may have inputs and outputs connected from computational block from either only from left-hand side as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A; or only from right-hand side; or from both left-hand and right-

5 hand sides as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B.

Referring to diagram 100C in FIG. 1C, in one embodiment, an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ where $N_1 = 400$; $N_2 = 1600$; $d = 2$; and $s = 1$ corresponding to one computational block, with each computational block having 16 inlet links namely I1, I2, I3, I4, I5, I6, I7, I8, I9, I10, I11, I12, I13, I14, I15,

10 and I16; and 4 outlet links namely O1, O2, O3, and O4. And for each computational block the corresponding partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C consists of two slices namely slice 1 and slice 2. Slice 1 consists of two rings namely (slice 1, ring 1) and (slice 1, ring 2). Similarly slice 2 consists of two rings namely (slice 2, ring 1) and (slice 2, ring 2).

15 The ring (slice 1, ring 1) consists of “m+1” stages namely (slice 1, ring 1, stage 0), (slice 1, ring 1, stage 1), ... (slice 1, ring 1, stage “m-1”), and (slice 1, ring 1, stage “m”). And the ring (slice 1, ring 2) consists of “n+1” stages namely (slice 1, ring 2, stage 0), (slice 1, ring 2, stage 1), ... (slice 1, ring 2, stage “n-1”), and (slice 1, ring 2, stage “n”), where “m” and “n” are positive integers.

20 Similarly the ring (slice 2, ring 1) consists of “x+1” stages namely (slice 2, ring 1, stage 0), (slice 2, ring 1, stage 1), ... (slice 2, ring 1, stage “x-1”), and (slice 2, ring 1, stage “x”). And the ring (slice 2, ring 2) consists of “y+1” stages namely (slice 2, ring 2, stage 0), (slice 2, ring 2, stage 1), ... (slice 2, ring 2, stage “y-1”), and (slice 2, ring 2, stage “y”), where “x” and “y” are positive integers.

25 In general “m” may be or may not be equal to “x” and “n” may be or may not be equal to “y”. Also in general, “m” may be or may not be equal to “n” and “x” may be or may not be equal to “y”.

Ring (slice 1, ring 1) has inlet links $Ri(1,1,1)$ and $Ri(1,1,2)$ from the left-hand side, and has outlet links $Bo(1,1,1)$ and $Bo(1,1,2)$ from left-hand side. Ring (slice 1, ring

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

1) also has inlet links $U_i(1,1,2m+1)$ and $U_i(1,1,2m+2)$ from the right-hand side, and has outlet links $F_o(1,1,2m+1)$ and $F_o(1,1,2m+2)$ from right-hand side. Ring (slice 1, ring 2) has inlet links $R_i(1,2,1)$ and $R_i(1,2,2)$ from left-hand side, and outlet links $B_o(1,2,1)$ and $B_o(1,2,2)$ from left-hand side. Ring (slice 1, ring 2) also has inlet links $U_i(1,2,2n+1)$ and $U_i(1,2,2n+2)$ from the right-hand side, and has outlet links $F_o(1,2,2n+1)$ and $F_o(1,2,2n+2)$ from right-hand side.

Ring (slice 2, ring 1) has inlet links $R_i(2,1,1)$ and $R_i(2,1,2)$ from the left-hand side, and has outlet links $B_o(2,1,1)$ and $B_o(2,1,2)$ from left-hand side. Ring (slice 2, ring 1) also has inlet links $U_i(2,1,2x+1)$ and $U_i(2,1,2x+2)$ from the right-hand side, and has outlet links $F_o(2,1,2x+1)$ and $F_o(2,1,2x+2)$ from right-hand side. Ring (slice 2, ring 2) has inlet links $R_i(2,2,1)$ and $R_i(2,2,2)$ from left-hand side, and outlet links $B_o(2,2,1)$ and $B_o(2,2,2)$ from left-hand side. Ring (slice 2, ring 2) also has inlet links $U_i(2,2,2y+1)$ and $U_i(2,2,2y+2)$ from the right-hand side, and has outlet links $F_o(2,2,2y+1)$ and $F_o(2,2,2y+2)$ from right-hand side.

15 And the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C consists of 16 inlet links and 4 outlet links corresponding to the two slices slice 1 and slice 2. From left-hand side, outlet link O1 of the computational block is connected to inlet link $R_i(1,1,1)$ of ring (slice 1, ring 1) and also inlet link of $R_i(1,2,1)$ of ring (slice 1, ring 2). Similarly from left-hand side, outlet link O2 of the computational block is connected to inlet link $R_i(1,1,2)$ of Ring (slice 1, ring 1) and also inlet link of $R_i(1,2,2)$ of Ring (slice 20 1, ring 2). And from left-hand side, outlet link $B_o(1,1,1)$ of Ring (slice 1, ring 1) is connected to inlet link I1 of the computational block. From left-hand side, Outlet link $B_o(1,1,2)$ of Ring (slice 1, ring 1) is connected to inlet link I2 of the computational block. Similarly from left-hand side, outlet link $B_o(1,2,1)$ of Ring (slice 1, ring 2) is connected to inlet link I3 of the computational block. From left-hand side, outlet link $B_o(1,2,2)$ of Ring (slice 1, ring 2) is connected to inlet link I4 of the computational block.

From right-hand side, outlet link O1 of the computational block is connected to inlet link $U_i(1,1,2m+1)$ of ring (slice 1, ring 1) and also inlet link of $U_i(1,2,2n+1)$ of ring (slice 1, ring 2). Similarly from right-hand side, outlet link O2 of the computational block is connected to inlet link $U_i(1,1,2m+2)$ of Ring (slice 1, ring 1) and also inlet link of $U_i(1,2,2n+2)$ of Ring (slice 1, ring 2). And from right-hand side, outlet link $F_o(1,1,2m+1)$

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

of Ring (slice 1, ring 1) is connected to inlet link I5 of the computational block. From right-hand side, outlet link $Fo(1,1,2m+2)$ of Ring (slice 1, ring 1) is connected to inlet link I6 of the computational block. Similarly from right-hand side, outlet link $Fo(1,2,2n+1)$ of Ring (slice 1, ring 2) is connected to inlet link I7 of the computational block. From right-hand side, outlet link $Fo(1,2,2n+2)$ of Ring (slice 1, ring 2) is connected to inlet link I8 of the computational block.

From left-hand side, outlet link O3 of the computational block is connected to inlet link $Ri(2,1,1)$ of ring (slice 2, ring 1) and also inlet link of $Ri(2,2,1)$ of ring (slice 2, ring 2). Similarly from left-hand side, outlet link O4 of the computational block is connected to inlet link $Ri(2,1,2)$ of Ring (slice 2, ring 1) and also inlet link of $Ri(2,2,2)$ of Ring (slice 2, ring 2). And from left-hand side, outlet link $Bo(2,1,1)$ of Ring (slice 2, ring 1) is connected to inlet link I9 of the computational block. From left-hand side, Outlet link $Bo(2,1,2)$ of Ring (slice 2, ring 1) is connected to inlet link I10 of the computational block. Similarly from left-hand side, outlet link $Bo(2,2,1)$ of Ring (slice 2, ring 2) is connected to inlet link I11 of the computational block. From left-hand side, outlet link $Bo(2,2,2)$ of Ring (slice 2, ring 2) is connected to inlet link I12 of the computational block.

From right-hand side, outlet link O3 of the computational block is connected to inlet link $Ui(2,1,2x+1)$ of ring (slice 2, ring 1) and also inlet link of $Ui(2,2,2y+1)$ of ring (slice 2, ring 2). Similarly from right-hand side, outlet link O4 of the computational block is connected to inlet link $Ui(2,1,2x+2)$ of Ring (slice 2, ring 1) and also inlet link of $Ui(2,2,2y+2)$ of Ring (slice 2, ring 2). And from right-hand side, outlet link $Fo(2,1,2x+1)$ of Ring (slice 2, ring 1) is connected to inlet link I13 of the computational block. From right-hand side, outlet link $Fo(2,1,2x+2)$ of Ring (slice 2, ring 1) is connected to inlet link I14 of the computational block. Similarly from right-hand side, outlet link $Fo(2,2,2y+1)$ of Ring (slice 2, ring 2) is connected to inlet link I15 of the computational block. From right-hand side, outlet link $Fo(2,2,2y+2)$ of Ring (slice 2, ring 2) is connected to inlet link I16 of the computational block.

In this embodiment outlet links O1 and O2 of the computational block are connected only to slice 1. Similarly outlet links O3 and O4 of the computational block are connected only to slice 2.

AMENDMENT AFTER ALLOWANCE UNDER RULE 312, Contd.

Referring to two dimensional grid 800 in FIG. 8 illustrates, in another embodiment, each block of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C with 4 inlet links and 16 outlet links and the corresponding computational block with 16 inlet links and 4 outlet links. For example

5 block (1,1) of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C with 4 inlet links and 16 outlet links and the corresponding computational block with 16 inlet links and 4 outlet links. Similarly each of the 100 blocks of 2D-grid 800 has a separate partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C with 4 inlet links and 16 outlet links and the corresponding

10 computational block with 16 inlet links and 4 outlet links. Hence the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to 2D-grid 800 has $N_1 = 400$ inlet links and $N_2 = 1600$ outlet links. Since there are 100 computational blocks each one corresponding to one of the blocks with each computational block having 16 inlet links and 4 outlet links. Also the 2D-grid 800 is organized in the fourth quadrant of the 2D-

15 Plane. In other embodiments the 2D-grid 800 may be organized as either first quadrant, or second quadrant or third quadrant of the 2D-Plane.

Referring to partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C, the stage (slice 1, ring 1, stage 0) consists of 8 inputs namely $Ri(1,1,1)$, $Ri(1,1,2)$, $Ui(1,1,1)$, $Ui(1,1,2)$, $J(1,1,1)$, $K(1,1,1)$, $L(1,1,1)$, and $M(1,1,1)$; and 4 outputs

20 $Bo(1,1,1)$, $Bo(1,1,2)$, $Fo(1,1,1)$, and $Fo(1,1,2)$. The stage (slice 1, ring "1", stage "0") also consists of four 4:1 Muxes namely $F(1,1,1)$, $F(1,1,2)$, $B(1,1,1)$, and $B(1,1,2)$. The 4:1 Mux $F(1,1,1)$ has four inputs namely $Ri(1,1,1)$, $Ri(1,1,2)$, $Ui(1,1,2)$, and $J(1,1,1)$, and has one output $Fo(1,1,1)$. The 4:1 Mux $F(1,1,2)$ has four inputs namely $Ri(1,1,1)$, $Ri(1,1,2)$, $Ui(1,1,1)$, and $K(1,1,1)$, and has one output $Fo(1,1,2)$.

25 The 4:1 Mux $B(1,1,1)$ has four inputs namely $Ui(1,1,1)$, $Ui(1,1,2)$, $Ri(1,1,2)$, and $L(1,1,1)$, and has one output $Bo(1,1,1)$. The 4:1 Mux $B(1,1,2)$ has four inputs namely $Ui(1,1,1)$, $Ui(1,1,2)$, $Ri(1,1,1)$ and $M(1,1,1)$, and has one output $Bo(1,1,2)$. In different embodiments the inputs $J(1,1,1)$, $K(1,1,1)$, $L(1,1,1)$, and $M(1,1,1)$ are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical

30 network $V_{Comb}(N_1, N_2, d, s)$.