The stage (slice 1, ring 1, stage "m") consists of 8 inputs namely Ri(1,1,2m+1), Ri(1,1,2m+2), Ui(1,1,2m+1), Ui(1,1,2m+2), J(1,1,m+1), K(1,1,m+1), L(1,1,m+1), and M(1,1,m+1); and 4 outputs Bo(1,1,2m+1), Bo(1,1,2m+2), Fo(1,1,2m+1), and Fo(1,1,2m+2). The stage (slice 1, ring 1, stage "m") also consists of four 4:1 Muxes namely F(1,1,2m+1), F(1,1,2m+2), B(1,1,2m+1), and B(1,1,2m+2). The 4:1 Mux F(1,1,2m+1) has four inputs namely Ri(1,1,2m+1), Ri(1,1,2m+2), Ui(1,1,2m+2), and J(1,1,m+1), and has one output Fo(1,1,2m+1). The 4:1 Mux F(1,1,2m+2) has four inputs namely Ri(1,1,2m+1), Ri(1,1,2m+2), Ui(1,1,2m+1), and K(1,1,m+1), and has one output Fo(1,1,2m+2).

The 4:1 Mux B(1,1,2m+1) has four inputs namely Ui(1,1,2m+1), Ui(1,1,2m+2), Ri(1,1,2m+2), and L(1,1,m+1), and has one output Bo(1,1,2m+1). The 4:1 Mux B(1,1,2m+2) has four inputs namely Ui(1,1,2m+1), Ui(1,1,2m+2), Ri(1,1,2m+1) and M(1,1,m+1), and has one output Bo(1,1,2m+2). In different embodiments the inputs J(1,1,m+1), K(1,1,m+1), L(1,1,m+1), and M(1,1,m+1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 1, ring 1, stage 0), there are also stages (slice 1, ring 1, stage 1), (slice 1, ring 1, stage 2), (slice 1, ring 1, stage 3), ... (slice 1, ring 1, stage "m-1"), (slice 1, ring 1, stage "m") in that order, where the stages from (slice 1, ring 1, stage 1), (slice 1, ring 1, stage 2), ... , (slice 1, ring 1, stage "m-1") are not shown in the diagram 100C.

Referring to diagram 100C5 in FIG. 1C5 illustrates specific details of partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C, particularly the internal connections between two successive stages of any ring of any slice, in one embodiment. The stage (slice "c", ring "d", stage "e") consists of 8 inputs namely Ri(c,d,2e+1), Ri(c,d,2e+2), Ui(c,d,2e+1), Ui(c,d,2e+2), J(c,d,e+1), K(c,d,e+1), L(c,d,e+1), and M(c,d,e+1); and 4 outputs Bo(c,d,2e+1), Bo(c,d,2e+2), Fo(c,d,2e+1), and Fo(c,d,2e+2). The stage (slice "c", ring "d", stage "e") also consists of four 4:1 Muxes namely F(c,d,2e+1), F(c,d,2e+2), B(c,d,2e+1), and B(c,d,2e+2). The 4:1 Mux F(c,d,2e+1) has four inputs namely Ri(c,d,2e+1), Ri(c,d,2e+2), Ui(c,d,2e+2), and J(c,d,e+1), and has

one output Fo(c,d,2e+1). The 4:1 Mux F(c,d,2e+2) has four inputs namely Ri(c,d,2e+1), Ri(c,d,2e+2), Ui(c,d,2e+1), and K(c,d,e+1), and has one output Fo(c,d,2e+2).

The 4:1 Mux B(c,d,2e+1) has four inputs namely Ui(c,d,2e+1), Ui(c,d,2e+2), Ri(c,d,2e+2), and L(c,d,e+1), and has one output Bo(c,d,2e+1). The 4:1 Mux B(c,d,2e+2) has four inputs namely Ui(c,d,2e+1), Ui(c,d,2e+2), Ri(c,d,2e+1) and M(c,d,e+1), and has one output Bo(c,d,2e+2). In different embodiments the inputs J(c,d,e+1), K(c,d,e+1), L(c,d,e+1), and M(c,d,e+1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice "c", ring "d", stage "e+1") consists of 8 inputs namely Ri(c,d,2e+3), Ri(c,d,2e+4), Ui(c,d,2e+3), Ui(c,d,2e+4), J(c,d,e+2), K(c,d,e+2), L(c,d,e+2), and M(c,d,e+2); and 4 outputs Bo(c,d,2e+3), Bo(c,d,2e+4), Fo(c,d,2e+3), and Fo(c,d,2e+4). The stage (slice "c", ring "d", stage "e+1") also consists of four 4:1 Muxes namely F(c,d,2e+3), F(c,d,2e+4), B(c,d,2e+3), and B(c,d,2e+4). The 4:1 Mux F(c,d,2e+3) has four inputs namely Ri(c,d,2e+3), Ri(c,d,2e+4), Ui(c,d,2e+4), and J(c,d,e+2), and has one output Fo(c,d,2e+3). The 4:1 Mux F(c,d,2e+4) has four inputs namely Ri(c,d,2e+3), Ri(c,d,2e+4), Ui(c,d,2e+3), and K(c,d,e+2), and has one output Fo(c,d,2e+4).

The 4:1 Mux B(c,d,2e+3) has four inputs namely Ui(c,d,2e+3), Ui(c,d,2e+4), Ri(c,d,2e+4), and L(c,d,e+2), and has one output Bo(c,d,2e+3). The 4:1 Mux B(c,d,2e+4) has four inputs namely Ui(c,d,2e+3), Ui(c,d,2e+4), Ri(c,d,2e+3) and M(c,d,e+2), and has one output Bo(c,d,2e+4). In different embodiments the inputs J(c,d,e+2), K(c,d,e+2), L(c,d,e+2), and M(c,d,e+2) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The output Fo(c,d,2e+1) of the stage (slice "c", ring "d", stage "e") is connected to the input Ri(c,d,2e+3) of the stage (slice "c", ring "d", stage "e+1") which is called hereinafter an internal connection between two successive stages of a ring. And the output Bo(c,d,2e+3) of the stage (slice "c", ring "d", stage "e+1") is connected to the input Ui(c,d,2e+1) of the stage (slice "c", ring "d", stage "e"), is another internal connection between stage "e" and stage "e+1" of the ring (slice "c", ring "d").

Just the same way the two successive stages (slice "c', ring "d", stage "e") and (slice 'c", ring "d", stage "e+1") have internal connections between them as described above, any two successive stages have similar internal connections for any values of "c", "d", "e" of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C belonging to any block of the two dimensional grid 800 in FIG. 8, in some embodiments. For example stage (slice 1, ring 1, stage 0) and stage (slice 1, ring 1, stage 1) have similar internal connections; and stage (slice 1, ring 1, stage "m-1") and stage (slice 1, ring 1, stage "m") have similar internal connections.

Stage (slice 1, ring 1, stage 0) is also called hereinafter the "entry stage" or "first stage" of (slice 1, ring 1), since inlet links and outlet links of the computational block are directly connected to stage (slice 1, ring 1, stage 0). Also stage (slice 1, ring 1, stage "m") is hereinafter the "last stage" or "root stage" of (slice 1, ring 1).

The stage (slice 1, ring 2, stage 0) consists of 8 inputs namely Ri(1,2,1), Ri(1,2,2), Ui(1,2,1), Ui(1,2,2), J(1,2,1), K(1,2,1), L(1,2,1), and M(1,2,1); and 4 outputs Bo(1,2,1), Bo(1,2,2), Fo(1,2,1), and Fo(1,2,2). The stage (slice 1, ring "2", stage "0") also consists of four 4:1 Muxes namely F(1,2,1), F(1,2,2), B(1,2,1), and B(1,2,2). The 4:1 Mux F(1,2,1) has four inputs namely Ri(1,2,1), Ri(1,2,2), Ui(1,2,2), and J(1,2,1), and has one output Fo(1,2,1). The 4:1 Mux F(1,2,2) has four inputs namely Ri(1,2,1), Ri(1,2,2), Ui(1,2,1), and K(1,2,1), and has one output Fo(1,2,2).

The 4:1 Mux B(1,2,1) has four inputs namely Ui(1,2,1), Ui(1,2,2), Ri(1,2,2), and L(1,2,1), and has one output Bo(1,2,1). The 4:1 Mux B(1,2,2) has four inputs namely Ui(1,2,1), Ui(1,2,2), Ri(1,2,1) and M(1,2,1), and has one output Bo(1,2,2). In different embodiments the inputs J(1,2,1), K(1,2,1), L(1,2,1), and M(1,2,1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 1, ring 2, stage "n") consists of 8 inputs namely Ri(1,2,2n+1), Ri(1,2,2n+2), Ui(1,2,2n+1), Ui(1,2,2n+2), J(1,2,n+1), K(1,2,n+1), L(1,2,n+1), and M(1,2,n+1); and 4 outputs Bo(1,2,2n+1), Bo(1,2,2n+2), Fo(1,2,2n+1), and Fo(1,2,2n+2). The stage (slice 1, ring 2, stage "n") also consists of four 4:1 Muxes namely F(1,2,2n+1), F(1,2,2n+2), B(1,2,2n+1), and B(1,2,2n+2). The 4:1 Mux F(1,2,2n+1) has four inputs

namely Ri(1,2,2n+1), Ri(1,2,2n+2), Ui(1,2,2n+2), and J(1,2,n+1), and has one output Fo(1,2,2n+1). The 4:1 Mux F(1,2,2n+2) has four inputs namely Ri(1,2,2n+1), Ri(1,2,2n+2), Ui(1,2,2n+1), and K(1,2,n+1), and has one output Fo(1,2,2n+2).

The 4:1 Mux B(1,2,2n+1) has four inputs namely Ui(1,2,n+1), Ui(1,2,2n+2), Ri(1,2,2n+2), and L(1,2,n+1), and has one output Bo(1,2,2n+1). The 4:1 Mux B(1,2,2n+2) has four inputs namely Ui(1,2,2n+1), Ui(1,2,2n+2), Ri(1,2,2n+1) and M(1,2,n+1), and has one output Bo(1,2,2n+2). In different embodiments the inputs J(1,2,n+1), K(1,2,n+1), L(1,2,n+1), and M(1,2,n+1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 1, ring 2, stage 0), there are also stages (slice 1, ring 2, stage 1), (slice 1, ring 2, stage 2), (slice 1, ring 2, stage 3), ... (slice 1, ring 2, stage "n-1"), (slice 1, ring 2, stage "n") in that order, where the stages from (slice 1, ring 2, stage 1), (slice 1, ring 2, stage 2), ... , (slice 1, ring 2, stage "n-1") are not shown in the diagram 100C.

The stage (slice 2, ring 1, stage 0) consists of 8 inputs namely Ri(2,1,1), Ri(2,1,2), Ui(2,1,1), Ui(2,1,2), J(2,1,1), K(2,1,1), L(2,1,1), and M(2,1,1); and 4 outputs Bo(2,1,1), Bo(2,1,2), Fo(2,1,1), and Fo(2,1,2). The stage (slice 2, ring "1", stage "0") also consists of four 4:1 Muxes namely F(2,1,1), F(2,1,2), B(2,1,1), and B(2,1,2). The 4:1 Mux F(2,1,1) has four inputs namely Ri(2,1,1), Ri(2,1,2), Ui(2,1,2), and J(2,1,1), and has one output Fo(2,1,1). The 4:1 Mux F(2,1,2) has four inputs namely Ri(2,1,1), Ri(2,1,2), Ui(2,1,1), and K(2,1,1), and has one output Fo(2,1,2).

The 4:1 Mux B(2,1,1) has four inputs namely Ui(2,1,1), Ui(2,1,2), Ri(2,1,2), and L(2,1,1), and has one output Bo(2,1,1). The 4:1 Mux B(2,1,2) has four inputs namely Ui(2,1,1), Ui(2,1,2), Ri(2,1,1) and M(2,1,1), and has one output Bo(2,1,2). In different embodiments the inputs J(2,1,1), K(2,1,1), L(2,1,1), and M(2,1,1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 2, ring 1, stage "x") consists of 8 inputs namely Ri(2,1,2x+1), Ri(2,1,2x+2), Ui(2,1,2x+1), Ui(2,1,2x+2), J(2,1,x+1), K(2,1,x+1), L(2,1,x+1), and M(2,1,x+1); and 4 outputs Bo(2,1,2x+1), Bo(2,1,2x+2), Fo(2,1,2x+1), and Fo(2,1,2x+2). The stage (slice 2, ring 1, stage "x") also consists of four 4:1 Muxes namely F(2,1,2x+1), F(2,1,2x+2), B(2,1,2x+1), and B(2,1,2x+2). The 4:1 Mux F(2,1,2x+1) has four inputs namely Ri(2,1,2x+1), Ri(2,1,2x+2), Ui(2,1,2x+2), and J(2,1,x+1), and has one output Fo(2,1,2x+1). The 4:1 Mux F(2,1,2x+2) has four inputs namely Ri(2,1,2x+1), Ri(2,1,2x+2), Ui(2,1,2x+1), and K(2,1,x+1), and has one output Fo(2,1,2x+2).

The 4:1 Mux B(2,1,2x+1) has four inputs namely Ui(2,1,2x+1), Ui(2,1,2x+2), Ri(2,1,2x+2), and L(2,1,x+1), and has one output Bo(2,1,2x+1). The 4:1 Mux B(2,1,2x+2) has four inputs namely Ui(2,1,2x+1), Ui(2,1,2x+2), Ri(2,1,2x+1) and M(2,1,x+1), and has one output Bo(2,1,2x+2). In different embodiments the inputs J(2,1,x+1), K(2,1,x+1), L(2,1,x+1), and M(2,1,x+1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 2, ring 1, stage 0), there are also stages (slice 2, ring 1, stage 1), (slice 2, ring 1, stage 2), (slice 2, ring 1, stage 3), ... (slice 2, ring 1, stage "m-1"), (slice 2, ring 1, stage "x") in that order, where the stages from (slice 2, ring 1, stage 1), (slice 2, ring 1, stage 2), ... , (slice 2, ring 1, stage "x-1") are not shown in the diagram 100C.

The stage (slice 2, ring 2, stage 0) consists of 8 inputs namely Ri(2,2,1), Ri(2,2,2), Ui(2,2,1), Ui(2,2,2), J(2,2,1), K(2,2,1), L(2,2,1), and M(2,2,1); and 4 outputs Bo(2,2,1), Bo(2,2,2), Fo(2,2,1), and Fo(2,2,2). The stage (slice 2, ring "2", stage "0") also consists of four 4:1 Muxes namely F(2,2,1), F(2,2,2), B(2,2,1), and B(2,2,2). The 4:1 Mux F(2,2,1) has four inputs namely Ri(2,2,1), Ri(2,2,2), Ui(2,2,2), and J(2,2,1), and has one output Fo(2,2,1). The 4:1 Mux F(2,2,2) has four inputs namely Ri(2,2,1), Ri(2,2,2), Ui(2,2,1), and K(2,2,1), and has one output Fo(2,2,2).

The 4:1 Mux B(2,2,1) has four inputs namely Ui(2,2,1), Ui(2,2,2), Ri(2,2,2), and L(2,2,1), and has one output Bo(2,2,1). The 4:1 Mux B(2,2,2) has four inputs namely Ui(2,2,1), Ui(2,2,2), Ri(2,2,1) and M(2,2,1), and has one output Bo(2,2,2). In different

embodiments the inputs J(2,2,1), K(2,2,1), L(2,2,1), and M(2,2,1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 2, ring 2, stage "x") consists of 8 inputs namely Ri(2,2,2x+1), Ri(2,2,2x+2), Ui(2,2,2x+1), Ui(2,2,2x+2), J(2,2,x+1), K(2,2,x+1), L(2,2,x+1), and M(2,2,x+1); and 4 outputs Bo(2,2,2x+1), Bo(2,2,2x+2), Fo(2,2,2x+1), and Fo(2,2,2x+2). The stage (slice 2, ring 2, stage "y") also consists of four 4:1 Muxes namely F(2,2,2y+1), F(2,2,2y+2), B(2,2,2y+1), and B(2,2,2y+2). The 4:1 Mux F(2,2,2y+1) has four inputs namely Ri(2,2,2y+1), Ri(2,2,2y+2), Ui(2,2,2y+2), and J(2,2,y+1), and has one output Fo(2,2,2y+1). The 4:1 Mux F(2,2,2y+2) has four inputs namely Ri(2,2,2y+1), Ri(2,2,2y+2), Ui(2,2,2y+1), and K(2,2,y+1), and has one output Fo(2,2,2y+2).

The 4:1 Mux B(2,2,2y+1) has four inputs namely Ui(2,2,2y+1), Ui(2,2,2y+2), Ri(2,2,2y+2), and L(2,2,y+1), and has one output Bo(2,2,2y+1). The 4:1 Mux B(2,2,2y+2) has four inputs namely Ui(2,2,2y+1), Ui(2,2,2y+2), Ri(2,2,2y+1) and M(2,2,y+1), and has one output Bo(2,2,2y+2). In different embodiments the inputs J(2,2,y+1), K(2,2,y+1), L(2,2,y+1), and M(2,2,y+1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 2, ring 2, stage 0), there are also stages (slice 2, ring 2, stage 1), (slice 2, ring 2, stage 2), (slice 2, ring 2, stage 3), … (slice 2, ring 2, stage "y-1"), (slice 2, ring 2, stage "y") in that order, where the stages from (slice 2, ring 2, stage 1), (slice 2, ring 2, stage 2), … , (slice 2, ring 2, stage "y-1") are not shown in the diagram 100C.

As illustrated in diagram 100C5 in FIG. 1C5, the similar internal connections between two successive stages of any ring of any slice of partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C, in some embodiments are provided for all the slices c = 1, 2; for all the rings in each of the slices d = 1, 2; and for all the stages namely when c = 1, d = 1, e = [1,m]; when c=1, d=2, e=[1,n]; when c=2, d=1, e=[1,x]; and when c=2, d=2; e=[1,y].

Each stage of any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of $2 * d = 4$ outputs. Even though each stage has four 4:1 muxes, in other embodiments any of these stages can be one of the four by four switch diagrams namely 200A of FIG. 2A, 200B of FIG. 2B, 200C of FIG. 2C, and one of the eight by four switch diagrams namely 200E of FIG. 2E, 200F of FIG. 2F.

In general, any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ illustrated in 100C also may have inputs and outputs connected from computational block from either only from left-hand side as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A; or only from right-hand side; or from both left-hand and right-hand sides as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B.

Applicant now notes a few aspects of the diagram 100C in FIG. 1C an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to one computational block, with each computational block having 16 inlet links and 4 outlet links as follows: (Also these aspects are helpful in more optimization of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ as well as faster scheduling of the connections between outlet links of the computational blocks and the inlet links of the computational blocks.)

1) The partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C is divided into two slices namely slice 1 and slice 2. The outlet links of the computational block namely O1 and O2 are connected to only one slice i.e. slice 1. In other words outlet links O1 and O2 are absolutely not connected to slice 2. Similarly the outlet links of the computational block namely O3 and O4 are connected to only one slice i.e. slice 2. In other words outlet links O3 and O4 are absolutely not connected to slice 1. 2) The second aspect is all the hop wires and multi-drop hop wires originating from slice 1 from any block will be terminating only in the slice 1 of any other block. Similarly all the hop wires and multi-drop hop wires originating from slice 2 from any block will be terminating only in the slice 2 of any other block. 3) The third aspect is the mux whose output is directly connected to each inlet link of the computational block must have at

least one input connected from each slice of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C. That is for example since the 4:1 mux B(1,1,1), belonging to slice 1, and having its output Bo(1,1,1) directly connected to inlet link I1 must have at least one of its inputs connecting from an output of a mux of a stage of a ring of slice 2 as well. This property must be satisfied for all the inlet links of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C.

Referring to diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 illustrate the details of the foregoing third aspect of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C. Applicant notes that diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 are all actually part of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C and these separate diagrams are necessary only to avoid the clutter in the diagram 100C of FIG. 1C.

The connections illustrated between different slices in diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 are the only connections between different slices, in some exemplary embodiments. In general the connections between different slices are given only at the terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block.

Referring to diagram 100C1 in FIG. 1C1 illustrate the connections between the stage (slice 1, ring 1, stage 0) and between the stage (slice 2, ring 1, stage 0). The same connection that is given to the input Ui(1,1,1) is also connected to the input L(2,1,1). The same connection that is given to the input Ui(1,1,2) is also connected to the input M(2,1,1). Similarly the same connection that is given to the input Ui(2,1,1) is also connected to the input L(1,1,1). The same connection that is given to the input Ui(2,1,2) is also connected to the input M(1,1,1).

Therefore inlet link I1 can be essentially connected through the 4:1 mux B(1,1,1) with three of its inputs connecting from slice 1 namely Ui(1,1,1), Ui(1,1,2), Ri(1,1,2) and one input L(1,1,1) connecting from slice 2. The inlet link I2 can be essentially connected

through the 4:1 mux B(1,1,2) with three of its inputs connecting from slice 1 namely Ui(1,1,1), Ui(1,1,2), Ri(1,1,1) and one input M(1,1,1) connecting from slice 2. The inlet link I9 can be essentially connected through the 4:1 mux B(1,2,1) with three of its inputs connecting from slice 2 namely Ui(2,1,1), Ui(2,1,2), Ri(2,1,2) and one input L(2,1,1) connecting from slice 1. The inlet link I10 can be essentially connected through the 4:1 mux B(2,1,2) with three of its inputs connecting from slice 2 namely Ui(2,1,1), Ui(2,1,2), Ri(2,1,1) and one input M(2,1,1) connecting from slice 1. Hence all the inlet links I1, I2, I9 and I10 are all independently reachable from both slice 1 and slice2.

Referring to diagram 100C2 in FIG. 1C2 illustrate the connections between the stage (slice 1, ring 2, stage 0) and between the stage (slice 2, ring 2, stage 0). The same connection that is given to the input Ui(1,2,1) is also connected to the input M(2,2,1). The same connection that is given to the input Ui(1,2,2) is also connected to the input L(2,2,1). Similarly the same connection that is given to the input Ui(2,2,1) is also connected to the input M(1,2,1). The same connection that is given to the input Ui(2,2,2) is also connected to the input L(1,2,1).

Therefore inlet link I3 can be essentially connected through the 4:1 mux B(1,2,1) with three of its inputs connecting from slice 1 namely Ui(1,2,1), Ui(1,2,2), Ri(1,2,2) and one input M(2,2,1) connecting from slice 2. The inlet link I4 can be essentially connected through the 4:1 mux B(1,2,2) with three of its inputs connecting from slice 1 namely Ui(1,2,1), Ui(1,2,2), Ri(1,2,1) and one input M(1,2,1) connecting from slice 2. The inlet link I11 can be essentially connected through the 4:1 mux B(2,2,1) with three of its inputs connecting from slice 2 namely Ui(2,2,1), Ui(2,2,2), Ri(2,2,2) and one input L(2,2,1) connecting from slice 1. The inlet link I12 can be essentially connected through the 4:1 mux B(2,2,2) with three of its inputs connecting from slice 2 namely Ui(2,2,1), Ui(2,2,2), Ri(2,2,1) and one input M(2,2,1) connecting from slice 1. Hence all the inlet links I3, I4, I11 and I12 are all independently reachable from both slice 1 and slice2.

Referring to diagram 100C3 in FIG. 1C3 illustrate the connections between the stage (slice 1, ring 1, stage "m") and between the stage (slice 2, ring 2, stage "y"). The same connection that is given to the input Ri(1,1,2m+1) is also connected to the input J(2,2,y+1). The same connection that is given to the input Ri(1,1,2m+2) is also connected to the input K(2,2,y+1). Similarly the same connection that is given to the input

Ri(2,2,2y+1) is also connected to the input J(1,1,m+1). The same connection that is given to the input Ri(2,2,2y+2) is also connected to the input K(1,1,m+1).

Therefore inlet link I5 can be essentially connected through the 4:1 mux F(1,1,2m+1) with three of its inputs connecting from slice 1 namely Ri(1,1,2m+1), Ri(1,1,2m+2), Ui(1,1,2m+2) and one input J(1,1,m+1) connecting from slice 2. The inlet link I6 can be essentially connected through the 4:1 mux F(1,1,2m+2) with three of its inputs connecting from slice 1 namely Ri(1,1,2m+1), Ri(1,1,2m+2),Ui(1,1,2m+1) and one input K(1,1,m+1) connecting from slice 2. The inlet link I15 can be essentially connected through the 4:1 mux F(2,2,2y+1) with three of its inputs connecting from slice 2 namely Ri(2,2,2y+1), Ri(2,2,2y+2), Ui(2,2,2y+2) and one input J(2,2,y+1) connecting from slice 1. The inlet link I16 can be essentially connected through the 4:1 mux F(2,2,2y+2) with three of its inputs connecting from slice 2 namely Ri(2,2,2y+1), Ri(2,2,2y+2), Ui(2,2,2y+1) and one input K(2,2,y+1) connecting from slice 1. Hence all the inlet links I5, I6, I15 and I16 are all independently reachable from both slice 1 and slice2.

Referring to diagram 100C4 in FIG. 1C4 illustrate the connections between the stage (slice 1, ring 2, stage "n") and between the stage (slice 2, ring 1, stage "x"). The same connection that is given to the input Ri(1,2,2n+1) is also connected to the input K(2,1,x+1). The same connection that is given to the input Ri(1,2,2n+2) is also connected to the input J(2,1,x+1). Similarly the same connection that is given to the input Ri(2,1,2x+1) is also connected to the input K(1,2,n+1). The same connection that is given to the input Ri(2,1,2x+2) is also connected to the input J(1,2,n+1).

Therefore inlet link I7 can be essentially connected through the 4:1 mux F(1,2,2n+1) with three of its inputs connecting from slice 1 namely Ri(1,2,2n+1), Ri(1,2,2n+2), Ui(1,2,2n+2) and one input J(1,2,n+1) connecting from slice 2. The inlet link I8 can be essentially connected through the 4:1 mux F(1,2,2n+2) with three of its inputs connecting from slice 1 namely Ri(1,2,2n+1), Ri(1,2,2n+2),Ui(1,2,2n+1) and one input K(1,2,n+1) connecting from slice 2. The inlet link I13 can be essentially connected through the 4:1 mux F(2,1,2x+1) with three of its inputs connecting from slice 2 namely Ri(2,1,2x+1), Ri(2,1,2x+2), Ui(2,1,2x+2) and one input J(2,1,x+1) connecting from slice 1. The inlet link I14 can be essentially connected through the 4:1 mux F(2,1,2x+2) with

three of its inputs connecting from slice 2 namely Ri(2,1,2x+1), Ri(2,1,2x+2), Ui(2,1,2x+1) and one input K(2,1,x+1) connecting from slice 1. Hence all the inlet links I7, I8, I13 and I14 are all independently reachable from both slice 1 and slice2.

The connections illustrated between different slices, in several embodiments, in diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 are the only connections between different slices. And also the terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block have three inputs coming from one slice and one input coming from another slice. In other embodiments it is also possible so that the terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block have two inputs coming from one slice and two inputs coming from another slice.

Also in general the number of slices in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C may be more than or equal to two. In such a case terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block will have at least one input coming from each slice. And the outlet links of the computational block will be divided and connected to each slice; however each outlet link of the computational block will be connected to only one slice. Also in general the hop wires and multi-drop hop wires are connected to only between the corresponding slices of different blocks, in some embodiments some of the hop wires and multi-drop hop wires may be connected between different slices of different blocks even if it is done partially.

FIG. 2A illustrates a stage (ring "k", stage "m") 200A consists of 4 inputs namely Fi(k,2m+1), Fi(k,2m+2), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of six 2:1 Muxes namely F(k,2m+1), F(k,2m+2) (comprising in combination a forward switch), U(k,2m+1), U(k,2m+2) (comprising in combination a U-turn switch), B(k,2m+1), and B(k,2m+2) (comprising in combination a backward switch). The 2:1 Mux F(k,2m+1) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 2B illustrates a stage (ring "k", stage "m") 200B consists of 4 inputs namely Ri(k,2m+1), Ri(k,2m+2), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of eight 2:1 Muxes namely R(k,2m+1), R(k,2m+2) (comprising in combination a Reverse U-turn switch), F(k,2m+1), F(k,2m+2) (comprising in combination a forward switch), U(k,2m+1), U(k,2m+2) (comprising in combination a U-turn switch), B(k,2m+1), and B(k,2m+2) (comprising in combination a backward switch). The 2:1 Mux R(k,2m+1) has two inputs namely Ri(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 2C illustrates a stage (ring "k", stage "m") 200C consists of 4 inputs namely Fi(k,2m+1), Fi(k,2m+2), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Uo(k,2m+1), Uo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of four 2:1 Muxes namely F(k,2m+1), F(k,2m+2) (comprising in combination a forward switch), U(k,2m+1), and U(k,2m+2) (comprising in combination a U-turn switch). The 2:1 Mux F(k,2m+1) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one

output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Ui(k,2m+2) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+1) and Ui(k,2m+2) and has one output Uo(k,2m+2).

However the stage "m" of ring "k" with "m" stages of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 2 inputs and 2 outputs as shown in diagram 200D in FIG. 2D. FIG. 2D illustrates a stage (ring "k", stage "m") 200D consists of 2 inputs namely Fi(k,2m+1) and Fi(k,2m+2); and 2 outputs Fo(k,2m+1) and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of two 2:1 Muxes namely F(k,2m+1), F(k,2m+2) (comprising in combination a forward switch). The 2:1 Mux F(k,2m+1) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2). A stage with 2 inputs and 2 outputs is, in one embodiment, the "last stage" or "root stage" of ring.

The stage "m" of ring "k" with "m" stages of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 8 inputs and 4 outputs as shown in diagram 200E in FIG. 2E. FIG. 2E illustrates a stage (ring "k", stage "m") 200E consists of 8 inputs namely Fi(k,2m+1), Fi(k,2m+2), Bi(k,2m+1), Bi(k,2m+2), J, K, L, and M; and 4 outputs Uo(k,2m+1), Uo(k,2m+2), Ro(k,2m+1), and Ro(k,2m+2). The stage (ring "k", stage "m") also consists of eight 2:1 Muxes namely F(k,2m+1), F(k,2m+2) (comprising in combination a forward switch), R(k,2m+1), R(k,2m+2) (comprising in combination a Reverse U-turn switch), B(k,2m+1), B(k,2m+2) (comprising in combination a backward switch), U(k,2m+1), and U(k,2m+2) (comprising in combination a U-turn switch). The 2:1 Mux R(k,2m+1) has two inputs namely Fi(k,2m+1) and J, and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Fi(k,2m+2) and K, and has one output Fo(k,2m+2). The 2:1 Mux R(k,2m+1) has two inputs namely Fo(k,2m+1) and Bo(k,2m+2), and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Fo(k,2m+2) and Bo(k,2m+1) , and has one output Ro(k,2m+2).

The 2:1 Mux B(k,2m+1) has two inputs namely Bi(k,2m+1) and L, and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Bi(k,2m+2) and M, and has one output Bo(k,2m+2). The 2:1 Mux U(k,2m+1) has two inputs namely Bo(k,2m+1) and Fo(k,2m+2), and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Bo(k,2m+2) and Fo(k,2m+1), and has one output Uo(k,2m+2). In different embodiments the inputs J, K, L, and M are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The diagram 200E of FIG 2E eliminates the 180-degree turn paths from the internal connection Fi(k,2m+1) to the internal connection Uo(k,2m+1). Similarly the diagram 200E of FIG 2E eliminates the 180-degree turn paths from the connection Fi(k,2m+2) to the connection Uo(k,2m+2). The diagram 200E of FIG 2E eliminates the 180-degree turn paths from the internal connection Bi(k,2m+1) to the internal connection Ro(k,2m+1). Similarly the diagram 200E of FIG 2E eliminates the 180-degree turn paths from the connection Bi(k,2m+2) to the connection Ro(k,2m+2). Hence diagram 200E of FIG. 2E comprises a forward switch, a backward switch, U-turn switch and reverse U-turn switch without 180-degree U-turn paths.

In contrast to diagram 200E of FIG. 2E, the diagram 200A of FIG. 2A, diagram 200B of FIG. 2B, and diagram 200C of FIG. 2C provide 180-degree U-turn paths. Two exemplary 180-degree U-turn paths in diagram 200A of FIG. 2A are shown (by two types of dotted lines) in the attached replacement diagram of FIG. 2A. One of the 180-degree turn path shown in the replacement diagram of FIG. 2A starts at the internal connection Fi(k,2m+1) through the Mux F(k,2m+1) to Fo(k,2m+1) through the Mux U(k,2m+1) to Uo(k,2m+1) through the Mux B(k,2m+1) to the internal connection Bo(k,2m+1). The second of the 180-degree turn path shown in the replacement diagram of FIG. 2A starts at the hop wire Fi(k,2m+2) through the Mux F(k,2m+2) to Fo(k,2m+2) through the Mux U(k,2m+2) to Uo(k,2m+2) through the Mux B(k, 2m+2) to the hop wire Bo(k,2m+2).

The stage "m" of ring "k" with "m" stages of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 8 inputs and 4 outputs as shown in diagram 200F in FIG. 2F. FIG. 2F illustrates a stage (ring "k", stage "m") 200F

consists of 8 inputs namely Ri(k,2m+1), Ri(k,2m+2), Ui(k,2m+1), Ui(k,2m+2), J, K, L, and M; and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of four 4:1 Muxes namely F(k,2m+1), F(k,2m+2), B(k,2m+1), and B(k,2m+2). The 4:1 Mux F(k,2m+1) has four inputs namely Ri(k,2m+1), Ri(k,2m+2), Ui(k,2m+2), and J, and has one output Fo(k,2m+1). The 4:1 Mux F(k,2m+2) has four inputs namely Ri(k,2m+1), Ri(k,2m+2), Ui(k,2m+1), and K, and has one output Fo(k,2m+2).

The 4:1 Mux B(k,2m+1) has four inputs namely Ui(k,2m+1), Ui(k,2m+2), Ri(k,2m+2), and L, and has one output Bo(k,2m+1). The 4:1 Mux B(k,2m+2) has four inputs namely Ui(k,2m+1), Ui(k,2m+2), Ri(k,2m+1) and M, and has one output Bo(k,2m+2). In different embodiments the inputs J, K, L, and M are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The diagram 200F of FIG 2F eliminates the 180-degree turn paths from the internal connection Ri(k,2m+1) to the internal connection Bo(k,2m+1). Similarly the diagram 200F of FIG 2F eliminates the 180-degree turn paths from the connection Ri(k,2m+2) to the connection Bo(k,2m+2). The diagram 200F of FIG 2F eliminates the 180-degree turn paths from the internal connection Ui(k,2m+1) to the internal connection Fo(k,2m+1). Similarly the diagram 200F of FIG 2F eliminates the 180-degree turn paths from the connection Ui(k,2m+2) to the connection Fo(k,2m+2). Hence diagram 200F of FIG. 2F comprises an integrated switch of a backward switch, U-turn switch and reverse U-turn switch without 180-degree U-turn paths.

The number of stages in a ring of any block may not be equal to the number of stages in any other ring of the same of block or any ring of any other block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. For example the number of stages in ring 1 of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A or of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B or of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C is denoted by "m" and the number of stages in ring 2 of the partial multi-stage hierarchical network is denoted by "n", and so "m" may or may not be equal to "n". Similarly the number of stages in ring 2 corresponding to

block (3,3) of 2D-grid 800 may not be equal to the number of stages in ring 2 corresponding to block (6,9) of 2D-grid 800. Similarly in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C the number of stages in (slice 1, ring 2) corresponding to block (3,3) of 2D-grid 800 may not be equal to the number of stages in (slice 1, ring 2) corresponding to block (6,9) of 2D-grid 800.

Even though the number of inlet links to the computational block is four and the number of outlet links to the computational block is two in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A, the number of inlet links to the computational block is eight and the number of outlet links to the computational block is four in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B, and the number of inlet links to the computational block is sixteen and the number of outlet links to the computational block is four in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C, in other embodiments the number of inlet links to the computational block may be any arbitrary number and the number of outlet links to the computational block may also be another arbitrary number. However the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of inlet links to the computational block divided by $d = 2$ if the inputs and outputs are connected either only from left-hand side or only from right-hand side, if the number of inlet links to the computational block is greater than or equal to the number of outlet links to the computational block. In such a case one or more of the outlet links to the computational block are connected to more than one inlet links of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to a block. Similarly the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of inlet links to the computational block divided by $2 * d = 4$ if the inputs and outputs are connected from both left-hand side and from right-hand side, if the number of inlet links to the computational block is greater than or equal to the number of outlet links to the computational block.

Otherwise the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of outlet links to the computational block divided by $d = 2$ if the inputs and outputs are connected either only from left-hand side or only from right-hand side, if the number of outlet links to the computational block is greater than the number of inlet links to the computational block. In such a case one or more of the outlet links of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to a block are connected to more than one inlet link of the computational block. Similarly the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of outlet links to the computational block divided by $2 * d = 4$ if the inputs and outputs are connected from both left-hand side and from right-hand side, if the number of outlet links to the computational block is greater than or equal to the number of inlet links to the computational block.

In another embodiment, the number of inlet links to the computational block corresponding to a block of 2D-grid of blocks may or may not be equal to the number of inlet links to the computational block corresponding to another block. Similarly the number of outlet links to the computational block corresponding to a block of 2D-grid of blocks may or may not be equal to the number of outlet links to the computational block corresponding to another block. Hence the total number of rings of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to a block of 2D-grid of blocks may or may not be equal to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to another block. For example the total number of rings corresponding to block (4,5) of 2D-grid 800 may be two and the total number of rings in block (5,4) of 2D-grid 800 may be three.

A multi-stage hierarchical network can be represented with the notation $V_{Comb}(N_1, N_2, d, s)$, where N_1 represents the total number of inlet links of the complete multi-stage hierarchical network and N_2 represents the total number of outlet links of the complete multi-stage hierarchical network, d represents the number of inlet links of any ring in any block of the complete multi-stage hierarchical network either from only left-

hand side or only right-hand side, or equivalently the number of outlet links of any ring in any block of the complete multi-stage hierarchical network either from only left-hand side or only right-hand side, and when the inputs and outputs are connected from left-hand side, s is the ratio of number of outgoing links from each stage 0 of any ring in any block to the number of inlet links of any ring in any block of the complete multi-stage hierarchical network (for example the complete multi-stage hierarchical network corresponding to $V_{Comb}(N_1, N_2, d, s)$ 100A in FIG. 1A, $N_1 = 200$, $N_2 = 400$, $d = 2$, $s = 1$). Also a multi-stage hierarchical network where $N_1 = N_2 = N$ is represented as $V_{Comb}(N, d, s)$.

The diagram 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, and 300E of FIG. 3E are different embodiments of all the connections between two arbitrary successive stages in two different rings of the same block or two different rings of different blocks of 2D-grid 800. Referring to diagram 300A in FIG. 3A illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 4 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), and Ui(x,2p+2); and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of eight 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and Bo(x,2p+1) and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and Bo(x,2p+2) and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Ro(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+1) and Ro(x,2p+2) and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs

namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 4 inputs namely Ri(x,2p+3), Ri(x,2p+4), Ui(x,2p+3), and Ui(x,2p+4); and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of eight 2:1 Muxes namely R(x,2p+3), R(x,2p+4), F(x,2p+3), F(x,2p+4), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The 2:1 Mux R(x,2p+3) has two inputs namely Ri(x,2p+3) and Bo(x,2p+3) and has one output Ro(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs namely Ri(x,2p+4) and Bo(x,2p+4) and has one output Ro(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely Ro(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely Ro(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and Fo(x,2p+3) and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and Fo(x,2p+4) and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Ri(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 4 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), and Ui(y,2q+2); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of eight 2:1 Muxes namely R(y,2q+1), R(y,2q+2), F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and Bo(y,2q+1) and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Ri(y,2q+2) and Bo(y,2q+2) and has one output Ro(y,2q+2). The 2:1 Mux

F(y,2q+1) has two inputs namely Ro(y,2q+1) and Ro(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Ro(y,2q+1) and Ro(y,2q+2) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and Fo(y,2q+1) and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 4 inputs namely Ri(y,2q+3), Ri(y,2q+4), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of eight 2:1 Muxes namely R(y,2q+3), R(y,2q+4), F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux R(y,2q+3) has two inputs namely Ri(y,2q+3) and Bo(y,2q+3) and has one output Ro(y,2q+3). The 2:1 Mux R(y,2q+4) has two inputs namely Ri(y,2q+4) and Bo(y,2q+4) and has one output Ro(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely Ro(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Ro(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Ri(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Ri(y,2q+4) of the stage (ring "y", stage "q+1"). The output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to the input Ui(y,2q+2) of the stage (ring "y", stage "q").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to the input Ri(x,2p+4) of the stage (ring "x", stage "p+1"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

Ring "x" and ring "y" may or may not belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. If ring "x" and ring "y" belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are hereinafter called "internal hop wires". For example if "x = 2" and "y = 3" and both the ring 2 and ring 3 belong to the same block (9,9) of 2D-grid 800, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are "internal hop wires".

If ring "x" and ring "y" belong to the different blocks of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are hereinafter called "external hop wires". The external hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) may be horizontal wires or vertical wires. The length of the external hop wires is manhattan distance between the corresponding blocks, hereinafter "hop length". For example if ring "x" belongs to block (1,1) and ring "y" belongs to block (1,6) of 2D-grid 800 then the external hop wires are hereinafter called "horizontal external hop wires". And the hop length of the horizontal hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) is given by 6 – 1 = 5. Similarly if ring "x" and ring "y" belong to two blocks in the same horizontal row of 2D-grid 800, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are horizontal external hop wires.

For example if ring "x" belongs to block (1,1) and ring "y" belongs to block (9,1) of 2D-grid 800 then the external hop wires are hereinafter called "vertical external hop wires". And the hop length of the vertical hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) is given by 9 – 1 = 8. Similarly if ring "x" and ring "y" belong to two blocks in

the same vertical column of 2D-grid 800, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are vertical external hop wires. External hop wires are typically horizontal or vertical according to the current invention.

Referring to diagram 300B in FIG. 3B illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 8 inputs namely Fi(x,2p+1), Fi(x,2p+2), Bi(x,2p+1), Bi(x,2p+2), J1, K1, L1, and M1; and 4 outputs Uo(x,2p+1), Uo(x,2p+2), Ro(x,2p+1), and Ro(x,2p+2). The stage (ring "x", stage "p') also consists of eight 2:1 Muxes namely F(x,2p+1), F(x,2p+2), R(x,2p+1), R(x,2p+2), B(x,2p+1), B(x,2p+2), U(x,2p+1), and U(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Fi(x,2p+1) and J1, and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Fi(x,2p+2) and K1, and has one output Fo(x,2p+2). The 2:1 Mux R(x,2p+1) has two inputs namely Fo(x,2p+1) and Bo(x,2p+2), and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Fo(x,2p+2) and Bo(x,2p+1), and has one output Ro(x,2p+2).

The 2:1 Mux B(x,2p+1) has two inputs namely Bi(x,2p+1) and L1, and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Bi(x,2p+2) and M1, and has one output Bo(x,2p+2). The 2:1 Mux U(x,2p+1) has two inputs namely Bo(x,2p+1) and Fo(x,2p+2), and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Bo(x,2p+2) and Fo(x,2p+1), and has one output Uo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 8 inputs namely Fi(x,2p+3), Fi(x,2p+4), Bi(x,2p+3), Bi(x,2p+4), J2, K2, L2, and M2; and 4 outputs Uo(x,2p+3), Uo(x,2p+4), Ro(x,2p+3), and Ro(x,2p+4). The stage (ring "x", stage "p+1") also consists of eight 2:1 Muxes namely F(x,2p+3), F(x,2p+4), R(x,2p+3), R(x,2p+4), B(x,2p+3), B(x,2p+4), U(x,2p+3), and U(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely Fi(x,2p+3) and J2, and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely Fi(x,2p+4) and K2, and has one output Fo(x,2p+4). The 2:1 Mux R(x,2p+3) has

two inputs namely Fo(x,2p+3) and Bo(x,2p+4), and has one output Ro(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs namely Fo(x,2p+4) and Bo(x,2p+3), and has one output Ro(x,2p+4).

The 2:1 Mux B(x,2p+3) has two inputs namely Bi(x,2p+3) and L2, and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Bi(x,2p+4) and M2, and has one output Bo(x,2p+4). The 2:1 Mux U(x,2p+3) has two inputs namely Bo(x,2p+3) and Fo(x,2p+4), and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Bo(x,2p+4) and Fo(x,2p+3), and has one output Uo(x,2p+4).

The output Ro(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Fi(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Uo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Bi(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 8 inputs namely Fi(y,2q+1), Fi(y,2q+2), Bi(y,2q+1), Bi(y,2q+2), J3, K3, L3, and M3; and 4 outputs Uo(y,2q+1), Uo(y,2q+2), Ro(y,2q+1), and Ro(y,2q+2). The stage (ring "y", stage "q') also consists of eight 2:1 Muxes namely F(y,2q+1), F(y,2q+2), R(y,2q+1), R(y,2q+2), B(y,2q+1), B(y,2q+2), U(y,2q+1), and U(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Fi(y,2q+1) and J3, and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Fi(y,2q+2) and K3, and has one output Fo(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Fo(y,2q+1) and Bo(y,2q+2), and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Fo(y,2q+2) and Bo(y,2q+1) and has one output Ro(y,2q+2).

The 2:1 Mux B(y,2q+1) has two inputs namely Bi(y,2q+1) and L3, and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Bi(y,2q+2) and M3, and has one output Bo(y,2q+2). The 2:1 Mux U(y,2q+1) has two inputs namely Bo(y,2q+1) and Fo(y,2q+2), and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Bo(y,2q+2) and Fo(y,2q+1), and has one output Uo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 8 inputs namely Fi(y,2q+3), Fi(y,2q+4), Bi(y,2q+3), Bi(y,2q+4), J4, K4, L4, and M4; and 4 outputs Uo(y,2q+3), Uo(y,2q+4), Ro(y,2q+3), and Ro(y,2q+4). The stage (ring "y", stage "q+1") also consists

of eight 2:1 Muxes namely F(y,2q+3), F(y,2q+4), R(y,2q+3), R(y,2q+4), B(y,2q+3), B(y,2q+4), U(y,2q+3), and U(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely Fi(y,2q+3) and J4, and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Fi(y,2q+4) and K4, and has one output Fo(y,2q+4). The 2:1 Mux R(y,2q+3) has two inputs namely Fo(y,2q+3) and Bo(y,2q+4), and has one output Ro(y,2q+3). The 2:1 Mux R(y,2q+4) has two inputs namely Fo(y,2q+4) and Bo(y,2q+3), and has one output Ro(y,2q+4).

The 2:1 Mux B(y,2q+3) has two inputs namely Bi(y,2q+3) and L4, and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Bi(y,2q+4) and M4, and has one output Bo(y,2q+4). The 2:1 Mux U(y,2q+3) has two inputs namely Bo(y,2q+3) and Fo(y,2q+4), and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Bo(y,2q+4) and Fo(y,2q+3), and has one output Uo(y,2q+4).

The output Ro(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Fi(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Uo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Bi(y,2q+1) of the stage (ring "y", stage "q").

The output Uo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Bi(y,2q+2) of the stage (ring "y", stage "q"). The output Ro(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(1,2) to the input Fi(x,2p+2) of the stage (ring "x", stage "p").

The output Uo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(2,1) to the input Bi(y,2q+4) of the stage (ring "y", stage "q+1"). The output Ro(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to the input Fi(x,2p+4) of the stage (ring "x", stage "p+1").

In various embodiments, the inputs J1, K1, L1, and M1 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J2, K2, L2, and M2 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J3, K3, L3, and M3 are

connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Finally the inputs J4, K4, L4, and M4 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Referring to diagram 300C in FIG. 3C, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 4 inputs namely Fi(x,2p+1), Fi(x,2p+2), Ui(x,2p+1), and Ui(x,2p+2); and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of six 2:1 Muxes namely F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Fi(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Fi(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 4 inputs namely Fi(x,2p+3), Fi(x,2p+4), Ui(x,2p+3), and Ui(x,2p+4); and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of six 2:1 Muxes namely F(x,2p+3), F(x,2p+4), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely Fi(x,2p+3) and Fi(x,2p+4) and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely Fi(x,2p+3) and Fi(x,2p+4) and has one output Fo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and Fo(x,2p+3) and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and Fo(x,2p+4) and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Fi(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 4 inputs namely Fi(y,2q+1), Fi(y,2q+2), Ui(y,2q+1), and Ui(y,2q+2); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of six 2:1 Muxes namely F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and Fo(y,2q+1) and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 4 inputs namely Fi(y,2q+3), Fi(y,2q+4), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of six 2:1 Muxes namely F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely Fi(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Fi(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Fi(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Fi(y,2q+4) of the stage (ring "y", stage "q+1"). The output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to the input Ui(y,2q+2) of the stage (ring "y", stage "q").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to the input Fi(x,2p+4) of the stage (ring "x", stage "p+1"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

Referring to diagram 300D in FIG. 3D, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 4 inputs namely Fi(x,2p+1), Fi(x,2p+2), Ui(x,2p+1), and Ui(x,2p+2); and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of six 2:1 Muxes namely F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Fi(x,2p+1) and Fi(x,2p+2) and has one output

Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Fi(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 2 inputs namely Fi(x,2p+3), Fi(x,2p+4); and 2 outputs Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of two 2:1 Muxes namely F(x,2p+3) and F(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely Fi(x,2p+3) and Fi(x,2p+4) and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely Fi(x,2p+3) and Fi(x,2p+4) and has one output Fo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Fi(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Fo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 4 inputs namely Fi(y,2q+1), Fi(y,2q+2), Ui(y,2q+1), and Ui(y,2q+2); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of six 2:1 Muxes namely F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and Fo(y,2q+1) and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux

B(y,2q+2) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 4 inputs namely Fi(y,2q+3), Fi(y,2q+4), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of six 2:1 Muxes namely F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely Fi(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Fi(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Fi(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Fi(y,2q+4) of the stage (ring "y", stage "q+1"). The output Fo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to the input Ui(y,2q+2) of the stage (ring "y", stage "q").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to the input Fi(x,2p+4) of the stage (ring "x", stage "p+1"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

Referring to diagram 300E in FIG. 3E, illustrates all the connections between root stage of a ring namely the stage (ring "x", stage "p") and two other arbitrary successive

stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 4 inputs namely Fi(x,2p+1), Fi(x,2p+2), Ui(x,2p+1), and Ui(x,2p+2); and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of six 2:1 Muxes namely F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Fi(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Fi(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+2).

The stage (ring "y", stage "q") consists of 4 inputs namely Fi(y,2q+1), Fi(y,2q+2), Ui(y,2q+1), and Ui(y,2q+2); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of six 2:1 Muxes namely F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and Fo(y,2q+1) and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 4 inputs namely Fi(y,2q+3), Fi(y,2q+4), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of six 2:1 Muxes namely F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely Fi(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Fi(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Fi(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected via the wire Hop(1,2) to the input Ui(y,2q+2) of the stage (ring "y", stage "q"). The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Fi(y,2q+4) of the stage (ring "y", stage "q+1").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to the input Ui(x,2p+1) of the stage (ring "x", stage "p"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

Just like in diagram 300A of FIG. 3A, in diagram 300B of FIG. 3B, in diagram 300C of FIG. 3C, diagram 300D of FIG. 3D, and in diagram 300E of FIG. 3E, the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are either internal hop wires or horizontal external hop wires or vertical external hop wires (hereinafter alternatively referred to as "cross links" or "cross middle links").

The diagram 400A of FIG. 4A and 400B of FIG. 4B are different embodiments of all the connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks of 2D-grid 800. Referring to diagram 400A in FIG. 4A illustrates all the connections between an arbitrary stage of a ring namely the stages (ring "x", stage "p"), and another arbitrary stage of any other ring namely the stages (ring "y", stage "q") of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 8 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), J1, K1, L1, and M1; and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of eight 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and J1 and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and K1 and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Uo(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+2) and Uo(x,2p+1) and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and L1 and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and M1 and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Ro(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+2) and Ro(x,2p+1) and has one output Bo(x,2p+2).

The stage (ring "y", stage "q") consists of 8 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), J3, K3, L3, and M3; and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of eight 2:1 Muxes namely R(y,2q+1), R(y,2q+2), F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and J3 and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Ri(y,2q+2) and K3 and has one output Ro(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Ro(y,2q+1) and Uo(y,2q+2) and has one output

Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Ro(y,2q+2) and Uo(y,2q+1) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and L3, and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and M3, and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Ro(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+2) and Ro(y,2q+1) and has one output Bo(y,2q+2).

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Ri(y,2q+2) of the stage (ring "y", stage "q"). The output Bo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(1,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

Ring "x" and ring "y" may or may not belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. If ring "x" and ring "y" belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1) and Hop(1,2) are hereinafter called "internal hop wires". For example if "x = 2" and "y = 3" and both the ring 2 and ring 3 belong to the same block (9,9) of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are "internal hop wires".

If ring "x" and ring "y" belong to the different blocks of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1) and Hop(1,2) are hereinafter called "external hop wires". The external hop wires Hop(1,1) and Hop(1,2) may be horizontal wires or vertical wires. The length of the external hop wires is Manhattan distance between the corresponding blocks, hereinafter "hop length". For example if ring "x" belongs to block (1,1) and ring "y" belongs to block (1,6) of 2D-grid 800 then the external hop wires are hereinafter called "horizontal external hop wires". And the hop length of the horizontal hop wires Hop(1,1) and Hop(1,2) is given by 6 – 1 = 5. Similarly if ring "x" and ring "y" belong to two blocks in the same horizontal row of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are horizontal external hop wires.

For example if ring "x" belongs to block (1,1) and ring "y" belongs to block (9,1) of 2D-grid 800 then the external hop wires are hereinafter called "vertical external hop

wires". And the hop length of the vertical hop wires Hop(1,1) and Hop(1,2) is given by 9 – 1 = 8. Similarly if ring "x" and ring "y" belong to two blocks in the same vertical column of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are vertical external hop wires. External hop wires are typically horizontal or vertical according to the current invention.

Referring to diagram 400B in FIG. 4B illustrates all the connections between an arbitrary stage of a ring namely the stages (ring "x", stage "p"), and another arbitrary stage of any other ring namely the stages (ring "y", stage "q") of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 8 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), J1, K1, L1, and M1; and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of four 4:1 Muxes namely F(x,2p+1), F(x,2p+2), B(x,2p+1), and B(x,2p+2). The 4:1 Mux F(x,2p+1) has four inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+2), and J1 and has one output Fo(x,2p+1). The 4:1 Mux F(x,2p+2) has four inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), and K1 and has one output Fo(x,2p+2).

The 4:1 Mux B(x,2p+1) has four inputs namely Ui(x,2p+1), Ui(x,2p+2), Ri(x,2p+2), and L1 and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Ui(x,2p+1), Ui(x,2p+2), Ri(x,2p+1), and M1 and has one output Bo(x,2p+2).

The stage (ring "y", stage "q") consists of 8 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), J3, K3, L3, and M3; and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of four 4:1 Muxes namely F(y,2q+1), F(y,2q+2), B(y,2q+1), and B(y,2q+2). The 4:1 Mux F(y,2q+1) has four inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+2), and J3 and has one output Fo(y,2q+1). The 4:1 Mux F(y,2q+2) has four inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), and K3 and has one output Fo(y,2q+2).

The 4:1 Mux B(y,2q+1) has four inputs namely Ui(y,2q+1), Ui(y,2q+2), Ri(y,2q+2), and L3, and has one output Bo(y,2q+1). The 4:1 Mux B(y,2q+2) has four

inputs namely Ui(y,2q+1), Ui(y,2q+2), Ri(y,2q+1), and M3, and has one output Bo(y,2q+2).

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Ri(y,2q+2) of the stage (ring "y", stage "q"). The output Bo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(1,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

Ring "x" and ring "y" may or may not belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. If ring "x" and ring "y" belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1) and Hop(1,2) are hereinafter called "internal hop wires". For example if "x = 2" and "y = 3" and both the ring 2 and ring 3 belong to the same block (9,9) of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are "internal hop wires".

If ring "x" and ring "y" belong to the different blocks of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1) and Hop(1,2) are hereinafter called "external hop wires". The external hop wires Hop(1,1) and Hop(1,2) may be horizontal wires or vertical wires. The length of the external hop wires is Manhattan distance between the corresponding blocks, hereinafter "hop length". For example if ring "x" belongs to block (1,1) and ring "y" belongs to block (1,6) of 2D-grid 800 then the external hop wires are hereinafter called "horizontal external hop wires". And the hop length of the horizontal hop wires Hop(1,1) and Hop(1,2) is given by 6 – 1 = 5. Similarly if ring "x" and ring "y" belong to two blocks in the same horizontal row of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are horizontal external hop wires.

For example if ring "x" belongs to block (1,1) and ring "y" belongs to block (9,1) of 2D-grid 800 then the external hop wires are hereinafter called "vertical external hop wires". And the hop length of the vertical hop wires Hop(1,1) and Hop(1,2) is given by 9 – 1 = 8. Similarly if ring "x" and ring "y" belong to two blocks in the same vertical column of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are vertical external hop wires. External hop wires are typically horizontal or vertical according to the current invention.

The diagram 500A of FIG. 5A is an embodiments of all the connections with multi-drop hop wires, between two arbitrary successive stages in two different rings of different blocks of 2D-grid 800. Referring to diagram 500A in FIG. 5A illustrates all the connections with multi-drop hop wires, between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. The multi-drop hop wires are also connected to two other stages (ring "a", stage "s") and (ring "b", stage "t") belonging to a third block.

The stage (ring "x", stage "p") consists of 8 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), J1, K1, L1, and M1; and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of eight 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and J1, and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and K1, and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Uo(x,2p+2), and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+2) and Uo(x,2p+1), and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and L1, and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and M1, and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Ro(x,2p+2), and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+2) and Ro(x,2p+1), and has one output Bo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 8 inputs namely Ri(x,2p+3), Ri(x,2p+4), Ui(x,2p+3), Ui(x,2p+4), J2, K2, L2, and M2; and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of eight 2:1 Muxes namely R(x,2p+3), R(x,2p+4), F(x,2p+3), F(x,2p+4), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The 2:1 Mux R(x,2p+3) has two inputs namely Ri(x,2p+3) and J2, and has one output Ro(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs namely Ri(x,2p+4) and K2, and has one output Ro(x,2p+4). The 2:1 Mux

F(x,2p+3) has two inputs namely Ro(x,2p+3) and Uo(x,2p+4), and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely Ro(x,2p+4) and Uo(x,2p+3), and has one output Fo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and L2, and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and M2, and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Ro(x,2p+4), and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Uo(x,2p+4) and Ro(x,2p+3), and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Ri(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 8 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), J3, K3, L3, and M3; and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of eight 2:1 Muxes namely R(y,2q+1), R(y,2q+2), F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and J3, and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Ri(y,2q+2) and K3, and has one output Ro(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Ro(y,2q+1) and Uo(y,2q+2), and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Ro(y,2q+2) and Uo(y,2q+1) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and L3, and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and M3, and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Ro(y,2q+2), and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+2) and Ro(y,2q+1), and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 8 inputs namely Ri(y,2q+3), Ri(y,2q+4), Ui(y,2q+3), Ui(y,2q+4), J4, K4, L4, and M4; and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists

of eight 2:1 Muxes namely R(y,2q+3), R(y,2q+4), F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux R(y,2q+3) has two inputs namely Ri(y,2q+3) and J4, and has one output Ro(y,2q+3). The 2:1 Mux R(y,2q+4) has two inputs namely Ri(y,2q+4) and K4, and has one output Ro(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely Ro(y,2q+3) and Uo(y,2q+4), and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Ro(y,2q+4) and Uo(y,2q+3), and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and L4, and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and M4, and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Ro(y,2q+4), and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+4) and Ro(y,2q+3), and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Ri(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Ri(y,2q+4) of the stage (ring "y", stage "q+1"). The output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to the input Ui(y,2q+2) of the stage (ring "y", stage "q").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to the input Ri(x,2p+4) of the stage (ring "x", stage "p+1"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

In various embodiments, the inputs J1, K1, L1, and M1 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J2, K2, L2, and M2 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J3, K3, L3, and M3 are

connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Finally the inputs J4, K4, L4, and M4 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "a", stage "s") consists of 8 inputs namely Ri(a,2s+1), Ri(a,2s+2), Ui(a,2s+1), Ui(a,2s+2), J5, K5, L5, and M5; and 4 outputs Bo(a,2s+1), Bo(a,2s+2), Fo(a,2s+1), and Fo(a,2s+2). The stage (ring "a", stage "s') also consists of eight 2:1 Muxes namely R(a,2s+1), R(a,2s+2), F(a,2s+1), F(a,2s+2), U(a,2s+1), U(a,2s+2), B(a,2s+1), and B(a,2s+2). The 2:1 Mux R(a,2s+1) has two inputs namely Ri(a,2s+1) and J5, and has one output Ro(a,2s+1). The 2:1 Mux R(a,2s+2) has two inputs namely Ri(a,2s+2) and K5, and has one output Ro(a,2s+2). The 2:1 Mux F(a,2s+1) has two inputs namely Ro(a,2s+1) and Uo(a,2s+2), and has one output Fo(a,2s+1). The 2:1 Mux F(a,2s+2) has two inputs namely Ro(a,2s+2) and Uo(a,2s+1), and has one output Fo(a,2s+2).

The 2:1 Mux U(a,2s+1) has two inputs namely Ui(a,2s+1) and L5, and has one output Uo(a,2s+1). The 2:1 Mux U(a,2s+2) has two inputs namely Ui(a,2s+2) and M5, and has one output Uo(a,2s+2). The 2:1 Mux B(a,2s+1) has two inputs namely Uo(a,2s+1) and Ro(a,2s+2), and has one output Bo(a,2s+1). The 2:1 Mux B(a,2s+2) has two inputs namely Uo(a,2s+2) and Ro(a,2s+1), and has one output Bo(a,2s+2).

The stage (ring "b", stage "t") consists of 8 inputs namely Ri(b,2t+1), Ri(b,2t+2), Ui(b,2t+1), Ui(b,2t+2), J6, K6, L6, and M6; and 4 outputs Bo(b,2t+1), Bo(b,2t+2), Fo(b,2t+1), and Fo(b,2t+2). The stage (ring "b", stage "t') also consists of eight 2:1 Muxes namely R(b,2t+1), R(b,2t+2), F(b,2t+1), F(b,2t+2), U(b,2t+1), U(b,2t+2), B(b,2t+1), and B(b,2t+2). The 2:1 Mux R(b,2t+1) has two inputs namely Ri(b,2t+1) and J6, and has one output Ro(b,2t+1). The 2:1 Mux R(b,2t+2) has two inputs namely Ri(b,2t+2) and K6, and has one output Ro(b,2t+2). The 2:1 Mux F(b,2t+1) has two inputs namely Ro(b,2t+1) and Uo(b,2t+2), and has one output Fo(b,2t+1). The 2:1 Mux F(b,2t+2) has two inputs namely Ro(b,2t+2) and Uo(b,2t+1), and has one output Fo(b,2t+2).

The 2:1 Mux U(b,2t+1) has two inputs namely Ui(b,2t+1) and L6, and has one output Uo(b,2t+1). The 2:1 Mux U(b,2t+2) has two inputs namely Ui(b,2t+2) and M6, and has one output Uo(b,2t+2). The 2:1 Mux B(b,2t+1) has two inputs namely Uo(b,2t+1) and Ro(b,2t+2), and has one output Bo(b,2t+1). The 2:1 Mux B(b,2t+2) has two inputs namely Uo(b,2t+2) and Ro(b,2t+1), and has one output Bo(b,2t+2).

The wire Hop(1,1) starting from the output Fo(x,2p+2) of the stage (ring "x", stage "p") is also connected to L5 of the stage (ring "a", stage "s"), in addition to the input Ri(y,2q+4) of the stage (ring "y", stage "q+1"). The stage (ring "x", stage "p"), the stage (ring "a", stage "s"), and the stage (ring "y", stage "q+1") may belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Therefore the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may not be equal to the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "y", stage "q+1"). For example the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be one where as the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y+1") may be two. In such a case the wire Hop(1,1) is called hereinafter a "multi-drop hop wire". The wire Hop(1,1) may be either horizontal hop wire or vertical hop wire. Also multi-drop hop wires are either horizontal external hop wires or vertical external hop wires. Similarly the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be any number greater than or equal to one, and also the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y+1") may be any number greater or equal to one.

In general a multi-drop hop wire may be dropping or terminating in more than one different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. For example a multi-drop hop wire starting from one block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ may be terminating at three different blocks or four different blocks, etc.

The wire Hop(1,2) starting from the output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is also connected to J6 of the stage (ring "b", stage "t"), in addition to the

input Ui(y,2q+2) of the stage (ring "y", stage "q"). The wire Hop(1,2) is also an example of multi-drop hop wire when the stage (ring "x", stage "p+1"), the stage (ring "b", stage "t") and the stage (ring "y", stage "q") belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The wire Hop(2,1) starting from the output Fo(y,2q+2) of the stage (ring "y", stage "q") is also connected to M5 of the stage (ring "a", stage "s"), in addition to the input Ri(x,2p+4) of the stage (ring "x", stage "p+1"). The wire Hop(2,1) is also an example of multi-drop hop wire when the stage (ring "x", stage "p+1"), the stage (ring "a", stage "s") and the stage (ring "y", stage "q") belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The wire Hop(2,2) starting from the output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is also connected to K6 of the stage (ring "b", stage "t"), in addition to the input Ui(x,2p+2) of the stage (ring "x", stage "p"). The wire Hop(2,2) is also an example of multi-drop hop wire when the stage (ring "x", stage "p"), the stage (ring "b", stage "t") and the stage (ring "y", stage "q+1") belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

In various embodiments, the inputs J5, K5, L5, and M5 are connected from any of the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Also the inputs J6, K6, L6, and M6 are connected from any of the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The diagram 600A of FIG. 6A and 600B of FIG. 6B are different embodiments of all the connections with multi-drop hop wires, between two arbitrary stages in two different rings of different blocks of 2D-grid 800. Referring to diagram 600A in FIG. 6A illustrates all the connections with multi-drop hop wires, between an arbitrary stage of a ring namely the stages (ring "x", stage "p"), and another arbitrary stage of any other ring namely the stages (ring "y", stage "q") of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. The multi-drop hop wires are also connected to another stage (ring "a", stage "s") belonging to a third block.

The stage (ring "x", stage "p") consists of 8 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), J1, K1, L1, and M1; and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of eight 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and J1 and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and K1 and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Uo(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+2) and Uo(x,2p+1) and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and L1 and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and M1 and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Ro(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+2) and Ro(x,2p+1) and has one output Bo(x,2p+2).

The stage (ring "y", stage "q") consists of 8 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), J3, K3, L3, and M3; and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of eight 2:1 Muxes namely R(y,2q+1), R(y,2q+2), F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and J3 and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Ri(y,2q+2) and K3 and has one output Ro(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Ro(y,2q+1) and Uo(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Ro(y,2q+2) and Uo(y,2q+1) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and L3, and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and M3, and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Ro(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+2) and Ro(y,2q+1) and has one output Bo(y,2q+2).

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Ri(y,2q+2) of the stage (ring "y", stage "q"). The output Bo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(1,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

The wire Hop(1,1) starting from the output Fo(x,2p+2) of the stage (ring "x", stage "p") is also connected to L2 of the stage (ring "a", stage "s"), in addition to the input Ri(y,2q+2) of the stage (ring "y", stage "q"). The stage (ring "x", stage "p"), the stage (ring "a", stage "s"), and the stage (ring "y", stage "q") may belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Therefore the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may not be equal to the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "y", stage "q"). For example the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be one where as the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y") may be two. Hence the wire Hop(1,1) is a multi-drop hop wire. Also the wire Hop(1,1) is either horizontal external hop wire or vertical external hop wire. Similarly the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be any number greater than or equal to one, and also the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y") may be any number greater or equal to one.

The wire Hop(1,2) starting from the output Bo(y,2q+2) of the stage (ring "y", stage "q") is also connected to K2 of the stage (ring "a", stage "s"), in addition to the input Ui(x,2p+2) of the stage (ring "x", stage "p"). The wire Hop(1,2) is also an example of multi-drop hop wire when the stage (ring "x", stage "p"), the stage (ring "a", stage "s") and the stage (ring "y", stage "q") belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

In various embodiments, the inputs J2, K2, L2, and M2 are connected from any of the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Referring to diagram 600B in FIG. 6B illustrates all the connections with multi-drop hop wires, between an arbitrary stage of a ring namely the stages (ring "x", stage "p"), and another arbitrary stage of any other ring namely the stages (ring "y", stage "q") of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. The multi-drop hop wires are also connected to another stage (ring "a", stage "s") belonging to a third block.

The stage (ring "x", stage "p") consists of 8 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), J1, K1, L1, and M1; and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of four 4:1 Muxes namely F(x,2p+1), F(x,2p+2), B(x,2p+1), and B(x,2p+2). The 4:1 Mux F(x,2p+1) has four inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+2), and J1 and has one output Fo(x,2p+1). The 4:1 Mux F(x,2p+2) has four inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), and K1 and has one output Fo(x,2p+2).

The 4:1 Mux B(x,2p+1) has four inputs namely Ui(x,2p+1), Ui(x,2p+2), Ri(x,2p+2), and L1 and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Ui(x,2p+1), Ui(x,2p+2), Ri(x,2p+1), and M1 and has one output Bo(x,2p+2).

The stage (ring "y", stage "q") consists of 8 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), J3, K3, L3, and M3; and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of four 4:1 Muxes namely F(y,2q+1), F(y,2q+2), B(y,2q+1), and B(y,2q+2). The 4:1 Mux F(y,2q+1) has four inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+2), and J3 and has one output Fo(y,2q+1). The 4:1 Mux F(y,2q+2) has four inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), and K3 and has one output Fo(y,2q+2).

The 4:1 Mux B(y,2q+1) has four inputs namely Ui(y,2q+1), Ui(y,2q+2), Ri(y,2q+2), and L3, and has one output Bo(y,2q+1). The 4:1 Mux B(y,2q+2) has four inputs namely Ui(y,2q+1), Ui(y,2q+2), Ri(y,2q+1), and M3, and has one output Bo(y,2q+2).

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Ri(y,2q+2) of the stage (ring "y", stage "q"). The output

Bo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(1,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

The wire Hop(1,1) starting from the output Fo(x,2p+2) of the stage (ring "x", stage "p") is also connected to L2 and J2 of the stage (ring "a", stage "s"), in addition to the input Ri(y,2q+2) of the stage (ring "y", stage "q"). The stage (ring "x", stage "p"), the stage (ring "a", stage "s"), and the stage (ring "y", stage "q") may belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Therefore the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may not be equal to the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "y", stage "q"). For example the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be one where as the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y") may be two. Hence the wire Hop(1,1) is a multi-drop hop wire. Also the wire Hop(1,1) is either horizontal external hop wire or vertical external hop wire. Similarly the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be any number greater than or equal to one, and also the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y") may be any number greater or equal to one.

The wire Hop(1,2) starting from the output Bo(y,2q+2) of the stage (ring "y", stage "q") is also connected to K2 and M2 of the stage (ring "a", stage "s"), in addition to the input Ui(x,2p+2) of the stage (ring "x", stage "p"). The wire Hop(1,2) is also an example of multi-drop hop wire when the stage (ring "x", stage "p"), the stage (ring "a", stage "s") and the stage (ring "y", stage "q") belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

In various embodiments, the inputs J2, K2, L2, and M2 are connected from any of the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Referring to diagram 700A in FIG. 7A, illustrates, in one embodiment, the hop wire connections chart of a partial multi-stage hierarchical network

$V_{Comb}(N_1, N_2, d, s)$ 100A or a partial multi-stage hierarchical network

$V_{Comb}(N_1, N_2, d, s)$ 100B, or a partial multi-stage hierarchical network

$V_{Comb}(N_1, N_2, d, s)$ 100C, with m = 6 and n = 7. The hop wire connections chart shows two rings namely ring 1 and ring 2. And there are m+1 = 7 stages in ring 1 and n+1 = 8 stages in ring 2.

The hop wire connections chart 700A illustrates how the hop wires are connected between any two successive stages of all the rings corresponding to a block of 2D-grid 800. "Lx" denotes an internal hop wire connection, where symbol "L" denotes internal hop wire and "x" is an integer. For example "L1" between the stages (ring 1, stage 0) and (ring 1, stage 1) denotes that the corresponding hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are connected to two successive stages of another ring in the same block or alternatively hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are internal hop wires. Since there is also "L1" between the stages (ring 2, stage 0) and (ring 2, stage 1), there are internal hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected between the stages (ring 1, stage 0) and (ring 1, stage 1) and the stages (ring 2, stage 0) and (ring 2, stage 1). Hence there can be only two "L1" labels in the hop wire connection chart 700A.

Similarly there are two "L2" labels in the hop wire connections chart 700A. Since the label "L2" is given between the stages (ring 1, stage 5) and (ring 1, stage 6) and also the label "L2" is given between the stages (ring 2, stage 3) and (ring 2, stage 4), there are corresponding internal hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected between the stages (ring 1, stage 5) and (ring 1, stage 6) and the stages (ring 2, stage 3) and (ring 2, stage 4).

"Vx" denotes an external vertical hop wire, where symbol "V" denotes vertical external hop wire connections from blocks of the topmost row of 2D-grid 800 (i.e., row of blocks consisting of block (1,1), block (1,2), …., and block (1,10)) to the same corresponding stages of the same numbered ring of another block that is directly down south, with "x" vertical hop length, where "x" is a positive integer. For example "V1" between the stages (ring 1, stage 1) and (ring 1, stage 2) denote that from block (1,1) of 2D-grid 800 to another block directly below it, which is block (2,1), since "V1" denotes

hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 1) and (ring 1, stage 2) of block (1,1) to (ring 1, stage 1) and (ring 1, stage 2) of block (2,1). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 1) and (ring 1, stage 2) of block (3,1) to (ring 1, stage 1) and (ring 1, stage 2) of block (4,1). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 1) and (ring 1, stage 2) of block (9,1) to (ring 1, stage 1) and (ring 1, stage 2) of block (10,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

Similarly "V3" between the stages (ring 2, stage 1) and (ring 2, stage 2) denote that from block (1,1) of 2D-grid 800 to another block below it and at a hop length of 3 which is block (4,1), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 1) and (ring 2, stage 2) of block (1,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (4,1). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 1) and (ring 2, stage 2) of block (2,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (5,1). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 1) and (ring 2, stage 2) of block (7,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (10,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

If there is no block that is directly below a block with hop length equal to 3 then there is no vertical external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (8,1) does not have any block that is directly below and with hop length equal to 3 then none of the vertical external hop wires are connected from (ring 2, stage 1) and (ring 2, stage 2) of block (8,1). Similarly from (ring 2, stage 1) and (ring 2, stage 2) of block (9,1) and from (ring 2, stage 1) and (ring 2, stage 2) of block (10,1), none of the vertical external hop wires are connected. Similarly vertical external hop wires are connected corresponding to "V5", "V7" etc., labels given in the hop wire connections chart 700A.

"Ux" denotes an external vertical hop wire, where symbol "U" denotes vertical external hop wire connections starting from blocks that are "x" hop length below the

topmost row of 2D-grid 800 (i.e., row of blocks consisting of block (1+x,1), block (1+x,2), ..., and block (1+x,10)) to the same corresponding stages of the same numbered ring of another block that is directly down below, with "x" vertical hop length, where "x" is a positive integer. For example "U1" between the stages (ring 1, stage 2) and (ring 1, stage 3) denote that from block (2,1) of 2D-grid 800 to another block directly below it, which is block (3,1), since "U1" denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 2) and (ring 1, stage 3) of block (2,1) to (ring 1, stage 2) and (ring 1, stage 3) of block (3,1). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 2) and (ring 1, stage 3) of block (4,1) to (ring 1, stage 2) and (ring 1, stage 3) of block (5,1). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 2) and (ring 1, stage 3) of block (8,1) to (ring 1, stage 2) and (ring 1, stage 3) of block (9,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

If there is no block that is directly below a block with hop length equal to 1 then no vertical external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (10,1) does not have any block that is directly below and with hop length equal to 1 then none of the vertical external hop wires are connected from (ring 1, stage 2) and (ring 1, stage 3) of block (10,1). Similarly for all the blocks in each column from the topmost row up to the row "x", no vertical external hop wires are connected to the corresponding (ring 1, stage 2) and (ring 1, stage 3).

Similarly "U3" between the stages (ring 2, stage 2) and (ring 2, stage 3) denote that starting from blocks that are 3 hop length below the topmost row of 2D-grid 800 (i.e., row of blocks consisting of block (4,1), block (4,2), ..., and block (4,10)) to the same corresponding stages of the same numbered ring of another block that is directly down below, with vertical hop length of 3, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected. For example from block (4,1) of 2D-grid 800 to another block below it and at a hop length of 3 which is block (7,1), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 2) and (ring 2, stage 3) of block (4,1) to (ring 2, stage 1) and (ring 2, stage 2) of

block (7,1). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 2) and (ring 2, stage 3) of block (5,1) to (ring 2, stage 2) and (ring 2, stage 3) of block (8,1). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 2) and (ring 2, stage 3) of block (7,1) to (ring 2, stage 2) and (ring 2, stage 3) of block (10,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

If there is no block that is directly below a block with hop length equal to 3 then no vertical external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (8,1) does not have any block that is directly below and with hop length equal to 3 then none of the vertical external hop wires are connected from (ring 2, stage 2) and (ring 2, stage 3) of block (8,1). Similarly from (ring 2, stage 2) and (ring 2, stage 3) of block (9,1) and from (ring 2, stage 2) and (ring 2, stage 3) of block (10,1), none of the vertical external hop wires are connected. Similarly vertical external hop wires are connected corresponding to "U5", "U7" etc. labels given in the hop wire connections chart 700A.

"Hx" denotes an external horizontal hop wire, where symbol "H" denotes horizontal external hop wire connections from blocks of the leftmost column of 2D-grid 800 (i.e., column of blocks consisting of block (1,1), block (2,1), ..., and block (10,1)) to the same corresponding stages of the same numbered ring of another block that is directly to the right, with "x" horizontal hop length, where "x" is a positive integer. For example "H1" between the stages (ring 1, stage 3) and (ring 1, stage 4) denote that from block (1,1) of 2D-grid 800 to another block directly to the right, which is block (1,2), since "H1" denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 3) and (ring 1, stage 4) of block (1,1) to (ring 1, stage 3) and (ring 1, stage 4) of block (1,2). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 3) and (ring 1, stage 4) of block (1,3) to (ring 1, stage 3) and (ring 1, stage 4) of block (1,4). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 3) and (ring 1, stage 4) of

block (9,1) to (ring 1, stage 3) and (ring 1, stage 4) of block (10,1). The same pattern continues for all the rows starting from the block in the leftmost block of each row.

Similarly "H3" between the stages (ring 2, stage 4) and (ring 2, stage 5) denote that from block (1,1) of 2D-grid 800 to another block to the right and at a hop length of 3 which is block (1,4), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 4) and (ring 2, stage 5) of block (1,1) to (ring 2, stage 4) and (ring 2, stage 5) of block (1,4). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 4) and (ring 2, stage 5) of block (1,2) to (ring 2, stage 4) and (ring 2, stage 5) of block (1,5). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 4) and (ring 2, stage 5) of block (1,7) to (ring 2, stage 4) and (ring 2, stage 5) of block (1,10). The same pattern continues for all the columns starting from the block in the leftmost column of each row.

If there is no block that is directly to the right with hop length equal to 3 then there is no horizontal external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (1,8) does not have any block that is directly to the right and with hop length equal to 3 then none of the horizontal external hop wires are connected from (ring 2, stage 4) and (ring 2, stage 5) of block (1,8). Similarly from (ring 2, stage 4) and (ring 2, stage 5) of block (1,9) and from (ring 2, stage 4) and (ring 2, stage 5) of block (1,10), none of the horizontal external hop wires are connected. Similarly horizontal external hop wires are connected corresponding to "H5", "H7" etc., labels given in the hop wire connections chart 700A.

"Kx" denotes an external horizontal hop wire, where symbol "K" denotes horizontal external hop wire connections starting from blocks that are "x" hop length below the leftmost column of 2D-grid 800 (i.e., column of blocks consisting of block (1, 1+x), block (2, 1+x), …., and block (10, 1+x)) to the same corresponding stages of the same numbered ring of another block that is directly to the right, with "x" horizontal hop length, where "x" is a positive integer. For example "K1" between the stages (ring 1, stage 4) and (ring 1, stage 5) denote that from block (1,2) of 2D-grid 800 to another block directly to the right, which is block (1,3), since "K1" denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1,

stage 4) and (ring 1, stage 5) of block (1,2) to (ring 1, stage 4) and (ring 1, stage 5) of block (1,3). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 4) and (ring 1, stage 4) of block (1,4) to (ring 1, stage 4) and (ring 1, stage 5) of block (1,5). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 4) and (ring 1, stage 5) of block (1,8) to (ring 1, stage 4) and (ring 1, stage 5) of block (1,9). The same pattern continues for all the rows starting from the block in the leftmost column of each row.

If there is no block that is directly to the right of a block with hop length equal to 1 then no horizontal external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (1,10) does not have any block that is directly to the right and with hop length equal to 1 then none of the horizontal external hop wires are connected from (ring 1, stage 4) and (ring 1, stage 5) of block (1,10). Similarly for all the blocks in each row from the leftmost column up to the column "x", no horizontal external hop wires are connected to the corresponding (ring 1, stage 4) and (ring 1, stage 5).

Similarly "K3" between the stages (ring 2, stage 5) and (ring 2, stage 6) denote that starting from blocks that are 3 hop length to the right of the leftmost column of 2D-grid 800 (i.e., column of blocks consisting of block (1,4), block (2,4), ..., and block (10,4)) to the same corresponding stages of the same numbered ring of another block that is directly to the right, with horizontal hop length of 3, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected. For example from block (1,4) of 2D-grid 800 to another block to the right and at a hop length of 3 which is block (1,7), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 5) and (ring 2, stage 6) of block (1,4) to (ring 2, stage 5) and (ring 2, stage 6) of block (1,7). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 5) and (ring 2, stage 6) of block (1,5) to (ring 2, stage 5) and (ring 2, stage 6) of block (1,8). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 5) and (ring 2, stage 6) of block (1,7) to (ring 2, stage 5) and

(ring 2, stage 6) of block (1,10). The same pattern continues for all the rows starting from the block in the leftmost block of each row.

If there is no block that is directly to the right of a block with hop length equal to 3 then no horizontal external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (1,8) does not have any block that is directly to the right and with hop length equal to 3 then none of the horizontal external hop wires are connected from (ring 2, stage 5) and (ring 2, stage 6) of block (1,8). Similarly from (ring 2, stage 5) and (ring 2, stage 6) of block (1,9) and from (ring 2, stage 5) and (ring 2, stage 6) of block (1,10), none of the horizontal external hop wires are connected. Similarly horizontal external hop wires are connected corresponding to "K5", "K7" etc. labels given in the hop wire connections chart 700A.

In general the hop length of an external vertical hop wire can be any positive number. Similarly the hop length of an external horizontal hop wire can be any positive number. The hop wire connections between two arbitrary successive stages in two different rings of the same block or two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, and 300E of FIG. 3E. Similarly the multi-drop hop wire connections between two arbitrary successive stages in two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 500A of FIG. 5A.

In accordance with the invention, the hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may also be any one of the embodiments of either the diagrams 400A of FIG. 4A and 400B of FIG. 4B. Similarly the multi-drop hop wire connections between two arbitrary stages in two different rings of different blocks may also be any one of the embodiments of either the diagrams 600A of FIG. 6A or 600B of FIG. 6B.

In accordance with the current invention, either partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A of FIG. 1A or partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B of FIG. 1B, or partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C, corresponding to a block of 2D-grid of blocks 800

of FIG. 8, using any one of the embodiments of 200A-200E of FIGs. 2A-2E to implement a stage of a ring of the multi-stage hierarchical network, either by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, 300E of FIG. 3E, 500A of FIG. 5A, or by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may be any one of the embodiments of either the diagrams 400A of FIG. 4A, 400B of FIG. 4B, 600A of FIG. 6A, or 600B of FIG. 6B is very efficient in the reduction of the die size, power consumption, and for lower wire/path delay for higher performance for practical routing applications to particularly to set up broadcast, unicast and multicast connections. In general in accordance with the current invention, where N_1 and N_2 of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ may be arbitrarily large in size and also the 2D-grid size 800 may also be arbitrarily large in size in terms of both the number of rows and number of columns.

Delay Optimizations in Multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$:

The multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ according to the current invention can further be optimized to reduce the delay in the routed path of the connection. The delay optimized multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ is hereinafter denoted by $V_{D-Comb}(N_1, N_2, d, s)$. The delay optimizing embodiments of the stages of a ring are one of the diagrams namely 900A-900E of FIGs. 9A-9D, 1000A-1000F of FIGs. 10A-10F, and 1100A-1100C of FIGs. 11A-11C. The diagram 1200 of FIG. 12, 1300 of FIG. 13, 1400 of FIG. 14, and 1500 of FIG. 15 are different embodiments for the implementation of delay optimizations with all the connections between two arbitrary successive stages in two different rings of the same block or two different rings of different blocks of 2D-grid 800.

FIG. 9A illustrates a stage (ring "k", stage "m") 900A consists of 5 inputs namely Fi(k,2m+1), Fi(k,2m+2), YFi(k,2m+1), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of seven 2:1 Muxes namely YF(k,2m+1), F(k,2m+1), F(k,2m+2), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The 2:1 Mux YF(k,2m+1) has two inputs namely Fi(k,2m+1) and YFi(k,2m+1) and has one output YFo(k,2m+1). The 2:1 Mux F(k,2m+1) has two inputs namely YFo(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely YFo(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 9B illustrates a stage (ring "k", stage "m") 900B consists of 5 inputs namely Fi(k,2m+1), Fi(k,2m+2), YUi(k,2m+1), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of seven 2:1 Muxes namely F(k,2m+1), F(k,2m+2), YF(k,2m+1), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux YU(k,2m+1) has two inputs namely Ui(k,2m+1) and YUi(k,2m+1) and has one output YUo(k,2m+1). The 2:1 Mux U(k,2m+1) has two inputs namely YUo(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 9C illustrates a stage (ring "k", stage "m") 900C consists of 5 inputs namely Fi(k,2m+1), Fi(k,2m+2), UYi(k,2m+1), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of five 2:1 Muxes namely F(k,2m+1), F(k,2m+2), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The stage (ring "k", stage "m") also consists of one 3:1 Mux namely UY(k,2m+1). The 2:1 Mux F(k,2m+1) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 3:1 Mux UY(k,2m+1) has three inputs namely Ui(k,2m+1), UYi(k,2m+1) and Fo(k,2m+1) and has one output UYo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 9D illustrates a stage (ring "k", stage "m") 900D consists of 6 inputs namely Fi(k,2m+1), Fi(k,2m+2), YFi(k,2m+1), Ui(k,2m+1), Ui(k,2m+2), and YUi(k,2m+1); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of eight 2:1 Muxes namely F(k,2m+1), F(k,2m+2), YF(k,2m+1), U(k,2m+1), U(k,2m+2), YU(k,2m+1), B(k,2m+1), and B(k,2m+2). The 2:1 Mux YF(k,2m+1) has two inputs namely Fi(k,2m+1) and YFi(k,2m+1) and has one output YFo(k,2m+1). The 2:1 Mux F(k,2m+1) has two inputs namely YFo(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely YFo(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux YU(k,2m+1) has two inputs namely Ui(k,2m+1) and YUi(k,2m+1) and has one output YUo(k,2m+1). The 2:1 Mux U(k,2m+1) has two inputs namely YUo(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 9E illustrates a stage (ring "k", stage "m") 900E consists of 6 inputs namely Fi(k,2m+1), Fi(k,2m+2), YFi(k,2m+1), Ui(k,2m+1), Ui(k,2m+2), and UYi(k,2m+1); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of six 2:1 Muxes namely F(k,2m+1), F(k,2m+2), YF(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The stage (ring "k", stage "m") also consists of one 3:1 Mux namely UY(k,2m+1). The 2:1 Mux YF(k,2m+1) has two inputs namely Fi(k,2m+1) and YFi(k,2m+1) and has one output YFo(k,2m+1). The 2:1 Mux F(k,2m+1) has two inputs namely YFo(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely YFo(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 3:1 Mux UY(k,2m+1) has three inputs namely Ui(k,2m+1), UYi(k,2m+1) and Fo(k,2m+1) and has one output UYo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 10A illustrates a stage (ring "k", stage "m") 1000A consists of 5 inputs namely Ri(k,2m+1), Ri(k,2m+2), YRi(k,2m+1), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of nine 2:1 Muxes namely R(k,2m+1), R(k,2m+2), YR(k,2m+1), F(k,2m+1), F(k,2m+2), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The 2:1 Mux YR(k,2m+1) has two inputs namely Ri(k,2m+1) and YRi(k,2m+1) and has one output YRo(k,2m+1). The 2:1 Mux R(k,2m+1) has two inputs namely YRo(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs

namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 10B illustrates a stage (ring "k", stage "m") 1000B consists of 5 inputs namely Ri(k,2m+1), Ri(k,2m+2), RYi(k,2m+1), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of seven 2:1 Muxes namely R(k,2m+2), F(k,2m+1), F(k,2m+2), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The stage (ring "k", stage "m") also consists of one 3:1 Mux namely RY(k,2m+1). The 3:1 Mux RY(k,2m+1) has three inputs namely Ri(k,2m+1), RYi(k,2m+1), and Bo(k,2m+1), and has one output RYo(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely RYo(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely RYo(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 10C illustrates a stage (ring "k", stage "m") 1000C consists of 5 inputs namely Ri(k,2m+1), Ri(k,2m+2), Ui(k,2m+1), Ui(k,2m+2), and YUi(k,2m+1); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of nine 2:1 Muxes namely R(k,2m+1), R(k,2m+2), F(k,2m+1), F(k,2m+2), YU(k,2m+1), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The 2:1 Mux R(k,2m+1) has two inputs namely Ri(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux YU(k,2m+1) has two inputs namely Ui(k,2m+1) and YUi(k,2m+1) and has one output YUo(k,2m+1). The 2:1 Mux U(k,2m+1) has two inputs namely YUo(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 10D illustrates a stage (ring "k", stage "m") 1000D consists of 5 inputs namely Ri(k,2m+1), Ri(k,2m+2), Ui(k,2m+1), Ui(k,2m+2), and UYi(k,2m+1); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of seven 2:1 Muxes namely R(k,2m+1), R(k,2m+2), F(k,2m+1), F(k,2m+2), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The stage (ring "k", stage "m") also consists of one 3:1 Mux namely UY(k,2m+1). The 2:1 Mux R(k,2m+1) has two inputs namely Ri(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+2).

The 3:1 Mux UY(k,2m+1) has three inputs namely Ui(k,2m+1), UYi(k,2m+1), and Fo(k,2m+1), and has one output UYo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 10E illustrates a stage (ring "k", stage "m") 1000E consists of 6 inputs namely Ri(k,2m+1), Ri(k,2m+2), YRi(k,2m+1), Ui(k,2m+1), Ui(k,2m+2), and YUi(k,2m+1); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of ten 2:1 Muxes namely YR(k,2m+1), R(k,2m+1), R(k,2m+2), F(k,2m+1), F(k,2m+2), YU(k,2m+1), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The 2:1 Mux YR(k,2m+1) has two inputs namely Ri(k,2m+1) and YRi(k,2m+1) and has one output YRo(k,2m+1). The 2:1 Mux

R(k,2m+1) has two inputs namely YRo(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux YU(k,2m+1) has two inputs namely Ui(k,2m+1) and YUi(k,2m+1) and has one output YUo(k,2m+1). The 2:1 Mux U(k,2m+1) has two inputs namely YUo(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 10F illustrates a stage (ring "k", stage "m") 1000F consists of 6 inputs namely Ri(k,2m+1), Ri(k,2m+2), RYi(k,2m+1), Ui(k,2m+1), Ui(k,2m+2), and UYi(k,2m+1); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of six 2:1 Muxes namely R(k,2m+2), F(k,2m+1), F(k,2m+2), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The stage (ring "k", stage "m") also consists of two 3:1 Mux namely RY(k,2m+1) and UY(k,2m+1). The 3:1 Mux RY(k,2m+1) has three inputs namely Ri(k,2m+1), RYi(k,2m+1), and Bo(k,2m+1) and has one output RYo(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely RYo(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely RYo(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+2).

The 3:1 Mux UY(k,2m+1) has three inputs namely Ui(k,2m+1), UYi(k,2m+1), and Fo(k,2m+1), and has one output UYo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 11A illustrates a stage (ring "k", stage "m") 1100A consists of 5 inputs namely Ri(k,2m+1), Ri(k,2m+2), FYi(k,2m+2), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of seven 2:1 Muxes namely R(k,2m+1), R(k,2m+2), F(k,2m+1), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The stage (ring "k", stage "m") also consists of one 3:1 Mux namely FY(k,2m+2). The 2:1 Mux R(k,2m+1) has two inputs namely Ri(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 3:1 Mux FY(k,2m+2) has three inputs namely Ro(k,2m+1), Ro(k,2m+2), and FYi(k,2m+2), and has one output FYo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and FYo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 11B illustrates a stage (ring "k", stage "m") 1100B consists of 5 inputs namely Ri(k,2m+1), Ri(k,2m+2), Ui(k,2m+1), Ui(k,2m+2), and BYi(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of seven 2:1 Muxes namely R(k,2m+1), R(k,2m+2), F(k,2m+1), F(k,2m+2), U(k,2m+1), U(k,2m+2), and B(k,2m+1). The stage (ring "k", stage "m") also consists of one 3:1 Mux namely BY(k,2m+2). The 2:1 Mux R(k,2m+1) has two inputs namely Ri(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Ro(k,2m+1), and Ro(k,2m+2), and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs

namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 3:1 Mux BY(k,2m+2) has three inputs namely Uo(k,2m+1), Uo(k,2m+2), and BYi(k,2m+2), and has one output BYo(k,2m+2).

FIG. 11C illustrates a stage (ring "k", stage "m") 1100C consists of 6 inputs namely Ri(k,2m+1), Ri(k,2m+2), FYi(k,2m+2), Ui(k,2m+1), Ui(k,2m+2), and BYi(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of six 2:1 Muxes namely R(k,2m+1), R(k,2m+2), F(k,2m+1), U(k,2m+1), U(k,2m+2), and B(k,2m+1). The stage (ring "k", stage "m") also consists of two 3:1 Muxes namely FY(k,2m+2) and BY(k,2m+2). The 2:1 Mux R(k,2m+1) has two inputs namely Ri(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 3:1 Mux FY(k,2m+2) has three inputs namely Ro(k,2m+1), Ro(k,2m+2), and FYi(k,2m+2), and has one output FYo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and FYo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 3:1 Mux BY(k,2m+2) has three inputs namely Uo(k,2m+1), Uo(k,2m+2), and BYi(k,2m+2) and has one output BYo(k,2m+2).

Referring to diagram 1200 in FIG. 12, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 5 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), and UYi(x,2p+1); and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p") also consists of seven 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+2),

B(x,2p+1), and B(x,2p+2). The stage (ring "x", stage "p") also consists of one 3:1 Mux namely UY(x,2p+1). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and Bo(x,2p+1) and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and Bo(x,2p+2) and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Ro(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+1) and Ro(x,2p+2) and has one output Fo(x,2p+2).

The 3:1 Mux UY(x,2p+1) has three inputs namely Ui(x,2p+1), UYi(x,2p+1), and Fo(x,2p+1), and has one output UYo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely UYo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely UYo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 5 inputs namely Ri(x,2p+3), Ri(x,2p+4), RYi(x,2p+3), Ui(x,2p+3), and Ui(x,2p+4); and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of seven 2:1 Muxes namely R(x,2p+4), F(x,2p+3), F(x,2p+4), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The stage (ring "x", stage "p+1") also consists of one 3:1 Mux namely RY(x,2p+3). The 3:1 Mux RY(x,2p+3) has three inputs namely Ri(x,2p+3), RYi(x,2p+3), and Bo(x,2p+3), and has one output RYo(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs namely Ri(x,2p+4) and Bo(x,2p+4) and has one output Ro(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely RYo(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely RYo(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and Fo(x,2p+3) and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and Fo(x,2p+4) and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Ri(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 5 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), and YUi(y,2q+1); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q") also consists of nine 2:1 Muxes namely R(y,2q+1), R(y,2q+2), F(y,2q+1), F(y,2q+2), YU(y,2q+1), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and Bo(y,2q+1) and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Ri(y,2q+2) and Bo(y,2q+2) and has one output Ro(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Ro(y,2q+1) and Ro(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Ro(y,2q+1) and Ro(y,2q+2) and has one output Fo(y,2q+2).

The 2:1 Mux YU(y,2q+1) has two inputs namely Ui(y,2q+1) and YUi(y,2q+1) and has one output YUo(y,2q+1). The 2:1 Mux U(y,2q+1) has two inputs namely YUo(y,2q+1) and Fo(y,2q+1) and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 5 inputs namely Ri(y,2q+3), Ri(y,2q+4), YRi(y,2q+3), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of nine 2:1 Muxes namely R(y,2q+3), R(y,2q+4), YR(y,2q+3), F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux YR(y,2q+3) has two inputs namely Ri(y,2q+3) and YRi(y,2q+3) and has one output YRo(y,2q+3). The 2:1 Mux R(y,2q+3) has two inputs namely YRo(y,2q+3) and Bo(y,2q+3) and has one output Ro(y,2q+3). The 2:1 Mux R(y,2q+4) has two inputs namely Ri(y,2q+4) and Bo(y,2q+4) and has one output Ro(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely

Ro(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Ro(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Ri(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to two inputs namely input Ri(y,2q+4) of the stage (ring "y", stage "q+1") and input YUi(y,2q+1) of the stage (ring "y", stage "q"). The output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to two inputs namely input Ui(y,2q+2) of the stage (ring "y", stage "q") and input YRi(y,2q+3) of the stage (ring "y", stage "q+1").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to two inputs namely input Ri(x,2p+4) of the stage (ring "x", stage "p+1") and input UYi(x,2p+1) of the stage (ring "x", stage "p"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to two inputs namely input Ui(x,2p+2) of the stage (ring "x", stage "p") and input RYi(x,2p+3) of the stage (ring "x", stage "p+1").

Referring to diagram 1300 in FIG. 13, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 6 inputs namely Fi(x,2p+1), Fi(x,2p+2), YFi(x,2p+1), Ui(x,2p+1), Ui(x,2p+2), and YUi(x,2p+1); and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p") also consists of eight 2:1 Muxes namely F(x,2p+1), F(x,2p+2), YF(x,2p+1), U(x,2p+1), U(x,2p+2), YU(x,2p+1), B(x,2p+1), and B(x,2p+2). The 2:1 Mux YF(x,2p+1) has two inputs namely Fi(x,2p+1) and YFi(x,2p+1) and has one output YFo(x,2p+1). The 2:1 Mux F(x,2p+1) has two inputs namely YFo(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely YFo(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+2).

The 2:1 Mux YU(x,2p+1) has two inputs namely Ui(x,2p+1) and YUi(x,2p+1) and has one output YUo(x,2p+1). The 2:1 Mux U(x,2p+1) has two inputs namely YUo(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 6 inputs namely Ri(x,2p+3), Ri(x,2p+4), YRi(x,2p+3), Ui(x,2p+3), Ui(x,2p+4), and YUi(x,2p+3); and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of ten 2:1 Muxes namely YR(x,2p+3), R(x,2p+3), R(x,2p+4), F(x,2p+3), F(x,2p+4), YU(x,2p+3), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The 2:1 Mux YR(x,2p+3) has two inputs namely Ri(x,2p+3) and YRi(x,2p+3) and has one output YRo(x,2p+3). The 2:1 Mux R(x,2p+3) has two inputs namely YRo(x,2p+3) and Bo(x,2p+3) and has one output Ro(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs namely Ri(x,2p+4) and Bo(x,2p+4) and has one output Ro(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely Ro(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely Ro(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+4).

The 2:1 Mux YU(x,2p+3) has two inputs namely Ui(x,2p+3) and YUi(x,2p+3) and has one output YUo(x,2p+3). The 2:1 Mux U(x,2p+3) has two inputs namely YUo(x,2p+3) and Fo(x,2p+3) and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4)

has two inputs namely Ui(x,2p+4) and Fo(x,2p+4) and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Ri(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 6 inputs namely Fi(y,2q+1), Fi(y,2q+2), YFi(y,2q+1), Ui(y,2q+1), Ui(y,2q+2), and UYi(y,2q+1); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q") also consists of six 2:1 Muxes namely F(y,2q+1), F(y,2q+2), YF(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The stage (ring "y", stage "q") also consists of one 3:1 Mux namely UY(y,2q+1). The 2:1 Mux YF(y,2q+1) has two inputs namely Fi(y,2q+1) and YFi(y,2q+1) and has one output YFo(y,2q+1). The 2:1 Mux F(y,2q+1) has two inputs namely YFo(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely YFo(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+2).

The 3:1 Mux UY(y,2q+1) has three inputs namely Ui(y,2q+1), UYi(y,2q+1) and Fo(y,2q+1) and has one output UYo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely UYo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely UYo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 6 inputs namely Ri(y,2q+3), Ri(y,2q+4), RYi(y,2q+3), Ui(y,2q+3), Ui(y,2q+4), and UYi(y,2q+3); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "2q+1") also consists of six 2:1 Muxes namely R(y,2q+4), F(y,2q+3), F(y,2q+4), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The stage (ring "y", stage "2q+1") also consists of two 3:1 Mux namely RY(y,2q+3) and UY(y,2q+3). The 3:1 Mux RY(y,2q+3) has three inputs

namely Ri(y,2q+3), RYi(y,2q+3), and Bo(y,2q+3) and has one output RYo(y,2q+3). The 2:1 Mux R(y,2q+4) has two inputs namely Ri(y,2q+4) and Bo(y,2q+4) and has one output Ro(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely RYo(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely RYo(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+4).

The 3:1 Mux UY(y,2q+3) has three inputs namely Ui(y,2q+3), UYi(y,2q+3), and Fo(y,2q+3), and has one output UYo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely UYo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely UYo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Ri(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to two inputs namely input Ri(y,2q+4) of the stage (ring "y", stage "q+1") and input UYi(y,2q+1) of the stage (ring "y", stage "q"). The output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to two inputs namely input Ui(y,2q+2) of the stage (ring "y", stage "q") and input RYi(y,2q+3) of the stage (ring "y", stage "q+1").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to two inputs namely input Ri(x,2p+4) of the stage (ring "x", stage "p+1") and input YUi(x,2p+1) of the stage (ring "x", stage "p"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to two inputs namely input Ui(x,2p+2) of the stage (ring "x", stage "p") and input YRi(x,2p+3) of the stage (ring "x", stage "p+1").

Referring to diagram 1400 in FIG. 14, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages

(ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 5 inputs namely Fi(x,2p+1), Fi(x,2p+2), YUi(x,2p+1), Ui(x,2p+1), and Ui(x,2p+2); and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p") also consists of seven 2:1 Muxes namely F(x,2p+1), F(x,2p+2), YF(x,2p+1), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Fi(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Fi(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+2).

The 2:1 Mux YU(x,2p+1) has two inputs namely Ui(x,2p+1) and YUi(x,2p+1) and has one output YUo(x,2p+1). The 2:1 Mux U(x,2p+1) has two inputs namely YUo(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 5 inputs namely Fi(x,2p+3), Fi(x,2p+4), YFi(x,2p+3), Ui(x,2p+3), and Ui(x,2p+4); and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of seven 2:1 Muxes namely YF(x,2p+3), F(x,2p+3), F(x,2p+4), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The 2:1 Mux YF(x,2p+3) has two inputs namely Fi(x,2p+3) and YFi(x,2p+3) and has one output YFo(x,2p+3). The 2:1 Mux F(x,2p+3) has two inputs namely YFo(x,2p+3) and Fi(x,2p+4) and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely YFo(x,2p+3) and Fi(x,2p+4) and has one output Fo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and Fo(x,2p+3) and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and Fo(x,2p+4) and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+3). The 2:1 Mux

B(x,2p+4) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Fi(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 5 inputs namely Fi(y,2q+1), Fi(y,2q+2), UYi(y,2q+1), Ui(y,2q+1), and Ui(y,2q+2); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q") also consists of five 2:1 Muxes namely F(y,2q+1), F(y,2q+2), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The stage (ring "y", stage "q") also consists of one 3:1 Mux namely UY(y,2q+1). The 2:1 Mux F(y,2q+1) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+2).

The 3:1 Mux UY(y,2q+1) has three inputs namely Ui(y,2q+1), UYi(y,2q+1) and Fo(y,2q+1) and has one output UYo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely UYo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely UYo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 5 inputs namely Fi(y,2q+3), Fi(y,2q+4), YFi(y,2q+3), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of seven 2:1 Muxes namely YF(y,2q+3), F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux YF(y,2q+3) has two inputs namely Fi(y,2q+3) and YFi(y,2q+3) and has one output YFo(y,2q+3). The 2:1 Mux F(y,2q+3) has two inputs namely YFo(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely YFo(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Fi(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to two inputs namely input Fi(y,2q+4) of the stage (ring "y", stage "q+1") and input UYi(y,2q+1) of the stage (ring "y", stage "q"). The output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to two inputs namely input Ui(y,2q+2) of the stage (ring "y", stage "q") and input YFi(y,2q+3) of the stage (ring "y", stage "q+1").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to two inputs namely input Fi(x,2p+4) of the stage (ring "x", stage "p+1") and input YUi(x,2p+1) of the stage (ring "x", stage "p"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to two inputs namely input Ui(x,2p+2) of the stage (ring "x", stage "p") and input YFi(x,2p+3) of the stage (ring "x", stage "p+1").

Referring to diagram 1500 in FIG. 15, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 5 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), and BYi(x,2p+2); and 4 outputs Bo(x,2p+1),

Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p") also consists of seven 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), and B(x,2p+1). The stage (ring "x", stage "p") also consists of one 3:1 Mux namely BY(x,2p+2). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and Bo(x,2p+1) and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and Bo(x,2p+2) and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Ro(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+1), and Ro(x,2p+2), and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 3:1 Mux BY(x,2p+2) has three inputs namely Uo(x,2p+1), Uo(x,2p+2), and BYi(x,2p+2), and has one output BYo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 5 inputs namely Ri(x,2p+3), Ri(x,2p+4), FYi(x,2p+4), Ui(x,2p+3), and Ui(x,2p+4); and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of seven 2:1 Muxes namely R(x,2p+3), R(x,2p+4), F(x,2p+3), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The stage (ring "x", stage "p+1") also consists of one 3:1 Mux namely FY(x,2p+4). The 2:1 Mux R(x,2p+3) has two inputs namely Ri(x,2p+3) and Bo(x,2p+3) and has one output Ro(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs namely Ri(x,2p+4) and Bo(x,2p+4) and has one output Ro(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely Ro(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+3). The 3:1 Mux FY(x,2p+4) has three inputs namely Ro(x,2p+3), Ro(x,2p+4), and FYi(x,2p+4), and has one output FYo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and Fo(x,2p+3) and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and FYo(x,2p+4) and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+3). The 2:1 Mux

B(x,2p+4) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Ri(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 6 inputs namely Ri(y,2q+1), Ri(y,2q+2), FYi(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), and BYi(y,2q+2); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q") also consists of six 2:1 Muxes namely R(y,2q+1), R(y,2q+2), F(y,2q+1), U(y,2q+1), U(y,2q+2), and B(y,2q+1). The stage (ring "y", stage "q") also consists of two 3:1 Muxes namely FY(y,2q+2) and BY(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and Bo(y,2q+1) and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Ri(y,2q+2) and Bo(y,2q+2) and has one output Ro(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Ro(y,2q+1) and Ro(y,2q+2) and has one output Fo(y,2q+1). The 3:1 Mux FY(y,2q+2) has three inputs namely Ro(y,2q+1), Ro(y,2q+2), and FYi(y,2q+2), and has one output FYo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and Fo(y,2q+1) and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and FYo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 3:1 Mux BY(y,2q+2) has three inputs namely Uo(y,2q+1), Uo(y,2q+2), and BYi(y,2q+2) and has one output BYo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 5 inputs namely Fi(y,2q+3), Fi(y,2q+4), YFi(y,2q+3), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of seven 2:1 Muxes namely YF(y,2q+3), F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux YF(y,2q+3) has two inputs namely Fi(y,2q+3) and YFi(y,2q+3) and has one output YFo(y,2q+3). The 2:1 Mux F(y,2q+3) has two inputs namely YFo(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux

F(y,2q+4) has two inputs namely YFo(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Fi(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to two inputs namely input Fi(y,2q+4) of the stage (ring "y", stage "q+1") and input BYi(y,2q+1) of the stage (ring "y", stage "q"). The output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to two inputs namely input Ui(y,2q+2) of the stage (ring "y", stage "q") and input YFi(y,2q+3) of the stage (ring "y", stage "q+1").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to two inputs namely input Ri(x,2p+4) of the stage (ring "x", stage "p+1") and input BYi(x,2p+1) of the stage (ring "x", stage "p"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to two inputs namely input Ui(x,2p+2) of the stage (ring "x", stage "p") and input YFi(x,2p+4) of the stage (ring "x", stage "p+1").

In accordance with the current invention, either partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100A of FIG. 1A, or partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100B of FIG. 1B, or partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C, corresponding to a block of 2D-grid of blocks 800 of FIG. 8, using any one of the embodiments of 200A-200F of FIGs. 2A-2F,

900A-900E of FIGs. 9A-9E, 1000A-1000F of FIGs. 10A-10F, 1100A-1100C of FIGs. 11A-11C to implement a stage of a ring of the multi-stage hierarchical network, either by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, 300E of FIG. 3E, 500A of FIG. 5A, 1200 of FIG. 12, 1300 of FIG. 13, 1400 of FIG. 14, and 1500 of FIG. 15 or by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may be any one of the embodiments of either the diagrams 400A of FIG. 4A, 400B of FIG. 4B, 600A of FIG. 6A, or 600B of FIG. 6B is very efficient in the reduction of the die size, power consumption, and highly optimized for lower wire/path delay for higher performance for practical routing applications to particularly to set up broadcast, unicast and multicast connections. In general in accordance with the current invention, where N_1 and N_2 of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ may be arbitrarily large in size and also the 2D-grid size 800 may also be arbitrarily large in size in terms of both the number of rows and number of columns.

1) Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in programmable integrated circuit applications. FIG. 16A2 illustrates the detailed diagram 1600A2 for the implementation of the diagram 1600A1 in programmable integrated circuit embodiments. Each crosspoint is implemented by a transistor coupled between the corresponding inlet link and outlet link, and a programmable cell in programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by transistor C(1,1) coupled between inlet link IL1 and outlet link OL1, and programmable cell P(1,1); crosspoint CP(1,2) is implemented by transistor C(1,2) coupled between inlet link IL1 and outlet link OL2, and programmable cell P(1,2); crosspoint CP(2,1) is implemented by transistor C(2,1) coupled between inlet link IL2 and outlet link OL1, and programmable cell P(2,1); and crosspoint CP(2,2) is implemented by transistor C(2,2) coupled between inlet link IL2 and outlet link OL2, and programmable cell P(2,2).

If the programmable cell is programmed ON, the corresponding transistor couples the corresponding inlet link and outlet link. If the programmable cell is programmed OFF, the corresponding inlet link and outlet link are not connected. For example if the programmable cell P(1,1) is programmed ON, the corresponding transistor C(1,1) couples the corresponding inlet link IL1 and outlet link OL1. If the programmable cell P(1,1) is programmed OFF, the corresponding inlet link IL1 and outlet link OL1 are not connected. In volatile programmable integrated circuit embodiments the programmable cell may be an SRAM (Static Random Address Memory) cell. In non-volatile programmable integrated circuit embodiments the programmable cell may be a Flash memory cell. Also the programmable integrated circuit embodiments may implement field programmable logic arrays (FPGA) devices, or programmable Logic devices (PLD), or Application Specific Integrated Circuits (ASIC) embedded with programmable logic circuits or 3D-FPGAs.

FIG. 16A2 also illustrates a buffer B1 on inlet link IL2. The signals driven along inlet link IL2 are amplified by buffer B1. Buffer B1 can be inverting or non-inverting buffer. Buffers such as B1 are used to amplify the signal in links which are usually long.

In other embodiments all the $d*d$ switches described in the current invention are also implemented using muxes of different sizes controlled by SRAM cells or flash cells etc.

2) One-time Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in one-time programmable integrated circuit applications. FIG. 16A3 illustrates the detailed diagram 1600A3 for the implementation of the diagram 1600A1 in one-time programmable integrated circuit embodiments. Each crosspoint is implemented by a via coupled between the corresponding inlet link and outlet link in one-time programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by via V(1,1) coupled between inlet link IL1 and outlet link OL1; crosspoint CP(1,2) is implemented by via V(1,2) coupled between inlet link IL1 and outlet link OL2; crosspoint CP(2,1) is implemented by via V(2,1) coupled between inlet link IL2 and outlet link OL1; and

crosspoint CP(2,2) is implemented by via V(2,2) coupled between inlet link IL2 and outlet link OL2.

If the via is programmed ON, the corresponding inlet link and outlet link are permanently connected which is denoted by thick circle at the intersection of inlet link and outlet link. If the via is programmed OFF, the corresponding inlet link and outlet link are not connected which is denoted by the absence of thick circle at the intersection of inlet link and outlet link. For example in the diagram 1600A3 the via V(1,1) is programmed ON, and the corresponding inlet link IL1 and outlet link OL1 are connected as denoted by thick circle at the intersection of inlet link IL1 and outlet link OL1; the via V(2,2) is programmed ON, and the corresponding inlet link IL2 and outlet link OL2 are connected as denoted by thick circle at the intersection of inlet link IL2 and outlet link OL2; the via V(1,2) is programmed OFF, and the corresponding inlet link IL1 and outlet link OL2 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL1 and outlet link OL2; the via V(2,1) is programmed OFF, and the corresponding inlet link IL2 and outlet link OL1 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL2 and outlet link OL1. One-time programmable integrated circuit embodiments may be anti-fuse based programmable integrated circuit devices or mask programmable structured ASIC devices.

3) Integrated Circuit Placement and Route Embodiments:

All the embodiments disclosed in the current invention are useful in Integrated Circuit Placement and Route applications, for example in ASIC backend Placement and Route tools. FIG. 16A4 illustrates the detailed diagram 1600A4 for the implementation of the diagram 1600A1 in Integrated Circuit Placement and Route embodiments. In an integrated circuit since the connections are known a-priori, the switch and crosspoints are actually virtual. However the concept of virtual switch and virtual crosspoint using the embodiments disclosed in the current invention reduces the number of required wires, wire length needed to connect the inputs and outputs of different netlists and the time required by the tool for placement and route of netlists in the integrated circuit.

Each virtual crosspoint is used to either to hardwire or provide no connectivity between the corresponding inlet link and outlet link. Specifically crosspoint CP(1,1) is

implemented by direct connect point DCP(1,1) to hardwire (i.e., to permanently connect) inlet link IL1 and outlet link OL1 which is denoted by the thick circle at the intersection of inlet link IL1 and outlet link OL1; crosspoint CP(2,2) is implemented by direct connect point DCP(2,2) to hardwire inlet link IL2 and outlet link OL2 which is denoted by the thick circle at the intersection of inlet link IL2 and outlet link OL2. The diagram 1600A4 does not show direct connect point DCP(1,2) and direct connect point DCP(1,3) since they are not needed and in the hardware implementation they are eliminated. Alternatively inlet link IL1 needs to be connected to outlet link OL1 and inlet link IL1 does not need to be connected to outlet link OL2. Also inlet link IL2 needs to be connected to outlet link OL2 and inlet link IL2 does not need to be connected to outlet link OL1. Furthermore in the example of the diagram 1600A4, there is no need to drive the signal of inlet link IL1 horizontally beyond outlet link OL1 and hence the inlet link IL1 is not even extended horizontally until the outlet link OL2. Also the absence of direct connect point DCP(2,1) illustrates there is no need to connect inlet link IL2 and outlet link OL1.

In summary in integrated circuit placement and route tools, the concept of virtual switches and virtual cross points is used during the implementation of the placement & routing algorithmically in software, however during the hardware implementation cross points in the cross state are implemented as hardwired connections between the corresponding inlet link and outlet link, and in the bar state are implemented as no connection between inlet link and outlet link.

3) More Application Embodiments:

All the embodiments disclosed in the current invention are also useful in the design of SoC interconnects, Field programmable interconnect chips, parallel computer systems and in time-space-time switches.

Scheduling Method Embodiments the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$:

FIG. 17 shows a high-level flowchart of a scheduling method 1700, in one embodiment executed to setup multicast and unicast connections in the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ disclosed in this invention. According to this embodiment, the set of multicast connections are initialized to the beginning of the set in act 1710. Then the control goes to act 1720. In act 1720, next multicast connection is selected in sequence form the set of multicast connections. Then the control goes to act 1730.

In act 1730 it is checked if this is the next multicast connection in sequence is NULL or i.e. all the multicast connections are scheduled. If act 1730 results "no", that is there are more multicast connections to be scheduled the control goes to act 1740. In act 1740 it is checked if this multicast connection is being scheduled for the first time. Or if it is not scheduled for the first time, it is checked if any one of the links taken by this multicast connection is oversubscribed by any other multicast connection is checked. If either the multicast connection is being scheduled for the first time or if any one of the links taken by this multicast connection is oversubscribed the control goes to act 1750. Otherwise control goes to act 1720 where the next multicast connection will be selected. So act 1720, act 1730, and act 1740 are executed in a loop.

In act 1750 the multicast connection is not being scheduled for the first time and since at least one of the links taken by this multicast connection is oversubscribed, the complete path taken this multicast connection is cleared or the multicast connection's path is ripped. Then the control goes to act 1760. In act 1760, using the well-known A* search algorithm the least cost path from its source outlet link of the computational block to all the target inlet links of the corresponding computational blocks are found out one after another target inlet links. The cost function used is based on the Manhattan distance between the target inlet link's block and source outlet link's block by taking the delays on each wire is considered in the cost function and also that longest wires are chosen first in the A* search algorithm.

According to the current invention, before scheduling the set of multicast connections in the scheduling method 1700, first a set of static cost tables will be prepared with the least cost paths from each link of the partial multistage network $V_{Comb}(N_1, N_2, d, s)$ to each outgoing hop wire from that partial multistage network as well as to each inlet link of the computational block connected form that partial multistage network. So there will be as many cost tables created equal to the sum of the total number of outgoing hop wires from the partial multistage network and the inlet links of the computational block connected form that partial multistage network. Each cost table will also have as many entries as there are internal links of that partial multistage network. And the value at each entry of these cost tables is equal to the total delay from the corresponding internal link to the corresponding outgoing hop wire or to the inlet link of the computational block.

In act 1760, according to the current invention, for the look-ahead cost computation during the A* search algorithm both the cost from the static cost tables from the current internal link in the current partial multistage network and the cost value computed based on the Manhattan distance between the target inlet link's block and the current link's corresponding block by taking the delays on each wire into consideration are added. Also the least of the cost values from all the cost tables corresponding to the current link and all the outgoing wires in the right direction of the target block, is selected before it is added to the Manhattan distance based cost. Finally in act 1760, the multicast connection is scheduled as for the A* search algorithm. Then the control goes to act 1770.

In act 1770, the demand cost and history cost of each link used by the current multicast connection are updated. And the control goes to act 1720. Thus act 1720, act 1730, act 1740, act 1750, act 1760, and act 1770 are executed in a loop to schedule the multicast connections by going through the list of all multicast connections which will be one pass or iteration.

In act 1730 results "yes", i.e. all the required multicast connections in the list are scheduled in this pass or iteration, then the control goes to act 1780. In act 1780, the total number of links in the complete multistage network that are taken by more than one multicast connection are counted, hereinafter "OSN" or "Over Subscription nodes". Then the control goes to act 1790. In act 1790 it will be checked and if OSN is not equal to zero

then the act 1790 results in "no" and the control goes to act 1710 to start the next iteration or pass to schedule all the required multicast connections in the list of all multicast connections. Thus act 1710, act 1720, act 1730, act 1740, act 1750, act 1760, act 1770, act 1780, and act 1790 are executed in a loop to implement different passes or iterations of scheduling the set of all multicast connections. If the act 1790 results in "yes", that means no link in the complete multistage network is taken by more than one multicast connection and hence the scheduling is successfully completed.

Each multicast connection of the type described above in reference to method 1700 of FIG. 17 can be unicast connection, a multicast connection or a broadcast connection, depending on the example.

Inter-block and Intra-block Scheduling Method Embodiments the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$:

FIG. 18 shows a high-level flowchart of a scheduling method 1800, in one embodiment executed to setup multicast connections in the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ disclosed in this invention in two steps (one for each act 1810 and act 1820 as shown in FIG. 18) namely: 1) scheduling the set of multicast connections outside the blocks of 2D-grid of blocks with each block corresponding to a partial multi-stage network, or in between the blocks of the complete multi-stage network, or alternatively on the external wires of the complete multi-stage network hereinafter "inter-block scheduling". Inter-block scheduling is implemented in act 1810 so that there are no OSN nodes. During inter-block scheduling the partial multi-stage hierarchical network corresponding to each block is considered as a single stage network or alternatively each internal wire of the partial multi-stage hierarchical network is directly connected to each outgoing wire or external wire of the partial multi-stage hierarchical network, and 2) scheduling the set of multicast connections inside the blocks of 2D-grid of blocks with each block corresponding to a partial multi-stage network or alternatively on the internal wires of the complete multi-stage network hereinafter "intra-block scheduling". The act 1820 implements intra-block scheduling for each block so that there are no OSN nodes.

The act 1810 may be implemented by the scheduling method 1700 of FIG. 17. Similarly in act 1820 for each block of the multi-stage hierarchical network, the inter-block scheduling may be implemented by the scheduling method 1700 of FIG. 17.

In accordance with the current invention, the scheduling method 1700 of FIG. 17 and the scheduling method 1800 of FIG. 18 are applicable to either partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100A of FIG. 1A, or partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100B of FIG. 1B, or partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C, corresponding to a block of 2D-grid of blocks 800 of FIG. 8, using any one of the embodiments of 200A-200F of FIGs. 2A-2F, 900A-900E of FIGs. 9A-9E, 1000A-1000F of FIGs. 10A-10F, 1100A-1100C of FIGs. 11A-11C to implement a stage of a ring of the multi-stage hierarchical network, either by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, 300E of FIG. 3E, 500A of FIG. 5A, 1200 of FIG. 12, 1300 of FIG. 13, 1400 of FIG. 14, and 1500 of FIG. 15 or by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may be any one of the embodiments of either the diagrams 400A of FIG. 4A, 400B of FIG. 4B, 600A of FIG. 6A, or 600B of FIG. 6B is very efficient in the reduction of the die size, power consumption, and highly optimized for lower wire/path delay for higher performance for practical routing applications to particularly to set up broadcast, unicast and multicast connections.

Numerous modifications and adaptations of the embodiments, implementations, and examples described herein will be apparent to the skilled artisan in view of the disclosure.

REMARKS

Applicant respectfully submits that entry of the foregoing Amendment pursuant to Rule 312 (37 C.F.R. § 1.312) does not raise any new issues. Consequently, pursuant to Rule 312, it is requested that the foregoing Amendment be entered.

CONCLUSION

For all of the above reasons, applicant submits that the amendments to abstract, cross reference to related applications, summary of invention, and amendments to specification are now in proper form. Therefore applicant submits that this application is now in condition for allowance, which action he respectfully solicits.

Conditional request for Constructive Assistance

Applicant has amended the claims of this application so that they are proper, definite, and define novel structure which is also unobvious. If, for any reason this application is not believed to be in full condition for allowance, applicant respectfully request the constructive assistance and suggestions of the Examiner pursuant to M.P.E.P § 2173.02 and § 707.07(j) in order that the undersigned can place this application in allowable condition as soon as possible and without the need for further proceedings.

Very respectfully,

/Venkat Konda/

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16/562,450	09/06/2019	Venkat Konda	V-0060US	6438

TITLE OF INVENTION: FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	02/18/2021

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/562,450	09/06/2019	Venkat Konda	V-0060US	6438

TITLE OF INVENTION: FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	02/18/2021

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GIDADO, RASHEED	2464	370-411000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/562,450	09/06/2019	Venkat Konda	V-0060US	6438

38139 7590 11/18/2020

Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

EXAMINER	
GIDADO, RASHEED	
ART UNIT	**PAPER NUMBER**
2464	

DATE MAILED: 11/18/2020

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/562,450	Applicant(s) Konda, Venkat	
	Examiner RASHEED GIDADO	Art Unit 2464	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 11/09/2020.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-20 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/RASHEED GIDADO/
Primary Examiner, Art Unit 2464

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/562,450	Konda, Venkat
	Examiner	Art Unit
	RASHEED GIDADO	2464

CPC - Searched*		
Symbol	Date	Examiner
H04L49/1515,102	08/03/2020	RG

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Inventor/Assignee Search in EAST	08/03/2020	RG
Inventor/Assignee Search in PALM	08/03/2020	RG
EAST (USPAT, USPGPUB, EPO, DERWENT, FPRS) Search	08/03/2020	RG
IEEE, IP.COM, Google Patent Search	08/03/2020	RG
H04L49/1515,102 with text search	08/03/2020	RG
Updated EAST Search History	11/11/2020	RG
ProQuest Search	11/15/2020	RG

/RASHEED GIDADO/ Primary Examiner, Art Unit 2464	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/562,450	Konda, Venkat
	Examiner	Art Unit
	RASHEED GIDADO	2464

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	Interference Search History Printout	11/11/2020	RG

/RASHEED GIDADO/ Primary Examiner, Art Unit 2464	

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/562,450	Konda, Venkat
	Examiner	**Art Unit**
	RASHEED GIDADO	2464

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☑ Claims renumbered in the same order as presented by applicant ☑ CPA ☑ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/03/2020	11/15/2020							
	1	✓	=							
	2	✓	=							
	3	✓	=							
	4	✓	=							
	5	✓	=							
	6	✓	=							
	7	✓	=							
	8	✓	=							
	9	✓	=							
	10	✓	=							
	11	✓	=							
	12	✓	=							
	13	✓	=							
	14	✓	=							
	15	✓	=							
	16	✓	=							
	17	✓	=							
	18	✓	=							
	19	✓	=							
	20	✓	=							

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/562,450	Konda, Venkat
	Examiner	**Art Unit**
	RASHEED GIDADO	2464

CPC						
Symbol					**Type**	**Version**
H04L	/	49	/	1515	F	2013-01-01
H04L	/	49	/	102	I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/RASHEED GIDADO/ Primary Examiner, Art Unit 2464	15 November 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1B

U.S. Patent and Trademark Office — Part of Paper No.: 20201115

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/562,450	Konda, Venkat
	Examiner	**Art Unit**
	RASHEED GIDADO	2464

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H04L	/	12	/	933

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/RASHEED GIDADO/ Primary Examiner, Art Unit 2464	15 November 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1B

U.S. Patent and Trademark Office — Part of Paper No.: 20201115

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/562,450	Konda, Venkat
	Examiner	Art Unit
	RASHEED GIDADO	2464

☑ Claims renumbered in the same order as presented by applicant ☑ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10		19										
	2		11		20										
	3		12												
	4		13												
	5		14												
	6		15												
	7		16												
	8		17												
	9		18												

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/RASHEED GIDADO/ Primary Examiner, Art Unit 2464	15 November 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1B

U.S. Patent and Trademark Office Part of Paper No.: 20201115

Dialog

STIC
Scientific and Technical Information Center

Search Strategy from Dialog

November 15 2020 20:22

Search Strategy

Databases: Inspec®

Set#	Searched for	Results
S1	(("Uturn switch" or "U-turn switch") near/40 multiplexer) near/40 ("multistage network" or "multi-stage network")	0°
S2	("Uturn switch" or "U-turn switch") near/40 ("multistage network" or "multi-stage network")	0°
S3	multiplexer near/40 ("multistage network" or "multi-stage network")	3°
S4	(multiplexer near/40 ring) near/40 stage	19°
S5	(multiplexer near/40 (link or path or route)) near/40 stage	57°
S6	((switch near/40 multiplexer) near/40 (link or path or route)) near/40 stage	10°
S7	((switch near/40 multiplexer) near/40 (link or path or route)) near/40 (hop near/2 wire)	0°

° Duplicates are removed from the search and from the result count.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	3	"14199168"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 11:41
S2	932	H04L49/1515.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:01
S3	11,172	370/254.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:01
S4	86	Venkat near2 Konda.in.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:02
S5	7	"20110037498"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:05
S6	3	"20030117945"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:09
S7	2	"20030117946"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:10
S8	142	("6088353" "8830993" "8898611" "20120269190" "20140313930" "20150046895" "20150049768" "6237006" "6425007" "7392488" "7725499" "7945854" "7945854" "20020169801" "20050273730" "20080104002" "20100333038" "20130339918" "20140072777"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2015/09/30 12:26

		"5590250" "6018523" "6091723" "6829618" "6901575" "7086824" "7310786" "8661371" "8719737" "8850367" "9122838" "20020083410" "20060190847" "20070268731" "20130204584" "20140189611" "20140372958" "20150186340" "20150217889" "3561509" "3589243" "3589249" "4442150" "4599802" "4976553" "5284404" "5295280" "5448687" "5701416" "6060641" "6082056").pn.				
S9	1,433	370/386.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:27
S10	17	hierarchical near2 (rout$3 or network) same (two-dimension$3 or 2-D) same switch	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:29
S11	36	stage same block same (two-dimension$3 or 2-D) same switch	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:30
S12	28	S11 not S10	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:33
S13	3	"6091723".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:37
S14	3	"20120269190"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:56
S15	5	"14329876"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/17 20:15
S16	971	H04L49/1515,202.cpc.	US-PGPUB; USPAT;	ADJ	ON	2016/01/17 20:58

			FPRS; EPO; JPO; DERWENT			
S17	507	370/411.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/17 20:58
S18	17	hierarchical near2 (rout$3 or network) same (two-dimension$3 or 2-D) same switch	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/17 20:58
S19	1,602	(rout$3 or network) same (two-dimension$3 or 2-D) same switch	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/17 20:59
S20	19	S19 and S16	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/17 20:59
S21	10	S19 and S17	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/17 20:59
S22	248	stage same switch and (rout$3 or network) same (two-dimension$3 or 2-D) same switch	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/17 21:00
S23	75	link$3 same stage same switch and (rout$3 or network) same (two-dimension$3 or 2-D) same switch	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/17 21:00
S24	2	"8898611".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/18 11:15
S25	2	"6335930".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/18 11:35

S26	2	"8898611".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/07/07 12:37
S27	920	(network or sub$1network) with (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/07/07 13:21
S28	7	(network or sub$1network) with (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same (inlet or input) near2 link	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/07/07 13:22
S29	81	switch same (network or sub$1network) with (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/07/07 13:23
S30	49	switch same (network or sub$1network) with (partition$3 or divid$3 or split$4) with (block or slic$3) same link	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/07/07 13:24
S31	2	multiplexer same switch same (network or sub$1network) with (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/07/07 13:24
S32	8	"20030012222"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/07/07 13:49
S33	2	"20090181703"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/07/07 13:53
S40	9	"9509634".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/02/15 14:08
S41	0	"15331855"	US-PGPUB; USPAT; FPRS; EPO;	ADJ	ON	2017/02/15 14:11

			JPO; DERWENT			
S42	3	"14384853"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/02/16 10:38
S43	5	"14199168"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/02/16 11:57
S44	2,096	H04L49/1515,102.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/02/16 18:38
S45	26	multiplexer same switch same (network or sub$1network) same (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/07/19 21:35
S46	167	(channel or path or link$3) same stage same switch and (rout$3 or network) same (two-dimension$3 or 2-D) same switch	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/07/19 21:36
S47	7	"14329876"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/11/12 18:45
S52	1	"15884911"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/12/20 13:41
S53	6	"9929977".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/12/20 13:42
S54	2,408	H04L49/1515,102.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/12/20 13:58

S55	98	venkat near2 Konda.in.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/12/20 13:58
S56	44	(BSS ID or BSS-ID or BSSID or BSS identifier or BSS identification) same (plurality or multiple or several or different) near2 (BSS or basic service set) same (color or colour)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/12/20 15:43
S57	6	"9942193".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/12/20 15:46
S58	252	circuit with multi$1stage near3 (network or system) same (link or channel or path)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2019/03/29 16:59
S62	65	((("KONDA") near3 ("Venkat"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2019/03/31 23:12
S63	67	switch same (network or sub$1network) with (partition$3 or divid$3 or split$4) with (block or slic$3) same link	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2019/03/31 23:24
S64	67	S63	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2019/03/31 23:24
S65	31	multiplexer same switch same (network or sub$1network) same (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2019/03/31 23:24
S66	31	S65	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2019/03/31 23:24
S70	1	"16562450"	US-PGPUB; USPAT; FPRS; EPO;	ADJ	ON	2020/08/03 09:44

			JPO; DERWENT			
S71	2,701	H04L49/1515,102.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 10:28
S72	16,129	370/254,386,411.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 10:29
S73	106	S71 and S72	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 10:29
S74	107	venkat near2 konda.in.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 10:29
S75	29	(mux or multiplexer or multiplex$3) same switch and S74	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 10:34
S76	2	(multiple or several or different or two or many or pluralit$3 or first or second$3) near2 (logic block or programmable logic) with ("same" or similar or identical or different) with (link or channel or path or port or interface) and (multiple or several or different or two or many or pluralit$3 or first or second$3) near2 (subnetwork or sub$1network or mini$1network or mininetwork or partial network or partial multistage network or partial multi$1stage network) with ("same" or similar or identical or different) with (slice or ring or stage)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:08
S77	1	switch with (mux or multiplexer or multiplexing device or multiplexing node) same (subnetwork or partial network or mini$1network multi$1stage network or multistage network or sub$1network) and (U$1turn switch or U-switch or turn switch)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:41

S78	2	"8269523".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:48
S79	2	"8898611".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:49
S80	5	"9529958".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:49
S81	2	"8270400".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:49
S82	2	"8170040".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:49
S83	2	"8363649".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:50
S84	4	"6185220".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:51
S85	2	"6940308".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:51
S86	4	"5451936".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:51
S87	6	"6018523".pn.	US-PGPUB; USPAT; FPRS; EPO;	ADJ	ON	2020/08/03 11:52

			JPO; DERWENT			
S88	4	"5153843".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:52
S89	72	(mux or multiplexer or multiplexing device or multiplexing node) same stage same switch and (rout$3 or network) same (two-dimension$3 or 2-D) same switch	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:53
S90	3	internal near2 (hop wire or wire or hop cable) same external near2 (hop wire or wire or hop cable) same (Two or more or plurality or multiple or several) near2 link same (mux or multiplexer or multiplexing device or multiplexing node)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 12:27
S91	88	(multi$1stage or multistage) near2 network and internal near2 (hop wire or wire or hop cable) or external near2 (hop wire or wire or hop cable) same (mux or multiplexer or multiplexing device or multiplexing node)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 12:28
S92	1,803	(multi or plurality or two or more or multiple) near2 stage same (inward or inlet or incoming or input) near2 (link or channel or path) same (outward or output or outlet or outgoing) near2 (link or channel or path)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/11/11 19:20
S93	438	(multi or plurality or two or more or multiple) near2 stage with (network or system) same (inward or inlet or incoming or input) near2 (link or channel or path) same (outward or output or outlet or outgoing) near2 (link or channel or path)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/11/11 19:21
S94	10,456	(two or more or multiple or different or plurality) same switch same (inward or inlet or incoming or input) near2 (link or channel or path) same (outward or output or outlet or outgoing) near2 (link or channel or path)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/11/11 19:23
S95	509	S94 and S92	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/11/11 19:24

S96	178	S94 and S93	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/11/11 19:24
S97	12	U$1turn near3 switch and S93	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/11/11 19:25
S98	12	U$1turn near3 switch and S92	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/11/11 19:26
S99	12	U$1turn near3 switch and S94	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/11/11 19:26

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S34	228	H04L49/1515.cpc.	USPAT	ADJ	ON	2016/07/07 13:35
S35	228	H04L49/1515,202.cpc.	USPAT	ADJ	ON	2016/07/07 13:35
S36	11	Venkat near2 Konda.in.	USPAT	ADJ	ON	2016/07/07 13:35
S37	14	stage same block same (two-dimension$3 or 2-D) same switch	USPAT	ADJ	ON	2016/07/07 13:36
S38	49	link$3 same stage same switch and (rout$3 or network) same (two-dimension$3 or 2-D) same switch	USPAT	ADJ	ON	2016/07/07 13:36
S39	37	switch same (network or sub$1network) with (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	USPAT	ADJ	ON	2016/07/07 13:36
S48	42	switch same (network or sub$1network) with (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	USPAT	ADJ	ON	2017/11/12 18:04
S49	5	hierarchical near2 (rout$3 or network) same (two-dimension$3 or 2-D) same switch	USPAT	ADJ	ON	2017/11/12 18:04

S50	266	H04L49/1515,202.cpc.	USPAT	ADJ	ON	2017/11/12 18:04
S51	1	"14329876"	USPAT	ADJ	ON	2017/11/12 18:44
S59	920	H04L49/1515,102.cpc.	US-PGPUB; USPAT	ADJ	ON	2019/03/29 16:58
S60	45	venkat near2 Konda.in.	US-PGPUB; USPAT	ADJ	ON	2019/03/29 16:58
S61	146	circuit with multi$1stage near3 (network or system) same (link or channel or path)	US-PGPUB; USPAT	ADJ	ON	2019/03/29 16:59
S67	22	multiplexer same switch same (network or sub$1network) same (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	US-PGPUB; USPAT	ADJ	ON	2019/03/31 23:23
S68	89	switch same (network or sub$1network) with (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	US-PGPUB; USPAT	ADJ	ON	2019/03/31 23:23
S69	920	H04L49/1515,102.cpc.	US-PGPUB; USPAT	ADJ	ON	2019/03/31 23:24

11/15/2020 8:24:01 PM
C:\Users\rgidado\Documents\EAST\Workspaces\16562450.wsp

Electronic Acknowledgement Receipt

EFS ID:	41065215
Application Number:	16562450
International Application Number:	
Confirmation Number:	6438
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkat Konda
Filer Authorized By:	
Attorney Docket Number:	V-0060US
Receipt Date:	09-NOV-2020
Filing Date:	06-SEP-2019
Time Stamp:	06:06:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	Amndmnt-V_0060.pdf	319570 b6a7823d6aabb602171ae07360fb2fa2d47379c8	no	38

Warnings:

Information:					
2	Drawings-only black and white line drawings	V-0060US-Figs-mkup-rplc.pdf	167045 6c6f3df5a8261c9e8ad395c8b68addd03af692f0	no	6
Warnings:					
Information:					
			Total Files Size (in bytes):	486615	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

AMENDMENT

In The United States Patent And Trademark Office

Application Number: 16/562,450

Application Filed: 9/6/2019

Applicant(s): Venkat Konda

Title: Fast Scheduling and Optimization of Multi-stage Hierarchical Networks

Examiner/Art Unit: Rasheed Gidado / 2464

San Jose, 2020 November 9, Mon

AMENDMENT

(And the response to office letter dated August 7, 2020)

Mail Stop Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, Virginia, 22313-1450

Dear Sir/Madam:

This replies to the office action from the United States Patent and Trademark Office mailed on August 7, 2020 in connection with the above-identified patent application. Pursuant to 37 CFR § 1.121, applicant respectfully requests that the above application be amended as follows:

In response to the amendments to the fix the minor errors in the specification, pursuant to 37 CFR § 1.121, applicant respectfully requests that the above application

further be amended as follows:

IN RESPONSE, AMENDMENTS TO THE SPECIFICATION (ABSTRACT OF THE DISCLOSURE) begin on page 3 of this paper.

IN RESPONSE, AMENDMENTS TO THE SPECIFICATION (CROSS REFERENCE TO RELATED APPLICATIONS) begin on page 3 of this paper.

IN RESPONSE, AMENDMENTS TO THE SPECIFICATION (SUMMARY OF INVENTION) begin on page 4 of this paper.

IN RESPONSE, AMENDMENTS TO THE DRAWINGS begin on page 6 of this paper and include both an attached replacement sheet and an annotated sheet showing changes.

IN RESPONSE, AMENDMENTS TO THE SPECIFICATION (DETAILED DESCRPTION OF THE INVENTION) begin on page 7 of this paper.

IN RESPONSE, DOUBLE PATENTING) begin on page 18 of this paper.

IN RESPONSE, AMENDMENTS TO THE CLAIMS are reflected in the listing of claims which begins on page 18 of this paper.

I. IN RESPONSE TO AMENDMENTS TO THE SPECIFICATION (ABSTRACT OF THE DISCLOSURE):

Please replace paragraph beginning at page 134, line 5 with the following amended paragraph:

Significantly optimized multi-stage networks ~~with~~ including scheduling methods for faster scheduling of connections, useful in wide target applications, with VLSI layouts using only horizontal wires and vertical ~~links~~ wires to route large scale ~~sub-integrated circuit blocks~~ partial multi-stage hierarchical networks having inlet and outlet links, and laid out in an integrated circuit device in a two-dimensional grid arrangement of blocks are ~~presented~~ disclosed. The optimized multi-stage networks in each block employ ~~several~~ one or more slices of rings of stages of switches with inlet and outlet links of ~~sub-integrated circuit blocks~~ partial multi-stage hierarchical networks connecting to rings from either ~~left-hand side only, or from right-hand side only, or from both~~ left-hand side ~~and~~ or right-hand side; and employ hop wires or multi-drop ~~links where outlet links of cross links~~ hop wires wherein hop wires or multi-drop wires are connected from switches ~~in a~~ of stages of ~~a~~ rings of slices of a first ~~in one sub-integrated circuit block~~ partial multi-stage hierarchical network ~~are connected~~ to ~~either inlet links of~~ switches ~~in the another~~ of stages of ~~a~~ rings of slices of ~~in the same or another sub-integrated circuit block~~ the first or a second partial multi-stage hierarchical network.

II. IN RESPONSE TO AMENDMENTS TO THE SPECIFICATION (CROSS REFERENCE TO RELATED APPLICATIONS):

Please replace paragraph beginning at page 1, line 6 with the following amended paragraph:

This application is Continuation Application and claims priority to US Application Serial No. 15/884,911 entitled "FAST SCHEDULING AND OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed January 31, 2018, which is Continuation Application and claims priority to US Application Serial No. 15/331,855 entitled "FAST SCHEDULING AND OPTIMIZATION OF MULTI-STAGE

HIERARCHICAL NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed October 22, 2016, issued as US Patent No. 9,929,977 on March 27, 2018, which is Continuation Application and claims priority to US Application Serial No. 14/329,876 entitled "FAST SCHEDULING AND OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed July 11, 2014, issued as US Patent No. 9,509,634 on November 29, 2016, which claims priority to U.S. Provisional Patent Application Serial No. 61/846,083 entitled "FAST SCHEDULING AND OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed July 15, 2013, and also Continuation-in-Part Application and claims priority to US Application Serial No. US14/199,168 entitled "OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS FOR PRACTICAL ROUTING APPLICATIONS" by Venkat Konda assigned to the same assignee as the current application, filed March 6, 2014, issued as US Patent No. 9,374,322 on June 21, 2016, which in turn is bypass continuation application and claims priority to PCT Application Serial No. PCT/US12/53814 entitled "OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS FOR PRACTICAL ROUTING APPLICATIONS" by Venkat Konda assigned to the same assignee as the current application, filed September 6, 2012, which is Continuation-in-Part application and claims priority to U.S. Provisional Patent Application Serial No. 61/531,615 entitled "OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS FOR PRACTICAL ROUTING APPLICATIONS" by Venkat Konda assigned to the same assignee as the current application, filed September 7, 2011.

III. IN RESPONSE TO AMENDMENTS TO THE SPECIFICATION (SUMMARY OF INVENTION):

Please amend page 6, line 3 to page 7, line 10 of the summary of invention as follows:

Significantly optimized multi-stage networks for faster scheduling of connections, useful in wide target applications, with VLSI layouts (or floor plans) using only

horizontal wires and vertical ~~links~~ wires to route large scale ~~sub-integrated circuit blocks~~ partial multi-stage hierarchical networks having inlet and outlet links, and laid out in an integrated circuit device in a two-dimensional grid arrangement of blocks, (for example in an FPGA where the ~~sub-integrated circuit blocks~~ partial multi-stage hierarchical networks ~~are~~ to route Lookup Tables, or memory blocks, or DSP blocks) are ~~presented~~ disclosed. The optimized multi-stage networks in each block employ ~~several~~ one or more slices of rings of stages of switches with inlet and outlet links of ~~sub-integrated circuit blocks~~ partial multi-stage hierarchical networks connecting to rings from either ~~left-hand side only, or from right-hand side only, or from both~~ left-hand side ~~and~~ or right-hand side.

The optimized multi-stage networks ~~with their VLSI layouts~~ employ hop wires or ~~shuffle exchange~~ multi-drop ~~links where outlet links of cross links~~ hop wires wherein hop wires or multi-drop wires are connected from switches ~~in a~~ of stages of ~~a~~ rings of slices of a first ~~in one sub-integrated circuit block~~ partial multi-stage hierarchical network ~~are connected~~ to ~~either inlet links of~~ switches ~~in the another~~ of stages of ~~a~~ rings of slices of ~~in another sub-integrated circuit block~~ a second partial multi-stage hierarchical network or ~~inlet links of~~ switches ~~in the another~~ of stages of ~~a~~ rings of slices of ~~in the same sub-integrated circuit block~~ the first partial multi-stage hierarchical network so that said ~~cross links~~ hop wires or multi-drop hop wires are either vertical ~~links~~ wires or horizontal wires ~~and vice versa~~.

The VLSI layouts exploit spatial locality so that ~~different sub-integrated circuit blocks~~ partial multi-stage hierarchical networks that are spatially nearer are connected with shorter ~~shuffle exchange links~~ hop wires compared to the ~~shuffle exchange links~~ hop wires between spatially farther ~~sub-integrated circuit blocks~~ partial multi-stage hierarchical networks. The optimized multi-stage networks provide high routability for broadcast, unicast and multicast connections, yet with the benefits of significantly lower cross points hence smaller area, lower signal latency, lower power and with significant fast compilation or routing time. Various scheduling methods are also disclosed to schedule a set of multicast connections in the multi-stage hierarchical network.

The optimized multi-stage networks $V_{Comb}(N_1, N_2, d, s)$ & $V_{D-Comb}(N_1, N_2, d, s)$ according to the current invention inherit the properties of one or more~~, in addition to~~

~~additional properties,~~ generalized multi-stage and pyramid networks $V(N_1, N_2, d, s)$ & $V_P(N_1, N_2, d, s)$, generalized folded multi-stage and pyramid networks $V_{fold}(N_1, N_2, d, s)$ & $V_{fold-p}(N_1, N_2, d, s)$, generalized butterfly fat tree and butterfly fat pyramid networks $V_{bft}(N_1, N_2, d, s)$ & $V_{bfp}(N_1, N_2, d, s)$, generalized multi-link multi-stage and pyramid networks $V_{mlink}(N_1, N_2, d, s)$ & $V_{mlink-p}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage and pyramid networks $V_{fold-mlink}(N_1, N_2, d, s)$ & $V_{fold-mlink-p}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree and butterfly fat pyramid networks $V_{mlink-bft}(N_1, N_2, d, s)$ & $V_{mlink-bfp}(N_1, N_2, d, s)$, generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$, and generalized cube connected cycles networks $V_{CCC}(N_1, N_2, d, s)$ for s = 1,2,3 or any number in general.

IV. IN RESPONSE TO AMENDMENTS TO THE DRAWINGS:

Attached hereto is a replacement diagram of FIG. 2A to illustrate two exemplary 180-degree U-turn paths in diagram 200A of FIG. 2A shown by two types of dotted lines.

Attached hereto is a marked-up sheet showing amendments to FIG. 2C, FIG. 2E, and FIG. 3B. Also enclosed is a replacement sheet for amended FIG. 2C, FIG. 2E, and FIG. 3B. The amendments to the drawings of FIG. 2C, FIG. 2E, and FIG. 3B are to correct the labels of the F, B, R and U Muxes to be consistent with the other drawings.

Next, pursuant to 37 C.F.R. § 1.83(a) attached hereto is a marked-up sheet showing amendments to FIG. 3B. Also enclosed is a replacement sheet for amended FIG. 3B.

The amendment to FIG. 3B is supported first by the original specification of the present application referring to pyramid networks disclosed on Page 17, lines 5 – 21. These pyramid networks are first disclosed at Page 75, lines 19 – 20, Page 79, lines 26 –

29, and Page 96, lines 4 – 12, of US Application Serial No. 13/502,207 issued as US Patent No. 8,898,611 which is incorporated by reference in its entirety.

V. IN RESPONSE TO AMENDMENTS TO THE SPECIFICATION (DETAILED DESCRPTION OF THE INVENTION)

Next, Please amend Page 46, lines 14 – 23 of the specification as follows:

FIG. 2C illustrates a stage (ring "k", stage "m") 200C consists of 4 inputs namely Fi(k,2m+1), Fi(k,2m+2), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Uo(k,2m+1), Uo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of four 2:1 Muxes namely F(k,2m+1), F(k,2m+2), U(k,2m+1), and U(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Ui(k,2m+2) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+1) and Ui(k,2m+2) and has one output Uo(k,2m+2).

An unedited version of amended Page 46, lines 14 – 23 appears below:

FIG. 2C illustrates a stage (ring "k", stage "m") 200C consists of 4 inputs namely Fi(k,2m+1), Fi(k,2m+2), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Uo(k,2m+1), Uo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of four 2:1 Muxes namely F(k,2m+1), F(k,2m+2), U(k,2m+1), and U(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Ui(k,2m+2) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+1) and Ui(k,2m+2) and has one output Uo(k,2m+2).

Next, please amend Page 47, lines 4 - 23 of the specification as follows:

The stage "m" of ring "k" with "m" stages of the partial multi-stage pyramid network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 8 inputs and 4 outputs as shown in diagram 200E in FIG. 2E. FIG. 2E illustrates a stage (ring "k", stage "m") 200E consists of 8 inputs namely FRi(k,2m+1), FRi(k,2m+2), BUi(k,2m+1), BUi(k,2m+2), J, K, L, and M; and 4 outputs UBo(k,2m+1), UBo(k,2m+2), RFo(k,2m+1), and RFo(k,2m+2). The stage (ring "k", stage "m") also consists of eight 2:1 Muxes namely FR(k,2m+1), FR(k,2m+2), RF(k,2m+1), RF(k,2m+2), BU(k,2m+1), BU(k,2m+2), UB(k,2m+1), and UB(k,2m+2). The 2:1 Mux R(k,2m+1) has two inputs namely FRi(k,2m+1) and J, and has one output FRo(k,2m+1). The 2:1 Mux FR(k,2m+2) has two inputs namely FRi(k,2m+2) and K, and has one output FRo(k,2m+2). The 2:1 Mux RF(k,2m+1) has two inputs namely FRo(k,2m+1) and BUo(k,2m+2), and has one output RFo(k,2m+1). The 2:1 Mux RF(k,2m+2) has two inputs namely FRo(k,2m+2) and BUo(k,2m+1), and has one output RFo(k,2m+2).

The 2:1 Mux BU(k,2m+1) has two inputs namely BUi(k,2m+1) and L, and has one output BUo(k,2m+1). The 2:1 Mux BU(k,2m+2) has two inputs namely BUi(k,2m+2) and M, and has one output BUo(k,2m+2). The 2:1 Mux UB(k,2m+1) has two inputs namely BUo(k,2m+1) and FRo(k,2m+2), and has one output UBo(k,2m+1). The 2:1 Mux UB(k,2m+2) has two inputs namely BUo(k,2m+2) and FRo(k,2m+1), and has one output UBo(k,2m+2). In different embodiments the inputs J, K, L, and M are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

An unedited version of amended Page 47, lines 4 - 23 appears below:

The stage "m" of ring "k" with "m" stages of the partial multi-stage pyramid network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 8 inputs and 4 outputs as shown in diagram 200E in FIG. 2E. FIG. 2E illustrates a stage (ring "k", stage "m") 200E consists of 8 inputs namely Fi(k,2m+1), Fi(k,2m+2), Bi(k,2m+1), Bi(k,2m+2), J, K, L, and M; and 4 outputs Uo(k,2m+1), Uo(k,2m+2), Ro(k,2m+1), and Ro(k,2m+2). The stage (ring "k", stage "m") also consists of eight 2:1 Muxes namely F(k,2m+1), F(k,2m+2), R(k,2m+1), R(k,2m+2), B(k,2m+1), B(k,2m+2), U(k,2m+1), and U(k,2m+2). The 2:1 Mux R(k,2m+1) has two inputs namely Fi(k,2m+1) and J, and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Fi(k,2m+2) and K, and has one output Fo(k,2m+2). The 2:1 Mux R(k,2m+1) has two inputs namely Fo(k,2m+1) and Bo(k,2m+2), and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Fo(k,2m+2) and Bo(k,2m+1) , and has one output Ro(k,2m+2).

The 2:1 Mux B(k,2m+1) has two inputs namely Bi(k,2m+1) and L, and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Bi(k,2m+2) and M, and has one output Bo(k,2m+2). The 2:1 Mux U(k,2m+1) has two inputs namely Bo(k,2m+1) and Fo(k,2m+2), and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Bo(k,2m+2) and Fo(k,2m+1), and has one output Uo(k,2m+2). In different embodiments the inputs J, K, L, and M are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Next, please amend Page 55, line 4 to Page 57, line 22 of the specification as follows:

The stage (ring "x", stage "p") consists of 8 inputs namely FRi(x,2p+1), FRi(x,2p+2), BUi(x,2p+1), BUi(x,2p+2), J1, K1, L1, and M1; and 4 outputs URo(x,2p+1), URo(x,2p+2), RFo(x,2p+1), and RFo(x,2p+2). The stage (ring "x", stage "p') also consists of eight 2:1 Muxes namely FR(x,2p+1), FR(x,2p+2), RF(x,2p+1), RF(x,2p+2), BU(x,2p+1), BU(x,2p+2), UR(x,2p+1), and UR(x,2p+2). The 2:1 Mux FR(x,2p+1) has two inputs namely FRi(x,2p+1) and J1, and has one output FRo(x,2p+1). The 2:1 Mux FR(x,2p+2) has two inputs namely FRi(x,2p+2) and K1, and has one output FRo(x,2p+2). The 2:1 Mux RF(x,2p+1) has two inputs namely FRo(x,2p+1) and BUo(x,2p+2), and has one output RFo(x,2p+1). The 2:1

Mux RF(x,2p+2) has two inputs namely FRo(x,2p+2) and BUo(x,2p+1), and has one output RFo(x,2p+2).

The 2:1 Mux BU(x,2p+1) has two inputs namely BUi(x,2p+1) and L1, and has one output BUo(x,2p+1). The 2:1 Mux BU(x,2p+2) has two inputs namely BUi(x,2p+2) and M1, and has one output BUo(x,2p+2). The 2:1 Mux UB(x,2p+1) has two inputs namely BUo(x,2p+1) and FRo(x,2p+2), and has one output UBo(x,2p+1). The 2:1 Mux UB(x,2p+2) has two inputs namely BUo(x,2p+2) and FRo(x,2p+1), and has one output UBo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 8 inputs namely FRi(x,2p+3), FRi(x,2p+4), BUi(x,2p+3), BUi(x,2p+4), J2, K2, L2, and M2; and 4 outputs UBo(x,2p+3), UBo(x,2p+4), RFo(x,2p+3), and RFo(x,2p+4). The stage (ring "x", stage "p+1") also consists of eight 2:1 Muxes namely FR(x,2p+3), FR(x,2p+4), RF(x,2p+3), RF(x,2p+4), BU(x,2p+3), BU(x,2p+4), UB(x,2p+3), and UB(x,2p+4). The 2:1 Mux FR(x,2p+3) has two inputs namely FRi(x,2p+3) and J2, and has one output FRo(x,2p+3). The 2:1 Mux FR(x,2p+4) has two inputs namely FRi(x,2p+4) and K2, and has one output FRo(x,2p+4). The 2:1 Mux RF(x,2p+3) has two inputs namely FRo(x,2p+3) and BUo(x,2p+4), and has one output RFo(x,2p+3). The 2:1 Mux RF(x,2p+4) has two inputs namely FRo(x,2p+4) and BUo(x,2p+3), and has one output RFo(x,2p+4).

The 2:1 Mux BU(x,2p+3) has two inputs namely BUi(x,2p+3) and L2, and has one output BUo(x,2p+3). The 2:1 Mux BU(x,2p+4) has two inputs namely BUi(x,2p+4) and M2, and has one output BUo(x,2p+4). The 2:1 Mux UB(x,2p+3) has two inputs namely BUo(x,2p+3) and FRo(x,2p+4), and has one output UBo(x,2p+3). The 2:1 Mux UB(x,2p+4) has two inputs namely BUo(x,2p+4) and FRo(x,2p+3), and has one output UBo(x,2p+4).

The output RFo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input FRi(x,2p+3) of the stage (ring "x", stage "p+1"). And the output UBo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input BUi(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 8 inputs namely FRi(y,2q+1), FRi(y,2q+2), BUi(y,2q+1), BUi(y,2q+2), J3, K3, L3, and M3; and 4 outputs UBo(y,2q+1), UBo(y,2q+2), RFo(y,2q+1), and RFo(y,2q+2). The stage (ring "y", stage "q') also consists of eight 2:1 Muxes namely FR(y,2q+1), FR(y,2q+2), RF(y,2q+1), RF(y,2q+2), BU(y,2q+1), BU(y,2q+2), UB(y,2q+1), and UB(y,2q+2). The 2:1 Mux FR(y,2q+1) has two inputs namely FRi(y,2q+1) and J3, and has one output FRo(y,2q+1). The 2:1 Mux FR(y,2q+2) has two inputs namely FRi(y,2q+2) and K3, and has one output FRo(y,2q+2). The 2:1 Mux RF(y,2q+1) has two inputs namely FRo(y,2q+1) and BUo(y,2q+2), and has one output RFo(y,2q+1). The 2:1 Mux RF(y,2q+2) has two inputs namely FRo(y,2q+2) and BUo(y,2q+1) and has one output RFo(y,2q+2).

The 2:1 Mux BU(y,2q+1) has two inputs namely BUi(y,2q+1) and L3, and has one output BUo(y,2q+1). The 2:1 Mux BU(y,2q+2) has two inputs namely BUi(y,2q+2) and M3, and has one output BUo(y,2q+2). The 2:1 Mux UB(y,2q+1) has two inputs namely BUo(y,2q+1) and FRo(y,2q+2), and has one output UBo(y,2q+1). The 2:1 Mux UB(y,2q+2) has two inputs namely BUo(y,2q+2) and FRo(y,2q+1), and has one output UBo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 8 inputs namely FRi(y,2q+3), FRi(y,2q+4), BUi(y,2q+3), BUi(y,2q+4), J4, K4, L4, and M4; and 4 outputs UBo(y,2q+3), UBo(y,2q+4), RFo(y,2q+3), and RFo(y,2q+4). The stage (ring "y", stage "q+1") also consists of eight 2:1 Muxes namely FR(y,2q+3), FR(y,2q+4), RF(y,2q+3), RF(y,2q+4), BU(y,2q+3), BU(y,2q+4), UB(y,2q+3), and UB(y,2q+4). The 2:1 Mux FR(y,2q+3) has two inputs namely FRi(y,2q+3) and J4, and has one output FRo(y,2q+3). The 2:1 Mux FR(y,2q+4) has two inputs namely FRi(y,2q+4) and K4, and has one output FRo(y,2q+4). The 2:1 Mux RF(y,2q+3) has two inputs namely FRo(y,2q+3) and BUo(y,2q+4), and has one output RFo(y,2q+3). The 2:1 Mux RF(y,2q+4) has two inputs namely FRo(y,2q+4) and BUo(y,2q+3), and has one output RFo(y,2q+4).

The 2:1 Mux BU(y,2q+3) has two inputs namely BUi(y,2q+3) and L4, and has one output BUo(y,2q+3). The 2:1 Mux BU(y,2q+4) has two inputs namely BUi(y,2q+4) and M4, and has one output BUo(y,2q+4). The 2:1 Mux UB(y,2q+3)

has two inputs namely BUo(y,2q+3) and FRo(y,2q+4), and has one output UBo(y,2q+3). The 2:1 Mux UB(y,2q+4) has two inputs namely BUo(y,2q+4) and FRo(y,2q+3), and has one output UBo(y,2q+4).

The output RFo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input FRi(y,2q+3) of the stage (ring "y", stage "q+1"). And the output UBo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input BUi(y,2q+1) of the stage (ring "y", stage "q").

The output UFo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input BRi(y,2q+24) of the stage (ring "y", stage "q+1"). The output RBo(yx,2qp+24) of the stage (ring "yx", stage "qp+1") is connected via the wire Hop(1,2) to the input FUi(xy,2pq+2) of the stage (ring "xy", stage "pq").

The output UFo(xy,2pq+42) of the stage (ring "xy", stage "pq+1") is connected via the wire Hop(2,1) to the input BRi(yx,2qp+4) of the stage (ring "yx", stage "qp+1"). The output RBo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to the input FUi(x,2p+42) of the stage (ring "x", stage "p+1").

An unedited version of amended Page 55, line 4 to Page 57, line 22 appears below:

The stage (ring "x", stage "p") consists of 8 inputs namely Fi(x,2p+1), Fi(x,2p+2), Bi(x,2p+1), Bi(x,2p+2), J1, K1, L1, and M1; and 4 outputs Uo(x,2p+1), Uo(x,2p+2), Ro(x,2p+1), and Ro(x,2p+2). The stage (ring "x", stage "p') also consists of eight 2:1 Muxes namely F(x,2p+1), F(x,2p+2), R(x,2p+1), R(x,2p+2), B(x,2p+1), B(x,2p+2), U(x,2p+1), and U(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Fi(x,2p+1) and J1, and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Fi(x,2p+2) and K1, and has one output Fo(x,2p+2). The 2:1 Mux R(x,2p+1) has two inputs namely Fo(x,2p+1) and Bo(x,2p+2), and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Fo(x,2p+2) and Bo(x,2p+1), and has one output Ro(x,2p+2).

The 2:1 Mux B(x,2p+1) has two inputs namely Bi(x,2p+1) and L1, and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Bi(x,2p+2) and M1, and has one output Bo(x,2p+2). The 2:1 Mux U(x,2p+1) has two inputs namely Bo(x,2p+1) and Fo(x,2p+2), and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Bo(x,2p+2) and Fo(x,2p+1), and has one output Uo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 8 inputs namely Fi(x,2p+3), Fi(x,2p+4), Bi(x,2p+3), Bi(x,2p+4), J2, K2, L2, and M2; and 4 outputs Uo(x,2p+3), Uo(x,2p+4), Ro(x,2p+3), and Ro(x,2p+4). The stage (ring "x", stage "p+1") also consists of eight 2:1 Muxes namely F(x,2p+3), F(x,2p+4), R(x,2p+3), R(x,2p+4), B(x,2p+3), B(x,2p+4), U(x,2p+3), and U(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely Fi(x,2p+3) and J2, and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely Fi(x,2p+4) and K2, and has one output Fo(x,2p+4). The 2:1 Mux R(x,2p+3) has two inputs namely Fo(x,2p+3) and Bo(x,2p+4), and has one output Ro(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs namely Fo(x,2p+4) and Bo(x,2p+3), and has one output Ro(x,2p+4).

The 2:1 Mux B(x,2p+3) has two inputs namely Bi(x,2p+3) and L2, and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Bi(x,2p+4) and M2, and has one output Bo(x,2p+4). The 2:1 Mux U(x,2p+3) has two inputs namely Bo(x,2p+3) and Fo(x,2p+4), and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Bo(x,2p+4) and Fo(x,2p+3), and has one output Uo(x,2p+4).

The output Ro(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Fi(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Uo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Bi(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 8 inputs namely Fi(y,2q+1), Fi(y,2q+2), Bi(y,2q+1), Bi(y,2q+2), J3, K3, L3, and M3; and 4 outputs Uo(y,2q+1), Uo(y,2q+2), Ro(y,2q+1), and Ro(y,2q+2). The stage (ring "y", stage "q') also consists of eight 2:1 Muxes namely F(y,2q+1), F(y,2q+2), R(y,2q+1), R(y,2q+2),

B(y,2q+1), B(y,2q+2), U(y,2q+1), and U(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Fi(y,2q+1) and J3, and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Fi(y,2q+2) and K3, and has one output Fo(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Fo(y,2q+1) and Bo(y,2q+2), and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Fo(y,2q+2) and Bo(y,2q+1) and has one output Ro(y,2q+2).

The 2:1 Mux B(y,2q+1) has two inputs namely Bi(y,2q+1) and L3, and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Bi(y,2q+2) and M3, and has one output Bo(y,2q+2). The 2:1 Mux U(y,2q+1) has two inputs namely Bo(y,2q+1) and Fo(y,2q+2), and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Bo(y,2q+2) and Fo(y,2q+1), and has one output Uo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 8 inputs namely Fi(y,2q+3), Fi(y,2q+4), Bi(y,2q+3), Bi(y,2q+4), J4, K4, L4, and M4; and 4 outputs Uo(y,2q+3), Uo(y,2q+4), Ro(y,2q+3), and Ro(y,2q+4). The stage (ring "y", stage "q+1") also consists of eight 2:1 Muxes namely F(y,2q+3), F(y,2q+4), R(y,2q+3), R(y,2q+4), B(y,2q+3), B(y,2q+4), U(y,2q+3), and U(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely Fi(y,2q+3) and J4, and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Fi(y,2q+4) and K4, and has one output Fo(y,2q+4). The 2:1 Mux R(y,2q+3) has two inputs namely Fo(y,2q+3) and Bo(y,2q+4), and has one output Ro(y,2q+3). The 2:1 Mux R(y,2q+4) has two inputs namely Fo(y,2q+4) and Bo(y,2q+3), and has one output Ro(y,2q+4).

The 2:1 Mux B(y,2q+3) has two inputs namely Bi(y,2q+3) and L4, and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Bi(y,2q+4) and M4, and has one output Bo(y,2q+4). The 2:1 Mux U(y,2q+3) has two inputs namely Bo(y,2q+3) and Fo(y,2q+4), and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Bo(y,2q+4) and Fo(y,2q+3), and has one output Uo(y,2q+4).

The output Ro(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Fi(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Uo(y,2q+3) of

the stage (ring "y", stage "q+1") is connected to the input Bi(y,2q+1) of the stage (ring "y", stage "q").

The output Uo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Bi(y,2q+2) of the stage (ring "y", stage "q"). The output Ro(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(1,2) to the input Fi(x,2p+2) of the stage (ring "x", stage "p").

The output Uo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(2,1) to the input Bi(y,2q+4) of the stage (ring "y", stage "q+1"). The output Ro(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to the input Fi(x,2p+4) of the stage (ring "x", stage "p+1").

Please insert at all the five following lines listed below, with --(comprising in combination a forward switch)--

1) on page 45, line 17 after "F(k,2m+1), F(k,2m+2)"
2) on page 46, line 1 after "F(k,2m+1), F(k,2m+2)"
3) on page 46, line 17 after "F(k,2m+1), F(k,2m+2)"
4) on page 46, line 29 after "F(k,2m+1), F(k,2m+2)"
5) on page 47, line 10 after "F(k,2m+1), F(k,2m+2)"

Please insert at all the four following lines listed below, with --(comprising in combination a backward switch)--

1) on page 45, lines 17 - 18 after "B(k,2m+1), B(k,2m+2)"
2) on page 46, line 2 after "B(k,2m+1), B(k,2m+2)"
3) on page 47, line 10 after "B(k,2m+1), B(k,2m+2)"

Please insert at all the five following lines listed below, with --(comprising in combination a U-turn switch)--

1) on page 45, line 17 after "U(k,2m+1), U(k,2m+2)"

2) on page 46, lines 1 - 2 after "U(k,2m+1), U(k,2m+2)"

3) on page 46, lines 17 after "U(k,2m+1), U(k,2m+2)"

4) on page 47, line 10 after "U(k,2m+1), U(k,2m+2)"

Please insert at all the four following lines listed below, with --(comprising in combination a Reverse U-turn switch)--

1) on page 46, line 1 after "R(k,2m+1), R(k,2m+2)"

2) on page 47, line 9 after "R(k,2m+1), R(k,2m+2)"

Please insert on page 7, line 13 after "computational block" with –(hereinafter alternatively referred to as "programmable logic block")--

Please insert on page 17, line 18 after "integrated circuit" with –(hereinafter alternatively referred to as "integrated circuit device" or "IC device")--

Please insert on page 19, line 5 after "an internal connection" with –(hereinafter alternatively referred to as "straight link" or "straight middle link")--

Please insert on page 65, line 4 after "vertical external hop wires" with –(hereinafter alternatively referred to as "cross links" or "cross middle links")--

Pursuant to 37 C.F.R. § 1.83(a), with the support in the original diagram 200E of FIG. 2E, please insert after page 47, line 23 two new paragraphs as follows:

"The diagram 200E of FIG 2E eliminates the 180-degree turn paths from the internal connection Fi(k,2m+1) to the internal connection Uo(k,2m+1). Similarly the diagram 200E of FIG 2E eliminates the 180-degree turn paths from the connection Fi(k,2m+2) to the connection Uo(k,2m+2). The diagram 200E of

FIG 2E eliminates the 180-degree turn paths from the internal connection Bi(k,2m+1) to the internal connection Ro(k,2m+1). Similarly the diagram 200E of FIG 2E eliminates the 180-degree turn paths from the connection Bi(k,2m+2) to the connection Ro(k,2m+2). Hence diagram 200E of FIG. 2E comprises a forward switch, a backward switch, U-turn switch and reverse U-turn switch without 180-degree U-turn paths.

In contrast to diagram 200E of FIG. 2E, the diagram 200A of FIG. 2A, diagram 200B of FIG. 2B, and diagram 200C of FIG. 2C provide 180-degree U-turn paths. Two exemplary 180-degree U-turn paths in diagram 200A of FIG. 2A are shown (by two types of dotted lines) in the attached replacement diagram of FIG. 2A. One of the 180-degree turn path shown in the replacement diagram of FIG. 2A starts at the internal connection Fi(k,2m+1) through the Mux F(k,2m+1) to Fo(k,2m+1) through the Mux U(k,2m+1) to Uo(k,2m+1) through the Mux B(k,2m+1) to the internal connection Bo(k,2m+1). The second of the 180-degree turn path shown in the replacement diagram of FIG. 2A starts at the hop wire Fi(k,2m+2) through the Mux F(k,2m+2) to Fo(k,2m+2) through the Mux U(k,2m+2) to Uo(k,2m+2) through the Mux B(k, 2m+2) to the hop wire Bo(k,2m+2)."

Pursuant to 37 C.F.R. § 1.83(b), with the support in the original diagram 200F of FIG. 2F please insert after page 48, line 10 a new paragraph as follows:

"The diagram 200F of FIG 2F eliminates the 180-degree turn paths from the internal connection Ri(k,2m+1) to the internal connection Bo(k,2m+1). Similarly the diagram 200F of FIG 2F eliminates the 180-degree turn paths from the connection Ri(k,2m+2) to the connection Bo(k,2m+2). The diagram 200F of FIG 2F eliminates the 180-degree turn paths from the internal connection Ui(k,2m+1) to the internal connection Fo(k,2m+1). Similarly the diagram 200F of FIG 2F eliminates the 180-degree turn paths from the connection Ui(k,2m+2) to the connection Fo(k,2m+2). Hence diagram 200F of FIG. 2F comprises an integrated switch of a backward switch, U-turn switch and reverse U-turn switch without 180-degree U-turn paths."

VI. IN RESPONSE TO DOUBLE PATENTING

Applicant has carefully reviewed the submission of terminal disclosures to avoid double patenting issues as follows:

U.S. Patent No. 9,929,977 is the parent patent of U.S. Patent No. 10,412,025 and so a terminal disclaimer was filed with U.S. Patent 9,929,977 and accepted. Since the current application is terminal disclaimed with U.S. Patent No. 10,412,025, the current application is in turn terminal disclaimed with U.S. patent No. 9,929,977.

U.S. patent No. 9,509,634 is the parent patent of U.S. Patent 9,929,977 and so a terminal disclaimer was filed with U.S. Patent 9,929,977 and accepted. So the current application is in turn terminal disclaimed with U.S. patent No. 9,509,634.

Applicant submits that the claims presented eliminate the double patenting issue with US Patent No. 8,898,611. US Patent No. 8,898,611 disclosed locality based optimization of various multi-stage networks to be laid out in a two-dimensional grid. Compared to the current application these optimized networks require large number of stages, require non-replicable subnetworks with respective to wires while necessitating the laborious designing of different external horizontal and vertical hop wires (or cross links) for different subnetworks. If the size of the network changes it requires completely new external hop wire design. Also these networks require long length external hop wires and require design of special routing algorithms. For the above reason, applicant respectfully submits that the claims in the current application eliminate the need for filing terminal disclaimer with US Patent No. 8,898,611.

VII. AMENDMENTS TO THE CLAIMS

Claims: Claims 1 - 9, 12, 15 - 16, and 19 of record are currently amended. Claims 10, 11, 13, 14, 17, 18, 20 of record are originally submitted claims as follows (For the above reasons, applicant respectfully submits that the currently amended claims and the remaining original claims are patentable over the cited prior art):

CLAIMS

What is claimed is:

1. (Currently Amended): ~~A programmable integrated circuit comprising a plurality of programmable logic blocks and a network,~~ A multi-stage hierarchical network comprising a plurality of partial multi-stage networks,

each ~~programmable logic block~~ partial multi-stage network of said plurality of ~~programmable logic blocks~~ partial multi-stage networks comprising a plurality of inlet links and a plurality of outlet links; and

~~said network comprising a plurality of partial multi-stage networks wherein each programmable logic block of said plurality of programmable logic blocks is coupled with at least one of said plurality of partial multi-stage networks; and~~

~~said plurality of programmable logic blocks coupled with~~ said plurality of partial multi-stage networks arranged in a two-dimensional grid of a plurality of rows and a plurality of columns; and

each partial multi-stage network of said plurality of partial multi-stage networks further comprising one or more slices, each slice of said one or more slices further comprising one or more rings, each ring of said one or more rings further comprising y stages, where ~~$y \geq 1$~~ $y \geq 2$; and

each stage of said y stages comprising at least one switch of size $d_i \times d_0$, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of said at least one switch of size $d_i \times d_0$ having d_i incoming links and d_0 outgoing links; and each switch of said at least one switch of size $d_i \times d_0$ further comprising a plurality of multiplexers of size $d \geq 2$ with each multiplexer of said plurality of multiplexers comprising d inputs and one output; and

said at least one switch of size $d_i \times d_0$ comprises either only a forward switch, or only a backward switch, or both a forward switch and a backward switch, or a forward switch, a backward switch and U-turn switch, or a forward switch, a backward switch and a U-turn switch without 180 degree turn paths or a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch or a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180 degree turn paths, or an integrated switch of a forward switch, a backward switch and U-turn switch, or an integrated switch of a forward switch, a backward switch and a U-turn switch without 180 degree turn paths or an integrated switch of a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch or an integrated switch of a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180 degree turn paths; and

said d_i incoming links and said d_0 outgoing links comprises a plurality of internal connections and a plurality of hop wires; and said plurality of hop wires further comprising a plurality of internal hop wires or a plurality of external hop wires; and

each ~~inlet~~ outlet link of said plurality of ~~inlet~~ outlet links is connected to the output of one of said plurality of multiplexers of one switch of said at least one switch of size $d_i \times d_0$ of one stage of said y stages of one partial multi-stage network of said plurality of partial multi-stage networks, and each ~~outlet~~ inlet link of said plurality of ~~outlet~~ inlet links is connected to one of the inputs of one or more of said plurality of multiplexers of one or more said switches of said at least one switch of size $d_i \times d_0$ of one or more said stages of said y stages of one or more said plurality of partial multi-stage networks; and

a first ~~programmable logic block of said plurality of programmable logic blocks~~ partial multi-stage network of said plurality of partial multi-stage networks comprising the same or different number of said plurality of inlet links as a second ~~programmable logic block of said plurality of programmable logic blocks~~ partial multi-stage network of said plurality of partial multi-stage networks and a first ~~programmable logic block of said plurality of programmable logic blocks~~ partial multi-stage network of said plurality of partial multi-stage networks comprising the same or different number of said plurality of outlet links as a second ~~programmable logic block of said plurality of programmable logic~~

~~blocks~~ partial multi-stage network of said plurality of partial multi-stage networks; a first partial multi-stage network of said plurality of partial multi-stage networks comprising the same or different number of said one or more slices as a second partial multi-stage network of said plurality of partial multi-stage networks; a first slice of said one or more slices comprising the same or different number of said one or more rings as a second slice of said one or more slices; a first ring of said one or more rings comprising the same or different number of said y stages as a second ring of said one or more rings; and a first stage of said y stages comprising the same or different number of said at least one switch of size $d_i \times d_0$ as a second stage of said y stages; a first switch of said at least one switch of size $d_i \times d_0$ is the same or different size as a second switch of said at least one switch of size $d_i \times d_0$; a first multiplexer in said plurality of multiplexers of size $d \geq 2$ is the same or different size as a second multiplexer in said plurality of multiplexers of size $d \geq 2$; and

each internal connection of said plurality of internal connections connected from the output of a first multiplexer of said plurality of multiplexers of a first switch of said at least one switch of size $d_i \times d_0$ of a first stage of said y stages of a first ring of said one or more rings to a first input of said d inputs of a second multiplexer of said plurality of multiplexers of a second switch of said at least one switch of size $d_i \times d_0$ of a second stage of said y stages of the first ring of said one or more rings; and

each internal hop wire of said plurality of internal hop wires is connected from the output of a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a first ring of said one or more rings of a slice of said one or more slices to a first input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_0$ of one or more stages of said y stages of one or more rings different from the first ring of said one or more rings of the same slice of said one or more slices; and

each external hop wire of said plurality of external hop wires is connected from the output a multiplexer of said plurality of multiplexers of a switch of said at least one switch of

size $d_i \times d_0$ of a stage of said y stages of a ring of said one or more rings of a slice of said one or more slices of a first partial multi-stage network of said plurality of partial multi-stage networks to an input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_0$ of one or more stages of said y stages of said one or more rings of a slice of said one or more slices of one or more partial multi-stage networks different from the first partial multi-stage network of said plurality of partial multi-stage networks; and

one or more external hop wires of said plurality of external hop wires are either connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size $d_i \times d_0$ in same numbered stages of said y stages in three or more partial multi-stage networks of said plurality of partial multi-stage networks or connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size $d_i \times d_0$ in different numbered stages of said y stages, ~~when $y \geq 2$,~~ in three or more partial multi-stage networks of said plurality of partial multi-stage networks.

2. (Currently Amended): The ~~programmable integrated circuit~~ multi-stage hierarchical network of claim 1, wherein said plurality of external hop wires are connected vertically (hereinafter "vertical ~~links~~ wires"), or horizontally (hereinafter "horizontal ~~links~~ wires"~~), or by both vertical links and horizontal links~~; and

each partial multi-stage network of said plurality of partial multi-stage networks comprising said one or more slices is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or

each partial multi-stage network of said plurality of partial multi-stage networks comprising said horizontal ~~links~~ wires and said vertical ~~links~~ wires is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or

each partial multi-stage network of said plurality of partial multi-stage networks comprising both said one or more slices, and said horizontal ~~links~~ wires and said vertical

~~links~~ wires is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid.

3. (Currently Amended): The ~~programmable integrated circuit~~ multi-stage hierarchical network of claim 1, wherein said plurality of external hop wires are cascaded through only one multiplexer of said plurality of multiplexers at each switch of said at least one switch of size $d_i \times d_0$.

4. (Currently Amended): The ~~programmable integrated circuit~~ multi-stage hierarchical network of claim 1, wherein said one or more external hop wires of said plurality of external hop wires are connected between at least one same numbered stage in all said plurality of partial multi-stage networks, or one or more external hop wires of said plurality of external hop wires are connected between at least two not same numbered stages of said y stages in all said plurality of partial multi-stage networks; or

said plurality of external hop wires are all connected between same numbered stages of said y stages in all stages of said y stages of all said plurality of partial multi-stage networks.

5. (Currently Amended): The ~~programmable integrated circuit~~ multi-stage hierarchical network of claim 1, wherein ~~one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks are not connected to any other stages of said y stages in another partial multi-stage network of said plurality of partial multi-stage networks, or,~~

~~one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks are connected to stages of said y stages in another partial multi-stage network of said plurality of partial multi-stage networks by one or more external hop wires of said plurality of external hop wires, only when said two-dimensional grid is replicated by increasing said plurality of rows or said plurality of columns.~~

each multiplexer of said plurality of multiplexers of size $d \geq 2$ is of size d = 4 or d >= 4.

6. (Currently Amended): The ~~programmable integrated circuit~~ multi-stage hierarchical network of claim 1, wherein one or more of external hop wires of said plurality of external hop wires are implemented in two or more metal layers, or

each multiplexer of said plurality of multiplexers of size $d \geq 2$ is configurable by SRAM cells or Flash Cells, or

said plurality of external hop wires use a plurality of buffers to amplify signals driven through them; and said plurality of buffers are either inverting or non-inverting buffers, or

one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks comprising a switch of size $(d_i + m) \times (d_o + n)$, where $d_i \geq 2$, $d_o \geq 2$, $m \geq 0$, $n \geq 0$ or

one or more of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks comprising six 2:1 multiplexers, or eight 2:1 multiplexers, or four 3:1 multiplexers, or four 4:1 multiplexers.

7. (Currently Amended): The ~~programmable integrated circuit~~ multi-stage hierarchical network of claim 1, wherein said at least one switch of size $d_i \times d_0$ of said y stages are either fully populated or partially populated, or

said plurality of partial multi-stage networks are implemented in a 3D integrated circuit device.

8. (Currently Amended): A programmable integrated circuit comprising a plurality of programmable logic blocks and a multi-stage hierarchical network,

each programmable logic block of said plurality of programmable logic blocks comprising a plurality of inlet links and a plurality of outlet links; and

said multi-stage hierarchical network comprising a plurality of partial multi-stage networks wherein each programmable logic block of said plurality of programmable logic blocks is coupled with at least one partial multi-stage network of said plurality of partial multi-stage networks; and

said plurality of programmable logic blocks coupled with said plurality of partial multi-stage networks arranged in a two-dimensional grid of a plurality of rows and a plurality of columns; and

each partial multi-stage network of said plurality of partial multi-stage networks further comprising one or more slices, each slice of said one or more slices further comprising one or more rings, each ring of said one or more rings further comprising y stages, where ~~$y \geq 1$~~ $y \geq 2$; and

each stage of said y stages comprising at least one switch of size $d_i \times d_0$, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of said at least one switch of size $d_i \times d_0$ having d_i incoming links and d_0 outgoing links; and each switch of said at least one switch of size $d_i \times d_0$ further comprising a plurality of multiplexers of size $d \geq 2$ with each multiplexer of said plurality of multiplexers comprising d inputs and one output; and

said at least one switch of size $d_i \times d_0$ comprises either only a forward switch, or only a backward switch, or both a forward switch and a backward switch, or a forward switch, a backward switch and U-turn switch, or a forward switch, a backward switch and a U-turn switch without 180 degree turn paths, or an integrated switch of a forward switch, a backward switch and U-turn switch, or an integrated switch of a forward switch, a backward switch and a U-turn switch without 180 degree turn paths~~;~~, or an integrated switch of a forward switch, a backward switch and U-turn switch, or an integrated switch of a forward switch, a backward switch and a U-turn switch without 180 degree turn paths or an integrated switch of a forward switch, a backward switch, a U-turn switch and

a reverse U-turn switch or an integrated switch of a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180 degree turn paths; and

said d_i incoming links and said d_0 outgoing links comprises a plurality of internal connections and a plurality of hop wires; and said plurality of hop wires further comprising a plurality of internal hop wires or a plurality of external hop wires; and

each inlet link of said plurality of inlet links is connected to the output of one of said plurality of multiplexers of one switch of said at least one switch of size $d_i \times d_0$ of one stage of said y stages of one partial multi-stage network of said plurality of partial multi-stage networks, and each outlet link of said plurality of outlet links is connected to one of the inputs of one or more of said plurality of multiplexers of one or more said switches of said at least one switch of size $d_i \times d_0$ of one or more said stages of said y stages of one or more said plurality of partial multi-stage networks; and

a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of inlet links as a second programmable logic block of said plurality of programmable logic blocks and a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of outlet links as a second programmable logic block of said plurality of programmable logic blocks; a first partial multi-stage network of said plurality of partial multi-stage networks comprising the same or different number of said one or more slices as a second partial multi-stage network of said plurality of partial multi-stage networks; a first slice of said one or more slices comprising the same or different number of said one or more rings as a second slice of said one or more slices; a first ring of said one or more rings comprising the same or different number of said y stages as a second ring of said one or more rings; and a first stage of said y stages comprising the same or different number of said at least one switch of size $d_i \times d_0$ as a second stage of said y stages; a first switch of said at least one switch of size $d_i \times d_0$ is the same or different size as a second switch of said at least one switch of size $d_i \times d_0$; a

first multiplexer in said plurality of multiplexers of size $d \geq 2$ is the same or different size as a second multiplexer in said plurality of multiplexers of size $d \geq 2$; and

each internal connection of said plurality of internal connections connected from the output of a first multiplexer of said plurality of multiplexers of a first switch of said at least one switch of size $d_i \times d_0$ of a first stage of said y stages of a first ring of said one or more rings to a first input of said d inputs of a second multiplexer of said plurality of multiplexers of a second switch of said at least one switch of size $d_i \times d_0$ of a second stage of said y stages of the first ring of said one or more rings; and

each internal hop wire of said plurality of internal hop wires is connected from the output of a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a first ring of said one or more rings of a slice of said one or more slices to a first input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_0$ of one or more stages of said y stages of one or more rings different from the first ring of said one or more rings of the same slice of said one or more slices; and

each external hop wire of said plurality of external hop wires is connected from the output a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a ring of said one or more rings of a slice of said one or more slices of a first partial multi-stage network of said plurality of partial multi-stage networks to an input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_0$ of one or more stages of said y stages of said one or more rings of a slice of said one or more slices of one or more partial multi-stage networks different from the first partial multi-stage network of said plurality of partial multi-stage networks; and

one or more external hop wires of said plurality of external hop wires are either connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size $d_i \times d_0$ in same numbered stages of said y stages in three or more partial

multi-stage networks of said plurality of partial multi-stage networks or connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size $d_i \times d_0$ in different numbered stages of said y stages, ~~when $y \geq 2$,~~ in three or more partial multi-stage networks of said plurality of partial multi-stage networks.

9. (Currently Amended): The programmable integrated circuit of claim 8 wherein said plurality of external hop wires are connected vertically (hereinafter "vertical ~~links~~ wires"), or horizontally (hereinafter "horizontal ~~links~~ wires"~~), or by both vertical links and horizontal links~~; and

each partial multi-stage network of said plurality of partial multi-stage networks comprising said one or more slices is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or

each partial multi-stage network of said plurality of partial multi-stage networks comprising said horizontal ~~links~~ wires and said vertical ~~links~~ wires is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or

each partial multi-stage network of said plurality of partial multi-stage networks comprising both said one or more slices, and said horizontal ~~links~~ wires and said vertical ~~links~~ wires is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid.

10. (Original): The programmable integrated circuit of claim 8, wherein said plurality of external hop wires are cascaded through only one multiplexer of said plurality of multiplexers at each switch of said at least one switch of size $d_i \times d_0$.

11. (Original): The programmable integrated circuit of claim 8, wherein said one or more external hop wires of said plurality of external hop wires are connected between at least one same numbered stage in all said plurality of partial multi-stage networks, or

one or more external hop wires of said plurality of external hop wires are connected between at least two not same numbered stages of said y stages in all said plurality of partial multi-stage networks; or

said plurality of external hop wires are all connected between same numbered stages of said y stages in all stages of said y stages of all said plurality of partial multi-stage networks.

12. (Currently Amended): The programmable integrated circuit of claim 8, wherein ~~one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks are not connected to any other stages of said y stages in another partial multi-stage network of said plurality of partial multi-stage networks, or,~~

~~one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks are connected to stages of said y stages in another partial multi-stage network of said plurality of partial multi-stage networks by one or more external hop wires of said plurality of external hop wires, only when said two-dimensional grid is replicated by increasing said plurality of rows or said plurality of columns.~~

each multiplexer of said plurality of multiplexers of size $d \geq 2$ is of size d = 4 or d >= 4.

13. (Original): The programmable integrated circuit of claim 8, wherein one or more of external hop wires of said plurality of external hop wires are implemented in two or more metal layers, or

each multiplexer of said plurality of multiplexers of size $d \geq 2$ is configurable by SRAM cells or Flash Cells, or

said plurality of external hop wires use a plurality of buffers to amplify signals driven through them; and said plurality of buffers are either inverting or non-inverting buffers, or

one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks comprising a switch of size $(d_i + m) \times (d_o + n)$, where $d_i \geq 2$, $d_o \geq 2$, $m \geq 0$, $n \geq 0$ or

one or more of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks comprising six 2:1 multiplexers, or eight 2:1 multiplexers, or four 3:1 multiplexers, or four 4:1 multiplexers.

14. (Original): The programmable integrated circuit of claim 8, wherein said at least one switch of size $d_i \times d_0$ of said y stages are either fully populated or partially populated, or

said plurality of partial multi-stage networks are implemented in a 3D integrated circuit device.

15. (Currently Amended): A programmable integrated circuit comprising a plurality of programmable logic blocks and a multi-stage hierarchical network,

each programmable logic block of said plurality of programmable logic blocks comprising a plurality of inlet links and a plurality of outlet links; and

said multi-stage hierarchical network comprising a plurality of partial multi-stage networks wherein each programmable logic block of said plurality of programmable logic blocks is coupled with at least one partial multi-stage network of said plurality of partial multi-stage networks; and

said plurality of programmable logic blocks coupled with said plurality of partial multi-stage networks arranged in a two-dimensional grid of a plurality of rows and a plurality of columns; and

each partial multi-stage network of said plurality of partial multi-stage networks further comprising one or more slices, each slice of said one or more slices further comprising one or more rings, each ring of said one or more rings further comprising y stages, where ~~$y \geq 1$~~ $y \geq 2$; and

each stage of said y stages comprising at least one switch of size $d_i \times d_0$, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of said at least one switch of size $d_i \times d_0$ having d_i incoming links and d_0 outgoing links; and each switch of said at least one switch of size $d_i \times d_0$ further comprising a plurality of multiplexers of size $d \geq 2$ with each multiplexer of said plurality of multiplexers comprising d inputs and one output; and

~~said at least one switch of size $d_i \times d_0$ comprises either only a forward switch, or only a backward switch, or both a forward switch and a backward switch, or a forward switch, a backward switch and U-turn switch, or a forward switch, a backward switch and a U-turn switch without 180 degree turn paths, or an integrated switch of a forward switch, a backward switch and U-turn switch, or an integrated switch of a forward switch, a backward switch and a U-turn switch without 180 degree turn paths; and~~

said d_i incoming links and said d_0 outgoing links comprises a plurality of internal connections and a plurality of hop wires; and said plurality of hop wires further comprising a plurality of internal hop wires or a plurality of external hop wires; and

each inlet link of ~~S~~said plurality of inlet links is connected to the output of one of said plurality of multiplexers of one switch of said at least one switch of size $d_i \times d_0$ of one stage of said y stages of one partial multi-stage network of said plurality of partial multi-stage networks, and each outlet link of said plurality of outlet links is connected to one of the inputs of one or more of said plurality of multiplexers of one or more said switches of said at least one switch of size $d_i \times d_0$ of one or more said stages of said y stages of one or more said plurality of partial multi-stage networks; and

a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of inlet links as a second programmable logic block of said plurality of programmable logic blocks and a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of outlet links as a second programmable logic block of said plurality of programmable logic blocks; a first partial multi-stage network of said plurality of partial multi-stage networks comprising the same or different number of said one or more slices as a second partial multi-stage network of said plurality of partial multi-stage networks; a first slice of said one or more slices comprising the same or different number of said one or more rings as a second slice of said one or more slices; a first ring of said one or more rings comprising the same or different number of said y stages as a second ring of said one or more rings; and a first stage of said y stages comprising the same or different number of said at least one switch of size $d_i \times d_0$ as a second stage of said y stages; a first switch of said at least one switch of size $d_i \times d_0$ is the same or different size as a second switch of said at least one switch of size $d_i \times d_0$; a first multiplexer in said plurality of multiplexers of size $d \geq 2$ is the same or different size as a second multiplexer in said plurality of multiplexers of size $d \geq 2$; and

each internal connection of said plurality of internal connections connected from the output of a first multiplexer of said plurality of multiplexers of a first switch of said at least one switch of size $d_i \times d_0$ of a first stage of said y stages of a first ring of said one or more rings to a first input of said d inputs of a second multiplexer of said plurality of multiplexers of a second switch of said at least one switch of size $d_i \times d_0$ of a second stage of said y stages of the first ring of said one or more rings ; and

each internal hop wire of said plurality of internal hop wires is connected from the output of a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a first ring of said one or more rings of a slice of said one or more slices to a first input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size

$d_i \times d_0$ of one or more stages of said y stages of one or more rings different from the first ring of said one or more rings of the same slice of said one or more slices ; and

each external hop wire of said plurality of external hop wires is connected from the output a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a ring of said one or more rings of a slice of said one or more slices of a first partial multi-stage network of said plurality of partial multi-stage networks to an input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_0$ of one or more stages of said y stages of said one or more rings of a slice of said one or more slices of one or more partial multi-stage networks different from the first partial multi-stage network of said plurality of partial multi-stage networks; and

one or more external hop wires of said plurality of external hop wires are either connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size $d_i \times d_0$ in same numbered stages of said y stages in three or more partial multi-stage networks of said plurality of partial multi-stage networks or connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size $d_i \times d_0$ in different numbered stages of said y stages, ~~when $y \geq 2$,~~ in three or more partial multi-stage networks of said plurality of partial multi-stage networks.

16. (Currently Amended): The programmable integrated circuit of claim 15, The programmable integrated circuit of claim 8 wherein said plurality of external hop wires are connected vertically (hereinafter "vertical ~~links~~ wires"), or horizontally (hereinafter "horizontal ~~links~~ wires"~~), or by both vertical links and horizontal links~~; and

each partial multi-stage network of said plurality of partial multi-stage networks comprising said one or more slices is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or

each partial multi-stage network of said plurality of partial multi-stage networks comprising said horizontal ~~links~~ wires and said vertical ~~links~~ wires is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or

each partial multi-stage network of said plurality of partial multi-stage networks comprising both said one or more slices, and said horizontal ~~links~~ wires and said vertical ~~links~~ wires is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid.

17. (Original): The programmable integrated circuit of claim 15, wherein said plurality of external hop wires are cascaded through only one multiplexer of said plurality of multiplexers at each switch of said at least one switch of size $d_i \times d_0$.

18. (Original): The programmable integrated circuit of claim 15, wherein said one or more external hop wires of said plurality of external hop wires are connected between at least one same numbered stage in all said plurality of partial multi-stage networks, or

one or more external hop wires of said plurality of external hop wires are connected between at least two not same numbered stages of said y stages in all said plurality of partial multi-stage networks; or

said plurality of external hop wires are all connected between same numbered stages of said y stages in all stages of said y stages of all said plurality of partial multi-stage networks.

19. (Currently Amended): The programmable integrated circuit of claim 15, wherein ~~one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks are not connected to any other stages of said y stages in another partial multi-stage network of said plurality of partial multi-stage networks, or,~~

~~one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks are connected to stages of said y stages in another partial multi-stage network of said plurality of partial multi-stage networks by one or more external hop wires of said plurality of external hop wires, only when said two-dimensional grid is replicated by increasing said plurality of rows or said plurality of columns.~~

each multiplexer of said plurality of multiplexers of size $d \geq 2$ is of size d = 4 or d >= 4.

20. (Original): The programmable integrated circuit of claim 15, wherein one or more of external hop wires of said plurality of external hop wires are implemented in two or more metal layers, or

each multiplexer of said plurality of multiplexers of size $d \geq 2$ is configurable by SRAM cells or Flash Cells, or

said plurality of external hop wires use a plurality of buffers to amplify signals driven through them; and said plurality of buffers are either inverting or non-inverting buffers, or

one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks comprising a switch of size $(d_i + m) \times (d_o + n)$, where $d_i \geq 2$, $d_o \geq 2$, $m \geq 0$, $n \geq 0$ or

one or more of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks comprising six 2:1 multiplexers, or eight 2:1 multiplexers, or four 3:1 multiplexers, or four 4:1 multiplexers, or

said at least one switch of size $d_i \times d_0$ of said y stages are either fully populated or partially populated, or

said plurality of partial multi-stage networks are implemented in a 3D integrated circuit device

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REMARKS

Applicant respectfully submits that entry of the foregoing Amendment pursuant to 37 CFR § 1.121 does not raise any new issues.

FIG. 2A is amended to illustrate two exemplary 180-degree U-turn paths.

FIG. 2C, FIG. 2E, and FIG. 3B are amended to correct the labels of the F, B, R and U Muxes to be consistent with the other drawings.

Pursuant to 37 C.F.R. § 1.83(a), FIG. 3B is amended to illustrate the pyramid links provided between the switches in the same stage. Also, the written description has been amended to conform to amended FIG. 3B and to refer to the disclosure in related patent incorporated by reference in the present application.

In the specification and the abstract of the disclosure, minor typographical errors were fixed and the written description has been amended to correct minor editorial problems. The specification for the drawings of FIG. 2C, FIG. 2E, and FIG. 3B is also amended to correctly describe the amended drawings of FIG. 2C, FIG. 2E, and FIG. 3B.

Also, the written description has been amended to clarify forward switch, backward switch and U-turn switch, reverse U-turn switch, integrated circuit device or IC device, straight link or straight middle link, cross links or cross middle links, stages without 180-degree turn paths, and stages with integrated switches without 180-degree turn paths.

The amended claims will not require substantial additional work on the part of the Office.

Consequently, pursuant to 37 CFR § 1.121, it is requested that the foregoing Amendment be entered.

CONCLUSION

For all of the above reasons, applicant submits that the Claims are now in proper form, and that the Claims all define patentably over the prior art. Therefore applicant submits that this application is now in condition for allowance, which action he respectfully solicits.

Conditional request for Constructive Assistance

Applicant has amended the claims of this application so that they are proper, definite, and define novel structure which is also unobvious. If, for any reason this application is not believed to be in full condition for allowance, applicant respectfully request the constructive assistance and suggestions of the Examiner pursuant to M.P.E.P § 2173.02 and § 707.07(j) in order that the undersigned can place this application in allowable condition as soon as possible and without the need for further proceedings.

Respectfully Submitted,

/Venkat Konda/

Venkat Konda

Konda Technologies, Inc (USPTO Customer Number: 38139)

6278 Grand Oak Way

San Jose, CA 95135

Phone: 408-472-3273

Markup sheet

FIG. 2A

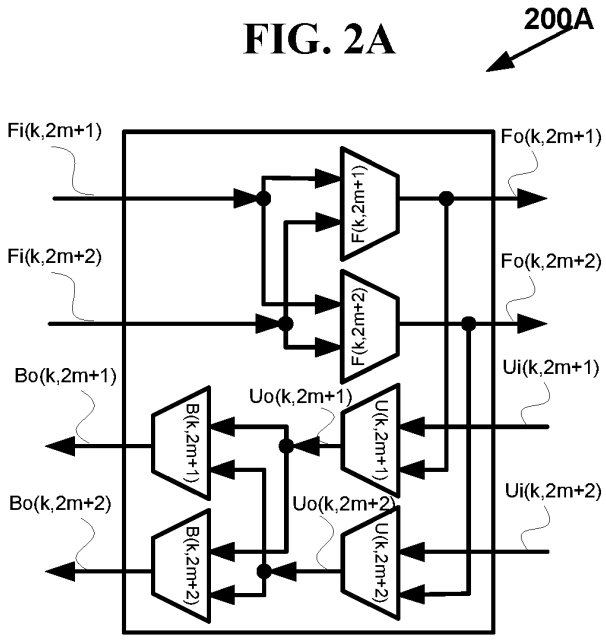


FIG. 2B

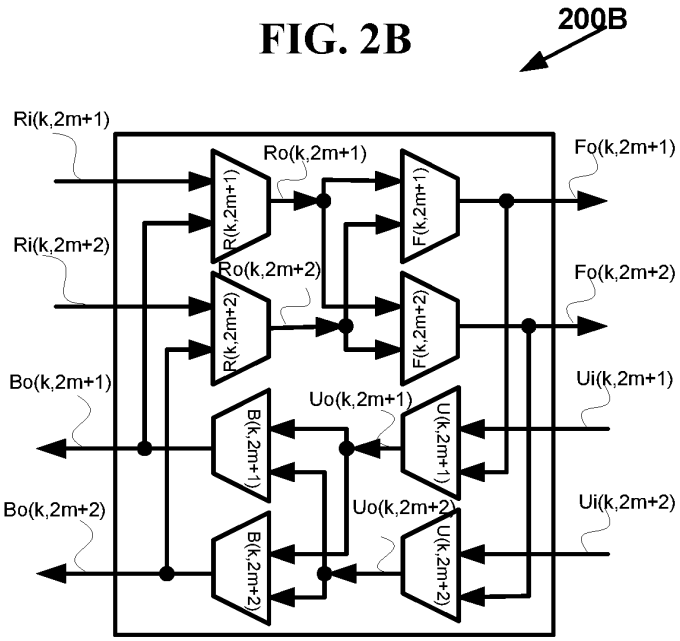


FIG. 2C

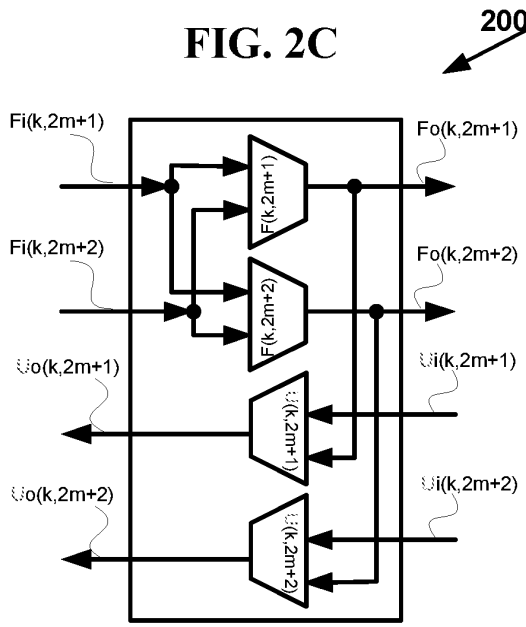
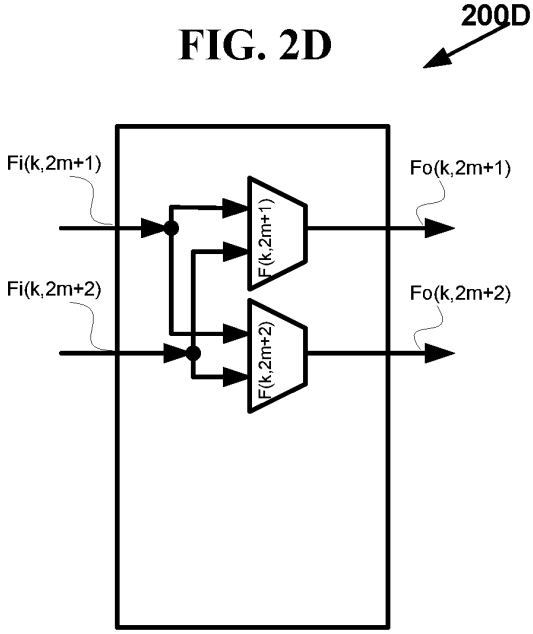


FIG. 2D



Markup sheet

FIG. 2E

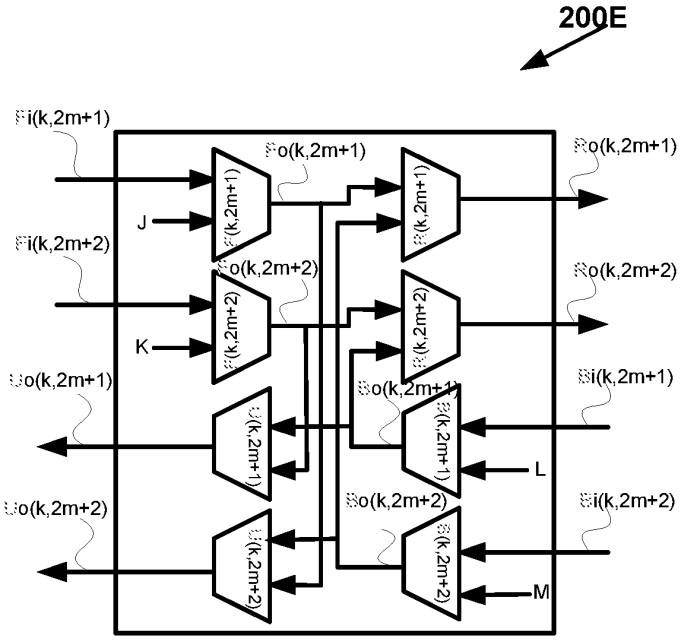
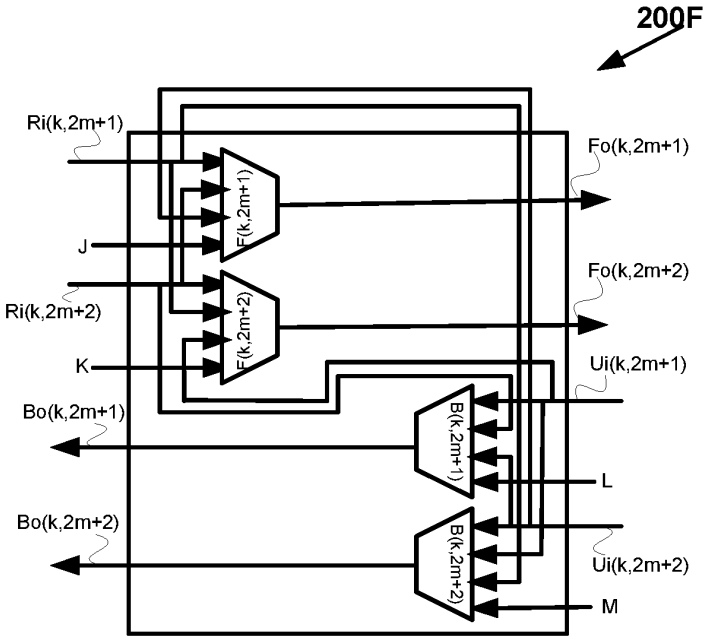
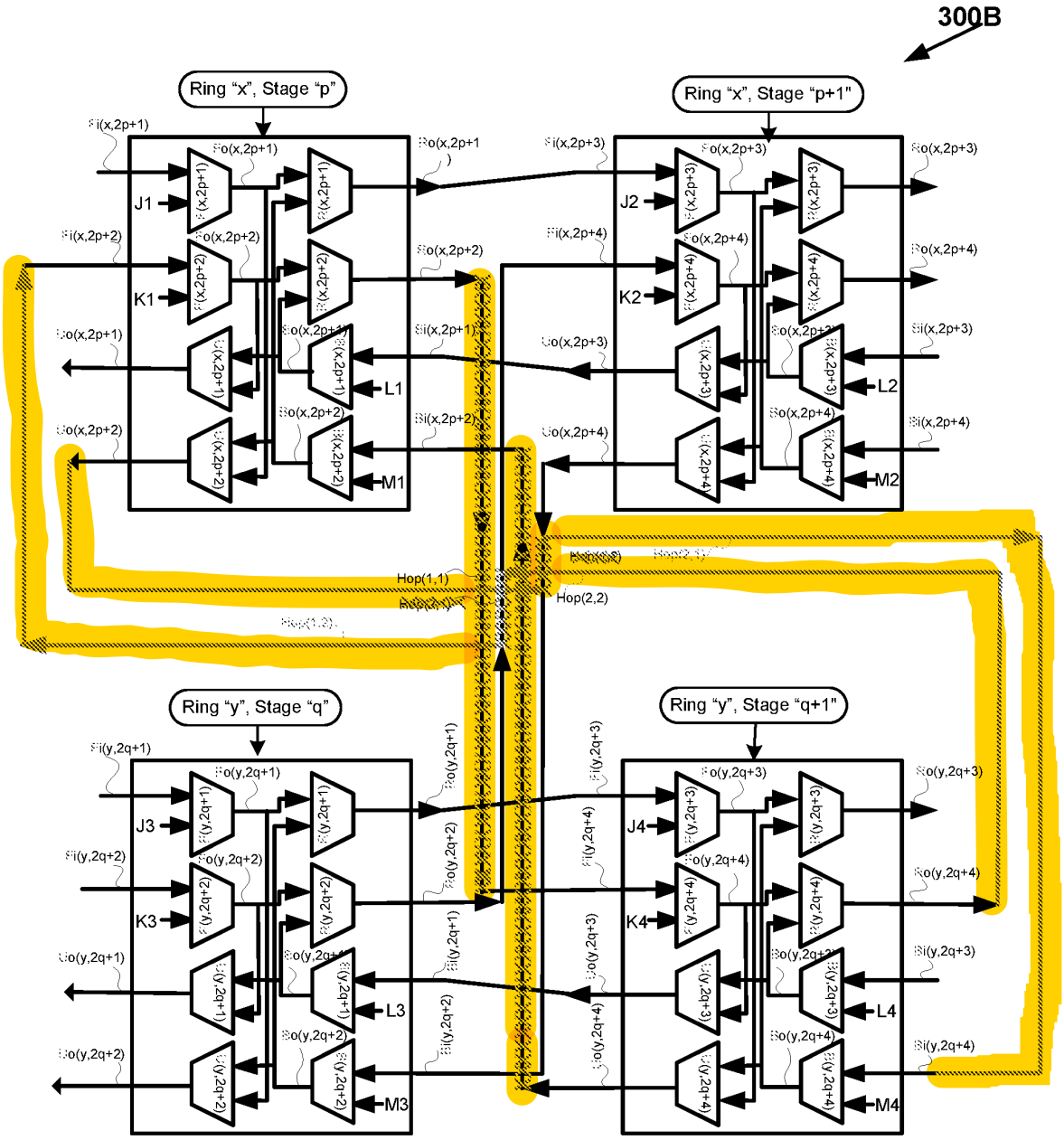


FIG. 2F



Markup sheet

FIG. 3B



Replacement sheet

FIG. 2A

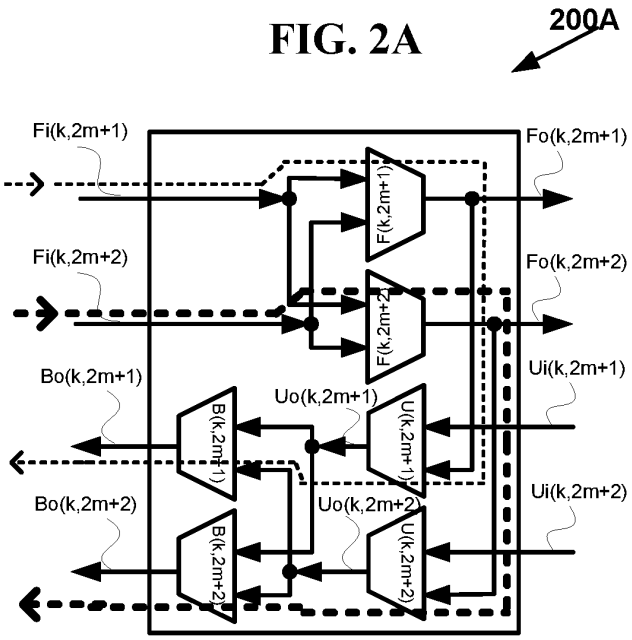


FIG. 2B

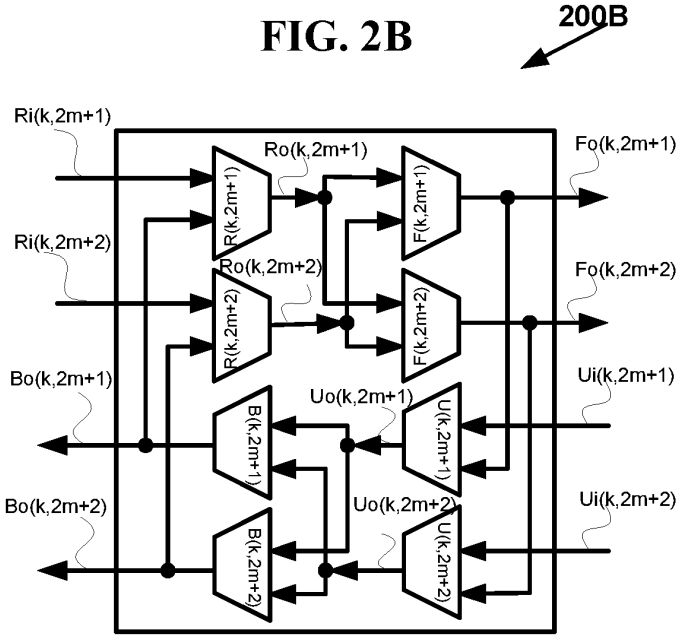


FIG. 2C

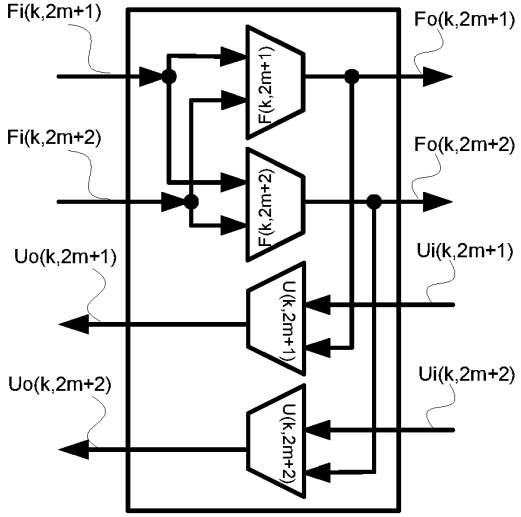
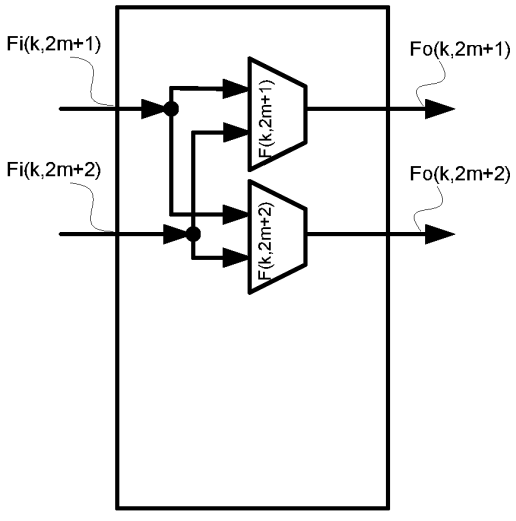


FIG. 2D



Replacement sheet

FIG. 2E

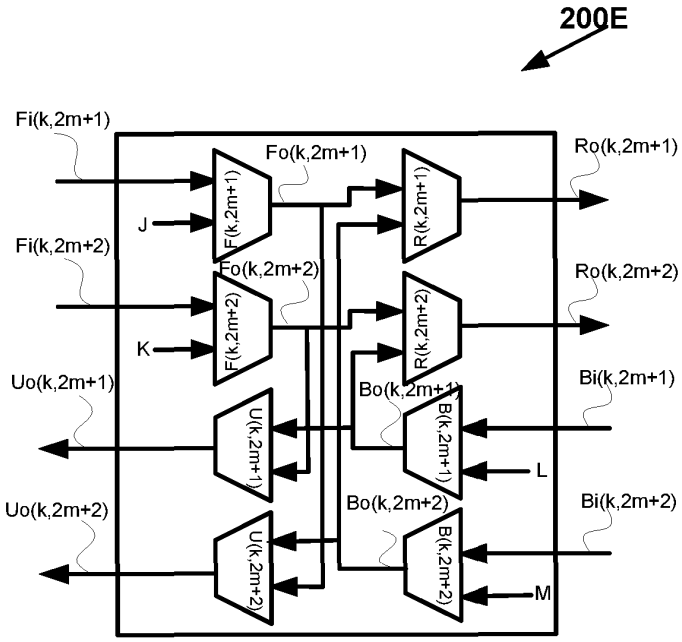
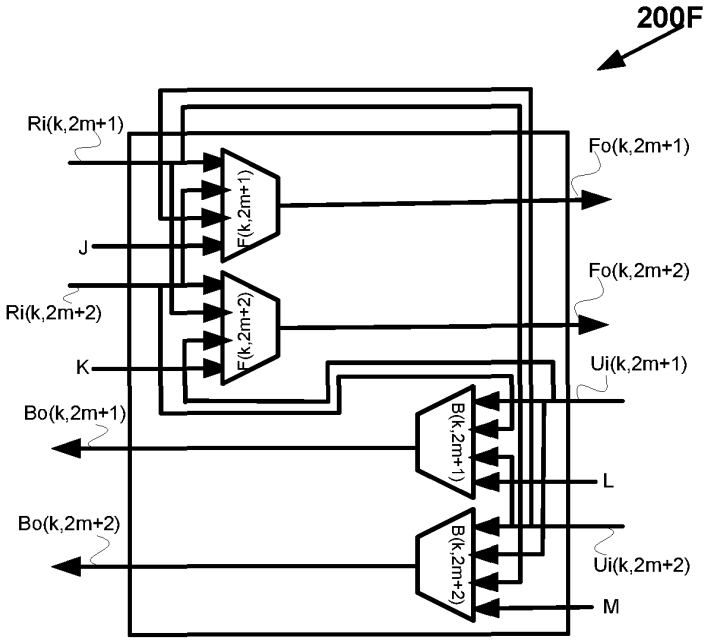
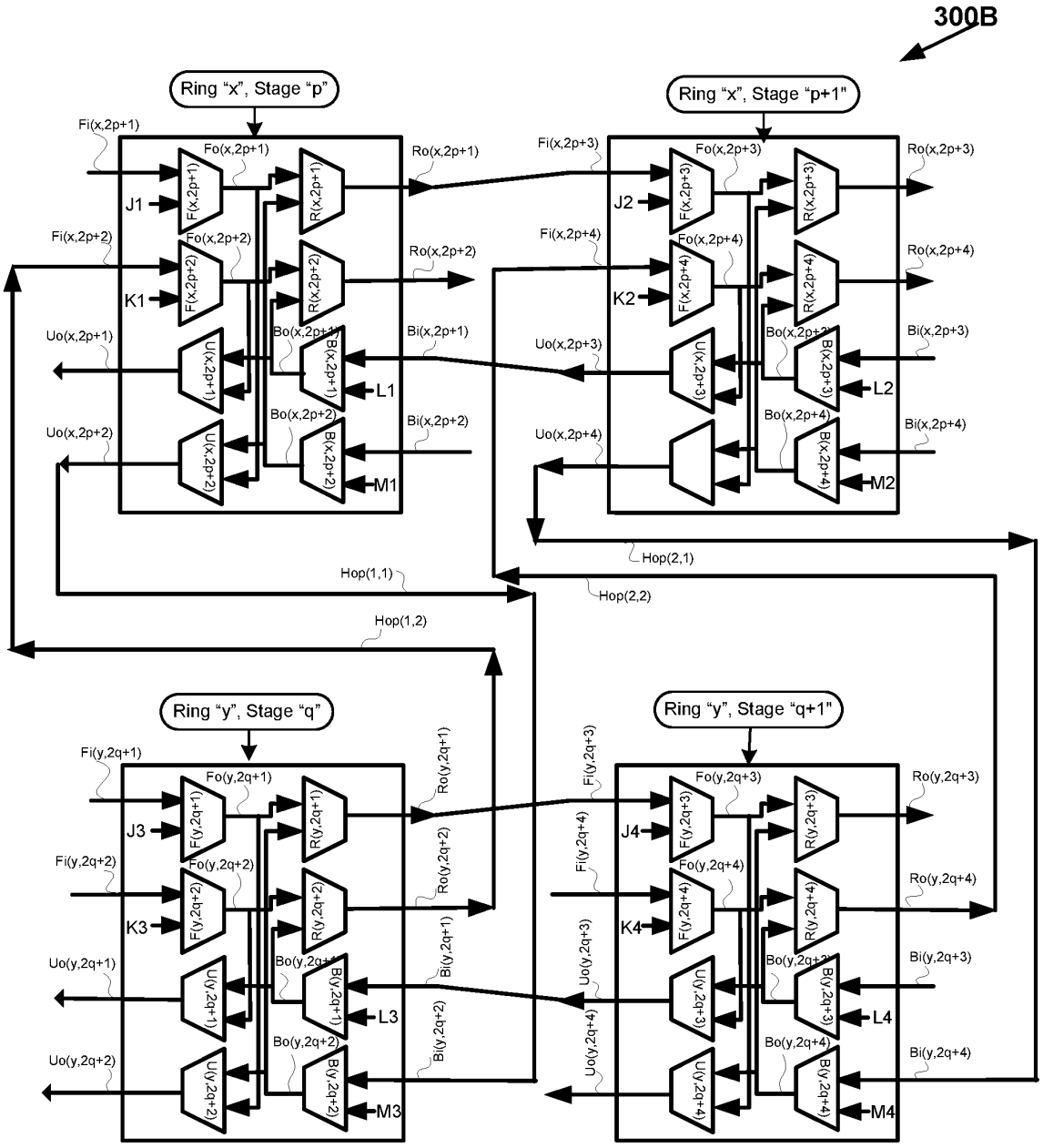


FIG. 2F



Replacement sheet

FIG. 3B



PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/562,450	Filing Date 09/06/2019	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	11/09/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/ZETA T ADAMS/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/562,450	09/06/2019	Venkat Konda	V-0060US	6438

38139 7590 08/07/2020

Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

EXAMINER	
GIDADO, RASHEED	

ART UNIT	PAPER NUMBER
2464	

NOTIFICATION DATE	DELIVERY MODE
08/07/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

venkat@kondatech.com
vkonda@gmail.com

Office Action Summary	Application No. 16/562,450	Applicant(s) Konda, Venkat	
	Examiner RASHEED GIDADO	Art Unit 2464	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 09/06/2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-20 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 09/06/2019 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

1. This communication is response to the application filed 09/06/2019. Claims 1-20 are pending and presented for examination.

Notice of Pre-AIA or AIA Status

2. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 09/06/2019 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Terminal Disclaimer

7. The terminal disclaimer filed on 09/06/2019 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of

the full statutory term of patent No. 10,412,025 is acknowledged. The terminal disclaimer has been recorded.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) -

706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

6. Claims 1-20 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 9,929,977 (hereafter Patent '977). Although the claims at issue are not identical, they are not patentably distinct from each other because both set of claims are claiming the same invention with minor difference since applicant merely broadens the claims of Patent '977 to arrive at the claims of the current application. Thus, both set of claims are obvious variant of each other.

7. Claims 1-20 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 8,898,611 (hereafter Patent '611). Although the claims at issue are not identical, they are not patentably distinct from each other because both set of claims are claiming the same invention with minor difference, thus they are obvious variant of each other. Applicant merely broadens the claims of

Patent '611 to arrive at claims of the current application. Thus, the claims of Patent '611 encompass the claims of the current application. It would have been obvious to one of ordinary skills in the art at the time of the invention to rearrange the claims of the Patent '611 to arrive at the claims of the current application based on user design preference to achieve desired design preference.

8. Claims 1-20 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 9,509,634 (hereafter '634). Although the claims at issue are not identical, they are not patentably distinct from each other because both set of claims are claiming the same invention with minor difference, thus they are obvious variant of each other. Applicant merely broadens the claims of Patent '634 to arrive at claims of the current application. Thus, the claims of Patent '634 encompass the claims of the current application. It would have been obvious to one of ordinary skills in the art at the time of the invention to rearrange the claims of the Patent '634 to arrive at the claims of the current application based on user design preference to achieve desired design preference.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ 2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is

anticipated by a patent claim to a species within that genus)". ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED; May 30, 2001).

Allowable Subject Matter

9. Claims 1-20 would be allowable if rewritten or amended to overcome the rejection(s) under the non-statutory double patenting rejection.

The cited references fails to explicitly disclose, fairly suggests, or render obvious on the following when considered with other limitations in the claim: said d, incoming links and said do outgoing links comprises a plurality of internal connections and a plurality of hop wires; and said plurality of hop wires further comprising a plurality of internal hop wires or a plurality of external hop wires; and each inlet link of said plurality of inlet links is connected to the output of one of said plurality of multiplexers of one switch of said at least one switch of size d, x do of one stage of said y stages of one partial multi-stage network of said plurality of partial multi- stage networks, and each outlet link of said plurality of outlet links is connected to one of the inputs of one or more of said plurality of multiplexers of one or more said switches of said at least one switch of size d, x do of one or more said stages of said y stages of one or more said plurality of partial multi-stage networks; and a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of inlet links as a second programmable logic block of said plurality of programmable logic blocks and a first programmable logic block of said plurality of programmable logic blocks comprising

the same or different number of said plurality of outlet links as a second programmable logic block of said plurality of programmable logic blocks; a first partial multi-stage network of said plurality of partial multi-stage networks comprising the same or different number of said one or more slices as a second partial multi-stage network of said plurality of partial multi-stage networks; a first slice of said one or more slices comprising the same or different number of said one or more rings as a second slice of said one or more slices; a first ring of said one or more rings comprising the same or different number of said y stages as a second ring of said one or more rings; and a first stage of said y stages comprising the same or different number of said at least one switch of size d, x do as a second stage of said y stages; a first switch of said at least one switch of size d, x do is the same or different size as a second switch of said at least one switch of size d, x do; a first multiplexer in said plurality of multiplexers of size d 2 is the same or different size as a second multiplexer in said plurality of multiplexers of size d > 2; and each internal connection of said plurality of internal connections connected from the output of a first multiplexer of said plurality of multiplexers of a first switch of said at least one switch of size d, x do of a first stage of said y stages of a first ring of said one or more rings to a first input of said d inputs of a second multiplexer of said plurality of multiplexers of a second switch of said at least one switch of size d, x do of a second stage of said y stages of the first ring of said one or more rings; and each internal hop wire of said plurality of internal hop wires is connected from the output of a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size d, x do of a stage of said y stages of a first ring of said one or more rings of a slice of said one or more slices to a first input of said d inputs of one or more multiplexers of

said plurality of multiplexers of one or more switches of said at least one switch of size d, x do of one or more stages of said y stages of one or more rings different from the first ring of said one or more rings of the same slice of said one or more slices; and each external hop wire of said plurality of external hop wires is connected from the output a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size d, x do of a stage of said y stages of a ring of said one or more rings of a slice of said one or more slices of a first partial multi-stage network of said plurality of partial multi-stage networks to an input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size d x d0 of one or more stages of said y stages of said one or more rings of a slice of said one or more slices of one or more partial multi-stage networks different from the first partial multi-stage network of said plurality of partial multi-stage networks; and one or more external hop wires of said plurality of external hop wires are either connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size d, x do in same numbered stages of said y stages in two or more partial multi-stage networks of said plurality of partial multi-stage networks or connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size d, x do in different numbered stages of said y stages, when y 2, in two or more partial multi-stage networks of said plurality of partial multi-stage networks.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US Patent 6,504,841 to Larson et al. discloses three-dimensional interconnection geometries for multi-stage switching networks using flexible ribbon cable connection between multiple planes.
- US Patent 7,167,481 to Steele et al. discloses technique for computing pathways in a multi-stage switch fabric through exploitation of symmetrical links.
- US Patent 6,215,786 Larson et al. discloses implementation of multi-stage switching networks.
- US Patent 7,397,796 to Smiljanic discloses load balancing algorithms in non-blocking multistage packet switches.
- US Patent 8,265,070 to Khanduri discloses system and method for implementing a multistage network using a two-dimensional array of tiles.
- US Patent 8,804,710 to Aybay et al. discloses system architecture for a scalable and distributed multi-stage switch fabric.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to RASHEED GIDADO whose telephone number is (571)270-7645. The examiner can normally be reached on Monday - Friday 8AM-5PM EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RASHEED GIDADO/
Primary Examiner, Art Unit 2464

Notice of References Cited	Application/Control No. 16/562,450	Applicant(s)/Patent Under Reexamination Konda, Venkat	
	Examiner RASHEED GIDADO	Art Unit 2464	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-8265070-B2	09-2012	Khanduri; Puneet	H04L49/1515	370/387
*	B	US-8804710-B2	08-2014	Aybay; Gunes	H04L49/1515	370/388
*	C	US-6504841-B1	01-2003	Larson; Brian Ralph	H04L49/1515	370/386
*	D	US-7167481-B2	01-2007	Steele; David C.	H04L49/1515	370/230
*	E	US-6215786-B1	04-2001	Larson; Brian Ralph	H04L49/1515	370/386
*	F	US-7397796-B1	07-2008	Smiljani ; Aleksandra	H04L49/1515	370/335
	G					
	H					
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FOREIGN PATENT DOCUMENTS

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	N					
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	P					
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	R					
	S					
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*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	X	

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/562,450	Konda, Venkat
	Examiner	**Art Unit**
	RASHEED GIDADO	2464

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☑ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/03/2020								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
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	7	✓								
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	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/562,450	Konda, Venkat
	Examiner	Art Unit
	RASHEED GIDADO	2464

CPC - Searched*		
Symbol	Date	Examiner
H04L49/1515,102	08/03/2020	RG

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

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Search Notes		
Search Notes	Date	Examiner
Inventor/Assignee Search in EAST	08/03/2020	RG
Inventor/Assignee Search in PALM	08/03/2020	RG
EAST (USPAT, USPGPUB, EPO, DERWENT, FPRS) Search	08/03/2020	RG
IEEE, IP.COM, Google Patent Search	08/03/2020	RG
H04L49/1515,102 with text search	08/03/2020	RG

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/RASHEED GIDADO/ Primary Examiner, Art Unit 2464	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	16/562,450 - GAU: 2464
Filing Date	09-06-2019
First Named Inventor	Venkat Konda
Art Unit	
Examiner Name	
Attorney Docket Number	V-0060US

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 8269523-b2	09-18-2012	Venkat Konda	all FIGs
	2	US- 8898611-b2	11-25-2014	Venkat Konda	all FIGs
	3	US- 9529958-b2	12-27-2016	Venkat Konda	all FIGs
	4	US- 8270400-b2	09-18-2012	Venkat Konda	all FIGs
	5	US- 8170040-b2	05-01-2012	Venkat Konda	all FIGs
	6	US- 8363649-b2	01-29-2013	Venkat Konda	all FIGs
	7	US- 6185220-b1	02-06-2001	Muthukrishnan et. al.	layout FIGs
	8	US- 6940308-b2	09-06-2005	Wong	layout FIGs
	9	US- 5451936	09-19-1995	Yang et. al.	layout FIGs
	10	US- 5153843	10-061992	Kenneth E. Batcher	layout FIGs
	11	US- 6018523	01-25-2000	Shimon Even	layout FIGs
	12	US-			
	13	US-			
	14	US-			
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		US-			

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Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/RASHEED GIDADO/	Date Considered	08/03/2020

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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Bibliographic Data

Application No: 16/562,450

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /RASHEED GIDADO/ Examiner's Signature | Initials

Title: FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/06/2019	370	2464	V-0060US
RULE			

APPLICANTS

INVENTORS

Venkat Konda, San Jose, CA, UNITED STATES

CONTINUING DATA

This application is a CON of 15884911 01/31/2018 PAT 10412025

15884911 is a CON of 15331855 10/22/2016 PAT 9929977

15331855 is a CON of 14329876 07/11/2014 PAT 9509634

14329876 is a CIP of 14199168 03/06/2014 PAT 9374322

14329876 has PRO of 61846083 07/15/2013

14199168 is a CON of PCT/US12/53814 09/06/2012

PCT/US12/53814 has PRO of 61531615 09/07/2011

FOREIGN APPLICATIONS

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Sheet 1 of 1

Complete if Known	
Application Number	16/562,450 - GAU: 2464
Filing Date	09-06-2019
First Named Inventor	Venkat Konda
Art Unit	
Examiner Name	
Attorney Docket Number	V-0060US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
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	2	F. Petrini et. al., "k-ary n-trees: High performance networks for massively parallel architectures, in: Proceedings of the 11th Intl Parallel Proc. Symp. , IPPS'97, pp. 87-93	
	3	P.Pande et al. "Evaluation of MP-SoC Interconnect Architectures: a Case Study", Proceedings of 4th IWSOC, Banff, Alberta, Canada, 19th-21st July, 2004	
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	5	M. Lin, A. El Gamal, "A Low-Power Field-Programmable Gate Array Routing Fabric," IEEE Transactions on Very Large Scale Integration, Vol. 17, No. 10, pp. 1481-1494, Oct. 2009	
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Examiner Signature	/RASHEED GIDADO/	Date Considered	08/03/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	16/562,450 - GAU: 2464
Filing Date	09-06-2019
First Named Inventor	Venkat Konda
Art Unit	
Examiner Name	
Attorney Docket Number	V-0060US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	C. Clos, "A Study of Non-Blocking Switching Networks," Bell System Technical Journal, 32:406-424, 1953.	
	2	A. DeHon, "Balancing Interconnect and Computation in a Reconfigurable Computing Array," ACM Int. Symp. on FPGA, pp. 69-78, Feb. 1999	
	3	Chihming Chang, Rami Melhem, "Arbitrary Size Benes Networks", Journal: Parallel Processing Letters - PPL , vol. 7, no. 3, pp. 279-284, 1997.	
	4	HODA EL-SAYED and ABDOU YOUSSEF; "The r-truncated Benes Networks and their Randomized Routing Algorithms"1997 Intl Conf on Parallel and Dist Sys, Seoul, Korea, December 1997.	
	5	Guy Lemieux and David Lewis, "Using Sparse Crossbars within LUT Clusters", Procds of the ACM/SIGDA Intl Symp on Field Prog Gate Arrays 2001, Feb. 11–13, 2001, Monterey, CA.	
	6	P. Manuel, W. K. Qureshi, A. William, A. Muthumalai, "VLSI layout of Benes networks,", J. of Discrete Math. Sci. & Cryptography, vol. 10, no, 4, pp. 461-472, 2007	
	7	Quinn, Michael J, "Parallel Computing: Theory and Practice", 2nd. ed., 1994, McGraw Hill Series in computer Science, Networks, and parallel computing, ISBN 0-07-051294-9	
	8	Ronald I. Greenberg, "The Fat-Pyramid and Universal Parallel Computation Independent of wire delay" IEEE Trans. Computers, 43(12):1358-1364, December 1994.	
	9	Hypertree: A Multiprocessor Interconnection Topology , by James R. Goodman and Carlo H Sequin, Computer Science Technical Report #427, Dept , of EECS, University of California	
	10	Data Movement Techniques for the pyramid computer, Russ Miller and Quentin F. Stout, SIAM Journal on Computing, Vol. 16, no. 1, pp. 38 - 60, Feb. 1987.	

Examiner Signature	/RASHEED GIDADO/	Date Considered	08/03/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

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PTO/SB/08b (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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	1	Guy Lemieux et.al., Generating highlyroutablesparse crossbars for PLDs. In ACMISIGDA Int'l. Symposium on Field Programmable Gate Arrays, pp155-164, Monterey, CA, February 2000	
	2	S. Sivaswamy et. al., "HARP: hard-wired routing pattern FPGAs", FPGA'05, Monterey, California, USA, February 20–22, 2005.	
	3	Yeh, C.-H., E.A. Varvarigos, and B. Parhami, "Efficient VLSI layouts of hypercubic networks," Proc. Symp. Frontiers of Massively Parallel Computation, Feb. 1999	
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Examiner Signature	/RASHEED GIDADO/	Date Considered	08/03/2020

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	1	A. DeHon, "Unifying Mesh- and Tree-Based Programmable Interconnect," IEEE Trans. on Very Large Scale Int. Systems, vol. 12, no. 10, pp. 1051-1065, Oct. 2004	
	2	Guy Lemieux and David Lewis. Analtyical framework for switch block design. In Intl. Conference on Field Programmable Logic and Applications, pages 122-131, September 2002.	
	3	Chen, G; Lau, FCM, "A tight layout of the cube-connected cycles", The 4th International Conference on High Perf. Computing, Bangalore, India, 18-21 December 1997, p. 422-427	
	4	Michael Shyu, Yu-Dong Chang, Guang-Ming Wu, and Yao-Wen Chang, "Generic universal switch blocks. IEEE Transactions on Computers,49(4):348-359, April 2000.	
	5	Y. Yamada, et. al. , ```Folded Fat H-Tree: an interconnection topology for Dynamically Reconfigurable Processor Array", Embed and Ubiq. Cmpting, Intl Conf. EUC 2004.	
	6	V. P. Roychdowdhury et. al., "Segmented Channel Routing," IEEE Trans on Computer-Aided Design of Integrated Circuits and Systems, Vol. 12, No. 1, pp. 79-95, January 1993.	
	7	André DeHon. Compact, Multilayer Layout for Butterfly Fat-Tree. In Twelfth Annual ACM Symposium on Parallel Algs and Architectures (SPAA 2000), pages 206--215, July 9-12, 2000	

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	3	"14199168"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 11:41
S2	932	H04L49/1515.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:01
S3	11,172	370/254.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:01
S4	86	Venkat near2 Konda.in.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:02
S5	7	"20110037498"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:05
S6	3	"20030117945"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:09
S7	2	"20030117946"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:10
S8	142	("6088353" "8830993" "8898611" "20120269190" "20140313930" "20150046895" "20150049768" "6237006" "6425007" "7392488" "7725499" "7945854" "7945854" "20020169801" "20050273730" "20080104002" "20100333038" "20130339918" "20140072777"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2015/09/30 12:26

		"5590250" "6018523" "6091723" "6829618" "6901575" "7086824" "7310786" "8661371" "8719737" "8850367" "9122838" "20020083410" "20060190847" "20070268731" "20130204584" "20140189611" "20140372958" "20150186340" "20150217889" "3561509" "3589243" "3589249" "4442150" "4599802" "4976553" "5284404" "5295280" "5448687" "5701416" "6060641" "6082056").pn.				
S9	1,433	370/386.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:27
S10	17	hierarchical near2 (rout$3 or network) same (two-dimension$3 or 2-D) same switch	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:29
S11	36	stage same block same (two-dimension$3 or 2-D) same switch	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:30
S12	28	S11 not S10	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:33
S13	3	"6091723".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:37
S14	3	"20120269190"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2015/09/30 12:56
S15	5	"14329876"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/17 20:15
S16	971	H04L49/1515,202.cpc.	US-PGPUB; USPAT;	ADJ	ON	2016/01/17 20:58

			FPRS; EPO; JPO; DERWENT			
S17	507	370/411.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/17 20:58
S18	17	hierarchical near2 (rout$3 or network) same (two-dimension$3 or 2-D) same switch	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/17 20:58
S19	1,602	(rout$3 or network) same (two-dimension$3 or 2-D) same switch	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/17 20:59
S20	19	S19 and S16	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/17 20:59
S21	10	S19 and S17	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/17 20:59
S22	248	stage same switch and (rout$3 or network) same (two-dimension$3 or 2-D) same switch	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/17 21:00
S23	75	link$3 same stage same switch and (rout$3 or network) same (two-dimension$3 or 2-D) same switch	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/17 21:00
S24	2	"8898611".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/18 11:15
S25	2	"6335930".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/01/18 11:35

S26	2	"8898611".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/07/07 12:37
S27	920	(network or sub$1network) with (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/07/07 13:21
S28	7	(network or sub$1network) with (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same (inlet or input) near2 link	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/07/07 13:22
S29	81	switch same (network or sub$1network) with (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/07/07 13:23
S30	49	switch same (network or sub$1network) with (partition$3 or divid$3 or split$4) with (block or slic$3) same link	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/07/07 13:24
S31	2	multiplexer same switch same (network or sub$1network) with (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/07/07 13:24
S32	8	"20030012222"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/07/07 13:49
S33	2	"20090181703"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/07/07 13:53
S40	9	"9509634".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/02/15 14:08
S41	0	"15331855"	US-PGPUB; USPAT; FPRS; EPO;	ADJ	ON	2017/02/15 14:11

			JPO; DERWENT			
S42	3	"14384853"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/02/16 10:38
S43	5	"14199168"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/02/16 11:57
S44	2,096	H04L49/1515,102.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/02/16 18:38
S45	26	multiplexer same switch same (network or sub$1network) same (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/07/19 21:35
S46	167	(channel or path or link$3) same stage same switch and (rout$3 or network) same (two-dimension$3 or 2-D) same switch	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/07/19 21:36
S47	7	"14329876"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/11/12 18:45
S52	1	"15884911"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/12/20 13:41
S53	6	"9929977".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/12/20 13:42
S54	2,408	H04L49/1515,102.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/12/20 13:58

S55	98	venkat near2 Konda.in.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/12/20 13:58
S56	44	(BSS ID or BSS-ID or BSSID or BSS identifier or BSS identification) same (plurality or multiple or several or different) near2 (BSS or basic service set) same (color or colour)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/12/20 15:43
S57	6	"9942193".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/12/20 15:46
S58	252	circuit with multi$1stage near3 (network or system) same (link or channel or path)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2019/03/29 16:59
S62	65	((("KONDA") near3 ("Venkat"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2019/03/31 23:12
S63	67	switch same (network or sub$1network) with (partition$3 or divid$3 or split$4) with (block or slic$3) same link	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2019/03/31 23:24
S64	67	S63	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2019/03/31 23:24
S65	31	multiplexer same switch same (network or sub$1network) same (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2019/03/31 23:24
S66	31	S65	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2019/03/31 23:24
S70	1	"16562450"	US-PGPUB; USPAT; FPRS; EPO;	ADJ	ON	2020/08/03 09:44

			JPO; DERWENT			
S71	2,701	H04L49/1515,102.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 10:28
S72	16,129	370/254,386,411.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 10:29
S73	106	S71 and S72	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 10:29
S74	107	venkat near2 konda.in.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 10:29
S75	29	(mux or multiplexer or multiplex$3) same switch and S74	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 10:34
S76	2	(multiple or several or different or two or many or pluralit$3 or first or second$3) near2 (logic block or programmable logic) with ("same" or similar or identical or different) with (link or channel or path or port or interface) and (multiple or several or different or two or many or pluralit$3 or first or second$3) near2 (subnetwork or sub$1network or mini$1network or mininetwork or partial network or partial multistage network or partial multi$1stage network) with ("same" or similar or identical or different) with (slice or ring or stage)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:08
S77	1	switch with (mux or multiplexer or multiplexing device or multiplexing node) same (subnetwork or partial network or mini$1network multi$1stage network or multistage network or sub$1network) and (U$1turn switch or U-switch or turn switch)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:41

S78	2	"8269523".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:48
S79	2	"8898611".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:49
S80	5	"9529958".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:49
S81	2	"8270400".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:49
S82	2	"8170040".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:49
S83	2	"8363649".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:50
S84	4	"6185220".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:51
S85	2	"6940308".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:51
S86	4	"5451936".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:51
S87	6	"6018523".pn.	US-PGPUB; USPAT; FPRS; EPO;	ADJ	ON	2020/08/03 11:52

			JPO; DERWENT			
S88	4	"5153843".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:52
S89	72	(mux or multiplexer or multiplexing device or multiplexing node) same stage same switch and (rout$3 or network) same (two-dimension$3 or 2-D) same switch	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 11:53
S90	3	internal near2 (hop wire or wire or hop cable) same external near2 (hop wire or wire or hop cable) same (Two or more or plurality or multiple or several) near2 link same (mux or multiplexer or multiplexing device or multiplexing node)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 12:27
S91	88	(multi$1stage or multistage) near2 network and internal near2 (hop wire or wire or hop cable) or external near2 (hop wire or wire or hop cable) same (mux or multiplexer or multiplexing device or multiplexing node)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	ADJ	ON	2020/08/03 12:28

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S34	228	H04L49/1515.cpc.	USPAT	ADJ	ON	2016/07/07 13:35
S35	228	H04L49/1515,202.cpc.	USPAT	ADJ	ON	2016/07/07 13:35
S36	11	Venkat near2 Konda.in.	USPAT	ADJ	ON	2016/07/07 13:35
S37	14	stage same block same (two-dimension$3 or 2-D) same switch	USPAT	ADJ	ON	2016/07/07 13:36
S38	49	link$3 same stage same switch and (rout$3 or network) same (two-dimension$3 or 2-D) same switch	USPAT	ADJ	ON	2016/07/07 13:36
S39	37	switch same (network or sub$1network) with (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	USPAT	ADJ	ON	2016/07/07 13:36
S48	42	switch same (network or sub$1network) with (partition$3 or divid$3 or split$4) near5	USPAT	ADJ	ON	2017/11/12 18:04

		(slic$3 or division or part or region or zone or section) same link				
S49	5	hierarchical near2 (rout$3 or network) same (two-dimension$3 or 2-D) same switch	USPAT	ADJ	ON	2017/11/12 18:04
S50	266	H04L49/1515,202.cpc.	USPAT	ADJ	ON	2017/11/12 18:04
S51	1	"14329876"	USPAT	ADJ	ON	2017/11/12 18:44
S59	920	H04L49/1515,102.cpc.	US-PGPUB; USPAT	ADJ	ON	2019/03/29 16:58
S60	45	venkat near2 Konda.in.	US-PGPUB; USPAT	ADJ	ON	2019/03/29 16:58
S61	146	circuit with multi$1stage near3 (network or system) same (link or channel or path)	US-PGPUB; USPAT	ADJ	ON	2019/03/29 16:59
S67	22	multiplexer same switch same (network or sub$1network) same (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	US-PGPUB; USPAT	ADJ	ON	2019/03/31 23:23
S68	89	switch same (network or sub$1network) with (partition$3 or divid$3 or split$4) near5 (slic$3 or division or part or region or zone or section) same link	US-PGPUB; USPAT	ADJ	ON	2019/03/31 23:23
S69	920	H04L49/1515,102.cpc.	US-PGPUB; USPAT	ADJ	ON	2019/03/31 23:24

8/3/2020 1:34:52 PM
C:\Users\rgidado\Documents\EAST\Workspaces\16562450.wsp

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
* 16/562,450 *	16/562,450	Konda, Venkat	
	Examiner	**Art Unit**	
	GIDADO, RASHEED	2464	

Document Code - DISQ	**Internal Document - DO NOT MAIL**

TERMINAL DISCLAIMER	☑ APPROVED	☐ DISAPPROVED
Date Filed: **06 September 2019**	**This patent is subject to a Terminal Disclaimer**	

Approved/Disapproved by:

/JEAN PROCTOR/

Technology Center: OPLC

Telephone: (571)272-1040

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/562,450	09/06/2019	Venkat Konda	V-0060US

CONFIRMATION NO. 6438

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

PUBLICATION NOTICE

OC000000115208305

Title:FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS

Publication No.US-2020-0076744-A1
Publication Date:03/05/2020

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/562,450

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	75		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	330		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	380		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*	x 50 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	x 230 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			200			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	985		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/562,450	09/06/2019		1065	V-0060US	20	3

CONFIRMATION NO. 6438

UPDATED FILING RECEIPT

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

OC000000112943050

Date Mailed: 11/27/2019

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

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Inventor(s)

Venkat Konda, San Jose, CA;

Applicant(s)

Venkat Konda, San Jose, CA;

Assignment For Published Patent Application

Konda Technologies Inc., San Jose, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 15/884,911 01/31/2018 PAT 10412025
which is a CON of 15/331,855 10/22/2016 PAT 9929977
which is a CON of 14/329,876 07/11/2014 PAT 9509634
which claims benefit of 61/846,083 07/15/2013
and is a CIP of 14/199,168 03/06/2014 PAT 9374322
which is a CON of PCT/US12/53814 09/06/2012
which claims benefit of 61/531,615 09/07/2011

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 09/16/2019

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/562,450**

Projected Publication Date: 03/05/2020

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: Yes

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Electronic Patent Application Fee Transmittal

Application Number:	16562450
Filing Date:	06-Sep-2019
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Filer:	Venkat Konda
Attorney Docket Number:	V-0060US

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY FILING FEE (ELECTRONIC FILING)	4011	1	75	75
UTILITY SEARCH FEE	2111	1	330	330
UTILITY EXAMINATION FEE	2311	1	380	380
Pages:				
UTILITY APPL SIZE FEE PER 50 SHEETS >100	2081	1	200	200
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	2051	1	80	80

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1065**

Electronic Acknowledgement Receipt	
EFS ID:	37497374
Application Number:	16562450
International Application Number:	
Confirmation Number:	6438
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkat Konda
Filer Authorized By:	
Attorney Docket Number:	V-0060US
Receipt Date:	18-OCT-2019
Filing Date:	06-SEP-2019
Time Stamp:	13:11:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1065
RAM confirmation Number	E20190HD14121474
Deposit Account	
Authorized User	
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Fee Worksheet (SB06)	fee-info.pdf	38429 3e99e8abbbf9f57caf2985263d0ab9aa41e41b92	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	38429		

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National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/562,450	09/06/2019	Venkat Konda	V-0060US

CONFIRMATION NO. 6438

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

PGPUB REJECTION NOTICE

OC000000111787513

Date Mailed: 10/10/2019

NOTICE REGARDING NONPUBLICATION REQUEST

The nonpublication request filed on 10/07/2019 is acknowledged.

- The request cannot be accepted because 35 U.S.C. § 122(b)(2)(B)(i) and 37 CFR 1.213 require that any nonpublication request be submitted upon filing. Therefore, the application remains subject to the publication provisions of 35 U.S.C. § 122(b) and 37 CFR 1.211.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ltaba/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/562,450	09/06/2019	Venkat Konda	V-0060US

CONFIRMATION NO. 6438

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

FORMALITIES LETTER

OC000000111787512

Date Mailed: 10/10/2019

NOTICE OF INCOMPLETE REPLY (NONPROVISIONAL)

Filing Date Granted

The U.S. Patent and Trademark Office has received your reply on 10/07/2019 to the NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION (Notice) mailed 09/19/2019 and it has been entered into the application. The reply, however, is not a complete reply for the reason(s) listed below. A complete reply must be timely filed to prevent ABANDONMENT of the above-identified application. Replies should be mailed to: Mail Stop Missing Parts, Commissioner for Patents, P.O.Box 1450, Alexandria VA 22313-1450.

The period for reply continues to run from the date of the Notice mailed 09/19/2019. Applicant must submit all required items and pay any fees required below within two months from the date of the NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION to avoid abandonment. If the reply is submitted after two months from the date of the NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION, extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

Items Required to Avoid Abandonment:

The required items noted below SHOULD be filed along with any items required above.

- The statutory basic filing fee is missing.
- The application search fee was not received.
- The application examination fee was not received.
- Surcharge as set forth in 37 CFR 1.16(f) was not received.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of the Notice to avoid abandonment is/are itemized below. Small entity discount is in effect. If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **75** basic filing fee.
- $ **200** for **21** electronically equivalent pages in excess of **100** application size fee.
- $ **80** surcharge.
- $ **330** search fee.
- $ **380** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1065** TOTAL FEE BALANCE DUE.

Mail date of Notice: 09/19/2019

Last date that extension may be obtained: (Note: The petition and fee must be received by this date, or include a proper certificate of mailing under 37 CFR 1.8 with a date on or before this date, and extend the time to include this date.) 04/19/2020

Length of Extension of Time	Fee under 37 CFR 1.17(a) effective March 19, 2013		
(response due on or before)	Undiscounted	Small Entity	Micro Entity
One Month (12/19/2019)	$200	$100	$50
Two Months (01/19/2020)	$600	$300	$150
Three Months (02/19/2020)	$1400	$700	$350
Four Months (03/19/2020)	$2200	$1100	$550
Five Months (04/19/2020)	$3000	$1500	$750

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ltaba/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/562,450	09/06/2019	Venkat Konda	V-0060US

CONFIRMATION NO. 6438

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

OC000000111787515

Date Mailed: 10/10/2019

NOTICE OF ACCEPTANCE OF AUTHORIZATION TO PERMIT ACCESS TO APPLICATION VIA PRIORITY DOCUMENT EXCHANGE

This is in response to the applicant's authorization to permit access to the application-as-filed by participating offices under 37 CFR 1.14(h)(1) submitted on 10/07/2019.

The authorization to permit access to the application under 37 CFR 1.14(h)(1) is accepted.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ltaba/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/562,450	09/06/2019	Venkat Konda	V-0060US

CONFIRMATION NO. 6438

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

OC000000111787518

Date Mailed: 10/10/2019

NOTICE OF ACCEPTANCE OF AUTHORIZATION TO PERMIT ACCESS TO SEARCH RESULTS

This is in response to the applicant's authorization to permit access to the search results from the instant application under 37 CFR 1.14(h)(2) submitted on 10/07/2019.

The authorization to permit access to the search results under 37 CFR 1.14(h)(2) is accepted.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ltaba/

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/562,450

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	75		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	330		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	380		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*	x 50 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	x 230 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			200			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	985		TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

Doc Code: PD.TO.AUTH
Document Description: Auth or Resc of Auth to Access Appl by DAS/PDX Office

PTO/SB/39 (11-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

AUTHORIZATION OR RESCISSION OF AUTHORIZATION TO PERMIT ACCESS TO APPLICATION-AS-FILED BY PARTICIPATING OFFICES

Send completed form to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

Application Number (if known):	Filing Date:
16/562,450	09/09/2019
First Named Inventor:	Attorney Docket Number:
Venkat Konda	V-0060US

Title (Required)
Fast Scheduling and Optimization of Multi-Stage Hierarchical Networks

Check either box 1 or 2 below, but **not** both:

1. ☒ By checking this box, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization(WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

2. ☐ By checking this box, the undersigned hereby **rescinds the previous authority granted to the USPTO** to provide the EPO, JPO, KIPO, SIPO, WIPO or any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement access to the documents and information identified in paragraph 1 above.

This rescission of the previous authorization will not be effective unless and until an appropriate USPTO official recognizes and acts on the rescission.

However, once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

NOTE: This form must be signed by an authorized party in accordance with 37 CFR 1.14(c). Please see 37 CFR 1.4(d) for the form of the signature. If necessary, submit multiple forms for more than one signature, see below.*

Signature /Venkat Konda/	Date 10/07/2019
Name (Print/Typed) Venkat Konda	Practitioner Registration Number (If applicable)
Name of Assignee (if applicable)	Title (if applicable)

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.14(h). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	37387274
Application Number:	16562450
International Application Number:	
Confirmation Number:	6438
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkat Konda
Filer Authorized By:	
Attorney Docket Number:	V-0060US
Receipt Date:	07-OCT-2019
Filing Date:	06-SEP-2019
Time Stamp:	17:37:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	V-0060US-aia0014-Scan.pdf	9587927 dd552debcf544f706e555bb2dac9ee6df9e6d8af	no	7

Warnings:

Information:					
This is not an USPTO supplied ADS fillable form					
2	Auth or Resc of Auth to Access Search Results	V-0060US-sb0039.pdf	115171 3a90f45dbee54bab06b7e2b48a7681a07d32a58c	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	9703098	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/14 (12-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	V-0060US
	Application Number	
Title of Invention	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
Dr.	Venkat		Konda	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	San Jose	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	6278 Grand Oak Way		
Address 2			
City	San jose	State/Province	CA
Postal Code	95135	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	38139		
Email Address	venkat@kondatech.com	Add Email	Remove Email

Application Information:

Title of the Invention	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS		
Attorney Docket Number	V-0060US	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	30	Suggested Figure for Publication (if any)	6B

Filing By Reference :

PTO/AIA/14 (12-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	V-0060US
	Application Number	
Title of Invention	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS	

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☒ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	38139		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	15/884911	2018-01-31
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/884911	Continuation of	15/331855	2016-10-22	9929977	2018-03-27

Prior Application Status	Patented	Remove

PTO/AIA/14 (12-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	V-0060US
	Application Number	
Title of Invention	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS	

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/331855	Continuation of	14/329876	2014-07-11	9509634	2016-11-29

Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
14/329876	Claims benefit of provisional	61/846083	2013-07-15

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14/329876	Continuation in part of	14/199168	2014-03-06	9374322	2016-06-21

Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
14/199168	Continuation of	PCT/US12/53814	2012-09-06

Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
PCT/US12/53814	Claims benefit of provisional	61/531615	2011-09-07

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

PTO/AIA/14 (12-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	V-0060US
	Application Number	
Title of Invention	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☒ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (12-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	V-0060US
	Application Number	
Title of Invention	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS	

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	Konda Technologies Inc.		
Mailing Address Information For Applicant:			
Address 1	6278 Grand Oak Way		
Address 2			
City	San Jose	**State/Province**	CA
Country	US	Postal Code	95135
Phone Number	408-472-3273	Fax Number	408-238-2478
Email Address	venkat@kondatech.com		

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

PTO/AIA/14 (12-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	V-0060US
	Application Number	
Title of Invention	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS	

Organization Name	Konda Technologies Inc.

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	6278 Grand Oak Way		
Address 2			
City	San Jose	**State/Province**	CA
Country i	US	Postal Code	95135
Phone Number	408-472-3273	Fax Number	408-238-2478
Email Address	venkat@kondatech.com		

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	/venkat konda/			Date (YYYY-MM-DD)	2019-10-07
First Name	Venkat	Last Name	Konda	Registration Number	

Additional Signature may be generated within this form by selecting the Add button.

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent C o o p eration Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/562,450

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	75		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	330		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	380		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*	x 50 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	x 230 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			200			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	985		TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/562,450	09/06/2019	Venkat Konda	V-0060US

CONFIRMATION NO. 6438

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

FORMALITIES LETTER

OC000000111190823

Date Mailed: 09/19/2019

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- Complete residence information, either city and state or city and country for **Venkat Konda** has not been provided. Residence information is required, separately from the mailing address, if the inventor lives at a location which is different from where the inventor customarily receives mail. Also, a valid state code or a valid country code must be provided. For lists of valid state and valid country codes, see the Instructions for Application Data Sheet available at https://www.uspto.gov/patent/forms/forms-patent-applications-filed-or-after-september-16-2012. There is an indication on either the ADS or the inventor's oath or declaration that the mailing address and residence information is not the same for this inventor.
  Applicant must provide the residence information on either:
  - An inventor's oath or declaration in compliance with 37 CFR 1.63, or
  - A properly marked up application data sheet (ADS) in compliance with 37 CFR 1.76.
- A complete mailing address that includes either the city and state or city and country, for each inventor has not been submitted. Applicant must provide the mailing address on either:
  - An inventor's oath or declaration in compliance with 37 CFR 1.63, or
  - A properly marked up application data sheet (ADS) in compliance with 37 CFR 1.76.

  Note that an inventor's mailing address is required even if a correspondence address has been submitted. An inventor's mailing address may not necessarily be the same as the correspondence address for the application and must be separately submitted in the manner set forth above. If the inventor lives at a location which is different from the inventor's mailing address, the inventor's residence (either city and state or city and country) must also be separately submitted in the manner set forth above. For lists of valid state and valid country codes, see the Instructions for Application Data Sheet available at https://www.uspto.gov/patent/forms/forms-patent-applications-filed-or-after-september-16-2012.
  Mailing address information is needed for the following inventor(s): **Venkat Konda**
- The statutory basic filing fee is missing.

- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. Small entity discount is in effect. If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **75** basic filing fee.
- $ **200** for **21** electronically equivalent pages in excess of **100** application size fee.
- $ **80** surcharge.
- $ **330** search fee.
- $ **380** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1065** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- The ADS received on 09/06/2019 was not properly signed. Therefore, the Office will treat it only as a transmittal letter. See 37 CFR 1.76(e). Inventorship has not been set by this document and any foreign priority or domestic benefit claims contained therein are ineffective. See 37 CFR 1.55 or 37 CFR 1.78.
  If the applicant wishes to submit another ADS:
  - o It must be properly signed by a party under 37 CFR 1.33(b), and be signed in compliance with 37 CFR 1.4(d).
  - o Changes to the information of record must be properly marked up in compliance with 37 CFR 1.76(c), i.e., must identify the information that is being changed, with underlining for insertions, and strike-through or brackets for text removed. In general, the identification of the information being changed should be made relative to the most recent filing receipt.
  - o Benefit and priority claims must be presented in an ADS in compliance with 37 CFR 1.76(c) and within the time periods specified in 37 CFR 1.55 and 1.78.

  If an ADS as set forth above is provided, the filing of the inventor's oath or declaration may be postponed until the application is otherwise in condition for allowance. See 37 CFR 1.53(f). Note that the inventor's oath or declaration must be filed no later than the date on which the issue fee has been paid.

In order to make changes to the information of record, an ADS must be properly signed and properly marked up relative to the current information of record.

Proper signature: The ADS must be signed with a handwritten signature or proper S-signature by:

- A patent practitioner, with the practitioner's registration number accompanying the signature (e.g., immediately below or adjacent to the signature), or
- The applicant, if the applicant is an individual other than the inventor(s) and no power of attorney has been appointed, or

• All of the inventors, if no other applicant has been established and no power of attorney has been appointed. A proper S-signature consists of only letters and/or Arabic numerals, with appropriate spaces and commas, periods, apostrophes, or hyphens for punctuation contained between a first single forward slash mark before, and a second single forward slash mark after, the S-signature.

Proper markings: The ADS must identify the changes being made with underlining for insertions and strike-through or brackets for text removed. No other markings or indications are acceptable. Where an ADS providing corrected or updated information does not contain all of the sections of the ADS, the entire section in which changes are being made must be included in the ADS. Information of record can generally be found on the latest filing receipt.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/hchin/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/562,450	09/06/2019	Venkat Konda	V-0060US

CONFIRMATION NO. 6438

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

PGPUB REJECTION NOTICE

OC000000111190824

Date Mailed: 09/19/2019

NOTICE REGARDING NONPUBLICATION REQUEST

The nonpublication request filed on 09/06/2019 is acknowledged.

- The request for non-publication has not been recognized because it is not signed in compliance with 37 CFR 1.33(b) as required by 37 CFR 1.213(a)(4).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/hchin/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/562,450	09/06/2019	Venkat Konda	V-0060US

CONFIRMATION NO. 6438

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

OC000000111190826

Date Mailed: 09/19/2019

Improper Submission of Authorization to Permit Access to Application by Participating Offices under 37 CFR 1.14(h)(1) (Priority Document Exchange)

The Authorization to Permit Access to Application-As-Filed by Participating Offices under 37 CFR 1.14(h)(1) (authorization to permit access to application via priority document exchange) submitted on 09/06/2019 in the above-identified application is not accepted because:

- It was not properly signed. If applicant still wishes to provide authorization to permit access under 37 CFR 1.14(h)(1), applicant must submit a properly signed authorization (e.g., PTO/SB/39).

Any authorization should be submitted prior to filing a subsequent foreign application with a participating intellectual property office in which priority is claimed to the above-identified U.S. application to ensure that it is likely that the participating foreign intellectual property office will be successful in its attempt to retrieve a copy of the U.S. priority application from the Office.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/hchin/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/562,450	09/06/2019		0.00	V-0060US	20	3

CONFIRMATION NO. 6438

38139
Konda Technologies, Inc
6278 GRAND OAK WAY
SAN JOSE, CA 95135

FILING RECEIPT

OC000000111190822

Date Mailed: 09/19/2019

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Venkat Konda, Residence Not Provided;

Applicant(s)

Venkat Konda, Residence Not Provided;

Power of Attorney: None

Domestic Applications for which benefit is claimed - None.
A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 09/16/2019

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/562,450**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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PTO/AIA/15 (03-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	V-0060US
First Named Inventor	Venkat Konda
Title	
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [✓] **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. [✓] **Applicant asserts small entity status.** See 37 CFR 1.27
3. [ ] **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. [✓] **Specification** [*Total Pages* 134] Both the claims and abstract must start on a new page. *(See MPEP § 608.01(a) for information on the preferred arrangement)*
5. [✓] **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 30]
6. **Inventor's Oath or Declaration** [*Total Pages* ____] *(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   a. [✓] Newly executed (original or copy)
   b. [ ] A copy from a prior application (37 CFR 1.63(d))
7. [✓] **Application Data Sheet** ** See note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. **CD-ROM or CD-R** in duplicate, large table, or Computer Program (*Appendix*)
   [ ] Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission** (*if applicable, items a. – c. are required*)
   a. [ ] Computer Readable Form (CRF)
   b. [ ] Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] Paper
   c. [ ] Statements verifying identity of above copies

ADDRESS TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**

ACCOMPANYING APPLICATION PAPERS

10. [ ] **Assignment Papers** (cover sheet & document(s)) Name of Assignee ____
11. [ ] **37 CFR 3.73(c) Statement** (*when there is an assignee*) [ ] **Power of Attorney**
12. [ ] **English Translation Document** (*if applicable*)
13. [ ] **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    [ ] Copies of citations attached
14. [ ] **Preliminary Amendment**
15. [ ] **Return Receipt Postcard** (*MPEP § 503*) (*Should be specifically itemized*)
16. [ ] **Certified Copy of Priority Document(s)** (*if foreign priority is claimed*)
17. [ ] **Nonpublication Request** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. [ ] **Other:** ____

*Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS

[✓] The address associated with Customer Number: 38139 **OR** [ ] Correspondence address below

Name	Venkat Konda				
Address	6278 Grand Oak Way				
City	San Jose	State	CA	Zip Code	95135
Country	USA	Telephone	408-472-3273	Email	venkat@kondatech.com

Signature	/Venkat Konda/	Date	09-06-2019
Name (Print/Type)	Venkat Konda	Registration No. (Attorney/Agent)	

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/01 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [■] The attached application, or
- [ ] United States application or PCT international application number _____

  filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Venkat Konda Date (Optional): 09-06-2019

Signature: /Venkat Konda/

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal					
Application Number:					
Filing Date:					
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS				
First Named Inventor/Applicant Name:	venkat konda				
Filer:	Venkat Konda				
Attorney Docket Number:	V-0060US				
Filed as Small Entity					
Filing Fees for Utility under 35 USC 111(a)					
Description		**Fee Code**	**Quantity**	**Amount**	**Sub-Total in USD($)**
Basic Filing:					
UTILITY FILING FEE (ELECTRONIC FILING)		4011	1	75	75
UTILITY SEARCH FEE		2111	1	330	330
UTILITY EXAMINATION FEE		2311	1	380	380
Pages:					
UTILITY APPL SIZE FEE PER 50 SHEETS >100		2081	1	200	200
Claims:					
Miscellaneous-Filing:					
Petition:					

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**985**

Electronic Acknowledgement Receipt	
EFS ID:	37083112
Application Number:	16562450
International Application Number:	
Confirmation Number:	6438
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS
First Named Inventor/Applicant Name:	venkat konda
Customer Number:	38139
Filer:	Venkat Konda
Filer Authorized By:	
Attorney Docket Number:	V-0060US
Receipt Date:	06-SEP-2019
Filing Date:	
Time Stamp:	03:24:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Specification	V-0060US.pdf	541046 047936c9be6180ed77b390e378c15252d5f4a487	no	134
Warnings:					

Information:					
2	Drawings-only black and white line drawings	V-0060US-Figs.pdf	276200 c086396fa0fc587963dde0882b4af9a14005e795	no	30
Warnings:					
Information:					
3	Application Data Sheet	V-0060US-aia0014.pdf	1597701 33ae4f6c1775c84c6508a723d7408a7e8e30950c	no	7
Warnings:					
Information:					
4	Transmittal of New Application	V-0060US-aia0015.pdf	338087 15516d7084a8bbe0dfd13d3738850c010088a311	no	2
Warnings:					
Information:					
5	Oath or Declaration filed	V-0060US-aia0001.pdf	150928 3d0bf8df96a455cf5a82b0dd39758629779f4a0d	no	2
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	36706 0d219330327f7f14f88aa62af8a05a558d02c381	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2940668		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

FIG. 1A

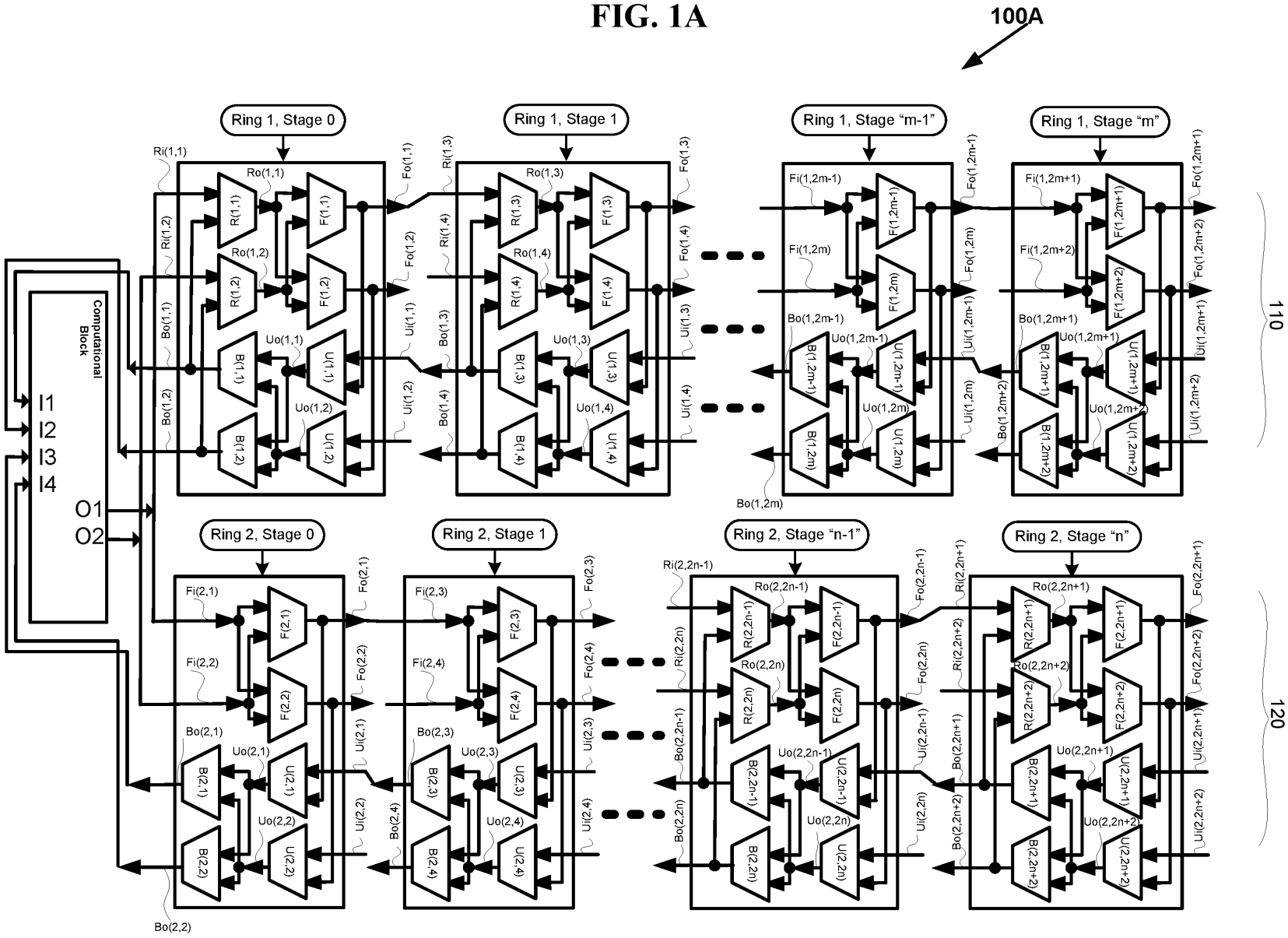
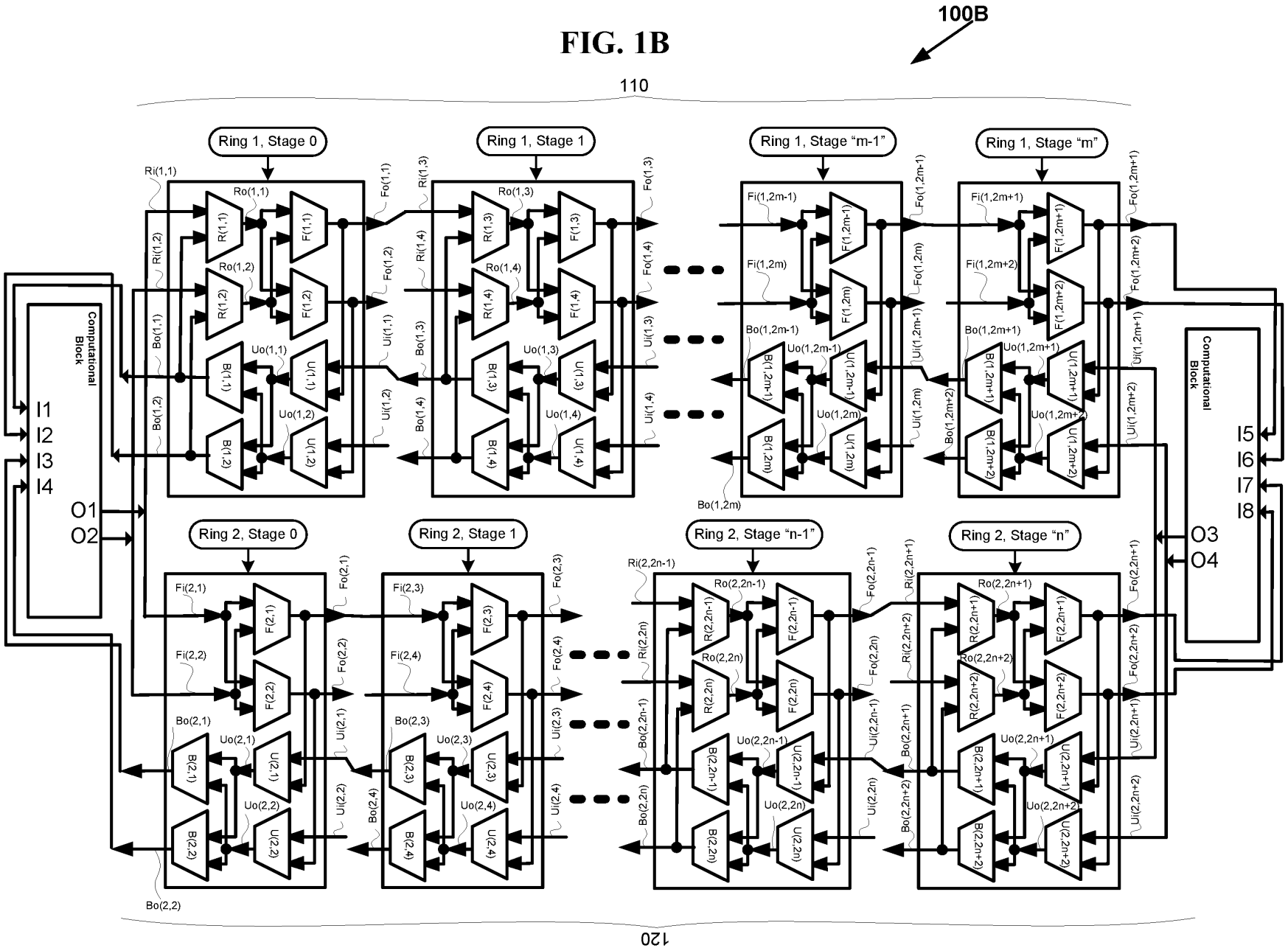

100A
Ring 1, Stage 0
Ring 1, Stage 1
Ring 1, Stage "m-1"
Ring 1, Stage "m"
Ring 2, Stage 0
Ring 2, Stage 1
Ring 2, Stage "n-1"
Ring 2, Stage "n"
Computational Block
I1
I2
I3
I4
O1
O2
110
120

FIG. 1B


100B
110
120
Ring 1, Stage 0
Ring 1, Stage 1
Ring 1, Stage "m-1"
Ring 1, Stage "m"
Ring 2, Stage 0
Ring 2, Stage 1
Ring 2, Stage "n-1"
Ring 2, Stage "n"
Computational Block
I1
I2
I3
I4
O1
O2
I5
I6
I7
I8
O3
O4

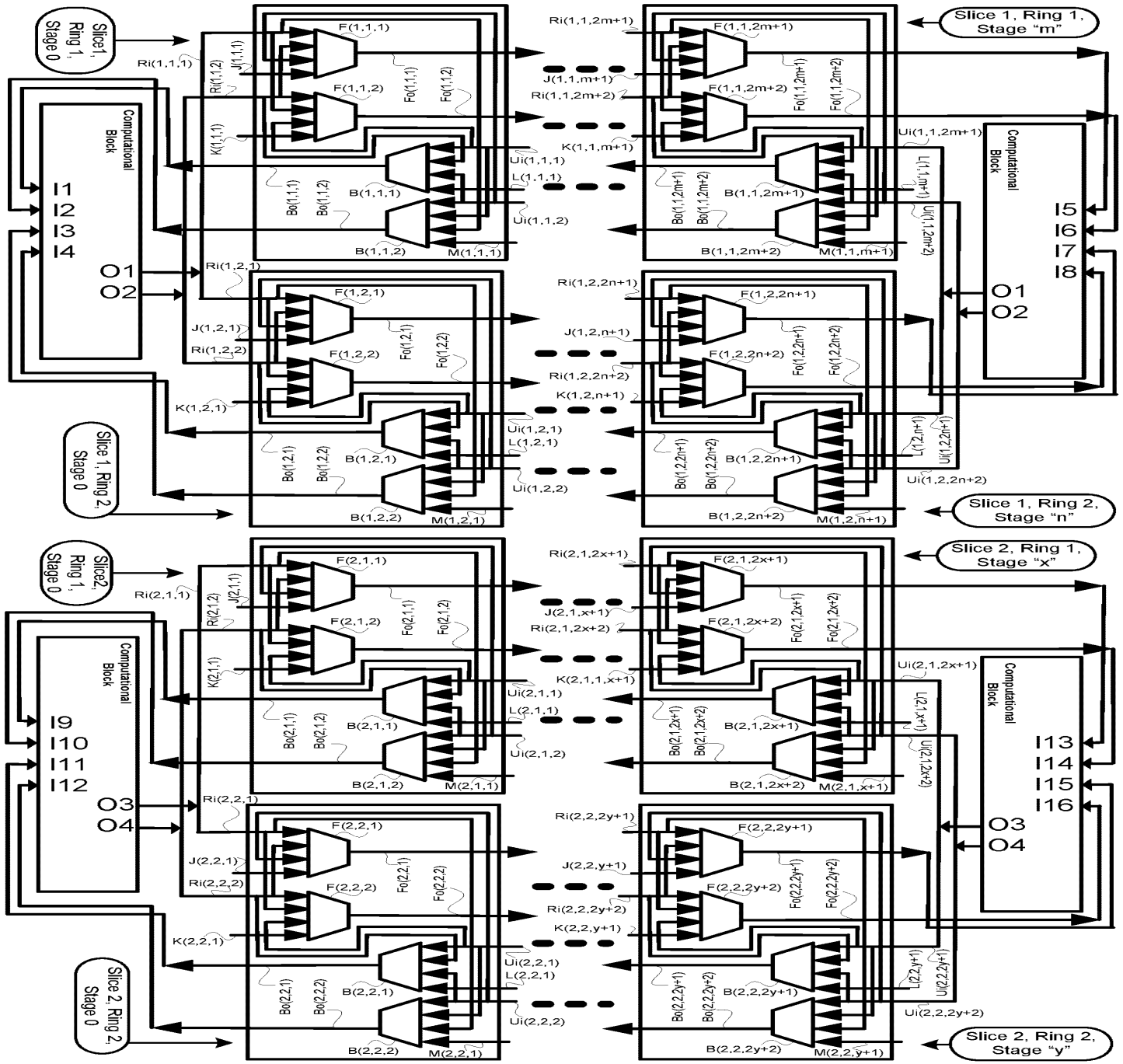

Slice1, Ring 1, Stage 0
Slice 1, Ring 2, Stage 0
Slice2, Ring 1, Stage 0
Slice 2, Ring 2, Stage 0
Slice 1, Ring 1, Stage "m"
Slice 1, Ring 2, Stage "n"
Slice 2, Ring 1, Stage "x"
Slice 2, Ring 2, Stage "y"
Computational Block
I1 I2 I3 I4
O1 O2
I5 I6 I7 I8
I9 I10 I11 I12
O3 O4
I13 I14 I15 I16
F(1,1,1)
F(1,1,2)
Fo(1,1,1)
Fo(1,1,2)
Ri(1,1,1)
J(1,1,1)
Ri(1,1,2)
K(1,1,1)
Bo(1,1,1)
Bo(1,1,2)
B(1,1,1)
B(1,1,2)
M(1,1,1)
Ui(1,1,1)
L(1,1,1)
Ui(1,1,2)
Ri(1,1,2m+1)
J(1,1,m+1)
Ri(1,1,2m+2)
K(1,1,m+1)
Ui(1,1,2m+1)
L(1,1,m+1)
Ui(1,1,2m+2)
Ri(1,2,1)
J(1,2,1)
Ri(1,2,2)
K(1,2,1)
Ri(1,2,2n+1)
J(1,2,n+1)
Ri(1,2,2n+2)
K(1,2,n+1)
Ui(1,2,1)
L(1,2,1)
Ui(1,2,2)
Ui(1,2,2n+2)
Ri(2,1,1)
Ri(2,1,2x+1)
Ri(2,2,1)
Ri(2,2,2y+1)
Ui(2,1,1)
Ui(2,1,2)
Ui(2,1,2x+1)
Ui(2,2,1)
Ui(2,2,2)
Ui(2,2,2y+2)

FIG. 1C

100C

FIG. 1C1

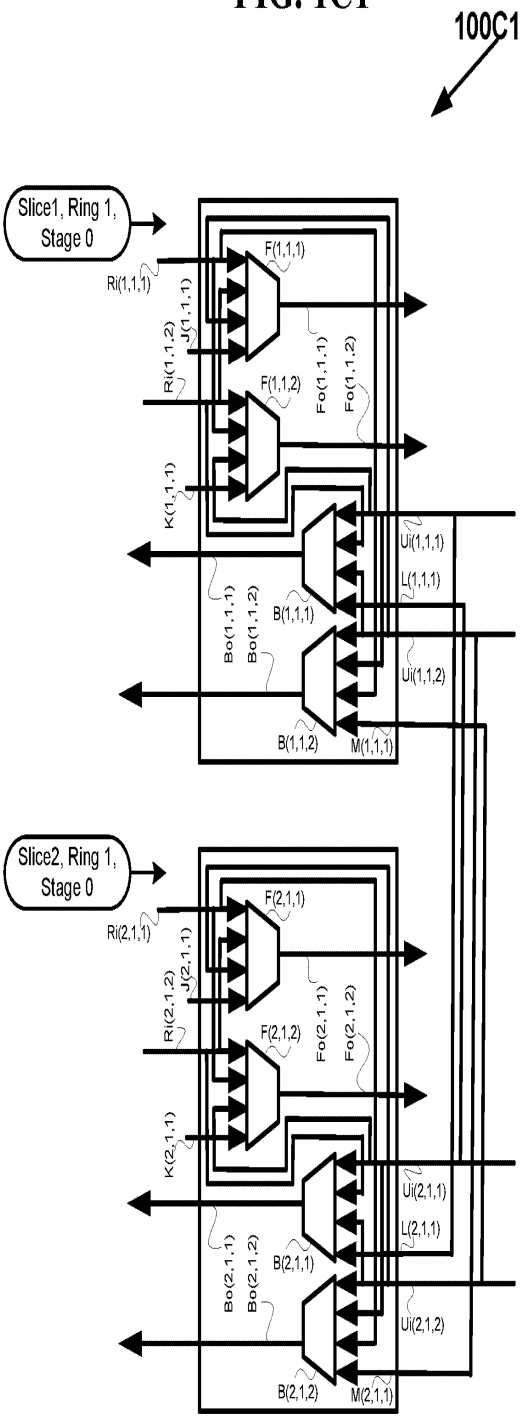


FIG. 1C2

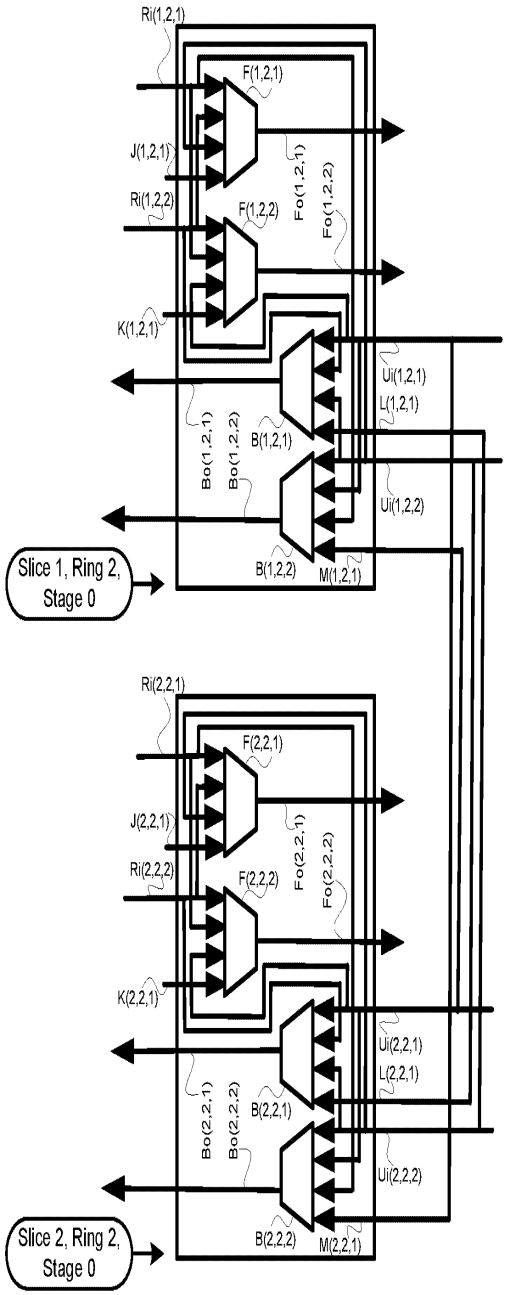


FIG. 1C3

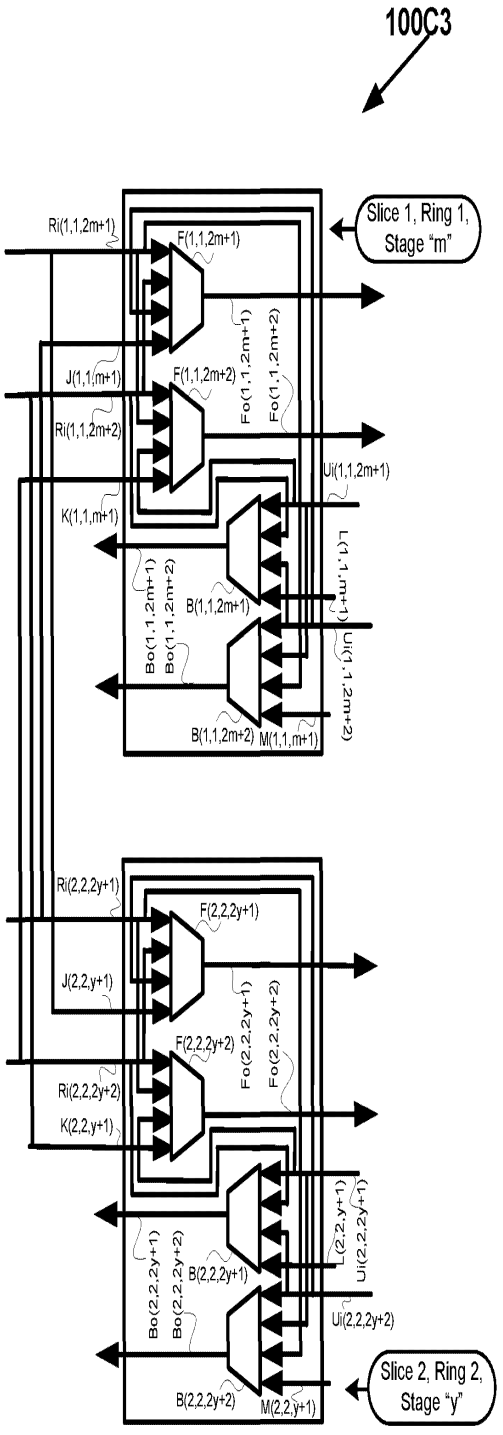


FIG. 1C4

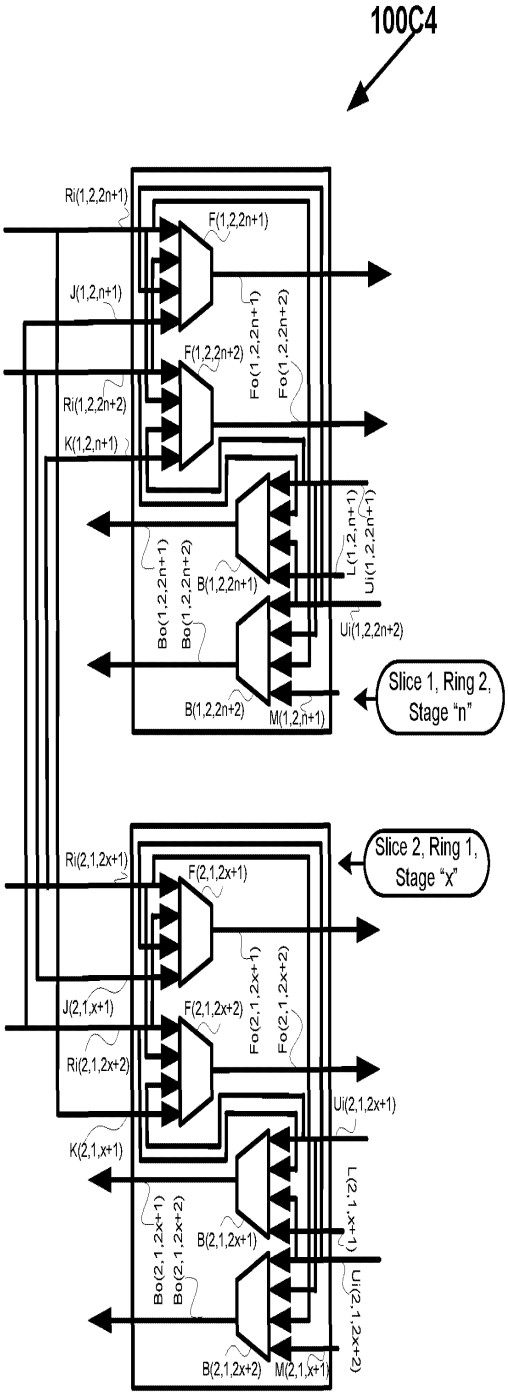


FIG. 1C5

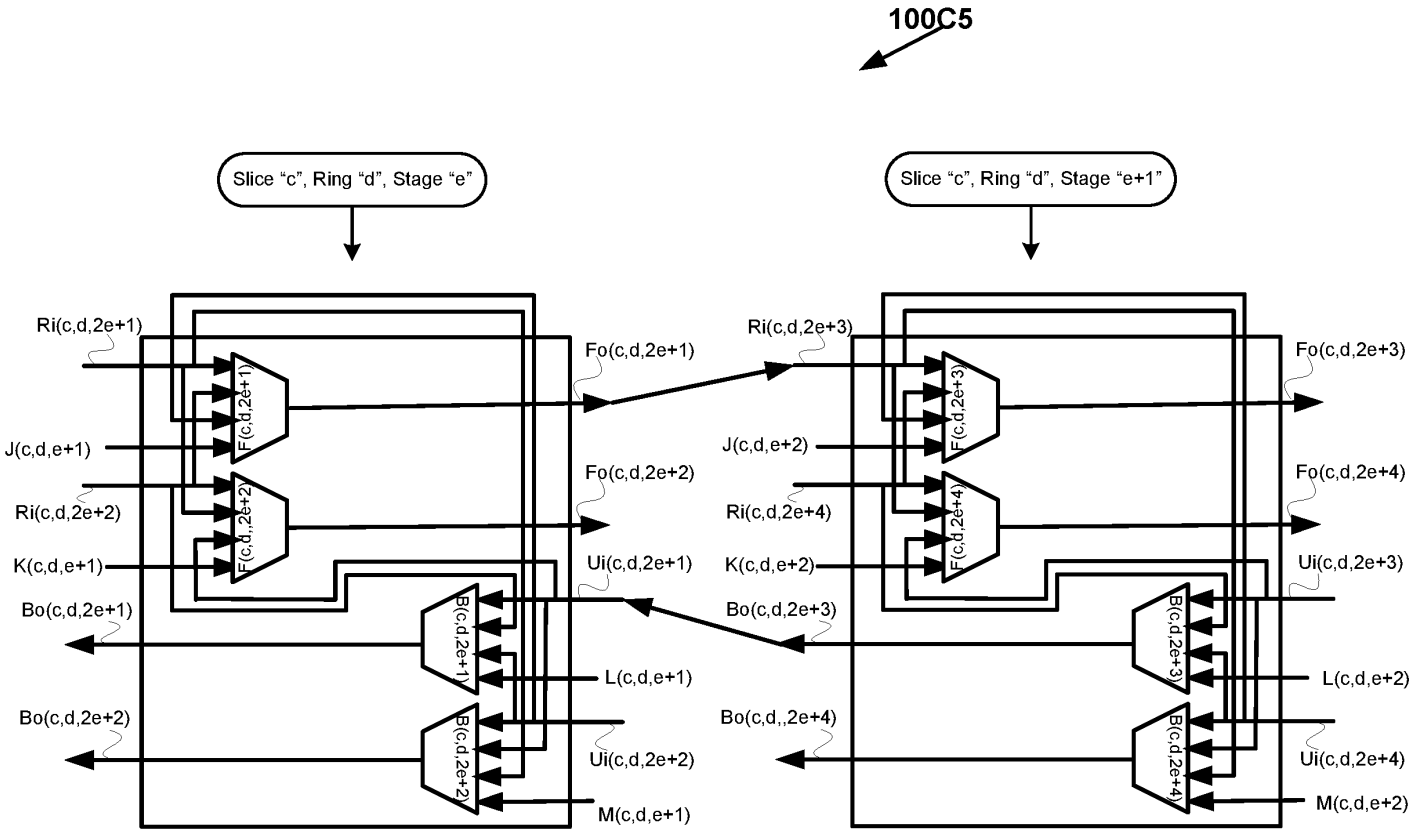

100C5
Slice "c", Ring "d", Stage "e"
Slice "c", Ring "d", Stage "e+1"
Ri(c,d,2e+1)
J(c,d,e+1)
Ri(c,d,2e+2)
K(c,d,e+1)
Bo(c,d,2e+1)
Bo(c,d,2e+2)
Fo(c,d,2e+1)
Fo(c,d,2e+2)
Ui(c,d,2e+1)
L(c,d,e+1)
Ui(c,d,2e+2)
M(c,d,e+1)
F(c,d,2e+1)
F(c,d,,2e+2)
B(c,d,2e+1)
B(c,d,2e+2)
Ri(c,d,2e+3)
J(c,d,e+2)
Ri(c,d,2e+4)
K(c,d,e+2)
Bo(c,d,2e+3)
Bo(c,d,,2e+4)
Fo(c,d,2e+3)
Fo(c,d,2e+4)
Ui(c,d,2e+3)
L(c,d,e+2)
Ui(c,d,2e+4)
M(c,d,e+2)
F(c,d,2e+3)
F(c,d,2e+4)
B(c,d,2e+3)
B(c,d,2e+4)

FIG. 2A

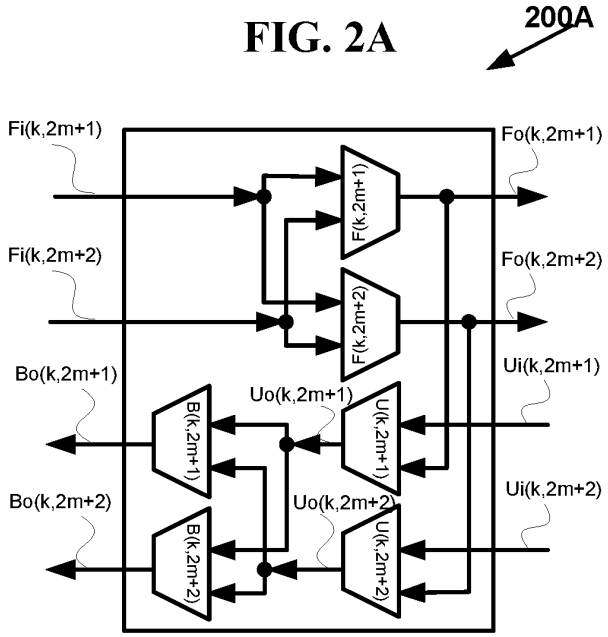


FIG. 2B

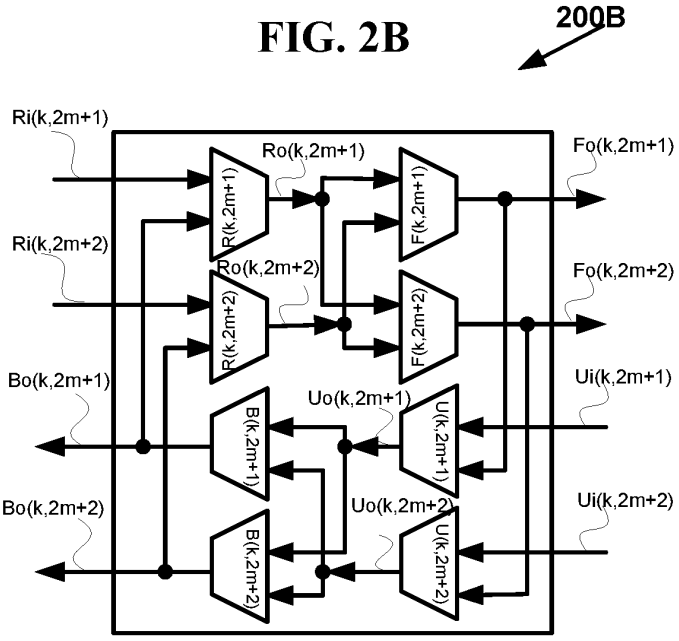


FIG. 2C

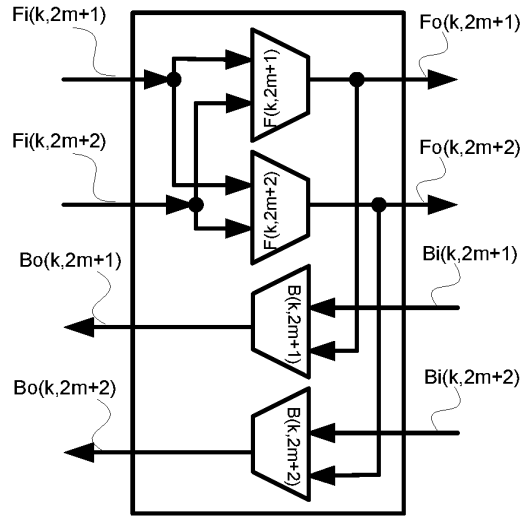


FIG. 2D

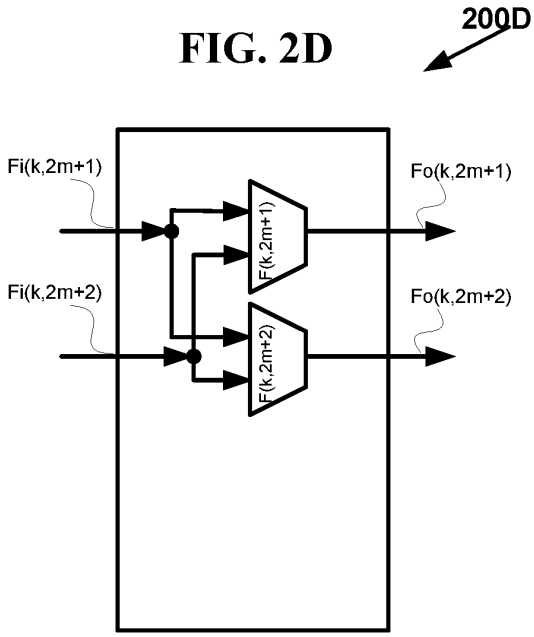


FIG. 2E

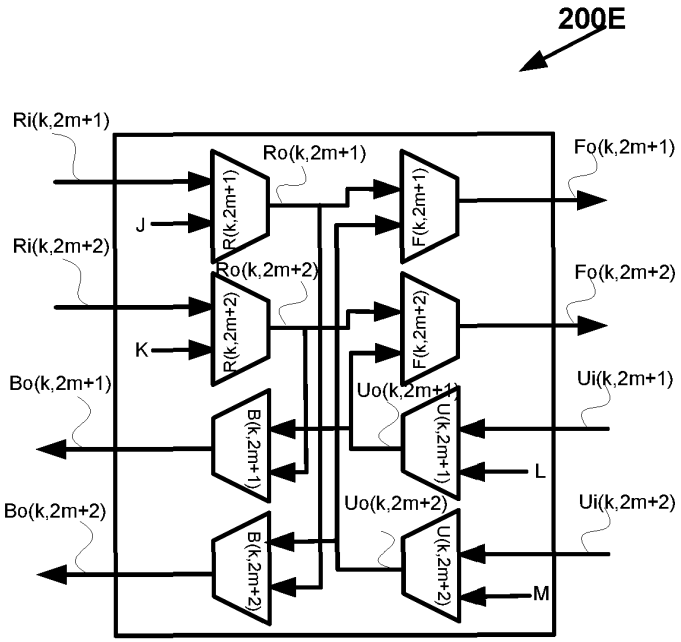

200E
Ri(k,2m+1)
Ro(k,2m+1)
Fo(k,2m+1)
J
R(k,2m+1)
F(k,2m+1)
Ri(k,2m+2)
Ro(k,2m+2)
Fo(k,2m+2)
K
R(k,2m+2)
F(k,2m+2)
Bo(k,2m+1)
Uo(k,2m+1)
Ui(k,2m+1)
B(k,2m+1)
U(k,2m+1)
L
Bo(k,2m+2)
Uo(k,2m+2)
Ui(k,2m+2)
B(k,2m+2)
U(k,2m+2)
M

FIG. 2F

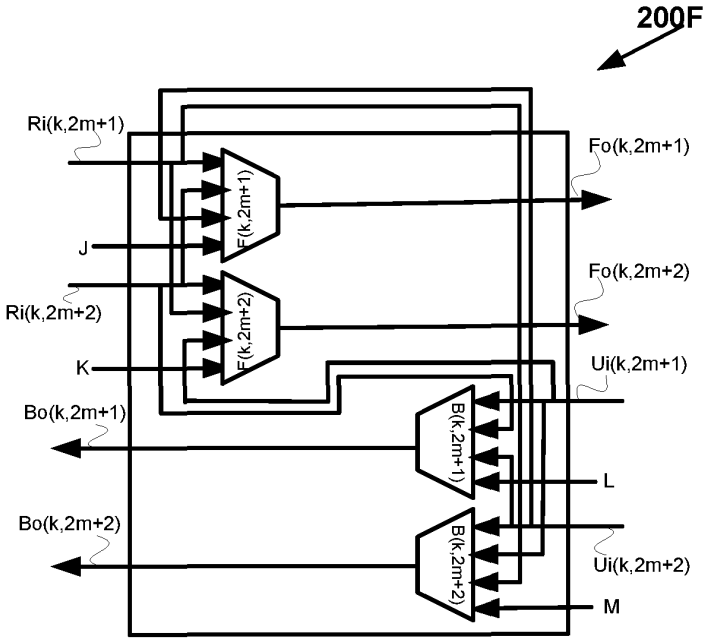

200F
Ri(k,2m+1)
Fo(k,2m+1)
F(k,2m+1)
J
Fo(k,2m+2)
Ri(k,2m+2)
F(k,2m+2)
K
Ui(k,2m+1)
Bo(k,2m+1)
B(k,2m+1)
L
Bo(k,2m+2)
B(k,2m+2)
Ui(k,2m+2)
M

FIG. 3A

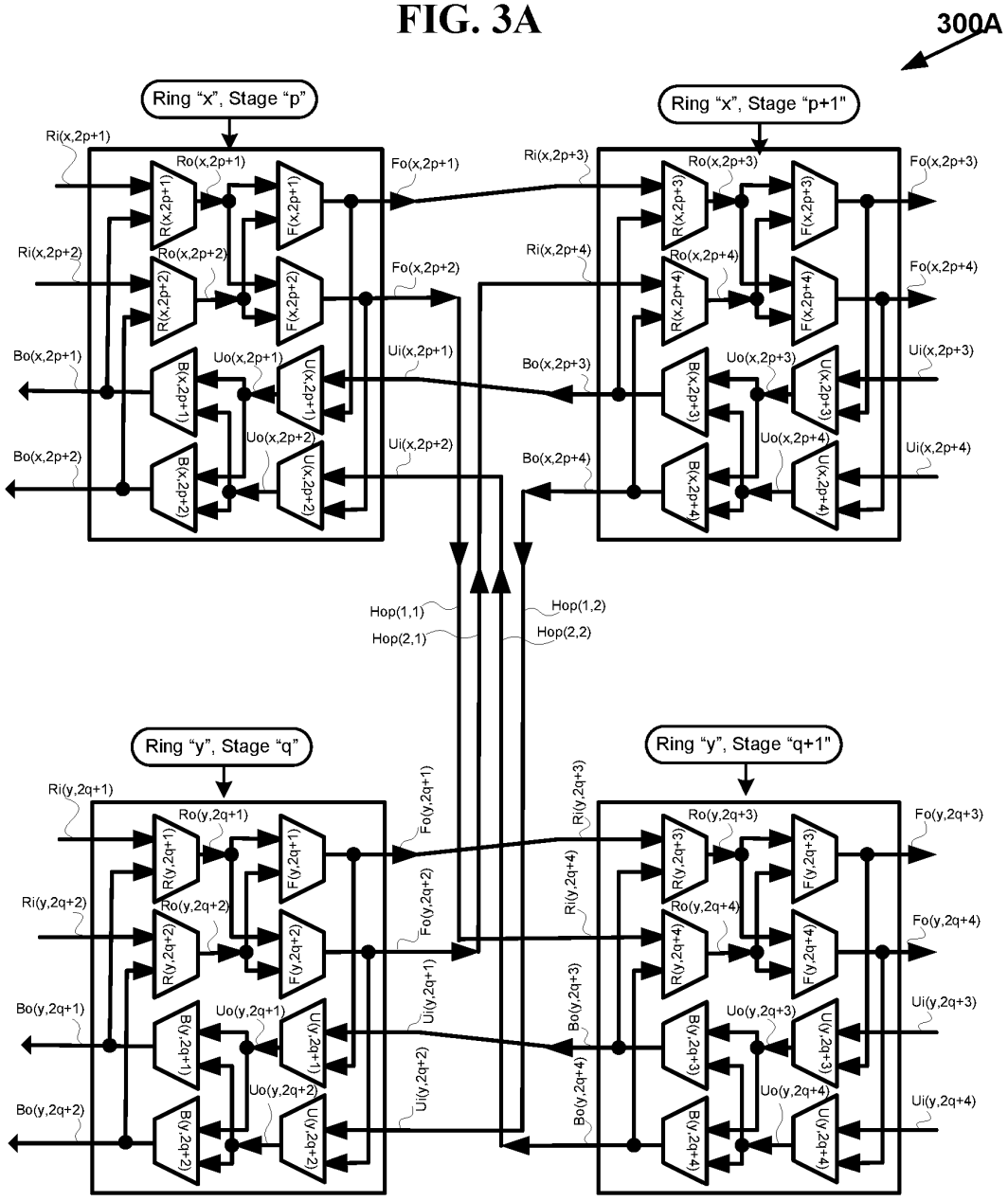

300A
Ring "x", Stage "p"
Ring "x", Stage "p+1"
Ring "y", Stage "q"
Ring "y", Stage "q+1"
Ri(x,2p+1)
Ro(x,2p+1)
Fo(x,2p+1)
Ri(x,2p+2)
Ro(x,2p+2)
Fo(x,2p+2)
Bo(x,2p+1)
Uo(x,2p+1)
Ui(x,2p+1)
Bo(x,2p+2)
Uo(x,2p+2)
Ui(x,2p+2)
Ri(x,2p+3)
Ro(x,2p+3)
Fo(x,2p+3)
Ri(x,2p+4)
Ro(x,2p+4)
Fo(x,2p+4)
Bo(x,2p+3)
Uo(x,2p+3)
Ui(x,2p+3)
Bo(x,2p+4)
Uo(x,2p+4)
Ui(x,2p+4)
Hop(1,1)
Hop(2,1)
Hop(1,2)
Hop(2,2)
Ri(y,2q+1)
Ro(y,2q+1)
Fo(y,2q+1)
Ri(y,2q+2)
Ro(y,2q+2)
Fo(y,2q+2)
Bo(y,2q+1)
Uo(y,2q+1)
Ui(y,2q+1)
Bo(y,2q+2)
Uo(y,2q+2)
Ui(y,2q+2)
Ri(y,2q+3)
Ro(y,2q+3)
Fo(y,2q+3)
Ri(y,2q+4)
Ro(y,2q+4)
Fo(y,2q+4)
Bo(y,2q+3)
Uo(y,2q+3)
Ui(y,2q+3)
Bo(y,2q+4)
Uo(y,2q+4)
Ui(y,2q+4)

FIG. 3B

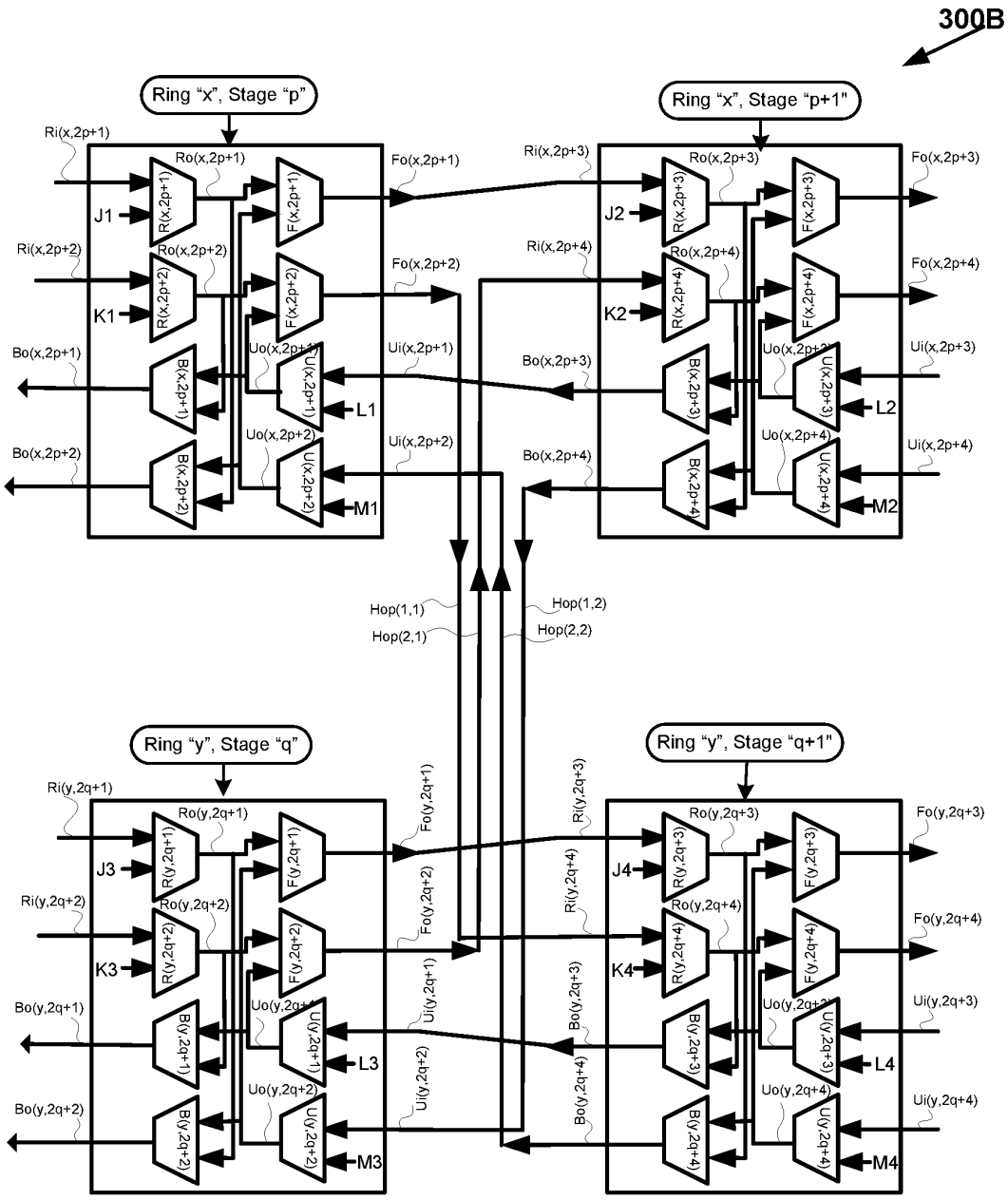

300B
Ring "x", Stage "p"
Ring "x", Stage "p+1"
Ring "y", Stage "q"
Ring "y", Stage "q+1"
J1
J2
J3
J4
K1
K2
K3
K4
L1
L2
L3
L4
M1
M2
M3
M4
Hop(1,1)
Hop(1,2)
Hop(2,1)
Hop(2,2)

FIG. 3C

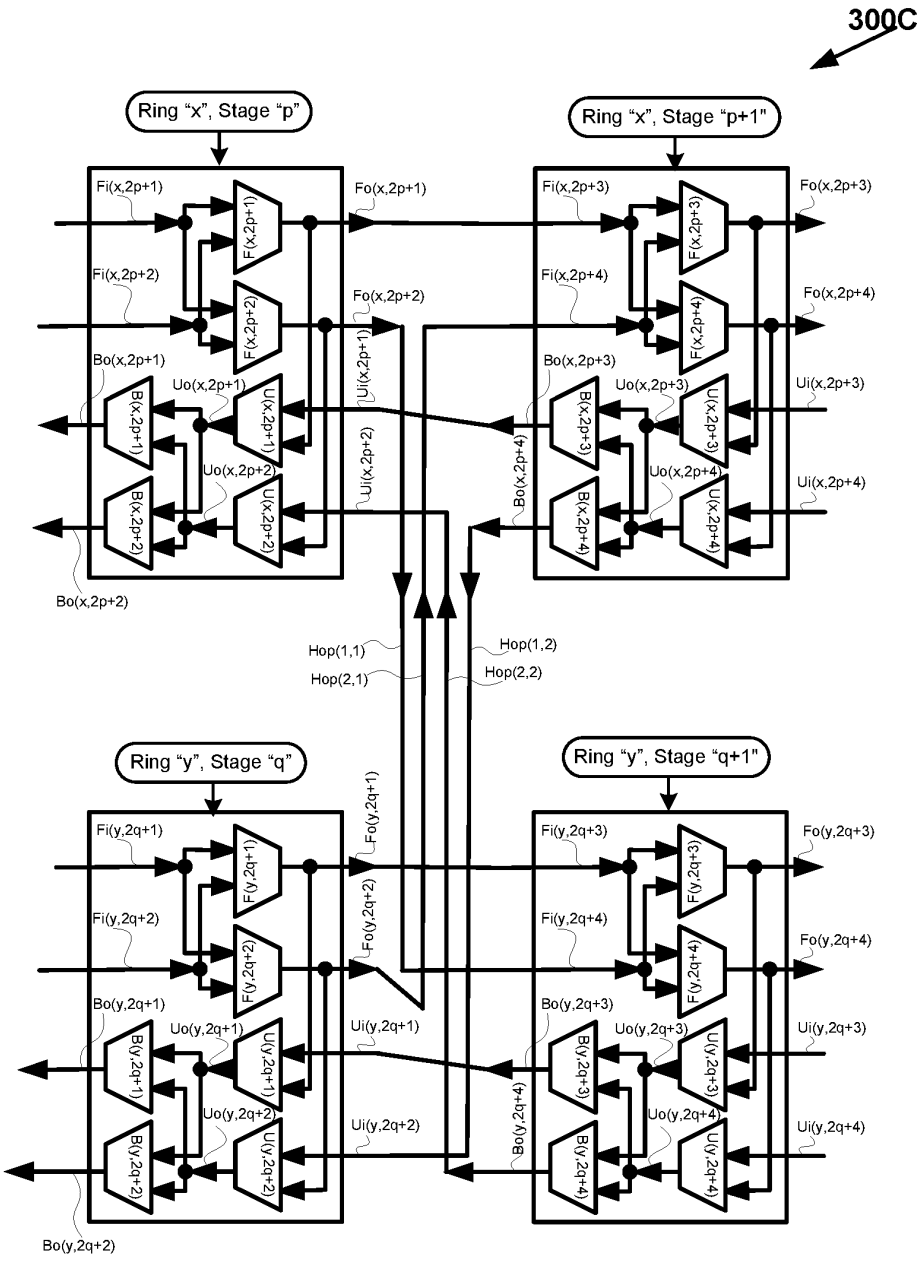

300C
Ring "x", Stage "p"
Ring "x", Stage "p+1"
Ring "y", Stage "q"
Ring "y", Stage "q+1"
Fi(x,2p+1)
Fi(x,2p+2)
Fi(x,2p+3)
Fi(x,2p+4)
Fo(x,2p+1)
Fo(x,2p+2)
Fo(x,2p+3)
Fo(x,2p+4)
F(x,2p+1)
F(x,2p+2)
F(x,2p+3)
F(x,2p+4)
Bo(x,2p+1)
Bo(x,2p+2)
Bo(x,2p+3)
Bo(x,2p+4)
B(x,2p+1)
B(x,2p+2)
B(x,2p+3)
B(x,2p+4)
Uo(x,2p+1)
Uo(x,2p+2)
Uo(x,2p+3)
Uo(x,2p+4)
U(x,2p+1)
U(x,2p+2)
U(x,2p+3)
U(x,2p+4)
Ui(x,2p+1)
Ui(x,2p+2)
Ui(x,2p+3)
Ui(x,2p+4)
Hop(1,1)
Hop(2,1)
Hop(1,2)
Hop(2,2)
Fi(y,2q+1)
Fi(y,2q+2)
Fi(y,2q+3)
Fi(y,2q+4)
Fo(y,2q+1)
Fo(y,2q+2)
Fo(y,2q+3)
Fo(y,2q+4)
F(y,2q+1)
F(y,2q+2)
F(y,2q+3)
F(y,2q+4)
Bo(y,2q+1)
Bo(y,2q+2)
Bo(y,2q+3)
Bo(y,2q+4)
B(y,2q+1)
B(y,2q+2)
B(y,2q+3)
B(y,2q+4)
Uo(y,2q+1)
Uo(y,2q+2)
Uo(y,2q+3)
Uo(y,2q+4)
U(y,2q+1)
U(y,2q+2)
U(y,2q+3)
U(y,2q+4)
Ui(y,2q+1)
Ui(y,2q+2)
Ui(y,2q+3)
Ui(y,2q+4)

FIG. 3D

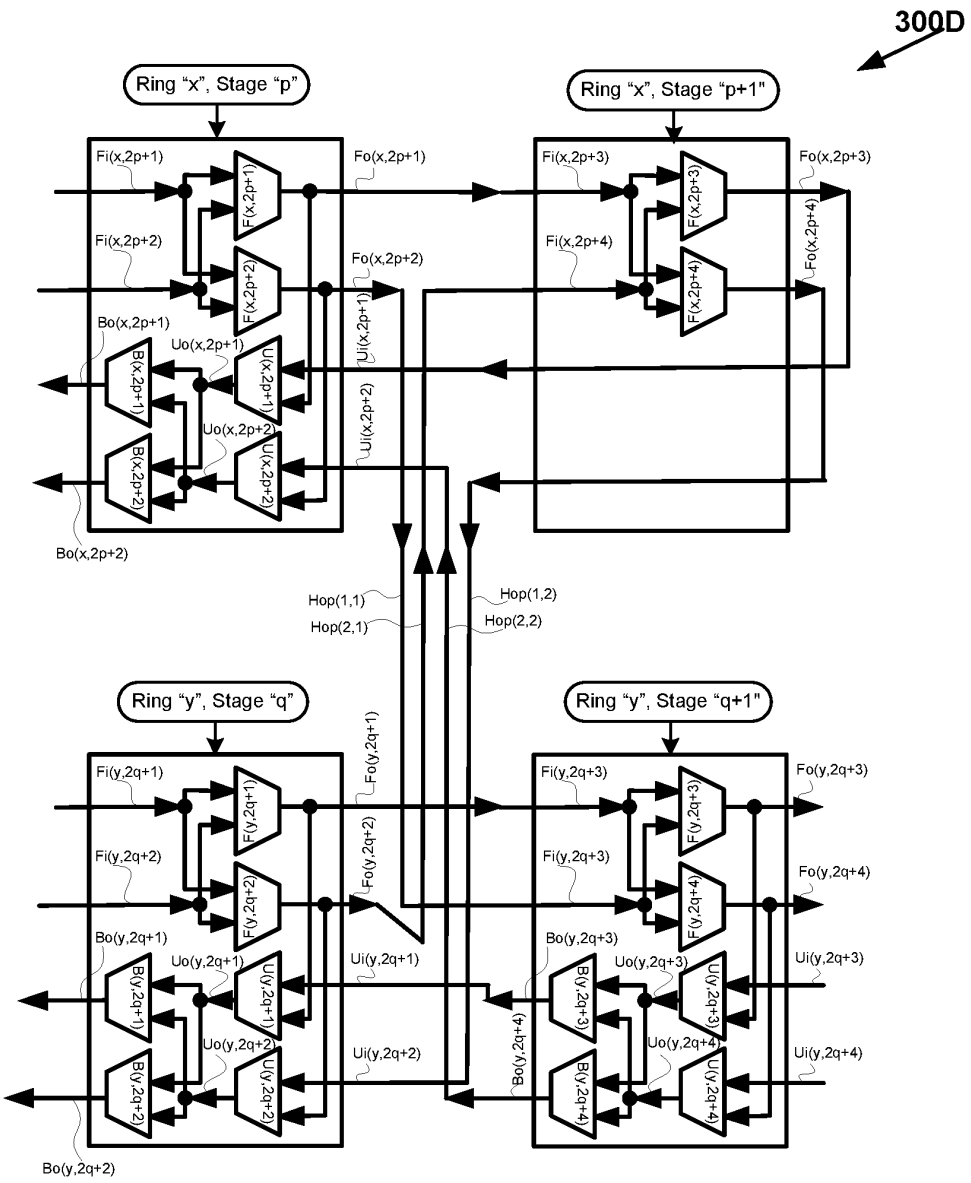

300D
Ring "x", Stage "p"
Ring "x", Stage "p+1"
Ring "y", Stage "q"
Ring "y", Stage "q+1"
Fi(x,2p+1)
Fi(x,2p+2)
Fi(x,2p+3)
Fi(x,2p+4)
Fo(x,2p+1)
Fo(x,2p+2)
Fo(x,2p+3)
Fo(x,2p+4)
F(x,2p+1)
F(x,2p+2)
F(x,2p+3)
F(x,2p+4)
Bo(x,2p+1)
Bo(x,2p+2)
Uo(x,2p+1)
Uo(x,2p+2)
B(x,2p+1)
B(x,2p+2)
U(x,2p+1)
U(x,2p+2)
Ui(x,2p+1)
Ui(x,2p+2)
Hop(1,1)
Hop(1,2)
Hop(2,1)
Hop(2,2)
Fi(y,2q+1)
Fi(y,2q+2)
Fi(y,2q+3)
Fi(y,2q+4)
Fo(y,2q+1)
Fo(y,2q+2)
Fo(y,2q+3)
Fo(y,2q+4)
F(y,2q+1)
F(y,2q+2)
F(y,2q+3)
F(y,2q+4)
Bo(y,2q+1)
Bo(y,2q+2)
Bo(y,2q+3)
Bo(y,2q+4)
Uo(y,2q+1)
Uo(y,2q+2)
Uo(y,2q+3)
Uo(y,2q+4)
B(y,2q+1)
B(y,2q+2)
B(y,2q+3)
B(y,2q+4)
U(y,2q+1)
U(y,2q+2)
U(y,2q+3)
U(y,2q+4)
Ui(y,2q+1)
Ui(y,2q+2)
Ui(y,2q+3)
Ui(y,2q+4)

FIG. 3E

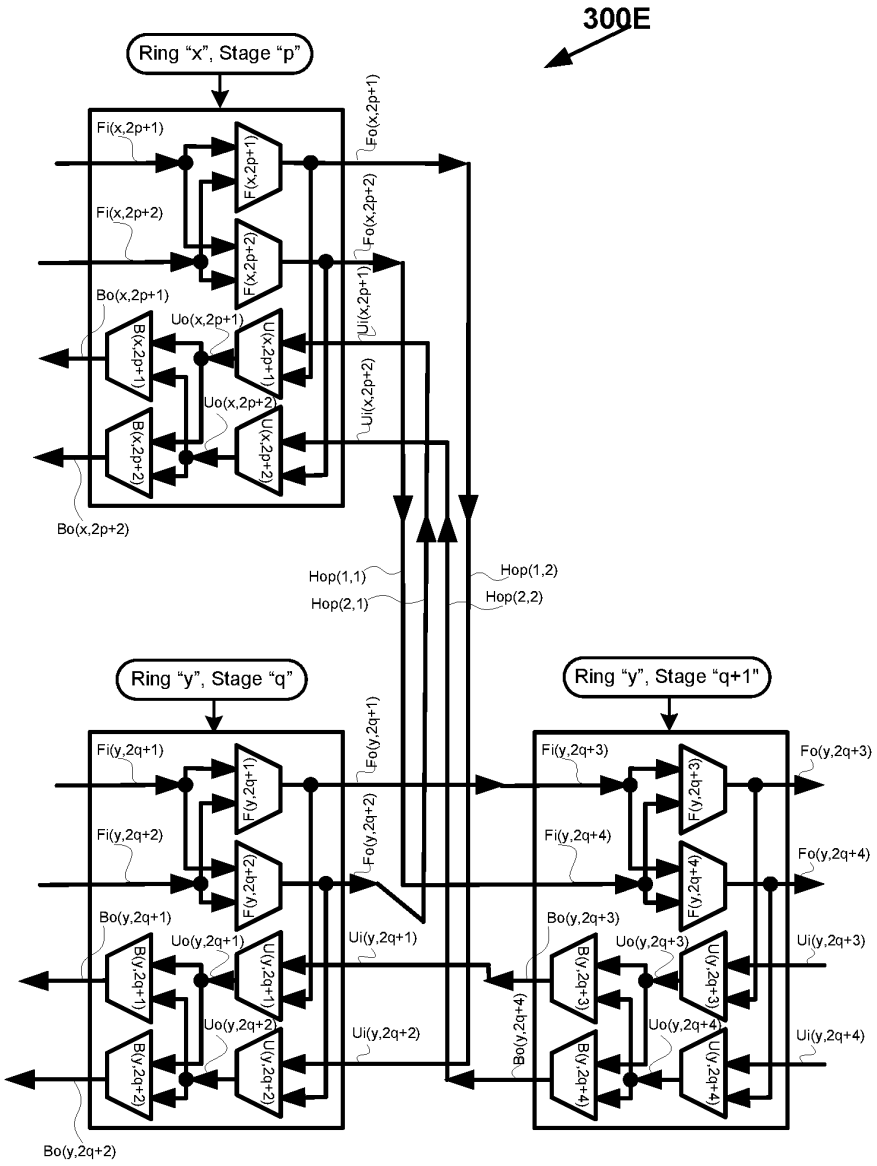

300E
Ring "x", Stage "p"
Fi(x,2p+1)
Fi(x,2p+2)
Bo(x,2p+1)
Bo(x,2p+2)
Uo(x,2p+1)
Uo(x,2p+2)
F(x,2p+1)
F(x,2p+2)
B(x,2p+1)
B(x,2p+2)
U(x,2p+1)
U(x,2p+2)
Fo(x,2p+1)
Fo(x,2p+2)
Ui(x,2p+1)
Ui(x,2p+2)
Hop(1,1)
Hop(2,1)
Hop(1,2)
Hop(2,2)
Ring "y", Stage "q"
Ring "y", Stage "q+1"
Fi(y,2q+1)
Fi(y,2q+2)
Fi(y,2q+3)
Fi(y,2q+4)
Bo(y,2q+1)
Bo(y,2q+2)
Bo(y,2q+3)
Bo(y,2q+4)
Uo(y,2q+1)
Uo(y,2q+2)
Uo(y,2q+3)
Uo(y,2q+4)
F(y,2q+1)
F(y,2q+2)
F(y,2q+3)
F(y,2q+4)
B(y,2q+1)
B(y,2q+2)
B(y,2q+3)
B(y,2q+4)
U(y,2q+1)
U(y,2q+2)
U(y,2q+3)
U(y,2q+4)
Fo(y,2q+1)
Fo(y,2q+2)
Fo(y,2q+3)
Fo(y,2q+4)
Ui(y,2q+1)
Ui(y,2q+2)
Ui(y,2q+3)
Ui(y,2q+4)

FIG. 4A

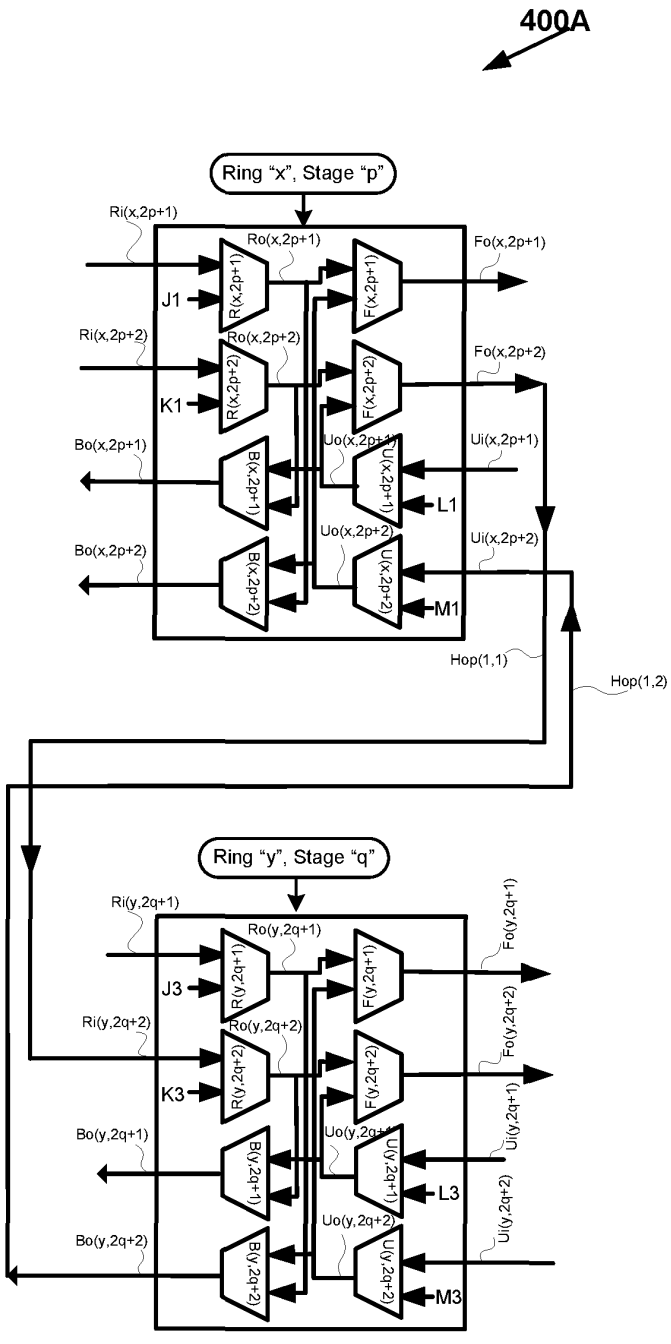

400A
Ring "x", Stage "p"
Ri(x,2p+1)
Ro(x,2p+1)
Fo(x,2p+1)
J1
R(x,2p+1)
F(x,2p+1)
Ri(x,2p+2)
Ro(x,2p+2)
Fo(x,2p+2)
K1
R(x,2p+2)
F(x,2p+2)
Bo(x,2p+1)
Uo(x,2p+1)
Ui(x,2p+1)
B(x,2p+1)
U(x,2p+1)
L1
Bo(x,2p+2)
Uo(x,2p+2)
Ui(x,2p+2)
B(x,2p+2)
U(x,2p+2)
M1
Hop(1,1)
Hop(1,2)
Ring "y", Stage "q"
Ri(y,2q+1)
Ro(y,2q+1)
Fo(y,2q+1)
J3
R(y,2q+1)
F(y,2q+1)
Ri(y,2q+2)
Ro(y,2q+2)
Fo(y,2q+2)
K3
R(y,2q+2)
F(y,2q+2)
Bo(y,2q+1)
Uo(y,2q+1)
Ui(y,2q+1)
B(y,2q+1)
U(y,2q+1)
L3
Bo(y,2q+2)
Uo(y,2q+2)
Ui(y,2q+2)
B(y,2q+2)
U(y,2q+2)
M3

FIG. 4B

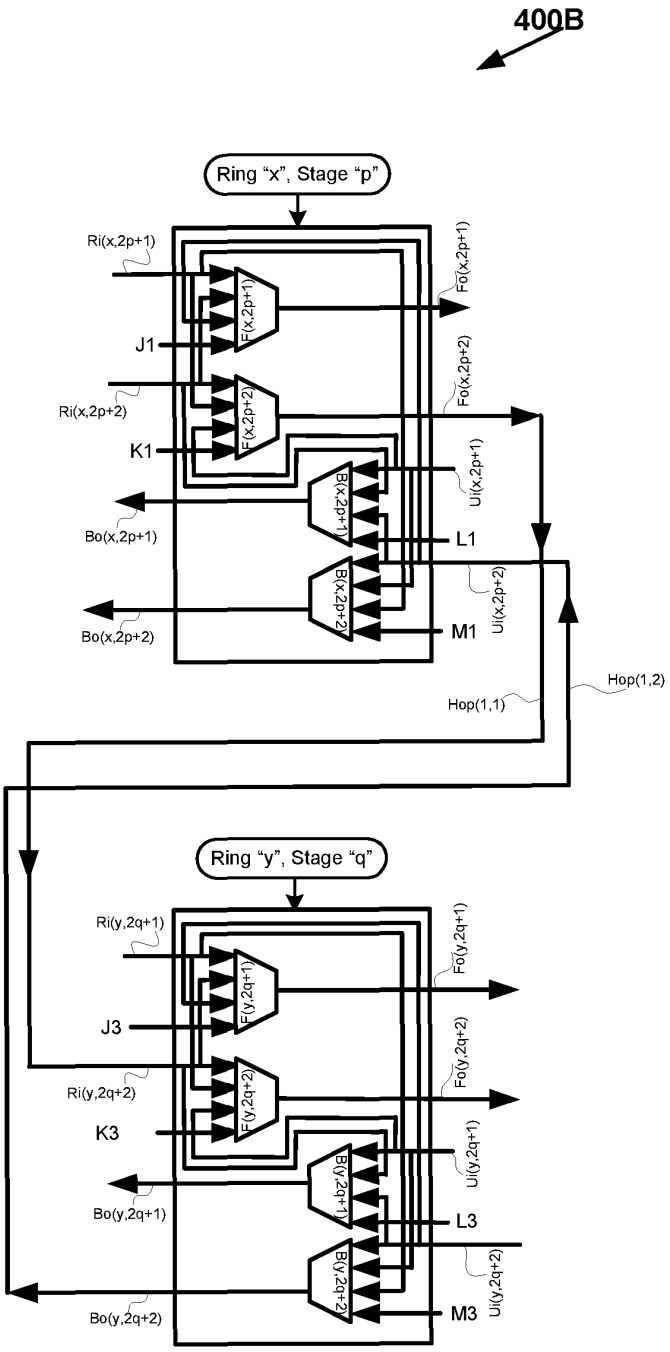

400B
Ring "x", Stage "p"
Ri(x,2p+1)
Fo(x,2p+1)
F(x,2p+1)
J1
Fo(x,2p+2)
Ri(x,2p+2)
F(x,2p+2)
K1
Bi(x,2p+1)
Ui(x,2p+1)
Bo(x,2p+1)
L1
Bi(x,2p+2)
Ui(x,2p+2)
Bo(x,2p+2)
M1
Hop(1,2)
Hop(1,1)
Ring "y", Stage "q"
Ri(y,2q+1)
Fo(y,2q+1)
F(y,2q+1)
J3
Fo(y,2q+2)
Ri(y,2q+2)
F(y,2q+2)
K3
Bi(y,2q+1)
Ui(y,2q+1)
Bo(y,2q+1)
L3
Bi(y,2q+2)
Ui(y,2q+2)
Bo(y,2q+2)
M3

FIG. 5A

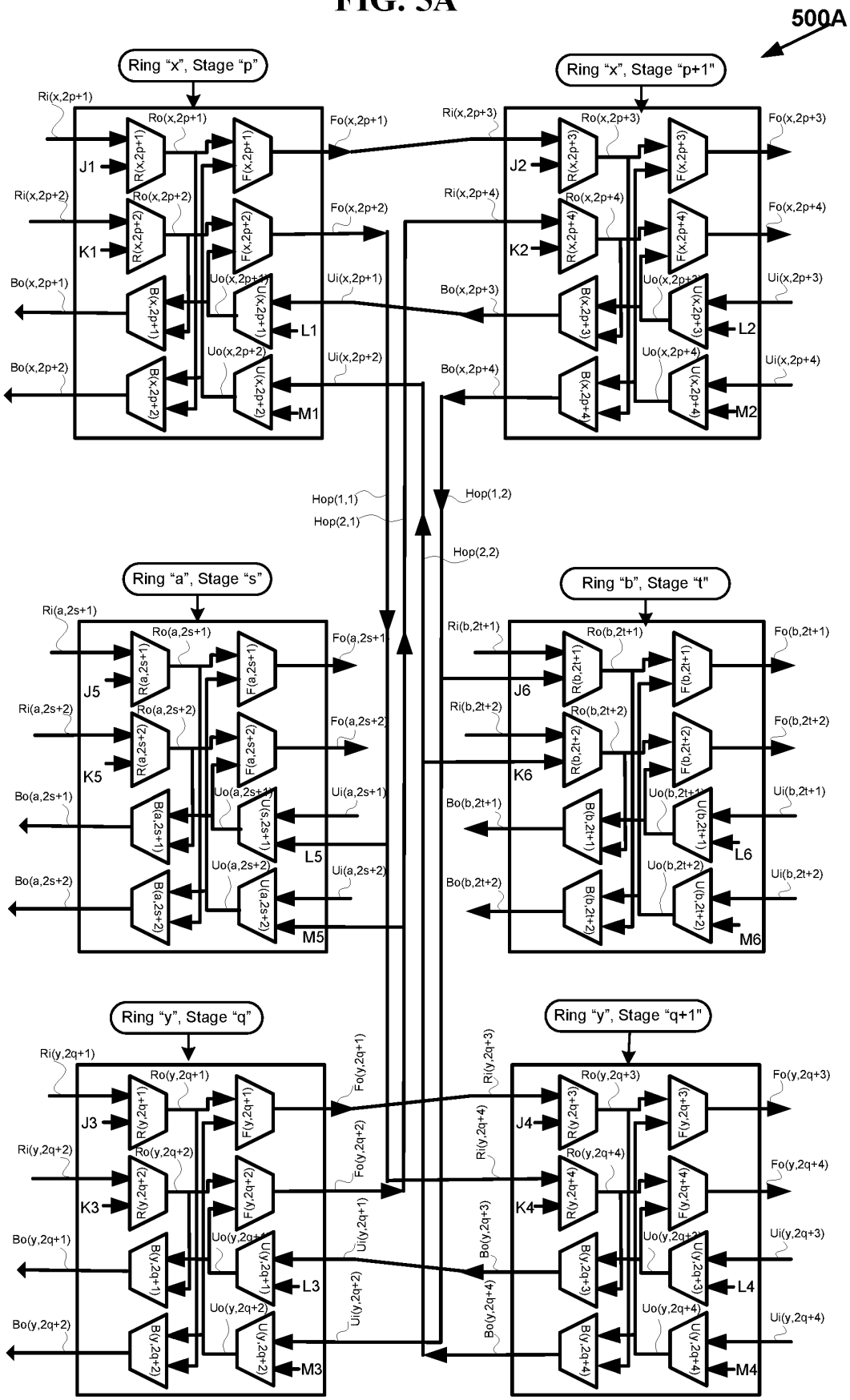

500A
Ring "x", Stage "p"
Ring "x", Stage "p+1"
Ring "a", Stage "s"
Ring "b", Stage "t"
Ring "y", Stage "q"
Ring "y", Stage "q+1"
Hop(1,1)
Hop(1,2)
Hop(2,1)
Hop(2,2)
J1
J2
J3
J4
J5
J6
K1
K2
K3
K4
K5
K6
L1
L2
L3
L4
L5
L6
M1
M2
M3
M4
M5
M6

FIG. 6A

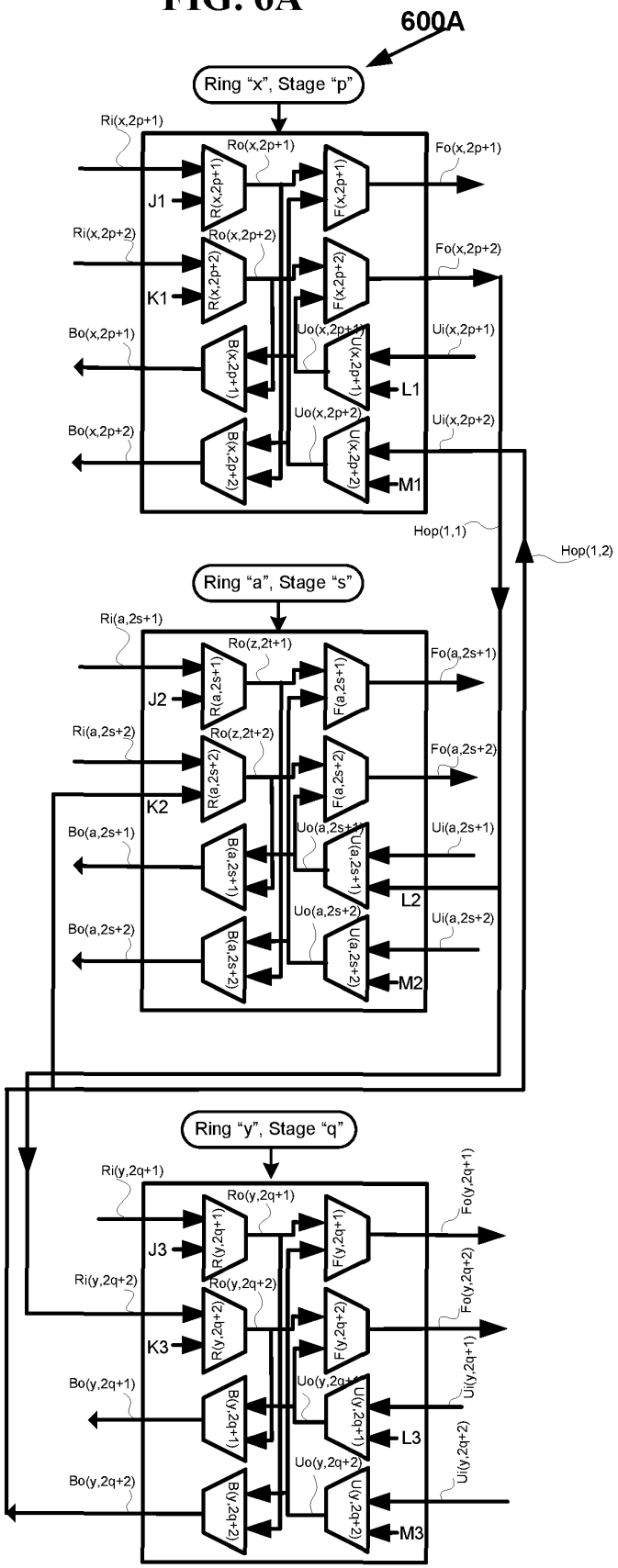

600A
Ring "x", Stage "p"
Ri(x,2p+1)
Ro(x,2p+1)
Fo(x,2p+1)
J1
R(x,2p+1)
F(x,2p+1)
Ri(x,2p+2)
Ro(x,2p+2)
Fo(x,2p+2)
K1
R(x,2p+2)
F(x,2p+2)
Bo(x,2p+1)
Uo(x,2p+1)
Ui(x,2p+1)
B(x,2p+1)
U(x,2p+1)
L1
Bo(x,2p+2)
Uo(x,2p+2)
Ui(x,2p+2)
B(x,2p+2)
U(x,2p+2)
M1
Hop(1,1)
Hop(1,2)
Ring "a", Stage "s"
Ri(a,2s+1)
Ro(z,2t+1)
Fo(a,2s+1)
J2
R(a,2s+1)
F(a,2s+1)
Ri(a,2s+2)
Ro(z,2t+2)
Fo(a,2s+2)
K2
R(a,2s+2)
F(a,2s+2)
Bo(a,2s+1)
Uo(a,2s+1)
Ui(a,2s+1)
B(a,2s+1)
U(a,2s+1)
L2
Bo(a,2s+2)
Uo(a,2s+2)
Ui(a,2s+2)
B(a,2s+2)
U(a,2s+2)
M2
Ring "y", Stage "q"
Ri(y,2q+1)
Ro(y,2q+1)
Fo(y,2q+1)
J3
R(y,2q+1)
F(y,2q+1)
Ri(y,2q+2)
Ro(y,2q+2)
Fo(y,2q+2)
K3
R(y,2q+2)
F(y,2q+2)
Bo(y,2q+1)
Uo(y,2q+1)
Ui(y,2q+1)
B(y,2q+1)
U(y,2q+1)
L3
Bo(y,2q+2)
Uo(y,2q+2)
Ui(y,2q+2)
B(y,2q+2)
U(y,2q+2)
M3

FIG. 6B

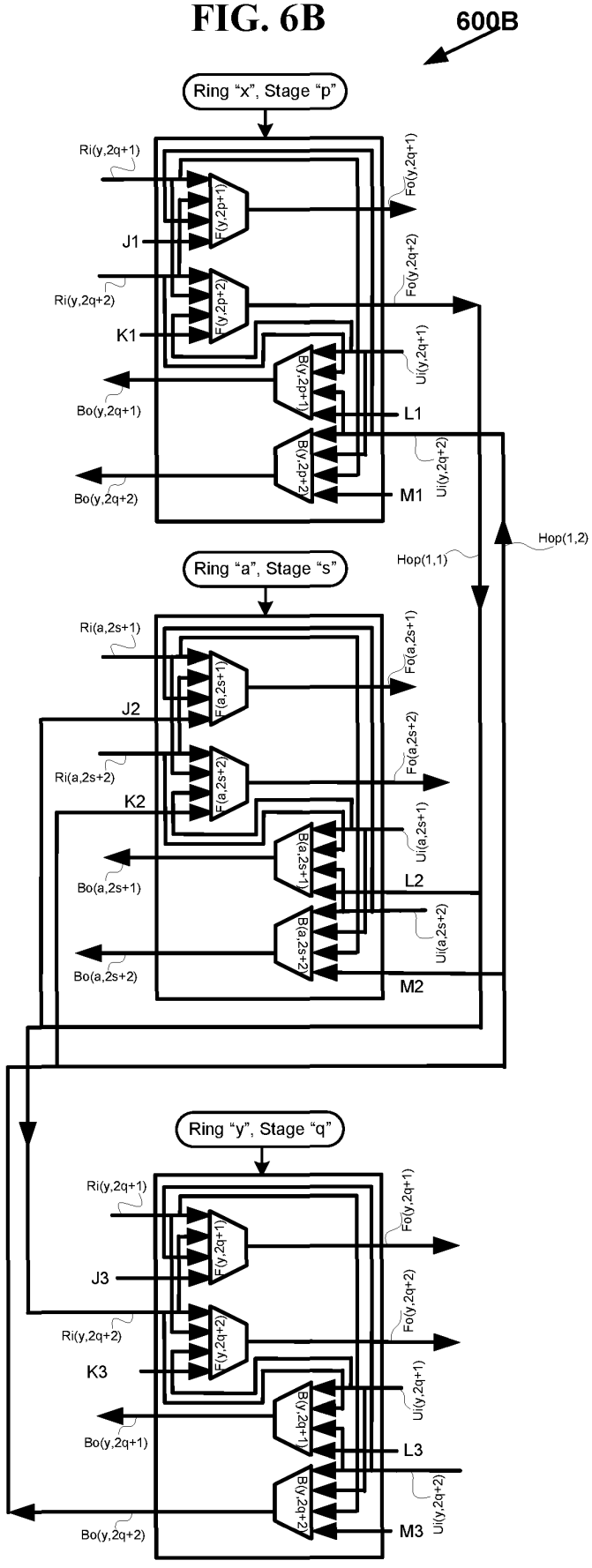

600B
Ring "x", Stage "p"
Ri(y,2q+1)
J1
Ri(y,2q+2)
K1
Bo(y,2q+1)
Bo(y,2q+2)
F(y,2p+1)
F(y,2p+2)
B(y,2p+1)
B(y,2p+2)
Fo(y,2q+1)
Fo(y,2q+2)
Ui(y,2q+1)
Ui(y,2q+2)
L1
M1
Hop(1,1)
Hop(1,2)
Ring "a", Stage "s"
Ri(a,2s+1)
J2
Ri(a,2s+2)
K2
Bo(a,2s+1)
Bo(a,2s+2)
F(a,2s+1)
F(a,2s+2)
B(a,2s+1)
B(a,2s+2)
Fo(a,2s+1)
Fo(a,2s+2)
Ui(a,2s+1)
Ui(a,2s+2)
L2
M2
Ring "y", Stage "q"
Ri(y,2q+1)
J3
Ri(y,2q+2)
K3
Bo(y,2q+1)
Bo(y,2q+2)
F(y,2q+1)
F(y,2q+2)
B(y,2q+1)
B(y,2q+2)
Fo(y,2q+1)
Fo(y,2q+2)
Ui(y,2q+1)
Ui(y,2q+2)
L3
M3

FIG. 7A

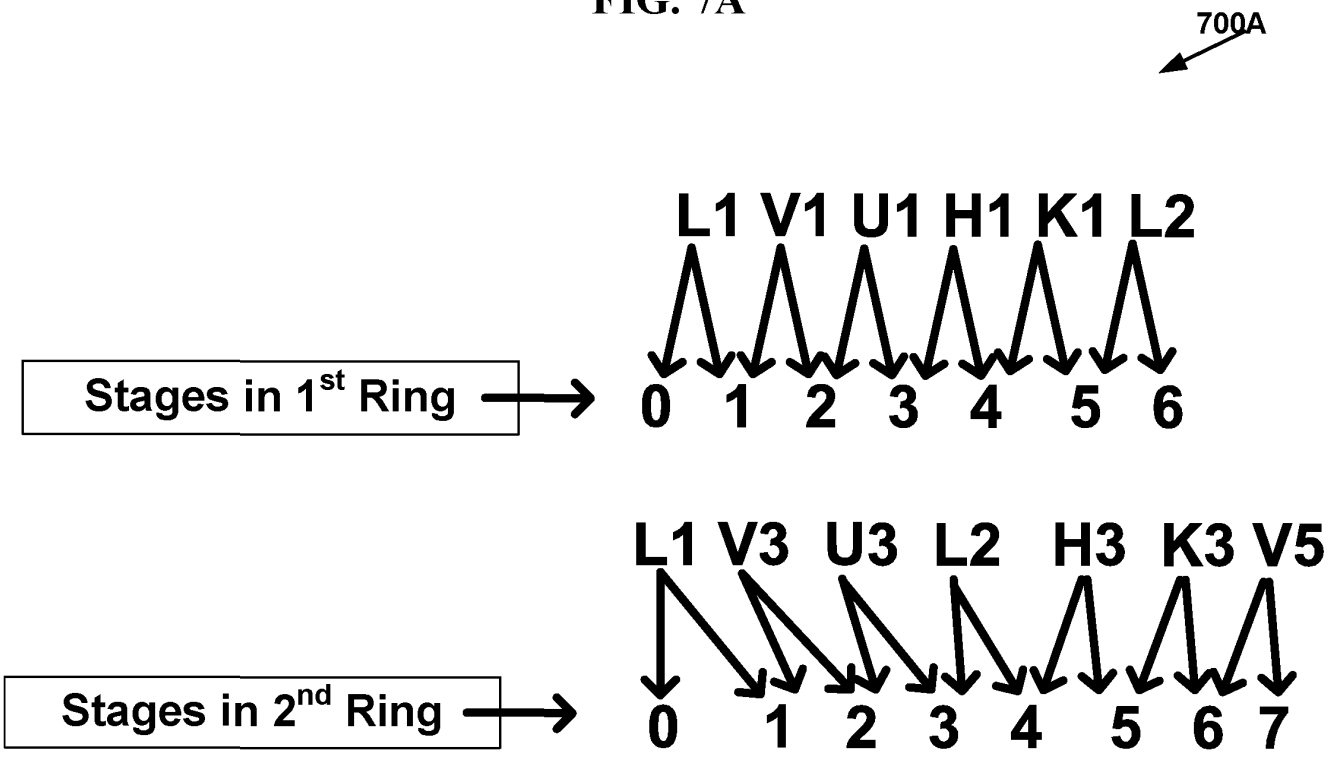

700A
L1 V1 U1 H1 K1 L2
Stages in 1st Ring
0 1 2 3 4 5 6
L1 V3 U3 L2 H3 K3 V5
Stages in 2nd Ring
0 1 2 3 4 5 6 7

FIG. 8

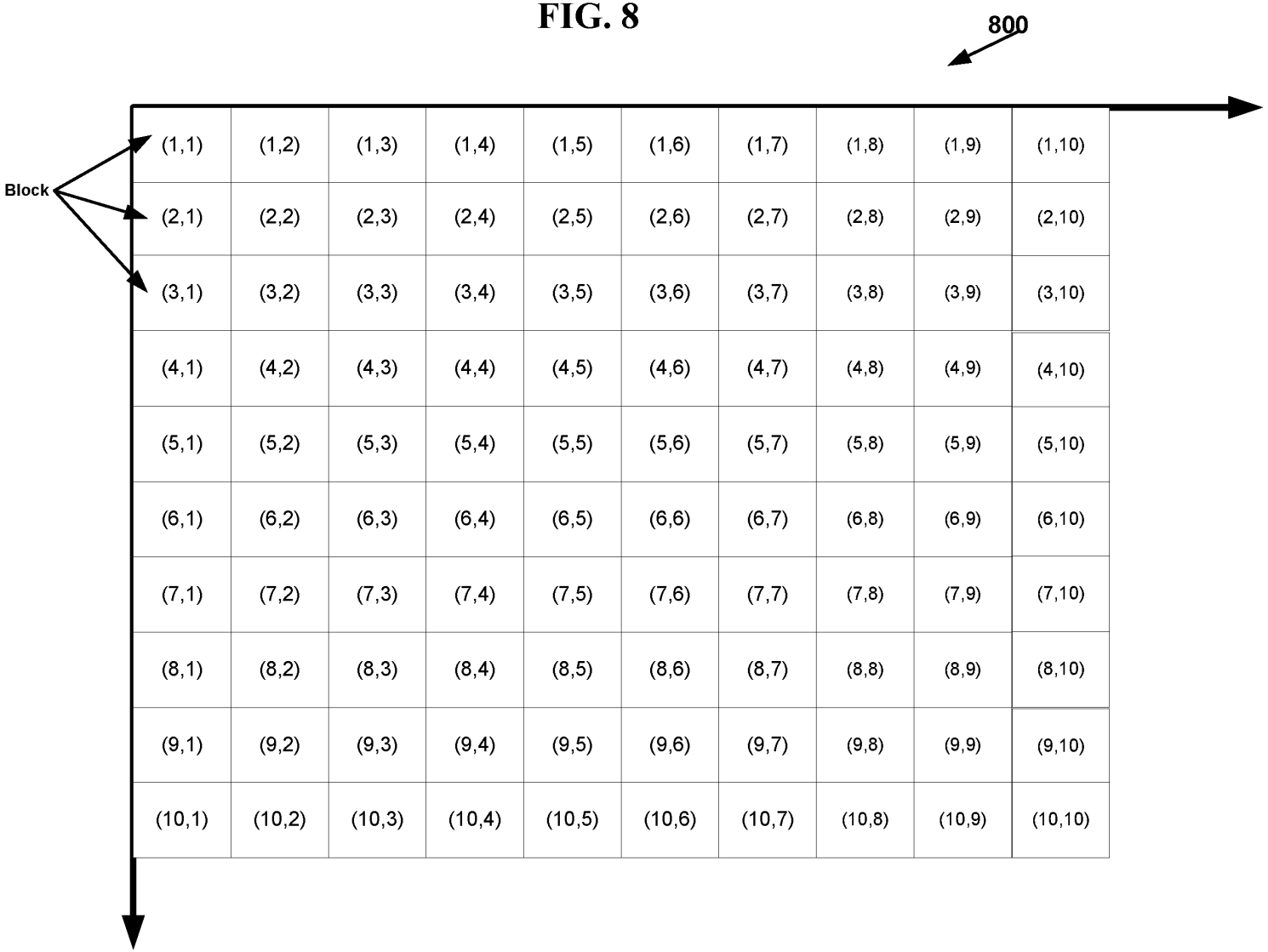

800
Block
(1,1) (1,2) (1,3) (1,4) (1,5) (1,6) (1,7) (1,8) (1,9) (1,10)
(2,1) (2,2) (2,3) (2,4) (2,5) (2,6) (2,7) (2,8) (2,9) (2,10)
(3,1) (3,2) (3,3) (3,4) (3,5) (3,6) (3,7) (3,8) (3,9) (3,10)
(4,1) (4,2) (4,3) (4,4) (4,5) (4,6) (4,7) (4,8) (4,9) (4,10)
(5,1) (5,2) (5,3) (5,4) (5,5) (5,6) (5,7) (5,8) (5,9) (5,10)
(6,1) (6,2) (6,3) (6,4) (6,5) (6,6) (6,7) (6,8) (6,9) (6,10)
(7,1) (7,2) (7,3) (7,4) (7,5) (7,6) (7,7) (7,8) (7,9) (7,10)
(8,1) (8,2) (8,3) (8,4) (8,5) (8,6) (8,7) (8,8) (8,9) (8,10)
(9,1) (9,2) (9,3) (9,4) (9,5) (9,6) (9,7) (9,8) (9,9) (9,10)
(10,1) (10,2) (10,3) (10,4) (10,5) (10,6) (10,7) (10,8) (10,9) (10,10)

FIG. 9A

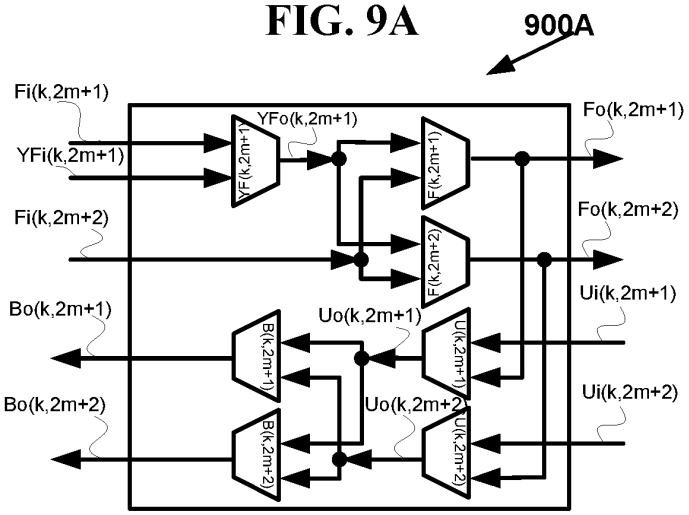


FIG. 9B

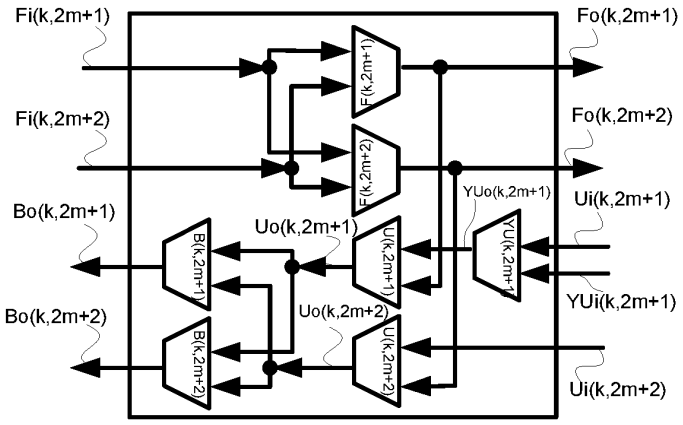


FIG. 9C

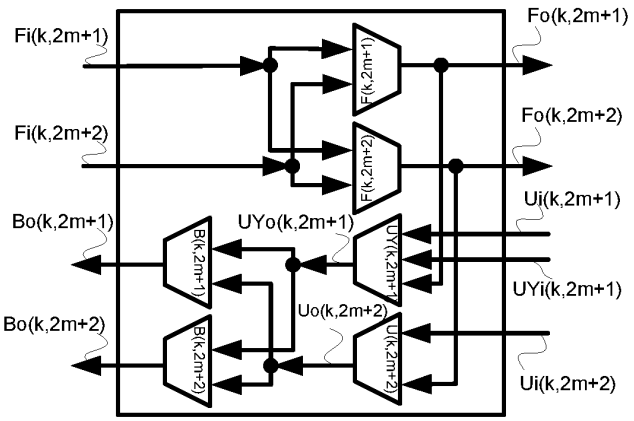


FIG. 9D

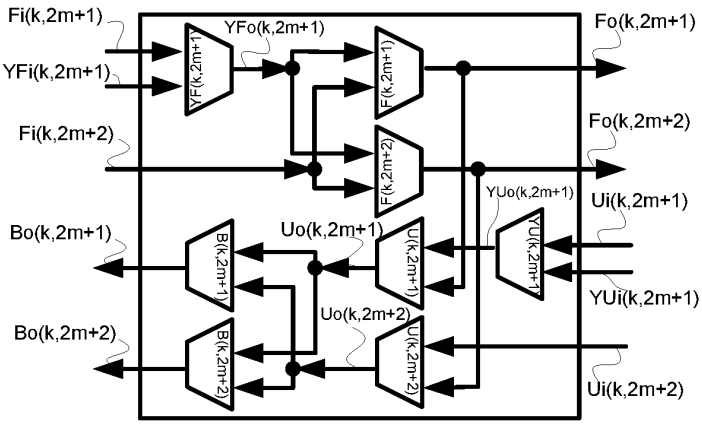


FIG. 9E

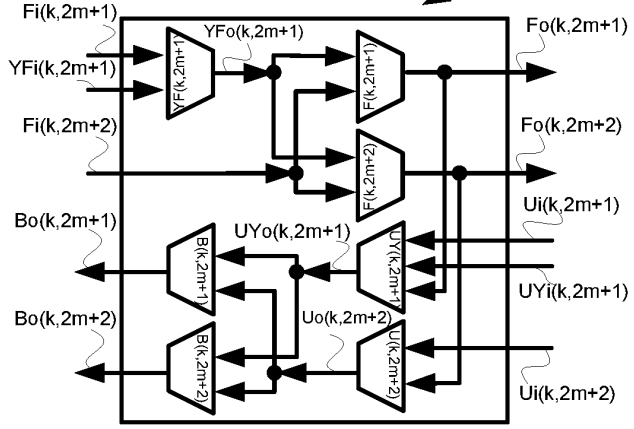


FIG. 10A 1000A

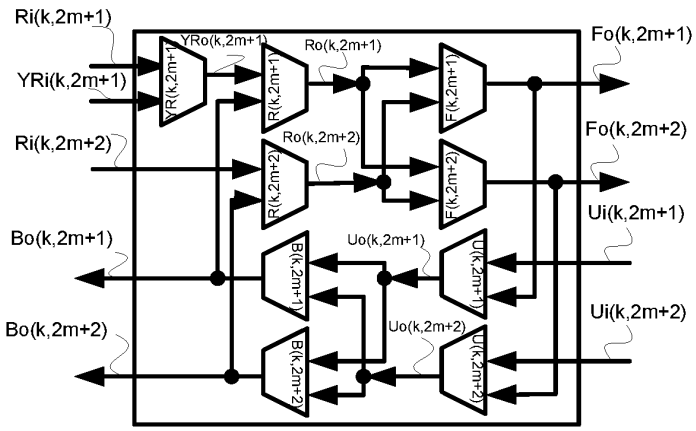


FIG. 10B 1000B

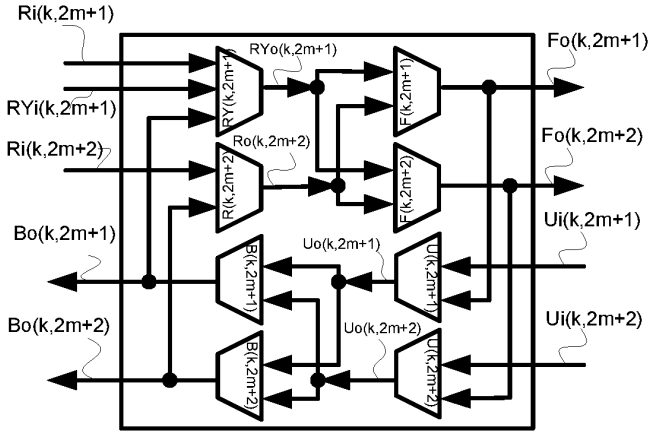


FIG. 10C 1000C

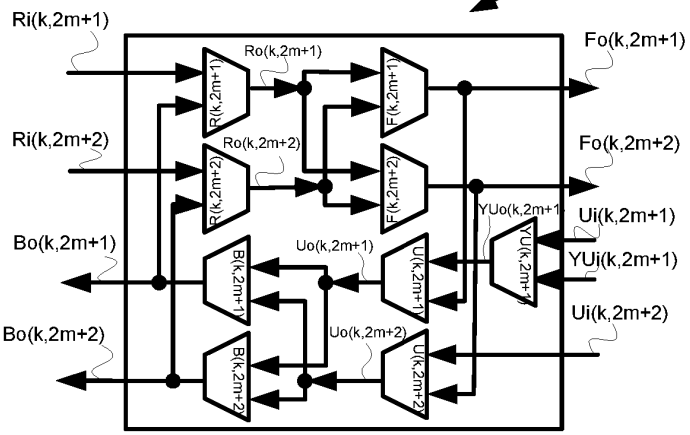


FIG. 10D 1000D

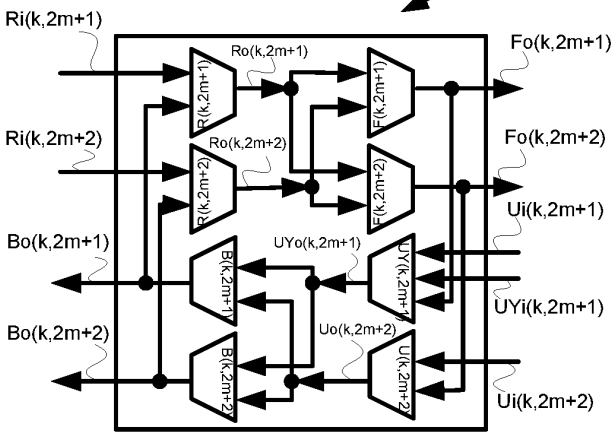


FIG. 10E 1000E

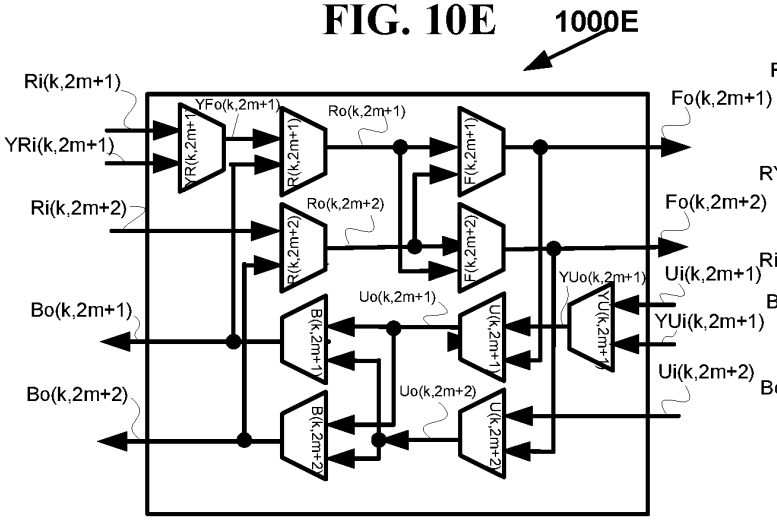


FIG. 10F 1000F

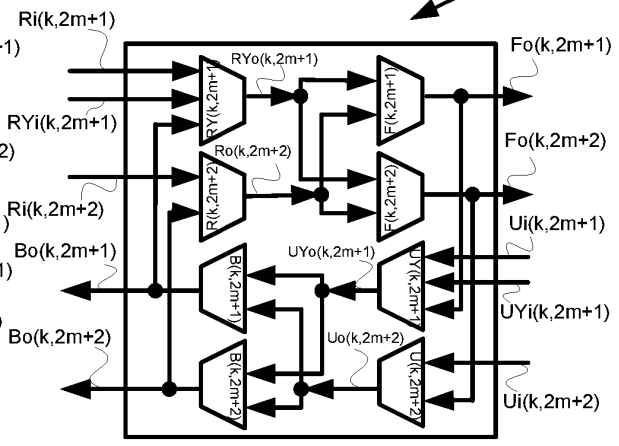


FIG. 11A

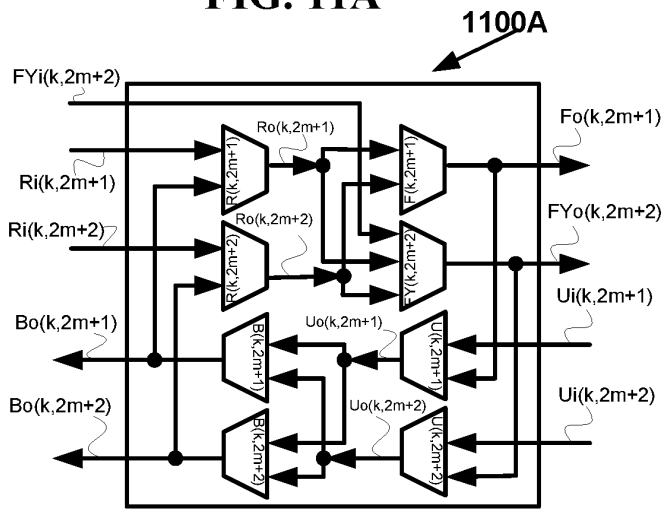


FIG. 11B

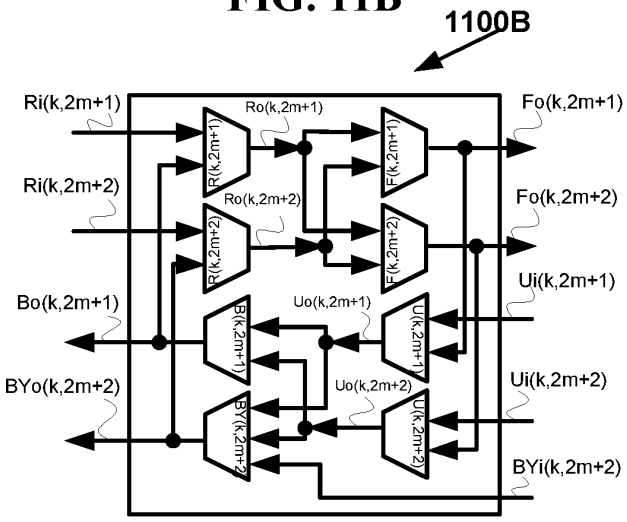


FIG. 11C

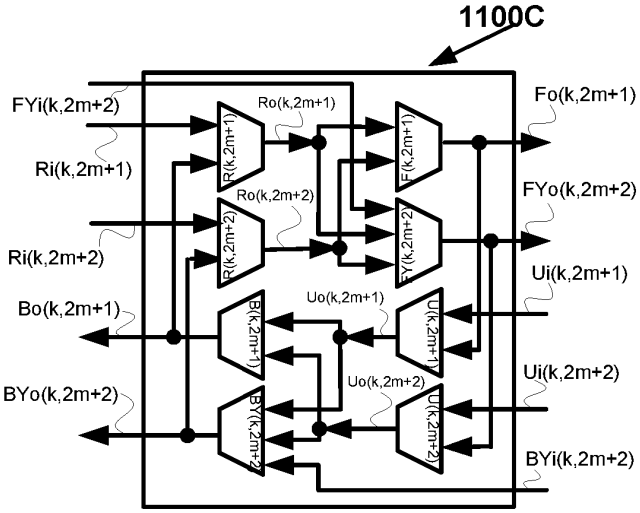


FIG. 12

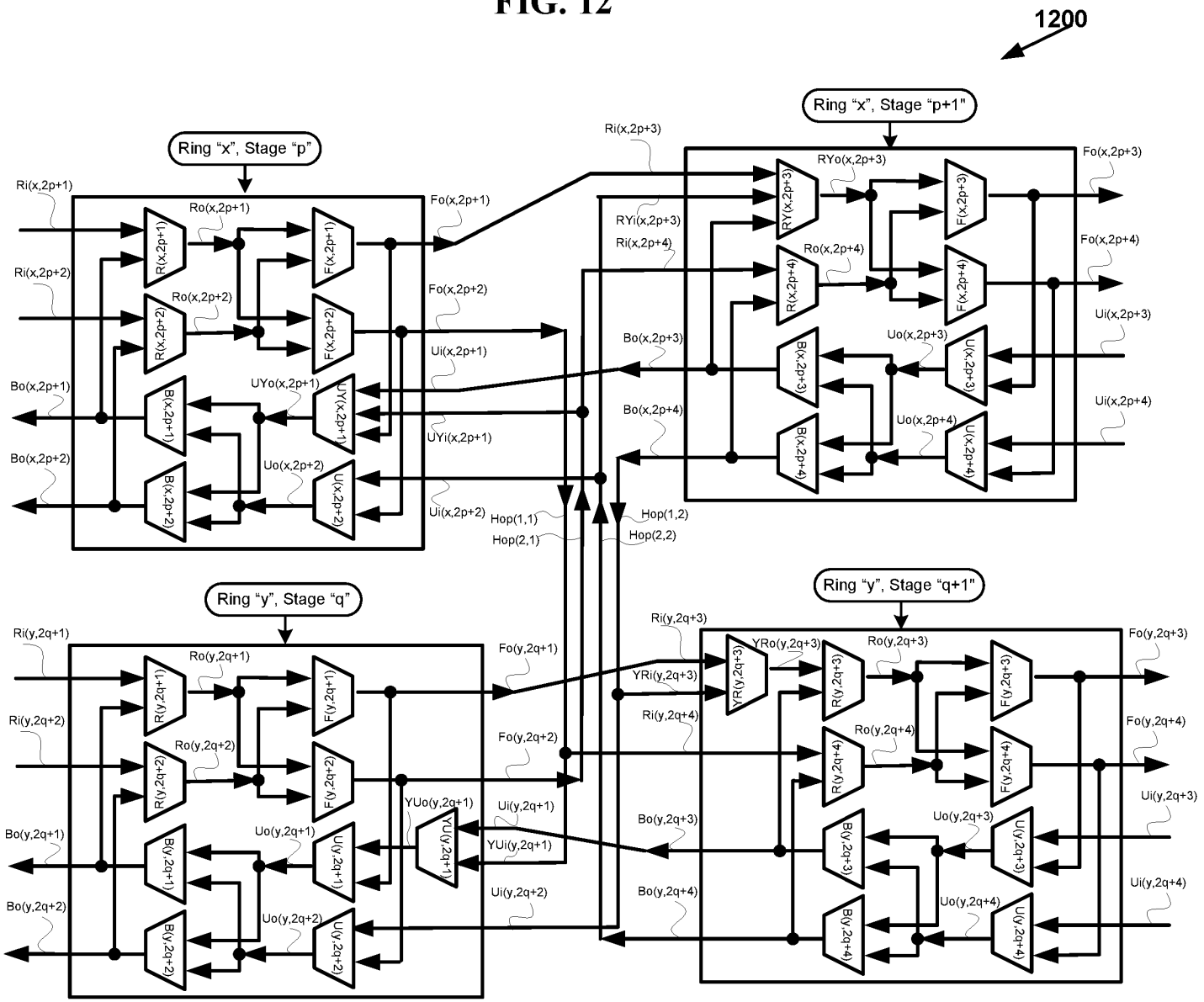

1200
Ring "x", Stage "p"
Ring "x", Stage "p+1"
Ring "y", Stage "q"
Ring "y", Stage "q+1"
Ri(x,2p+1)
Ri(x,2p+2)
Ri(x,2p+3)
Ri(x,2p+4)
Ro(x,2p+1)
Ro(x,2p+2)
Ro(x,2p+3)
Ro(x,2p+4)
Fo(x,2p+1)
Fo(x,2p+2)
Fo(x,2p+3)
Fo(x,2p+4)
Bo(x,2p+1)
Bo(x,2p+2)
Bo(x,2p+3)
Bo(x,2p+4)
UYo(x,2p+1)
Uo(x,2p+2)
Uo(x,2p+3)
Uo(x,2p+4)
Ui(x,2p+1)
Ui(x,2p+2)
Ui(x,2p+3)
Ui(x,2p+4)
UYi(x,2p+1)
RYo(x,2p+3)
RYi(x,2p+3)
Hop(1,1)
Hop(2,1)
Hop(1,2)
Hop(2,2)
Ri(y,2q+1)
Ri(y,2q+2)
Ri(y,2q+3)
Ri(y,2q+4)
Ro(y,2q+1)
Ro(y,2q+2)
Ro(y,2q+3)
Ro(y,2q+4)
Fo(y,2q+1)
Fo(y,2q+2)
Fo(y,2q+3)
Fo(y,2q+4)
Bo(y,2q+1)
Bo(y,2q+2)
Bo(y,2q+3)
Bo(y,2q+4)
YUo(y,2q+1)
Uo(y,2q+1)
Uo(y,2q+2)
Uo(y,2q+3)
Uo(y,2q+4)
Ui(y,2q+1)
Ui(y,2q+2)
Ui(y,2q+3)
Ui(y,2q+4)
YUi(y,2q+1)
YRo(y,2q+3)
YRi(y,2q+3)

FIG. 13

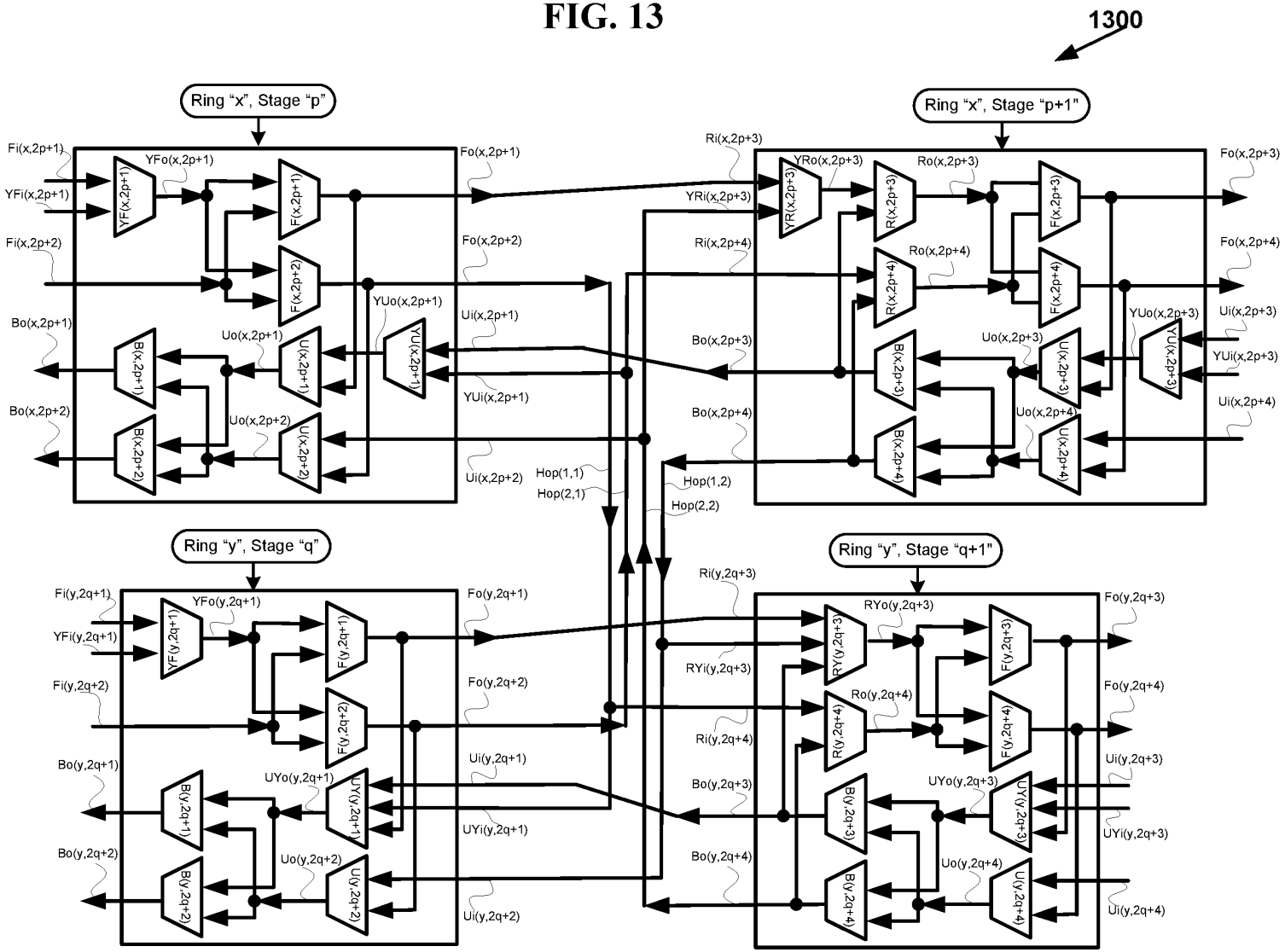

1300
Ring "x", Stage "p"
Ring "x", Stage "p+1"
Ring "y", Stage "q"
Ring "y", Stage "q+1"
Fi(x,2p+1)
YFi(x,2p+1)
Fi(x,2p+2)
Bo(x,2p+1)
Bo(x,2p+2)
YFo(x,2p+1)
YF(x,2p+1)
F(x,2p+1)
F(x,2p+2)
B(x,2p+1)
B(x,2p+2)
U(x,2p+1)
U(x,2p+2)
YU(x,2p+1)
Fo(x,2p+1)
Fo(x,2p+2)
YUo(x,2p+1)
Uo(x,2p+1)
Uo(x,2p+2)
Ui(x,2p+1)
YUi(x,2p+1)
Ui(x,2p+2)
Ri(x,2p+3)
YRi(x,2p+3)
Ri(x,2p+4)
Bo(x,2p+3)
Bo(x,2p+4)
YRo(x,2p+3)
YR(x,2p+3)
Ro(x,2p+3)
R(x,2p+3)
Ro(x,2p+4)
R(x,2p+4)
F(x,2p+3)
F(x,2p+4)
B(x,2p+3)
B(x,2p+4)
U(x,2p+3)
U(x,2p+4)
YU(x,2p+3)
Fo(x,2p+3)
Fo(x,2p+4)
YUo(x,2p+3)
Uo(x,2p+3)
Uo(x,2p+4)
Ui(x,2p+3)
YUi(x,2p+3)
Ui(x,2p+4)
Hop(1,1)
Hop(2,1)
Hop(1,2)
Hop(2,2)
Fi(y,2q+1)
YFi(y,2q+1)
Fi(y,2q+2)
Bo(y,2q+1)
Bo(y,2q+2)
YFo(y,2q+1)
YF(y,2q+1)
F(y,2q+1)
F(y,2q+2)
B(y,2q+1)
B(y,2q+2)
U(y,2q+1)
U(y,2q+2)
UY(y,2q+1)
Fo(y,2q+1)
Fo(y,2q+2)
UYo(y,2q+1)
Uo(y,2q+2)
Ui(y,2q+1)
UYi(y,2q+1)
Ui(y,2q+2)
Ri(y,2q+3)
RYi(y,2q+3)
Ri(y,2q+4)
Bo(y,2q+3)
Bo(y,2q+4)
RYo(y,2q+3)
RY(y,2q+3)
Ro(y,2q+4)
R(y,2q+4)
F(y,2q+3)
F(y,2q+4)
B(y,2q+3)
B(y,2q+4)
U(y,2q+3)
U(y,2q+4)
UY(y,2q+3)
Fo(y,2q+3)
Fo(y,2q+4)
UYo(y,2q+3)
Uo(y,2q+4)
Ui(y,2q+3)
UYi(y,2q+3)
Ui(y,2q+4)

FIG. 14

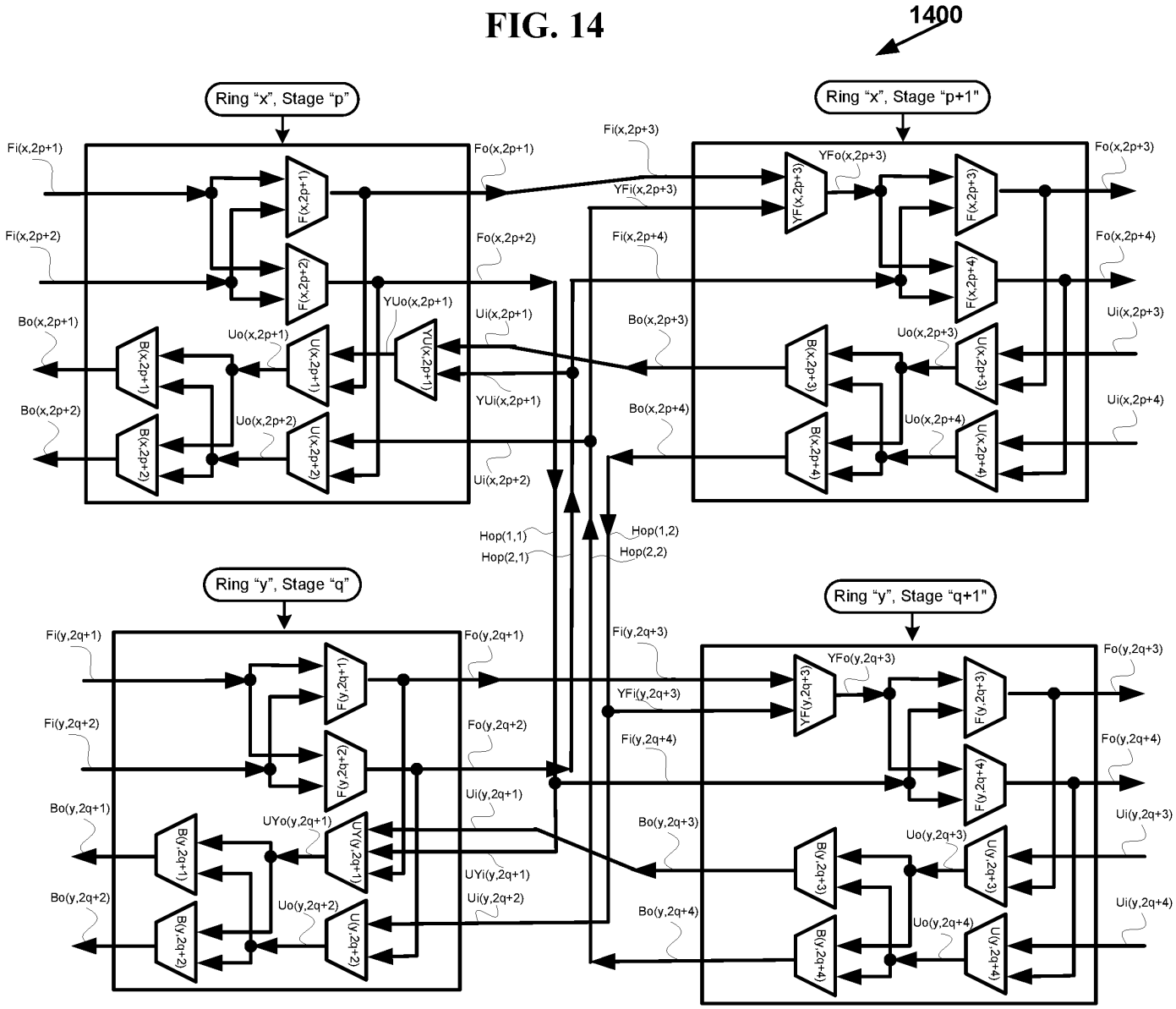
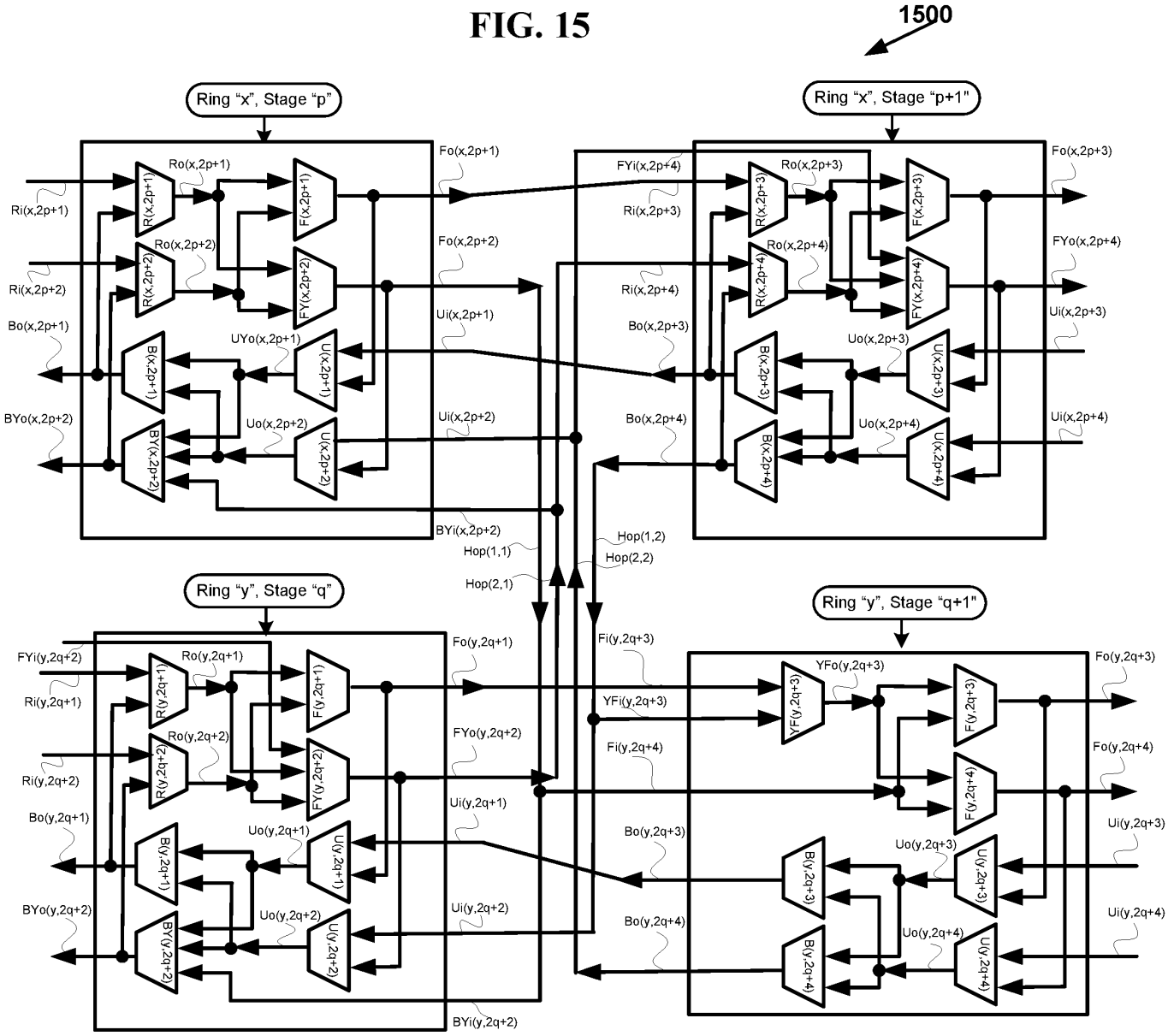

1400
Ring "x", Stage "p"
Ring "x", Stage "p+1"
Ring "y", Stage "q"
Ring "y", Stage "q+1"
Fi(x,2p+1)
Fi(x,2p+2)
Fo(x,2p+1)
Fo(x,2p+2)
Bo(x,2p+1)
Bo(x,2p+2)
Uo(x,2p+1)
Uo(x,2p+2)
YUo(x,2p+1)
Ui(x,2p+1)
YUi(x,2p+1)
Ui(x,2p+2)
F(x,2p+1)
F(x,2p+2)
B(x,2p+1)
B(x,2p+2)
U(x,2p+1)
U(x,2p+2)
YU(x,2p+1)
Fi(x,2p+3)
Fi(x,2p+4)
Fo(x,2p+3)
Fo(x,2p+4)
YFi(x,2p+3)
YFo(x,2p+3)
Bo(x,2p+3)
Bo(x,2p+4)
Uo(x,2p+3)
Uo(x,2p+4)
Ui(x,2p+3)
Ui(x,2p+4)
YF(x,2p+3)
F(x,2p+3)
F(x,2p+4)
B(x,2p+3)
B(x,2p+4)
U(x,2p+3)
U(x,2p+4)
Hop(1,1)
Hop(2,1)
Hop(1,2)
Hop(2,2)
Fi(y,2q+1)
Fi(y,2q+2)
Fo(y,2q+1)
Fo(y,2q+2)
Bo(y,2q+1)
Bo(y,2q+2)
UYo(y,2q+1)
Uo(y,2q+2)
Ui(y,2q+1)
UYi(y,2q+1)
Ui(y,2q+2)
F(y,2q+1)
F(y,2q+2)
B(y,2q+1)
B(y,2q+2)
UY(y,2q+1)
U(y,2q+2)
Fi(y,2q+3)
Fi(y,2q+4)
Fo(y,2q+3)
Fo(y,2q+4)
YFi(y,2q+3)
YFo(y,2q+3)
Bo(y,2q+3)
Bo(y,2q+4)
Uo(y,2q+3)
Uo(y,2q+4)
Ui(y,2q+3)
Ui(y,2q+4)
YF(y,2q+3)
F(y,2q+3)
F(y,2q+4)
B(y,2q+3)
B(y,2q+4)
U(y,2q+3)
U(y,2q+4)

FIG. 15


1500
Ring "x", Stage "p"
Ring "x", Stage "p+1"
Ring "y", Stage "q"
Ring "y", Stage "q+1"
Ri(x,2p+1)
Ri(x,2p+2)
Bo(x,2p+1)
BYo(x,2p+2)
Ro(x,2p+1)
Ro(x,2p+2)
Fo(x,2p+1)
Fo(x,2p+2)
Ui(x,2p+1)
Ui(x,2p+2)
UYo(x,2p+1)
Uo(x,2p+2)
BYi(x,2p+2)
FYi(x,2p+4)
Ri(x,2p+3)
Ri(x,2p+4)
Bo(x,2p+3)
Bo(x,2p+4)
Ro(x,2p+3)
Ro(x,2p+4)
Fo(x,2p+3)
FYo(x,2p+4)
Ui(x,2p+3)
Ui(x,2p+4)
Uo(x,2p+3)
Uo(x,2p+4)
Hop(1,1)
Hop(2,1)
Hop(1,2)
Hop(2,2)
FYi(y,2q+2)
Ri(y,2q+1)
Ri(y,2q+2)
Bo(y,2q+1)
BYo(y,2q+2)
Ro(y,2q+1)
Ro(y,2q+2)
Fo(y,2q+1)
FYo(y,2q+2)
Ui(y,2q+1)
Ui(y,2q+2)
Uo(y,2q+1)
Uo(y,2q+2)
BYi(y,2q+2)
Fi(y,2q+3)
YFi(y,2q+3)
Fi(y,2q+4)
Bo(y,2q+3)
Bo(y,2q+4)
YFo(y,2q+3)
Fo(y,2q+3)
Fo(y,2q+4)
Ui(y,2q+3)
Ui(y,2q+4)
Uo(y,2q+3)
Uo(y,2q+4)

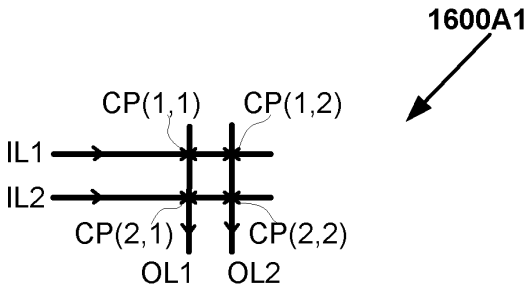


FIG. 16A1
(Prior Art)

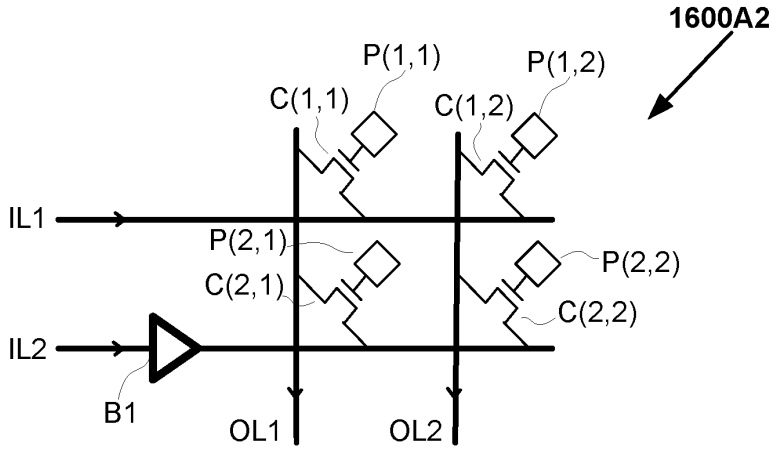


FIG. 16A2
(Prior Art)

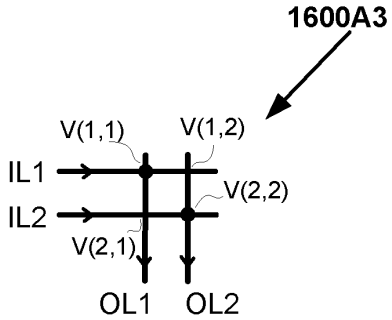


FIG. 16A3
(Prior Art)

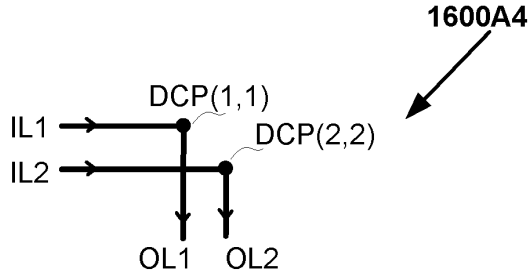


FIG. 16A4
(Prior Art)

FIG. 17

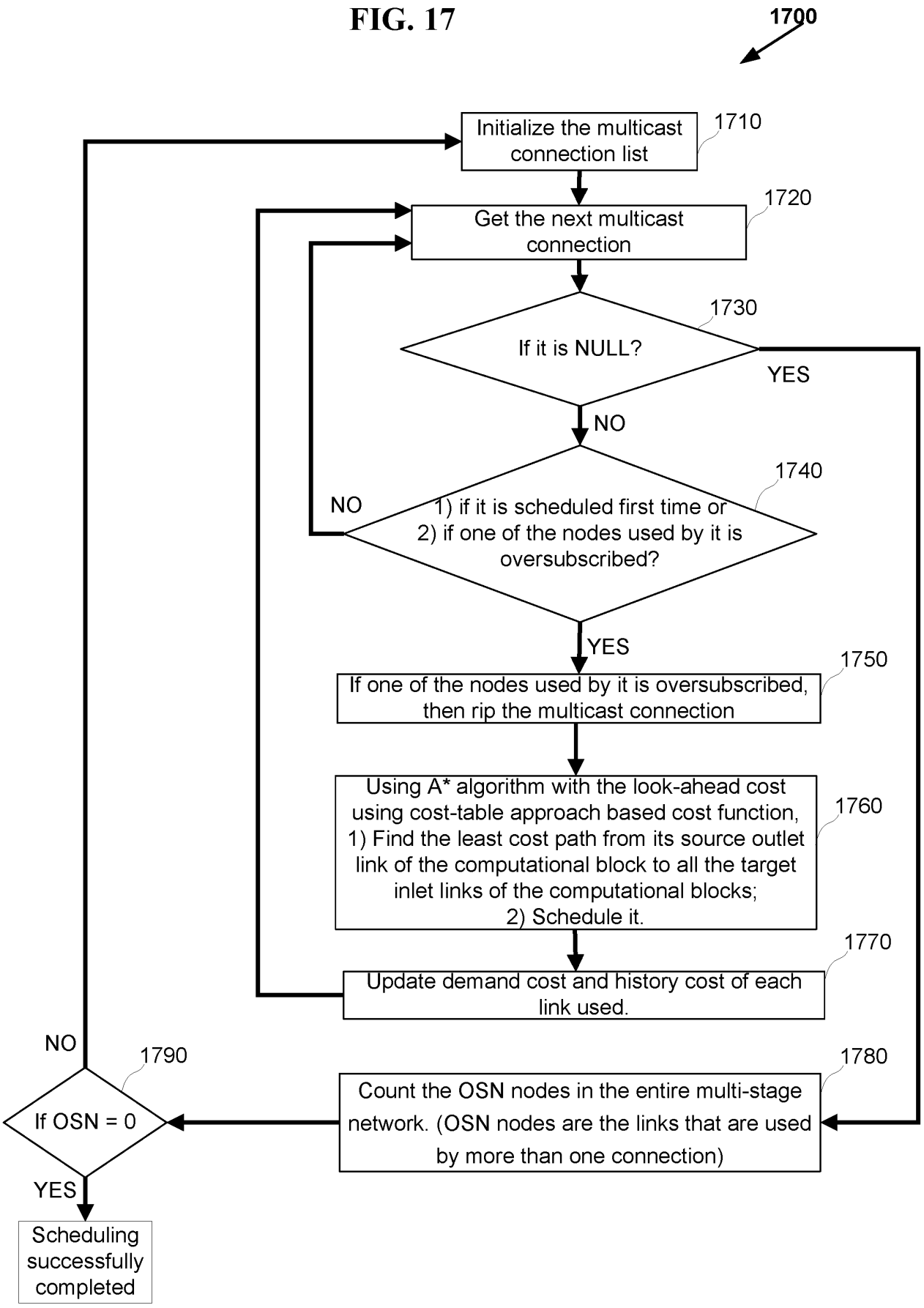
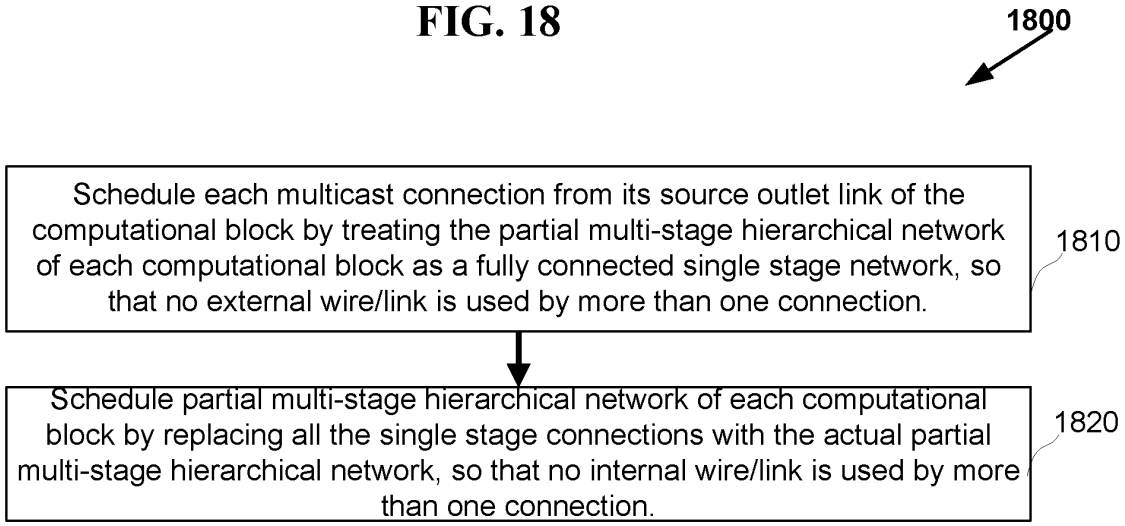

1700
Initialize the multicast connection list
1710
Get the next multicast connection
1720
If it is NULL?
1730
YES
NO
1) if it is scheduled first time or
2) if one of the nodes used by it is oversubscribed?
1740
NO
YES
If one of the nodes used by it is oversubscribed, then rip the multicast connection
1750
Using A* algorithm with the look-ahead cost using cost-table approach based cost function,
1) Find the least cost path from its source outlet link of the computational block to all the target inlet links of the computational blocks;
2) Schedule it.
1760
Update demand cost and history cost of each link used.
1770
Count the OSN nodes in the entire multi-stage network. (OSN nodes are the links that are used by more than one connection)
1780
If OSN = 0
1790
NO
YES
Scheduling successfully completed

FIG. 18


1800
Schedule each multicast connection from its source outlet link of the computational block by treating the partial multi-stage hierarchical network of each computational block as a fully connected single stage network, so that no external wire/link is used by more than one connection.
1810
Schedule partial multi-stage hierarchical network of each computational block by replacing all the single stage connections with the actual partial multi-stage hierarchical network, so that no internal wire/link is used by more than one connection.
1820

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	V-0060US
	Application Number	
Title of Invention	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
Dr.	Venkat		Konda	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	State/Province	Country of Residence
San Jose	CA	US

Mailing Address of Inventor:

Address 1	6278 Grand Oak Way
Address 2	
City	San jose
State/Province	CA
Postal Code	95135
Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	38139		
Email Address	venkat@kondatech.com	Add Email	Remove Email

Application Information:

Title of the Invention	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS		
Attorney Docket Number	V-0060US	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	30	Suggested Figure for Publication (if any)	6B

Filing By Reference :

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	V-0060US
	Application Number	
Title of Invention	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS	

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☒ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	38139		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	15/884911	2018-01-31

Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/884911	Continuation of	15/331855	2016-10-22	9929977	2018-03-27

Prior Application Status	Patented		Remove

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	V-0060US
	Application Number	
Title of Invention	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS	

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/331855	Continuation of	14/329876	2014-07-11	9509634	2016-11-29
Prior Application Status				Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
14/329876	Claims benefit of provisional	61/846083	2013-07-15		
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14/329876	Continuation in part of	14/199168	2014-03-06	9374322	2016-06-21
Prior Application Status				Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
14/199168	Continuation of	PCT/US12/53814	2012-09-06		
Prior Application Status				Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
PCT/US12/53814	Claims benefit of provisional	61/531615	2011-09-07		
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.				Add	

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.			Add

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	V-0060US
	Application Number	
Title of Invention	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☒ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	V-0060US
	Application Number	
Title of Invention	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS	

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	Konda Technologies Inc.

Mailing Address Information For Applicant:

Address 1	6278 Grand Oak Way		
Address 2			
City	San Jose	**State/Province**	CA
Country	US	Postal Code	95135
Phone Number	408-472-3273	Fax Number	408-238-2478
Email Address	venkat@kondatech.com		

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

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If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	V-0060US
	Application Number	
Title of Invention	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS	

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	/venkat konda/			Date (YYYY-MM-DD)	2019-09-06
First Name	Venkat	Last Name	Konda	Registration Number	

Additional Signature may be generated within this form by selecting the Add button. Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent C o o p eration Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING "REFERENCE" APPLICATION	Docket Number (Optional) V-0060US

In re Application of: Konda Technologies Inc.

Application No.: 16/562450

Filed: 09-06-2019

For: FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS

The applicant, Konda Technologies Inc., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending **reference** Application Number 15/884,911, filed, 01/31/2018, as the term of any patent granted on said **reference** application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending **reference** application. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the **reference** application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term of any patent granted on said **reference** application, "as the term of any patent granted on said **reference** application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending **reference** application," in the event that: any such patent granted on the pending **reference** application expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

Check either box 1 or 2 below, if appropriate.

1. ☑ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☐ The undersigned is an attorney or agent of record. Reg. No. _____

/Venkat Konda/	09/06/2019
Signature	Date
Venkat Konda	
Typed or printed name	
Founder/CEO	408-472-3273
Title	Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) is included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal	
Application Number:	16562450
Filing Date:	
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Filer:	Venkat Konda
Attorney Docket Number:	V-0060US
Filed as Small Entity	
Filing Fees for **Utility under 35 USC 111(a)**	

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
STATUTORY OR TERMINAL DISCLAIMER	2814	1	160	160
		Total in USD ($)		**160**

Electronic Acknowledgement Receipt	
EFS ID:	37083123
Application Number:	16562450
International Application Number:	
Confirmation Number:	6438
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkat Konda
Filer Authorized By:	
Attorney Docket Number:	V-0060US
Receipt Date:	06-SEP-2019
Filing Date:	
Time Stamp:	03:39:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$160
RAM confirmation Number	E201996447394799
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer Filed	V-0060US-aia0025.pdf	295829 93727fbd35227b4e31cf7a2d0ef58f0b440d afde	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	29867 e867c58d0bd0a11997a25827916ea550c46 c53a3	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	325696		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
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PTO/SB/08b (07-09)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	
Filing Date	09-06-2019
First Named Inventor	Venkat Konda
Art Unit	
Examiner Name	
Attorney Docket Number	V-0060US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	C. Clos, "A Study of Non-Blocking Switching Networks," Bell System Technical Journal, 32:406-424, 1953.	
	2	A. DeHon, "Balancing Interconnect and Computation in a Reconfigurable Computing Array," ACM Int. Symp. on FPGA, pp. 69-78, Feb. 1999	
	3	Chihming Chang, Rami Melhem, "Arbitrary Size Benes Networks", Journal: Parallel Processing Letters - PPL , vol. 7, no. 3, pp. 279-284, 1997.	
	4	HODA EL-SAYED and ABDOU YOUSSEF; "The r-truncated Benes Networks and their Randomized Routing Algorithms"1997 Intl Conf on Parallel and Dist Sys, Seoul, Korea, December 1997.	
	5	Guy Lemieux and David Lewis, "Using Sparse Crossbars within LUT Clusters", Procds of the ACM/SIGDA Intl Symp on Field Prog Gate Arrays 2001, Feb. 11–13, 2001, Monterey, CA.	
	6	P. Manuel, W. K. Qureshi, A. William, A. Muthumalai, "VLSI layout of Benes networks,", J. of Discrete Math. Sci. & Cryptography, vol. 10, no, 4, pp. 461-472, 2007	
	7	Quinn, Michael J, "Parallel Computing: Theory and Practice", 2nd. ed., 1994, McGraw Hill Series in computer Science, Networks, and parallel computing, ISBN 0-07-051294-9	
	8	Ronald I. Greenberg, "The Fat-Pyramid and Universal Parallel Computation Independent of wire delay" IEEE Trans. Computers, 43(12):1358-1364, December 1994.	
	9	Hypertree: A Multiprocessor Interconnection Topology , by James R. Goodman and Carlo H Sequin, Computer Science Technical Report #427, Dept , of EECS, University of California	
	10	Data Movement Techniques for the pyramid computer, Russ Miller and Quentin F. Stout, SIAM Journal on Computing, Vol. 16, no. 1, pp. 38 - 60, Feb. 1987.	

Examiner Signature		Date Considered	

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[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

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Electronic Acknowledgement Receipt	
EFS ID:	37084112
Application Number:	16562450
International Application Number:	
Confirmation Number:	6438
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkat Konda
Filer Authorized By:	
Attorney Docket Number:	V-0060US
Receipt Date:	06-SEP-2019
Filing Date:	
Time Stamp:	09:54:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	16-562450-sb0008b.pdf	366215 c009f531c4c633ad045da86045088de8d4bcd8f4	no	2

Warnings:

Information:					
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Information:					
3	Non Patent Literature	Clos1953.pdf	7975907 d6a9c66d332e4c29888ccde6179427c0ba887aa9	no	19
Warnings:					
Information:					
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Warnings:					
Information:					
5	Non Patent Literature	fixedws_fpga99.pdf	1537050 ed8daa940d6fb2f63f9231280b1ee7e181653f8b	no	10
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6	Non Patent Literature	Goodman-Sequin1981.pdf	3211686 d6f9f7eaab18a0e7ed42e01b567354e2bacbab38	no	39
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7	Non Patent Literature	Greenberg1994.pdf	12957830 9e92f9830a8848dcde5fe6f13cf9b346da84f167	no	12
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Information:					
8	Non Patent Literature	Manuel07.pdf	324448 28c24822eaa8b56ffa3fa1e02e3246e229c28ac1	no	7
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9	Non Patent Literature	Miller-Stout1987.pdf	3124080 83ca3b770a7eaffe22b5897c91b352aecfbb8132	no	23
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10	Non Patent Literature	Parallel-Computing-MQuinn-1994.pdf	3499947 49bc645440cbb88779a58e37a350e398a13c9ef9	no	22
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Information:					
		Total Files Size (in bytes):	33457503		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	
Filing Date	09-06-2019
First Named Inventor	Venkat Konda
Art Unit	
Examiner Name	
Attorney Docket Number	V-0060US

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 8269523-b2	09-18-2012	Venkat Konda	all FIGs
	2	US- 8898611-b2	11-25-2014	Venkat Konda	all FIGs
	3	US- 9529958-b2	12-27-2016	Venkat Konda	all FIGs
	4	US- 8270400-b2	09-18-2012	Venkat Konda	all FIGs
	5	US- 8170040-b2	05-01-2012	Venkat Konda	all FIGs
	6	US- 8363649-b2	01-29-2013	Venkat Konda	all FIGs
	7	US- 6185220-b1	02-06-2001	Muthukrishnan et. al.	layout FIGs
	8	US- 6940308-b2	09-06-2005	Wong	layout FIGs
	9	US- 5451936	09-19-1995	Yang et. al.	layout FIGs
	10	US- 5153843	10-061992	Kenneth E. Batcher	layout FIGs
	11	US- 6018523	01-25-2000	Shimon Even	layout FIGs
	12	US-			
	13	US-			
	14	US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

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Electronic Acknowledgement Receipt	
EFS ID:	37084179
Application Number:	16562450
International Application Number:	
Confirmation Number:	6438
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkat Konda
Filer Authorized By:	
Attorney Docket Number:	V-0060US
Receipt Date:	06-SEP-2019
Filing Date:	
Time Stamp:	09:59:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	16-562450-sb0008b.pdf	253174 867533e02f119a816cb7fa6e26ba15d92810cdaa	no	2

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Art Unit	
Examiner Name	
Attorney Docket Number	V-0060US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	A. DeHon, "Unifying Mesh- and Tree-Based Programmable Interconnect," IEEE Trans. on Very Large Scale Int. Systems, vol. 12, no. 10, pp. 1051-1065, Oct. 2004	
	2	Guy Lemieux and David Lewis. Analtyical framework for switch block design. In Intl. Conference on Field Programmable Logic and Applications, pages 122-131, September 2002.	
	3	Chen, G; Lau, FCM, "A tight layout of the cube-connected cycles", The 4th International Conference on High Perf. Computing, Bangalore, India, 18-21 December 1997, p. 422-427	
	4	Michael Shyu, Yu-Dong Chang, Guang-Ming Wu, and Yao-Wen Chang, "Generic universal switch blocks. IEEE Transactions on Computers,49(4):348-359, April 2000.	
	5	Y. Yamada, et. al. , ```Folded Fat H-Tree: an interconnection topology for Dynamically Reconfigurable Processor Array", Embed and Ubiq. Cmpting, Intl Conf. EUC 2004.	
	6	V. P. Roychdowdhury et. al., "Segmented Channel Routing," IEEE Trans on Computer-Aided Design of Integrated Circuits and Systems, Vol. 12, No. 1, pp. 79-95, January 1993.	
	7	André DeHon. Compact, Multilayer Layout for Butterfly Fat-Tree. In Twelfth Annual ACM Symposium on Parallel Algs and Architectures (SPAA 2000), pages 206--215, July 9-12, 2000	

Examiner Signature		Date Considered	

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Electronic Acknowledgement Receipt

EFS ID:	37084298
Application Number:	16562450
International Application Number:	
Confirmation Number:	6438
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
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File Listing:

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1	Information Disclosure Statement (IDS) Form (SB08)	16-562450-sb0008b.pdf	372935 9681faa402c410490db47a4e1c8c083955157866	no	2

Warnings:

Information:					
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2	Non Patent Literature	chen97tighter.pdf	323946 0dd2b5cbe895ff3ee8cd042029c2681fdd9de6d3	no	17
Warnings:					
Information:					
3	Non Patent Literature	DeHon-Unify-Mesh-Tree.pdf	1438096 6ddb3d1e190b2a260735612085845bd2420e7395c	no	15
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4	Non Patent Literature	Segmented-Routing.pdf	1410463 74349da7d5c21a06a3fbbe8a991296781c77b49e	no	17
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5	Non Patent Literature	Switchbox-Design.pdf	151991 87be02898d4d0bf00141b602a90007c7f9a76e09	no	10
Warnings:					
Information:					
6	Non Patent Literature	tc-gusb.pdf	578658 0281587e0334ddcb7ce8b8fc128a84a2972ced97	no	12
Warnings:					
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7	Non Patent Literature	yamada-euc-2004.pdf	199391 ca0d82b4e0733949bdac38ce71e1bb66ec5ba302	no	10
Warnings:					
Information:					
8	Non Patent Literature	fold-spaa2000.pdf	199719 c70318b2c9e36d6a8e97400a432f5d2c3b5ed502	no	10
Warnings:					
Information:					

Total Files Size (in bytes):	4675199

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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PTO/SB/08b (07-09)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	
Filing Date	09-06-2019
First Named Inventor	Venkat Konda
Art Unit	
Examiner Name	
Attorney Docket Number	V-0060US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	Ivo Dobbelaere, Mark Horowitz, and Abbas El Gamal. Regenerative feedback repeaters for programmable interconnections. IEEE Journal of Solid-State Circuits, 30(11), 1995.	
	2	F. Petrini et. al., "k-ary n-trees: High performance networks for massively parallel architectures, in: Proceedings of the 11th Intl Parallel Proc. Symp. , IPPS'97, pp. 87-93	
	3	P.Pande et al. "Evaluation of MP-SoC Interconnect Architectures: a Case Study", Proceedings of 4th IWSOC, Banff, Alberta, Canada, 19th-21st July, 2004	
	4	Yeh, C.-H., Varvarigos, E.A., Parhami, B.: Multilayer VLSI layout for interconnection networks. In: Proc. Intl. Conf. on Parallel Processing, 2000.	
	5	M. Lin, A. El Gamal, "A Low-Power Field-Programmable Gate Array Routing Fabric," IEEE Transactions on Very Large Scale Integration, Vol. 17, No. 10, pp. 1481-1494, Oct. 2009	
	6	AVIOR, A et. al., A Tight Layout of the Butterfly Network. Proc. 8-th Annual ACM Symp. on Parallel Alg. and Arch. (SPAA '96), ACM Press Ed., 1996, pp 170–175.	
	7	A. El Gamal et. al., "An Architecture for Electrically Configurable Gate Arrays," IEEE Jrnl of Solid-State Circuits, Vol. 24, No. 2, pp. 394-398, April 1989.	
	8	Vaughn Betz et. al., Directional bias and non-uniformity in FPGA global routing architectures. In IEEE/ACM Intl. Conference on Computer-Aided Design, pp. 652-659, san jose, 96	
	9	W. Tsu et. al., "HSRA: High-Speed, Hierarchical Synchronous Reconfigurable Array," in Procds. of the Intl. Symp. on Field-Programmable Gate Arrays, February 1999, pp. 125-134	
	10	André DeHon. Rent's Rule Based Switching Requirements. In System-Level Interconnect Prediction (SLIP 2001), pages 197--204, March 31--April 1, 2001	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	37084392
Application Number:	16562450
International Application Number:	
Confirmation Number:	6438
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkat Konda
Filer Authorized By:	
Attorney Docket Number:	V-0060US
Receipt Date:	06-SEP-2019
Filing Date:	
Time Stamp:	10:16:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	16-562450-sb0008b.pdf	366843 3dd7a735f0021b4c54d675cdced27f00f3539629	no	2

Warnings:

Information:					
This is not an USPTO supplied IDS fillable form					
2	Non Patent Literature	iccad96.pdf	61851 db9bd3def8037be018e5dfcab0485641a2d52eb1	no	8
Warnings:					
Information:					
3	Non Patent Literature	Interconnect-Architecture.pdf	477835 d983056a29d99c7a98d2a192fc68dd6319b5a62e	no	5
Warnings:					
Information:					
4	Non Patent Literature	light-layout-of-butterfly-network.pdf	286748 b1185d69acf8ae11965f973e3ce25d3039363dcf	no	14
Warnings:					
Information:					
5	Non Patent Literature	LP-FPGA-Fabric.pdf	1080349 f9418381d3375c3a053afb58a207d362057b4d46	no	14
Warnings:					
Information:					
6	Non Patent Literature	ML-VLSI-layouts-for-InterconNetwks.pdf	109196 d09cd8c0e4fa8875381783ff939a165cd9ba8884	no	8
Warnings:					
Information:					
7	Non Patent Literature	pandep-MP-SoC-Interconn.pdf	210576 dec2bd4b967d5facd4b59d783b97636b4a922a1e	no	4
Warnings:					
Information:					
8	Non Patent Literature	petrini97kary.pdf	119892 86e78185b99255ad0e063a3eeb151106ff4c05ae	no	7
Warnings:					
Information:					

9	Non Patent Literature	Programmable-interconnections.pdf	959944 5d5bbd957fbdba455f41cfad06e99e3448faf29c	no	8
Warnings:					
Information:					
10	Non Patent Literature	rentsw-slip01.pdf	1446852 b1cba481afb7f05bd0bd03cc64bdecde5eb2db58	no	8
Warnings:					
Information:					
		Total Files Size (in bytes):	5120086		

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New Applications Under 35 U.S.C. 111

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PTO/SB/08b (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	
Filing Date	09-06-2019
First Named Inventor	Venkat Konda
Art Unit	
Examiner Name	
Attorney Docket Number	V-0060US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	Guy Lemieux et.al., Generating highlyroutablesparse crossbars for PLDs. In ACMISIGDA Int'l. Symposium on Field Programmable Gate Arrays, pp155-164, Monterey, CA, February 2000	
	2	S. Sivaswamy et. al., "HARP: hard-wired routing pattern FPGAs", FPGA'05, Monterey, California, USA, February 20–22, 2005.	
	3	Yeh, C.-H., E.A. Varvarigos, and B. Parhami, "Efficient VLSI layouts of hypercubic networks," Proc. Symp. Frontiers of Massively Parallel Computation, Feb. 1999	
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Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Acknowledgement Receipt	
EFS ID:	37084646
Application Number:	16562450
International Application Number:	
Confirmation Number:	6438
Title of Invention:	FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkat Konda
Filer Authorized By:	
Attorney Docket Number:	V-0060US
Receipt Date:	06-SEP-2019
Filing Date:	
Time Stamp:	10:32:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	16-562450-sb0008b.pdf	369485 6a72fd7d6389e88075882eb60b80c6e807a6cdf2	no	2

Warnings:

Information:					
This is not an USPTO supplied IDS fillable form					
2	Non Patent Literature	Efficient-layout-of-hyperCntwks.pdf	235617 cea3f29ab13dbe4f26e5abd98ab609adf9806b8c	no	8
Warnings:					
Information:					
3	Non Patent Literature	fpga05-harp.pdf	261760 e9a60a1a1e2d7b2ab393590e3109eac3ec78b0df	no	9
Warnings:					
Information:					
4	Non Patent Literature	Generating-2000.pdf	191395 72b0f7ce5f8fc1bdb81a7b829f802f2118c4c209	no	10
Warnings:					
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		Total Files Size (in bytes):	1058257		

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FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS

Venkat Konda

CROSS REFERENCE TO RELATED APPLICATIONS

This application is Continuation Application and claims priority to US Application Serial No. 15/884,911 entitled "FAST SCHEDULING AND OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed January 31, 2018, which is Continuation Application and claims priority to US Application Serial No. 15/331,855 entitled "FAST SCHEDULING AND OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed October 22, 2016, issued as US Patent No. 9,929,977 on March 27, 2018, which is Continuation Application and claims priority to US Application Serial No. 14/329,876 entitled "FAST SCHEDULING AND OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed July 11, 2014, issued as US Patent No. 9,509,634 on November 29, 2016, which claims priority to U.S. Provisional Patent Application Serial No. 61/846,083 entitled "FAST SCHEDULING AND OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed July 15, 2013, and also Continuation-in-Part Application and claims priority to US Application Serial No. US14/199,168 entitled "OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS FOR PRACTICAL ROUTING APPLICATIONS" by Venkat Konda assigned to the same assignee as the current application, filed March 6, 2014, issued as US Patent No. 9,374,322 on June 21, 2016, which claims priority to PCT Application Serial No. PCT/US12/53814 entitled "OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS FOR PRACTICAL ROUTING APPLICATIONS" by Venkat Konda assigned to the same assignee as the current

application, filed September 6, 2012, which is Continuation-in-Part application and claims priority to U.S. Provisional Patent Application Serial No. 61/531,615 entitled "OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS FOR PRACTICAL ROUTING APPLICATIONS" by Venkat Konda assigned to the same assignee as the current application, filed September 7, 2011.

This application is related to and incorporates by reference in its entirety the US Patent No. 8,270,400 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, issued September 18, 2012, which claims priority to PCT Application Serial No. PCT/US08/56064 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed March 6, 2008, which claims priority to U.S. Provisional Patent Application Serial No. 60/905,526 entitled "LARGE SCALE CROSSPOINT REDUCTION WITH NONBLOCKING UNICAST & MULTICAST IN ARBITRARILY LARGE MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed March 6, 2007, and U.S. Provisional Patent Application Serial No. 60/940, 383 entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety US Patent No. 8,170,040 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, issued May 1, 2012, which claims priority to PCT Application Serial No. PCT/US08/64603 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, which claims priority to U.S. Provisional Patent Application Serial No. 60/940, 387 entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007, and U.S. Provisional Patent Application Serial No. 60/940, 390 entitled "FULLY CONNECTED GENERALIZED

MULTI-LINK BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007

This application is related to and incorporates by reference in its entirety US Patent No. 8,363,649 entitled "FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, issued January 29, 2013, which claims priority to PCT Application Serial No. PCT/US08/64604 entitled "FULLY CONNECTED GENERALIZED MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, which claims priority to U.S. Provisional Patent Application Serial No. 60/940, 389 entitled "FULLY CONNECTED GENERALIZED REARRANGEABLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007, U.S. Provisional Patent Application Serial No. 60/940, 391 entitled "FULLY CONNECTED GENERALIZED FOLDED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007 and U.S. Provisional Patent Application Serial No. 60/940, 392 entitled "FULLY CONNECTED GENERALIZED STRICTLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety US Patent No. 8,269,523 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS" by Venkat Konda assigned to the same assignee as the current application, issued September 18, 2012, which claims priority to PCT Application Serial No. PCT/U08/64605 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 22, 2008, which claims priority to U.S. Provisional Patent Application Serial No. 60/940, 394 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed May 25, 2007.

This application is related to and incorporates by reference in its entirety US Patent No. 8,898,611 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED AND PYRAMID NETWORKS WITH LOCALITY EXPLOITATION" by Venkat Konda assigned to the same assignee as the current application, issued November 25, 2014, which claims priority to PCT Application Serial No. PCT/US10/52984 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED AND PYRAMID NETWORKS WITH LOCALITY EXPLOITATION" by Venkat Konda assigned to the same assignee as the current application, filed October 16, 2010, which claims priority to U.S. Provisional Patent Application Serial No. 61/252, 603 entitled "VLSI LAYOUTS OF FULLY CONNECTED NETWORKS WITH LOCALITY EXPLOITATION" by Venkat Konda assigned to the same assignee as the current application, filed October 16, 2009, and U.S. Provisional Patent Application Serial No. 61/252, 609 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED AND PYRAMID NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed October 16, 2009.

BACKGROUND OF INVENTION

Multi-stage interconnection networks such as Benes networks and butterfly fat tree networks are widely useful in telecommunications, parallel and distributed computing. However VLSI layouts, known in the prior art, of these interconnection networks in an integrated circuit are inefficient and complicated.

Other multi-stage interconnection networks including butterfly fat tree networks, Banyan networks, Batcher-Banyan networks, Baseline networks, Delta networks, Omega networks and Flip networks have been widely studied particularly for self-routing packet switching applications. Also Benes Networks with radix of two have been widely studied and it is known that Benes Networks of radix two are shown to be built with back to back baseline networks which are rearrangeably nonblocking for unicast connections.

The most commonly used VLSI layout in an integrated circuit is based on a two-dimensional grid model comprising only horizontal and vertical tracks. An intuitive interconnection network that utilizes two-dimensional grid model is 2D Mesh Network and its variations such as segmented mesh networks. Hence routing networks used in VLSI layouts are typically 2D mesh networks and its variations. However Mesh Networks require large scale cross points typically with a growth rate of $O(N^2)$ where N is the number of computing elements, ports, or logic elements depending on the application.

Multi-stage interconnection network with a growth rate of $O(N \times \log N)$ requires significantly small number of cross points. U.S. Patent 6,185,220 entitled "Grid Layouts of Switching and Sorting Networks" granted to Muthukrishnan et al. describes a VLSI layout using existing VLSI grid model for Benes and Butterfly networks. U.S. Patent 6,940,308 entitled "Interconnection Network for a Field Programmable Gate Array" granted to Wong describes a VLSI layout where switches belonging to lower stage of Benes Network are laid out close to the logic cells and switches belonging to higher stages are laid out towards the center of the layout.

Due to the inefficient and in some cases impractical VLSI layout of Benes and butterfly fat tree networks on a semiconductor chip, today mesh networks and segmented mesh networks are widely used in the practical applications such as field programmable gate arrays (FPGAs), programmable logic devices (PLDs), and parallel computing interconnects. The prior art VLSI layouts of Benes and butterfly fat tree networks and VLSI layouts of mesh networks and segmented mesh networks require large area to implement the switches on the chip, large number of wires, longer wires, with increased power consumption, increased latency of the signals which effect the maximum clock speed of operation. Some networks may not even be implemented practically on a chip due to the lack of efficient layouts.

Fully connected Benes and butterfly fat tree networks are an over kill for certain practical routing applications and need to be optimized to significantly improve area, power and performance of the routing network.

SUMMARY OF INVENTION

Significantly optimized multi-stage networks for faster scheduling of connections, useful in wide target applications, with VLSI layouts (or floor plans) using only horizontal and vertical links to route large scale sub-integrated circuit blocks having inlet and outlet links, and laid out in an integrated circuit device in a two-dimensional grid arrangement of blocks, (for example in an FPGA where the sub-integrated circuit blocks are Lookup Tables, or memory blocks, or DSP blocks) are presented. The optimized multi-stage networks in each block employ several slices of rings of stages of switches with inlet and outlet links of sub-integrated circuit blocks connecting to rings from either left-hand side only, or from right-hand side only, or from both left-hand side and right-hand side.

The optimized multi-stage networks with their VLSI layouts employ shuffle exchange multi-drop links where outlet links of cross links from switches in a stage of a ring in one sub-integrated circuit block are connected to either inlet links of switches in the another stage of a ring in another sub-integrated circuit block or inlet links of switches in the another stage of a ring in the same sub-integrated circuit block so that said cross links are either vertical links or horizontal and vice versa.

The VLSI layouts exploit spatial locality so that different sub-integrated circuit blocks that are spatially nearer are connected with shorter shuffle exchange links compared to the shuffle exchange links between spatially farther sub-integrated circuit blocks. The optimized multi-stage networks provide high routability for broadcast, unicast and multicast connections, yet with the benefits of significantly lower cross points hence smaller area, lower signal latency, lower power and with significant fast compilation or routing time. Various scheduling methods are also disclosed to schedule a set of multicast connections in the multi-stage hierarchical network.

The optimized multi-stage networks $V_{Comb}(N_1, N_2, d, s)$ & $V_{D-Comb}(N_1, N_2, d, s)$ according to the current invention inherit the properties of one or more, in addition to

additional properties, generalized multi-stage and pyramid networks $V(N_1,N_2,d,s)$ & $V_p(N_1,N_2,d,s)$, generalized folded multi-stage and pyramid networks $V_{fold}(N_1,N_2,d,s)$ & $V_{fold-p}(N_1,N_2,d,s)$, generalized butterfly fat tree and butterfly fat pyramid networks $V_{bft}(N_1,N_2,d,s)$ & $V_{bfp}(N_1,N_2,d,s)$, generalized multi-link multi-stage and pyramid networks $V_{mlink}(N_1,N_2,d,s)$ & $V_{mlink-p}(N_1,N_2,d,s)$, generalized folded multi-link multi-stage and pyramid networks $V_{fold-mlink}(N_1,N_2,d,s)$ & $V_{fold-mlink-p}(N_1,N_2,d,s)$, generalized multi-link butterfly fat tree and butterfly fat pyramid networks $V_{mlink-bft}(N_1,N_2,d,s)$ & $V_{mlink-bfp}(N_1,N_2,d,s)$, generalized hypercube networks $V_{hcube}(N_1,N_2,d,s)$, and generalized cube connected cycles networks $V_{CCC}(N_1,N_2,d,s)$ for s = 1,2,3 or any number in general.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1A is a diagram 100A of an exemplary partial multi-stage hierarchical network corresponding to one block with 4 inputs and 2 outputs of a computational block connecting only from left-hand side, to route practical applications such as FPGA routing of hardware designs in accordance with the invention.

FIG. 1B is a diagram 100B of an exemplary partial multi-stage hierarchical network corresponding to one block with 8 inputs and 4 outputs of a computational block connecting from both left-hand side and right-hand side, to route practical applications such as FPGA routing of hardware designs in accordance with the invention.

FIG. 1C is a diagram 100C of an exemplary partial multi-stage hierarchical network corresponding to one block, by dividing the network into two parallel and independent slices, with 16 inputs and 4 outputs of a computational block connecting from both left-hand side and right-hand side, to route practical applications such as FPGA routing of hardware designs in accordance with the invention.

FIG. 1C1 is a diagram 100C1, FIG. 1C2 is a diagram 100C2, FIG. 1C3 is a diagram 100C3, and FIG. 1C4 is a diagram 100C4 illustrate the specific details of the diagram 100C of FIG. 1C, particularly the connections between different slices.

FIG. 1C5 is a diagram 100C5 illustrate the specific details of the diagram 100C of FIG. 1C, particularly the internal connections between two successive stages of any ring of any slice, in one embodiment.

FIG. 2A is a diagram 200A, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block.

FIG. 2B is a diagram 200B, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block.

FIG. 2C is a diagram 200C, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block.

FIG. 2D is a diagram 200D, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block.

FIG. 2E is a diagram 200E, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block.

FIG. 2F is a diagram 200F, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block.

FIG. 3A is a diagram 300A, in an embodiment of, all the connections between two successive stages of two different rings in the same block or in two different blocks of a multi-stage hierarchical network.

FIG. 3B is a diagram 300B, in an embodiment of, all the connections between two successive stages of two different rings in the same block or in two different blocks of a multi-stage hierarchical network.

FIG. 3C is a diagram 300C, in an embodiment of, all the connections between two successive stages of two different rings in the same block or in two different blocks of a multi-stage hierarchical network.

FIG. 3D is a diagram 300D, in an embodiment of, all the connections between two successive stages of two different rings in the same block or in two different blocks of a multi-stage hierarchical network.

FIG. 3E is a diagram 300E, in an embodiment of, all the connections between two successive stages of two different rings in the same block or in two different blocks of a multi-stage hierarchical network.

FIG. 4A is a diagram 400A, in an embodiment of, all the connections between different stages of two different rings in the same block or in two different blocks of a multi-stage hierarchical network.

FIG. 4B is a diagram 400B, in an embodiment of, all the connections between different stages of two different rings in the same block or in two different blocks of a multi-stage hierarchical network.

FIG. 5A is a diagram 500A, in an embodiment of, all the connections with multi-drop hop wires, between two successive stages of two different rings in the same block or in two different blocks of a multi-stage hierarchical network.

FIG. 6A is a diagram 600A, in an embodiment of, all the connections with multi-drop hop wires, between different stages of two different rings in the same block or in two different blocks of a multi-stage hierarchical network.

FIG. 6B is a diagram 600B, in an embodiment of, all the connections with multi-drop hop wires, between different stages of two different rings in the same block or in two different blocks of a multi-stage hierarchical network.

FIG. 7A is a diagram 700A, is an embodiment of hop wire connection chart corresponding to a block of multi-stage hierarchical network, where the inter-ring

connections are given between two successive stages of two different rings as described in diagrams 300A of FIG. 3A to 300E of FIG. 3E.

FIG. 8 is a diagram 800, is an embodiment of 2D-grid of blocks with each block corresponding to a partial multi-stage network to implement an exemplary multi-stage hierarchical network, in accordance with the invention.

FIG. 9A is a diagram 900A, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block, with delay optimizations.

FIG. 9B is a diagram 900B, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block, with delay optimizations.

FIG. 9C is a diagram 900C, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block, with delay optimizations.

FIG. 9D is a diagram 900D, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block, with delay optimizations.

FIG. 9E is a diagram 900E, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block, with delay optimizations.

FIG. 10A is a diagram 1000A, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block, with delay optimizations.

FIG. 10B is a diagram 1000B, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block, with delay optimizations.

FIG. 10C is a diagram 1000C, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block, with delay optimizations.

FIG. 10D is a diagram 1000D, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block, with delay optimizations.

FIG. 10E is a diagram 1000E, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block, with delay optimizations.

FIG. 10F is a diagram 1000F, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block, with delay optimizations.

FIG. 11A is a diagram 1100A, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block, with delay optimizations.

FIG. 11B is a diagram 1100B, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block, with delay optimizations.

FIG. 11C is a diagram 1100C, in an embodiment of, a stage in a ring of multi-stage hierarchical network corresponding to one block, with delay optimizations.

FIG. 12 is a diagram 1200, in an embodiment, all the connections between two successive stages of two different rings in the same block or in two different blocks of a multi-stage hierarchical network with delay optimizations.

FIG. 13 is a diagram 1300, in one embodiment, all the connections between two successive stages of two different rings in the same block or in two different blocks of a multi-stage hierarchical network with delay optimizations.

FIG. 14 is a diagram 1400, in an embodiment of, all the connections between two successive stages of two different rings in the same block or in two different blocks of a multi-stage hierarchical network with delay optimizations.

FIG. 15 is a diagram 1500, in an embodiment of, all the connections between two successive stages of two different rings in the same block or in two different blocks of a multi-stage hierarchical network with delay optimizations.

FIG. 16A1 is a diagram 1600A1 of an exemplary prior art implementation of a two by two switch; FIG. 16A2 is a diagram 1600A2 for programmable integrated circuit prior art implementation of the diagram 1600A1 of FIG. 16A1; FIG. 16A3 is a diagram 1600A3 for one-time programmable integrated circuit prior art implementation of the diagram 1600A1 of FIG. 16A1; FIG. 16A4 is a diagram 1600A4 for integrated circuit placement and route implementation of the diagram 1600A1 of FIG. 16A1.

FIG. 17 is high-level flowchart of a scheduling method 1700 according to the invention, used to set up a set of multicast connections in the complete multi-stage hierarchical network as disclosed in the current invention.

FIG. 18 is high-level flowchart of a scheduling method 1800 according to the invention, used to set up a set of multicast connections first on the external wires and then on internal wires in the complete multi-stage hierarchical network as disclosed in the current invention.

DETAILED DESCRIPTION OF THE INVENTION

Fully connected multi-stage hierarchical networks are an over kill in every dimension such as area, power, and performance for certain practical routing applications and need to be optimized to significantly improve savings in area, power and performance of the routing network. The present invention discloses several embodiments of the optimized multi-stage hierarchical networks for practical routing applications along with their VLSI layout (floor plan) feasibility and simplicity.

The multi-stage hierarchical networks considered for optimization in the current invention include: generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$, and generalized cube connected cycles networks $V_{ccc}(N_1, N_2, d, s)$ for s = 1,2,3 or any number in general. Alternatively the optimized multi-stage hierarchical networks disclosed in this invention inherit the properties of one or more of these networks, in addition to additional properties that may not be exhibited these networks.

The optimized multi-stage hierarchical networks disclosed are applicable for practical routing applications, with several goals such as: 1) all the signals in the design starting from an inlet link of the network to an outlet link of the network need to be setup without blocking. These signals may consist of broadcast, unicast and multicast connections; Each routing resource may need to be used by only one signal or connection; 2) physical area consumed by the routing network to setup all the signals needs to be small; 3) power consumption of the network needs to be small, after the signals are setup. Power may be both static power and dynamic power; 4) Delay of the signal or a connection needs to be small after it is setup through a path using several routing resources in the path. The smaller the delay of the connections will lead to faster performance of the design. Typically delay of the critical connections determines the performance of the design on a given network; 5) Designs need to be not only routed through the network (i.e., all the signals need to be setup from inlet links of the network to the outlet links of the network.), but also the routing needs to be in faster time using efficient routing algorithms; 6) Efficient VLSI layout of the network is also critical and can greatly influence all the other parameters including the area taken up by the network on the chip, total number of wires, length of the wires, delay through the signal paths and hence the maximum clock speed of operation.

The different varieties of multi-stage networks described in various embodiments in the current invention have not been implemented previously on the semiconductor chips. The practical application of these networks includes Field Programmable Gate Array (FPGA) chips. Current commercial FPGA products such as Xilinx's Vertex, Altera's Stratix, Lattice's ECPx implement island-style architecture using mesh and segmented mesh routing interconnects using either full crossbars or sparse crossbars. These routing interconnects consume large silicon area for crosspoints, long wires, large signal propagation delay and hence consume lot of power.

The current invention discloses the optimization and scheduling methods of multi-stage hierarchical networks with fast scheduling of connections, for practical routing applications of numerous types of multi-stage networks also using multi-drop links. The

optimizations disclosed in the current invention are applicable to including the numerous generalized multi-stage networks disclosed in the following patent applications:

1) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-stage networks $V(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,270,400 that is incorporated by reference above.

2) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,170,040 that is incorporated by reference above.

3) Rearrangeably nonblocking for arbitrary fan-out multicast and unicast, and strictly nonblocking for unicast for generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$ and generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,363,649 that is incorporated by reference above.

4) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,170,040 that is incorporated by reference above.

5) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,363,649 that is incorporated by reference above.

6) Strictly nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$ and generalized folded multi-link

multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in the US Patent No. 8,363,649 that is incorporated by reference above.

7) VLSI layouts of numerous types of multi-stage networks are described in the US Patent No. 8,269,523 entitled "VLSI LAYOUTS OF FULLY CONNECTED NETWORKS" that is incorporated by reference above.

8) VLSI layouts of numerous types of multi-stage networks are described in the US Patent No. 8,898,611 entitled "VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED AND PYRAMID NETWORKS WITH LOCALITY EXPLOITATION" that is incorporated by reference above.

In addition the optimization with the VLSI layouts disclosed in the current invention are also applicable to generalized multi-stage pyramid networks $V_p(N_1, N_2, d, s)$, generalized folded multi-stage pyramid networks $V_{fold-p}(N_1, N_2, d, s)$, generalized butterfly fat pyramid networks $V_{bfp}(N_1, N_2, d, s)$, generalized multi-link multi-stage pyramid networks $V_{mlink-p}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage pyramid networks $V_{fold-mlink-p}(N_1, N_2, d, s)$, generalized multi-link butterfly fat pyramid networks $V_{mlink-bfp}(N_1, N_2, d, s)$, generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ and generalized cube connected cycles networks $V_{CCC}(N_1, N_2, d, s)$ for s = 1,2,3 or any number in general.

Finally the current invention discloses the optimizations and VLSI layouts of multi-stage hierarchical networks $V_{Comb}(N_1, N_2, d, s)$ and the optimizations and VLSI layouts of multi-stage hierarchical networks $V_{D-Comb}(N_1, N_2, d, s)$ for practical routing applications (particularly to set up broadcast, unicast and multicast connections), where "Comb" denotes the combination of and "D-Comb" denotes the delay optimized combination of any of the generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks

$V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, generalized multi-stage pyramid networks $V_p(N_1, N_2, d, s)$, generalized folded multi-stage pyramid networks $V_{fold-p}(N_1, N_2, d, s)$, generalized butterfly fat pyramid networks $V_{bfp}(N_1, N_2, d, s)$, generalized multi-link multi-stage pyramid networks $V_{mlink-p}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage pyramid networks $V_{fold-mlink-p}(N_1, N_2, d, s)$, generalized multi-link butterfly fat pyramid networks $V_{mlink-bfp}(N_1, N_2, d, s)$, generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$, and generalized cube connected cycles networks $V_{ccc}(N_1, N_2, d, s)$ for s = 1,2,3 or any number in general.

Multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$:

Referring to diagram 100A in FIG. 1A, in one embodiment, an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ where $N_1 = 200$; $N_2 = 400$; d = 2; and s = 1 corresponding to one computational block, with each computational block having 4 inlet links namely I1, I2, I3, and I4; and 2 outlet links namely O1 and O2. And for each computational block the corresponding partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists of two rings 110 and 120, where ring 110 consists of "m+1" stages namely (ring 1, stage 0), (ring 1, stage 1), … (ring 1, stage "m-1"), and (ring 1, stage "m"), and ring 120 consists of "n+1" stages namely (ring 2, stage 0), (ring 2, stage 1), … (ring 2, stage "n-1"), and (ring 2, stage "n"), where "m" and "n" are positive integers.

Ring 110 has inlet links Ri(1,1) and Ri(1,2), and has outlet links Bo(1,1) and Bo(1,2). Ring 120 has inlet links Fi(2,1) and Fi(2,2), and outlet links Bo(2,1) and Bo(2,2). And hence the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists of 4 inlet links and 4 outlet links corresponding to the two rings 110 and 120. Outlet link O1 of the computational block is connected to inlet link Ri(1,1) of ring 110 and also inlet link of Fi(2,1) of ring 120. Similarly outlet link O2 of the computational

block is connected to inlet link Ri(1,2) of Ring 110 and also inlet link of Fi(2,2) of Ring 120. And outlet link Bo(1,1) of Ring 110 is connected to inlet link I1 of the computational block. Outlet link Bo(1,2) of Ring 110 is connected to inlet link I2 of the computational block. Similarly outlet link Bo(2,1) of Ring 120 is connected to inlet link I3 of the computational block. Outlet link Bo(2,2) of Ring 120 is connected to inlet link I4 of the computational block. Since in this embodiment outlet link O1 of the computational block is connected to both inlet link Ri(1,1) of ring 110 and inlet link Fi(2,1) of ring 120; and outlet link O2 of the computational block is connected to both inlet link Ri(1,2) of ring 110 and inlet link Fi(2,2) of ring 120, the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists of 2 inlet links and 4 outlet links.

The two dimensional grid 800 in FIG. 8 illustrates an exemplary arrangement of 100 blocks arranged in 10 rows and 10 columns, in an embodiment. Each row of 2D-grid consisting of 10 block numbers namely the first row consists of the blocks (1,1), (1,2), (1,3), … , (1,9), and (1,10). The second row consists of the blocks (2,1), (2,2), (2,3), … , (2,9), and (2,10). Similarly 2D-grid 800 consists of 10 rows of each with 10 blocks and finally the tenth row consists of the blocks (10,1), (10,2), (10,3), … , (10,9), and (10,10). Each block of 2D-grid 800, in one embodiment, is part of the die area of a semiconductor integrated circuit, so that the complete 2D-grid 800 of 100 blocks represents the complete die of the semiconductor integrated circuit. In one embodiment, each block of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A with 2 inlet links and 4 outlet links and the corresponding computational block with 4 inlet links and 2 outlet links. For example block (1,1) of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A with 2 inlet links and 4 outlet links and the corresponding computational block with 4 inlet links and 2 outlet links. Similarly each of the 100 blocks of 2D-grid 800 has a separate partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A with 2 inlet links and 4 outlet links and the corresponding computational block with 4 inlet links and 2 outlet links. Hence the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to 2D-grid 800 has $N_1 = 200$ inlet links and $N_2 = 400$ outlet links. And there are 100 computational blocks each one

corresponding to one of the blocks with each computational block having 4 inlet links and 2 outlet links. Also the 2D-grid 800 is organized in the fourth quadrant of the 2D-Plane. In other embodiments the 2D-grid 800 may be organized as either first quadrant, or second quadrant or third quadrant of the 2D-Plane.

Referring to partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A in FIG. 1A, the stage (ring 1, stage 0) consists of 4 inputs namely Ri(1,1), Ri(1,2), Ui(1,1), and Ui(1,2); and 4 outputs Bo(1,1), Bo(1,2), Fo(1,1), and Fo(1,2). The stage (ring 1, stage 0) also consists of eight 2:1 multiplexers (A multiplexer is hereinafter called a "mux") namely R(1,1), R(1,2), F(1,1), F(1,2), U(1,1), U(1,2), B(1,1), and B(1,2). The 2:1 Mux R(1,1) has two inputs namely Ri(1,1) and Bo(1,1) and has one output Ro(1,1). The 2:1 Mux R(1,2) has two inputs namely Ri(1,2) and Bo(1,2) and has one output Ro(1,2). The 2:1 Mux F(1,1) has two inputs namely Ro(1,1) and Ro(1,2) and has one output Fo(1,1). The 2:1 Mux F(1,2) has two inputs namely Ro(1,1) and Ro(1,2) and has one output Fo(1,2).

The 2:1 Mux U(1,1) has two inputs namely Ui(1,1) and Fo(1,1) and has one output Uo(1,1). The 2:1 Mux U(1,2) has two inputs namely Ui(1,2) and Fo(1,2) and has one output Uo(1,2). The 2:1 Mux B(1,1) has two inputs namely Uo(1,1) and Uo(1,2) and has one output Bo(1,1). The 2:1 Mux B(1,2) has two inputs namely Uo(1,1) and Uo(1,2) and has one output Bo(1,2).

The stage (ring 1, stage 1) consists of 4 inputs namely Ri(1,3), Ri(1,4), Ui(1,3), and Ui(1,4); and 4 outputs Bo(1,3), Bo(1,4), Fo(1,3), and Fo(1,4). The stage (ring 1, stage 1) also consists of eight 2:1 Muxes namely R(1,3), R(1,4), F(1,3), F(1,4), U(1,3), U(1,4), B(1,3), and B(1,4). The 2:1 Mux R(1,3) has two inputs namely Ri(1,3) and Bo(1,3) and has one output Ro(1,3). The 2:1 Mux R(1,4) has two inputs namely Ri(1,4) and Bo(1,4) and has one output Ro(1,4). The 2:1 Mux F(1,3) has two inputs namely Ro(1,3) and Ro(1,4) and has one output Fo(1,3). The 2:1 Mux F(1,4) has two inputs namely Ro(1,3) and Ro(1,4) and has one output Fo(1,4).

The 2:1 Mux U(1,3) has two inputs namely Ui(1,3) and Fo(1,3) and has one output Uo(1,3). The 2:1 Mux U(1,4) has two inputs namely Ui(1,4) and Fo(1,4) and has

one output Uo(1,4). The 2:1 Mux B(1,3) has two inputs namely Uo(1,3) and Uo(1,4) and has one output Bo(1,3). The 2:1 Mux B(1,4) has two inputs namely Uo(1,3) and Uo(1,4) and has one output Bo(1,4).

The output Fo(1,1) of the stage (ring 1, stage 0) is connected to the input Ri(1,3) of the stage (ring 1, stage 1) which is called hereinafter an internal connection between two successive stages of a ring. And the output Bo(1,3) of the stage (ring 1, stage 1) is connected to the input Ui(1,1) of the stage (ring 1, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1.

The stage (ring 1, stage "m-1") consists of 4 inputs namely Fi(1,2m-1), Fi(1,2m), Ui(1,2m-1), and Ui(1,2m); and 4 outputs Bo(1,2m-1), Bo(1,2m), Fo(1,2m-1), and Fo(1,2m). The stage (ring 1, stage "m-1') also consists of six 2:1 Muxes namely F(1,2m-1), F(1,2m), U(1,2m-1), U(1,2m), B(1,2m-1), and B(1,2m). The 2:1 Mux F(1,2m-1) has two inputs namely Fi(1,2m-1) and Fi(1,2m) and has one output Fo(1,2m-1). The 2:1 Mux F(1,2m) has two inputs namely Fi(1,2m-1) and Fi(1,2m) and has one output Fo(1,2m).

The 2:1 Mux U(1,2m-1) has two inputs namely Ui(1,2m-1) and Fo(1,2m-1) and has one output Uo(1,2m-1). The 2:1 Mux U(1,2m) has two inputs namely Ui(1,2m) and Fo(1,2m) and has one output Uo(1,2m). The 2:1 Mux B(1,2m-1) has two inputs namely Uo(1,2m-1) and Uo(1,2m) and has one output Bo(1,2m-1). The 2:1 Mux B(1,2m) has two inputs namely Uo(1,2m-1) and Uo(1,2m) and has one output Bo(1,2m).

The stage (ring 1, stage "m") consists of 4 inputs namely Fi(1,2m+1), Fi(1,2m+2), Ui(1,2m+1), and Ui(1,2m+2); and 4 outputs Bo(1,2m+1), Bo(1,2m+2), Fo(1,2m+1), and Fo(1,2m+2). The stage (ring 1, stage "m") also consists of six 2:1 Muxes namely F(1,2m+1), F(1,2m+2), U(1,2m+1), U(1,2m+2), B(1,2m+1), and B(1,2m+2). The 2:1 Mux F(1,2m+1) has two inputs namely Fi(1,2m+1) and Fi(1,2m+2) and has one output Fo(1,2m+1). The 2:1 Mux F(1,2m+2) has two inputs namely Fi(1,2m+1) and Fi(1,2m+2) and has one output Fo(1,2m+2).

The 2:1 Mux U(1,2m+1) has two inputs namely Ui(1,2m+1) and Fo(1,2m+1) and has one output Uo(1,2m+1). The 2:1 Mux U(1,2m+2) has two inputs namely Ui(1,2m+2) and Fo(1,2m+2) and has one output Uo(1,2m+2). The 2:1 Mux B(1,2m+1) has two inputs

namely Uo(1,2m+1) and Uo(1,2m+2) and has one output Bo(1,2m+1). The 2:1 Mux B(1,2m+2) has two inputs namely Uo(1,2m+1) and Uo(1,2m+2) and has one output Bo(1,2m+2).

The output Fo(1,2m-1) of the stage (ring 1, stage "m-1") is connected to the input Fi(1,2m+1) of the stage (ring 1, stage "m"), is an internal connection between stage "m-1" and stage "m" of the ring 1. And the output Bo(1,2m+1) of the stage (ring 1, stage "m") is connected to the input Ui(1,2m-1) of the stage (ring 1, stage "m-1"), is another internal connection between stage "m-1" and stage "m" of the ring 1

Just the same way the stages (ring 1, stage 0), (ring 1, stage 1), there are also stages (ring 1, stage 2), (ring 1, stage 3), … (ring 1, stage "m-1"), (ring 1, stage "m") in that order, where the stages from (ring 1, stage 2), (ring 1, stage 3), … , (ring 1, stage "m-2") are not shown in the diagram 100A. Just the same way the two successive stages (ring 1, stage 0) and (ring 1, stage 1) have internal connections between them as described before, any two successive stages have similar internal connections. For example (ring 1, stage 1) and (ring 1, stage 2) have similar internal connections and (ring 1, stage "m-2") and (ring 1, stage "m-1") have similar internal connections.

Stage (ring 1, stage 0) is also called hereinafter the "entry stage" or "first stage" of ring 1, since inlet links and outlet links of the computational block are directly connected to stage (ring 1, stage 0). Also stage (ring 1, stage "m") is hereinafter the "last stage" or "root stage" of ring 1.

The stage (ring 2, stage 0) consists of 4 inputs namely Fi(2,1), Fi(2,2), Ui(2,1), and Ui(2,2); and 4 outputs Bo(2,1), Bo(2,2), Fo(2,1), and Fo(2,2). The stage (ring 2, stage 0) also consists of six 2:1 Muxes namely F(2,1), F(2,2), U(2,1), U(2,2), B(2,1), and B(2,2). The 2:1 Mux F(2,1) has two inputs namely Fi(2,1) and Fi(2,2) and has one output Fo(2,1). The 2:1 Mux F(2,2) has two inputs namely Fi(2,1) and Fi(2,2) and has one output Fo(2,2).

The 2:1 Mux U(2,1) has two inputs namely Ui(2,1) and Fo(2,1) and has one output Uo(2,1). The 2:1 Mux U(2,2) has two inputs namely Ui(2,2) and Fo(2,2) and has one output Uo(2,2). The 2:1 Mux B(2,1) has two inputs namely Uo(2,1) and Uo(2,2) and

has one output Bo(2,1). The 2:1 Mux B(2,2) has two inputs namely Uo(2,1) and Uo(2,2) and has one output Bo(2,2).

The stage (ring 2, stage 1) consists of 4 inputs namely Fi(2,3), Fi(2,4), Ui(2,3), and Ui(2,4); and 4 outputs Bo(2,3), Bo(2,4), Fo(2,3), and Fo(2,4). The stage (ring 2, stage 1) also consists of six 2:1 Muxes namely F(2,3), F(2,4), U(2,3), U(2,4), B(2,3), and B(2,4). The 2:1 Mux F(2,3) has two inputs namely Fi(2,3) and Fi(2,4) and has one output Fo(2,3). The 2:1 Mux F(2,4) has two inputs namely Fi(2,3) and Fi(2,4) and has one output Fo(2,4).

The 2:1 Mux U(2,3) has two inputs namely Ui(2,3) and Fo(2,3) and has one output Uo(2,3). The 2:1 Mux U(2,4) has two inputs namely Ui(2,4) and Fo(2,4) and has one output Uo(2,4). The 2:1 Mux B(2,3) has two inputs namely Uo(2,3) and Uo(2,4) and has one output Bo(2,3). The 2:1 Mux B(2,4) has two inputs namely Uo(2,3) and Uo(2,4) and has one output Bo(2,4).

The output Fo(2,1) of the stage (ring 2, stage 0) is connected to the input Fi(2,3) of the stage (ring 2, stage 1), is an internal connection between stage 0 and stage 1 of the ring 2. And the output Bo(2,3) of the stage (ring 2, stage 1) is connected to the input Ui(2,1) of the stage (ring 2, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1..

The stage (ring 2, stage "n-1") consists of 4 inputs namely Ri(2,2n-1), Ri(2,2n), Ui(1,2n-1), and Ui(1,2n); and 4 outputs Bo(1,2n-1), Bo(1,2n), Fo(1,2n-1), and Fo(1,2n). The stage (ring 2, stage "n-1') also consists of eight 2:1 Muxes namely R(2,2n-1), R(2,2n), F(2,2n-1), F(1,2n), U(1,2n-1), U(1,2n), B(1,2n-1), and B(1,2n). The 2:1 Mux R(2,2n-1) has two inputs namely Ri(2,2n-1) and Bo(2,2n-1) and has one output Ro(2,2n-1). The 2:1 Mux R(2,2n) has two inputs namely Ri(2,2n) and Bo(2,2n) and has one output Ro(2,2n). The 2:1 Mux F(2,2n-1) has two inputs namely Ro(2,2n-1) and Ro(2,2n) and has one output Fo(2,2n-1). The 2:1 Mux F(2,2n) has two inputs namely Ro(2,2n-1) and Ro(2,2n) and has one output Fo(2,2n).

The 2:1 Mux U(2,2n-1) has two inputs namely Ui(2,2n-1) and Fo(2,2n-1) and has one output Uo(2,2n-1). The 2:1 Mux U(2,2n) has two inputs namely Ui(2,2n) and

Fo(2,2n) and has one output Uo(2,2n). The 2:1 Mux B(2,2n-1) has two inputs namely Uo(2,2n-1) and Uo(2,2n) and has one output Bo(2,2n-1). The 2:1 Mux B(2,2n) has two inputs namely Uo(2,2n-1) and Uo(2,2n) and has one output Bo(2,2n).

The stage (ring 2, stage "n") consists of 4 inputs namely Ri(2,2n+1), Ri(2,2n+2), Ui(2,2n+1), and Ui(2,2n+2); and 4 outputs Bo(2,2n+1), Bo(2,2n+2), Fo(2,2n+1), and Fo(2,2n+2). The stage (ring 2, stage "n") also consists of eight 2:1 Muxes namely R(2,2n+1), R(2,2n+2), F(2,2n+1), F(2,2n+2), U(2,2n+1), U(2,2n+2), B(2,2n+1), and B(2,2n+2). The 2:1 Mux R(2,2n+1) has two inputs namely Ri(2,2n+1) and Bo(2,2n+1) and has one output Ro(2,2n+1). The 2:1 Mux R(2,2n+2) has two inputs namely Ri(2,2n+2) and Bo(2,2n+2) and has one output Ro(2,2n+2). The 2:1 Mux F(2,2n+1) has two inputs namely Ro(2,2n+1) and Ro(2,2n+2) and has one output Fo(2,2n+1). The 2:1 Mux F(2,2n+2) has two inputs namely Ro(2,2n+1) and Ro(2,2n+2) and has one output Fo(2,2n+2).

The 2:1 Mux U(2,2n+1) has two inputs namely Ui(2,2n+1) and Fo(2,2n+1) and has one output Uo(2,2n+1). The 2:1 Mux U(2,2n+2) has two inputs namely Ui(2,2n+2) and Fo(2,2n+2) and has one output Uo(2,2n+2). The 2:1 Mux B(2,2n+1) has two inputs namely Uo(2,2n+1) and Uo(2,2n+2) and has one output Bo(2,2n+1). The 2:1 Mux B(2,2n+2) has two inputs namely Uo(2,2n+1) and Uo(2,2n+2) and has one output Bo(2,2n+2).

The output Fo(2,2n-1) of the stage (ring 2, stage "n-1") is connected to the input Ri(2,2n+1) of the stage (ring 2, stage "n"), is an internal connection between stage "n-1" and stage "n" of the ring 1. And the output Bo(2,2n+1) of the stage (ring 2, stage "n") is connected to the input Ui(2,2n-1) of the stage (ring 2, stage "n-1"), is another internal connection between stage "n-1" and stage "n" of the ring 1.

Each stage of any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A consists of 4 inputs and $2*d = 4$ outputs. Even though the stages (ring 1, stage 0), (ring 1, stage 1), (ring 2, stage "n-1"), and (ring 2, stage "n") each have eight 2:1 muxes, and the stages (ring 2, stage 0), (ring 2, stage 1), (ring 1, stage "m-1"), and (ring 1, stage "m") each have six 2:1 muxes, in other embodiments any

of these stages can be one of the four by four switch diagrams namely 200A of FIG. 2A, 200B of FIG. 2B, 200C of FIG. 2C, and one of the eight by four switch diagrams namely 200E of FIG. 2E, 200F of FIG. 2F.

Referring to diagram 100B in FIG. 1B, in one embodiment, an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ where $N_1 = 400$; $N_2 = 800$; $d = 2$; and $s = 1$ corresponding to one computational block, with each computational block having 8 inlet links namely I1, I2, I3, I4, I5, I6, I7, and I8; and 4 outlet links namely O1, O2, O3, and O4. And for each computational block the corresponding partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of two rings 110 and 120, where ring 110 consists of "m+1" stages namely (ring 1, stage 0), (ring 1, stage 1), … (ring 1, stage "m-1"), and (ring 1, stage "m"), and ring 120 consists of "n+1" stages namely (ring 2, stage 0), (ring 2, stage 1), … (ring 2, stage "n-1"), and (ring 2, stage "n"), where "m" and "n" are positive integers.

Ring 110 has inlet links Ri(1,1) and Ri(1,2) from the left-hand side, and has outlet links Bo(1,1) and Bo(1,2) from left-hand side. Ring 110 also has inlet links Ui(1,2m+1) and Ui(1,2m+2) from the right-hand side, and has outlet links Fo(1,2m+1) and Fo(1,2m+2) from right-hand side. Ring 120 has inlet links Fi(2,1) and Fi(2,2) from left-hand side, and outlet links Bo(2,1) and Bo(2,2) from left-hand side. Ring 120 also has inlet links Ui(2,2n+1) and Ui(2,2n+2) from the right-hand side, and has outlet links Fo(2,2n+1) and Fo(2,2n+2) from right-hand side.

And the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of 8 inlet links and 4 outlet links corresponding to the two rings 110 and 120. From left-hand side, outlet link O1 of the computational block is connected to inlet link Ri(1,1) of ring 110 and also inlet link of Fi(2,1) of ring 120. Similarly from left-hand side, outlet link O2 of the computational block is connected to inlet link Ri(1,2) of Ring 110 and also inlet link of Fi(2,2) of Ring 120. And from left-hand side, outlet link Bo(1,1) of Ring 110 is connected to inlet link I1 of the computational block. From left-hand side, Outlet link Bo(1,2) of Ring 110 is connected to inlet link I2 of the computational block. Similarly from left-hand side, outlet link Bo(2,1) of Ring 120 is connected to inlet link I3 of the

computational block. From left-hand side, outlet link Bo(2,2) of Ring 120 is connected to inlet link I4 of the computational block.

From right-hand side, outlet link O3 of the computational block is connected to inlet link Ui(1,2m+1) of ring 110 and also inlet link of Ui(2,2n+1) of ring 120. Similarly from right-hand side, outlet link O4 of the computational block is connected to inlet link Ui(1,2m+2) of Ring 110 and also inlet link of Ui(2,2n+2) of Ring 120. And from right-hand side, outlet link Fo(1,2m+1) of Ring 110 is connected to inlet link I5 of the computational block. From right-hand side, outlet link Fo(1,2m+2) of Ring 110 is connected to inlet link I6 of the computational block. Similarly from right-hand side, outlet link Fo(2,2n+1) of Ring 120 is connected to inlet link I7 of the computational block. From right-hand side, outlet link Fo(2,2n+2) of Ring 120 is connected to inlet link I8 of the computational block.

Since in this embodiment outlet link O1 of the computational block is connected to both inlet link Ri(1,1) of ring 110 and inlet link Fi(2,1) of ring 120; outlet link O2 of the computational block is connected to both inlet link Ri(1,2) of ring 110 and inlet link Fi(2,2) of ring 120; outlet link O3 of the computational block is connected to both inlet link Ui(1,2m+1) of ring 110 and inlet link Ui(2,2n+1) of ring 120; and outlet link O4 of the computational block is connected to both inlet link Ui(1,2m+2) of ring 110 and inlet link Ui(2,2n+2) of ring 120, the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of 4 inlet links and 8 outlet links.

Referring to two dimensional grid 800 in FIG. 8 illustrates, in another embodiment, each block of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B with 4 inlet links and 8 outlet links and the corresponding computational block with 8 inlet links and 4 outlet links. For example block (1,1) of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B with 4 inlet links and 8 outlet links and the corresponding computational block with 8 inlet links and 4 outlet links. Similarly each of the 100 blocks of 2D-grid 800 has a separate partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B with 4 inlet links and 8 outlet links and the corresponding

computational block with 8 inlet links and 4 outlet links. Hence the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to 2D-grid 800 has $N_1 = 400$ inlet links and $N_2 = 800$ outlet links. Since there are 100 computational blocks each one corresponding to one of the blocks with each computational block having 8 inlet links and 4 outlet links. Also the 2D-grid 800 is organized in the fourth quadrant of the 2D-Plane. In other embodiments the 2D-grid 800 may be organized as either first quadrant, or second quadrant or third quadrant of the 2D-Plane.

Referring to partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B in FIG. 1B, the stage (ring 1, stage 0) consists of 4 inputs namely Ri(1,1), Ri(1,2), Ui(1,1), and Ui(1,2); and 4 outputs Bo(1,1), Bo(1,2), Fo(1,1), and Fo(1,2). The stage (ring 1, stage 0) also consists of eight 2:1 multiplexers (A multiplexer is hereinafter called a "mux") namely R(1,1), R(1,2), F(1,1), F(1,2), U(1,1), U(1,2), B(1,1), and B(1,2). The 2:1 Mux R(1,1) has two inputs namely Ri(1,1) and Bo(1,1) and has one output Ro(1,1). The 2:1 Mux R(1,2) has two inputs namely Ri(1,2) and Bo(1,2) and has one output Ro(1,2). The 2:1 Mux F(1,1) has two inputs namely Ro(1,1) and Ro(1,2) and has one output Fo(1,1). The 2:1 Mux F(1,2) has two inputs namely Ro(1,1) and Ro(1,2) and has one output Fo(1,2).

The 2:1 Mux U(1,1) has two inputs namely Ui(1,1) and Fo(1,1) and has one output Uo(1,1). The 2:1 Mux U(1,2) has two inputs namely Ui(1,2) and Fo(1,2) and has one output Uo(1,2). The 2:1 Mux B(1,1) has two inputs namely Uo(1,1) and Uo(1,2) and has one output Bo(1,1). The 2:1 Mux B(1,2) has two inputs namely Uo(1,1) and Uo(1,2) and has one output Bo(1,2).

The stage (ring 1, stage 1) consists of 4 inputs namely Ri(1,3), Ri(1,4), Ui(1,3), and Ui(1,4); and 4 outputs Bo(1,3), Bo(1,4), Fo(1,3), and Fo(1,4). The stage (ring 1, stage 1) also consists of eight 2:1 Muxes namely R(1,3), R(1,4), F(1,3), F(1,4), U(1,3), U(1,4), B(1,3), and B(1,4). The 2:1 Mux R(1,3) has two inputs namely Ri(1,3) and Bo(1,3) and has one output Ro(1,3). The 2:1 Mux R(1,4) has two inputs namely Ri(1,4) and Bo(1,4) and has one output Ro(1,4). The 2:1 Mux F(1,3) has two inputs namely Ro(1,3) and

Ro(1,4) and has one output Fo(1,3). The 2:1 Mux F(1,4) has two inputs namely Ro(1,3) and Ro(1,4) and has one output Fo(1,4).

The 2:1 Mux U(1,3) has two inputs namely Ui(1,3) and Fo(1,3) and has one output Uo(1,3). The 2:1 Mux U(1,4) has two inputs namely Ui(1,4) and Fo(1,4) and has one output Uo(1,4). The 2:1 Mux B(1,3) has two inputs namely Uo(1,3) and Uo(1,4) and has one output Bo(1,3). The 2:1 Mux B(1,4) has two inputs namely Uo(1,3) and Uo(1,4) and has one output Bo(1,4).

The output Fo(1,1) of the stage (ring 1, stage 0) is connected to the input Ri(1,3) of the stage (ring 1, stage 1) which is called hereinafter an internal connection between two successive stages of a ring. And the output Bo(1,3) of the stage (ring 1, stage 1) is connected to the input Ui(1,1) of the stage (ring 1, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1.

The stage (ring 1, stage "m-1") consists of 4 inputs namely Fi(1,2m-1), Fi(1,2m), Ui(1,2m-1), and Ui(1,2m); and 4 outputs Bo(1,2m-1), Bo(1,2m), Fo(1,2m-1), and Fo(1,2m). The stage (ring 1, stage "m-1') also consists of six 2:1 Muxes namely F(1,2m-1), F(1,2m), U(1,2m-1), U(1,2m), B(1,2m-1), and B(1,2m). The 2:1 Mux F(1,2m-1) has two inputs namely Fi(1,2m-1) and Fi(1,2m) and has one output Fo(1,2m-1). The 2:1 Mux F(1,2m) has two inputs namely Fi(1,2m-1) and Fi(1,2m) and has one output Fo(1,2m).

The 2:1 Mux U(1,2m-1) has two inputs namely Ui(1,2m-1) and Fo(1,2m-1) and has one output Uo(1,2m-1). The 2:1 Mux U(1,2m) has two inputs namely Ui(1,2m) and Fo(1,2m) and has one output Uo(1,2m). The 2:1 Mux B(1,2m-1) has two inputs namely Uo(1,2m-1) and Uo(1,2m) and has one output Bo(1,2m-1). The 2:1 Mux B(1,2m) has two inputs namely Uo(1,2m-1) and Uo(1,2m) and has one output Bo(1,2m).

The stage (ring 1, stage "m") consists of 4 inputs namely Fi(1,2m+1), Fi(1,2m+2), Ui(1,2m+1), and Ui(1,2m+2); and 4 outputs Bo(1,2m+1), Bo(1,2m+2), Fo(1,2m+1), and Fo(1,2m+2). The stage (ring 1, stage "m") also consists of six 2:1 Muxes namely F(1,2m+1), F(1,2m+2), U(1,2m+1), U(1,2m+2), B(1,2m+1), and B(1,2m+2). The 2:1 Mux F(1,2m+1) has two inputs namely Fi(1,2m+1) and Fi(1,2m+2) and has one output

Fo(1,2m+1). The 2:1 Mux F(1,2m+2) has two inputs namely Fi(1,2m+1) and Fi(1,2m+2) and has one output Fo(1,2m+2).

The 2:1 Mux U(1,2m+1) has two inputs namely Ui(1,2m+1) and Fo(1,2m+1) and has one output Uo(1,2m+1). The 2:1 Mux U(1,2m+2) has two inputs namely Ui(1,2m+2) and Fo(1,2m+2) and has one output Uo(1,2m+2). The 2:1 Mux B(1,2m+1) has two inputs namely Uo(1,2m+1) and Uo(1,2m+2) and has one output Bo(1,2m+1). The 2:1 Mux B(1,2m+2) has two inputs namely Uo(1,2m+1) and Uo(1,2m+2) and has one output Bo(1,2m+2).

The output Fo(1,2m-1) of the stage (ring 1, stage "m-1") is connected to the input Fi(1,2m+1) of the stage (ring 1, stage "m"), is an internal connection between stage "m-1" and stage "m" of the ring 1. And the output Bo(1,2m+1) of the stage (ring 1, stage "m") is connected to the input Ui(1,2m-1) of the stage (ring 1, stage "m-1"), is another internal connection between stage "m-1" and stage "m" of the ring 1

Just the same way the stages (ring 1, stage 0), (ring 1, stage 1), there are also stages (ring 1, stage 2), (ring 1, stage 3), … (ring 1, stage "m-1"), (ring 1, stage "m") in that order, where the stages from (ring 1, stage 2), (ring 1, stage 3), … , (ring 1, stage "m-2") are not shown in the diagram 100B. Just the same way the two successive stages (ring 1, stage 0) and (ring 1, stage 1) have internal connections between them as described before, any two successive stages have similar internal connections. For example (ring 1, stage 1) and (ring 1, stage 2) have similar internal connections and (ring 1, stage "m-2") and (ring 1, stage "m-1") have similar internal connections.

Stage (ring 1, stage 0) is also called hereinafter the "entry stage" or "first stage" of ring 1, since inlet links and outlet links of the computational block are directly connected to stage (ring 1, stage 0). Also stage (ring 1, stage "m") is hereinafter the "last stage" or "root stage" of ring 1.

The stage (ring 2, stage 0) consists of 4 inputs namely Fi(2,1), Fi(2,2), Ui(2,1), and Ui(2,2); and 4 outputs Bo(2,1), Bo(2,2), Fo(2,1), and Fo(2,2). The stage (ring 2, stage 0) also consists of six 2:1 Muxes namely F(2,1), F(2,2), U(2,1), U(2,2), B(2,1), and B(2,2). The 2:1 Mux F(2,1) has two inputs namely Fi(2,1) and Fi(2,2) and has one output

Fo(2,1). The 2:1 Mux F(2,2) has two inputs namely Fi(2,1) and Fi(2,2) and has one output Fo(2,2).

The 2:1 Mux U(2,1) has two inputs namely Ui(2,1) and Fo(2,1) and has one output Uo(2,1). The 2:1 Mux U(2,2) has two inputs namely Ui(2,2) and Fo(2,2) and has one output Uo(2,2). The 2:1 Mux B(2,1) has two inputs namely Uo(2,1) and Uo(2,2) and has one output Bo(2,1). The 2:1 Mux B(2,2) has two inputs namely Uo(2,1) and Uo(2,2) and has one output Bo(2,2).

The stage (ring 2, stage 1) consists of 4 inputs namely Fi(2,3), Fi(2,4), Ui(2,3), and Ui(2,4); and 4 outputs Bo(2,3), Bo(2,4), Fo(2,3), and Fo(2,4). The stage (ring 2, stage 1) also consists of six 2:1 Muxes namely F(2,3), F(2,4), U(2,3), U(2,4), B(2,3), and B(2,4). The 2:1 Mux F(2,3) has two inputs namely Fi(2,3) and Fi(2,4) and has one output Fo(2,3). The 2:1 Mux F(2,4) has two inputs namely Fi(2,3) and Fi(2,4) and has one output Fo(2,4).

The 2:1 Mux U(2,3) has two inputs namely Ui(2,3) and Fo(2,3) and has one output Uo(2,3). The 2:1 Mux U(2,4) has two inputs namely Ui(2,4) and Fo(2,4) and has one output Uo(2,4). The 2:1 Mux B(2,3) has two inputs namely Uo(2,3) and Uo(2,4) and has one output Bo(2,3). The 2:1 Mux B(2,4) has two inputs namely Uo(2,3) and Uo(2,4) and has one output Bo(2,4).

The output Fo(2,1) of the stage (ring 2, stage 0) is connected to the input Fi(2,3) of the stage (ring 2, stage 1), is an internal connection between stage 0 and stage 1 of the ring 2. And the output Bo(2,3) of the stage (ring 2, stage 1) is connected to the input Ui(2,1) of the stage (ring 2, stage 0), is another internal connection between stage 0 and stage 1 of the ring 1..

The stage (ring 2, stage "n-1") consists of 4 inputs namely Ri(2,2n-1), Ri(2,2n), Ui(1,2n-1), and Ui(1,2n); and 4 outputs Bo(1,2n-1), Bo(1,2n), Fo(1,2n-1), and Fo(1,2n). The stage (ring 2, stage "n-1') also consists of eight 2:1 Muxes namely R(2,2n-1), R(2,2n), F(2,2n-1), F(1,2n), U(1,2n-1), U(1,2n), B(1,2n-1), and B(1,2n). The 2:1 Mux R(2,2n-1) has two inputs namely Ri(2,2n-1) and Bo(2,2n-1) and has one output Ro(2,2n-1). The 2:1 Mux R(2,2n) has two inputs namely Ri(2,2n) and Bo(2,2n) and has one output

Ro(2,2n). The 2:1 Mux F(2,2n-1) has two inputs namely Ro(2,2n-1) and Ro(2,2n) and has one output Fo(2,2n-1). The 2:1 Mux F(2,2n) has two inputs namely Ro(2,2n-1) and Ro(2,2n) and has one output Fo(2,2n).

The 2:1 Mux U(2,2n-1) has two inputs namely Ui(2,2n-1) and Fo(2,2n-1) and has one output Uo(2,2n-1). The 2:1 Mux U(2,2n) has two inputs namely Ui(2,2n) and Fo(2,2n) and has one output Uo(2,2n). The 2:1 Mux B(2,2n-1) has two inputs namely Uo(2,2n-1) and Uo(2,2n) and has one output Bo(2,2n-1). The 2:1 Mux B(2,2n) has two inputs namely Uo(2,2n-1) and Uo(2,2n) and has one output Bo(2,2n).

The stage (ring 2, stage "n") consists of 4 inputs namely Ri(2,2n+1), Ri(2,2n+2), Ui(2,2n+1), and Ui(2,2n+2); and 4 outputs Bo(2,2n+1), Bo(2,2n+2), Fo(2,2n+1), and Fo(2,2n+2). The stage (ring 2, stage "n") also consists of eight 2:1 Muxes namely R(2,2n+1), R(2,2n+2), F(2,2n+1), F(2,2n+2), U(2,2n+1), U(2,2n+2), B(2,2n+1), and B(2,2n+2). The 2:1 Mux R(2,2n+1) has two inputs namely Ri(2,2n+1) and Bo(2,2n+1) and has one output Ro(2,2n+1). The 2:1 Mux R(2,2n+2) has two inputs namely Ri(2,2n+2) and Bo(2,2n+2) and has one output Ro(2,2n+2). The 2:1 Mux F(2,2n+1) has two inputs namely Ro(2,2n+1) and Ro(2,2n+2) and has one output Fo(2,2n+1). The 2:1 Mux F(2,2n+2) has two inputs namely Ro(2,2n+1) and Ro(2,2n+2) and has one output Fo(2,2n+2).

The 2:1 Mux U(2,2n+1) has two inputs namely Ui(2,2n+1) and Fo(2,2n+1) and has one output Uo(2,2n+1). The 2:1 Mux U(2,2n+2) has two inputs namely Ui(2,2n+2) and Fo(2,2n+2) and has one output Uo(2,2n+2). The 2:1 Mux B(2,2n+1) has two inputs namely Uo(2,2n+1) and Uo(2,2n+2) and has one output Bo(2,2n+1). The 2:1 Mux B(2,2n+2) has two inputs namely Uo(2,2n+1) and Uo(2,2n+2) and has one output Bo(2,2n+2).

The output Fo(2,2n-1) of the stage (ring 2, stage "n-1") is connected to the input Ri(2,2n+1) of the stage (ring 2, stage "n"), is an internal connection between stage "n-1" and stage "n" of the ring 1. And the output Bo(2,2n+1) of the stage (ring 2, stage "n") is connected to the input Ui(2,2n-1) of the stage (ring 2, stage "n-1"), is another internal connection between stage "n-1" and stage "n" of the ring 1.

Each stage of any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of $2 * d = 4$ outputs. Even though each stage has four 4:1 muxes, in other embodiments any of these stages can be one of the four by four switch diagrams namely 200A of FIG. 2A, 200B of FIG. 2B, 200C of FIG. 2C, and one of the eight by four switch diagrams namely 200E of FIG. 2E, 200F of FIG. 2F.

In general, any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ may have inputs and outputs connected from computational block from either only from left-hand side as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A; or only from right-hand side; or from both left-hand and right-hand sides as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B.

Referring to diagram 100C in FIG. 1C, in one embodiment, an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ where $N_1 = 400$; $N_2 = 1600$; $d = 2$; and $s = 1$ corresponding to one computational block, with each computational block having 16 inlet links namely I1, I2, I3, I4, I5, I6, I7, I8, I9, I10, I11, I12, I13, I14, I15, and I16 ; and 4 outlet links namely O1, O2, O3, and O4. And for each computational block the corresponding partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C consists of two slices namely slice 1 and slice 2. Slice 1 consists of two rings namely (slice 1, ring 1) and (slice 1, ring 2). Similarly slice 2 consists of two rings namely (slice 2, ring 1) and (slice 2, ring 2).

The ring (slice 1, ring 1) consists of "m+1" stages namely (slice 1, ring 1, stage 0), (slice 1, ring 1, stage 1), … (slice 1, ring 1, stage "m-1"), and (slice 1, ring 1, stage "m"). And the ring (slice 1, ring 2) consists of "n+1" stages namely (slice 1, ring 2, stage 0), (slice 1, ring 2, stage 1), … (slice 1, ring 2, stage "n-1"), and (slice 1, ring 2, stage "n"), where "m" and "n" are positive integers.

Similarly the ring (slice 2, ring 1) consists of "x+1" stages namely (slice 2, ring 1, stage 0), (slice 2, ring 1, stage 1), … (slice 2, ring 1, stage "x-1"), and (slice 2, ring 1, stage "x"). And the ring (slice 2, ring 2) consists of "y+1" stages namely (slice 2, ring 2,

stage 0), (slice 2, ring 2, stage 1), … (slice 2, ring 2, stage "y-1"), and (slice 2, ring 2, stage "y"), where "x" and "y" are positive integers.

In general "m" may be or may not be equal to "x" and "n" may be or may not be equal to "y". Also in general, "m" may be or may not be equal to "n" and "x" may be or may not be equal to "y".

Ring (slice 1, ring 1) has inlet links Ri(1,1,1) and Ri(1,1,2) from the left-hand side, and has outlet links Bo(1,1,1) and Bo(1,1,2) from left-hand side. Ring (slice 1, ring 1) also has inlet links Ui(1,1,2m+1) and Ui(1,1,2m+2) from the right-hand side, and has outlet links Fo(1,1,2m+1) and Fo(1,1,2m+2) from right-hand side. Ring (slice 1, ring 2) has inlet links Ri(1,2,1) and Ri(1,2,2) from left-hand side, and outlet links Bo(1,2,1) and Bo(1,2,2) from left-hand side. Ring (slice 1, ring 2) also has inlet links Ui(1,2,2n+1) and Ui(1,2,2n+2) from the right-hand side, and has outlet links Fo(1,2,2n+1) and Fo(1,2,2n+2) from right-hand side.

Ring (slice 2, ring 1) has inlet links Ri(2,1,1) and Ri(2,1,2) from the left-hand side, and has outlet links Bo(2,1,1) and Bo(2,1,2) from left-hand side. Ring (slice 2, ring 1) also has inlet links Ui(2,1,2x+1) and Ui(2,1,2x+2) from the right-hand side, and has outlet links Fo(2,1,2x+1) and Fo(2,1,2x+2) from right-hand side. Ring (slice 2, ring 2) has inlet links Ri(2,2,1) and Ri(2,2,2) from left-hand side, and outlet links Bo(2,2,1) and Bo(2,2,2) from left-hand side. Ring (slice 2, ring 2) also has inlet links Ui(2,2,2y+1) and Ui(2,2,2y+2) from the right-hand side, and has outlet links Fo(2,2,2y+1) and Fo(2,2,2y+2) from right-hand side.

And the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C consists of 16 inlet links and 4 outlet links corresponding to the two slices slice 1 and slice 2. From left-hand side, outlet link O1 of the computational block is connected to inlet link Ri(1,1,1) of ring (slice 1, ring 1) and also inlet link of Ri(1,2,1) of ring (slice 1, ring 2). Similarly from left-hand side, outlet link O2 of the computational block is connected to inlet link Ri(1,1,2) of Ring (slice 1, ring 1) and also inlet link of Ri(1,2,2) of Ring (slice 1, ring 2). And from left-hand side, outlet link Bo(1,1,1) of Ring (slice 1, ring 1) is connected to inlet link I1 of the computational block. From left-hand side, Outlet link

Bo(1,1,2) of Ring (slice 1, ring 1) is connected to inlet link I2 of the computational block. Similarly from left-hand side, outlet link Bo(1,2,1) of Ring (slice 1, ring 2) is connected to inlet link I3 of the computational block. From left-hand side, outlet link Bo(1,2,2) of Ring (slice 1, ring 2) is connected to inlet link I4 of the computational block.

From right-hand side, outlet link O1 of the computational block is connected to inlet link Ui(1,1,2m+1) of ring (slice 1, ring 1) and also inlet link of Ui(1,2,2n+1) of ring (slice 1, ring 2). Similarly from right-hand side, outlet link O2 of the computational block is connected to inlet link Ui(1,1,2m+2) of Ring (slice 1, ring 1) and also inlet link of Ui(1,2,2n+2) of Ring (slice 1, ring 2). And from right-hand side, outlet link Fo(1,1,2m+1) of Ring (slice 1, ring 1) is connected to inlet link I5 of the computational block. From right-hand side, outlet link Fo(1,1,2m+2) of Ring (slice 1, ring 1) is connected to inlet link I6 of the computational block. Similarly from right-hand side, outlet link Fo(1,2,2n+1) of Ring (slice 1, ring 2) is connected to inlet link I7 of the computational block. From right-hand side, outlet link Fo(1,2,2n+2) of Ring (slice 1, ring 2) is connected to inlet link I8 of the computational block.

From left-hand side, outlet link O3 of the computational block is connected to inlet link Ri(2,1,1) of ring (slice 2, ring 1) and also inlet link of Ri(2,2,1) of ring (slice 2, ring 2). Similarly from left-hand side, outlet link O4 of the computational block is connected to inlet link Ri(2,1,2) of Ring (slice 2, ring 1) and also inlet link of Ri(2,2,2) of Ring (slice 2, ring 2). And from left-hand side, outlet link Bo(2,1,1) of Ring (slice 2, ring 1) is connected to inlet link I9 of the computational block. From left-hand side, Outlet link Bo(2,1,2) of Ring (slice 2, ring 1) is connected to inlet link I10 of the computational block. Similarly from left-hand side, outlet link Bo(2,2,1) of Ring (slice 2, ring 2) is connected to inlet link I11 of the computational block. From left-hand side, outlet link Bo(2,2,2) of Ring (slice 2, ring 2) is connected to inlet link I12 of the computational block.

From right-hand side, outlet link O3 of the computational block is connected to inlet link Ui(2,1,2x+1) of ring (slice 2, ring 1) and also inlet link of Ui(2,2,2y+1) of ring (slice 2, ring 2). Similarly from right-hand side, outlet link O4 of the computational block is connected to inlet link Ui(2,1,2x+2) of Ring (slice 2, ring 1) and also inlet link of

Ui(2,2,2y+2) of Ring (slice 2, ring 2). And from right-hand side, outlet link Fo(2,1,2x+1) of Ring (slice 2, ring 1) is connected to inlet link I13 of the computational block. From right-hand side, outlet link Fo(2,1,2x+2) of Ring (slice 2, ring 1) is connected to inlet link I14 of the computational block. Similarly from right-hand side, outlet link Fo(2,2,2y+1) of Ring (slice 2, ring 2) is connected to inlet link I15 of the computational block. From right-hand side, outlet link Fo(2,2,2y+2) of Ring (slice 2, ring 2) is connected to inlet link I16 of the computational block.

In this embodiment outlet links O1 and O2 of the computational block are connected only to slice 1. Similarly outlet links O3 and O4 of the computational block are connected only to slice 2.

Referring to two dimensional grid 800 in FIG. 8 illustrates, in another embodiment, each block of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C with 4 inlet links and 16 outlet links and the corresponding computational block with 16 inlet links and 4 outlet links. For example block (1,1) of 2D-grid 800 consists of one of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C with 4 inlet links and 16 outlet links and the corresponding computational block with 16 inlet links and 4 outlet links. Similarly each of the 100 blocks of 2D-grid 800 has a separate partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C with 4 inlet links and 16 outlet links and the corresponding computational block with 16 inlet links and 4 outlet links. Hence the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to 2D-grid 800 has $N_1 = 400$ inlet links and $N_2 = 1600$ outlet links. Since there are 100 computational blocks each one corresponding to one of the blocks with each computational block having 16 inlet links and 4 outlet links. Also the 2D-grid 800 is organized in the fourth quadrant of the 2D-Plane. In other embodiments the 2D-grid 800 may be organized as either first quadrant, or second quadrant or third quadrant of the 2D-Plane.

Referring to partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C, the stage (slice 1, ring 1, stage 0) consists of 8 inputs namely Ri(1,1,1), Ri(1,1,2), Ui(1,1,1), Ui(1,1,2), J(1,1,1), K(1,1,1), L(1,1,1), and M(1,1,1); and 4 outputs

Bo(1,1,1), Bo(1,1,2), Fo(1,1,1), and Fo(1,1,2). The stage (slice 1, ring "1", stage "0") also consists of four 4:1 Muxes namely F(1,1,1), F(1,1,2), B(1,1,1), and B(1,1,2). The 4:1 Mux F(1,1,1) has four inputs namely Ri(1,1,1), Ri(1,1,2), Ui(1,1,2), and J(1,1,1), and has one output Fo(1,1,1). The 4:1 Mux F(1,1,2) has four inputs namely Ri(1,1,1), Ri(1,1,2), Ui(1,1,1), and K(1,1,1), and has one output Fo(1,1,2).

The 4:1 Mux B(1,1,1) has four inputs namely Ui(1,1,1), Ui(1,1,2), Ri(1,1,2), and L(1,1,1), and has one output Bo(1,1,1). The 4:1 Mux B(1,1,2) has four inputs namely Ui(1,1,1), Ui(1,1,2), Ri(1,1,1) and M(1,1,1), and has one output Bo(1,1,2). In different embodiments the inputs J(1,1,1), K(1,1,1), L(1,1,1), and M(1,1,1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 1, ring 1, stage "m") consists of 8 inputs namely Ri(1,1,2m+1), Ri(1,1,2m+2), Ui(1,1,2m+1), Ui(1,1,2m+2), J(1,1,m+1), K(1,1,m+1), L(1,1,m+1), and M(1,1,m+1); and 4 outputs Bo(1,1,2m+1), Bo(1,1,2m+2), Fo(1,1,2m+1), and Fo(1,1,2m+2). The stage (slice 1, ring 1, stage "m") also consists of four 4:1 Muxes namely F(1,1,2m+1), F(1,1,2m+2), B(1,1,2m+1), and B(1,1,2m+2). The 4:1 Mux F(1,1,2m+1) has four inputs namely Ri(1,1,2m+1), Ri(1,1,2m+2), Ui(1,1,2m+2), and J(1,1,m+1), and has one output Fo(1,1,2m+1). The 4:1 Mux F(1,1,2m+2) has four inputs namely Ri(1,1,2m+1), Ri(1,1,2m+2), Ui(1,1,2m+1), and K(1,1,m+1), and has one output Fo(1,1,2m+2).

The 4:1 Mux B(1,1,2m+1) has four inputs namely Ui(1,1,2m+1), Ui(1,1,2m+2), Ri(1,1,2m+2), and L(1,1,m+1), and has one output Bo(1,1,2m+1). The 4:1 Mux B(1,1,2m+2) has four inputs namely Ui(1,1,2m+1), Ui(1,1,2m+2), Ri(1,1,2m+1) and M(1,1,m+1), and has one output Bo(1,1,2m+2). In different embodiments the inputs J(1,1,m+1), K(1,1,m+1), L(1,1,m+1), and M(1,1,m+1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 1, ring 1, stage 0), there are also stages (slice 1, ring 1, stage 1), (slice 1, ring 1, stage 2), (slice 1, ring 1, stage 3), … (slice 1, ring 1, stage

"m-1"), (slice 1, ring 1, stage "m") in that order, where the stages from (slice 1, ring 1, stage 1), (slice 1, ring 1, stage 2), … , (slice 1, ring 1, stage "m-1") are not shown in the diagram 100C.

Referring to diagram 100C5 in FIG. 1C5 illustrates specific details of partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C, particularly the internal connections between two successive stages of any ring of any slice, in one embodiment. The stage (slice "c", ring "d", stage "e") consists of 8 inputs namely Ri(c,d,2e+1), Ri(c,d,2e+2), Ui(c,d,2e+1), Ui(c,d,2e+2), J(c,d,e+1), K(c,d,e+1), L(c,d,e+1), and M(c,d,e+1); and 4 outputs Bo(c,d,2e+1), Bo(c,d,2e+2), Fo(c,d,2e+1), and Fo(c,d,2e+2). The stage (slice "c", ring "d", stage "e") also consists of four 4:1 Muxes namely F(c,d,2e+1), F(c,d,2e+2), B(c,d,2e+1), and B(c,d,2e+2). The 4:1 Mux F(c,d,2e+1) has four inputs namely Ri(c,d,2e+1), Ri(c,d,2e+2), Ui(c,d,2e+2), and J(c,d,e+1), and has one output Fo(c,d,2e+1). The 4:1 Mux F(c,d,2e+2) has four inputs namely Ri(c,d,2e+1), Ri(c,d,2e+2), Ui(c,d,2e+1), and K(c,d,e+1), and has one output Fo(c,d,2e+2).

The 4:1 Mux B(c,d,2e+1) has four inputs namely Ui(c,d,2e+1), Ui(c,d,2e+2), Ri(c,d,2e+2), and L(c,d,e+1), and has one output Bo(c,d,2e+1). The 4:1 Mux B(c,d,2e+2) has four inputs namely Ui(c,d,2e+1), Ui(c,d,2e+2), Ri(c,d,2e+1) and M(c,d,e+1), and has one output Bo(c,d,2e+2). In different embodiments the inputs J(c,d,e+1), K(c,d,e+1), L(c,d,e+1), and M(c,d,e+1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice "c", ring "d", stage "e+1") consists of 8 inputs namely Ri(c,d,2e+3), Ri(c,d,2e+4), Ui(c,d,2e+3), Ui(c,d,2e+4), J(c,d,e+2), K(c,d,e+2), L(c,d,e+2), and M(c,d,e+2); and 4 outputs Bo(c,d,2e+3), Bo(c,d,2e+4), Fo(c,d,2e+3), and Fo(c,d,2e+4). The stage (slice "c", ring "d", stage "e+1") also consists of four 4:1 Muxes namely F(c,d,2e+3), F(c,d,2e+4), B(c,d,2e+3), and B(c,d,2e+4). The 4:1 Mux F(c,d,2e+3) has four inputs namely Ri(c,d,2e+3), Ri(c,d,2e+4), Ui(c,d,2e+4), and J(c,d,e+2), and has one output Fo(c,d,2e+3). The 4:1 Mux F(c,d,2e+4) has four inputs namely Ri(c,d,2e+3), Ri(c,d,2e+4), Ui(c,d,2e+3), and K(c,d,e+2), and has one output Fo(c,d,2e+4).

The 4:1 Mux B(c,d,2e+3) has four inputs namely Ui(c,d,2e+3), Ui(c,d,2e+4), Ri(c,d,2e+4), and L(c,d,e+2), and has one output Bo(c,d,2e+3). The 4:1 Mux B(c,d,2e+4) has four inputs namely Ui(c,d,2e+3), Ui(c,d,2e+4), Ri(c,d,2e+3) and M(c,d,e+2), and has one output Bo(c,d,2e+4). In different embodiments the inputs J(c,d,e+2), K(c,d,e+2), L(c,d,e+2), and M(c,d,e+2) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The output Fo(c,d,2e+1) of the stage (slice "c", ring "d", stage "e") is connected to the input Ri(c,d,2e+3) of the stage (slice "c", ring "d", stage "e+1") which is called hereinafter an internal connection between two successive stages of a ring. And the output Bo(c,d,2e+3) of the stage (slice "c", ring "d", stage "e+1") is connected to the input Ui(c,d,2e+1) of the stage (slice "c", ring "d", stage "e"), is another internal connection between stage "e" and stage "e+1" of the ring (slice "c", ring "d").

Just the same way the two successive stages (slice "c', ring "d", stage "e") and (slice 'c", ring "d", stage "e+1") have internal connections between them as described above, any two successive stages have similar internal connections for any values of "c", "d", "e" of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C belonging to any block of the two dimensional grid 800 in FIG. 8, in some embodiments. For example stage (slice 1, ring 1, stage 0) and stage (slice 1, ring 1, stage 1) have similar internal connections; and stage (slice 1, ring 1, stage "m-1") and stage (slice 1, ring 1, stage "m") have similar internal connections.

Stage (slice 1, ring 1, stage 0) is also called hereinafter the "entry stage" or "first stage" of (slice 1, ring 1), since inlet links and outlet links of the computational block are directly connected to stage (slice 1, ring 1, stage 0). Also stage (slice 1, ring 1, stage "m") is hereinafter the "last stage" or "root stage" of (slice 1, ring 1).

The stage (slice 1, ring 2, stage 0) consists of 8 inputs namely Ri(1,2,1), Ri(1,2,2), Ui(1,2,1), Ui(1,2,2), J(1,2,1), K(1,2,1), L(1,2,1), and M(1,2,1); and 4 outputs Bo(1,2,1), Bo(1,2,2), Fo(1,2,1), and Fo(1,2,2). The stage (slice 1, ring "2", stage "0") also consists of four 4:1 Muxes namely F(1,2,1), F(1,2,2), B(1,2,1), and B(1,2,2). The 4:1 Mux F(1,2,1) has four inputs namely Ri(1,2,1), Ri(1,2,2), Ui(1,2,2), and J(1,2,1), and has one

output Fo(1,2,1). The 4:1 Mux F(1,2,2) has four inputs namely Ri(1,2,1), Ri(1,2,2), Ui(1,2,1), and K(1,2,1), and has one output Fo(1,2,2).

The 4:1 Mux B(1,2,1) has four inputs namely Ui(1,2,1), Ui(1,2,2), Ri(1,2,2), and L(1,2,1), and has one output Bo(1,2,1). The 4:1 Mux B(1,2,2) has four inputs namely Ui(1,2,1), Ui(1,2,2), Ri(1,2,1) and M(1,2,1), and has one output Bo(1,2,2). In different embodiments the inputs J(1,2,1), K(1,2,1), L(1,2,1), and M(1,2,1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 1, ring 2, stage "n") consists of 8 inputs namely Ri(1,2,2n+1), Ri(1,2,2n+2), Ui(1,2,2n+1), Ui(1,2,2n+2), J(1,2,n+1), K(1,2,n+1), L(1,2,n+1), and M(1,2,n+1); and 4 outputs Bo(1,2,2n+1), Bo(1,2,2n+2), Fo(1,2,2n+1), and Fo(1,2,2n+2). The stage (slice 1, ring 2, stage "n") also consists of four 4:1 Muxes namely F(1,2,2n+1), F(1,2,2n+2), B(1,2,2n+1), and B(1,2,2n+2). The 4:1 Mux F(1,2,2n+1) has four inputs namely Ri(1,2,2n+1), Ri(1,2,2n+2), Ui(1,2,2n+2), and J(1,2,n+1), and has one output Fo(1,2,2n+1). The 4:1 Mux F(1,2,2n+2) has four inputs namely Ri(1,2,2n+1), Ri(1,2,2n+2), Ui(1,2,2n+1), and K(1,2,n+1), and has one output Fo(1,2,2n+2).

The 4:1 Mux B(1,2,2n+1) has four inputs namely Ui(1,2,n+1), Ui(1,2,2n+2), Ri(1,2,2n+2), and L(1,2,n+1), and has one output Bo(1,2,2n+1). The 4:1 Mux B(1,2,2n+2) has four inputs namely Ui(1,2,2n+1), Ui(1,2,2n+2), Ri(1,2,2n+1) and M(1,2,n+1), and has one output Bo(1,2,2n+2). In different embodiments the inputs J(1,2,n+1), K(1,2,n+1), L(1,2,n+1), and M(1,2,n+1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 1, ring 2, stage 0), there are also stages (slice 1, ring 2, stage 1), (slice 1, ring 2, stage 2), (slice 1, ring 2, stage 3), … (slice 1, ring 2, stage "n-1"), (slice 1, ring 2, stage "n") in that order, where the stages from (slice 1, ring 2, stage 1), (slice 1, ring 2, stage 2), … , (slice 1, ring 2, stage "n-1") are not shown in the diagram 100C.

The stage (slice 2, ring 1, stage 0) consists of 8 inputs namely Ri(2,1,1), Ri(2,1,2), Ui(2,1,1), Ui(2,1,2), J(2,1,1), K(2,1,1), L(2,1,1), and M(2,1,1); and 4 outputs Bo(2,1,1), Bo(2,1,2), Fo(2,1,1), and Fo(2,1,2). The stage (slice 2, ring "1", stage "0") also consists of four 4:1 Muxes namely F(2,1,1), F(2,1,2), B(2,1,1), and B(2,1,2). The 4:1 Mux F(2,1,1) has four inputs namely Ri(2,1,1), Ri(2,1,2), Ui(2,1,2), and J(2,1,1), and has one output Fo(2,1,1). The 4:1 Mux F(2,1,2) has four inputs namely Ri(2,1,1), Ri(2,1,2), Ui(2,1,1), and K(2,1,1), and has one output Fo(2,1,2).

The 4:1 Mux B(2,1,1) has four inputs namely Ui(2,1,1), Ui(2,1,2), Ri(2,1,2), and L(2,1,1), and has one output Bo(2,1,1). The 4:1 Mux B(2,1,2) has four inputs namely Ui(2,1,1), Ui(2,1,2), Ri(2,1,1) and M(2,1,1), and has one output Bo(2,1,2). In different embodiments the inputs J(2,1,1), K(2,1,1), L(2,1,1), and M(2,1,1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 2, ring 1, stage "x") consists of 8 inputs namely Ri(2,1,2x+1), Ri(2,1,2x+2), Ui(2,1,2x+1), Ui(2,1,2x+2), J(2,1,x+1), K(2,1,x+1), L(2,1,x+1), and M(2,1,x+1); and 4 outputs Bo(2,1,2x+1), Bo(2,1,2x+2), Fo(2,1,2x+1), and Fo(2,1,2x+2). The stage (slice 2, ring 1, stage "x") also consists of four 4:1 Muxes namely F(2,1,2x+1), F(2,1,2x+2), B(2,1,2x+1), and B(2,1,2x+2). The 4:1 Mux F(2,1,2x+1) has four inputs namely Ri(2,1,2x+1), Ri(2,1,2x+2), Ui(2,1,2x+2), and J(2,1,x+1), and has one output Fo(2,1,2x+1). The 4:1 Mux F(2,1,2x+2) has four inputs namely Ri(2,1,2x+1), Ri(2,1,2x+2), Ui(2,1,2x+1), and K(2,1,x+1), and has one output Fo(2,1,2x+2).

The 4:1 Mux B(2,1,2x+1) has four inputs namely Ui(2,1,2x+1), Ui(2,1,2x+2), Ri(2,1,2x+2), and L(2,1,x+1), and has one output Bo(2,1,2x+1). The 4:1 Mux B(2,1,2x+2) has four inputs namely Ui(2,1,2x+1), Ui(2,1,2x+2), Ri(2,1,2x+1) and M(2,1,x+1), and has one output Bo(2,1,2x+2). In different embodiments the inputs J(2,1,x+1), K(2,1,x+1), L(2,1,x+1), and M(2,1,x+1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 2, ring 1, stage 0), there are also stages (slice 2, ring 1, stage 1), (slice 2, ring 1, stage 2), (slice 2, ring 1, stage 3), … (slice 2, ring 1, stage "m-1"), (slice 2, ring 1, stage "x") in that order, where the stages from (slice 2, ring 1, stage 1), (slice 2, ring 1, stage 2), … , (slice 2, ring 1, stage "x-1") are not shown in the diagram 100C.

The stage (slice 2, ring 2, stage 0) consists of 8 inputs namely Ri(2,2,1), Ri(2,2,2), Ui(2,2,1), Ui(2,2,2), J(2,2,1), K(2,2,1), L(2,2,1), and M(2,2,1); and 4 outputs Bo(2,2,1), Bo(2,2,2), Fo(2,2,1), and Fo(2,2,2). The stage (slice 2, ring "2", stage "0") also consists of four 4:1 Muxes namely F(2,2,1), F(2,2,2), B(2,2,1), and B(2,2,2). The 4:1 Mux F(2,2,1) has four inputs namely Ri(2,2,1), Ri(2,2,2), Ui(2,2,2), and J(2,2,1), and has one output Fo(2,2,1). The 4:1 Mux F(2,2,2) has four inputs namely Ri(2,2,1), Ri(2,2,2), Ui(2,2,1), and K(2,2,1), and has one output Fo(2,2,2).

The 4:1 Mux B(2,2,1) has four inputs namely Ui(2,2,1), Ui(2,2,2), Ri(2,2,2), and L(2,2,1), and has one output Bo(2,2,1). The 4:1 Mux B(2,2,2) has four inputs namely Ui(2,2,1), Ui(2,2,2), Ri(2,2,1) and M(2,2,1), and has one output Bo(2,2,2). In different embodiments the inputs J(2,2,1), K(2,2,1), L(2,2,1), and M(2,2,1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (slice 2, ring 2, stage "x") consists of 8 inputs namely Ri(2,2,2x+1), Ri(2,2,2x+2), Ui(2,2,2x+1), Ui(2,2,2x+2), J(2,2,x+1), K(2,2,x+1), L(2,2,x+1), and M(2,2,x+1); and 4 outputs Bo(2,2,2x+1), Bo(2,2,2x+2), Fo(2,2,2x+1), and Fo(2,2,2x+2). The stage (slice 2, ring 2, stage "y") also consists of four 4:1 Muxes namely F(2,2,2y+1), F(2,2,2y+2), B(2,2,2y+1), and B(2,2,2y+2). The 4:1 Mux F(2,2,2y+1) has four inputs namely Ri(2,2,2y+1), Ri(2,2,2y+2), Ui(2,2,2y+2), and J(2,2,y+1), and has one output Fo(2,2,2y+1). The 4:1 Mux F(2,2,2y+2) has four inputs namely Ri(2,2,2y+1), Ri(2,2,2y+2), Ui(2,2,2y+1), and K(2,2,y+1), and has one output Fo(2,2,2y+2).

The 4:1 Mux B(2,2,2y+1) has four inputs namely Ui(2,2,2y+1), Ui(2,2,2y+2), Ri(2,2,2y+2), and L(2,2,y+1), and has one output Bo(2,2,2y+1). The 4:1 Mux B(2,2,2y+2) has four inputs namely Ui(2,2,2y+1), Ui(2,2,2y+2), Ri(2,2,2y+1) and

M(2,2,y+1), and has one output Bo(2,2,2y+2). In different embodiments the inputs J(2,2,y+1), K(2,2,y+1), L(2,2,y+1), and M(2,2,y+1) are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Just the same way the stage (slice 2, ring 2, stage 0), there are also stages (slice 2, ring 2, stage 1), (slice 2, ring 2, stage 2), (slice 2, ring 2, stage 3), … (slice 2, ring 2, stage "y-1"), (slice 2, ring 2, stage "y") in that order, where the stages from (slice 2, ring 2, stage 1), (slice 2, ring 2, stage 2), … , (slice 2, ring 2, stage "y-1") are not shown in the diagram 100C.

As illustrated in diagram 100C5 in FIG. 1C5, the similar internal connections between two successive stages of any ring of any slice of partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C, in some embodiments are provided for all the slices c = 1, 2; for all the rings in each of the slices d = 1, 2; and for all the stages namely when c = 1, d = 1, e = [1,m]; when c=1, d=2, e=[1,n]; when c=2, d=1, e=[1,x]; and when c=2, d=2; e=[1,y].

Each stage of any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B consists of $2 * d = 4$ outputs. Even though each stage has four 4:1 muxes, in other embodiments any of these stages can be one of the four by four switch diagrams namely 200A of FIG. 2A, 200B of FIG. 2B, 200C of FIG. 2C, and one of the eight by four switch diagrams namely 200E of FIG. 2E, 200F of FIG. 2F.

In general, any ring of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ illustrated in 100C also may have inputs and outputs connected from computational block from either only from left-hand side as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A; or only from right-hand side; or from both left-hand and right-hand sides as in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B.

Applicant now notes a few aspects of the diagram 100C in FIG. 1C an exemplary partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to one computational block, with each computational block having 16 inlet links and 4 outlet links as follows: (Also these aspects are helpful in more optimization of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ as well as faster scheduling of the connections between outlet links of the computational blocks and the inlet links of the computational blocks.)

1) The partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C in FIG. 1C is divided into two slices namely slice 1 and slice 2. The outlet links of the computational block namely O1 and O2 are connected to only one slice i.e. slice 1. In other words outlet links O1 and O2 are absolutely not connected to slice 2. Similarly the outlet links of the computational block namely O3 and O4 are connected to only one slice i.e. slice 2. In other words outlet links O3 and O4 are absolutely not connected to slice 1. 2) The second aspect is all the hop wires and multi-drop hop wires originating from slice 1 from any block will be terminating only in the slice 1 of any other block. Similarly all the hop wires and multi-drop hop wires originating from slice 2 from any block will be terminating only in the slice 2 of any other block. 3) The third aspect is the mux whose output is directly connected to each inlet link of the computational block must have at least one input connected from each slice of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C. That is for example since the 4:1 mux B(1,1,1), belonging to slice 1, and having its output Bo(1,1,1) directly connected to inlet link I1 must have at least one of its inputs connecting from an output of a mux of a stage of a ring of slice 2 as well. This property must be satisfied for all the inlet links of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C.

Referring to diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 illustrate the details of the foregoing third aspect of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C. Applicant notes that diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 are all actually part of the

partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C and these separate diagrams are necessary only to avoid the clutter in the diagram 100C of FIG. 1C.

The connections illustrated between different slices in diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 are the only connections between different slices, in some exemplary embodiments. In general the connections between different slices are given only at the terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block.

Referring to diagram 100C1 in FIG. 1C1 illustrate the connections between the stage (slice 1, ring 1, stage 0) and between the stage (slice 2, ring 1, stage 0). The same connection that is given to the input Ui(1,1,1) is also connected to the input L(2,1,1). The same connection that is given to the input Ui(1,1,2) is also connected to the input M(2,1,1). Similarly the same connection that is given to the input Ui(2,1,1) is also connected to the input L(1,1,1). The same connection that is given to the input Ui(2,1,2) is also connected to the input M(1,1,1).

Therefore inlet link I1 can be essentially connected through the 4:1 mux B(1,1,1) with three of its inputs connecting from slice 1 namely Ui(1,1,1), Ui(1,1,2), Ri(1,1,2) and one input L(1,1,1) connecting from slice 2. The inlet link I2 can be essentially connected through the 4:1 mux B(1,1,2) with three of its inputs connecting from slice 1 namely Ui(1,1,1), Ui(1,1,2), Ri(1,1,1) and one input M(1,1,1) connecting from slice 2. The inlet link I9 can be essentially connected through the 4:1 mux B(1,2,1) with three of its inputs connecting from slice 2 namely Ui(2,1,1), Ui(2,1,2), Ri(2,1,2) and one input L(2,1,1) connecting from slice 1. The inlet link I10 can be essentially connected through the 4:1 mux B(2,1,2) with three of its inputs connecting from slice 2 namely Ui(2,1,1), Ui(2,1,2), Ri(2,1,1) and one input M(2,1,1) connecting from slice 1. Hence all the inlet links I1, I2, I9 and I10 are all independently reachable from both slice 1 and slice2.

Referring to diagram 100C2 in FIG. 1C2 illustrate the connections between the stage (slice 1, ring 2, stage 0) and between the stage (slice 2, ring 2, stage 0). The same connection that is given to the input Ui(1,2,1) is also connected to the input M(2,2,1). The

same connection that is given to the input Ui(1,2,2) is also connected to the input L(2,2,1). Similarly the same connection that is given to the input Ui(2,2,1) is also connected to the input M(1,2,1). The same connection that is given to the input Ui(2,2,2) is also connected to the input L(1,2,1).

Therefore inlet link I3 can be essentially connected through the 4:1 mux B(1,2,1) with three of its inputs connecting from slice 1 namely Ui(1,2,1), Ui(1,2,2), Ri(1,2,2) and one input M(2,2,1) connecting from slice 2. The inlet link I4 can be essentially connected through the 4:1 mux B(1,2,2) with three of its inputs connecting from slice 1 namely Ui(1,2,1), Ui(1,2,2), Ri(1,2,1) and one input M(1,2,1) connecting from slice 2. The inlet link I11 can be essentially connected through the 4:1 mux B(2,2,1) with three of its inputs connecting from slice 2 namely Ui(2,2,1), Ui(2,2,2), Ri(2,2,2) and one input L(2,2,1) connecting from slice 1. The inlet link I12 can be essentially connected through the 4:1 mux B(2,2,2) with three of its inputs connecting from slice 2 namely Ui(2,2,1), Ui(2,2,2), Ri(2,2,1) and one input M(2,2,1) connecting from slice 1. Hence all the inlet links I3, I4, I11 and I12 are all independently reachable from both slice 1 and slice2.

Referring to diagram 100C3 in FIG. 1C3 illustrate the connections between the stage (slice 1, ring 1, stage “m”) and between the stage (slice 2, ring 2, stage “y”). The same connection that is given to the input Ri(1,1,2m+1) is also connected to the input J(2,2,y+1). The same connection that is given to the input Ri(1,1,2m+2) is also connected to the input K(2,2,y+1). Similarly the same connection that is given to the input Ri(2,2,2y+1) is also connected to the input J(1,1,m+1). The same connection that is given to the input Ri(2,2,2y+2) is also connected to the input K(1,1,m+1).

Therefore inlet link I5 can be essentially connected through the 4:1 mux F(1,1,2m+1) with three of its inputs connecting from slice 1 namely Ri(1,1,2m+1), Ri(1,1,2m+2), Ui(1,1,2m+2) and one input J(1,1,m+1) connecting from slice 2. The inlet link I6 can be essentially connected through the 4:1 mux F(1,1,2m+2) with three of its inputs connecting from slice 1 namely Ri(1,1,2m+1), Ri(1,1,2m+2),Ui(1,1,2m+1) and one input K(1,1,m+1) connecting from slice 2. The inlet link I15 can be essentially connected through the 4:1 mux F(2,2,2y+1) with three of its inputs connecting from slice 2 namely Ri(2,2,2y+1), Ri(2,2,2y+2), Ui(2,2,2y+2) and one input J(2,2,y+1) connecting

from slice 1. The inlet link I16 can be essentially connected through the 4:1 mux F(2,2,2y+2) with three of its inputs connecting from slice 2 namely Ri(2,2,2y+1), Ri(2,2,2y+2), Ui(2,2,2y+1) and one input K(2,2,y+1) connecting from slice 1. Hence all the inlet links I5, I6, I15 and I16 are all independently reachable from both slice 1 and slice2.

Referring to diagram 100C4 in FIG. 1C4 illustrate the connections between the stage (slice 1, ring 2, stage "n") and between the stage (slice 2, ring 1, stage "x"). The same connection that is given to the input Ri(1,2,2n+1) is also connected to the input K(2,1,x+1). The same connection that is given to the input Ri(1,2,2n+2) is also connected to the input J(2,1,x+1). Similarly the same connection that is given to the input Ri(2,1,2x+1) is also connected to the input K(1,2,n+1). The same connection that is given to the input Ri(2,1,2x+2) is also connected to the input J(1,2,n+1).

Therefore inlet link I7 can be essentially connected through the 4:1 mux F(1,2,2n+1) with three of its inputs connecting from slice 1 namely Ri(1,2,2n+1), Ri(1,2,2n+2), Ui(1,2,2n+2) and one input J(1,2,n+1) connecting from slice 2. The inlet link I8 can be essentially connected through the 4:1 mux F(1,2,2n+2) with three of its inputs connecting from slice 1 namely Ri(1,2,2n+1), Ri(1,2,2n+2),Ui(1,2,2n+1) and one input K(1,2,n+1) connecting from slice 2. The inlet link I13 can be essentially connected through the 4:1 mux F(2,1,2x+1) with three of its inputs connecting from slice 2 namely Ri(2,1,2x+1), Ri(2,1,2x+2), Ui(2,1,2x+2) and one input J(2,1,x+1) connecting from slice 1. The inlet link I14 can be essentially connected through the 4:1 mux F(2,1,2x+2) with three of its inputs connecting from slice 2 namely Ri(2,1,2x+1), Ri(2,1,2x+2), Ui(2,1,2x+1) and one input K(2,1,x+1) connecting from slice 1. Hence all the inlet links I7, I8, I13 and I14 are all independently reachable from both slice 1 and slice2.

The connections illustrated between different slices, in several embodiments, in diagram 100C1 in FIG. 1C1, diagram 100C2 in FIG. 1C2, diagram 100C3 in FIG. 1C3, and diagram 100C4 in FIG. 1C4 are the only connections between different slices. And also the terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block have three inputs coming from one slice and one input coming from another slice. In other embodiments it is also possible so that the

terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block have two inputs coming from one slice and two inputs coming from another slice.

Also in general the number of slices in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C may be more than or equal to two. In such a case terminating muxes i.e. whose outputs are directly connected to one of the inlet links of the computational block will have at least one input coming from each slice. And the outlet links of the computational block will be divided and connected to each slice; however each outlet link of the computational block will be connected to only one slice. Also in general the hop wires and multi-drop hop wires are connected to only between the corresponding slices of different blocks, in some embodiments some of the hop wires and multi-drop hop wires may be connected between different slices of different blocks even if it is done partially.

FIG. 2A illustrates a stage (ring "k", stage "m") 200A consists of 4 inputs namely Fi(k,2m+1), Fi(k,2m+2), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of six 2:1 Muxes namely F(k,2m+1), F(k,2m+2), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 2B illustrates a stage (ring "k", stage "m") 200B consists of 4 inputs namely Ri(k,2m+1), Ri(k,2m+2), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists

of eight 2:1 Muxes namely R(k,2m+1), R(k,2m+2), F(k,2m+1), F(k,2m+2), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The 2:1 Mux R(k,2m+1) has two inputs namely Ri(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 2C illustrates a stage (ring "k", stage "m") 200C consists of 4 inputs namely Fi(k,2m+1), Fi(k,2m+2), Bi(k,2m+1), and Bi(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of four 2:1 Muxes namely F(k,2m+1), F(k,2m+2), B(k,2m+1), and B(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux B(k,2m+1) has two inputs namely Bi(k,2m+1) and Bi(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Bi(k,2m+1) and Bi(k,2m+2) and has one output Bo(k,2m+2).

However the stage "m+1" of ring "k" with "m+1" stages of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 2 inputs and 2 outputs as shown in diagram 200D in FIG. 2D. FIG. 2D illustrates a stage (ring "k", stage "m") 200D consists of 2 inputs namely Fi(k,2m+1) and Fi(k,2m+2); and 2 outputs Fo(k,2m+1) and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of two 2:1 Muxes namely F(k,2m+1), F(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely

Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2). A stage with $d = 2$ inputs and $d = 2$ outputs is typically the "last stage" or "root stage" of ring.

The stage "m" of ring "k" with "m" stages of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 8 inputs and 4 outputs as shown in diagram 200E in FIG. 2E. FIG. 2E illustrates a stage (ring "k", stage "m") 200E consists of 8 inputs namely Ri(k,2m+1), Ri(k,2m+2), Ui(k,2m+1), Ui(k,2m+2), J, K, L, and M; and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of eight 2:1 Muxes namely R(k,2m+1), R(k,2m+2), F(k,2m+1), F(k,2m+2), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The 2:1 Mux R(k,2m+1) has two inputs namely Ri(k,2m+1) and J, and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and K, and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Uo(k,2m+2), and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Ro(k,2m+2) and Uo(k,2m+1) , and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and L, and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and M, and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Ro(k,2m+2), and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+2) and Ro(k,2m+1), and has one output Bo(k,2m+2). In different embodiments the inputs J, K, L, and M are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage "m" of ring "k" with "m" stages of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, in another embodiment, may have 8 inputs and 4 outputs as shown in diagram 200F in FIG. 2F. FIG. 2F illustrates a stage (ring "k", stage "m") 200F consists of 8 inputs namely Ri(k,2m+1), Ri(k,2m+2), Ui(k,2m+1), Ui(k,2m+2), J, K, L, and M; and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of four 4:1 Muxes namely F(k,2m+1), F(k,2m+2),

B(k,2m+1), and B(k,2m+2). The 4:1 Mux F(k,2m+1) has four inputs namely Ri(k,2m+1), Ri(k,2m+2), Ui(k,2m+2), and J, and has one output Fo(k,2m+1). The 4:1 Mux F(k,2m+2) has four inputs namely Ri(k,2m+1), Ri(k,2m+2), Ui(k,2m+1), and K, and has one output Fo(k,2m+2).

The 4:1 Mux B(k,2m+1) has four inputs namely Ui(k,2m+1), Ui(k,2m+2), Ri(k,2m+2), and L, and has one output Bo(k,2m+1). The 4:1 Mux B(k,2m+2) has four inputs namely Ui(k,2m+1), Ui(k,2m+2), Ri(k,2m+1) and M, and has one output Bo(k,2m+2). In different embodiments the inputs J, K, L, and M are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The number of stages in a ring of any block may not be equal to the number of stages in any other ring of the same of block or any ring of any other block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. For example the number of stages in ring 1 of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A or of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B or of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C is denoted by "m" and the number of stages in ring 2 of the partial multi-stage hierarchical network is denoted by "n", and so "m" may or may not be equal to "n". Similarly the number of stages in ring 2 corresponding to block (3,3) of 2D-grid 800 may not be equal to the number of stages in ring 2 corresponding to block (6,9) of 2D-grid 800. Similarly in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C the number of stages in (slice 1, ring 2) corresponding to block (3,3) of 2D-grid 800 may not be equal to the number of stages in (slice 1, ring 2) corresponding to block (6,9) of 2D-grid 800.

Even though the number of inlet links to the computational block is four and the number of outlet links to the computational block is two in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A, the number of inlet links to the computational block is eight and the number of outlet links to the computational block is four in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B, and the

number of inlet links to the computational block is sixteen and the number of outlet links to the computational block is four in the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C, in other embodiments the number of inlet links to the computational block may be any arbitrary number and the number of outlet links to the computational block may also be another arbitrary number. However the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of inlet links to the computational block divided by $d = 2$ if the inputs and outputs are connected either only from left-hand side or only from right-hand side, if the number of inlet links to the computational block is greater than or equal to the number of outlet links to the computational block. In such a case one or more of the outlet links to the computational block are connected to more than one inlet links of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to a block. Similarly the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of inlet links to the computational block divided by $2 * d = 4$ if the inputs and outputs are connected from both left-hand side and from right-hand side, if the number of inlet links to the computational block is greater than or equal to the number of outlet links to the computational block.

Otherwise the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of outlet links to the computational block divided by $d = 2$ if the inputs and outputs are connected either only from left-hand side or only from right-hand side, if the number of outlet links to the computational block is greater than the number of inlet links to the computational block. In such a case one or more of the outlet links of the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ corresponding to a block are connected to more than one inlet link of the computational block. Similarly the total number of rings of all the slices corresponding to the partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ of a block is generally equal to the number of outlet links to

the computational block divided by $2*d=4$ if the inputs and outputs are connected from both left-hand side and from right-hand side, if the number of outlet links to the computational block is greater than or equal to the number of inlet links to the computational block.

In another embodiment, the number of inlet links to the computational block corresponding to a block of 2D-grid of blocks may or may not be equal to the number of inlet links to the computational block corresponding to another block. Similarly the number of outlet links to the computational block corresponding to a block of 2D-grid of blocks may or may not be equal to the number of outlet links to the computational block corresponding to another block. Hence the total number of rings of the partial multi-stage hierarchical network $V_{Comb}(N_1,N_2,d,s)$ corresponding to a block of 2D-grid of blocks may or may not be equal to the partial multi-stage hierarchical network $V_{Comb}(N_1,N_2,d,s)$ corresponding to another block. For example the total number of rings corresponding to block (4,5) of 2D-grid 800 may be two and the total number of rings in block (5,4) of 2D-grid 800 may be three.

A multi-stage hierarchical network can be represented with the notation $V_{Comb}(N_1,N_2,d,s)$, where N_1 represents the total number of inlet links of the complete multi-stage hierarchical network and N_2 represents the total number of outlet links of the complete multi-stage hierarchical network, d represents the number of inlet links of any ring in any block of the complete multi-stage hierarchical network either from only left-hand side or only right-hand side, or equivalently the number of outlet links of any ring in any block of the complete multi-stage hierarchical network either from only left-hand side or only right-hand side, and when the inputs and outputs are connected from left-hand side, s is the ratio of number of outgoing links from each stage 0 of any ring in any block to the number of inlet links of any ring in any block of the complete multi-stage hierarchical network (for example the complete multi-stage hierarchical network corresponding to $V_{Comb}(N_1,N_2,d,s)$ 100A in FIG. 1A, $N_1=200$, $N_2=400$, $d=2$, $s=1$). Also a multi-stage hierarchical network where $N_1=N_2=N$ is represented as $V_{Comb}(N,d,s)$.

The diagram 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, and 300E of FIG. 3E are different embodiments of all the connections between two arbitrary successive stages in two different rings of the same block or two different rings of different blocks of 2D-grid 800. Referring to diagram 300A in FIG. 3A illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 4 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), and Ui(x,2p+2); and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of eight 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and Bo(x,2p+1) and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and Bo(x,2p+2) and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Ro(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+1) and Ro(x,2p+2) and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 4 inputs namely Ri(x,2p+3), Ri(x,2p+4), Ui(x,2p+3), and Ui(x,2p+4); and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of eight 2:1 Muxes namely R(x,2p+3), R(x,2p+4), F(x,2p+3), F(x,2p+4), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The 2:1 Mux R(x,2p+3) has two inputs namely Ri(x,2p+3) and Bo(x,2p+3) and has one output Ro(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs

namely Ri(x,2p+4) and Bo(x,2p+4) and has one output Ro(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely Ro(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely Ro(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and Fo(x,2p+3) and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and Fo(x,2p+4) and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Ri(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 4 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), and Ui(y,2q+2); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of eight 2:1 Muxes namely R(y,2q+1), R(y,2q+2), F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and Bo(y,2q+1) and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Ri(y,2q+2) and Bo(y,2q+2) and has one output Ro(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Ro(y,2q+1) and Ro(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Ro(y,2q+1) and Ro(y,2q+2) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and Fo(y,2q+1) and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux

B(y,2q+2) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 4 inputs namely Ri(y,2q+3), Ri(y,2q+4), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of eight 2:1 Muxes namely R(y,2q+3), R(y,2q+4), F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux R(y,2q+3) has two inputs namely Ri(y,2q+3) and Bo(y,2q+3) and has one output Ro(y,2q+3). The 2:1 Mux R(y,2q+4) has two inputs namely Ri(y,2q+4) and Bo(y,2q+4) and has one output Ro(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely Ro(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Ro(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Ri(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Ri(y,2q+4) of the stage (ring "y", stage "q+1"). The output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to the input Ui(y,2q+2) of the stage (ring "y", stage "q").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to the input Ri(x,2p+4) of the stage (ring "x", stage "p+1"). The output

Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

Ring "x" and ring "y" may or may not belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. If ring "x" and ring "y" belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are hereinafter called "internal hop wires". For example if "x = 2" and "y = 3" and both the ring 2 and ring 3 belong to the same block (9,9) of 2D-grid 800, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are "internal hop wires".

If ring "x" and ring "y" belong to the different blocks of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are hereinafter called "external hop wires". The external hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) may be horizontal wires or vertical wires. The length of the external hop wires is manhattan distance between the corresponding blocks, hereinafter "hop length". For example if ring "x" belongs to block (1,1) and ring "y" belongs to block (1,6) of 2D-grid 800 then the external hop wires are hereinafter called "horizontal external hop wires". And the hop length of the horizontal hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) is given by 6 – 1 = 5. Similarly if ring "x" and ring "y" belong to two blocks in the same horizontal row of 2D-grid 800, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are horizontal external hop wires.

For example if ring "x" belongs to block (1,1) and ring "y" belongs to block (9,1) of 2D-grid 800 then the external hop wires are hereinafter called "vertical external hop wires". And the hop length of the vertical hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) is given by 9 – 1 = 8. Similarly if ring "x" and ring "y" belong to two blocks in the same vertical column of 2D-grid 800, then the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are vertical external hop wires. External hop wires are typically horizontal or vertical according to the current invention.

Referring to diagram 300B in FIG. 3B illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x",

stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 8 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), J1, K1, L1, and M1; and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of eight 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and J1, and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and K1, and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Uo(x,2p+2), and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+2) and Uo(x,2p+1), and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and L1, and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and M1, and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Ro(x,2p+2), and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+2) and Ro(x,2p+1), and has one output Bo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 8 inputs namely Ri(x,2p+3), Ri(x,2p+4), Ui(x,2p+3), Ui(x,2p+4), J2, K2, L2, and M2; and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of eight 2:1 Muxes namely R(x,2p+3), R(x,2p+4), F(x,2p+3), F(x,2p+4), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The 2:1 Mux R(x,2p+3) has two inputs namely Ri(x,2p+3) and J2, and has one output Ro(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs namely Ri(x,2p+4) and K2, and has one output Ro(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely Ro(x,2p+3) and Uo(x,2p+4), and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely Ro(x,2p+4) and Uo(x,2p+3), and has one output Fo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and L2, and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and M2, and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Ro(x,2p+4), and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Uo(x,2p+4) and Ro(x,2p+3), and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Ri(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 8 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), J3, K3, L3, and M3; and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of eight 2:1 Muxes namely R(y,2q+1), R(y,2q+2), F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and J3, and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Ri(y,2q+2) and K3, and has one output Ro(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Ro(y,2q+1) and Uo(y,2q+2), and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Ro(y,2q+2) and Uo(y,2q+1) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and L3, and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and M3, and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Ro(y,2q+2), and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+2) and Ro(y,2q+1), and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 8 inputs namely Ri(y,2q+3), Ri(y,2q+4), Ui(y,2q+3), Ui(y,2q+4), J4, K4, L4, and M4; and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of eight 2:1 Muxes namely R(y,2q+3), R(y,2q+4), F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux R(y,2q+3) has two inputs namely

Ri(y,2q+3) and J4, and has one output Ro(y,2q+3). The 2:1 Mux R(y,2q+4) has two inputs namely Ri(y,2q+4) and K4, and has one output Ro(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely Ro(y,2q+3) and Uo(y,2q+4), and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Ro(y,2q+4) and Uo(y,2q+3), and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and L4, and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and M4, and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Ro(y,2q+4), and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+4) and Ro(y,2q+3), and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Ri(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Ri(y,2q+4) of the stage (ring "y", stage "q+1"). The output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to the input Ui(y,2q+2) of the stage (ring "y", stage "q").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to the input Ri(x,2p+4) of the stage (ring "x", stage "p+1"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

In various embodiments, the inputs J1, K1, L1, and M1 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J2, K2, L2, and M2 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J3, K3, L3, and M3 are connected from any of the outputs of any other stages of any ring of any block of the

multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Finally the inputs J4, K4, L4, and M4 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Referring to diagram 300C in FIG. 3C, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 4 inputs namely Fi(x,2p+1), Fi(x,2p+2), Ui(x,2p+1), and Ui(x,2p+2); and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of six 2:1 Muxes namely F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Fi(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Fi(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 4 inputs namely Fi(x,2p+3), Fi(x,2p+4), Ui(x,2p+3), and Ui(x,2p+4); and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of six 2:1 Muxes namely F(x,2p+3), F(x,2p+4), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely Fi(x,2p+3) and Fi(x,2p+4) and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely Fi(x,2p+3) and Fi(x,2p+4) and has one output Fo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and Fo(x,2p+3) and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and Fo(x,2p+4) and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Fi(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 4 inputs namely Fi(y,2q+1), Fi(y,2q+2), Ui(y,2q+1), and Ui(y,2q+2); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of six 2:1 Muxes namely F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and Fo(y,2q+1) and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 4 inputs namely Fi(y,2q+3), Fi(y,2q+4), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of six 2:1 Muxes namely F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely Fi(y,2q+3) and Fi(y,2q+4) and has one

output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Fi(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Fi(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Fi(y,2q+4) of the stage (ring "y", stage "q+1"). The output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to the input Ui(y,2q+2) of the stage (ring "y", stage "q").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to the input Fi(x,2p+4) of the stage (ring "x", stage "p+1"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

Referring to diagram 300D in FIG. 3D, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 4 inputs namely Fi(x,2p+1), Fi(x,2p+2), Ui(x,2p+1), and Ui(x,2p+2); and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of six 2:1 Muxes namely

F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Fi(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Fi(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 2 inputs namely Fi(x,2p+3), Fi(x,2p+4); and 2 outputs Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of two 2:1 Muxes namely F(x,2p+3) and F(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely Fi(x,2p+3) and Fi(x,2p+4) and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely Fi(x,2p+3) and Fi(x,2p+4) and has one output Fo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Fi(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Fo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 4 inputs namely Fi(y,2q+1), Fi(y,2q+2), Ui(y,2q+1), and Ui(y,2q+2); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of six 2:1 Muxes namely F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and Fo(y,2q+1) and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2)

and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 4 inputs namely Fi(y,2q+3), Fi(y,2q+4), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of six 2:1 Muxes namely F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely Fi(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Fi(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Fi(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Fi(y,2q+4) of the stage (ring "y", stage "q+1"). The output Fo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to the input Ui(y,2q+2) of the stage (ring "y", stage "q").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to the input Fi(x,2p+4) of the stage (ring "x", stage "p+1"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

Referring to diagram 300E in FIG. 3E, illustrates all the connections between root stage of a ring namely the stage (ring "x", stage "p") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 4 inputs namely Fi(x,2p+1), Fi(x,2p+2), Ui(x,2p+1), and Ui(x,2p+2); and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of six 2:1 Muxes namely F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Fi(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Fi(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+2).

The stage (ring "y", stage "q") consists of 4 inputs namely Fi(y,2q+1), Fi(y,2q+2), Ui(y,2q+1), and Ui(y,2q+2); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of six 2:1 Muxes namely F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and Fo(y,2q+1) and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux

B(y,2q+2) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 4 inputs namely Fi(y,2q+3), Fi(y,2q+4), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of six 2:1 Muxes namely F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely Fi(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Fi(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Fi(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected via the wire Hop(1,2) to the input Ui(y,2q+2) of the stage (ring "y", stage "q"). The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Fi(y,2q+4) of the stage (ring "y", stage "q+1").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to the input Ui(x,2p+1) of the stage (ring "x", stage "p"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

Just like in diagram 300A of FIG. 3A, in diagram 300B of FIG. 3B, in diagram 300C of FIG. 3C, diagram 300D of FIG. 3D, and in diagram 300E of FIG. 3E, the wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are either internal hop wires or horizontal external hop wires or vertical external hop wires.

The diagram 400A of FIG. 4A and 400B of FIG. 4B are different embodiments of all the connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks of 2D-grid 800. Referring to diagram 400A in FIG. 4A illustrates all the connections between an arbitrary stage of a ring namely the stages (ring "x", stage "p"), and another arbitrary stage of any other ring namely the stages (ring "y", stage "q") of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 8 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), J1, K1, L1, and M1; and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of eight 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and J1 and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and K1 and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Uo(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+2) and Uo(x,2p+1) and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and L1 and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and M1 and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Ro(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+2) and Ro(x,2p+1) and has one output Bo(x,2p+2).

The stage (ring "y", stage "q") consists of 8 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), J3, K3, L3, and M3; and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of

eight 2:1 Muxes namely R(y,2q+1), R(y,2q+2), F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and J3 and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Ri(y,2q+2) and K3 and has one output Ro(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Ro(y,2q+1) and Uo(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Ro(y,2q+2) and Uo(y,2q+1) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and L3, and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and M3, and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Ro(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+2) and Ro(y,2q+1) and has one output Bo(y,2q+2).

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Ri(y,2q+2) of the stage (ring "y", stage "q"). The output Bo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(1,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

Ring "x" and ring "y" may or may not belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. If ring "x" and ring "y" belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1) and Hop(1,2) are hereinafter called "internal hop wires". For example if "x = 2" and "y = 3" and both the ring 2 and ring 3 belong to the same block (9,9) of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are "internal hop wires".

If ring "x" and ring "y" belong to the different blocks of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1) and Hop(1,2) are hereinafter called "external hop wires". The external hop wires Hop(1,1) and Hop(1,2) may be horizontal wires or vertical wires. The length of the external hop wires is Manhattan distance between the corresponding blocks, hereinafter "hop length". For example if ring "x" belongs to block (1,1) and ring "y" belongs to block (1,6) of 2D-grid 800 then the external hop wires are hereinafter called "horizontal external hop wires".

And the hop length of the horizontal hop wires Hop(1,1) and Hop(1,2) is given by 6 – 1 = 5. Similarly if ring "x" and ring "y" belong to two blocks in the same horizontal row of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are horizontal external hop wires.

For example if ring "x" belongs to block (1,1) and ring "y" belongs to block (9,1) of 2D-grid 800 then the external hop wires are hereinafter called "vertical external hop wires". And the hop length of the vertical hop wires Hop(1,1) and Hop(1,2) is given by 9 – 1 = 8. Similarly if ring "x" and ring "y" belong to two blocks in the same vertical column of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are vertical external hop wires. External hop wires are typically horizontal or vertical according to the current invention.

Referring to diagram 400B in FIG. 4B illustrates all the connections between an arbitrary stage of a ring namely the stages (ring "x", stage "p"), and another arbitrary stage of any other ring namely the stages (ring "y", stage "q") of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 8 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), J1, K1, L1, and M1; and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of four 4:1 Muxes namely F(x,2p+1), F(x,2p+2), B(x,2p+1), and B(x,2p+2). The 4:1 Mux F(x,2p+1) has four inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+2), and J1 and has one output Fo(x,2p+1). The 4:1 Mux F(x,2p+2) has four inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), and K1 and has one output Fo(x,2p+2).

The 4:1 Mux B(x,2p+1) has four inputs namely Ui(x,2p+1), Ui(x,2p+2), Ri(x,2p+2), and L1 and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Ui(x,2p+1), Ui(x,2p+2), Ri(x,2p+1), and M1 and has one output Bo(x,2p+2).

The stage (ring "y", stage "q") consists of 8 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), J3, K3, L3, and M3; and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of

four 4:1 Muxes namely F(y,2q+1), F(y,2q+2), B(y,2q+1), and B(y,2q+2). The 4:1 Mux F(y,2q+1) has four inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+2), and J3 and has one output Fo(y,2q+1). The 4:1 Mux F(y,2q+2) has four inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), and K3 and has one output Fo(y,2q+2).

The 4:1 Mux B(y,2q+1) has four inputs namely Ui(y,2q+1), Ui(y,2q+2), Ri(y,2q+2), and L3, and has one output Bo(y,2q+1). The 4:1 Mux B(y,2q+2) has four inputs namely Ui(y,2q+1), Ui(y,2q+2), Ri(y,2q+1), and M3, and has one output Bo(y,2q+2).

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Ri(y,2q+2) of the stage (ring "y", stage "q"). The output Bo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(1,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

Ring "x" and ring "y" may or may not belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. If ring "x" and ring "y" belong to the same block of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1) and Hop(1,2) are hereinafter called "internal hop wires". For example if "x = 2" and "y = 3" and both the ring 2 and ring 3 belong to the same block (9,9) of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are "internal hop wires".

If ring "x" and ring "y" belong to the different blocks of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$, then the wires Hop(1,1) and Hop(1,2) are hereinafter called "external hop wires". The external hop wires Hop(1,1) and Hop(1,2) may be horizontal wires or vertical wires. The length of the external hop wires is Manhattan distance between the corresponding blocks, hereinafter "hop length". For example if ring "x" belongs to block (1,1) and ring "y" belongs to block (1,6) of 2D-grid 800 then the external hop wires are hereinafter called "horizontal external hop wires". And the hop length of the horizontal hop wires Hop(1,1) and Hop(1,2) is given by 6 – 1 = 5. Similarly if ring "x" and ring "y" belong to two blocks in the same horizontal row of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are horizontal external hop wires.

For example if ring "x" belongs to block (1,1) and ring "y" belongs to block (9,1) of 2D-grid 800 then the external hop wires are hereinafter called "vertical external hop wires". And the hop length of the vertical hop wires Hop(1,1) and Hop(1,2) is given by 9 – 1 = 8. Similarly if ring "x" and ring "y" belong to two blocks in the same vertical column of 2D-grid 800, then the wires Hop(1,1) and Hop(1,2) are vertical external hop wires. External hop wires are typically horizontal or vertical according to the current invention.

The diagram 500A of FIG. 5A is an embodiments of all the connections with multi-drop hop wires, between two arbitrary successive stages in two different rings of different blocks of 2D-grid 800. Referring to diagram 500A in FIG. 5A illustrates all the connections with multi-drop hop wires, between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. The multi-drop hop wires are also connected to two other stages (ring "a", stage "s") and (ring "b", stage "t") belonging to a third block.

The stage (ring "x", stage "p") consists of 8 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), J1, K1, L1, and M1; and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of eight 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and J1, and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and K1, and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Uo(x,2p+2), and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+2) and Uo(x,2p+1), and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and L1, and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and M1, and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely

Uo(x,2p+1) and Ro(x,2p+2), and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+2) and Ro(x,2p+1), and has one output Bo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 8 inputs namely Ri(x,2p+3), Ri(x,2p+4), Ui(x,2p+3), Ui(x,2p+4), J2, K2, L2, and M2; and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of eight 2:1 Muxes namely R(x,2p+3), R(x,2p+4), F(x,2p+3), F(x,2p+4), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The 2:1 Mux R(x,2p+3) has two inputs namely Ri(x,2p+3) and J2, and has one output Ro(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs namely Ri(x,2p+4) and K2, and has one output Ro(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely Ro(x,2p+3) and Uo(x,2p+4), and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely Ro(x,2p+4) and Uo(x,2p+3), and has one output Fo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and L2, and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and M2, and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Ro(x,2p+4), and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Uo(x,2p+4) and Ro(x,2p+3), and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Ri(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 8 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), J3, K3, L3, and M3; and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of eight 2:1 Muxes namely R(y,2q+1), R(y,2q+2), F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and J3, and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Ri(y,2q+2) and K3, and has one output Ro(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Ro(y,2q+1) and Uo(y,2q+2), and has one output

Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Ro(y,2q+2) and Uo(y,2q+1) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and L3, and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and M3, and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Ro(y,2q+2), and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+2) and Ro(y,2q+1), and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 8 inputs namely Ri(y,2q+3), Ri(y,2q+4), Ui(y,2q+3), Ui(y,2q+4), J4, K4, L4, and M4; and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of eight 2:1 Muxes namely R(y,2q+3), R(y,2q+4), F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux R(y,2q+3) has two inputs namely Ri(y,2q+3) and J4, and has one output Ro(y,2q+3). The 2:1 Mux R(y,2q+4) has two inputs namely Ri(y,2q+4) and K4, and has one output Ro(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely Ro(y,2q+3) and Uo(y,2q+4), and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Ro(y,2q+4) and Uo(y,2q+3), and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and L4, and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and M4, and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Ro(y,2q+4), and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+4) and Ro(y,2q+3), and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Ri(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Ri(y,2q+4) of the stage (ring "y", stage "q+1"). The output

Bo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to the input Ui(y,2q+2) of the stage (ring "y", stage "q").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to the input Ri(x,2p+4) of the stage (ring "x", stage "p+1"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

In various embodiments, the inputs J1, K1, L1, and M1 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J2, K2, L2, and M2 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Similarly the inputs J3, K3, L3, and M3 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Finally the inputs J4, K4, L4, and M4 are connected from any of the outputs of any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The stage (ring "a", stage "s") consists of 8 inputs namely Ri(a,2s+1), Ri(a,2s+2), Ui(a,2s+1), Ui(a,2s+2), J5, K5, L5, and M5; and 4 outputs Bo(a,2s+1), Bo(a,2s+2), Fo(a,2s+1), and Fo(a,2s+2). The stage (ring "a", stage "s') also consists of eight 2:1 Muxes namely R(a,2s+1), R(a,2s+2), F(a,2s+1), F(a,2s+2), U(a,2s+1), U(a,2s+2), B(a,2s+1), and B(a,2s+2). The 2:1 Mux R(a,2s+1) has two inputs namely Ri(a,2s+1) and J5, and has one output Ro(a,2s+1). The 2:1 Mux R(a,2s+2) has two inputs namely Ri(a,2s+2) and K5, and has one output Ro(a,2s+2). The 2:1 Mux F(a,2s+1) has two inputs namely Ro(a,2s+1) and Uo(a,2s+2), and has one output Fo(a,2s+1). The 2:1 Mux F(a,2s+2) has two inputs namely Ro(a,2s+2) and Uo(a,2s+1), and has one output Fo(a,2s+2).

The 2:1 Mux U(a,2s+1) has two inputs namely Ui(a,2s+1) and L5, and has one output Uo(a,2s+1). The 2:1 Mux U(a,2s+2) has two inputs namely Ui(a,2s+2) and M5, and has one output Uo(a,2s+2). The 2:1 Mux B(a,2s+1) has two inputs namely

Uo(a,2s+1) and Ro(a,2s+2), and has one output Bo(a,2s+1). The 2:1 Mux B(a,2s+2) has two inputs namely Uo(a,2s+2) and Ro(a,2s+1), and has one output Bo(a,2s+2).

The stage (ring "b", stage "t") consists of 8 inputs namely Ri(b,2t+1), Ri(b,2t+2), Ui(b,2t+1), Ui(b,2t+2), J6, K6, L6, and M6; and 4 outputs Bo(b,2t+1), Bo(b,2t+2), Fo(b,2t+1), and Fo(b,2t+2). The stage (ring "b", stage "t') also consists of eight 2:1 Muxes namely R(b,2t+1), R(b,2t+2), F(b,2t+1), F(b,2t+2), U(b,2t+1), U(b,2t+2), B(b,2t+1), and B(b,2t+2). The 2:1 Mux R(b,2t+1) has two inputs namely Ri(b,2t+1) and J6, and has one output Ro(b,2t+1). The 2:1 Mux R(b,2t+2) has two inputs namely Ri(b,2t+2) and K6, and has one output Ro(b,2t+2). The 2:1 Mux F(b,2t+1) has two inputs namely Ro(b,2t+1) and Uo(b,2t+2), and has one output Fo(b,2t+1). The 2:1 Mux F(b,2t+2) has two inputs namely Ro(b,2t+2) and Uo(b,2t+1), and has one output Fo(b,2t+2).

The 2:1 Mux U(b,2t+1) has two inputs namely Ui(b,2t+1) and L6, and has one output Uo(b,2t+1). The 2:1 Mux U(b,2t+2) has two inputs namely Ui(b,2t+2) and M6, and has one output Uo(b,2t+2). The 2:1 Mux B(b,2t+1) has two inputs namely Uo(b,2t+1) and Ro(b,2t+2), and has one output Bo(b,2t+1). The 2:1 Mux B(b,2t+2) has two inputs namely Uo(b,2t+2) and Ro(b,2t+1), and has one output Bo(b,2t+2).

The wire Hop(1,1) starting from the output Fo(x,2p+2) of the stage (ring "x", stage "p") is also connected to L5 of the stage (ring "a", stage "s"), in addition to the input Ri(y,2q+4) of the stage (ring "y", stage "q+1"). The stage (ring "x", stage "p"), the stage (ring "a", stage "s"), and the stage (ring "y", stage "q+1") may belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Therefore the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may not be equal to the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "y", stage "q+1"). For example the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be one where as the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y+1") may be two. In such a case the wire Hop(1,1) is called hereinafter a "multi-drop hop wire". The wire Hop(1,1) may be either horizontal hop wire or vertical hop wire. Also multi-drop hop wires are

either horizontal external hop wires or vertical external hop wires. Similarly the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be any number greater than or equal to one, and also the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y+1") may be any number greater or equal to one.

In general a multi-drop hop wire may be dropping or terminating in more than one different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. For example a multi-drop hop wire starting from one block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ may be terminating at three different blocks or four different blocks, etc.

The wire Hop(1,2) starting from the output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is also connected to J6 of the stage (ring "b", stage "t"), in addition to the input Ui(y,2q+2) of the stage (ring "y", stage "q"). The wire Hop(1,2) is also an example of multi-drop hop wire when the stage (ring "x", stage "p+1"), the stage (ring "b", stage "t") and the stage (ring "y", stage "q") belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The wire Hop(2,1) starting from the output Fo(y,2q+2) of the stage (ring "y", stage "q") is also connected to M5 of the stage (ring "a", stage "s"), in addition to the input Ri(x,2p+4) of the stage (ring "x", stage "p+1"). The wire Hop(2,1) is also an example of multi-drop hop wire when the stage (ring "x", stage "p+1"), the stage (ring "a", stage "s") and the stage (ring "y", stage "q") belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The wire Hop(2,2) starting from the output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is also connected to K6 of the stage (ring "b", stage "t"), in addition to the input Ui(x,2p+2) of the stage (ring "x", stage "p"). The wire Hop(2,2) is also an example of multi-drop hop wire when the stage (ring "x", stage "p"), the stage (ring "b", stage "t") and the stage (ring "y", stage "q+1") belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

In various embodiments, the inputs J5, K5, L5, and M5 are connected from any of the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Also the inputs J6, K6, L6, and M6 are connected from any of the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

The diagram 600A of FIG. 6A and 600B of FIG. 6B are different embodiments of all the connections with multi-drop hop wires, between two arbitrary stages in two different rings of different blocks of 2D-grid 800. Referring to diagram 600A in FIG. 6A illustrates all the connections with multi-drop hop wires, between an arbitrary stage of a ring namely the stages (ring "x", stage "p"), and another arbitrary stage of any other ring namely the stages (ring "y", stage "q") of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. The multi-drop hop wires are also connected to another stage (ring "a", stage "s") belonging to a third block.

The stage (ring "x", stage "p") consists of 8 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), J1, K1, L1, and M1; and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of eight 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and J1 and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and K1 and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Uo(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+2) and Uo(x,2p+1) and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and L1 and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and M1 and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Ro(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+2) and Ro(x,2p+1) and has one output Bo(x,2p+2).

The stage (ring "y", stage "q") consists of 8 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), J3, K3, L3, and M3; and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of eight 2:1 Muxes namely R(y,2q+1), R(y,2q+2), F(y,2q+1), F(y,2q+2), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and J3 and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Ri(y,2q+2) and K3 and has one output Ro(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Ro(y,2q+1) and Uo(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Ro(y,2q+2) and Uo(y,2q+1) and has one output Fo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and L3, and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and M3, and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Ro(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+2) and Ro(y,2q+1) and has one output Bo(y,2q+2).

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Ri(y,2q+2) of the stage (ring "y", stage "q"). The output Bo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(1,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

The wire Hop(1,1) starting from the output Fo(x,2p+2) of the stage (ring "x", stage "p") is also connected to L2 of the stage (ring "a", stage "s"), in addition to the input Ri(y,2q+2) of the stage (ring "y", stage "q"). The stage (ring "x", stage "p"), the stage (ring "a", stage "s"), and the stage (ring "y", stage "q") may belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Therefore the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may not be equal to the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "y", stage "q"). For example the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be one where as the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y") may be two. Hence the wire

Hop(1,1) is a multi-drop hop wire. Also the wire Hop(1,1) is either horizontal external hop wire or vertical external hop wire. Similarly the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be any number greater than or equal to one, and also the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y") may be any number greater or equal to one.

The wire Hop(1,2) starting from the output Bo(y,2q+2) of the stage (ring "y", stage "q") is also connected to K2 of the stage (ring "a", stage "s"), in addition to the input Ui(x,2p+2) of the stage (ring "x", stage "p"). The wire Hop(1,2) is also an example of multi-drop hop wire when the stage (ring "x", stage "p"), the stage (ring "a", stage "s") and the stage (ring "y", stage "q") belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

In various embodiments, the inputs J2, K2, L2, and M2 are connected from any of the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Referring to diagram 600B in FIG. 6B illustrates all the connections with multi-drop hop wires, between an arbitrary stage of a ring namely the stages (ring "x", stage "p"), and another arbitrary stage of any other ring namely the stages (ring "y", stage "q") of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. The multi-drop hop wires are also connected to another stage (ring "a", stage "s") belonging to a third block.

The stage (ring "x", stage "p") consists of 8 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), J1, K1, L1, and M1; and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p') also consists of four 4:1 Muxes namely F(x,2p+1), F(x,2p+2), B(x,2p+1), and B(x,2p+2). The 4:1 Mux F(x,2p+1) has four inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+2), and J1 and has one output Fo(x,2p+1). The 4:1 Mux F(x,2p+2) has four inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), and K1 and has one output Fo(x,2p+2).

The 4:1 Mux B(x,2p+1) has four inputs namely Ui(x,2p+1), Ui(x,2p+2), Ri(x,2p+2), and L1 and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Ui(x,2p+1), Ui(x,2p+2), Ri(x,2p+1), and M1 and has one output Bo(x,2p+2).

The stage (ring "y", stage "q") consists of 8 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), J3, K3, L3, and M3; and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q') also consists of four 4:1 Muxes namely F(y,2q+1), F(y,2q+2), B(y,2q+1), and B(y,2q+2). The 4:1 Mux F(y,2q+1) has four inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+2), and J3 and has one output Fo(y,2q+1). The 4:1 Mux F(y,2q+2) has four inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), and K3 and has one output Fo(y,2q+2).

The 4:1 Mux B(y,2q+1) has four inputs namely Ui(y,2q+1), Ui(y,2q+2), Ri(y,2q+2), and L3, and has one output Bo(y,2q+1). The 4:1 Mux B(y,2q+2) has four inputs namely Ui(y,2q+1), Ui(y,2q+2), Ri(y,2q+1), and M3, and has one output Bo(y,2q+2).

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to the input Ri(y,2q+2) of the stage (ring "y", stage "q"). The output Bo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(1,2) to the input Ui(x,2p+2) of the stage (ring "x", stage "p").

The wire Hop(1,1) starting from the output Fo(x,2p+2) of the stage (ring "x", stage "p") is also connected to L2 and J2 of the stage (ring "a", stage "s"), in addition to the input Ri(y,2q+2) of the stage (ring "y", stage "q"). The stage (ring "x", stage "p"), the stage (ring "a", stage "s"), and the stage (ring "y", stage "q") may belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$. Therefore the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may not be equal to the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "y", stage "q"). For example the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be one where as the hop length between the blocks consisting of the

stage (ring "x", stage "p") and the stage (ring "q", stage "y") may be two. Hence the wire Hop(1,1) is a multi-drop hop wire. Also the wire Hop(1,1) is either horizontal external hop wire or vertical external hop wire. Similarly the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "a", stage "s") may be any number greater than or equal to one, and also the hop length between the blocks consisting of the stage (ring "x", stage "p") and the stage (ring "q", stage "y") may be any number greater or equal to one.

The wire Hop(1,2) starting from the output Bo(y,2q+2) of the stage (ring "y", stage "q") is also connected to K2 and M2 of the stage (ring "a", stage "s"), in addition to the input Ui(x,2p+2) of the stage (ring "x", stage "p"). The wire Hop(1,2) is also an example of multi-drop hop wire when the stage (ring "x", stage "p"), the stage (ring "a", stage "s") and the stage (ring "y", stage "q") belong to three different blocks of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

In various embodiments, the inputs J2, K2, L2, and M2 are connected from any of the multi-drop hop wires starting from any other stages of any ring of any block of the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$.

Referring to diagram 700A in FIG. 7A, illustrates, in one embodiment, the hop wire connections chart of a partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A or a partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B, or a partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C, with m = 6 and n = 7. The hop wire connections chart shows two rings namely ring 1 and ring 2. And there are m+1 = 7 stages in ring 1 and n+1 = 8 stages in ring 2.

The hop wire connections chart 700A illustrates how the hop wires are connected between any two successive stages of all the rings corresponding to a block of 2D-grid 800. "Lx" denotes an internal hop wire connection, where symbol "L" denotes internal hop wire and "x" is an integer. For example "L1" between the stages (ring 1, stage 0) and (ring 1, stage 1) denotes that the corresponding hop wires Hop(1,1), Hop(1,2), Hop(2,1),

and Hop(2,2) are connected to two successive stages of another ring in the same block or alternatively hop wires Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) are internal hop wires. Since there is also "L1" between the stages (ring 2, stage 0) and (ring 2, stage 1), there are internal hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected between the stages (ring 1, stage 0) and (ring 1, stage 1) and the stages (ring 2, stage 0) and (ring 2, stage 1). Hence there can be only two "L1" labels in the hop wire connection chart 700A.

Similarly there are two "L2" labels in the hop wire connections chart 700A. Since the label "L2" is given between the stages (ring 1, stage 5) and (ring 1, stage 6) and also the label "L2" is given between the stages (ring 2, stage 3) and (ring 2, stage 4), there are corresponding internal hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected between the stages (ring 1, stage 5) and (ring 1, stage 6) and the stages (ring 2, stage 3) and (ring 2, stage 4).

"Vx" denotes an external vertical hop wire, where symbol "V" denotes vertical external hop wire connections from blocks of the topmost row of 2D-grid 800 (i.e., row of blocks consisting of block (1,1), block (1,2), …., and block (1,10)) to the same corresponding stages of the same numbered ring of another block that is directly down south, with "x" vertical hop length, where "x" is a positive integer. For example "V1" between the stages (ring 1, stage 1) and (ring 1, stage 2) denote that from block (1,1) of 2D-grid 800 to another block directly below it, which is block (2,1), since "V1" denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 1) and (ring 1, stage 2) of block (1,1) to (ring 1, stage 1) and (ring 1, stage 2) of block (2,1). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 1) and (ring 1, stage 2) of block (3,1) to (ring 1, stage 1) and (ring 1, stage 2) of block (4,1). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 1) and (ring 1, stage 2) of block (9,1) to (ring 1, stage 1) and (ring 1, stage 2) of block (10,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

Similarly "V3" between the stages (ring 2, stage 1) and (ring 2, stage 2) denote that from block (1,1) of 2D-grid 800 to another block below it and at a hop length of 3 which is block (4,1), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 1) and (ring 2, stage 2) of block (1,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (4,1). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 1) and (ring 2, stage 2) of block (2,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (5,1). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 1) and (ring 2, stage 2) of block (7,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (10,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

If there is no block that is directly below a block with hop length equal to 3 then there is no vertical external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (8,1) does not have any block that is directly below and with hop length equal to 3 then none of the vertical external hop wires are connected from (ring 2, stage 1) and (ring 2, stage 2) of block (8,1). Similarly from (ring 2, stage 1) and (ring 2, stage 2) of block (9,1) and from (ring 2, stage 1) and (ring 2, stage 2) of block (10,1), none of the vertical external hop wires are connected. Similarly vertical external hop wires are connected corresponding to "V5", "V7" etc., labels given in the hop wire connections chart 700A.

"Ux" denotes an external vertical hop wire, where symbol "U" denotes vertical external hop wire connections starting from blocks that are "x" hop length below the topmost row of 2D-grid 800 (i.e., row of blocks consisting of block (1+x,1), block (1+x,2), …., and block (1+x,10)) to the same corresponding stages of the same numbered ring of another block that is directly down below, with "x" vertical hop length, where "x" is a positive integer. For example "U1" between the stages (ring 1, stage 2) and (ring 1, stage 3) denote that from block (2,1) of 2D-grid 800 to another block directly below it, which is block (3,1), since "U1" denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 2) and (ring 1, stage 3) of block (2,1) to (ring 1, stage 2) and (ring 1, stage 3) of block (3,1). It also

means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 2) and (ring 1, stage 3) of block (4,1) to (ring 1, stage 2) and (ring 1, stage 3) of block (5,1). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 2) and (ring 1, stage 3) of block (8,1) to (ring 1, stage 2) and (ring 1, stage 3) of block (9,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

If there is no block that is directly below a block with hop length equal to 1 then no vertical external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (10,1) does not have any block that is directly below and with hop length equal to 1 then none of the vertical external hop wires are connected from (ring 1, stage 2) and (ring 1, stage 3) of block (10,1). Similarly for all the blocks in each column from the topmost row up to the row "x", no vertical external hop wires are connected to the corresponding (ring 1, stage 2) and (ring 1, stage 3).

Similarly "U3" between the stages (ring 2, stage 2) and (ring 2, stage 3) denote that starting from blocks that are 3 hop length below the topmost row of 2D-grid 800 (i.e., row of blocks consisting of block (4,1), block (4,2), …., and block (4,10)) to the same corresponding stages of the same numbered ring of another block that is directly down below, with vertical hop length of 3, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected. For example from block (4,1) of 2D-grid 800 to another block below it and at a hop length of 3 which is block (7,1), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 2) and (ring 2, stage 3) of block (4,1) to (ring 2, stage 1) and (ring 2, stage 2) of block (7,1). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 2) and (ring 2, stage 3) of block (5,1) to (ring 2, stage 2) and (ring 2, stage 3) of block (8,1). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 2) and (ring 2, stage 3) of block (7,1) to (ring 2, stage 2) and (ring 2, stage 3) of block (10,1). The same pattern continues for all the columns starting from the block in the topmost row of each column.

If there is no block that is directly below a block with hop length equal to 3 then no vertical external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (8,1) does not have any block that is directly below and with hop length equal to 3 then none of the vertical external hop wires are connected from (ring 2, stage 2) and (ring 2, stage 3) of block (8,1). Similarly from (ring 2, stage 2) and (ring 2, stage 3) of block (9,1) and from (ring 2, stage 2) and (ring 2, stage 3) of block (10,1), none of the vertical external hop wires are connected. Similarly vertical external hop wires are connected corresponding to "U5", "U7" etc. labels given in the hop wire connections chart 700A.

"Hx" denotes an external horizontal hop wire, where symbol "H" denotes horizontal external hop wire connections from blocks of the leftmost column of 2D-grid 800 (i.e., column of blocks consisting of block (1,1), block (2,1), …., and block (10,1)) to the same corresponding stages of the same numbered ring of another block that is directly to the right, with "x" horizontal hop length, where "x" is a positive integer. For example "H1" between the stages (ring 1, stage 3) and (ring 1, stage 4) denote that from block (1,1) of 2D-grid 800 to another block directly to the right, which is block (1,2), since "H1" denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 3) and (ring 1, stage 4) of block (1,1) to (ring 1, stage 3) and (ring 1, stage 4) of block (1,2). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 3) and (ring 1, stage 4) of block (1,3) to (ring 1, stage 3) and (ring 1, stage 4) of block (1,4). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 3) and (ring 1, stage 4) of block (9,1) to (ring 1, stage 3) and (ring 1, stage 4) of block (10,1). The same pattern continues for all the rows starting from the block in the leftmost block of each row.

Similarly "H3" between the stages (ring 2, stage 4) and (ring 2, stage 5) denote that from block (1,1) of 2D-grid 800 to another block to the right and at a hop length of 3 which is block (1,4), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 4) and (ring 2, stage 5) of block (1,1) to (ring 2, stage 4) and (ring 2, stage 5) of block (1,4). It also means there are external hop wire

connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 4) and (ring 2, stage 5) of block (1,2) to (ring 2, stage 4) and (ring 2, stage 5) of block (1,5). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 4) and (ring 2, stage 5) of block (1,7) to (ring 2, stage 4) and (ring 2, stage 5) of block (1,10). The same pattern continues for all the columns starting from the block in the leftmost column of each row.

If there is no block that is directly to the right with hop length equal to 3 then there is no horizontal external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (1,8) does not have any block that is directly to the right and with hop length equal to 3 then none of the horizontal external hop wires are connected from (ring 2, stage 4) and (ring 2, stage 5) of block (1,8). Similarly from (ring 2, stage 4) and (ring 2, stage 5) of block (1,9) and from (ring 2, stage 4) and (ring 2, stage 5) of block (1,10), none of the horizontal external hop wires are connected. Similarly horizontal external hop wires are connected corresponding to "H5", "H7" etc., labels given in the hop wire connections chart 700A.

"Kx" denotes an external horizontal hop wire, where symbol "K" denotes horizontal external hop wire connections starting from blocks that are "x" hop length below the leftmost column of 2D-grid 800 (i.e., column of blocks consisting of block (1, 1+x), block (2, 1+x), …., and block (10, 1+x)) to the same corresponding stages of the same numbered ring of another block that is directly to the right, with "x" horizontal hop length, where "x" is a positive integer. For example "K1" between the stages (ring 1, stage 4) and (ring 1, stage 5) denote that from block (1,2) of 2D-grid 800 to another block directly to the right, which is block (1,3), since "K1" denotes hop length of 1, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 4) and (ring 1, stage 5) of block (1,2) to (ring 1, stage 4) and (ring 1, stage 5) of block (1,3). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 4) and (ring 1, stage 4) of block (1,4) to (ring 1, stage 4) and (ring 1, stage 5) of block (1,5). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 1, stage 4) and (ring 1, stage 5) of block (1,8) to (ring 1, stage 4) and (ring 1, stage 5) of

block (1,9). The same pattern continues for all the rows starting from the block in the leftmost column of each row.

If there is no block that is directly to the right of a block with hop length equal to 1 then no horizontal external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (1,10) does not have any block that is directly to the right and with hop length equal to 1 then none of the horizontal external hop wires are connected from (ring 1, stage 4) and (ring 1, stage 5) of block (1,10). Similarly for all the blocks in each row from the leftmost column up to the column "x", no horizontal external hop wires are connected to the corresponding (ring 1, stage 4) and (ring 1, stage 5).

Similarly "K3" between the stages (ring 2, stage 5) and (ring 2, stage 6) denote that starting from blocks that are 3 hop length to the right of the leftmost column of 2D-grid 800 (i.e., column of blocks consisting of block (1,4), block (2,4), …., and block (10,4)) to the same corresponding stages of the same numbered ring of another block that is directly to the right, with horizontal hop length of 3, there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) connected. For example from block (1,4) of 2D-grid 800 to another block to the right and at a hop length of 3 which is block (1,7), there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 5) and (ring 2, stage 6) of block (1,4) to (ring 2, stage 5) and (ring 2, stage 6) of block (1,7). It also means there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 5) and (ring 2, stage 6) of block (1,5) to (ring 2, stage 5) and (ring 2, stage 6) of block (1,8). This pattern continues and finally there are external hop wire connections Hop(1,1), Hop(1,2), Hop(2,1), and Hop(2,2) from (ring 2, stage 5) and (ring 2, stage 6) of block (1,7) to (ring 2, stage 5) and (ring 2, stage 6) of block (1,10). The same pattern continues for all the rows starting from the block in the leftmost block of each row.

If there is no block that is directly to the right of a block with hop length equal to 3 then no horizontal external hop wire connections is given corresponding to those two successive stages of the blocks. For example block (1,8) does not have any block that is directly to the right and with hop length equal to 3 then none of the horizontal external

hop wires are connected from (ring 2, stage 5) and (ring 2, stage 6) of block (1,8). Similarly from (ring 2, stage 5) and (ring 2, stage 6) of block (1,9) and from (ring 2, stage 5) and (ring 2, stage 6) of block (1,10), none of the horizontal external hop wires are connected. Similarly horizontal external hop wires are connected corresponding to "K5", "K7" etc. labels given in the hop wire connections chart 700A.

In general the hop length of an external vertical hop wire can be any positive number. Similarly the hop length of an external horizontal hop wire can be any positive number. The hop wire connections between two arbitrary successive stages in two different rings of the same block or two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, and 300E of FIG. 3E. Similarly the multi-drop hop wire connections between two arbitrary successive stages in two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 500A of FIG. 5A.

In accordance with the invention, the hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may also be any one of the embodiments of either the diagrams 400A of FIG. 4A and 400B of FIG. 4B. Similarly the multi-drop hop wire connections between two arbitrary stages in two different rings of different blocks may also be any one of the embodiments of either the diagrams 600A of FIG. 6A or 600B of FIG. 6B.

In accordance with the current invention, either partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100A of FIG. 1A or partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100B of FIG. 1B, or partial multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C, corresponding to a block of 2D-grid of blocks 800 of FIG. 8, using any one of the embodiments of 200A-200E of FIGs. 2A-2E to implement a stage of a ring of the multi-stage hierarchical network, either by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams

300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, 300E of FIG. 3E, 500A of FIG. 5A, or by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may be any one of the embodiments of either the diagrams 400A of FIG. 4A, 400B of FIG. 4B, 600A of FIG. 6A, or 600B of FIG. 6B is very efficient in the reduction of the die size, power consumption, and for lower wire/path delay for higher performance for practical routing applications to particularly to set up broadcast, unicast and multicast connections. In general in accordance with the current invention, where N_1 and N_2 of the complete multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ may be arbitrarily large in size and also the 2D-grid size 800 may also be arbitrarily large in size in terms of both the number of rows and number of columns.

Delay Optimizations in Multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$:

The multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ according to the current invention can further be optimized to reduce the delay in the routed path of the connection. The delay optimized multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ is hereinafter denoted by $V_{D-Comb}(N_1, N_2, d, s)$. The delay optimizing embodiments of the stages of a ring are one of the diagrams namely 900A-900E of FIGs. 9A-9D, 1000A-1000F of FIGs. 10A-10F, and 1100A-1100C of FIGs. 11A-11C. The diagram 1200 of FIG. 12, 1300 of FIG. 13, 1400 of FIG. 14, and 1500 of FIG. 15 are different embodiments for the implementation of delay optimizations with all the connections between two arbitrary successive stages in two different rings of the same block or two different rings of different blocks of 2D-grid 800.

FIG. 9A illustrates a stage (ring "k", stage "m") 900A consists of 5 inputs namely Fi(k,2m+1), Fi(k,2m+2), YFi(k,2m+1), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of seven 2:1 Muxes namely YF(k,2m+1), F(k,2m+1), F(k,2m+2), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The 2:1 Mux YF(k,2m+1) has two

inputs namely Fi(k,2m+1) and YFi(k,2m+1) and has one output YFo(k,2m+1). The 2:1 Mux F(k,2m+1) has two inputs namely YFo(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely YFo(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 9B illustrates a stage (ring "k", stage "m") 900B consists of 5 inputs namely Fi(k,2m+1), Fi(k,2m+2), YUi(k,2m+1), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of seven 2:1 Muxes namely F(k,2m+1), F(k,2m+2), YF(k,2m+1), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux YU(k,2m+1) has two inputs namely Ui(k,2m+1) and YUi(k,2m+1) and has one output YUo(k,2m+1). The 2:1 Mux U(k,2m+1) has two inputs namely YUo(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 9C illustrates a stage (ring "k", stage "m") 900C consists of 5 inputs namely Fi(k,2m+1), Fi(k,2m+2), UYi(k,2m+1), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of five 2:1 Muxes namely F(k,2m+1), F(k,2m+2), U(k,2m+2), B(k,2m+1),

and B(k,2m+2). The stage (ring "k", stage "m") also consists of one 3:1 Mux namely UY(k,2m+1). The 2:1 Mux F(k,2m+1) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Fi(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 3:1 Mux UY(k,2m+1) has three inputs namely Ui(k,2m+1), UYi(k,2m+1) and Fo(k,2m+1) and has one output UYo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 9D illustrates a stage (ring "k", stage "m") 900D consists of 6 inputs namely Fi(k,2m+1), Fi(k,2m+2), YFi(k,2m+1), Ui(k,2m+1), Ui(k,2m+2), and YUi(k,2m+1); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of eight 2:1 Muxes namely F(k,2m+1), F(k,2m+2), YF(k,2m+1), U(k,2m+1), U(k,2m+2), YU(k,2m+1), B(k,2m+1), and B(k,2m+2). The 2:1 Mux YF(k,2m+1) has two inputs namely Fi(k,2m+1) and YFi(k,2m+1) and has one output YFo(k,2m+1). The 2:1 Mux F(k,2m+1) has two inputs namely YFo(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely YFo(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux YU(k,2m+1) has two inputs namely Ui(k,2m+1) and YUi(k,2m+1) and has one output YUo(k,2m+1). The 2:1 Mux U(k,2m+1) has two inputs namely YUo(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 9E illustrates a stage (ring "k", stage "m") 900E consists of 6 inputs namely Fi(k,2m+1), Fi(k,2m+2), YFi(k,2m+1), Ui(k,2m+1), Ui(k,2m+2), and UYi(k,2m+1); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k",

stage "m") also consists of six 2:1 Muxes namely F(k,2m+1), F(k,2m+2), YF(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The stage (ring "k", stage "m") also consists of one 3:1 Mux namely UY(k,2m+1). The 2:1 Mux YF(k,2m+1) has two inputs namely Fi(k,2m+1) and YFi(k,2m+1) and has one output YFo(k,2m+1). The 2:1 Mux F(k,2m+1) has two inputs namely YFo(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely YFo(k,2m+1) and Fi(k,2m+2) and has one output Fo(k,2m+2).

The 3:1 Mux UY(k,2m+1) has three inputs namely Ui(k,2m+1), UYi(k,2m+1) and Fo(k,2m+1) and has one output UYo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 10A illustrates a stage (ring "k", stage "m") 1000A consists of 5 inputs namely Ri(k,2m+1), Ri(k,2m+2), YRi(k,2m+1), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of nine 2:1 Muxes namely R(k,2m+1), R(k,2m+2), YR(k,2m+1), F(k,2m+1), F(k,2m+2), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The 2:1 Mux YR(k,2m+1) has two inputs namely Ri(k,2m+1) and YRi(k,2m+1) and has one output YRo(k,2m+1). The 2:1 Mux R(k,2m+1) has two inputs namely YRo(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux

B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 10B illustrates a stage (ring "k", stage "m") 1000B consists of 5 inputs namely Ri(k,2m+1), Ri(k,2m+2), RYi(k,2m+1), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of seven 2:1 Muxes namely R(k,2m+2), F(k,2m+1), F(k,2m+2), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The stage (ring "k", stage "m") also consists of one 3:1 Mux namely RY(k,2m+1). The 3:1 Mux RY(k,2m+1) has three inputs namely Ri(k,2m+1), RYi(k,2m+1), and Bo(k,2m+1), and has one output RYo(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely RYo(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely RYo(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 10C illustrates a stage (ring "k", stage "m") 1000C consists of 5 inputs namely Ri(k,2m+1), Ri(k,2m+2), Ui(k,2m+1), Ui(k,2m+2), and YUi(k,2m+1); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of nine 2:1 Muxes namely R(k,2m+1), R(k,2m+2), F(k,2m+1), F(k,2m+2), YU(k,2m+1), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The 2:1 Mux R(k,2m+1) has two inputs namely Ri(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux YU(k,2m+1) has two inputs namely Ui(k,2m+1) and YUi(k,2m+1) and has one output YUo(k,2m+1). The 2:1 Mux U(k,2m+1) has two inputs namely YUo(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 10D illustrates a stage (ring "k", stage "m") 1000D consists of 5 inputs namely Ri(k,2m+1), Ri(k,2m+2), Ui(k,2m+1), Ui(k,2m+2), and UYi(k,2m+1); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of seven 2:1 Muxes namely R(k,2m+1), R(k,2m+2), F(k,2m+1), F(k,2m+2), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The stage (ring "k", stage "m") also consists of one 3:1 Mux namely UY(k,2m+1). The 2:1 Mux R(k,2m+1) has two inputs namely Ri(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+2).

The 3:1 Mux UY(k,2m+1) has three inputs namely Ui(k,2m+1), UYi(k,2m+1), and Fo(k,2m+1), and has one output UYo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 10E illustrates a stage (ring "k", stage "m") 1000E consists of 6 inputs namely Ri(k,2m+1), Ri(k,2m+2), YRi(k,2m+1), Ui(k,2m+1), Ui(k,2m+2), and YUi(k,2m+1); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of ten 2:1 Muxes namely YR(k,2m+1), R(k,2m+1), R(k,2m+2), F(k,2m+1), F(k,2m+2), YU(k,2m+1), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The 2:1 Mux YR(k,2m+1) has two inputs namely

Ri(k,2m+1) and YRi(k,2m+1) and has one output YRo(k,2m+1). The 2:1 Mux R(k,2m+1) has two inputs namely YRo(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+2).

The 2:1 Mux YU(k,2m+1) has two inputs namely Ui(k,2m+1) and YUi(k,2m+1) and has one output YUo(k,2m+1). The 2:1 Mux U(k,2m+1) has two inputs namely YUo(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 10F illustrates a stage (ring "k", stage "m") 1000F consists of 6 inputs namely Ri(k,2m+1), Ri(k,2m+2), RYi(k,2m+1), Ui(k,2m+1), Ui(k,2m+2), and UYi(k,2m+1); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of six 2:1 Muxes namely R(k,2m+2), F(k,2m+1), F(k,2m+2), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The stage (ring "k", stage "m") also consists of two 3:1 Mux namely RY(k,2m+1) and UY(k,2m+1). The 3:1 Mux RY(k,2m+1) has three inputs namely Ri(k,2m+1), RYi(k,2m+1), and Bo(k,2m+1) and has one output RYo(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely RYo(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely RYo(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+2).

The 3:1 Mux UY(k,2m+1) has three inputs namely Ui(k,2m+1), UYi(k,2m+1), and Fo(k,2m+1), and has one output UYo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one

output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely UYo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 11A illustrates a stage (ring "k", stage "m") 1100A consists of 5 inputs namely Ri(k,2m+1), Ri(k,2m+2), FYi(k,2m+2), Ui(k,2m+1), and Ui(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of seven 2:1 Muxes namely R(k,2m+1), R(k,2m+2), F(k,2m+1), U(k,2m+1), U(k,2m+2), B(k,2m+1), and B(k,2m+2). The stage (ring "k", stage "m") also consists of one 3:1 Mux namely FY(k,2m+2). The 2:1 Mux R(k,2m+1) has two inputs namely Ri(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 3:1 Mux FY(k,2m+2) has three inputs namely Ro(k,2m+1), Ro(k,2m+2), and FYi(k,2m+2), and has one output FYo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and FYo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 2:1 Mux B(k,2m+2) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+2).

FIG. 11B illustrates a stage (ring "k", stage "m") 1100B consists of 5 inputs namely Ri(k,2m+1), Ri(k,2m+2), Ui(k,2m+1), Ui(k,2m+2), and BYi(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of seven 2:1 Muxes namely R(k,2m+1), R(k,2m+2), F(k,2m+1), F(k,2m+2), U(k,2m+1), U(k,2m+2), and B(k,2m+1). The stage (ring "k", stage "m") also consists of one 3:1 Mux namely BY(k,2m+2). The 2:1 Mux R(k,2m+1) has two inputs namely Ri(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 2:1 Mux F(k,2m+2) has two inputs namely Ro(k,2m+1), and Ro(k,2m+2), and has one output Fo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and Fo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 3:1 Mux BY(k,2m+2) has three inputs namely Uo(k,2m+1), Uo(k,2m+2), and BYi(k,2m+2), and has one output BYo(k,2m+2).

FIG. 11C illustrates a stage (ring "k", stage "m") 1100C consists of 6 inputs namely Ri(k,2m+1), Ri(k,2m+2), FYi(k,2m+2), Ui(k,2m+1), Ui(k,2m+2), and BYi(k,2m+2); and 4 outputs Bo(k,2m+1), Bo(k,2m+2), Fo(k,2m+1), and Fo(k,2m+2). The stage (ring "k", stage "m") also consists of six 2:1 Muxes namely R(k,2m+1), R(k,2m+2), F(k,2m+1), U(k,2m+1), U(k,2m+2), and B(k,2m+1). The stage (ring "k", stage "m") also consists of two 3:1 Muxes namely FY(k,2m+2) and BY(k,2m+2). The 2:1 Mux R(k,2m+1) has two inputs namely Ri(k,2m+1) and Bo(k,2m+1) and has one output Ro(k,2m+1). The 2:1 Mux R(k,2m+2) has two inputs namely Ri(k,2m+2) and Bo(k,2m+2) and has one output Ro(k,2m+2). The 2:1 Mux F(k,2m+1) has two inputs namely Ro(k,2m+1) and Ro(k,2m+2) and has one output Fo(k,2m+1). The 3:1 Mux FY(k,2m+2) has three inputs namely Ro(k,2m+1), Ro(k,2m+2), and FYi(k,2m+2), and has one output FYo(k,2m+2).

The 2:1 Mux U(k,2m+1) has two inputs namely Ui(k,2m+1) and Fo(k,2m+1) and has one output Uo(k,2m+1). The 2:1 Mux U(k,2m+2) has two inputs namely Ui(k,2m+2) and FYo(k,2m+2) and has one output Uo(k,2m+2). The 2:1 Mux B(k,2m+1) has two inputs namely Uo(k,2m+1) and Uo(k,2m+2) and has one output Bo(k,2m+1). The 3:1 Mux BY(k,2m+2) has three inputs namely Uo(k,2m+1), Uo(k,2m+2), and BYi(k,2m+2) and has one output BYo(k,2m+2).

Referring to diagram 1200 in FIG. 12, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 5 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), and UYi(x,2p+1); and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p") also consists of seven 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The stage (ring "x", stage "p") also consists of one 3:1 Mux namely UY(x,2p+1). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and Bo(x,2p+1) and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and Bo(x,2p+2) and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Ro(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+1) and Ro(x,2p+2) and has one output Fo(x,2p+2).

The 3:1 Mux UY(x,2p+1) has three inputs namely Ui(x,2p+1), UYi(x,2p+1), and Fo(x,2p+1), and has one output UYo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely UYo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely UYo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 5 inputs namely Ri(x,2p+3), Ri(x,2p+4), RYi(x,2p+3), Ui(x,2p+3), and Ui(x,2p+4); and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of seven 2:1 Muxes namely R(x,2p+4), F(x,2p+3), F(x,2p+4), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The stage (ring "x", stage "p+1") also consists of one 3:1 Mux namely RY(x,2p+3). The 3:1 Mux RY(x,2p+3) has three inputs namely Ri(x,2p+3), RYi(x,2p+3), and Bo(x,2p+3), and has one output RYo(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs namely Ri(x,2p+4) and Bo(x,2p+4) and has one output Ro(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely RYo(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely RYo(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and Fo(x,2p+3) and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4)

and Fo(x,2p+4) and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Ri(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 5 inputs namely Ri(y,2q+1), Ri(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), and YUi(y,2q+1); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q") also consists of nine 2:1 Muxes namely R(y,2q+1), R(y,2q+2), F(y,2q+1), F(y,2q+2), YU(y,2q+1), U(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and Bo(y,2q+1) and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Ri(y,2q+2) and Bo(y,2q+2) and has one output Ro(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Ro(y,2q+1) and Ro(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Ro(y,2q+1) and Ro(y,2q+2) and has one output Fo(y,2q+2).

The 2:1 Mux YU(y,2q+1) has two inputs namely Ui(y,2q+1) and YUi(y,2q+1) and has one output YUo(y,2q+1). The 2:1 Mux U(y,2q+1) has two inputs namely YUo(y,2q+1) and Fo(y,2q+1) and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 5 inputs namely Ri(y,2q+3), Ri(y,2q+4), YRi(y,2q+3), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of nine 2:1 Muxes namely R(y,2q+3), R(y,2q+4), YR(y,2q+3), F(y,2q+3), F(y,2q+4),

U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux YR(y,2q+3) has two inputs namely Ri(y,2q+3) and YRi(y,2q+3) and has one output YRo(y,2q+3). The 2:1 Mux R(y,2q+3) has two inputs namely YRo(y,2q+3) and Bo(y,2q+3) and has one output Ro(y,2q+3). The 2:1 Mux R(y,2q+4) has two inputs namely Ri(y,2q+4) and Bo(y,2q+4) and has one output Ro(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely Ro(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely Ro(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring “y”, stage “q”) is connected to the input Ri(y,2q+3) of the stage (ring “y”, stage “q+1”). And the output Bo(y,2q+3) of the stage (ring “y”, stage “q+1”) is connected to the input Ui(y,2q+1) of the stage (ring “y”, stage “q”).

The output Fo(x,2p+2) of the stage (ring “x”, stage “p”) is connected via the wire Hop(1,1) to two inputs namely input Ri(y,2q+4) of the stage (ring “y”, stage “q+1”) and input YUi(y,2q+1) of the stage (ring “y”, stage “q”). The output Bo(x,2p+4) of the stage (ring “x”, stage “p+1”) is connected via the wire Hop(1,2) to two inputs namely input Ui(y,2q+2) of the stage (ring “y”, stage “q”) and input YRi(y,2q+3) of the stage (ring “y”, stage “q+1”).

The output Fo(y,2q+2) of the stage (ring “y”, stage “q”) is connected via the wire Hop(2,1) to two inputs namely input Ri(x,2p+4) of the stage (ring “x”, stage “p+1”) and input UYi(x,2p+1) of the stage (ring “x”, stage “p”). The output Bo(y,2q+4) of the stage (ring “y”, stage “q+1”) is connected via the wire Hop(2,2) to two inputs namely input Ui(x,2p+2) of the stage (ring “x”, stage “p”) and input RYi(x,2p+3) of the stage (ring “x”, stage “p+1”).

Referring to diagram 1300 in FIG. 13, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 6 inputs namely Fi(x,2p+1), Fi(x,2p+2), YFi(x,2p+1), Ui(x,2p+1), Ui(x,2p+2), and YUi(x,2p+1); and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p") also consists of eight 2:1 Muxes namely F(x,2p+1), F(x,2p+2), YF(x,2p+1), U(x,2p+1), U(x,2p+2), YU(x,2p+1), B(x,2p+1), and B(x,2p+2). The 2:1 Mux YF(x,2p+1) has two inputs namely Fi(x,2p+1) and YFi(x,2p+1) and has one output YFo(x,2p+1). The 2:1 Mux F(x,2p+1) has two inputs namely YFo(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely YFo(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+2).

The 2:1 Mux YU(x,2p+1) has two inputs namely Ui(x,2p+1) and YUi(x,2p+1) and has one output YUo(x,2p+1). The 2:1 Mux U(x,2p+1) has two inputs namely YUo(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 6 inputs namely Ri(x,2p+3), Ri(x,2p+4), YRi(x,2p+3), Ui(x,2p+3), Ui(x,2p+4), and YUi(x,2p+3); and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of ten 2:1 Muxes namely YR(x,2p+3), R(x,2p+3), R(x,2p+4), F(x,2p+3), F(x,2p+4), YU(x,2p+3), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The 2:1 Mux YR(x,2p+3) has two inputs namely Ri(x,2p+3) and YRi(x,2p+3) and has one output YRo(x,2p+3). The 2:1 Mux R(x,2p+3) has two inputs namely YRo(x,2p+3) and Bo(x,2p+3) and has one output Ro(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs namely Ri(x,2p+4) and Bo(x,2p+4) and has one output Ro(x,2p+4). The 2:1 Mux

F(x,2p+3) has two inputs namely Ro(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely Ro(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+4).

The 2:1 Mux YU(x,2p+3) has two inputs namely Ui(x,2p+3) and YUi(x,2p+3) and has one output YUo(x,2p+3). The 2:1 Mux U(x,2p+3) has two inputs namely YUo(x,2p+3) and Fo(x,2p+3) and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and Fo(x,2p+4) and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Ri(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 6 inputs namely Fi(y,2q+1), Fi(y,2q+2), YFi(y,2q+1), Ui(y,2q+1), Ui(y,2q+2), and UYi(y,2q+1); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q") also consists of six 2:1 Muxes namely F(y,2q+1), F(y,2q+2), YF(y,2q+1), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The stage (ring "y", stage "q") also consists of one 3:1 Mux namely UY(y,2q+1). The 2:1 Mux YF(y,2q+1) has two inputs namely Fi(y,2q+1) and YFi(y,2q+1) and has one output YFo(y,2q+1). The 2:1 Mux F(y,2q+1) has two inputs namely YFo(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely YFo(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+2).

The 3:1 Mux UY(y,2q+1) has three inputs namely Ui(y,2q+1), UYi(y,2q+1) and Fo(y,2q+1) and has one output UYo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely UYo(y,2q+1) and Uo(y,2q+2) and has one output

Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely UYo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 6 inputs namely Ri(y,2q+3), Ri(y,2q+4), RYi(y,2q+3), Ui(y,2q+3), Ui(y,2q+4), and UYi(y,2q+3); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "2q+1") also consists of six 2:1 Muxes namely R(y,2q+4), F(y,2q+3), F(y,2q+4), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The stage (ring "y", stage "2q+1") also consists of two 3:1 Mux namely RY(y,2q+3) and UY(y,2q+3). The 3:1 Mux RY(y,2q+3) has three inputs namely Ri(y,2q+3), RYi(y,2q+3), and Bo(y,2q+3) and has one output RYo(y,2q+3). The 2:1 Mux R(y,2q+4) has two inputs namely Ri(y,2q+4) and Bo(y,2q+4) and has one output Ro(y,2q+4). The 2:1 Mux F(y,2q+3) has two inputs namely RYo(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely RYo(y,2q+3) and Ro(y,2q+4) and has one output Fo(y,2q+4).

The 3:1 Mux UY(y,2q+3) has three inputs namely Ui(y,2q+3), UYi(y,2q+3), and Fo(y,2q+3), and has one output UYo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely UYo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely UYo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Ri(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to two inputs namely input Ri(y,2q+4) of the stage (ring "y", stage "q+1") and input UYi(y,2q+1) of the stage (ring "y", stage "q"). The output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to two inputs namely input Ui(y,2q+2) of the stage (ring "y", stage "q") and input RYi(y,2q+3) of the stage (ring "y", stage "q+1").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to two inputs namely input Ri(x,2p+4) of the stage (ring "x", stage "p+1") and input YUi(x,2p+1) of the stage (ring "x", stage "p"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to two inputs namely input Ui(x,2p+2) of the stage (ring "x", stage "p") and input YRi(x,2p+3) of the stage (ring "x", stage "p+1").

Referring to diagram 1400 in FIG. 14, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 5 inputs namely Fi(x,2p+1), Fi(x,2p+2), YUi(x,2p+1), Ui(x,2p+1), and Ui(x,2p+2); and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p") also consists of seven 2:1 Muxes namely F(x,2p+1), F(x,2p+2), YF(x,2p+1), U(x,2p+1), U(x,2p+2), B(x,2p+1), and B(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Fi(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Fi(x,2p+1) and Fi(x,2p+2) and has one output Fo(x,2p+2).

The 2:1 Mux YU(x,2p+1) has two inputs namely Ui(x,2p+1) and YUi(x,2p+1) and has one output YUo(x,2p+1). The 2:1 Mux U(x,2p+1) has two inputs namely YUo(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 2:1 Mux B(x,2p+2) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 5 inputs namely Fi(x,2p+3), Fi(x,2p+4), YFi(x,2p+3), Ui(x,2p+3), and Ui(x,2p+4); and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of seven 2:1 Muxes namely YF(x,2p+3), F(x,2p+3), F(x,2p+4), U(x,2p+3), U(x,2p+4),

B(x,2p+3), and B(x,2p+4). The 2:1 Mux YF(x,2p+3) has two inputs namely Fi(x,2p+3) and YFi(x,2p+3) and has one output YFo(x,2p+3). The 2:1 Mux F(x,2p+3) has two inputs namely YFo(x,2p+3) and Fi(x,2p+4) and has one output Fo(x,2p+3). The 2:1 Mux F(x,2p+4) has two inputs namely YFo(x,2p+3) and Fi(x,2p+4) and has one output Fo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and Fo(x,2p+3) and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and Fo(x,2p+4) and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Fi(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 5 inputs namely Fi(y,2q+1), Fi(y,2q+2), UYi(y,2q+1), Ui(y,2q+1), and Ui(y,2q+2); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q") also consists of five 2:1 Muxes namely F(y,2q+1), F(y,2q+2), U(y,2q+2), B(y,2q+1), and B(y,2q+2). The stage (ring "y", stage "q") also consists of one 3:1 Mux namely UY(y,2q+1). The 2:1 Mux F(y,2q+1) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+1). The 2:1 Mux F(y,2q+2) has two inputs namely Fi(y,2q+1) and Fi(y,2q+2) and has one output Fo(y,2q+2).

The 3:1 Mux UY(y,2q+1) has three inputs namely Ui(y,2q+1), UYi(y,2q+1) and Fo(y,2q+1) and has one output UYo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2) and Fo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely UYo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 2:1 Mux B(y,2q+2) has two inputs namely UYo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 5 inputs namely Fi(y,2q+3), Fi(y,2q+4), YFi(y,2q+3), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of seven 2:1 Muxes namely YF(y,2q+3), F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux YF(y,2q+3) has two inputs namely Fi(y,2q+3) and YFi(y,2q+3) and has one output YFo(y,2q+3). The 2:1 Mux F(y,2q+3) has two inputs namely YFo(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely YFo(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Fi(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to two inputs namely input Fi(y,2q+4) of the stage (ring "y", stage "q+1") and input UYi(y,2q+1) of the stage (ring "y", stage "q"). The output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to two inputs namely input Ui(y,2q+2) of the stage (ring "y", stage "q") and input YFi(y,2q+3) of the stage (ring "y", stage "q+1").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to two inputs namely input Fi(x,2p+4) of the stage (ring "x", stage "p+1") and input YUi(x,2p+1) of the stage (ring "x", stage "p"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to two inputs namely input

Ui(x,2p+2) of the stage (ring "x", stage "p") and input YFi(x,2p+3) of the stage (ring "x", stage "p+1").

Referring to diagram 1500 in FIG. 15, illustrates all the connections between two arbitrary successive stages of a ring namely the stages (ring "x", stage "p") and (ring "x", stage "p+1") and two other arbitrary successive stages of any other ring namely the stages (ring "y", stage "q") and (ring "y", stage "q+1"), of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$.

The stage (ring "x", stage "p") consists of 5 inputs namely Ri(x,2p+1), Ri(x,2p+2), Ui(x,2p+1), Ui(x,2p+2), and BYi(x,2p+2); and 4 outputs Bo(x,2p+1), Bo(x,2p+2), Fo(x,2p+1), and Fo(x,2p+2). The stage (ring "x", stage "p") also consists of seven 2:1 Muxes namely R(x,2p+1), R(x,2p+2), F(x,2p+1), F(x,2p+2), U(x,2p+1), U(x,2p+2), and B(x,2p+1). The stage (ring "x", stage "p") also consists of one 3:1 Mux namely BY(x,2p+2). The 2:1 Mux R(x,2p+1) has two inputs namely Ri(x,2p+1) and Bo(x,2p+1) and has one output Ro(x,2p+1). The 2:1 Mux R(x,2p+2) has two inputs namely Ri(x,2p+2) and Bo(x,2p+2) and has one output Ro(x,2p+2). The 2:1 Mux F(x,2p+1) has two inputs namely Ro(x,2p+1) and Ro(x,2p+2) and has one output Fo(x,2p+1). The 2:1 Mux F(x,2p+2) has two inputs namely Ro(x,2p+1), and Ro(x,2p+2), and has one output Fo(x,2p+2).

The 2:1 Mux U(x,2p+1) has two inputs namely Ui(x,2p+1) and Fo(x,2p+1) and has one output Uo(x,2p+1). The 2:1 Mux U(x,2p+2) has two inputs namely Ui(x,2p+2) and Fo(x,2p+2) and has one output Uo(x,2p+2). The 2:1 Mux B(x,2p+1) has two inputs namely Uo(x,2p+1) and Uo(x,2p+2) and has one output Bo(x,2p+1). The 3:1 Mux BY(x,2p+2) has three inputs namely Uo(x,2p+1), Uo(x,2p+2), and BYi(x,2p+2), and has one output BYo(x,2p+2).

The stage (ring "x", stage "p+1") consists of 5 inputs namely Ri(x,2p+3), Ri(x,2p+4), FYi(x,2p+4), Ui(x,2p+3), and Ui(x,2p+4); and 4 outputs Bo(x,2p+3), Bo(x,2p+4), Fo(x,2p+3), and Fo(x,2p+4). The stage (ring "x", stage "p+1") also consists of seven 2:1 Muxes namely R(x,2p+3), R(x,2p+4), F(x,2p+3), U(x,2p+3), U(x,2p+4), B(x,2p+3), and B(x,2p+4). The stage (ring "x", stage "p+1") also consists of one 3:1 Mux

namely FY(x,2p+4). The 2:1 Mux R(x,2p+3) has two inputs namely Ri(x,2p+3) and Bo(x,2p+3) and has one output Ro(x,2p+3). The 2:1 Mux R(x,2p+4) has two inputs namely Ri(x,2p+4) and Bo(x,2p+4) and has one output Ro(x,2p+4). The 2:1 Mux F(x,2p+3) has two inputs namely Ro(x,2p+3) and Ro(x,2p+4) and has one output Fo(x,2p+3). The 3:1 Mux FY(x,2p+4) has three inputs namely Ro(x,2p+3), Ro(x,2p+4), and FYi(x,2p+4), and has one output FYo(x,2p+4).

The 2:1 Mux U(x,2p+3) has two inputs namely Ui(x,2p+3) and Fo(x,2p+3) and has one output Uo(x,2p+3). The 2:1 Mux U(x,2p+4) has two inputs namely Ui(x,2p+4) and FYo(x,2p+4) and has one output Uo(x,2p+4). The 2:1 Mux B(x,2p+3) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+3). The 2:1 Mux B(x,2p+4) has two inputs namely Uo(x,2p+3) and Uo(x,2p+4) and has one output Bo(x,2p+4).

The output Fo(x,2p+1) of the stage (ring "x", stage "p") is connected to the input Ri(x,2p+3) of the stage (ring "x", stage "p+1"). And the output Bo(x,2p+3) of the stage (ring "x", stage "p+1") is connected to the input Ui(x,2p+1) of the stage (ring "x", stage "p").

The stage (ring "y", stage "q") consists of 6 inputs namely Ri(y,2q+1), Ri(y,2q+2), FYi(y,2q+2), Ui(y,2q+1), Ui(y,2q+2), and BYi(y,2q+2); and 4 outputs Bo(y,2q+1), Bo(y,2q+2), Fo(y,2q+1), and Fo(y,2q+2). The stage (ring "y", stage "q") also consists of six 2:1 Muxes namely R(y,2q+1), R(y,2q+2), F(y,2q+1), U(y,2q+1), U(y,2q+2), and B(y,2q+1). The stage (ring "y", stage "q") also consists of two 3:1 Muxes namely FY(y,2q+2) and BY(y,2q+2). The 2:1 Mux R(y,2q+1) has two inputs namely Ri(y,2q+1) and Bo(y,2q+1) and has one output Ro(y,2q+1). The 2:1 Mux R(y,2q+2) has two inputs namely Ri(y,2q+2) and Bo(y,2q+2) and has one output Ro(y,2q+2). The 2:1 Mux F(y,2q+1) has two inputs namely Ro(y,2q+1) and Ro(y,2q+2) and has one output Fo(y,2q+1). The 3:1 Mux FY(y,2q+2) has three inputs namely Ro(y,2q+1), Ro(y,2q+2), and FYi(y,2q+2), and has one output FYo(y,2q+2).

The 2:1 Mux U(y,2q+1) has two inputs namely Ui(y,2q+1) and Fo(y,2q+1) and has one output Uo(y,2q+1). The 2:1 Mux U(y,2q+2) has two inputs namely Ui(y,2q+2)

and FYo(y,2q+2) and has one output Uo(y,2q+2). The 2:1 Mux B(y,2q+1) has two inputs namely Uo(y,2q+1) and Uo(y,2q+2) and has one output Bo(y,2q+1). The 3:1 Mux BY(y,2q+2) has three inputs namely Uo(y,2q+1), Uo(y,2q+2), and BYi(y,2q+2) and has one output BYo(y,2q+2).

The stage (ring "y", stage "q+1") consists of 5 inputs namely Fi(y,2q+3), Fi(y,2q+4), YFi(y,2q+3), Ui(y,2q+3), and Ui(y,2q+4); and 4 outputs Bo(y,2q+3), Bo(y,2q+4), Fo(y,2q+3), and Fo(y,2q+4). The stage (ring "y", stage "q+1") also consists of seven 2:1 Muxes namely YF(y,2q+3), F(y,2q+3), F(y,2q+4), U(y,2q+3), U(y,2q+4), B(y,2q+3), and B(y,2q+4). The 2:1 Mux YF(y,2q+3) has two inputs namely Fi(y,2q+3) and YFi(y,2q+3) and has one output YFo(y,2q+3). The 2:1 Mux F(y,2q+3) has two inputs namely YFo(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+3). The 2:1 Mux F(y,2q+4) has two inputs namely YFo(y,2q+3) and Fi(y,2q+4) and has one output Fo(y,2q+4).

The 2:1 Mux U(y,2q+3) has two inputs namely Ui(y,2q+3) and Fo(y,2q+3) and has one output Uo(y,2q+3). The 2:1 Mux U(y,2q+4) has two inputs namely Ui(y,2q+4) and Fo(y,2q+4) and has one output Uo(y,2q+4). The 2:1 Mux B(y,2q+3) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+3). The 2:1 Mux B(y,2q+4) has two inputs namely Uo(y,2q+3) and Uo(y,2q+4) and has one output Bo(y,2q+4).

The output Fo(y,2q+1) of the stage (ring "y", stage "q") is connected to the input Fi(y,2q+3) of the stage (ring "y", stage "q+1"). And the output Bo(y,2q+3) of the stage (ring "y", stage "q+1") is connected to the input Ui(y,2q+1) of the stage (ring "y", stage "q").

The output Fo(x,2p+2) of the stage (ring "x", stage "p") is connected via the wire Hop(1,1) to two inputs namely input Fi(y,2q+4) of the stage (ring "y", stage "q+1") and input BYi(y,2q+1) of the stage (ring "y", stage "q"). The output Bo(x,2p+4) of the stage (ring "x", stage "p+1") is connected via the wire Hop(1,2) to two inputs namely input Ui(y,2q+2) of the stage (ring "y", stage "q") and input YFi(y,2q+3) of the stage (ring "y", stage "q+1").

The output Fo(y,2q+2) of the stage (ring "y", stage "q") is connected via the wire Hop(2,1) to two inputs namely input Ri(x,2p+4) of the stage (ring "x", stage "p+1") and input BYi(x,2p+1) of the stage (ring "x", stage "p"). The output Bo(y,2q+4) of the stage (ring "y", stage "q+1") is connected via the wire Hop(2,2) to two inputs namely input Ui(x,2p+2) of the stage (ring "x", stage "p") and input YFi(x,2p+4) of the stage (ring "x", stage "p+1").

In accordance with the current invention, either partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100A of FIG. 1A, or partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100B of FIG. 1B, or partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C, corresponding to a block of 2D-grid of blocks 800 of FIG. 8, using any one of the embodiments of 200A-200F of FIGs. 2A-2F, 900A-900E of FIGs. 9A-9E, 1000A-1000F of FIGs. 10A-10F, 1100A-1100C of FIGs. 11A-11C to implement a stage of a ring of the multi-stage hierarchical network, either by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, 300E of FIG. 3E, 500A of FIG. 5A, 1200 of FIG. 12, 1300 of FIG. 13, 1400 of FIG. 14, and 1500 of FIG. 15 or by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may be any one of the embodiments of either the diagrams 400A of FIG. 4A, 400B of FIG. 4B, 600A of FIG. 6A, or 600B of FIG. 6B is very efficient in the reduction of the die size, power consumption, and highly optimized for lower wire/path delay for higher performance for practical routing applications to particularly to set up broadcast, unicast and multicast connections. In general in accordance with the current invention, where N_1 and N_2 of the complete multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ may be arbitrarily large in size and also the 2D-grid size 800 may also be arbitrarily large in size in terms of both the number of rows and number of columns.

1) Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in programmable integrated circuit applications. FIG. 16A2 illustrates the detailed diagram 1600A2 for the implementation of the diagram 1600A1 in programmable integrated circuit embodiments. Each crosspoint is implemented by a transistor coupled between the corresponding inlet link and outlet link, and a programmable cell in programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by transistor C(1,1) coupled between inlet link IL1 and outlet link OL1, and programmable cell P(1,1); crosspoint CP(1,2) is implemented by transistor C(1,2) coupled between inlet link IL1 and outlet link OL2, and programmable cell P(1,2); crosspoint CP(2,1) is implemented by transistor C(2,1) coupled between inlet link IL2 and outlet link OL1, and programmable cell P(2,1); and crosspoint CP(2,2) is implemented by transistor C(2,2) coupled between inlet link IL2 and outlet link OL2, and programmable cell P(2,2).

If the programmable cell is programmed ON, the corresponding transistor couples the corresponding inlet link and outlet link. If the programmable cell is programmed OFF, the corresponding inlet link and outlet link are not connected. For example if the programmable cell P(1,1) is programmed ON, the corresponding transistor C(1,1) couples the corresponding inlet link IL1 and outlet link OL1. If the programmable cell P(1,1) is programmed OFF, the corresponding inlet link IL1 and outlet link OL1 are not connected. In volatile programmable integrated circuit embodiments the programmable cell may be an SRAM (Static Random Address Memory) cell. In non-volatile programmable integrated circuit embodiments the programmable cell may be a Flash memory cell. Also the programmable integrated circuit embodiments may implement field programmable logic arrays (FPGA) devices, or programmable Logic devices (PLD), or Application Specific Integrated Circuits (ASIC) embedded with programmable logic circuits or 3D-FPGAs.

FIG. 16A2 also illustrates a buffer B1 on inlet link IL2. The signals driven along inlet link IL2 are amplified by buffer B1. Buffer B1 can be inverting or non-inverting buffer. Buffers such as B1 are used to amplify the signal in links which are usually long.

In other embodiments all the $d * d$ switches described in the current invention are also implemented using muxes of different sizes controlled by SRAM cells or flash cells etc.

2) One-time Programmable Integrated Circuit Embodiments:

All the embodiments disclosed in the current invention are useful in one-time programmable integrated circuit applications. FIG. 16A3 illustrates the detailed diagram 1600A3 for the implementation of the diagram 1600A1 in one-time programmable integrated circuit embodiments. Each crosspoint is implemented by a via coupled between the corresponding inlet link and outlet link in one-time programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by via V(1,1) coupled between inlet link IL1 and outlet link OL1; crosspoint CP(1,2) is implemented by via V(1,2) coupled between inlet link IL1 and outlet link OL2; crosspoint CP(2,1) is implemented by via V(2,1) coupled between inlet link IL2 and outlet link OL1; and crosspoint CP(2,2) is implemented by via V(2,2) coupled between inlet link IL2 and outlet link OL2.

If the via is programmed ON, the corresponding inlet link and outlet link are permanently connected which is denoted by thick circle at the intersection of inlet link and outlet link. If the via is programmed OFF, the corresponding inlet link and outlet link are not connected which is denoted by the absence of thick circle at the intersection of inlet link and outlet link. For example in the diagram 1600A3 the via V(1,1) is programmed ON, and the corresponding inlet link IL1 and outlet link OL1 are connected as denoted by thick circle at the intersection of inlet link IL1 and outlet link OL1; the via V(2,2) is programmed ON, and the corresponding inlet link IL2 and outlet link OL2 are connected as denoted by thick circle at the intersection of inlet link IL2 and outlet link OL2; the via V(1,2) is programmed OFF, and the corresponding inlet link IL1 and outlet link OL2 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL1 and outlet link OL2; the via V(2,1) is programmed OFF, and the corresponding inlet link IL2 and outlet link OL1 are not connected as denoted by the absence of thick circle at the intersection of inlet link IL2 and outlet link OL1. One-time

programmable integrated circuit embodiments may be anti-fuse based programmable integrated circuit devices or mask programmable structured ASIC devices.

3) Integrated Circuit Placement and Route Embodiments:

All the embodiments disclosed in the current invention are useful in Integrated Circuit Placement and Route applications, for example in ASIC backend Placement and Route tools. FIG. 16A4 illustrates the detailed diagram 1600A4 for the implementation of the diagram 1600A1 in Integrated Circuit Placement and Route embodiments. In an integrated circuit since the connections are known a-priori, the switch and crosspoints are actually virtual. However the concept of virtual switch and virtual crosspoint using the embodiments disclosed in the current invention reduces the number of required wires, wire length needed to connect the inputs and outputs of different netlists and the time required by the tool for placement and route of netlists in the integrated circuit.

Each virtual crosspoint is used to either to hardwire or provide no connectivity between the corresponding inlet link and outlet link. Specifically crosspoint CP(1,1) is implemented by direct connect point DCP(1,1) to hardwire (i.e., to permanently connect) inlet link IL1 and outlet link OL1 which is denoted by the thick circle at the intersection of inlet link IL1 and outlet link OL1; crosspoint CP(2,2) is implemented by direct connect point DCP(2,2) to hardwire inlet link IL2 and outlet link OL2 which is denoted by the thick circle at the intersection of inlet link IL2 and outlet link OL2. The diagram 1600A4 does not show direct connect point DCP(1,2) and direct connect point DCP(1,3) since they are not needed and in the hardware implementation they are eliminated. Alternatively inlet link IL1 needs to be connected to outlet link OL1 and inlet link IL1 does not need to be connected to outlet link OL2. Also inlet link IL2 needs to be connected to outlet link OL2 and inlet link IL2 does not need to be connected to outlet link OL1. Furthermore in the example of the diagram 1600A4, there is no need to drive the signal of inlet link IL1 horizontally beyond outlet link OL1 and hence the inlet link IL1 is not even extended horizontally until the outlet link OL2. Also the absence of direct connect point DCP(2,1) illustrates there is no need to connect inlet link IL2 and outlet link OL1.

In summary in integrated circuit placement and route tools, the concept of virtual switches and virtual cross points is used during the implementation of the placement & routing algorithmically in software, however during the hardware implementation cross points in the cross state are implemented as hardwired connections between the corresponding inlet link and outlet link, and in the bar state are implemented as no connection between inlet link and outlet link.

3) More Application Embodiments:

All the embodiments disclosed in the current invention are also useful in the design of SoC interconnects, Field programmable interconnect chips, parallel computer systems and in time-space-time switches.

Scheduling Method Embodiments the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$:

FIG. 17 shows a high-level flowchart of a scheduling method 1700, in one embodiment executed to setup multicast and unicast connections in the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ disclosed in this invention. According to this embodiment, the set of multicast connections are initialized to the beginning of the set in act 1710. Then the control goes to act 1720. In act 1720, next multicast connection is selected in sequence form the set of multicast connections. Then the control goes to act 1730.

In act 1730 it is checked if this is the next multicast connection in sequence is NULL or i.e. all the multicast connections are scheduled. If act 1730 results "no", that is there are more multicast connections to be scheduled the control goes to act 1740. In act 1740 it is checked if this multicast connection is being scheduled for the first time. Or if it is not scheduled for the first time, it is checked if any one of the links taken by this

multicast connection is oversubscribed by any other multicast connection is checked. If either the multicast connection is being scheduled for the first time or if any one of the links taken by this multicast connection is oversubscribed the control goes to act 1750. Otherwise control goes to act 1720 where the next multicast connection will be selected. So act 1720, act 1730, and act 1740 are executed in a loop.

In act 1750 the multicast connection is not being scheduled for the first time and since at least one of the links taken by this multicast connection is oversubscribed, the complete path taken this multicast connection is cleared or the multicast connection's path is ripped. Then the control goes to act 1760. In act 1760, using the well-known A* search algorithm the least cost path from its source outlet link of the computational block to all the target inlet links of the corresponding computational blocks are found out one after another target inlet links. The cost function used is based on the Manhattan distance between the target inlet link's block and source outlet link's block by taking the delays on each wire is considered in the cost function and also that longest wires are chosen first in the A* search algorithm.

According to the current invention, before scheduling the set of multicast connections in the scheduling method 1700, first a set of static cost tables will be prepared with the least cost paths from each link of the partial multistage network $V_{Comb}(N_1, N_2, d, s)$ to each outgoing hop wire from that partial multistage network as well as to each inlet link of the computational block connected form that partial multistage network. So there will be as many cost tables created equal to the sum of the total number of outgoing hop wires from the partial multistage network and the inlet links of the computational block connected form that partial multistage network. Each cost table will also have as many entries as there are internal links of that partial multistage network. And the value at each entry of these cost tables is equal to the total delay from the corresponding internal link to the corresponding outgoing hop wire or to the inlet link of the computational block.

In act 1760, according to the current invention, for the look-ahead cost computation during the A* search algorithm both the cost from the static cost tables from the current internal link in the current partial multistage network and the cost value

computed based on the Manhattan distance between the target inlet link's block and the current link's corresponding block by taking the delays on each wire into consideration are added. Also the least of the cost values from all the cost tables corresponding to the current link and all the outgoing wires in the right direction of the target block, is selected before it is added to the Manhattan distance based cost. Finally in act 1760, the multicast connection is scheduled as for the A* search algorithm. Then the control goes to act 1770.

In act 1770, the demand cost and history cost of each link used by the current multicast connection are updated. And the control goes to act 1720. Thus act 1720, act 1730, act 1740, act 1750, act 1760, and act 1770 are executed in a loop to schedule the multicast connections by going through the list of all multicast connections which will be one pass or iteration.

In act 1730 results "yes", i.e. all the required multicast connections in the list are scheduled in this pass or iteration, then the control goes to act 1780. In act 1780, the total number of links in the complete multistage network that are taken by more than one multicast connection are counted, hereinafter "OSN" or "Over Subscription nodes". Then the control goes to act 1790. In act 1790 it will be checked and if OSN is not equal to zero then the act 1790 results in "no" and the control goes to act 1710 to start the next iteration or pass to schedule all the required multicast connections in the list of all multicast connections. Thus act 1710, act 1720, act 1730, act 1740, act 1750, act 1760, act 1770, act 1780, and act 1790 are executed in a loop to implement different passes or iterations of scheduling the set of all multicast connections. If the act 1790 results in "yes", that means no link in the complete multistage network is taken by more than one multicast connection and hence the scheduling is successfully completed.

Each multicast connection of the type described above in reference to method 1700 of FIG. 17 can be unicast connection, a multicast connection or a broadcast connection, depending on the example.

Inter-block and Intra-block Scheduling Method Embodiments the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$:

FIG. 18 shows a high-level flowchart of a scheduling method 1800, in one embodiment executed to setup multicast connections in the multi-stage hierarchical network $V_{Comb}(N_1, N_2, d, s)$ disclosed in this invention in two steps (one for each act 1810 and act 1820 as shown in FIG. 18) namely: 1) scheduling the set of multicast connections outside the blocks of 2D-grid of blocks with each block corresponding to a partial multi-stage network, or in between the blocks of the complete multi-stage network, or alternatively on the external wires of the complete multi-stage network hereinafter "inter-block scheduling". Inter-block scheduling is implemented in act 1810 so that there are no OSN nodes. During inter-block scheduling the partial multi-stage hierarchical network corresponding to each block is considered as a single stage network or alternatively each internal wire of the partial multi-stage hierarchical network is directly connected to each outgoing wire or external wire of the partial multi-stage hierarchical network, and 2) scheduling the set of multicast connections inside the blocks of 2D-grid of blocks with each block corresponding to a partial multi-stage network or alternatively on the internal wires of the complete multi-stage network hereinafter "intra-block scheduling". The act 1820 implements intra-block scheduling for each block so that there are no OSN nodes.

The act 1810 may be implemented by the scheduling method 1700 of FIG. 17. Similarly in act 1820 for each block of the multi-stage hierarchical network, the inter-block scheduling may be implemented by the scheduling method 1700 of FIG. 17.

In accordance with the current invention, the scheduling method 1700 of FIG. 17 and the scheduling method 1800 of FIG. 18 are applicable to either partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100A of FIG. 1A, or partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100B of FIG. 1B, or partial multi-stage hierarchical network $V_{D-Comb}(N_1, N_2, d, s)$ 100C of FIG. 1C, corresponding to a block of 2D-grid of blocks 800 of FIG. 8, using any one of the embodiments of 200A-200F of FIGs. 2A-2F, 900A-900E of FIGs. 9A-9E, 1000A-1000F of FIGs. 10A-10F, 1100A-1100C of FIGs. 11A-11C to implement a stage of a ring of the multi-stage hierarchical

network, either by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks described in diagram 700A of FIG. 7A may be any one of the embodiments of either the diagrams 300A of FIG. 3A, 300B of FIG. 3B, 300C of FIG. 3C, 300D of FIG. 3D, 300E of FIG. 3E, 500A of FIG. 5A, 1200 of FIG. 12, 1300 of FIG. 13, 1400 of FIG. 14, and 1500 of FIG. 15 or by using the hop wire connections or multi-drop hop wire connections between two arbitrary stages in two different rings of the same block or two different rings of different blocks may be any one of the embodiments of either the diagrams 400A of FIG. 4A, 400B of FIG. 4B, 600A of FIG. 6A, or 600B of FIG. 6B is very efficient in the reduction of the die size, power consumption, and highly optimized for lower wire/path delay for higher performance for practical routing applications to particularly to set up broadcast, unicast and multicast connections.

Numerous modifications and adaptations of the embodiments, implementations, and examples described herein will be apparent to the skilled artisan in view of the disclosure.

CLAIMS

What is claimed is:

1. A programmable integrated circuit comprising a plurality of programmable logic blocks and a network,

each programmable logic block of said plurality of programmable logic blocks comprising a plurality of inlet links and a plurality of outlet links; and

said network comprising a plurality of partial multi-stage networks wherein each programmable logic block of said plurality of programmable logic blocks is coupled with at least one of said plurality of partial multi-stage networks; and

said plurality of programmable logic blocks coupled with said plurality of partial multi-stage networks arranged in a two-dimensional grid of a plurality of rows and a plurality of columns; and

each partial multi-stage network of said plurality of partial multi-stage networks further comprising one or more slices, each slice of said one or more slices further comprising one or more rings, each ring of said one or more rings further comprising y stages, where $y \geq 1$; and

each stage of said y stages comprising at least one switch of size $d_i \times d_0$, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of said at least one switch of size $d_i \times d_0$ having d_i incoming links and d_0 outgoing links; and each switch of said at least one switch of size $d_i \times d_0$ further comprising a plurality of multiplexers of size $d \geq 2$ with each multiplexer of said plurality of multiplexers comprising d inputs and one output; and

said at least one switch of size $d_i \times d_0$ comprises either only a forward switch, or only a backward switch, or both a forward switch and a backward switch, or a forward switch, a

backward switch and U-turn switch, or a forward switch, a backward switch and a U-turn switch without 180 degree turn paths or a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch or a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180 degree turn paths, or an integrated switch of a forward switch, a backward switch and U-turn switch, or an integrated switch of a forward switch, a backward switch and a U-turn switch without 180 degree turn paths or an integrated switch of a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch or an integrated switch of a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180 degree turn paths; and

said d_i incoming links and said d_0 outgoing links comprises a plurality of internal connections and a plurality of hop wires; and said plurality of hop wires further comprising a plurality of internal hop wires or a plurality of external hop wires; and

each inlet link of said plurality of inlet links is connected to the output of one of said plurality of multiplexers of one switch of said at least one switch of size $d_i \times d_0$ of one stage of said y stages of one partial multi-stage network of said plurality of partial multi-stage networks, and each outlet link of said plurality of outlet links is connected to one of the inputs of one or more of said plurality of multiplexers of one or more said switches of said at least one switch of size $d_i \times d_0$ of one or more said stages of said y stages of one or more said plurality of partial multi-stage networks; and

a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of inlet links as a second programmable logic block of said plurality of programmable logic blocks and a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of outlet links as a second programmable logic block of said plurality of programmable logic blocks; a first partial multi-stage network of said plurality of partial multi-stage networks comprising the same or different number of said one or more slices as a second partial multi-stage network of said plurality of partial multi-stage networks; a first slice of said one or more slices comprising the same

or different number of said one or more rings as a second slice of said one or more slices; a first ring of said one or more rings comprising the same or different number of said y stages as a second ring of said one or more rings; and a first stage of said y stages comprising the same or different number of said at least one switch of size $d_i \times d_0$ as a second stage of said y stages; a first switch of said at least one switch of size $d_i \times d_0$ is the same or different size as a second switch of said at least one switch of size $d_i \times d_0$; a first multiplexer in said plurality of multiplexers of size $d \geq 2$ is the same or different size as a second multiplexer in said plurality of multiplexers of size $d \geq 2$; and

each internal connection of said plurality of internal connections connected from the output of a first multiplexer of said plurality of multiplexers of a first switch of said at least one switch of size $d_i \times d_0$ of a first stage of said y stages of a first ring of said one or more rings to a first input of said d inputs of a second multiplexer of said plurality of multiplexers of a second switch of said at least one switch of size $d_i \times d_0$ of a second stage of said y stages of the first ring of said one or more rings; and

each internal hop wire of said plurality of internal hop wires is connected from the output of a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a first ring of said one or more rings of a slice of said one or more slices to a first input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_0$ of one or more stages of said y stages of one or more rings different from the first ring of said one or more rings of the same slice of said one or more slices; and

each external hop wire of said plurality of external hop wires is connected from the output a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a ring of said one or more rings of a slice of said one or more slices of a first partial multi-stage network of said plurality of partial multi-stage networks to an input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size

$d_i \times d_0$ of one or more stages of said y stages of said one or more rings of a slice of said one or more slices of one or more partial multi-stage networks different from the first partial multi-stage network of said plurality of partial multi-stage networks; and

one or more external hop wires of said plurality of external hop wires are either connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size $d_i \times d_0$ in same numbered stages of said y stages in two or more partial multi-stage networks of said plurality of partial multi-stage networks or connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size $d_i \times d_0$ in different numbered stages of said y stages, when $y \geq 2$, in two or more partial multi-stage networks of said plurality of partial multi-stage networks.

2. The programmable integrated circuit of claim 1, wherein said plurality of external hop wires are connected vertically (hereinafter "vertical links"), or horizontally (hereinafter "horizontal links"), or by both vertical links and horizontal links; and

each partial multi-stage network of said plurality of partial multi-stage networkscomprising said one or more slices is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or

each partial multi-stage network of said plurality of partial multi-stage networks comprising said horizontal links and said vertical links is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or

each partial multi-stage network of said plurality of partial multi-stage networks comprising both said one or more slices, and said horizontal links and said vertical links is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid.

3. The programmable integrated circuit of claim 1, wherein said plurality of external hop wires are cascaded through only one multiplexer of said plurality of multiplexers at each switch of said at least one switch of size $d_i \times d_0$.

4. The programmable integrated circuit of claim 1, wherein said one or more external hop wires of said plurality of external hop wires are connected between at least one same numbered stage in all said plurality of partial multi-stage networks, or one or more external hop wires of said plurality of external hop wires are connected between at least two not same numbered stages of said y stages in all said plurality of partial multi-stage networks; or

said plurality of external hop wires are all connected between same numbered stages of said y stages in all stages of said y stages of all said plurality of partial multi-stage networks.

5. The programmable integrated circuit of claim 1, wherein one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks are not connected to any other stages of said y stages in another partial multi-stage network of said plurality of partial multi-stage networks, or,

one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks are connected to stages of said y stages in another partial multi-stage network of said plurality of partial multi-stage networks by one or more external hop wires of said plurality of external hop wires, only when said two-dimensional grid is replicated by increasing said plurality of rows or said plurality of columns.

6. The programmable integrated circuit of claim 1, wherein one or more of external hop wires of said plurality of external hop wires are implemented in two or more metal layers, or

each multiplexer of said plurality of multiplexers of size $d \geq 2$ is configurable by SRAM cells or Flash Cells, or

said plurality of external hop wires use a plurality of buffers to amplify signals driven through them; and said plurality of buffers are either inverting or non-inverting buffers, or

one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks comprising a switch of size $(d_i + m) \times (d_o + n)$, where $d_i \geq 2$, $d_o \geq 2$, $m \geq 0$, $n \geq 0$ or

one or more of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks comprising six 2:1 multiplexers, or eight 2:1 multiplexers, or four 3:1 multiplexers, or four 4:1 multiplexers.

7. The programmable integrated circuit of claim 1, wherein said at least one switch of size $d_i \times d_0$ of said y stages are either fully populated or partially populated, or

said plurality of partial multi-stage networks are implemented in a 3D integrated circuit device.

8. A programmable integrated circuit comprising a plurality of programmable logic blocks and a network,

each programmable logic block of said plurality of programmable logic blocks comprising a plurality of inlet links and a plurality of outlet links; and

said network comprising a plurality of partial multi-stage networks wherein each programmable logic block of said plurality of programmable logic blocks is coupled with at least one of said plurality of partial multi-stage networks; and

said plurality of programmable logic blocks coupled with said plurality of partial multi-stage networks arranged in a two-dimensional grid of a plurality of rows and a plurality of columns; and

each partial multi-stage network of said plurality of partial multi-stage networks further comprising one or more slices, each slice of said one or more slices further comprising one or more rings, each ring of said one or more rings further comprising y stages, where $y \geq 1$; and

each stage of said y stages comprising at least one switch of size $d_i \times d_0$, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of said at least one switch of size $d_i \times d_0$ having d_i incoming links and d_0 outgoing links; and each switch of said at least one switch of size $d_i \times d_0$ further comprising a plurality of multiplexers of size $d \geq 2$ with each multiplexer of said plurality of multiplexers comprising d inputs and one output; and

said at least one switch of size $d_i \times d_0$ comprises either only a forward switch, or only a backward switch, or both a forward switch and a backward switch, or a forward switch, a backward switch and U-turn switch, or a forward switch, a backward switch and a U-turn switch without 180 degree turn paths, or an integrated switch of a forward switch, a backward switch and U-turn switch, or an integrated switch of a forward switch, a backward switch and a U-turn switch without 180 degree turn paths; and

said d_i incoming links and said d_0 outgoing links comprises a plurality of internal connections and a plurality of hop wires; and said plurality of hop wires further comprising a plurality of internal hop wires or a plurality of external hop wires; and

each inlet link of said plurality of inlet links is connected to the output of one of said plurality of multiplexers of one switch of said at least one switch of size $d_i \times d_0$ of one stage of said y stages of one partial multi-stage network of said plurality of partial multi-stage networks, and each outlet link of said plurality of outlet links is connected to one of the inputs of one or more of said plurality of multiplexers of one or more said switches of said at least one switch of size $d_i \times d_0$ of one or more said stages of said y stages of one or more said plurality of partial multi-stage networks; and

a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of inlet links as a second programmable logic block of said plurality of programmable logic blocks and a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of outlet links as a second programmable logic block of said plurality of programmable logic blocks; a first partial multi-stage network of said plurality of partial multi-stage networks comprising the same or different number of said one or more slices as a second partial multi-stage network of said plurality of partial multi-stage networks; a first slice of said one or more slices comprising the same or different number of said one or more rings as a second slice of said one or more slices; a first ring of said one or more rings comprising the same or different number of said y stages as a second ring of said one or more rings; and a first stage of said y stages comprising the same or different number of said at least one switch of size $d_i \times d_0$ as a second stage of said y stages; a first switch of said at least one switch of size $d_i \times d_0$ is the same or different size as a second switch of said at least one switch of size $d_i \times d_0$; a first multiplexer in said plurality of multiplexers of size $d \geq 2$ is the same or different size as a second multiplexer in said plurality of multiplexers of size $d \geq 2$; and

each internal connection of said plurality of internal connections connected from the output of a first multiplexer of said plurality of multiplexers of a first switch of said at least one switch of size $d_i \times d_0$ of a first stage of said y stages of a first ring of said one or more rings to a first input of said d inputs of a second multiplexer of said plurality of multiplexers of a second switch of said at least one switch of size $d_i \times d_0$ of a second stage of said y stages of the first ring of said one or more rings; and

each internal hop wire of said plurality of internal hop wires is connected from the output of a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a first ring of said one or more rings of a slice of said one or more slices to a first input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size

$d_i \times d_0$ of one or more stages of said y stages of one or more rings different from the first ring of said one or more rings of the same slice of said one or more slices; and

each external hop wire of said plurality of external hop wires is connected from the output a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a ring of said one or more rings of a slice of said one or more slices of a first partial multi-stage network of said plurality of partial multi-stage networks to an input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_0$ of one or more stages of said y stages of said one or more rings of a slice of said one or more slices of one or more partial multi-stage networks different from the first partial multi-stage network of said plurality of partial multi-stage networks; and

one or more external hop wires of said plurality of external hop wires are either connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size $d_i \times d_0$ in same numbered stages of said y stages in two or more partial multi-stage networks of said plurality of partial multi-stage networks or connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size $d_i \times d_0$ in different numbered stages of said y stages, when $y \geq 2$, in two or more partial multi-stage networks of said plurality of partial multi-stage networks.

9. The programmable integrated circuit of claim 8, wherein said plurality of external hop wires are connected vertically (hereinafter "vertical links"), or horizontally (hereinafter "horizontal links"), or by both vertical links and horizontal links; and

each partial multi-stage network of said plurality of partial multi-stage networkscomprising said one or more slices is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or

each partial multi-stage network of said plurality of partial multi-stage networks comprising said horizontal links and said vertical links is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or

each partial multi-stage network of said plurality of partial multi-stage networks comprising both said one or more slices, and said horizontal links and said vertical links is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid.

10. The programmable integrated circuit of claim 8, wherein said plurality of external hop wires are cascaded through only one multiplexer of said plurality of multiplexers at each switch of said at least one switch of size $d_i \times d_0$.

11. The programmable integrated circuit of claim 8, wherein said one or more external hop wires of said plurality of external hop wires are connected between at least one same numbered stage in all said plurality of partial multi-stage networks, or

one or more external hop wires of said plurality of external hop wires are connected between at least two not same numbered stages of said y stages in all said plurality of partial multi-stage networks; or

said plurality of external hop wires are all connected between same numbered stages of said y stages in all stages of said y stages of all said plurality of partial multi-stage networks.

12. The programmable integrated circuit of claim 8, wherein one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks are not connected to any other stages of said y stages in another partial multi-stage network of said plurality of partial multi-stage networks, or,

one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks are connected to stages of said y stages in

another partial multi-stage network of said plurality of partial multi-stage networks by one or more external hop wires of said plurality of external hop wires, only when said two-dimensional grid is replicated by increasing said plurality of rows or said plurality of columns.

13. The programmable integrated circuit of claim 8, wherein one or more of external hop wires of said plurality of external hop wires are implemented in two or more metal layers, or

each multiplexer of said plurality of multiplexers of size $d \geq 2$ is configurable by SRAM cells or Flash Cells, or

said plurality of external hop wires use a plurality of buffers to amplify signals driven through them; and said plurality of buffers are either inverting or non-inverting buffers, or

one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks comprising a switch of size $(d_i + m) \times (d_o + n)$, where $d_i \geq 2$, $d_o \geq 2$, $m \geq 0$, $n \geq 0$ or

one or more of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks comprising six 2:1 multiplexers, or eight 2:1 multiplexers, or four 3:1 multiplexers, or four 4:1 multiplexers.

14. The programmable integrated circuit of claim 8, wherein said at least one switch of size $d_i \times d_0$ of said y stages are either fully populated or partially populated, or

said plurality of partial multi-stage networks are implemented in a 3D integrated circuit device.

15. A programmable integrated circuit comprising a plurality of programmable logic blocks and a network,

each programmable logic block of said plurality of programmable logic blocks comprising a plurality of inlet links and a plurality of outlet links; and

said network comprising a plurality of partial multi-stage networks wherein each programmable logic block of said plurality of programmable logic blocks is coupled with at least one of said plurality of partial multi-stage networks; and

said plurality of programmable logic blocks coupled with said plurality of partial multi-stage networks arranged in a two-dimensional grid of a plurality of rows and a plurality of columns; and

each partial multi-stage network of said plurality of partial multi-stage networks further comprising one or more slices, each slice of said one or more slices further comprising one or more rings, each ring of said one or more rings further comprising y stages, where $y \geq 1$; and

each stage of said y stages comprising at least one switch of size $d_i \times d_0$, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of said at least one switch of size $d_i \times d_0$ having d_i incoming links and d_0 outgoing links; and each switch of said at least one switch of size $d_i \times d_0$ further comprising a plurality of multiplexers of size $d \geq 2$ with each multiplexer of said plurality of multiplexers comprising d inputs and one output; and

said at least one switch of size $d_i \times d_0$ comprises either only a forward switch, or only a backward switch, or both a forward switch and a backward switch, or a forward switch, a backward switch and U-turn switch, or a forward switch, a backward switch and a U-turn switch without 180 degree turn paths, or an integrated switch of a forward switch, a backward switch and U-turn switch, or an integrated switch of a forward switch, a backward switch and a U-turn switch without 180 degree turn paths; and

said d_i incoming links and said d_0 outgoing links comprises a plurality of internal connections and a plurality of hop wires; and said plurality of hop wires further comprising a plurality of internal hop wires or a plurality of external hop wires; and

each inlet link of Said plurality of inlet links is connected to the output of one of said plurality of multiplexers of one switch of said at least one switch of size $d_i \times d_0$ of one stage of said y stages of one partial multi-stage network of said plurality of partial multi-stage networks, and each outlet link of said plurality of outlet links is connected to one of the inputs of one or more of said plurality of multiplexers of one or more said switches of said at least one switch of size $d_i \times d_0$ of one or more said stages of said y stages of one or more said plurality of partial multi-stage networks; and

a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of inlet links as a second programmable logic block of said plurality of programmable logic blocks and a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of outlet links as a second programmable logic block of said plurality of programmable logic blocks; a first partial multi-stage network of said plurality of partial multi-stage networks comprising the same or different number of said one or more slices as a second partial multi-stage network of said plurality of partial multi-stage networks; a first slice of said one or more slices comprising the same or different number of said one or more rings as a second slice of said one or more slices; a first ring of said one or more rings comprising the same or different number of said y stages as a second ring of said one or more rings; and a first stage of said y stages comprising the same or different number of said at least one switch of size $d_i \times d_0$ as a second stage of said y stages; a first switch of said at least one switch of size $d_i \times d_0$ is the same or different size as a second switch of said at least one switch of size $d_i \times d_0$; a first multiplexer in said plurality of multiplexers of size $d \geq 2$ is the same or different size as a second multiplexer in said plurality of multiplexers of size $d \geq 2$; and

each internal connection of said plurality of internal connections connected from the output of a first multiplexer of said plurality of multiplexers of a first switch of said at least one switch of size $d_i \times d_0$ of a first stage of said y stages of a first ring of said one or more rings to a first input of said d inputs of a second multiplexer of said plurality of multiplexers of a second switch of said at least one switch of size $d_i \times d_0$ of a second stage of said y stages of the first ring of said one or more rings ; and

each internal hop wire of said plurality of internal hop wires is connected from the output of a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a first ring of said one or more rings of a slice of said one or more slices to a first input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_0$ of one or more stages of said y stages of one or more rings different from the first ring of said one or more rings of the same slice of said one or more slices ; and

each external hop wire of said plurality of external hop wires is connected from the output a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a ring of said one or more rings of a slice of said one or more slices of a first partial multi-stage network of said plurality of partial multi-stage networks to an input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_0$ of one or more stages of said y stages of said one or more rings of a slice of said one or more slices of one or more partial multi-stage networks different from the first partial multi-stage network of said plurality of partial multi-stage networks; and

one or more external hop wires of said plurality of external hop wires are either connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size $d_i \times d_0$ in same numbered stages of said y stages in three or more partial multi-stage networks of said plurality of partial multi-stage networks or connected between multiplexers of said plurality of multiplexers of switches of said at

least one switch of size $d_i \times d_0$ in different numbered stages of said y stages, when $y \geq 2$, in three or more partial multi-stage networks of said plurality of partial multi-stage networks.

16. The programmable integrated circuit of claim 15, wherein said plurality of external hop wires are connected vertically (hereinafter "vertical links"), or horizontally (hereinafter "horizontal links"), or by both vertical links and horizontal links; and

each partial multi-stage network of said plurality of partial multi-stage networks comprising said one or more slices is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or

each partial multi-stage network of said plurality of partial multi-stage networks comprising said horizontal links and said vertical links is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid, or

each partial multi-stage network of said plurality of partial multi-stage networks comprising both said one or more slices, and said horizontal links and said vertical links is replicated in either said plurality of rows or said plurality of columns of the two-dimensional grid.

17. The programmable integrated circuit of claim 15, wherein said plurality of external hop wires are cascaded through only one multiplexer of said plurality of multiplexers at each switch of said at least one switch of size $d_i \times d_0$.

18. The programmable integrated circuit of claim 15, wherein said one or more external hop wires of said plurality of external hop wires are connected between at least one same numbered stage in all said plurality of partial multi-stage networks, or

one or more external hop wires of said plurality of external hop wires are connected between at least two not same numbered stages of said y stages in all said plurality of partial multi-stage networks; or

said plurality of external hop wires are all connected between same numbered stages of said y stages in all stages of said y stages of all said plurality of partial multi-stage networks.

19. The programmable integrated circuit of claim 15, wherein one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks are not connected to any other stages of said y stages in another partial multi-stage network of said plurality of partial multi-stage networks, or,

one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks are connected to stages of said y stages in another partial multi-stage network of said plurality of partial multi-stage networks by one or more external hop wires of said plurality of external hop wires, only when said two-dimensional grid is replicated by increasing said plurality of rows or said plurality of columns.

20. The programmable integrated circuit of claim 15, wherein one or more of external hop wires of said plurality of external hop wires are implemented in two or more metal layers, or

each multiplexer of said plurality of multiplexers of size $d \geq 2$ is configurable by SRAM cells or Flash Cells, or

said plurality of external hop wires use a plurality of buffers to amplify signals driven through them; and said plurality of buffers are either inverting or non-inverting buffers, or

one or more stages of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks comprising a switch of size $(d_i + m) \times (d_o + n)$, where $d_i \geq 2$, $d_o \geq 2$, $m \geq 0$, $n \geq 0$ or

one or more of said y stages in one partial multi-stage network of said plurality of partial multi-stage networks comprising six 2:1 multiplexers, or eight 2:1 multiplexers, or four 3:1 multiplexers, or four 4:1 multiplexers, or

said at least one switch of size $d_i \times d_0$ of said y stages are either fully populated or partially populated, or

said plurality of partial multi-stage networks are implemented in a 3D integrated circuit device.

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FAST SCHEDULING AND OPTMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS

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ABSTRACT OF DISCLOSURE

Significantly optimized multi-stage networks with scheduling methods for faster scheduling of connections, useful in wide target applications, with VLSI layouts using only horizontal and vertical links to route large scale sub-integrated circuit blocks having inlet and outlet links, and laid out in an integrated circuit device in a two-dimensional grid arrangement of blocks are presented. The optimized multi-stage networks in each block employ several slices of rings of stages of switches with inlet and outlet links of sub-integrated circuit blocks connecting to rings from either left-hand side only, or from right-hand side only, or from both left-hand side and right-hand side; and employ multi-drop links where outlet links of cross links from switches in a stage of a ring in one sub-integrated circuit block are connected to either inlet links of switches in the another stage of a ring in the same or another sub-integrated circuit block.