United States Patent [19]

Fenwick et al.

[11] **4,001,692**

[45] **Jan. 4, 1977**

[54] **TIME DIVERSITY DATA TRANSMISSION APPARATUS**

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[73] Assignee: **Barry Research Corporation,** Sunnyvale, Calif.

[22] Filed: **July 7, 1975**

[21] Appl. No.: **593,690**

[52] **U.S. Cl.** .... **325/38 R;** 325/39; 325/40; 325/42; 325/56; 325/60; 343/204

[51] **Int. Cl.²** **H04B 7/06**

[58] **Field of Search** .... 325/56, 59, 60, 154, 325/40, 38 R, 39, 473–476, 65, 42; 343/176, 178, 200, 204; 179/15 R, 15 FD, 15 BA; 340/172.5

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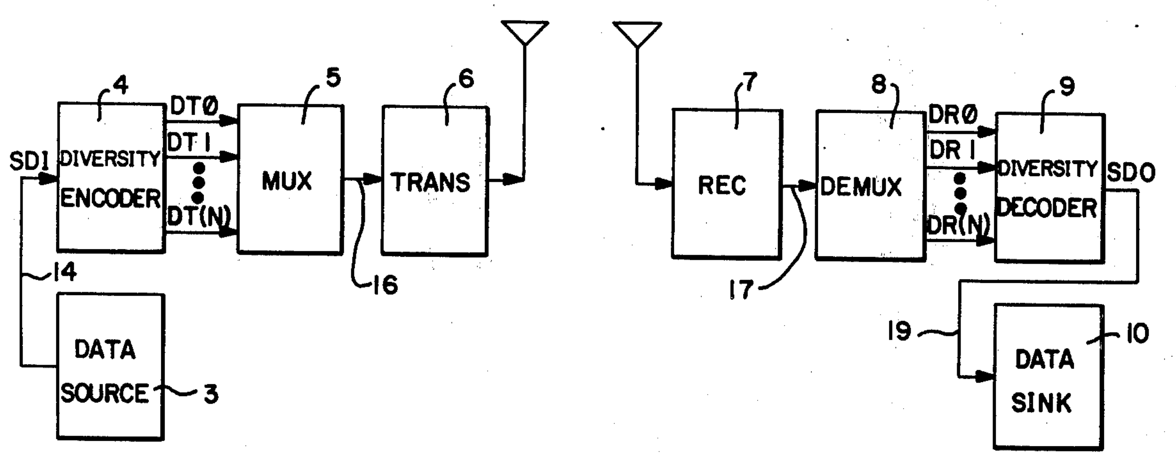
Primary Examiner—Robert L. Richardson
Assistant Examiner—Michael A. Masinick
Attorney, Agent, or Firm—Flehr, Hohbach, Test, Albritton & Herbert

[57] **ABSTRACT**

An asynchronous, time diversity transmission apparatus including a data encoder at a transmitting location and an error-correcting data decoder at a receiving location for overcoming the effects of signal fading, impulsive noise and interference. The asynchronous data encoder encodes a single input data stream into three or more redundant, parallel data outputs having time diversity introduced by successive delays. The data outputs are frequency multiplexed and propagated over a transmission circuit. Received data is demultiplexed and input to the data decoder where it is processed to remove the time diversity. Three or more outputs from the decoder are combined to form a single, error-corrected data output.

25 Claims, 5 Drawing Figures



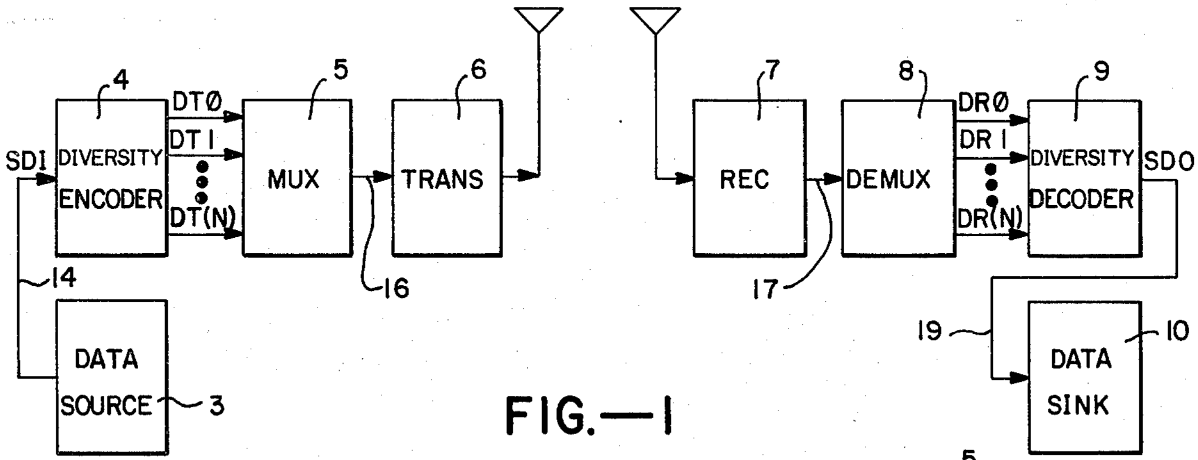


FIG.—1

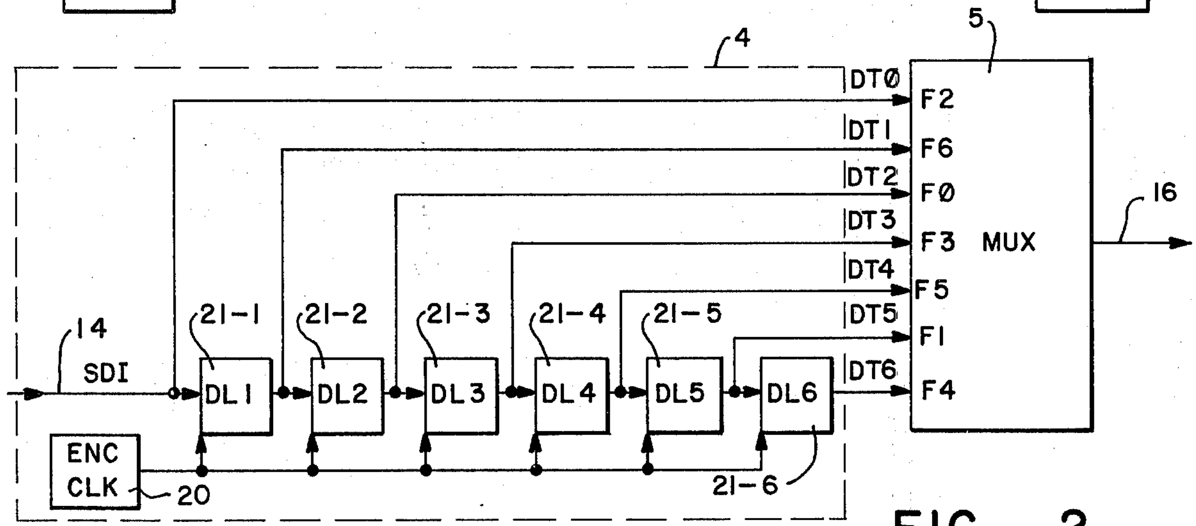


FIG.—2

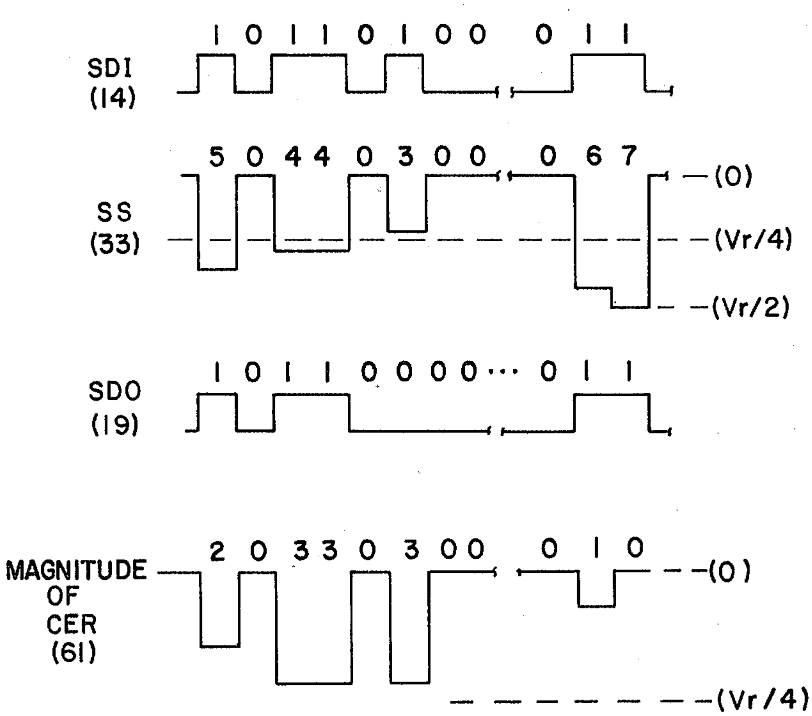
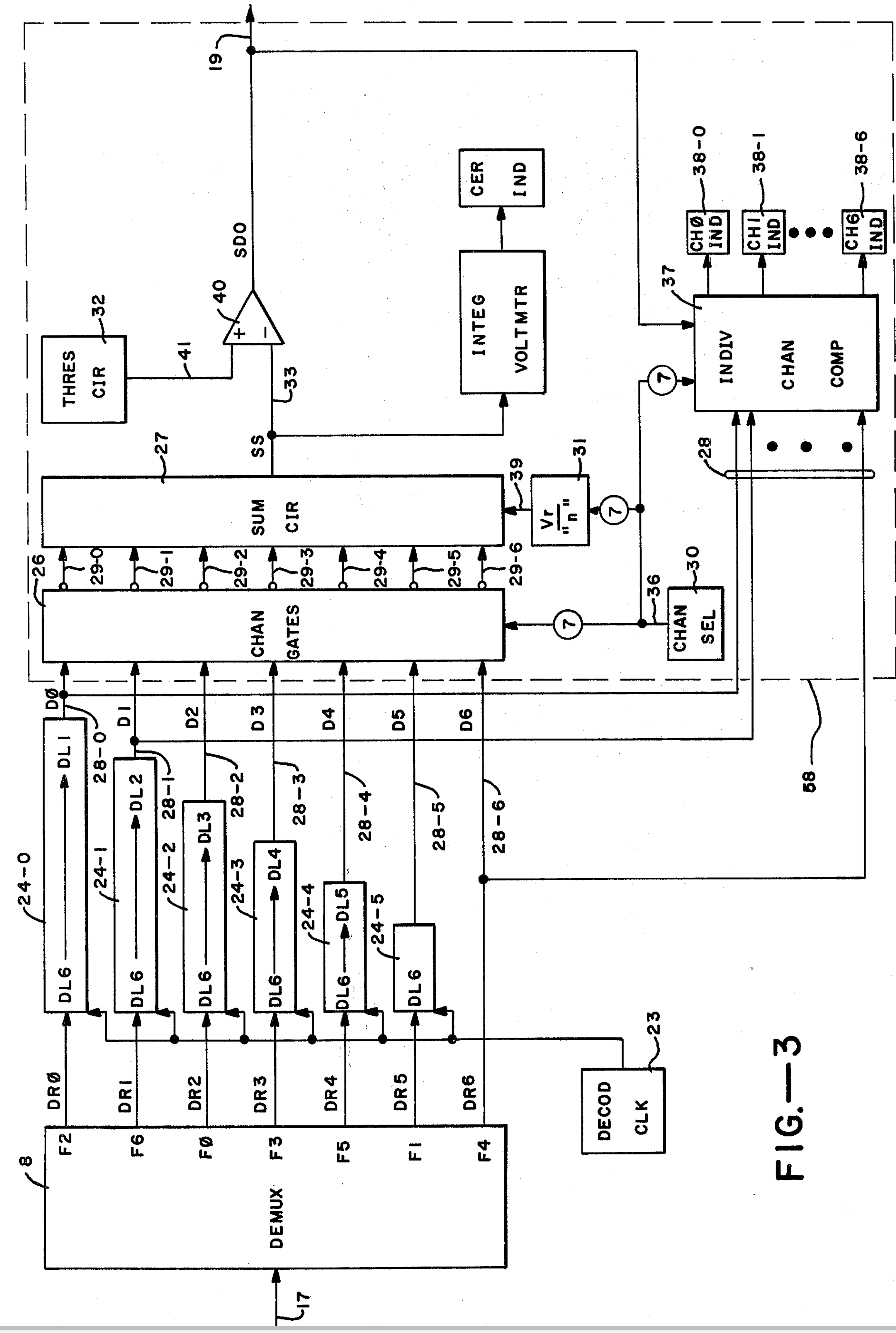


FIG.—5


DEMUX
F2
F6
FØ
F3
F5
F1
F4
DRØ
DR1
DR2
DR3
DR4
DR5
DR6
DL6
DL1
DL2
DL3
DL4
DL5
DECOD CLK
DØ
D1
D2
D3
D4
D5
D6
CHAN GATES
SUM CIR
THRES CIR
SDO
SS
INTEG VOLTMTR
CER IND
Vr "n"
CHAN SEL
INDIV CHAN COMP
CHØ IND
CH1 IND
CH6 IND
7
8
17
19
23
24-0
24-1
24-2
24-3
24-4
24-5
26
27
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28-0
28-1
28-2
28-3
28-4
28-5
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29-3
29-4
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37
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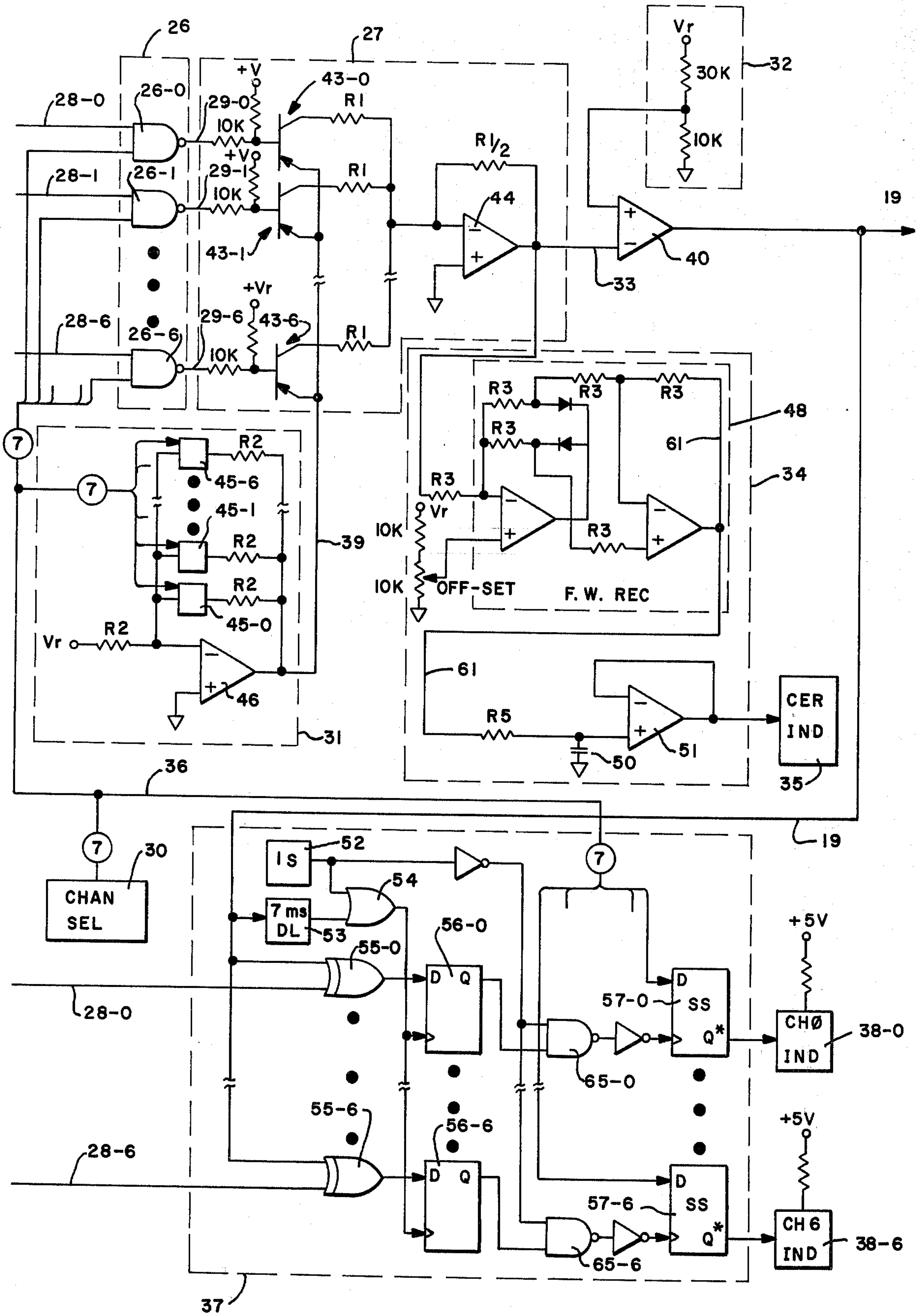
38-1
38-6
39
40
41
58

FIG.—3


26
27
Vr
30K
32
10K
28-0
26-0
29-0
+V
43-0
R1
10K
+V
R1/2
28-1
26-1
29-1
R1
10K
44
19
43-1
40
33
+Vr
28-6
29-6
43-6
R1
26-6
10K
R3
R3
R3
48
R3
7
R2
61
45-6
7
34
R3
45-1
Vr
R2
39
10K
R2
10K
OFF-SET
F. W. REC
45-0
R2
Vr
61
46
R5
CER
IND
51
31
50
36
35
19
7
52
IS
30
7
54
CHAN
SEL
7 ms
DL
53
56-0
+5V
55-0
D
Q
D
SS
57-0
Q*
CHØ
IND
38-0
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65-0
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+5V
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28-6
D
Q
D
57-6
SS
CH6
Q*
IND
38-6
65-6
37

FIG.—4

TIME DIVERSITY DATA TRANSMISSION APPARATUS

BACKGROUND OF THE INVENTION

The present invention relates to transmission apparatus including encoders and decoders useful for forward error correction and more specifically to transmission circuits in which the effects of signal loss, noise, and interference, or any of them, are time variable. The present invention is particularly useful in high frequency and troposcatter radio circuits.

Signal fading, impulsive noise and interference are deleterious effects frequently encountered in many transmission circuits. Where these effects are present, the quality of transmission is deteriorated and an increase in the transmission error-rate occurs. Radio circuits employed to transmit teleprinter information are particularly susceptible to these deliterious effects. Radio teleprinter information is typically transmitted at a rate of up to 75 bits per second (baud).

The quality of a transmission circuit is frequently measured in terms of its character error rate (CER). The character error rate is defined as the percentage of erroneous characters received relative to the total number of characters transmitted in a given time period.

Prior art techniques for improving the performance of data transmission circuits have utilized many different forms of redundancy in connection with forward error correction. Diversity systems employing space diversity, polarization diversity, frequency diversity or time diversity have all been known in one form or another.

The term "time diversity" has usually been interpreted to mean synchronous transmission of data two or more times with a time delay between each transmission. Each received data bit is compared with a corresponding delayed data bit. In such systems, synchronous operation is required in order to identify each bit. Synchronous operation has the undersireable requirement of being dependent upon the transmission data rate. A change in data rate requires a corresponding change in synchronous clocking in the transmitter and receiver apparatus. If a difference is observed between bits as a result of a comparison of bits, an error is identified. When an error is identified, one of the data bits, for example the earlier transmitted data bit, is the one selected for actual use. A time diversity system of this type has been described by L. E. Zegers in an article entitled "Error Control in Telephone Channels By Means of Time Diversity" appearing in the *Philips Research Report*, volumn 22, June, 1967.

The term "time diversity" has also been applied to systems in which data bits are divided in time, with one half of each bit being transmitted on one frequency and the other one half of each bit being transmitted on another frequency.

The performance quality of known diversity systems is not entirely satisfactory particularly when the effects of signal loss, noise or interference have a duration of up to several seconds. There is a need, therefore, for improved and economical apparatus useful in improving transmission and reducing character error rates in transmission circuits.

SUMMARY OF THE INVENTION

The present invention is an asynchronous time diversity method and apparatus which provides forward error correction in the transmission of data. The asynchronous capability of the invention permits many different transmission data rates to be utilized without requiring changes in operating frequency.

In transmitter circuitry, a serial input data stream is converted to three or more transmitter data streams. The transmitter data streams are each substantially identical to the input data stream except that in order to obtain time diversity, the transmitter data streams are successively delayed, in an encoder, relative to the input data stream. The transmitter data streams are multiplexed and transmitted to a receiver.

In receiver circuitry, a received signal is demultiplexed asynchronously to form three or more receiver data streams, one for each of the transmitter data streams. The receiver data streams are successively delayed, in a decoder, to remove the time diversity. The relative delays removed from the receiver data streams by the receiver decoder correspond to the relative delays introduced into the transmitter data streams by the transmitter encoder. The receiver data streams, after removal of time diversity, are algebraically added to form a sum data stream. The sum data stream is compared with a threshold to form an error-corrected output data stream.

In one preferred embodiment of the invention, the transmitter encoder includes two or more delay circuits for delaying the input data stream. The delay circuits are, for example, shift register stages which step the input data stream under control of an encoder clock. The input data stream is utilized as a first transmitter data stream. The output from the first shift register stage provides a delayed second transmitter data stream. The second transmitter data stream in turn is input to a second shift register stage and is delayed to provide a third transmitter data stream. Up to N transmitter data streams with successive delays are obtained with N shift register stages.

The frequency of the encoder clock is selected to be twenty or more times the data rate (baud rate) of the input data stream. Lower encoder clock frequencies tend to introduce increasing numbers of errors. While an asynchronous encoder clock appears more desireable in order to allow operation without change for many different data rates, bit synchronous encoder clocks can also be employed.

In one embodiment, each of the transmitter data streams is frequency multiplexed, is transmitted to the receiver, and is demultiplexed. After demultiplexing, there is one receiver data stream for each transmitter data stream.

The receiver decoder includes a delay circuit for each of the receiver data streams. The delay circuits include, for example, a plurality of shift register stages which are each stepped by a decoder clock. The number of stages in each delay circuit varies and is selected to remove the time diversity from the receiver data streams. The delay inserted in the transmitter data stream when added to the delay inserted in the corresponding receiver data stream is equal to a constant delay for all data streams. The constant delay is established by making the total number of shift register stages travelled by the combination of a transmitter

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