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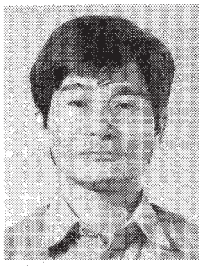

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A Single-Chip 300 Baud FSK Modem

ASHRAF K. TAKLA, MEMBER, IEEE, AND YUSUF A. HAQUE

Abstract **— A 300 baud single-chip FSK modem, implementing an RS-232 handshaking interface, will be described. The device is a full duplex asynchronous modem that meets both Bell 103 and CCITT V.21 specifications. It incorporates the protocol required for automatic answer/originate, loss of carrier termination, and a 14 s abort timer. The device also implements analog and digital loopback capabilities for local and remote testing, respectively. The chip is implemented using a double-poly CMOS technology and uses a standard 3.58 MHz colorburst TV crystal. Inclusion of the handshaking protocol facilitates interfacing the modem to a standard RS-232 interface in stand-alone applications, or a UART in other applications, where the modem is integrated into the data terminal equipment.**

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I. INTRODUCTION

MODEMS are a key component in the expanding world of data communications. These devices were traditionally expensive and built with MSI, some discrete and smaller SLI chips. With the advent of analog capability on MOS technology, rapid advances have been made. The device to be described here implements all the modulation, demodulation, filtering, as well as protocol control functions for both the internationally accepted 300 baud frequency shift keying standards in a 5 μm CMOS technology without requiring any external components, thus allowing a low-cost low-power stand-alone modem implementation [1].

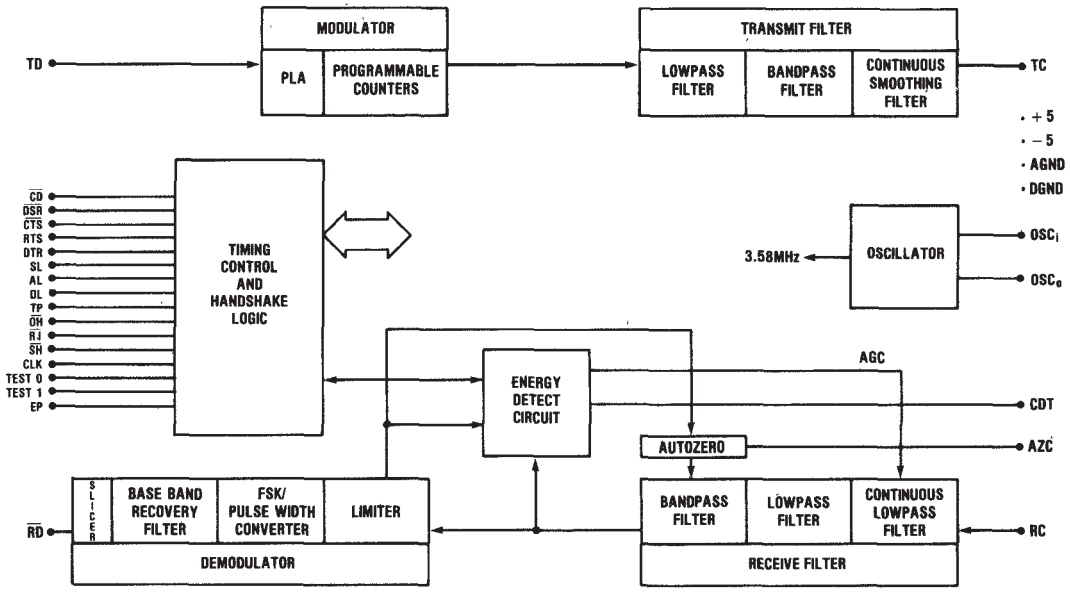


Fig. 1. 300 baud FSK modem block diagram.

II. System Architecture

The block diagram of the FSK modem is shown in Fig. 1. The input to the modulator is the TD (transmit data) signal, which is the digital data to be modulated. This input would typically be provided by the RS-232 interface, or a UART. The modulator generates a square wave whose frequency is shifted in response to the transmit data input.

The transmit filter outputs a frequency shift keying signal at the TC (transmit carrier) output. The frequency of the FSK signal corresponds to the fundamental frequency of the square wave at the input of the filter.

On the receive side, the receive filter, whose input is the receive carrier, rejects the adjacent channel energy and improves the signal-to-noise ratio of the incoming carrier.

The output of the receive filter is fed into the demodulator, where the digital data are retrieved from the filtered FSK signal.

The next major block is the energy detect circuit. It detects energy levels at which reception and demodulation of data are considered reliable.

The last block is the timing control and handshake logic, which, besides controlling all the other blocks, also implements the RS232 interface protocol and controls the Bell 103 and CCITT V.21 operations.

III. Modulator

The modulator generates a square wave whose frequency is shifted in a phase-continuous fashion. The generated frequency is a function of four signals: TD (transmit data), mode (answer/originate), SL (103/V.21 select), and V.25

TABLE I
Modulator Frequency As a Function of SL (V21/Bell 103), A/O (Answer/Originate), TD (Transmit Data), and V25 Answer Tone

MODE	SL	A/O	TD	V25	FREQUENCY (Hz)
103 ORIGINATE	0	0	0	0	1070
	0	0	1	0	1270
103 ANSWER	0	1	0	0	2025
	0	1	1	0	2225
V21 ORIGINATE	1	0	0	0	1180
	1	0	1	0	980
V21 ANSWER	1	1	0	0	1850
	1	1	1	0	1650
V25 ANSWER TONE	X	X	X	1	2100

those nine are used for 103 operation, two for high band, and two for low band. One of these two frequencies represents a mark and the other a space. Two bands are used to enable simultaneous transmission and reception of data on the same channel, hence, the duplex operation. The other four frequencies are allocated for V.21 operation, and the ninth frequency is used for V.25 answer tone.

The modulator, as shown in the left-hand side of Fig. 2, consists of a PLA (programmable logic array) driving a programmable polynomial counter, followed by a divide by 32. The polynomial counter generates 32 times the desired frequency. On each edge of this signal the PLA is updated, thus determining the frequency of next pulse. This ensures phase coherency of the generated signal. Since the output of the programmable polynomial counter is divided by 32, the maximum delay between TD and corresponding frequency shift at TC is 30 μs. The divide by 32 is also used as an auxiliary counter to control the divide of the

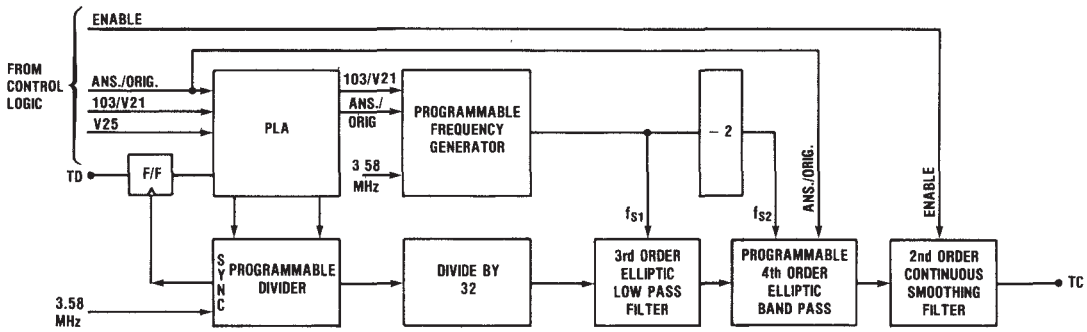
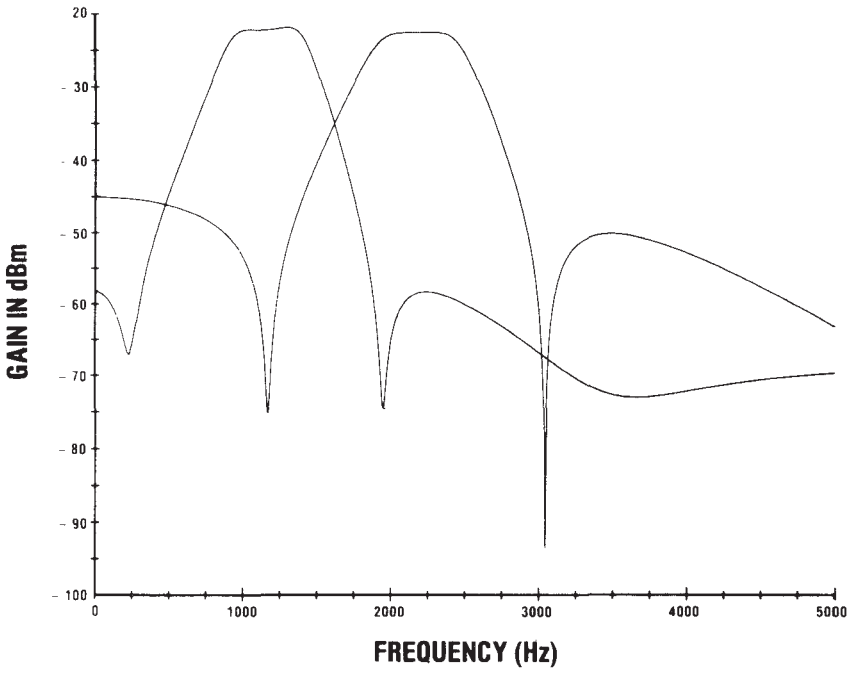


Fig. 2. Block diagram of the modulator.



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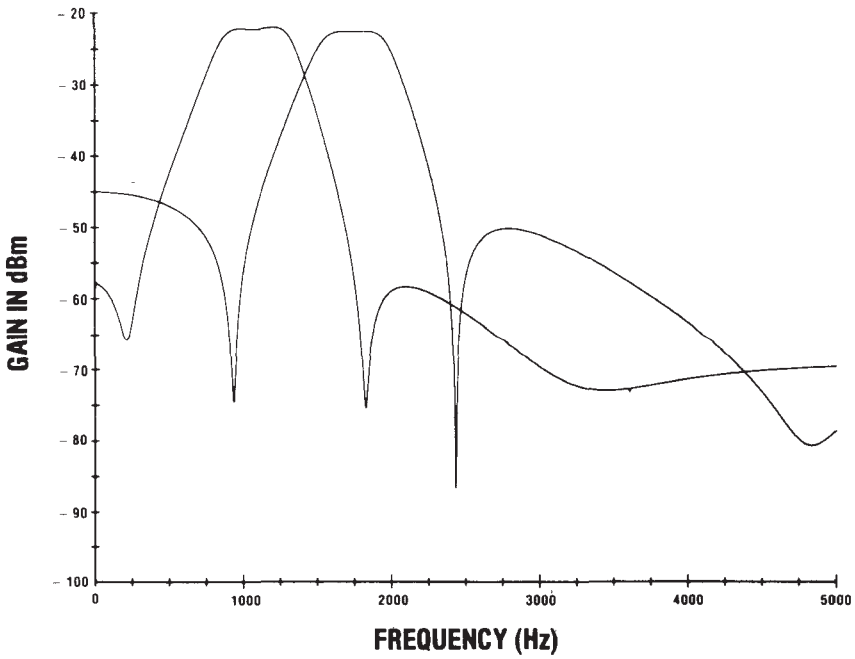


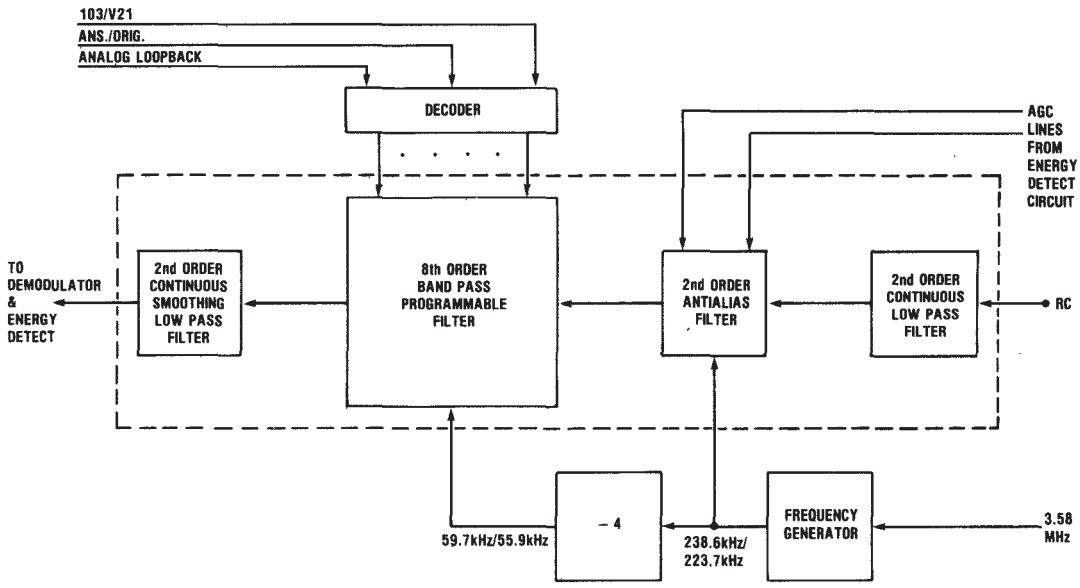


Fig. 4. Receive filter block diagram.

IV. Transmit Filter

The function of the transmit filter is to produce an FSK signal from the phase-continuous frequency-shifted square-wave input.

The structure of the ninth-order filter is shown in the right-hand side of Fig. 2, while its measured frequency response is shown in Fig. 3. The filter consists of three major sections. The first is a third-order switched capacitor elliptic low-pass filter, sampled at 111.9–223.7 kHz, depending on the mode of operation. The cutoff frequency of this filter is programmed by changing the sampling frequency.

The second section is a fourth-order elliptic bandpass filter which is programmed to operate in either the high or low band by changing both the capacitor ratios and the sampling frequency. The third section of the filter is a second-order Sallen and Key continuous smoothing filter. It attenuates the sampling frequency of the preceding section by more than 31 dB and produces a smooth FSK signal at its output.

The prime objective of the transmit filter is to pass the square wave fundamental component, while attenuating its harmonics. These harmonics could be located in the receive band. Unless attenuated by the transmit filter, they would be coupled back through the hybrid, unattenuated by the receive filter, thus causing degradation of bit error rate.

The transmit filter was designed to have a zero at the third harmonic of the square wave, to alleviate the above problem.

The second objective of the transmit filter is to attenuate the out-of-band energy. This is necessary since the modulation process produces energy over a broad spectrum and not just at the mark/space frequencies. The fundamental component is attenuated by 24 dB to produce a signal at

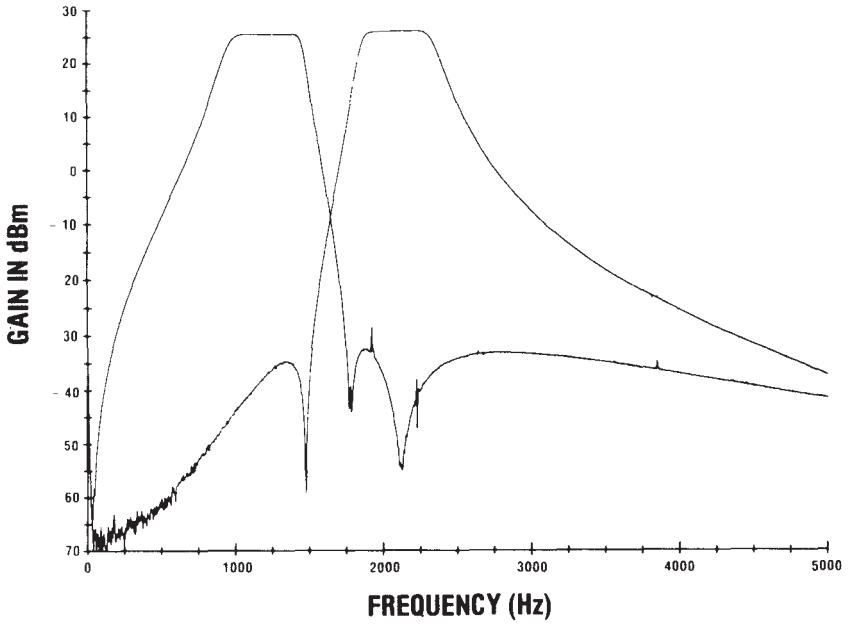
The filters were implemented using biquadratic switched-capacitor second-order sections allowing implementation of both poles and zeros [2]. The filters were designed using bilinear transformation [3] and the results were optimized for acceptable group delay and frequency attenuation performance.

V. Receive Filter

The block diagram of the receive filter is shown in Fig. 4. The receive carrier is first fed into a second-order Sallen and Key continuous low-pass filter, which is followed by a second-order antialiasing filter clocked at 4 times the frequency of the main filter to follow. This antialiasing filter attenuates the incoming signal by 41 dB at the sampling frequency of the following section. This minimizes the aliasing effects and allows the main filter to be clocked at a lower frequency with resulting smaller capacitor ratios [2]. The antialiasing filter has programmable gain that can vary between 5 and 17 dB. The gain of the filter is changed under control of the energy detect circuit thus implementing the automatic gain control function.

The next section is an eighth-order bandpass programmable filter. It can be programmed to operate in one of four configurations depending on the band (high or low) and the specifications (Bell 103 or CCITT V21). Changing the capacitor ratios and sampling frequencies is used to reconfigure this section for the appropriate transfer function. Both the transmit and receive filter can also be configured to work in the same band of frequency allowing true analog loopback, which facilitates testing.

The last section is a second-order Sallen and Key continuous low-pass filter. It attenuates the sampling frequency of the preceeding section by 20 dB and produces a smooth, filtered FSK output which is fed to the demodulator. This



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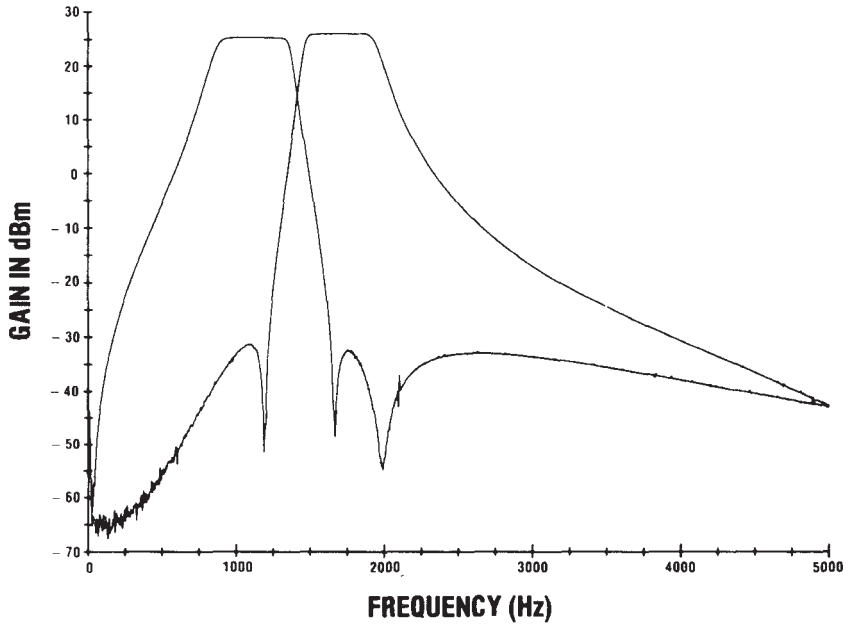

(b)

Fig. 5. Measured transfer function of the receive filter. (a) Bell 103. (b) CCITT V21 specifications.

The measured frequency response of the receive filter is shown in Fig. 5. The receive filter rejects out-of-band noise so that the filtered signal can be demodulated with a resulting low bit error rate.

The filter was designed to reject the adjacent channel energy, which is attenuated by 60 dB. This is essential since that channel is used for carrier transmission, which is coupled back through the hybrid and into the receive section. Unless attenuated by the receive filter, this component would corrupt the demodulated data and result in excessive bit-error rate. The filter was also designed to minimize group delay distortion between the mark and and is centered around the center frequency of the received carrier.

The dynamic range of the receive signal is 50 dB due to the automatic gain control circuit employed.

VI. Demodulator

The demodulator is the most critical part of the modem. Its block diagram, the corresponding waveforms, and the measured frequency response of the baseband recovery filter are shown in Fig. 6.

The input to the demodulator is the filtered receive

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