4. A radio transceiver, comprising:

A) a transmitter, comprising:

i) a Nyquist filter;

ii) differential encoder means coupled to the Nyquist filter for filtering an input information signal to cause selective rotation of a phase value of a modulated signal by a predetermined amount; and

iii) frequency modulator means operably coupled to the differential encoder means for outputting the modulated signal; and

B) a receiver, which receiver does not have a Nyquist filter, for receiving and properly demodulating both:

i) a constant envelope signal occupying a first spectral bandwidth; and

ii) a non-constant envelope signal occupying a second spectral bandwidth, wherein the first spectral bandwidth is different from the second spectral bandwidth.

5. A radio communication system, comprising:

A) a first plurality of transceivers, each transceiver comprising:

i) a transmitter, comprising at least a Nyquist filter and transmitting a constant envelope signal occupying a first spectral bandwidth;

ii) receiver means, which receiver means does not have a Nyquist filter, for receiving and properly demodulating both:

a) a constant envelope signal occupying the first spectral bandwidth; and

b) a non-constant envelope signal occupying a second spectral bandwidth, which second spectral bandwidth is different than the first spectral bandwidth;

B) a second plurality of transceivers, each comprising:

i) a transmitter, comprising at least a Nyquist filter and transmitting a non-constant envelope signal occupying the second spectral bandwidth; and

ii) receiver means, which receiver means does not have a Nyquist filter, for receiving and properly demodulating both:

a) a constant envelope signal occupying the first spectral bandwidth; and

b) a non-constant envelope signal occupying the second spectral bandwidth;

such that transceivers from the first plurality of transceivers can compatibly communicate with transceivers from the second plurality of transceivers.

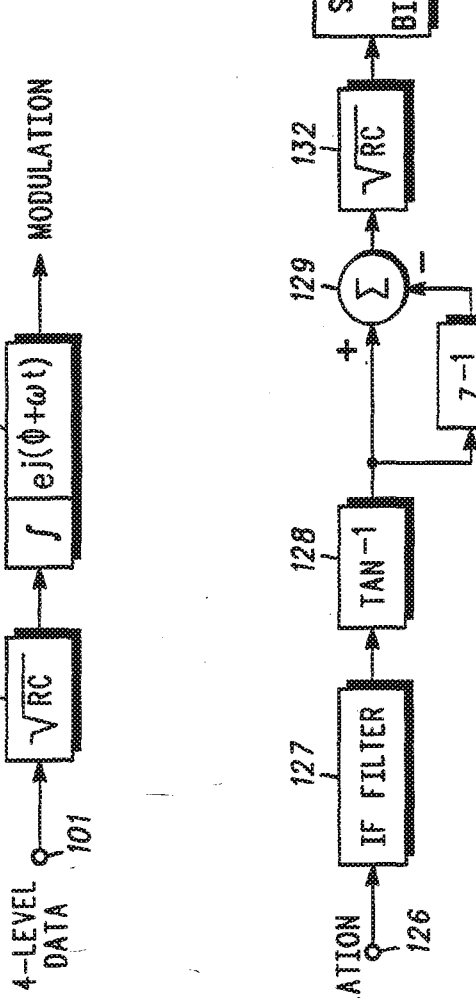

FIG. 1A
— PRIOR ART —

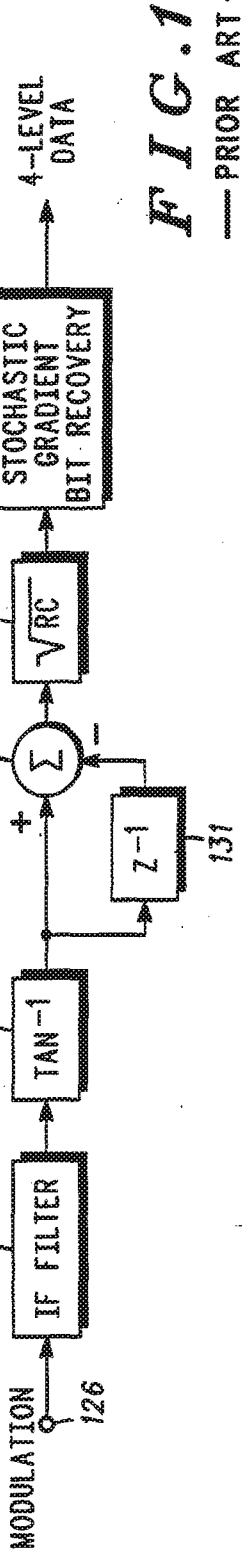

FIG. 1B
— PRIOR ART —

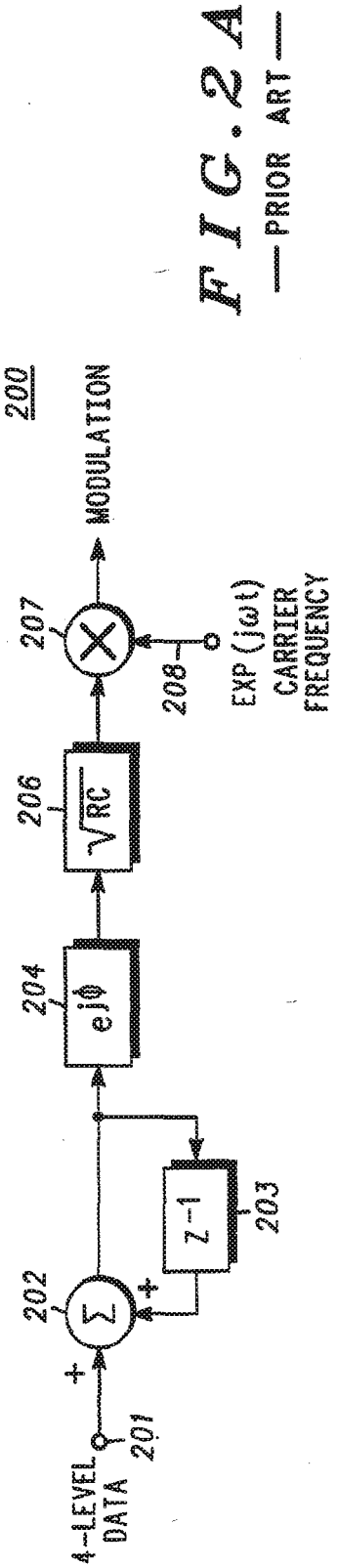

FIG. 2A
— PRIOR ART —

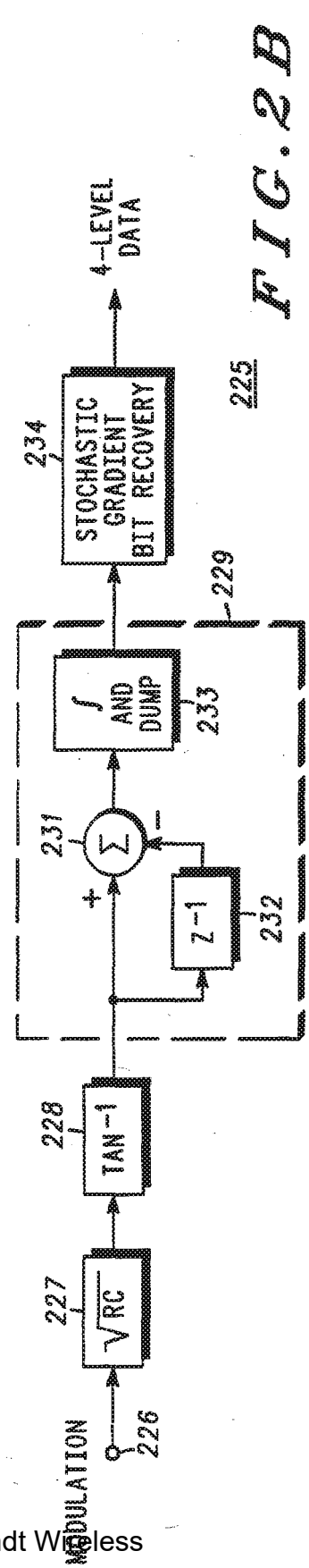

FIG. 2B
— PRIOR ART —

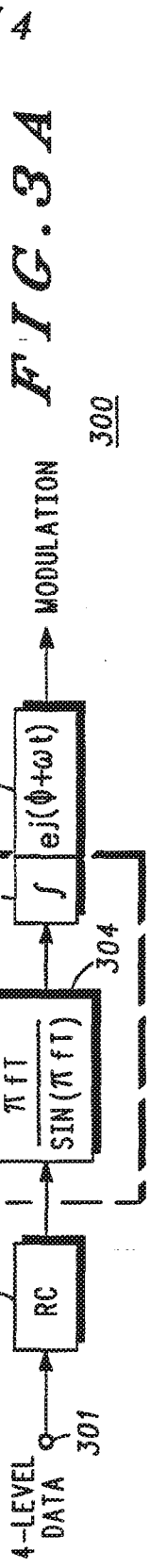

FIG. 3A

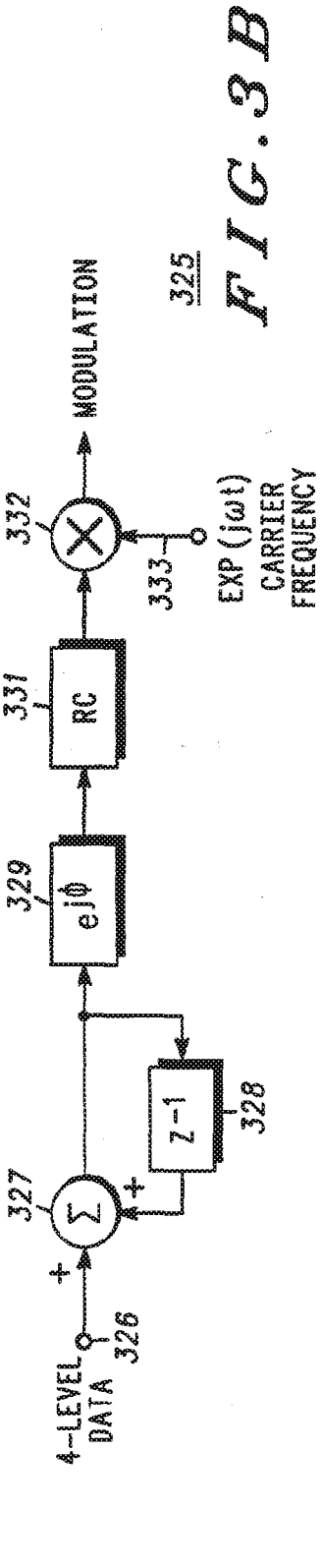

FIG. 3B

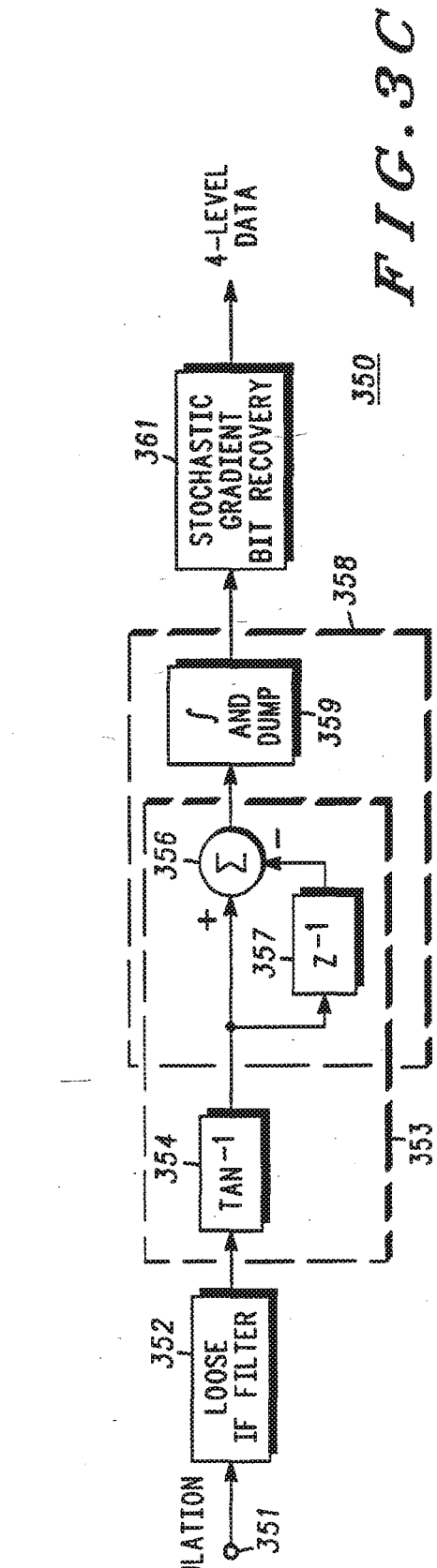
MODULATION
351
LOOSE IF FILTER
352
TAN⁻¹
354
353
Σ
356
357
Z⁻¹
I AND DUMP
359
358
STOCHASTIC GRADIENT BIT RECOVERY
361
350
4-LEVEL DATA

FIG. 3C

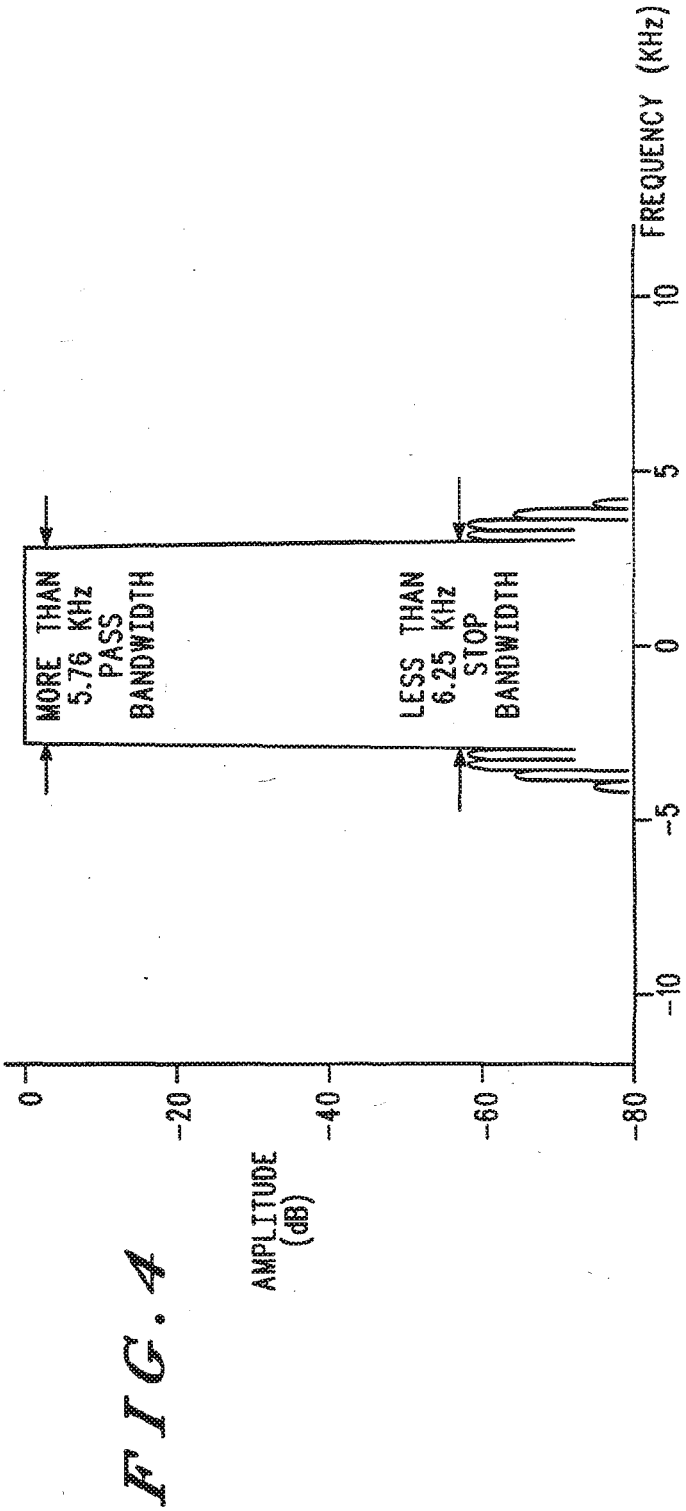
MORE THAN 5.76 KHz PASS BANDWIDTH
LESS THAN 6.25 KHz STOP BANDWIDTH
AMPLITUDE (dB)
0
-20
-40
-60
-80
FREQUENCY (KHz)
10
5
0
-5
-10

FIG. 4

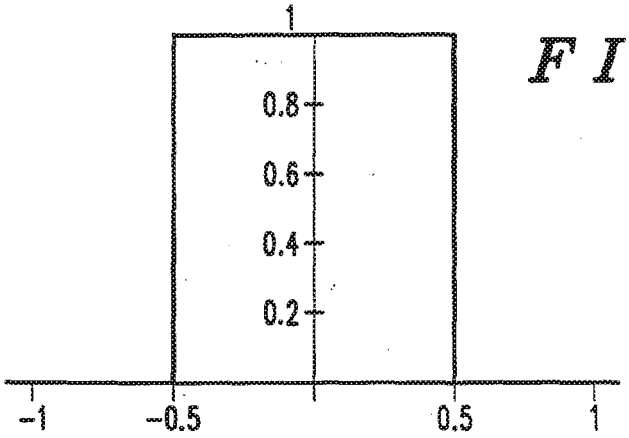

FIG. 5A

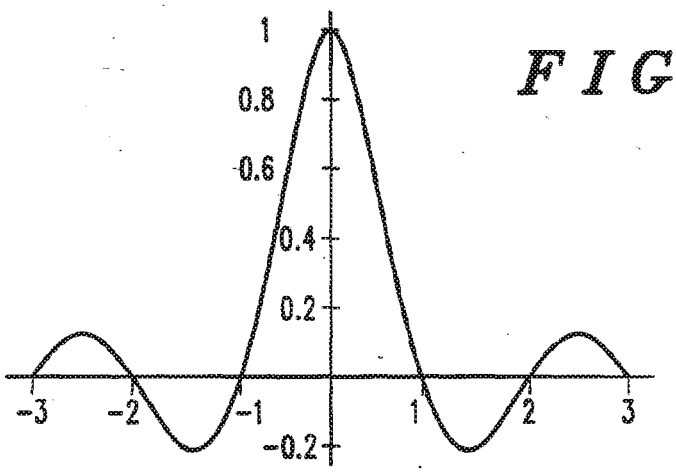

FIG. 5B

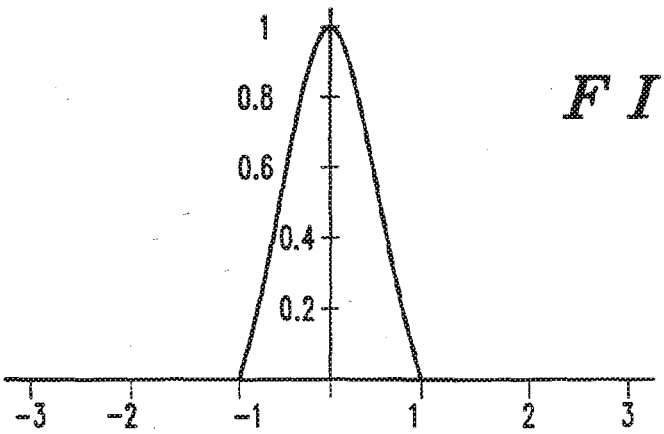

FIG. 5C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/05317

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) : H04L 27/10; H04L 27/18

US CL : 375/9

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : U.S. CL 375/8, 44, 45, 51,52, 58, 60,99; 455/49,50, 73, 74, 93, 142; 329/300, 304; 370/123

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A, 4,720,B39 (FEHER) 19 JANUARY 1988 (SEE FIGURE 1B, COL 2 LINES 29-42)	1-3
A	US,A, 4,601,04B (RYAN) 15 JULY 1986	1-5
A	US,A, 4,731,796 (MASTERTON) 15 MARCH 1988	1-5
A	US,A, 4,843,615 (DAVIS) 27 JUNE 1989	1-5

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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Date of the actual completion of the international search	Date of mailing of the international search report
10 SEPTEMBER 1992	21 OCT 1992
Name and mailing address of the ISA/ Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer SAFOUREK, BENEDICT V Telephone No. (703) 305-4364

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(81) Designated States: AU, BR, CA, JP, KR, VN.

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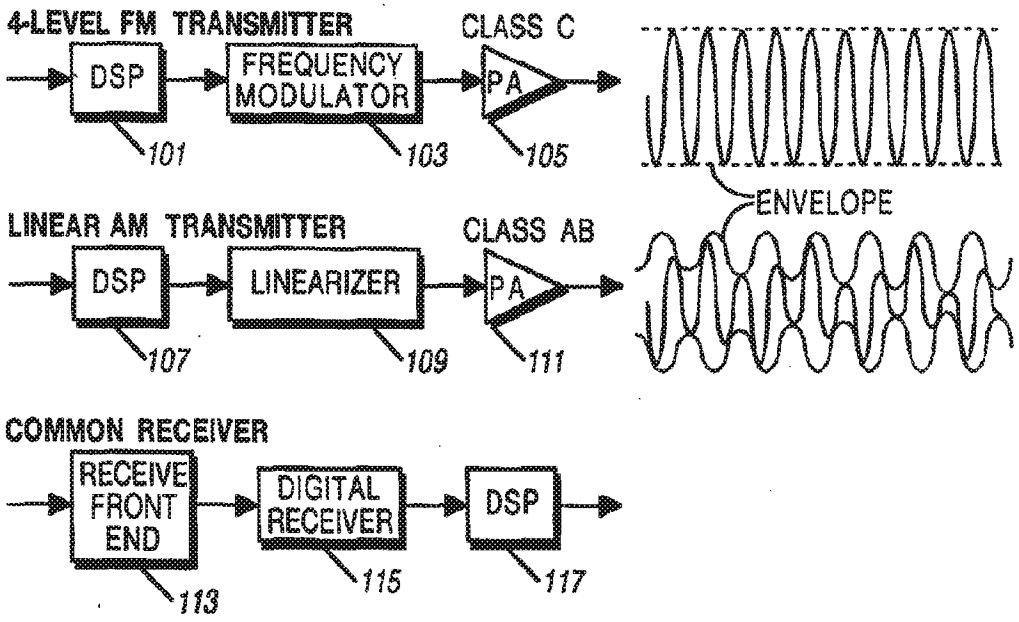
With international search report.

(54) Title: MULTIPLE-MODULATION COMMUNICATION SYSTEM



(57) Abstract

A multiple-modulation communication system includes a transmitter (201, 203, 205, 207, 209, 211, 213, 215, 217, 219) that modulates and transmits communication signals modulated by a first modulation technique (201, 203, 205, 207) and communication signals modulated by a second modulation technique (211, 213, 215, 217). The first modulation technique and the second modulation technique are different. The communication system also includes a receiver (221, 223, 225, 227, 229, 231) capable or receiving the communication signals modulated by the first modulation technique and the communication signals modulated by the second modulation technique and demodulating the communication signals.

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MULTIPLE-MODULATION COMMUNICATION SYSTEM

Field of the Invention

This invention relates to radio frequency signals, including but not limited to transmission and reception of amplitude modulated (AM) and frequency modulated (FM) signals.

Background of the Invention

A radio communication system permits transmission of information between a transmitter and a receiver. A radio frequency (RF) channel permits transmission of information between the transmitter and the receiver. By combining the information with an RF electromagnetic wave of a particular frequency, i.e., modulating the information signal onto a carrier frequency, the resultant modulated information signal may be transmitted through free space to a receiver. Various modulation techniques (e.g., amplitude (AM), frequency (FM), phase, and composite modulation) are known to combine the information signal with an electromagnetic wave. Communication units, such as portable radios, mobile radios, and base stations, contain transmitters and/or receivers.

A linear AM transmitter does not have as much coverage area, i.e., the signal does not travel as far, as an FM transmitter at the same peak transmit power level because the average envelope size of an AM transmission varies below the maximum output level, whereas the average envelope size of an FM transmission is constant at the maximum output level. An FM transmitter,

however, uses more energy to transmit at the same power level as an AM transmitter, and hence the FM transmitter will more quickly drain the battery of a portable transmitter.

Accordingly, there is a need for a transmitter which has the low power characteristic of an AM transmitter while retaining the advantage of coverage area of an FM transmitter.

Brief Description of the Drawings

FIG. 1 shows an FM transmitter, an AM transmitter, and a common receiver in accordance with the invention.

FIG. 2 shows a detailed FM transmitter, a detailed AM transmitter, and a detailed common receiver in accordance with the invention.

Description of a Preferred Embodiment

The following describes an apparatus for and method of transmitting communication signals with a single transmitter and receiving the same signals with a single receiver. Additional communication range is obtained when transmitting FM signals. More efficient battery performance is achieved when transmitting linear AM signals. A single transmitter transmits both AM and FM signals. A single receiver capable of differentiating phase differences demodulates either AM or FM signals. Only one receiver is necessary, and there is no need to inform the receiver of what type of modulation was performed on the transmitted signal.

In the preferred embodiment, FM modulators have 12.5 kHz channels and linear AM modulators have 6.25 kHz channels. The receiver can be the same in either case. The form of modulation used in the present invention is called QPSK-c. This modulation technique is discussed in detail in U.S. Application No. 07/629,931 titled "Multi-Modulation Scheme Compatible Radio" filed on behalf

of Alan L. Wilson et al. on December 19, 1990, which information is enclosed herein by reference. QPSK stands for Quaternary Phase Shift Keying. QPSK-c, where the c stands for compatible, is a linear differential form of QPSK that is AM and FM compatible. It is possible to transmit with a higher average power using FM, and hence increased coverage area is obtained for the signal than when AM is used. An AM transmitter, however, consumes less power and hence is a more efficient user of a portable radio's battery charge or power than an FM transmitter. When using QPSK-c modulation, 4-level FSK (Frequency Shift Keying) is used in FM transmissions and D-QPSK (Differential QPSK) is used in AM transmissions. Switching from AM to FM yields higher average power, and hence increased coverage area for the signal, at the cost of battery charge. Thus range is enhanced and greater coverage is obtained for the same radio, or communication unit, when such coverage is desired. Conversely, switching from FM to AM when extended range is not necessary conserves battery charge. In the present invention, the communication unit changes its type of modulation and thus is more quickly responsive to such a change. This is accomplished by, inter alia, an $x/(\sin x)$ filter, where $x = \pi fT$ in the preferred embodiment, and a phase angle integrator for the exponential function.

One part of FIG. 1 shows a conventional four-level FM transmitter. Information to be transmitted enters a digital signal processor (DSP) 101. The DSP 101 processes the information and sends it to frequency modulator 103 which passes the information to power amplifier (PA) 105 which is rated class C. As shown in FIG. 1, a class C four-level FM transmitter transmits a constant envelope.

A conventional linear AM transmitter is also shown in FIG. 1. Information to be transmitted is processed in DSP 107 and output to a conventional linearizer 109, the output of which is input to a class AB power amplifier 111. As seen in the diagram, an AM signal has a non-constant envelope. The average signal power of

an AM signal is less than the average signal power of an FM signal having the same peak envelope size.

Also shown in FIG. 1 is a common receiver which may receive information from both four-level FM transmitter and linear AM transmitters. The common receiver has a front-end receiver 113, a digital receiver 115, and a digital signal processor 117 that processes the information into data or audible speech. A linear AM transmitter has a time-varying amplitude that is reduced for high frequency deviation. Note that DSP 101, DSP 107, and DSP 117 also perform functions other than those shown. Throughout the specification and drawings, the DSP as shown may be a DSP 56001 available from Motorola, Inc.

FIG. 2 shows a detailed implementation of the transmitters and receiver of FIG. 1. An FM transmitter, yielding 4-level FSK data, is shown by blocks 201, 203, 205 and 207. 4-level data is input to a raised-cosine filter 201 which is a splatter filter of the Nyquist raised-cosine finite impulse response type with splatter filter transition ratio alpha = 0.2, as is known in the art. The FM transmitter includes a differential encoder comprised of blocks 203 and 205. A π fT/sin(π fT) filter 203 and an integrator 205 comprise the differential encoder. In the preferred embodiment, the integrator 205 is a simple integrator that uses the modulo 2π property of the phase to avoid overflowing, as is known in the art. The output of integrator 205 is the phase ϕ of the 4-level input signal. A detailed description of one implementation of the raised-cosine filter 201 and π fT/sin(π fT) filter 203 follows in the next paragraph. Phase modulator 207 takes the phase ϕ and modulates it, creating a complex-valued result that is designated $e^{j\phi}$. The output, $e^{j\phi}$, of phase modulator is input to switch 209.

The cascaded filter implementation of the Nyquist raised-cosine filter 201 and the π fT/sin(π fT) filter 203 may be implemented as follows. Let $H(\omega)$ equal the frequency response of an ideal Nyquist raised cosine filter. The normalized corner frequency is 1 radian/second, and the normalized symbol time (denoted by T) is π seconds, and

$$H(\omega) = 1 \quad \text{for } 1 - \alpha \geq |\omega|$$
$$H(\omega) = \frac{1}{2} + \frac{1}{2}\cos\left(\frac{\pi(|\omega| - 1 + \alpha)}{2\alpha}\right) \quad \text{for } 1 - \alpha < |\omega| \leq 1 + \alpha$$
$$H(\omega) = 0 \quad \text{for } 1 + \alpha < |\omega| .$$

The impulse response, h(t), of the filter is found with the inverse Fourier transform, and noting that H(ω) is an even function:

$$h(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} H(\omega)e^{j\omega t}d\omega = \frac{1}{\pi}\int_{0}^{\infty} H(\omega)\cos(\omega t)\,d\omega$$

$$= \frac{1}{\pi}\int_{0}^{1-\alpha} \cos(\omega t)\,d\omega + \frac{1}{2\pi}\int_{1-\alpha}^{1+\alpha} \cos(\omega t)\,d\omega + \frac{1}{2\pi}\int_{1-\alpha}^{1+\alpha} \cos\left(\frac{\pi(\omega - 1 + \alpha)}{2\alpha}\right)\cos(\omega t)\,d\omega$$

Using the identity $\cos(x)\cos(y) = 0.5\cos(x+y) + 0.5\cos(x-y)$ and performing the integration:

$$h(t) = \frac{\sin[(1-\alpha)t]}{\pi t} + \frac{\sin[(1+\alpha)t] - \sin[(1-\alpha)t]}{2\pi t}$$
$$+ \frac{\sin[\pi+(1+\alpha)t] - \sin[(1-\alpha)t]}{4\pi\left(\frac{\pi}{2\alpha} + t\right)} + \frac{\sin[\pi-(1+\alpha)t] + \sin[(1-\alpha)t]}{4\pi\left(\frac{\pi}{2\alpha} - t\right)}.$$

Using the identity $\sin(\pi+x) = -\sin(x)$, regrouping terms, and then using the identity $\sin(x+y) + \sin(x-y) = 2\sin(x)\cos(y)$:

$$h(t) = \frac{\pi}{8\alpha^2 t}\,\frac{\sin[(1+\alpha)t] + \sin[(1-\alpha)t]}{\left(\frac{\pi}{2\alpha}\right)^2} = \frac{\pi\sin(t)\cos(\alpha t)}{\alpha^2}.$$

The filter function h(t) can be sampled at discrete time intervals to realize the Nyquist raised-cosine finite impulse response filter 201.

The shaping filter, f(t), is derived as follows, where F(ω) is the frequency response of the shaping filter, T is the symbol time which equals 208.333 μsec for 9600 bits per second which equals π seconds for the normalized system used in H above, and

$$F(\omega) = \frac{\omega T/2}{\sin(\omega T/2)} \quad \text{for all frequencies.}$$

The frequency range of interest for $F(\omega)$ is $-1.2\pi < \omega T < 1.2\pi$, which is the frequency range covered by the Nyquist filter $H(\omega)$ when the roll-off factor $\alpha = 0.2$. In order to find a suitable impulse response, the function F will be approximated with a Fourier series of cosine terms, and the result will be transformed to the time domain.

A time interval to approximate F is first selected to be $\pm 1.33333\pi$, because it must exceed $\pm 1.2\pi$ and be less than $\pm 2\pi$ because there is a singularity in F at $\omega T = 2\pi$. The Fourier series expansion follows, where x is the normalized frequency:

$$F(x) = \frac{\pi x}{\sin(\pi x)} = f_0 + \sum_{k=1}^{\infty} f_k \cos\left(\frac{2\pi k x}{1.33333}\right) \text{ where } x = fT = \frac{\omega T}{2\pi},$$

$$f_0 = 0.75 \int_{-2/3}^{2/3} F(x)\, dx, \text{ and}$$

$$f_k = 1.5 \int_{-2/3}^{2/3} F(x) \cos\left(\frac{2\pi k x}{1.33333}\right) dx \quad \text{for } k > 0.$$

These integrals are easily evaluated numerically. The first twelve terms appear in the following table.

k	f_k	k	f_k
0	1.35697	6	0.0281791
1	-0.4839	7	-0.0210304
2	0.189043	8	0.0162746
3	-0.0982102	9	-0.0129571
4	0.0594481	10	0.0105541
5	-0.0396059	11	-0.00875928

Performing the inverse Fourier transform on the series as follows:

$$f(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} F(\omega)e^{j\omega t}d\omega = \frac{1}{2\pi}\int_{-\infty}^{\infty}\left(f_0 + \sum_{k=1}^{\infty} f_k \cos\left(\frac{2\pi kx}{1.33333}\right)\right)e^{j\omega t}\,d\omega$$

$$= \frac{1}{2\pi}\left(f_0\delta(t) + \sum_{k=1}^{\infty}\frac{f_k}{2}\delta(0.75\ kT) + \sum_{k=1}^{\infty}\frac{f_k}{2}\delta(-0.75\ kT)\right)$$

where $\delta(t)$ represents the Dirac delta function. Sampling at 8 samples per symbol yields non-zero samples and 0.75 x 8 = 6 sample intervals. The middle or 0th sample has amplitude f_0, and the remaining samples have amplitudes $f_k/2$ for k=±1, ±2, ±3,... Cascading the previously computed h(t) with f(t) yields the filters necessary for an FM $\pi/4$ DQPSK-c transmitter, as used in the preferred embodiment of the present invention. Although the above implementation is shown in band-limited form, band-limiting is optional and is not required for the present invention.

The AM transmitter, yielding D-QPSK data, is comprised of blocks 211, 213, 215, and 217. Four level data having levels of $\pm\pi/4$ and $\pm 3\pi/4$ enters a differential encoder comprised of a summer 211 and a delay 213. The output of this differential encoder enters a phase modulator 215, where the output of the phase modulator 215 has complex components I and Q at one sample per symbol. I represents the in-phase component, and Q represents the quadrature component. The output of modulator 215 is input to raised cosine filter 217 with alpha = 0.2 where raised cosine filter 217 is similar to raised cosine filter 201. The output of raised cosine filter 217 is input to switch 209. Whichever form of transmission is selected, either FM or AM, the output of that part of the transmitter is input to modulator 219, which modulates the signal to the carrier frequency ω.

Blocks 211, 213, and 215 each operate at the rate of one sample/symbol or 4800 symbols/second. Blocks 201 and 217 interpolate from 1 sample/symbol to N samples/symbol at the

output, where N is usually 10 or more, but at least greater than one. Blocks 203, 205, and 207 each operate at N samples/symbol.

For efficiency and to eliminate redundant parts in the preferred embodiment, only one class AB PA is used in the transmitter, thus the linear AM transmitter configuration of FIG. 1 is used to embody the entire transmitter of FIG. 2, blocks 201 through 219 inclusive. Because the preferred embodiment of the present invention uses a DSP, transmitter blocks 201, 203, 205, 207, 209, 211, 213, 215, 217, and 219 are easily implemented in the DSP 107 of the linear AM transmitter. Because blocks 201 through 219 are included in the DSP 107, it is unnecessary to duplicate DSP 101, frequency modulator 103, and PA 105. The modulator 219 is also implemented in the DSP 107, and the output of the modulator 219 is input to the linearizer 109 prior to transmission.

A detailed common receiver is also shown in FIG. 2. In the preferred embodiment, the receiver blocks 221, 223, 225, 227, 229, and 231 are all implemented in the DSP 117. When the receiver and transmitter are in the same communication unit or radio, one or more DSPs may be used to support the functions of DSP 107 and DSP 117. A loose IF (intermediate frequency) filter 221, first receives a modulated signal. The output of the loose IF filter 221 is input to inverse tangent function 223, which is part of a frequency demodulator including blocks 223, 225 and 227. Blocks 225 and 227 are also part of a differential encoder also including integrate and dump filter 229, the function of which is described in detail in the following paragraph. The output of block 223 is input to summer 227 and the positive form of the delayed component is subtracted from block 227 as output from block 225. The output of integrate and dump filter 229 is input to stochastic gradient bit recovery block 231 the output of which is four level data as transmitted initially. Stochastic gradient bit recovery is well known in the art. Because the receiver is sensitive only to phase, the envelope does not matter and both FM and AM transmission may be received and properly decoded by this common receiver. Thus, because a more powerful AM PA is required than for an FM PA for the same

range, a switch of the two modulations temporarily although draining more power gains extra (greater) coverage area.

The impulse response for the integrate and dump filter 229 is derived below, in a closed-form solution that is expressed in terms of the sine integral function Si(x), which is well known in the art. A band-limited integrate and dump filter is achieved when a portion of the side lobes are filtered out of the frequency response. The portion of the frequency response that is necessary for good fidelity in the symbol recovery is in the range $-(1+\alpha)/(2T)$ Hz to $(1+\alpha)/(2T)$ Hz. Because of a spectral null at 1/T Hz, the response is restricted to 1/T Hz cutoff. Where H(x) is the frequency response of a band-limited integrate and dump filter:

$$H(x) = \frac{\sin(\pi x)}{\pi x} \quad \text{for } |x| < 1$$

$$H(x) = 0 \quad \text{for } |x| \geq 1.$$

Where h(t) is the impulse response of the filter H(x), $\omega = 2\pi x$, and $H(\omega)$ is an even function:

$$h(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} H(\omega)e^{j\omega t}d\omega = \frac{1}{2\pi}\int_{-2\pi}^{2\pi} \frac{\sin(\omega/2)}{\omega/2} e^{j\omega t}d\omega$$

$$= \frac{1}{\pi}\int_{0}^{2\pi} \frac{2}{\omega}\sin(\omega/2)\cos(\omega t)\,d\omega$$

$$= \frac{1}{\pi}\int_{0}^{2\pi} \frac{1}{\omega}\left(\sin[(t+1/2)\,\omega] - \sin[(t-1/2)\,\omega]\right)d\omega$$

$$= \frac{1}{\pi}\left(\int_{0}^{2\pi(t+1/2)} \sin(y)\frac{dy}{y} - \int_{0}^{2\pi(t-1/2)} \sin(y)\frac{dy}{y}\right)$$

$$= \frac{1}{\pi}\{Si[2\pi(t+1/2)] - Si[2\pi(t-1/2)]\} \quad \text{where } Si(x) = \int_{0}^{x} \sin(t)\frac{dt}{t}.$$

Although the above implementation is shown in band-limited form, band-limiting is optional and is not required for the present invention.

Hence in the present invention, when it is desired for any reason by command or as determined by the radio, the radio will automatically switch from AM to FM to gain extra range for a particular signal. The radio or communication unit may also receive a signal, such as from a base station or other controlling unit including another radio, instructing it to transmit with a particular modulation. Similarly, the radio will automatically switch from FM to AM to gain better battery efficiency. This switching takes place in switch 209, which is controlled by a DSP in the preferred embodiment.

Although the preferred embodiment uses QPSK-c modulation, a common receiver can still be used for any modulation that distinguishes data by phase, i.e., where all the constellation points fall on a circle, such as QPSK, D-QPSK, and CORPSK (Correlated PSK).

Although a DSP is used to perform many of the functions of the present invention, discrete elements or other programmable logic may also be used and will achieve the same effect.

What is claimed is:

Claims

1. A communication system characterized by:

a transmitter that modulates and transmits communication signals modulated by a first modulation technique and communication signals modulated by a second modulation technique, wherein said first modulation technique and said second modulation technique are different; and

a receiver capable of receiving said communication signals modulated by said first modulation technique and said communication signals modulated by said second modulation technique and demodulating said communication signals.

2. The communication system of claim 1, further characterized in that said first modulation technique is amplitude modulation and said second modulation technique is frequency modulation.

3. The communication system of claim 1, further characterized in that said first modulation technique is differential quaternary phase shift keying and said second modulation technique is 4-level frequency shift keying.

4. The communication system of claim 1, further characterized in that said communication signals modulated by said first modulation technique are transmitted when low power consumption by said transmitter is desired.

5. The communication system of claim 1, further characterized in that said communication signals modulated by said second modulation technique are transmitted when greater signal coverage by said transmitter is desired.

6. A communication unit characterized by:

means for modulating communication signals by a first modulation technique, producing a first modulated signal;

means for modulating communication signals by a second modulation technique, producing a second modulated signal, wherein said first modulation technique and said second modulation technique are different;

means for selecting between said first modulated signal and said second modulated signal, producing a selected signal; and

a transmitter for transmitting said selected signal.

7. The communication unit of claim 6, further characterized in that said first modulation technique is amplitude modulation and said second modulation technique is frequency modulation.

8. The communication unit of claim 6, further characterized in that said first modulation technique is differential quaternary phase shift keying and said second modulation technique is 4-level frequency shift keying.

9. The communication unit of claim 6, further characterized in that said first modulated signal is selected when low power consumption by said transmitter is desired.

10. The communication unit of claim 6, further characterized in that said second modulated signal is selected when greater signal coverage by said transmitter is desired.

1/1

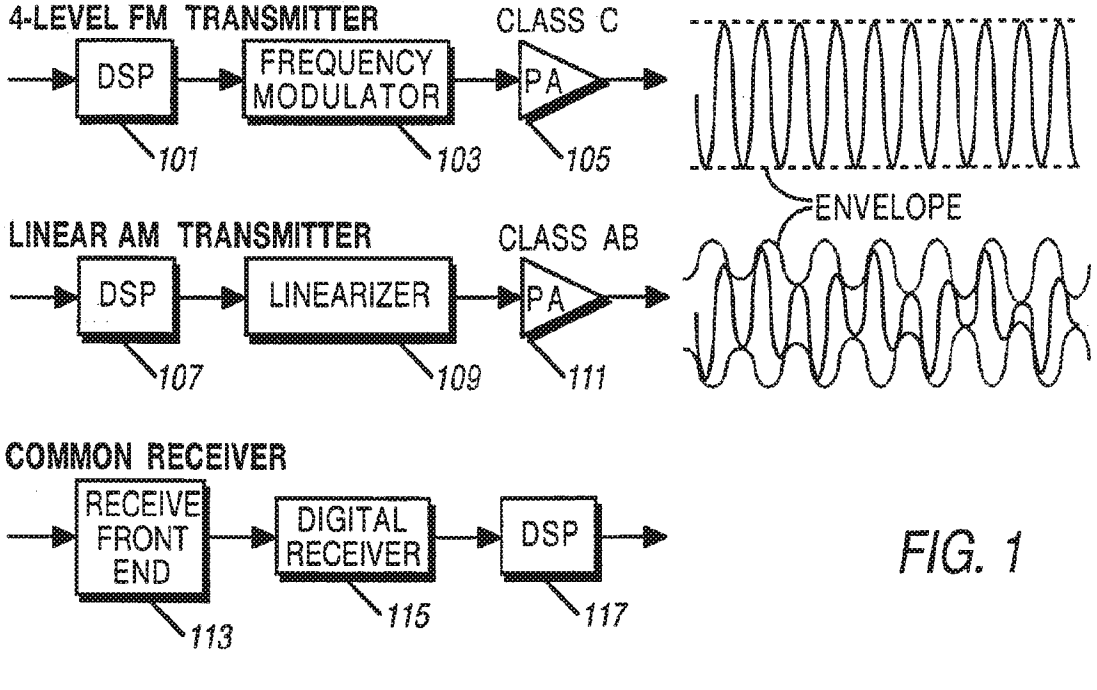
4-LEVEL FM TRANSMITTER
DSP
FREQUENCY MODULATOR
CLASS C
PA
101
103
105
ENVELOPE
LINEAR AM TRANSMITTER
DSP
LINEARIZER
CLASS AB
PA
107
109
111
COMMON RECEIVER
RECEIVE FRONT END
DIGITAL RECEIVER
DSP
113
115
117

FIG. 1

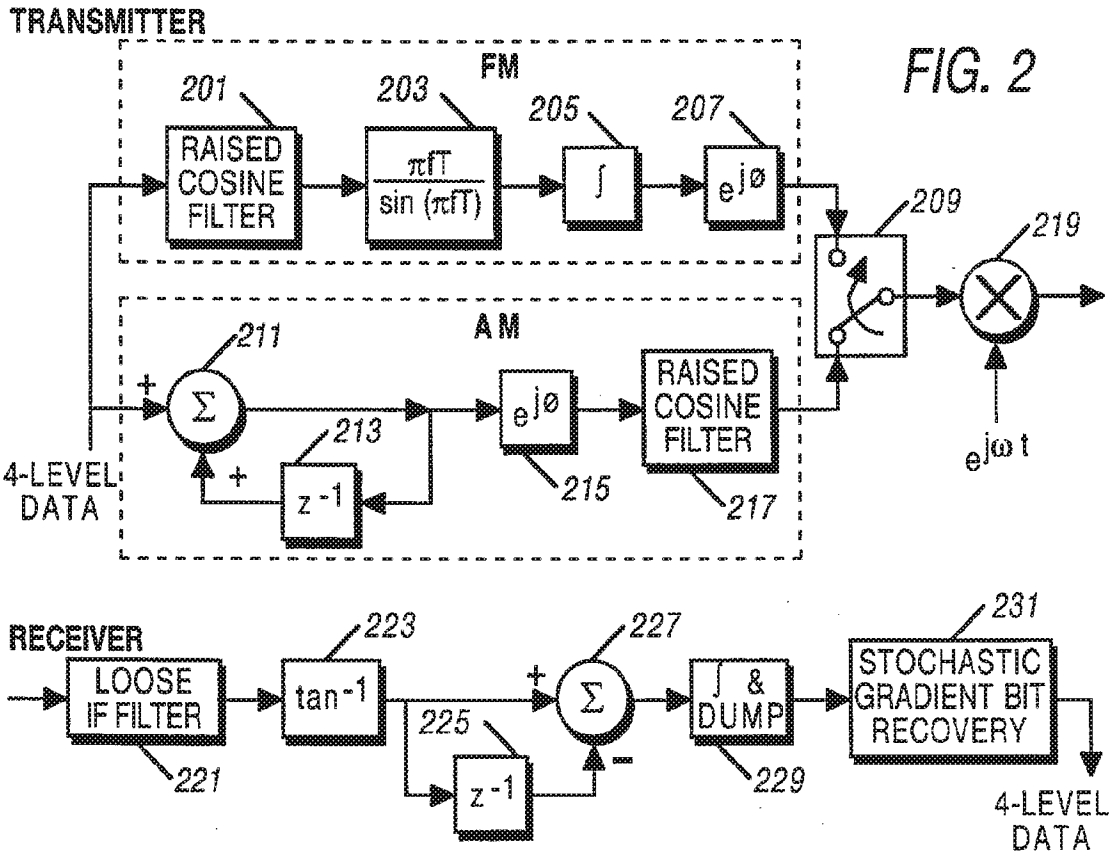
TRANSMITTER
FM
201
RAISED COSINE FILTER
203
πfT / sin (πfT)
205
∫
207
e^jø
209
219
AM
211
Σ
213
z -1
e^jø
215
RAISED COSINE FILTER
217
4-LEVEL DATA
e^jω t
RECEIVER
LOOSE IF FILTER
221
tan-1
223
225
z -1
227
Σ
∫ & DUMP
229
231
STOCHASTIC GRADIENT BIT RECOVERY
4-LEVEL DATA

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/00580

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H04L 27/10, 14, 16, 22; H04B 1/00, 02, 66, 16; 7/00
US CL :332/120, 151; 375/46, 59, 80; 455/61, 93, 102, 142, 343
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 332/108, 119, 120, 150, 151; 375/45, 46, 54, 59, 79, 80; 455/59, 61, 93, 101, 102, 108, 142, 205, 343

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US, A, 5,155,455 (COWLEY ET AL) 13 October 1992, Figure 2.	6-8, 10 --- 1-5, 9
X	US, A, 5,109,542 (ECKLUND) 28 April 1992, Abstract and Figure 1.	1-5
Y	Digital Analog Communication System, 1979 by John Wiley and Sons Inc., K. S. Shanmugam, "Power Requirements", pages 414, 416.	4, 9
A	US, A, 5,163,159 (RICH ET AL) 10 November 1992.	1-10
A	US, A, 4,660,192 (POMATTO SR.) 21 April 1987	1-10
A	US, A, 3,378,773 (JEFFERS) 16 April 1968.	1-10

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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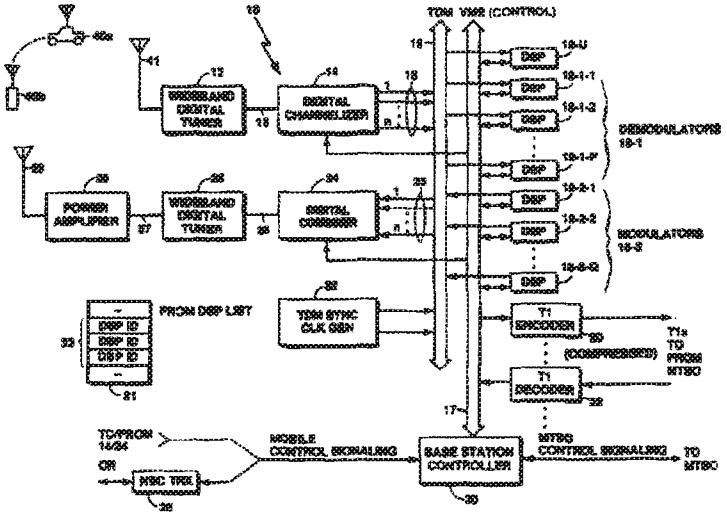

(57) Abstract

A wireless communication system basestation making use of a wideband, multichannel digital transceiver having incorporated therein a time division multiple-access (TDM) bus for providing digital samples of a plurality of wireless communication channels, wherein the time slot duration and frame rate of the TDM bus may be reconfigured. The invention allows various air interface standards, even those having different channel bandwidths, to be serviced by the same basestation, without having to install additional or different equipment, and by automatically redistributing signal processing resources, eliminating the need to reconfigure the basestation when different types of wireless signalling must be accomodated.

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WIDEBAND WIRELESS BASESTATION MAKING USE OF TIME DIVISION MULTIPLE-ACCESS BUS HAVING SELECTABLE NUMBER OF TIME SLOTS AND FRAME SYNCHRONIZATION TO SUPPORT DIFFERENT MODULATION STANDARDS

FIELD OF THE INVENTION

This invention relates generally to communication networks, and in particular to a wireless communication system basestation making use of a wideband, multichannel digital transceiver having incorporated therein a time division multiple-access (TDM) bus for providing digital samples of a plurality of wireless communication channels, wherein the TDM bus has a selectable number of time slots per frame, and a selectable frame synchronization rate, to permit dynamic allocation of modulator and demodulator signal processing resources, and to support wireless modulation standards of different bandwidths.

BACKGROUND

The basestations used by the providers of current day multiple channel wireless communication services, such as cellular mobile telephone (CMT) and personal communication systems (PCS), typically designate signal processing equipment for each single receiver channel. This is probably a result of the fact that each basestation is configured to provide communication capability for only a limited predetermined number of channels in the overall frequency spectrum that is available to the service provider.

A typical basestation may thus contain several racks of equipment which house multiple sets of receiver and transmitter signal processing components that service a prescribed subset of the available channels. For example, in an Advanced Mobile Phone Service (AMPS) cellular system, a typical basestation may service a pre-selected number of channels, such as 48, of the total number, such as 416, of the channels available to the service provider.

Certain types of wireless service providers would prefer, however, to employ equipment that would be more flexible, both in terms of where it can be located, as well as in the extent of the available bandwidth coverage provided by a particular transceiver site. This is particularly true in rural areas where cellular coverage may be concentrated along a highway, and for which the limited capacity of a conventional 48 channel

transceiver may be inadequate. This may also be true in other instances, where relatively large, secure, and protective structures for multiple racks of equipment are not necessarily available or cost effective, such as for PCS applications.

One way to resolve this difficulty is to implement a basestation transceiver using a high speed analog-to-digital (A/D) converter and equipment which makes use of efficient digital filtering algorithms such as the Fast Fourier Transform (FFT), to separate the incoming signal energy into multiple ones of the desired channels. On the transmit side, this basestation implementation includes an inverse FFT processing combiner which outputs a combined signal representative of the contents of the communication channel signals processed thereby. In this manner, relatively compact, lightweight, inexpensive, and reliable digital integrated circuits may be used to cover the entire channel capacity offered by the service provider, rather than only the subset of the available channels.

Thus unlike prior art basestations, the wideband digital basestation is capable of receiving any channel. While this provides a certain number of advantages as described above, it also poses a number of unique problems to the service provider.

Perhaps most importantly, there exists a need to efficiently support a varying number of active channels and the required connections into the public switched telephone network.

These connections should be made in such a way as to simplify call control. Indeed, it would be desirable for as many of the call set up control functions required by such a basestation were handled to the maximum extent possible by the basestation itself.

By so simplifying the network interface, the Mobile Telephone Switching Office (MTSO) and/or Mobile Switching Center (MSC) through which the basestation is connected to the Public Switched Telephone Network (PSTN) may be freed, as much as possible, from the details of maintaining a proper connection from the PSTN to the remote subscriber unit.

Secondly, the basestation should make efficient use of the available resources to process each call. In particular, while the wideband channelizer separates the signals into channels, certain other signal processing resources such as demodulators and modulators are also required.

Using the wideband front end, any channel in the bandwidth available to the service provider is available at any time. However, it is desirable for such a basestation

to only activate as many of the other, per-channel resources as is required to support the present call density.

By making the basestation's implementation of call processing resources as modular as possible, the basestation could initially be configured to support a limited number of channels. Then, as the demand for services grows, additional channels could be supported by the addition of the necessary resources.

In other instances, the basestation should be reconfigurable in the event of an change or expansion in one type of service. For example, given the emergence of several air interface standards such as code division multiple access (CDMA) as well as time division multiple access (TDMA) standards for cellular, it is desirable for a given wideband basestation to be able to support each such standard, thereby reducing the number of such basestations that need to be deployed. However, it would be desirable if the resources allocated to one particular air interface, when no longer needed, could then be made available to process signals formatted using the other air interface. That is, as the demands of one type of service or the other come and go, the basestation should be automatically reconfigured, without requiring an investment in new or different basestation resources.

Thus, several difficulties exist with a wideband digital basestation that can process at any time, any one of many channels in the RF bandwidth available to a service provider.

SUMMARY OF THE INVENTION

Briefly, the invention is a wideband transceiver basestation for a wireless communication system. The receiver portion of the basestation includes a digital channelizer which provides digital samples of multiple wireless channel signals, and a time division multiplexed (TDM) data bus, to provide switching functionality between the various channel outputs and other basestation receiver resources such as digital demodulators.

On the transmitter side, basestation signal processing resources such as digital modulators are also connected to a multichannel digital combiner over the TDM bus. Thus, the same flexibility in switching functionality is provided between transmitter signal processing resources and the transmitter channel inputs.

A synchronization and clock generation circuit has the capability of selecting the number of time slots, as well as the bus frame rate, to be used on the TDM bus. The number of time slots and the bus frame rate depend upon, respectively, the number of the channel signals and the bandwidth of each of the channel signals provided by the channelizer.

More particularly, the wideband basestation transceiver includes a receive antenna and one or more digital tuners that provide wideband digital signal energy to a digital channelizer. The digital channelizer, in turn, produces a plurality of channel signals, with each channel signal representing the signal energy in one of the radio frequency channels. The channel signals each consist of a series of digital samples.

The digital samples of each channel signal are, in turn, connected to a time division multiplex (TDM) bus. A basestation controller grants access to the TDM bus by each channel signal in a predetermined timeslot, in a predetermined order.

The samples of the digital channel signals are then forwarded to an available one of the associated receiver resources, such as a demodulator. The demodulators, typically implemented in a digital signal processor (DSP), are then connected to an outgoing landline such as a T1 line to a telephone switching office (MTSO) or mobile switching center (MSC) for further connection into the PSTN.

Accordingly, when the basestation is to support a particular number of channel signals simultaneously, each channel signal having a bandwidth as dictated by a particular modulation or air interface standard to be supported, the TDM bus reconfigured accordingly, to provide the required number of bus time slots, as well as the frame repeat rate required to support the desired per-channel sampling rate.

When it is desired that the basestation support a protocol which has a larger number of narrower bandwidth channels, the bus timing circuits are reconfigured to provide a correpondingly larger number of time slots at a slower frame rate, and, likewise, when the basestation is to support a protocol which has a smaller number of wider bandwidth channels, the bus timing circuits are again reconfigured to provide a smaller numnber of time slots at a higher frame rate.

As a result of the switching functionality provided by the TDM bus, the basestation is thus capable of supporting different signalling protocols, or air interface standards, which have different channel bandwidths.

The invention provides other advantages as well.

For example, the basestation may efficiently service both code division multiple access (CDMA) and time division multiple access (TDMA) signals at the same time. In such an arrangement, there are at least two digital channelizers, with one allocated to separating the incoming RF energy into the channel bandwidths required by TDMA, and another channelizer dedicated to separating the energy into the bandwidth required by CDMA. As the channels are activated, they are then serviced by the pool of demodulator resources, by allocating the correct number of additional time slots to accommodate each standard.

If, for example, a wideband CDMA mobile unit goes off line, the timeslots as modulators and demodulators freed thereby can be allocated to processing TDMA signals. This results in automatic on-demand redistribution of basestation resources to one signaling standard or another, without intervention by an MTSO, MSC, or the service provider in any way.

Such a system architecture also exhibits scalability, in the sense that additional DSP processors may be added to support additional channels as traffic increases, without having to change the RF front configuration. This is unlike the prior art, where each basestation had a fixed channel allocation, and, to add capacity, one must add additional narrowband receivers and transmitters.

As a result, a basestation according to the invention permits a wireless service provider much greater flexibility in planning implementations, as different and even future protocols can be supported.

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the advantages provided by the invention, reference should be had to the following detailed description together with the accompanying drawings, in which:

Fig. 1 is a block diagram of wideband digital basestation making use of a time division multiplex (TDM) bus according to the invention;

Fig. 2 is a more detailed block diagram showing addressable bus drivers and receivers which permits access to the TDM bus;

Fig. 3 is a detailed diagram of an addressable bus driver using a dual-port random access memory (DP-RAM);

Figs. 4A and 4B are timing diagrams showing the frame length and number of time slots on the TDM bus for two different channel bandwidths;

Fig. 5 is a detailed diagram of an addressable bus driver using a first-in, first-out (FIFO) memory;

Fig. 6 is a detailed diagram of an addressable bus receiver using a FIFO;

Fig. 7 is a detailed diagram of an addressable bus transmitter using a FIFO;

Fig. 8 is a sequence of operations performed by a basestation control processor in setting up a connection; and

Fig. 9 is an alternate embodiment of the invention making use of multiple tuners and channelizers to support multiple air interface standards while making maximum use of basestation resources.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Fig. 1 is a block diagram of a wideband wireless digital basestation 10 according to the invention. Briefly, the basestation 10 consists of a receive antenna 11, one or more wideband digital tuners 12, one or more digital channelizers 14, a time division multiplex (TDM) bus 16, a control bus 17, a plurality of digital signal processors (DSPs), a first subset of which are programmed to operate as demodulators 18-1-1, 18-1-2,...,18-1-P (collectively, demodulators 18-1); a second subset of which are programmed to operate as modulators 18-2-1, 18-2-2, ..., 18-2-Q; and a third subset 18-u of which are presently idle, transport signal (T-1) encoder 20, a T-1 decoder 22, one or more digital combiners 24, one or more wideband digital exciters 26, a power amplifier 28, a transmit antenna 29, a basestation control processor (controller) 30, and a TDM synchronization clock generator 32.

More particularly, the basestation exchanges radio frequency (RF) signals with a number of mobile subscriber terminals (mobiles) 40a, 40b. The RF carrier signals are modulated with voice and/or data (channel) signals which are to be coupled to the public switched telephone network (PSTN) by the basestation 10. The particular modulation in

used may be any one of a number of different wireless (air interface) standards such as the well known Advanced Mobile Phone Service (AMPS), time division multiple access (TDMA) such as IS-54B, code division multiple access (CDMA) such as IS-95, frequency hopping standards such as the European Groupe Speciale Mobile (GSM), personal communication network (PCN) standards, and the like. Indeed, in a manner that will be described below, the basestation 10 may even be configured to simultaneously process RF signals formatted according to more than one such air interface at the same time.

On the receive side (that is, with respect to the basestation 10), RF modulated signals are first received at the receive antenna 11, and forwarded to the wideband digital tuner 12. The digital tuner 12 downconverts the RF signal received at the antenna to a intermediate frequency (IF) and then performs an analog to digital (A/D) conversion to produce a digital composite signal 13.

Digital tuner 12 is wideband in the sense that it covers a substantial portion of the bandwidth available to the wireless service provider who is operating the basestation 10. For example, if the air interface implemented by the basestation 10 is IS-54B, the wideband digital tuner may downconvert as much as a 12.5 MegaHertz (MHz) bandwidth in the 800-900 MHz range which contains as many as 416 receive and transmit channel signals, each having an approximately 30 kiloHertz (kHz) bandwidth.

The digital channelizer 14 implements a channel bank to separate the downconverted composite digital signal 13 to a plurality, N, of digital channel signals 15.

This digital sampled signal is then further filtered to separate it into the individual 30 kHz channel signals. The digital channelizer 14 can thus be considered as a bank of digital filters with each filter having a 30 kHz bandwidth. The digital channelizer 14 may implement the filter bank using any of several different filter structures, and no particular digital filter structure is critical to the operation of the invention. However, in one preferred embodiment, the digital channelizer 14 consists of a set of convolutional digital filters and a Fast Fourier Transform (FFT) processor. The convolutional digital filters make use of multirate digital filter techniques, such as overlap and add, or polyphase, to efficiently implement a digital filter bank by grouping samples of the downconverted signal together, multiplying the sample groups by a convolutional function, and then forwarding the samples to the FFT for conversion into the n individual channel signals. Such filter banks may

implemented using any of the techniques as are described in the textbook by Crochiere, R.E., and Rabiner, L.R., entitled "Multirate Digital Signal Processing" (Englewood Cliffs, New Jersey: Prentice-Hall, 1983), pages 289-399.

In any event, the channelizer 14 provides N individual digital channel signals 15, wherein each of the N outputs represent information in one of the radio frequency channels originated by the mobile 40. Usually, one-half of the channels are used for transmitting signals and one-half for receiving signals. Thus, in the IS-54B example being described, N is 208, and thus there are 208 receive and 208 transmit channels implemented by the basestation 10.

These N digital channel signals are then provided over the time division multiplex (TDM) bus 16 to a plurality of digital signal processors (DSPs) 18-1-1, 18-1-2, ..., 18-1-P (collectively, demodulator-DSP 18-1). In a manner that will be understood in greater detail shortly, the TDM bus 16 operates as a time division multiplexed cross-bar switch. That is, any one of the N digital channel signals 15 may be connected to any one of the demodulator DSPs 18-1 via the TDM bus 16.

The exact nature of the timing of the TDM bus 16, that is, the number of time slots available for eaech frame of data samples output by the digital channelizer 14, and thus the manner in which the N digital channel signals are transferred over the TDM bus 16, changes depending upon the number of channel signals, N. The manner in which the basestation 10 accomodates these changes in the timing of the TDM bus 16 will be decribed in greater detail below.

The DSPs 18-1 are each programmed to remove the modulation on each channel signal 15 as specified by the air interface standard supported by the basestation 10. There typically is not a one-to-one correspondence between the number of DSPs 18-1 and the number of channel signals, N, provided by the channelizer 14. For example, the DSPs may each process a number, such as 24, of digital channel signals 15 at the same time.

The basestation controller 30, using the VME bus and TDM synchronization clock generator 32, manages access by individual digital channel signals 15 to the TDM bus 16, in a manner that will be described shortly.

The outputs of the digital signal processors 18-1, representing demodulated audio or data signals, are then forwarded over the VME bus 17 to the encoder 20. The VME

bus 17 is a well known industry standard relatively high frequency bus for interconnecting digital processors and components.

The encoder 20, in turn, reformats the demodulated signals as necessary for transmission to a local Mobile Telephone Switching Office (MTSO). The demodulated signals may be reformatted according to any one of a number of well-known time multiplex telephone signal transport protocols, such as the so-called T1 span (or E1). The T1 signals are then processed by the MTSO in an known fashion, to ultimately complete a telephone call from the subscriber unit 40 to a desired destination, such as another telephone subscriber who is connected to the Public Switched Telephone Network (PSTN).

Since each T1 span has a limited capacity, there may be more than one T1 signal necessary to accommodate all of the channels serviced by the basestation 10. In the example being discussed, each T1 signal may be formatted to carry up to 96 IS-54B bandwidth-compressed signals to the MTSO, assuming that the demodulated signals remain as compressed audio. Thus, as few as five T1 lines can be used to carry all of the 416 transmit and receive channels. When not all of the channels are busy, however, on as many of the T1 line resources as are necessary are connected to the MTSO, in a manner that will be understood shortly.

In other words, the demodulated signals output by the DSPs 18-1 may each be sub-rate (e.g., sub-DS0 frequency signals) which still contain additional encoding other than the air interface standard, such as impressed by a bandwidth compression scheme, which is not removed by the basestation 10. Rather, to minimize the required number of time slots used by the T1 signals, such compression may be removed at the MTSO.

The signal flow on the transmit side of the basestation 10 is analogous. Signals are received from the MTSO and provided to the T1 decoder 22, which removes the T1 formatting.

The unformatted T1 signals are then coupled to the DSPs 18 over the bus 17. A subset of the DSPs 18-2-1, 18-2-2, ..., 18-2-Q (collectively, modulators 18-2) then modulate these signals and presents them to the TDM bus 16. Ultimately, these are then each coupled to one of the N digital channel signals 23 input to the combiner 24. As was true in the receive direction, being a cross-bar swtich, the TDM bus 16 permits any one of the modulator DSPs 18-2 to be connected to any one of the channel signal inputs 23.

Although each modulator DSP 18-2 typically processes multiple channel signals, each such channel signal generated by the modulator DSP 18-2 is typically assigned one or more unique time slots on the TDM bus 16, with no two channel signals thus occupying the same time slot. Similarly, no two channel signals on the receive side ever occupy the same timeslot on the TDM bus 16.

As for the demodulators DSPs 18-1, the number of time slots assigned per frame on the TDM bus 16 varies, depending upon the channel bandwidth of the moduation standard implemented.

Other DSPs 18-u may be unused at a particular point in time. However, these unused DSPs remain as an available resource to the basestation 10, should a new mobile 40 request access. The manner in which DSPs are allocated at the time of setting up a call will be described in detail below.

The digital combiner 24 combines the TDM bus outputs to produce a composite IF digital signal 25 representing the N channels to be transmitted. The digital combiner 24 then feeds this combined signal to a digital exciter 26, which generates an RF signal 27. This RF signal 27 is then amplified by the power amplifier 28 and fed to the transmit antenna 29.

In order to set up each call, the basestation control processor 32 must exchange certain control information with the MTSO. For example, when a mobile unit 40 wishes to place a call, the mobile unit 40 indicates this by transmitting on one or more control signal channels. These control signals may be exchanged in one of several ways. As shown, the control signals may be in-band or out of band signals present in one or more of the channel signals output by the channelizer 14 or input to the combiner 24. Alternatively, a separate control signal transceiver 35 may be used to receive and transmit such control signaling.

In either event, the basestation 10 forwards the request for access by the mobile 40 to the MTSO, to set up the end to end connection. Upon receiving an indication from the MTSO that the connection can be made at the remote end, the basestation 10 then performs a number of steps, to insure that the appropriate data path through the TDM bus is then enabled to support communication with between the newly enabled mobile 40 and the MTSO.

For example, the MTSO typically returns a pair of T1 span line and T1 time slot identifiers. These inform the basestation controller 30 on which outgoing T1 line and time slot to place the received signal, and on which incoming T1 line and time slot it can expect to obtain the transmit signal for the mobile 40.

However, before proceeding with a detailed explanation of this call set-up process, a bit more detail of the operation of the TDM bus 16 will be provided. As shown in Fig. 2, the digital channelizer 14 consists of a convolutional digital filter 140, a fast Fourier transform (FFT) 142, as well as a TDM dual port (DP) driver 144.

The operation of the convolutional filter 140 and FFT 142 is not critical to the present invention, and is explained in the co-pending application. It is sufficient here to say that the convolutional filter 140 and FFT 142 make use of multirate digital signal processing techniques, such as overlap and add or polyphase, to efficiently implement a digital filter bank by (1) grouping samples of the downconverted signal 13 together and multiplying them by a weighting function, and then (2) forwarding them to the FFT 142 for conversion into the N individual channel signals.

An exemplary DSP demodulator 18-1-1 and modulator 18-2-1 are also shown in Fig. 2. The demodulator DSP 18-1-1 includes a TDM first-in first-out (FIFO) driver 180-1, a TDM FIFO receiver 182-1, a DSP central processing unit 184-1 and program memory 186-1. Similarly, the modulator DSP 18-2-1 includes a TDM FIFO driver 180-2, a TDM FIFO receiver 182-2, a DSP central processing unit 184-2 and program memory 186-2.

Indeed, the modulator and demodulator DSPs may share the same hardware architecture, with the only difference being the in the program which is enable in the program memory 186, which in turn may control whether the TDM receiver or TDM driver hardware is enabled.

Thus, in the DSP demodulator 18-1-1, only the TDM receiver 182-is enabled (as indicated by the dashed lines around the driver 180-1), since the demodulator 18-1-1 only receives data from the TDM bus 16. Likewise, only the TDM driver 180-2 is enabled in the DSP modulator 18-2-1, since it only transmits data on the TDM bus 16.

On the transmit side, the digital combiner 24 consists of a TDM dual port (DP) receiver 244, an inverse FFT 242, and deconvolutional digital filter 240. In a manner that is described below, the TDM DP receiver 244 reads each of the data samples off the

TDM bus 16 in their assigned time slot, and provides them to the inverse FFT 242 in the required order.

The samples are then operated on by the inverse FFT 242 and deconvolutional filter 240, to provide the composite digital signal 25 (Fig. 1).

Returning attention now to the channelizer 14, a detailed diagram of the TDM DP driver 144 is shown in Fig. 3. Briefly, it operates to assert the output samples from the FFT 142 in the proper time slots on the TDM bus 16. In order to simply the implementation of the TDM bus 16, these time slots are fixedly assigned to particular channels (such as in ascending order by frequency and time slot number). Thus, a sample of a given one, k, of the N channel signals, will always appear in a particular time slot, k, when it is active.

The DP driver 144 consists of a TDM slot counter 200, a first Dual Port Random Access Memory (DP-RAM) referred to as the enable DP-RAM 202, a second DP-RAM referred to as the data DP-RAM 204, and a driver 208 having an enable input EN.

As is conventional, each of the DP-RAMs have two separate address and data ports for reading and writing data, namely, input address and data ports AI and DI, and output address and data ports AO and DO.

In operation, the TDM slot counter 200 receives a pair of signals generated by the TDM synchronization circuit 32 (Fig. 1). The first signal, TDM CLK, is a digital clock signal identifying the clock periods, or time slots, on the TDM bus 16. The second signal is a TDM FRAME SYNC signal, indicating when a new frame starts on the TDM bus 16.

The TDM slot counter 200, which is a standard digital counter, receives the TDM FRAME SYNC signal at a reset input R, and the TDM CLK signal at a clock input (denoted by a chevron in the Figures). Thus, the TDM slot counter 200 continuously keeps track of which consecutively numbered slot on the TDM bus 16 is presently active.

According to the invention, the manner in which the signals are multiplexed onto the TDM bus 16 is changed, depending upon the bandwidth of channels in the modulation scheme being supported. In particular, the number of time slots per frame on the TDM bus 16 is adjusted, depending upon the bandwidth of the modulation of the air interface which is implemented.

Thus, for different air interface standards, the TDM slot counter 200 will receive different TDM CLK and different TDM FRAME SYNC signals. Turning attention

briefly to Figs. 4A and 4B, this concept will be better understood. As shown in Fig. 4A, for the IS-54B TDMA standard, the channelizer 14 provides 208 channels, each having a 30kHz bandwidth. The desired complex-valued (e.g., in-phase and quadrature) sampling rate of each TDMA channel is approximately 40kHz, so that the frame rate, that is, the rate at which each group of 208 samples is asserted on the TDM bus 16, is also set to 40kHz.

Accordingly, in order to support IS-54B channels, the TDM FRAME SYNC signal is controlled by the TDM synchronization clock generator 32 to reset the TDM slot counter 200 every 1/40 kHz, or every 25μs, and the TDM CLK signal is set to clock the complex-valued samples, one from each of the 208 channels, every 25 μs / 208; in other words, to provide approximately one TDM time slot every 121 ns.

As shown in Fig. 4B, for the IS-95 CDMA standard, the channelizer provides 10 channels, each having a 1.25 Mhz bandwidth. The desired complex-valued sampling rate of each channel is approximately 1.67 MHz, so that the frame rate is 600 ns.

Accordingly, in order to support IS-95 channels, the TDM FRAME SYNC signal is controlled to reset the TDM slot counter 200 every 600 ns, and the TDM CLK signal is set to clock the complex-valued samples, one from each of the 10 channels, every 600 ns / 10, or to provide approximately one TDM time slot every 60 ns.

As shown in Fig. 1, the TDM synchronization clock generator receives appropriate signals from the basestation controller 30 via the VMS bus 17 indicating the desired TDM CLK and desired TDM FRAME SYNC rate.

The manner in which data may be asserted on the TDM bus 16 in any of the time slots will now be described in detail. In particular, the enable RAM 202 generates an enable signal 203 indicating when the TDM DP driver 144 may assert data on the TDM bus 16. The AI and DI inputs to the enable DP-RAM 202 are typically written into by the basestation controller 30 during the process of setting up a new call. In particular, as shown in the table depicting the contents of the enable DP-RAM 202, a location in the RAM is associated with each time slot on the TDM bus 16 (e.g., if the TDM bus contained 512 time slots, then the RAM 202 has 512 locations).

A logical "0" in the associated enable DP-RAM 202 location indicates that the TDM driver is inactive in the time slot, that is, no data is to be asserted at that time. A

logical "1" in the associated location indicates that the time slot has been assigned to this particular TDM driver 144.

Thus, to enable a connection through the TDM bus 16, one step for the basestation controller 30, via the VME bus 17, is to write a logical "1" into the DP-RAM 202 location "x" associated with the newly enabled digital channel signal "x". In the example, shown, a "1" has been written at locations "27" and "30", indicating that this particular TDM driver 144 is now active in timeslot numbers 27 and 30.

The data DP-RAM 204 acts as a buffer, writing the digital channel signal samples output by the FFT at the DI input of the data DP-RAM 204. The DP-RAM 204 then stores the data samples until addressed by the TDM slot counter at the output side.

A data dual port (DP) RAM 204 is as a buffer in the case of processing the FFT output. This is because although the samples do come in bursts, or frames, the samples are not necessarily provided by the FFT 142 in the same order as they must be output onto the TDM bus 16. This is a particular phenomenon of at least one of the channelizer algorithms used. Thus, an address associated with each output sample from the FFT is used to determine at which location each sample is written in the data DP-RAM 204.

However, the input data is already in the correct order for the TDM FIFO driver 180-2 used by the DSP modulator. Such a TDM driver 180-2 can thus use a first-in first out memory (FIFO) 210 in the place of a data DP-RAM. As shown in Fig. 5, the configuration and operation of such as TDM FIFO driver 180-2 is somewhat similar to the DP driver 144.

In particular, the TDM slot counter 200, enable DP-RAM 202 and driver 208 operate in the same way as for the embodiment of Fig.3. The only difference is in the connection of the clock signals to the FIFO 210. On the input side, a clock signal is provided by the data source (e.g., the DSP processor 184-2) to cause data to be stored in the FIFO. The signal from the enable DP-RAM 202 is used to clock the FIFO output, DO.

A detailed diagram of the TDM FIFO receiver 182-1 is shown in Fig. 6. It includes a TDM slot counter 200, enable DP-RAM 202, bus receiver 212, and FIFO 214. The TDM slot counter 200 and enable DP-RAM 202 operate as for the TDM FIFO driver 180-1 shown in Fig. 5, to identify when the receiver 212 is to be active. The FIFO 214 is connected to the output of the receiver 212, having its input port connected to the enable

DP-RAM 202 output. The output side of the FIFO is clocked as needed by the destination for the data (such as the DSP processor 184-1 in Fig. 2).

The TDM DP receiver 244 is shown in detail in Fig. 7. As for each of the other driver/receivers, it includes a TDM slot counter 200, enable DP-RAM 202. It includes a data DP-RAM 220 operating similarly to the data DP-RAM in the TDM DP driver 144 (Fig. 3) and bus receiver 218.

With this background in mind, the details of how the basestation control processor 30 effects the switching operation of the TDM bus 16 can now be better understood.

Fig. 8 is a flowchart of these operations. This sequence of steps is initiated (step 300) when the basestation controller 30 receives control signals from the mobile 40 (Fig. 1) indicating that the mobile wishes to have access to the PSTN. The controller 30 then determines whether a free transmit and receive frequency (step 302) are available among the N channels.

An available modulator DSP and demodulator DSP resource are then identified (step 303) by examining a list 33 of free DSP resources maintained in a memory portion 31 of the basestation controller 30 (Fig. 1). The list 33 is updated by removing the two DSPs once allocated.

Access to an MTSO T1 channel (e.g., access to one or more T1 time slots as needed on a particular T1 span line) is then requested from the MTSO by issuing the appropriate MTSO control signaling (step 304). The MTSO then returns T1 span and time slot identifiers to be used for the transmit and receive channels for this connection.

In the next step (306), the appropriate destination and source information is written into the various TDM bus drivers and receivers.

In particular, given a receive channel identification, a receive channel signal time slot on the TDM bus is thus identified. The corresponding location of the enable DP-RAM 202 in the TDM DP driver 144 associated with this time slot is then set to a logical "1" in the manner already described.

Next, a logical "1" is also written into the enable DP-RAM in the TDM receiver 182-1 associated with the DSP demodulator 18-1 which was identified as being an available resource. If the per-channel bandwidth is greater than that which can be supported by a single timeslot, then a sufficient number of logical "1"s are written into the appropriate locations.

Also, now given a transmit channel identification, the free DSP modulator 18-2 is enabled (step 306) to use the TDM bus 16, by writing a logical "1" into the enable DP-RAM of the TDM driver 180-2 connected to the available one of the DSP modulators 18-2. To complete the connection, a logical "1" is also written into the location of the TDM DP receiver 244 associated with the identified transmit channel.

Finally (step 308), the basestation controller 30 issues control signals to the mobile 40 and MTSO to indicate that the connection has been set up.

The invention can also be used to advantage in implementing a basestation 10 which simultaneously services mobiles 40 which use different air interface standards. That is, the basestation 10 may at the same time process signals from a first mobile 40a which uses TDMA (IS-54B) signaling, as well as a second mobile 40b which uses CDMA signaling (IS-95).

As shown in Fig. 9, to support this implementation, the basestation 10 includes a pair of wideband digital tuners 12-1, 12-2. The first digital tuner 12-1 downconverts a bandwidth, such as 5 MHz, from an RF bandwidth which is occupied by TDMA signals. A second digital tuner section 12-2 downconverters a bandwidth, such as 7.5 MHz, which is occupied by CDMA signals.

Next, the tuners 12-1, 12-2 forward the downconverted signals to respective channelizers 14-1, 14-2. The TDMA channelizer 14-1 is configured to separate the received signal into the 30 kHz bandwidth channels specified by IS-54B. Likewise, the CDMA IS-95 channelizer 14-2 is configured to provide 1.25 MHz channels as specified by that standard.

The TDM synchronization clock generator 32 is appropriately set to provide a sufficient number of time slots on the TDM bus 16 to permit transmission of both the required number of samples from the TDMA channelizer 14-1 as well as the required number of samples from the CDMA channelizer 14-2.

The modulators and demodulators are then grouped according to the air interface modulation they must deal with. For example, at any given instant in time, a certain number of DSPs 18-1-T will have been allocated to operate as demodulators for the TDMA channels provided by the TDMA channelizer 14-1. A different set of DSP processors 18-1-C will be serving as demodulators for the CDMA channels provided by the CDMA channelizer 14-2. The active modulator DSPs will likewise be so allocated.

Thus, assuming that each of the DSPs 18 can be configured to execute either a TDMA modulation/demodulation program or a CDMA modulation/demodulation program by simply accessing the correct program memory, the available DSP resources and TDM bus time slots are only allocated as needed.

In other words, the DSPs (and associated T1 connections, for that matter) are allocated according to user demand automatically, and without intervention by the service provider. Thus, for example, as more customers migrate to using CDMA, additional CDMA channels are automatically made available and processed by the DSPs, at the expense of the unused TDMA channels.

A number of advantages can now be see for a basestation 10 configured according to the invention.

When the basestation is to receive and transmit channel signals having a bandwidth as dictated by a particular modulation or air interface standard to, the TDM bus is reconfigured accordingly, to provide the required number of bus time slots, as well as to provide a frame repeat rate approraite to support the required per-channel sampling rate.

When, at a different time, the basestation is to support a protocol having a larger number of narrower bandwidth channels, the bus timing circuits are reconfigured to provide a correpondingly larger number of time slots at a slower frame rate. Likewise, when the basestation is to support a protocol which has a smaller number of wider bandwidth channels, the bus timing circuits are again reconfigured to provide a smaller numnber of time slots at the higher required frame rate.

By disposing the TDM bus 16 between the output of the wideband digital channelizer 14 and the demodulator DSPs 18-1, the demodulator DSPs 18-1 may be allocated only as needed. Similarly, the modulator DSPs 18-2 are allocable as needed, since the TDM bus 16 is disposed between them and the digital combiner 24 as well.

Thus, if the basestation 10 is expected to service only a small number of channels, a correspondingly small number of modulator and demodulator DSPs can be installed in the basestation 10. As the basestation's demands increases, these additional RF channels can be serviced by simply adding more DSPs, and without having to reconfigure the RF front end.

Another advantage is provided in that this switching functionality is distributed at the basestation level as much as possible. In particular, unlike certain prior cellular signal switching techniques, the MTSO need not be concerned with the details of how the mobile units 40 are connected through the basestation. Indeed, the MTSO need not even know or care about which transmit and receive frequencies have been assigned to a particular mobile. All the MTSO need provide is identification of a T1 transport line and time slot on which it expects to receive and provide signals from and to the mobile.

Furthermore, because the basestation may efficiently allocate its demodulator/modulator resources, a number of different air interface standards may be supported by the basestation at the same time, without the need to determine in advance an exact plan for allocating receiver/transmitter resources for each air interface type. Upon detecting a request by a new mobile for access, the basestation simply determines the type of air interface used by the mobile, and then signals the appropriately programmed DSPs, or even initiates the DSPs to run a different modulator/demodulator program, as required to support the additional mobile.

While we have shown and described several embodiments in accordance with the present invention, it is to be understood that the invention is not limited thereto, but is susceptible to numerous changes and modifications as known to a person skilled in the art, and we therefore do not wish to be limited to the details shown and described herein but intend to cover all such changes and modifications as are obvious to one of ordinary skill in the art.

What is claimed is:

CLAIMS

1. A basestation for processing signals in a multiple mobile subscriber unit wireless communication system comprising:

an antenna for receiving signals from a plurality of the mobile units as a composite radio frequency, RF, signal;

wideband digital tuner means, connected to the antenna, for downconverting a selected bandwidth of the RF signal to an intermediate frequency, IF, signal and for performing an analog to digital conversion on the IF signal, to provide a wideband digital tuner output signal;

digital channelization means, being connected to receive the wideband tuner output signal, and providing multiple digital channel signal outputs, each digital channel signal output having a predetermined channel bandwidth, and each digital channel signal corresponding to one of the signals received from one of the mobile units;

a plurality of digital signal processing means, for providing digitally processed channel signal outputs; and

time division multiplex switching means, disposed between the multiple digital channel signal outputs and the plurality of digital signal processing means, the switching means for interconnecting any one of the multiple digital channel signal outputs to any one of the plurality of digital signal processing means; and

time division multipex synchronization timing means, connected to control the time division multiplex means, to provide, at a frame rate which depends upon the predetermined bandwidth of the channel signals, a plurality of time slots, the numer of time slots depending upon the number of digital channel signals.

2. The basestation of claim 1 wherein the signals received from the mobile units contain modulation, and the digital signal processors include demodulators to remove the modulation.

3. The basestation of claim 1 additionally comprising:

signal-transport encoding means, connected to the output of the digital signal processing means, for encoding the digitally processed channel outputs for further transmission to a mobile telephone switching office, MTSO.

4. The basestation of claim 3 wherein the signal-transport encoding means is a T1 encoder.

5. The basestation of claim 1 additionally comprising:

second digital channelization means, being connected to receive the wideband tuner output signal, and providing a second set of multiple digital channel signal outputs, each one of the second set of the digital channel signal outputs having a predetermined channel bandwidth which is different from the predetermined channel bandwidth of said above mentioned first digital channel signals, and each one of the second set of digital channel signals corresponding to one of the signals received from one of the mobile units.

6. The basestation of claim 1 additionally comprising:

second wideband tuner means, connected to the antenna, for downconverting a second selected bandwidth of the RF signal to a second intermediate frequency, IF, signal, and for performing an analog to digital conversion on the second IF signal, to provide a second wideband digital tuner output signal; and

second digital channelization means, being connected to receive the second wideband tuner output signal, and providing a second set of multiple digital channel signal outputs, each one of the second set of the digital channel signal outputs having a predetermined channel bandwidth which is different from the predetermined channel bandwidth of said above mentioned first digital channel signals, and each one of the second set of digital channel signals corresponding to one of the signals received from one of the mobile units.

7. A basestation as in claim 6 wherein the first and second set of digital channel signals are modulated in accordance with first and second standards, respectively.

8. A basestation as in claim 7 wherein the digital signal processors include a first set of digital signal processor means for demodulating said first set of digital channel signals, and a second set of digital signal processors for demodulating said second set of digital channel signals.

9. A basestation as in claim 7 wherein said first and second standards are each different one of a time division multiplex, TDMA, code division multiplex, CDMA, Advanced Mobile Phone System, AMPS, Personal Communications System , PCS, or Groupe Especiale Mobile, GSM.

10. A basestation as in claim 1 additionally comprising:

basestation controller means, connected to the time division multiplex switching means and the digital signal processing means, for maintaining a list of unused digital signal processing means that are not presently interconnected through the time division multiplex switching means to one of the digital channel outputs, and for dynamically allocating digital signal processing means from the list of unused digital signal processing means to be interconnected to one of the digital channel outputs only when the digital channel output contains an active signal being transmitted by the mobile unit which has not yet been assigned to one of the digital signal processing means.

11. A basestation as in claim 1 wherein the time division multiplex switching means further comprises:

a time division multiplex, TDM, data bus including data lines;

basestation controller means, connected to the TDM bus, and to generate TDM bus synchronization signals and driver address signals, the TDM bus synchronization signals used to identify access timeslots on the TDM bus; and

TDM bus driver means, connected to the TDM bus, the basestation controller means, and at least one of the digital channel signals, for receiving the TDM bus synchronization signals and the driver address signals, for storing the driver address signals, and for asserting the digital channel signal on the TDM bus when the value of driver address signals corresponds to the value of the bus synchronization signals, thereby indicating that a timeslot associated with the digital channel signal is currently active.

12. A basestation as in claim 11 wherein the basestation controller means, connected to the TDM bus, additionally generates receiver address signals, and the time division multiplex switching means additionally includes:

TDM bus receiver means, connected to the TDM bus, the basestation controller means, and at least one of the digital signal processor means, for receiving the TDM bus synchronization signals and the receiver address signals, for storing the receiver address signals, and for reading a signal asserted on the TDM bus and providing such asserted signal to the digital signal processor means when the value of receiver address signals corresponds to the value of the bus synchronization signals, indicating that a timeslot associated with the digital signal processor is currently active.

13. A wideband basestation as in claim 6 wherein the first and second channelizers each comprise:

a convolutional digital filter, connected to receive the respective one of the digitized wideband signals; and

a fast Fourier transform, FFT, processor, connected to receive the output of the convolutional digital filter, and to provide the digital channel signals.

14. A basestation as in claim 1 additionally comprising:

a second plurality of digital signal processing means, connected to receive digital input signals from a communication signal source;

a wideband digital combiner, being connected to receive a second plurality of digital channel signals, and to provide a composite digital signal for transmission;

wherein the time division multiplex switching means is also disposed between the second plurality of digital signal processors and the wideband digital combiner, the switching means connecting any one of the second set of digital signal processors to any one of the digital channel signals input to the combiner;

a wideband digital exciter, connected to receive the composite digital signal and to provide a combined RF signal; and

a transmit antenna, connected to receive the combined RF signal and the radiate the combined RF signal.

15. A basestation as in claim 14 additionally comprising:

basestation controller means, connected to the time division multiplex switching means and the first and second plurality of digital signal processing means, for

maintaining a list of all unused digital signal processing means that are not presently interconnected through the time division multiplex switching means to one of the digital channel outputs, and for dynamically allocating digital signal processing means from the list of unused digital signal processing means to function as one of the first or second digital signal processing means only when the digital channel output contains an active signal being transmitted by the mobile unit which has not yet been assigned to one of the digital signal processing means, or when the digital inputs from the communications source are active.

16. A wideband basestation transceiver including:

a wideband digital tuner that provides a wideband digital signal at an output;

a digital channelizer, connected to the wideband tuner, to produce a plurality of sampled channel signals, with each channel signal representing signal energy in one of a plurality of radio frequency channels serviced by the basestation;

a time division multiple-access, TDM, data bus;

means for selectively connecting the digital samples of each channel signal, in turn, to the TDM bus;

basestation controller means, for controlling the means for selectively connecting the digital samples of each channel signal to the TDM bus, by so connecting each channel signal in a predetermined timeslot, in a predetermined order;

means, coupled to the TDM bus, for selecting the digital samples in a particular timeslot, and for generating a reconstructed channel signal thereby;

means for allocating a demodulator to be coupled to the reconstructed channel signal when the associated radio frequency channel is active, the demodulator providing a demodulated channel signal;

means for allocating a T1 line encoder to the demodulated channel signal, to format the demodulated channel signal for transmission over a T1 span line;

means for coupling the T1 line to a mobile telephone switching office, MTSO, or mobile switching center, MSC, for further connection into the public switched telephone network, PSTN; and

A synchronization and clock generation circuit has the capability of selecting the number of time slots, as well as the bus frame rate, to be used on the TDM bus. The number of time slots and the bus frame rate depend upon, respectively, the number of the channel signals and the bandwidth of each of the channel signals provided by the channelizer.

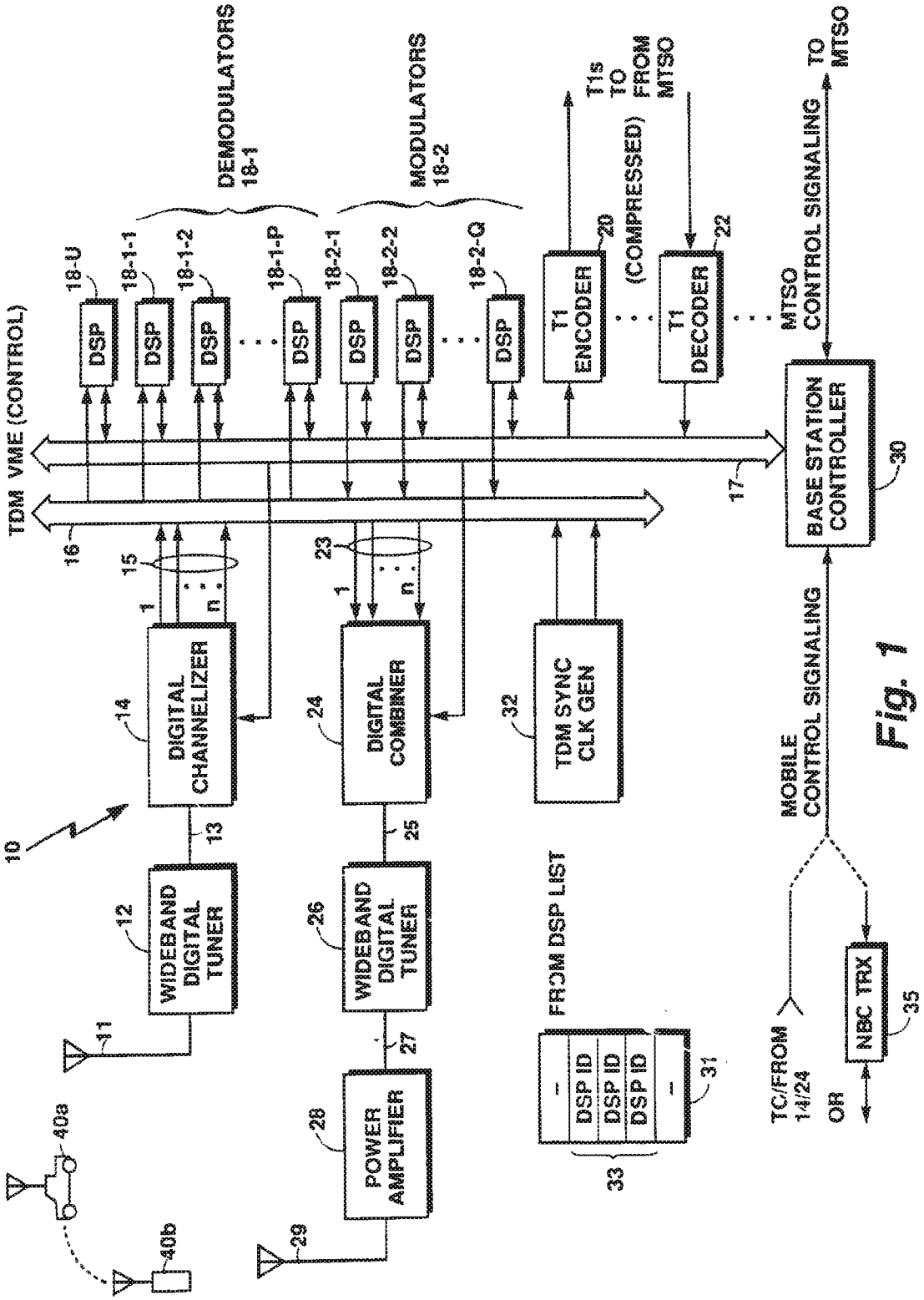


Fig. 1

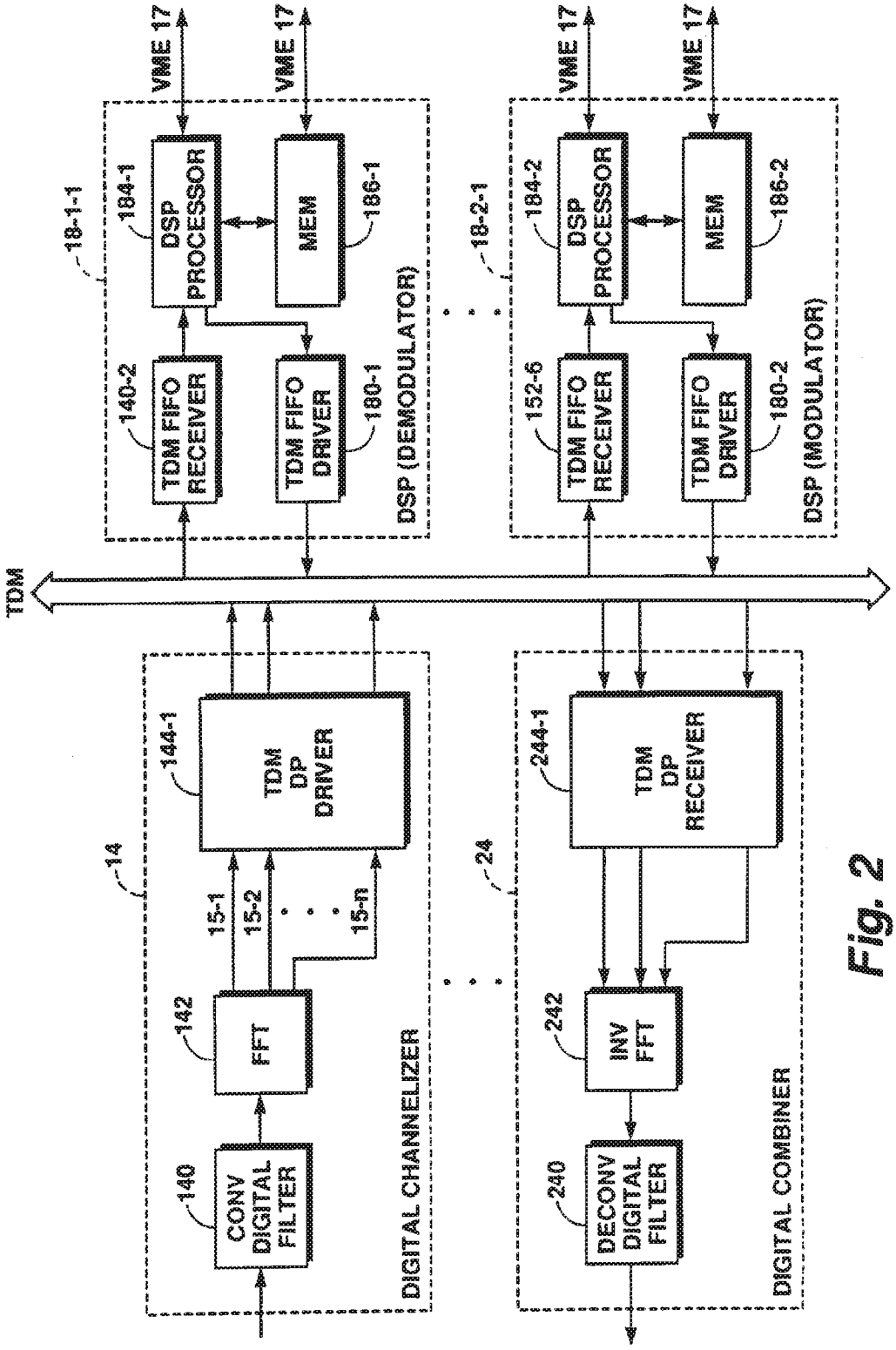
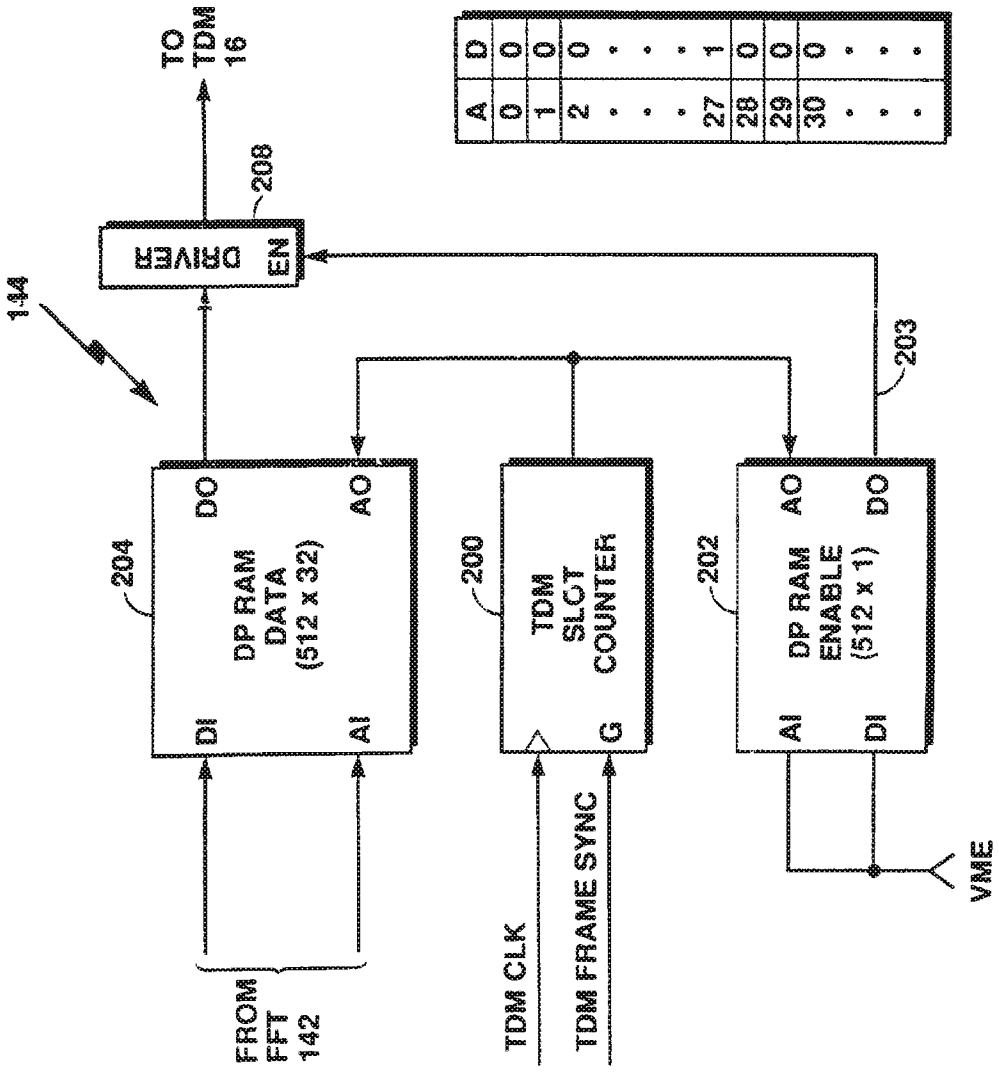


Fig. 2

Fig. 3


TO TDM 16
208
DRIVER
EN
144
203
204
DP RAM DATA (512 x 32)
DO
AO
DI
AI
200
TDM SLOT COUNTER
G
202
DP RAM ENABLE (512 x 1)
AO
DO
AI
DI
VME
FROM FFT 142
TDM CLK
TDM FRAME SYNC
A 0 1 2 . . . 27 28 29 30 . . .
D 0 0 0 . . . 1 0 0 0 . . .

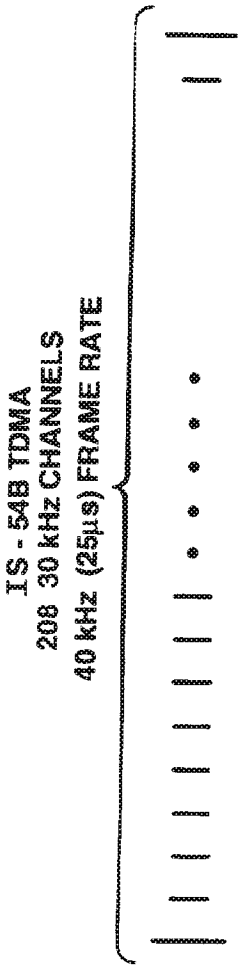


Fig. 4A

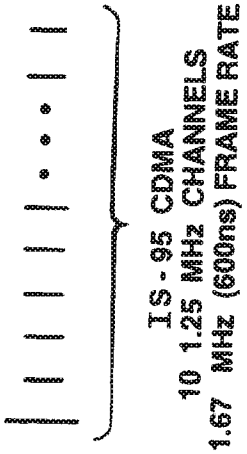
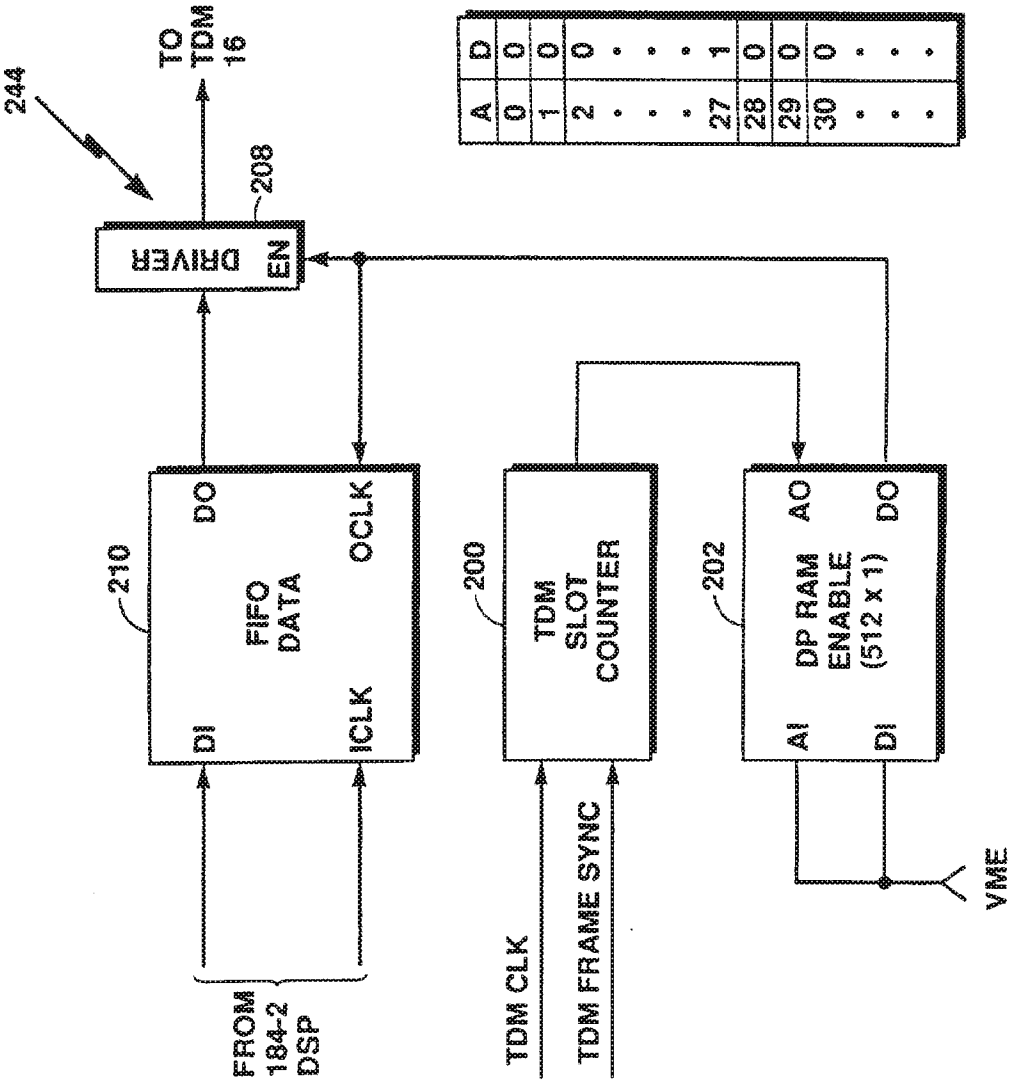


Fig. 4B

Fig. 5



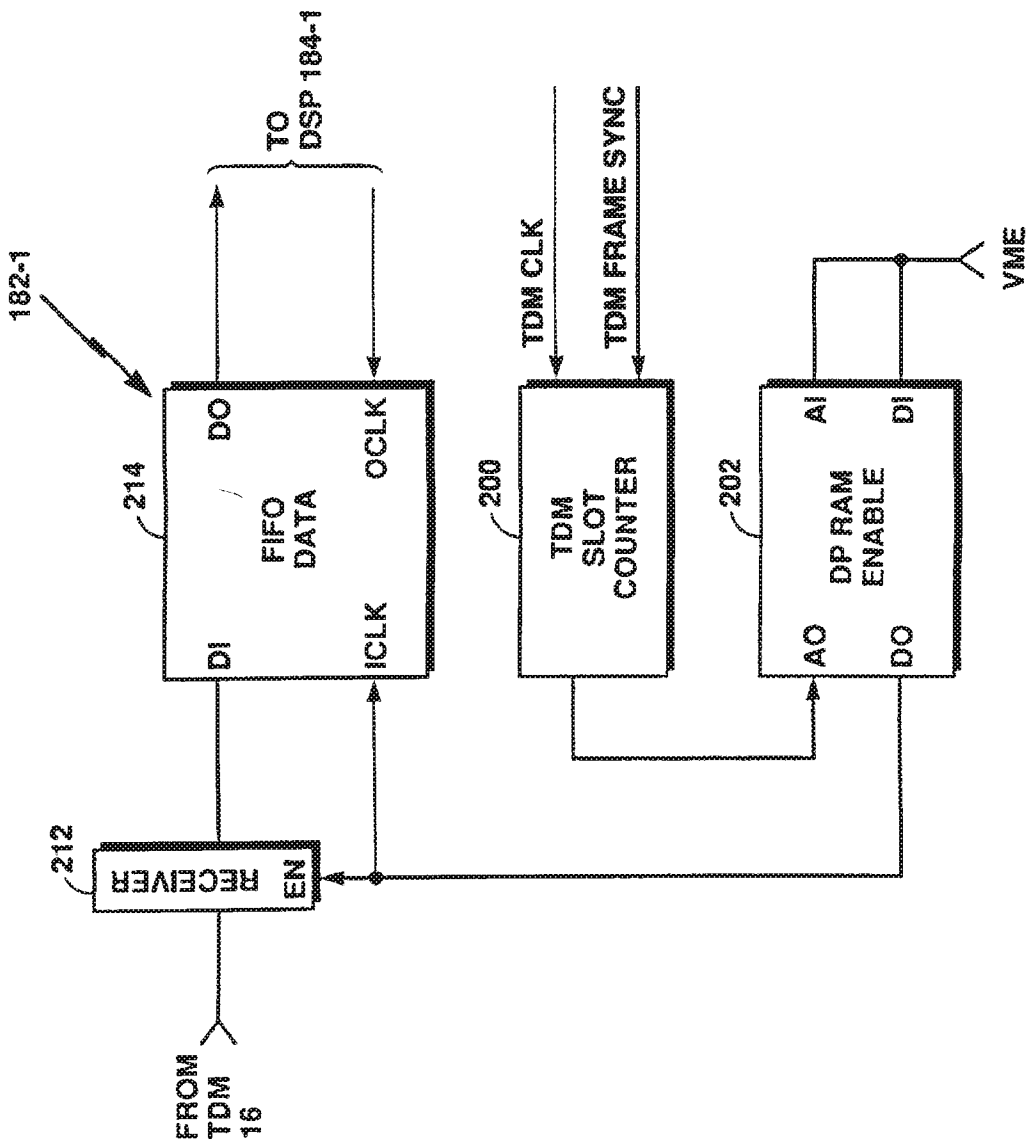
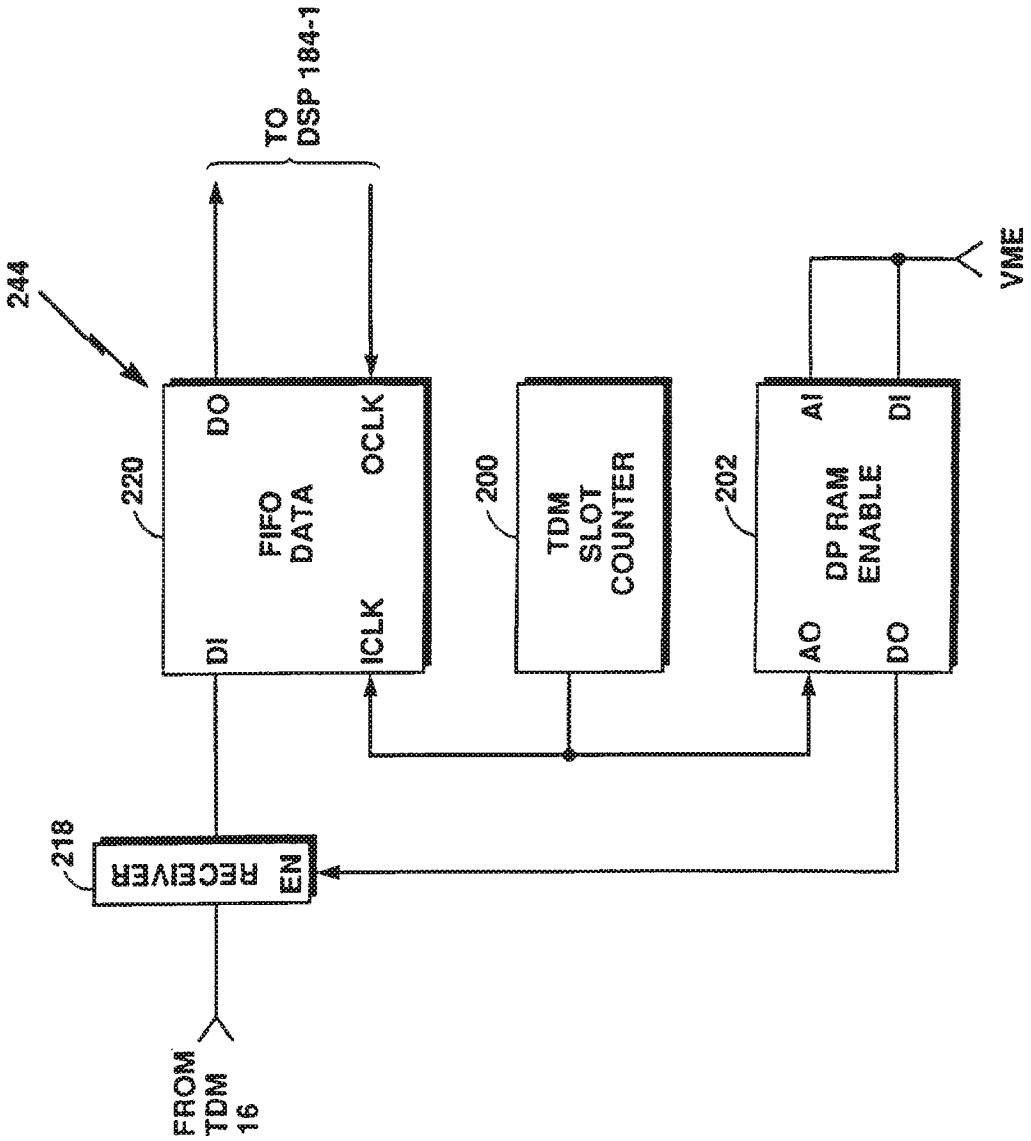


Fig. 6

Fig. 7



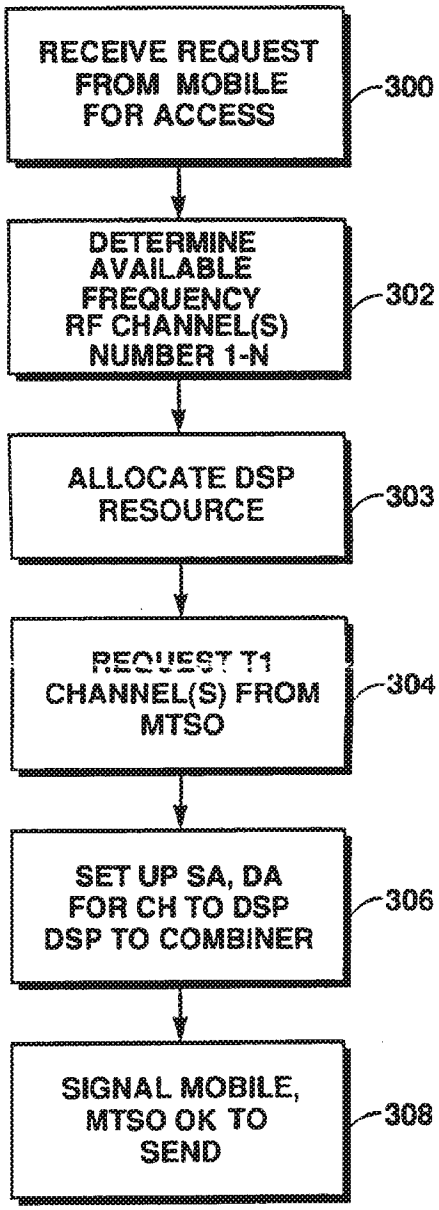


Fig. 8

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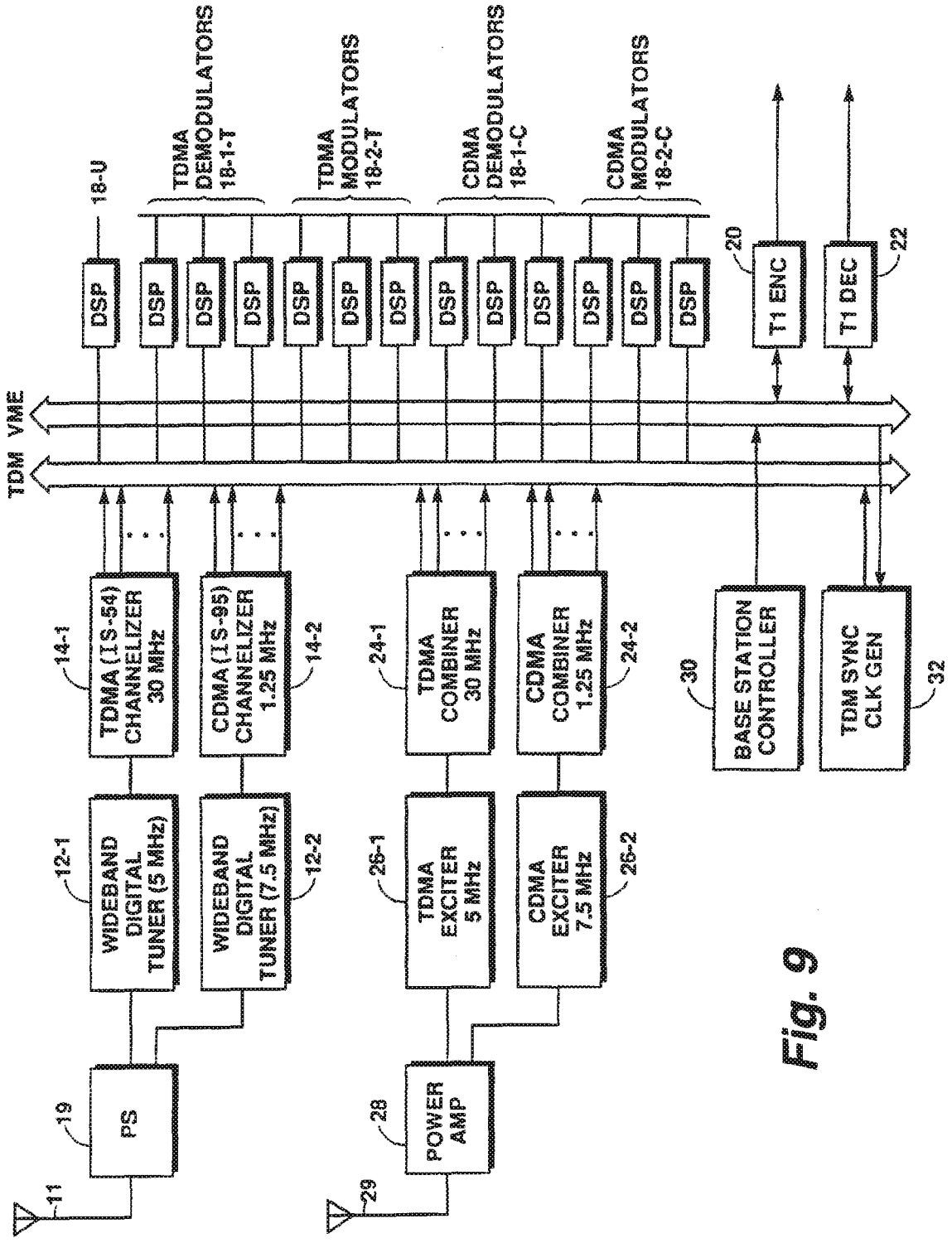

Fig. 9

INTERNATIONAL SEARCH REPORT

Interm. ...nal Application No
PCT/US 96/02200

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04Q7/30 H04B7/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04Q H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP,A,0 590 412 (SIEMENS) 6 April 1994 see claims 1-25; figures 1-4	1-16
X	EP,A,0 439 926 (ATT) 7 August 1991 see page 2, column 1, line 39 - column 2, line 43; figure 3	1-16
X	DE,A,44 23 582 (MOTOROLA) 12 January 1995 see claims 1-8; figures 1-4	1-16
X	EP,A,0 560 388 (NEC CORPORATION) 15 September 1993 see claims 1-5; figures 1-9	1-16
X	EP,A,0 605 182 (NIKI YOSHIRO) 6 July 1994 see claims 1-12	1,6-9,16

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

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2

Date of the actual completion of the international search	Date of mailing of the international search report
24 May 1996	04.07.96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Bischof, J-L

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INTERNATIONAL SEARCH REPORT

Interna...al Application No
PCT/US 96/02200

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP,A,0 507 384 (PHILIPS ELECTRONICS UK LIMITED) 7 October 1992 see page 3, line 1 - page 5, line 25; figures 1-7	1-8, 10-12, 14-16
X	EP,A,0 471 246 (MOTOROLA) 19 February 1992 see page 3, column 3, line 8 - column 4, line 26; claims 1-10; figure 1	1-8, 10-12, 14-16

2

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 96/02200

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A-590412	06-04-94	DE-A-	4232480	31-03-94
		DE-A-	4238410	19-05-94
		FI-A-	934235	29-03-94
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		JP-A-	5091079	09-04-93
		US-A-	5369637	29-11-94
EP-A-471246	19-02-92	US-A-	5111454	05-05-92

INTERNATIONAL SEARCH REPORT

information on patent family members

International Application No
PCT/US 96/02200

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-471246		AU-B- 641521	23-09-93
		AU-B- 8034991	20-02-92

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04L 1/12, 1/24, 5/14 — A3

(11) International Publication Number: **WO 97/15131**

(43) International Publication Date: 24 April 1997 (24.04.97)

(21) International Application Number: PCT/US96/16675

(22) International Filing Date: 18 October 1996 (18.10.96)

(30) Priority Data:
08/544,491 18 October 1995 (18.10.95) US

(71) Applicants: TELEFONAKTIEBOLAGET LM ERICSSON [SE/SE]; S-126 25 Stockholm (SE). ERICSSON INC. [US/US]; 7001 Development Drive, P.O. Box 13969, Research Triangle Park, NC 27709 (US).

(72) Inventor: RAITH, Alex, Krister; 805-A5 Park Ridge Road, Durham, NC 27713 (US).

(74) Agents: GRUDZIECKI, Ronald, L. et al.; Burns, Doane, Swecker & Mathis, L.L.P., P.O. Box 1404, Alexandria, VA 22313-1404 (US).

(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

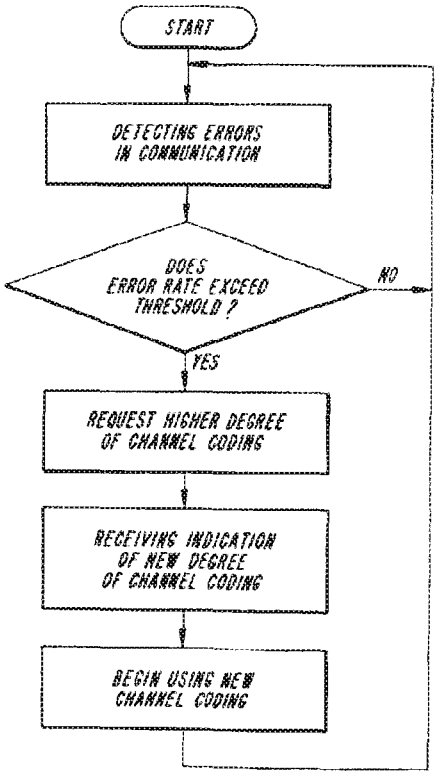
Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(88) Date of publication of the international search report:
5 June 1997 (05.06.97)

(54) Title: METHOD FOR IMPROVING THE EFFICIENCY OF TRANSMISSION IN MOBILE NETWORKS

(57) Abstract

A method for indicating a change in coding rate is disclosed so as to maintain synchronization between a communication system and a mobile station. A mobile station can request either to increase or decrease the degree of channel coding. The system can grant the request and send an indication to the mobile station indicating the new degree of coding. The indication is provided outside the field in which the coding rate is going to be changed. A modulation symbol alphabet can also be changed.



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GA	Gabon	MR	Mauritania	VN	Viet Nam

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 96/16675

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04L1/12 H04L1/24 H04L5/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 627 827 A (CSELT; PHILIPS) 7 December 1994 see abstract see page 2, line 4 - line 6 see page 2, line 48 - line 58 see page 3, line 47 - line 51 see page 3, line 56 - line 58 see page 4, line 4 - line 7 see page 4, line 24 - line 30	1-5
A	--- -/--	6-12

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

2

Date of the actual completion of the international search	Date of mailing of the international search report
15 April 1997	24.04.97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Scriven, P

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 188 271 A (OKI ELECTRIC INDUSTRY) 23 July 1986 see abstract see page 1, line 16 - line 19 see page 2, line 21 - line 27 see page 3, line 1 - line 6 see page 3, line 12 - line 24 see page 9, line 7 - line 13 see page 13, line 24 - page 14, line 15 see page 19, line 21 - page 20, line 6	1-5
A	---	6-12
X	EP 0 423 485 A (BOSCH) 24 April 1991 see column 1, line 3 - line 11 see column 1, line 52 - line 53 see column 2, line 1 - line 5 see column 2, line 18 - line 42	1-5
A	---	6-12
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A	---	6-12
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A	---	6-12
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A	---	1-5
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A	---	1-5
	-/--	

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 93 00751 A (MICROCOM SYSTEMS) 7 January 1993 see page 5, line 3 - line 7 see page 7, line 3 - line 7 see page 9, line 33 - page 10, line 1 see page 10, line 29 - page 11, line 2 see page 13, line 2 - line 6 see page 15, line 18 - line 36	6-12
A	---	1-5
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	-/--	

2

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PROCEEDINGS OF THE VEHICULAR TECHNOLOGY CONFERENCE, 25 - 28 July 1995, NEW YORK, US, pages 221-225, XP000550167 KAMIO ET AL.: "Performance of modulation-level-controlled adaptive-modulation under limited transmission delay time for land mobile communications" see abstract see page 221, right-hand column, paragraph 4 - page 222, left-hand column, paragraph 1 see figure 2	6-12
A	-----	1-5

2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 96/16675

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. Claims 1-5: Adjustment of the degree of channel coding.
2. Claims 6-12: Adjustment of the modulation symbol alphabet.

1. ☒ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searches without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 96/16675

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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INTERNATIONAL SEARCH REPORT

ormation on patent family members

Interr nal Application No
PCT/US 96/16675

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04L 1/12, H04Q 7/18 — A1

(11) International Publication Number: WO 97/24828

(43) International Publication Date: 10 July 1997 (10.07.97)

(21) International Application Number: PCT/JP96/03755

(22) International Filing Date: 24 December 1996 (24.12.96)

(30) Priority Data:
7/354309 29 December 1995 (29.12.95) JP

(71) Applicant: CASIO COMPUTER CO., LTD. [JP/JP]; 6-1, Nishi-Shinjuku 2-chome, Shinjuku-ku, Tokyo 160 (JP).

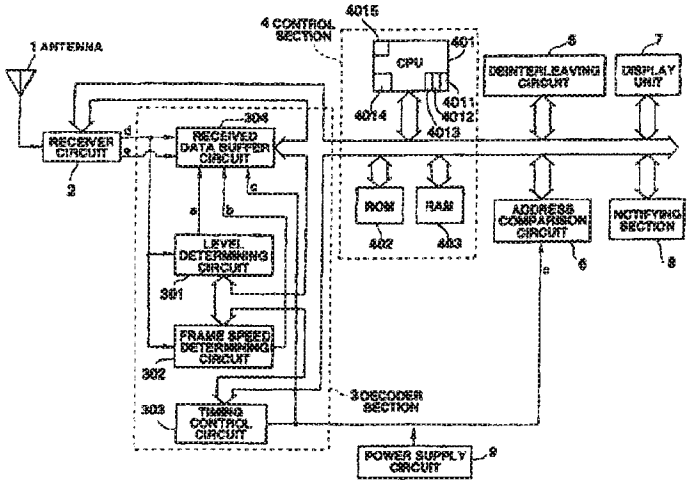
(72) Inventors: TACHIBANA, Toshiyuki; 278-102, Shimmachi, Ome-shi, Tokyo 198 (JP). SATO, Satoshi; 2-24-12, Nakamuraminami, Nerima-ku, Tokyo 176 (JP).

(74) Agents: SUZUYE, Takehiko et al.; Suzuye & Suzuye, 7-2, Kasumigaseki 3-chome, Chiyoda-ku, Tokyo 100 (JP).

(81) Designated States: AU, CA, CN, KR, MX, NO, PL, SG, Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (CH, DE, ES, FI, FR, GB, IT, NL, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: MULTI-RATE AND MULTIPLE-MODULATION FORMAT DATA RECEIVING APPARATUS AND METHOD OF DEINTERLEAVING DATA



(57) Abstract

When a frame information (F1)C2 defining the frame type in a transmission protocol format is received in a pager, data of a following interleaving portion is received. A receiving buffer circuit converts the received data from serial data into parallel data in accordance with the frame type, and a deinterleaving circuit reproduces (deinterleaves) the converted parallel data. The conversion means converts data received by one of a plurality of receiving means into parallel data corresponding to format data denoting data modulation mode and/or data transmission rate.

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D E S C R I P T I O N

MULTI-RATE AND MULTIPLE-MODULATION FORMAT DATA RECEIVING APPARATUS AND METHOD OF DEINTERLEAVING DATA

Technical Field

The present invention relates to a data receiving apparatus and a method of deinterleaving data for reproducing data transmitted by a modulation mode at a frame speed (or transmission rate) and by an interleaving mode arbitrarily selected from predetermined modulation modes, frame speeds and interleaving modes.

Background Art

Hitherto, NTT system and POCSAG system have been known as paging (wireless paging) systems.

The POCSAG system employs, for example, binary FSK (Frequency Shift Keying) method as a modulation mode and sets a frame speed to 512 bps (Bit/Second). When paging is performed, a paging service company transmits digital data, which has been FSK-modulated, to the called pager, at the rated frame speed. Thus, a service for communicating messages has been performed.

Meanwhile, the progress of the mobile communication technique made recently has resulted in the communication service charge being reduced. Thus, the mobile communication has been widely used in business, personal, and in particular, among the young, thus resulting in subscribers being increased. As a result,

addresses for the subscribers are in short and the traffic has been always congested. Thus, the conventional POCSAG system has encountered difficulty in providing service satisfactory for the subscribers.

Since the paging service has been in a great demand and the serviceable menus have been increased recently, there arise a necessity of improving the paging system. As a result, employment "RCR STD-43" in future has been decided as the next standard system.

The foregoing paging system (hereinafter called "STD-43") will briefly be described. The structure of data, which is employed in STD-43, is shown in FIG. 32. Referring to FIG. 32, symbol "A" shows the structure of data which is transmitted at a period of one hour and "B" shows one cycle of the data structure "A". Symbol "C" shows the structure of data in one frame of the cycle structure "B". Symbol "D" shows the block structure of one frame. The data structure "A" is composed of 15 cycles respectively given numbers "No. 0" to "No. 14".

The cycle structure "B" is composed of 128 frames respectively given numbers "No. 0" to "No. 127", which are transmitted at a period of four minutes. One frame has a data length of 1.875 seconds. Data in one frame of the frame structure cycle is sectioned into 8 section corresponding to the contents of data.

The eight section of the data contents is, as

indicated in the data structure "C" and the block structure "D", composed of sync structure D1 composed of, when viewed from the leading end, synchronization 1 (S1)C1, frame information (F1) C2 and synchronization 2 (S2)C3 and arranged to be transmitted at 115 ms (milliseconds); and interleaved block structure D2 composed of block information (B1) C4, address field (AF)C5, vector field (VF)C6, message field (MF)C7 and idle blocks (IB)C8 and arranged to be transmitted at a frame speed of 160 ms for each block so that 11 blocks are transmitted.

In the synchronizing signal section D, the synchronization 1 (S1)C1 is composed of 112-bit 2-level FM data (binary-FSK-modulated data, in detail) at 1600 bps, the synchronization 1 (S1)C1 containing frame pattern data including information of frame receiving timing, timing for receiving 1600 bps symbol data and the transmitted type selected from the following four frame types/rates with which the interleaving block portion D1 is interleaved/transmitted:

1. 2-Level FM 1600bps (Binary FSK Modulation/1600 bps)

2. 2-Level FM 3200bps (Binary FSK Modulation/3200 bps)

3. 4-Level FM 3200bps (Quadruple FSK Modulation/3200 bps)

4. 4-Level FM 6400bps (Quadruple FSK

Modulation/6400 bps)

The frame information (F1) C2 is composed of 32-bit 2-level FM data at 1600 bps and includes data (four bits) of cycle number of the cycle of the data structure "A" to which this frame belongs, data (7 bits) of the frame number of the cycle to which this frame belongs, and information of indication of plural transmitted operations and the number of the transmitted operations.

The interleaved block structure D2 formed of the synchronization 2 (S2)C3 and the block information (B1) C4 to the idle blocks (IB)C8 is data which is transmitted by means of the frame type specified by the synchronization 1 (S1)C1. The synchronization 2 (S2)C3 is a block for supplying timing information to the interleaved block structure D2 transmitted by the modulation method and the frame speed specified by the synchronization 1 (S1)C1 to enable the called pager to fetch the interleaved block structure D2.

The block information (BI)C4 is data disposed in block #0 of the interleaved block structure D2 and composed of one word. The block information (BI)C4 includes block information 1 for storing information of the word number (2 bits) which is used as the start point of address field (AF)C5 and the end point of the present field, to be described later, the word (6 bits) which is used as the start point of vector field (VF)C6 and the like, and block information items 2, 3 and 4 so

that ID of the simulcast system and, if the frame number is zero, information of the actual time, time zone and system message are stored.

The address field (AF)C5 is a field for storing address data of the called pager, the data to be stored being short address (32 bits) or long address (64 bits).

The vector filed (VF)C6 and the address field (AF)C5 form a pair and the vector field (VF)C6 is a field for storing the word at which the own message data is started in a message field (MF)C7 to be described later, the word length of own message data (hereinafter simply referred to message length) and information of the data format of the own message data.

The message field (MF)C7 is a field for storing message data corresponding to information specified by the vector field (VF)C6. The idle blocks (IB)C8 is an unused block to which a pattern composed of "1" or "0" is set.

The signal format shown in FIG. 32 is, in parallel, interleaved/transmitted in a time sequential manner in independent four phases "a", "b", "c" and "d". That is, if STD-43 is employed, the paging service company uses any one of the above-mentioned four phases or two to four phases to enable data in one frame having different contents to be multiplexed so as to be transmitted simultaneously.

In STD-43, the relationship between the phases of

the frame speeds is regulated as follows:

1600 bps: any one of phases "a", "b", "c" and "d" is used (multiplex degree: 1)

3200 bps: a pair of phases "a" and "c" or a pair of "b" and "d" is used (multiplex degree: 2)

6400 bps: all of the phases "a", "b", "c" and "d" are used (multiplex degree: 4)

The block structure of the interleaved block structure D2 will now be described. Referring to FIG. 32, one block is structured such that the frame speed is 160 ms. One block stores, in parallel, 8 rows (one row is called one word) for one phase, each row being composed of the following 32 bits:

Information (Information Bit): 21 bits

Parity(Check Bit): 10 bits

CK(Even-Number Parity Bit): 1 bit

The number of bits of data in one block is different depending upon the frame speed. The relationship between the frame speeds and the number of bits of data in one block is as follows:

1600 bps: 1 phase × 8 words × 32 bits = 256 bits

3200 bps: 2 phases × 8 words × 32 bits = 512 bits

6400 bps: 4 phases × 8 words × 32 bits = 1024 bits

The structure of bit data in one block at each frame speed will now be described with reference to FIG. 33 to 35. FIG. 33 shows the structure of bit data in one block at the frame speed of 1600 bps, FIG. 34

shows the structure of bit data in one block at the frame speed of 3200 bps and FIG. 35 shows the structure of bit data in one block at the frame speed of 6400 bps.

In the case where the interleaved block structure D2 is transmitted at 1600 bps, the structure of bit data in one block shown in FIG. 33 is employed. The transmitted order of bit data is, in a direction indicated by an arrow β shown in FIG. 33, as W(word)0a1, W1a1, W2a1, ..., W5a32, W6a32 and W7a32.

In the case where transmitted at 3200 bps is performed, the structure of bit data in one block as shown in FIG. 34 is employed. The transmitted order of bit data is, in a direction indicated by an arrow β shown in FIG. 34, as W0a1, W0c1, W1a1, ..., W6c32, W7a32 and W7c32 (in the case of 2-level FM), as W0a1 and W0c1, W1a1 and W1c1, W2a1 and W2c1, ...,W6a32 and W6c32, W7a32 and W7c32 (in the case of 4-level FM). In the case where transmitted at 6400 bps is performed, the structure of bit data in one block as shown in FIG. 35 is employed. The transmitted order of bit data is, in a direction indicated by an arrow β shown in FIG. 35, as W0a1 and W0b1, W0c1 and W0d1, W1a1 and W1b1, W1c1 and W1d1, ..., W6a32 and W6b32, W6c32 and W6d32, W7a32 and W7b32, W7c32 and W7d32 (in the case of 4-level FM).

As described above, STD-43 involves the number of bits of data in one block which is received at each frame speed and the interleaving mode being different.

Also in the case of the frame speed of 3200 bps, the structure of bit data becomes different depending upon whether the modulation mode is 2-level FM or 4-level FM.

When a paging service company employs paging system STD-43, one frame type is selected from four types of the frame types/rates in the synchronization 1 (S1)C1 of the sync structure D1. Thus, the number of bits of data in one frame which is transmitted to the called pager can arbitrarily be changed.

Therefore, if the called pager uniformly receives, amplifies and digitizes data, which has been transmitted in the wireless manner, to simply convert 2-level FM serial data into parallel data as has been performed by the conventional POCSAG system, meaningless serial data is unintentionally transmitted. Thus, a data reproducing method adaptable to STD-43 and capable of rearranging bit data to correspond to the received frame type must be provided for the pager.

The following methods of reproducing received data to be provided for the pager have been suggested:

(1) A method in which plural types of hardware units (decoders) adaptable to the respective frame speeds and the multiplex degree are mounted on the pager; any one of the mounted hardware unit is selected so that data transmitted at any one of the frame speeds is received; and bit data of the interleaved block structure D2 of above data is reproduced in accordance

with the multiplex degree and by the selected deinterleaving circuit.

(2) One type of hardware is mounted on a pager; and software for performing control to rearrange bit data in the interleaved block structure D2 in accordance with the frame type of the received data is installed so that received data is reproducing.

In the case where method (1) is employed, the pager is provided with a plurality of S/P conversion circuits for converting the serial data to the parallel data in accordance with the frame type of received data; and a rearranging circuit for rearranging the parallel data in order to separate data into each phase.

In the case where method (2) is employed, one S/P conversion circuit and the rearranging circuit are provided which are controlled by software. However, in the above-mentioned case (1), the number of hardware units which receive and reproduce data and which must be provided for the pager increases. What is even worse, since the structure of each of the circuits has a complicated structure, the size of the reception processing circuit after it has been mounted cannot be reduced. In the case of (2), the software must perform a heavier task and therefore the structure of the system becomes too complicated.

Disclosure of the Invention

Accordingly, the present invention is achieved to

solve expected problems to arise for a pager for receiving and reproducing data when STD-43 standard is employed and, thus, it is an object of the present invention to provide a data receiving apparatus and a method of reproducing received data which can keep the balance between hardware and software for use to receive and reproduce data and reduce the size of the hardware and the load which must be borne by the software.

Another object of the present invention is to provide a data receiving apparatus and a method of reproducing received data capable of adapting the above-mentioned data transmission method, keeping the balance of load distributed to hardware and software, and reducing the size of the circuit and load, which must be borne by a CPU.

In order to achieve the above-mentioned objects, according to the present invention, there is provided a data receiving apparatus comprising:

receiving means for receiving data;

plural reproducing means capable of reproducing received data having a format which can be recognized by said data receiving apparatus;

format data receiving means for receiving format data; and

selection means for selecting one of said plural reproducing means in accordance with the format data received by said format data receiving means.

Therefore, the load distributed to the hardware and the software can be balanced so that the size of the circuit and the load of the CPU are reduced.

The format data denotes a frame speed and the reproducing means is selected in accordance with the received frame speed. The reproducing process rate of the reproducing means is controlled in accordance with the frame speed received by the format data receiving means.

The format data denotes a modulation mode and the reproducing means is selected in accordance with the received modulation method. The received data is converted to parallel data in accordance with the modulation method.

The format data denotes a frame speed and a modulation mode and the reproducing means is selected in accordance with the received frame speed and the modulation method. The reproducing process rate of the reproducing means is controlled in accordance with the frame speed received by the format data receiving means. The received data is converted to parallel data in accordance with the modulation method.

The data reproducing process rate of the reproducing means is controlled in accordance with a data interleaving mode. Received data is converted into parallel data in accordance with the data interleaving mode.

Since the received data is converted into parallel data in accordance with the data interleaving mode, the load distributed to hardware and software can be balanced, and thus the size of the circuit and load, which must be borne by a CPU, can be reduced.

Plural registers used for converting the received data into parallel data are provided.

When parallel data is divided into predetermined units so as to be sequentially stored, stored parallel data are read sequentially in the storing order so as to be supplied to the selected reproducing means, and reproduced parallel data is stored in the storage position from which the same has been read, the operation required to transfer data in the data transmission process is performed by, for example, a DMA circuit in place of the CPU. Thus, the load of the CPU can furthermore be reduced.

When data which is reproduced in one operation by the reproducing means selected by the selection means is stored in data storage means, when reproducing timing of the reproducing means selected by the selection means is detected, parallel data is sequentially transmitted from the data storage means to the reproducing means and simultaneously parallel data transmitted from the conversion means is sequentially stored by the data storage means, the operation required to transmit and receive data in the data transmitted process is

performed by, for example, a DMA circuit in place of the CPU. Thus, the load of the CPU can furthermore be reduced.

The format data received by the format data receiving means is stored until the format data is received next.

An ID code of paging of the data receiving apparatus is stored, if the ID code is detected in reproduced data while continuing the reproducing operation of the reproducing means, the detected ID code and the stored ID code are compared with each other. If the ID codes do not coincide with each other, the reproducing operation of the reproducing means is interrupted.

By providing an interface, the data receiving operation of the data receiving apparatus is controlled in accordance with control data supplied from a connected external device through the interface. Therefore, even if data which cannot be processed by only the data receiving apparatus, it can be processed under control of the connected external device.

According to another aspect of the present invention, there is provided a method of deinterleaving data in which data received by plural rearranging circuits are reproduced into data comprising the following steps of:

receiving format data; and

selecting one of said plural rearranging circuits in accordance with received format data.

According to the above method, a rearranging circuit is selected from the plural rearranging circuits in accordance with information of the data format if information (synchronization 1(S1)C1) of the data format is received. Thus, received data is reproduced by the selected rearranging circuit.

Therefore, the load of the process distributed to the hardware and the software can be balanced. Thus, the size of the circuit and the load of the CPU can be reduced.

Brief Description of the Drawings

FIG. 1 is a block diagram showing a circuit of a pager which is a first embodiment of a data receiving apparatus according to the present invention;

FIG. 2 is a circuit diagram showing an example of the internal structure of the received data buffer circuit 304 shown in FIG. 1;

FIG. 3 shows the correspondence between input to registers 3042 (Ra to Rh) and output from latches 3043 (La to Lh) with respect to 64-bit data supplied to the received data buffer circuit 304 shown in FIG. 2;

FIG. 4 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data (phase "a") in a range α for one block, the frame type

of which is 1600 bps (2-level FM) and which is transmitted at a frame speed of 1600 bps as shown in FIG. 32 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 5 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data (a pair of phases "a" and "c") in a range "α 1", which is transmitted at the first time, in the range α for one block, the frame type of which is 3200 bps (2-level FM) and which is transmitted at a frame speed of 3200 bps as shown in FIG. 34 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 6 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data (a pair of phases "a" and "c") in a range "α 2" which is transmitted at the second time, in the range α for one block, the frame type of which is 3200 bps (2-level FM) and which is transmitted at a frame speed of 3200 bps as shown in FIG. 34 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 7 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data (a pair of phases "a" and "c") in a range "α 1", which is transmitted at the first time, in the range α for one

block, the frame type of which is 3200 bps (4-level FM) and which is transmitted at a frame speed of 3200 bps as shown in FIG. 34 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 8 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data (a pair of phases "a" and "c") in a range "α 2", which is transmitted at the second time, in the range α for one block, the frame type of which is 3200 bps (4-level FM) and which is transmitted at a frame speed of 3200 bps as shown in FIG. 34 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 9 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data in a range "α 1", which is transmitted at the first time, in the range α for one block, the frame type of which is 6400 bps (4-level FM) and which is transmitted at a frame speed of 6400 bps as shown in FIG. 35 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 10 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data in a range "α 2", which is transmitted at the second time, in the range α for one block, the frame type of which is 6400 bps (4-level FM) and which is transmitted at

a frame speed of 6400 bps as shown in FIG. 35 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 11 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data in a range "α 3", which is transmitted at the third time, in the range α for one block, the frame type of which is 6400 bps (4-level FM) and which is transmitted at a frame speed of 6400 bps as shown in FIG. 35 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 12 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data in a range "α 4", which is transmitted at the fourth time, in the range α for one block, the frame type of which is 6400 bps (4-level FM) and which is transmitted at a frame speed of 6400 bps as shown in FIG. 35 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 13 is a diagram showing an example of the structure of memory areas of the RAM 403 shown in FIG. 1;

FIG. 14 is a block diagram showing an example of the structure of the deinterleaving circuit 5 shown in FIG. 1;

FIG. 15 is a diagram showing a rearranging operation which is performed by a rearranging

circuit 502;

FIG. 16 is a diagram showing the rearranging operation which is performed by a rearranging circuit 503;

FIG. 17 a diagram showing the rearranging operation which is performed by a rearranging circuit 504;

FIG. 18 is a circuit diagram showing an example of the internal structure of the address comparison circuit 6 shown in FIG. 1;

FIGS. 19A and 19B are a flow chart showing a data receiving operation which is performed by the pager according to the first embodiment of the present invention;

FIG. 20 is a flow chart showing the data receiving operation which is performed by the pager according to the first embodiment of the present invention;

FIGS. 21A and 21B are a flow chart showing the data receiving operation which is performed by the pager according to the first embodiment of the present invention;

FIG. 22 is a flow chart showing the data receiving operation which is performed by the pager according to the first embodiment of the present invention;

FIG. 23 is a flow chart showing a reproducing operation which is performed by the deinterleaving circuit 5 of the pager according to the first embodiment of the present invention;

FIG. 24 is a block diagram showing a circuit of a pager according to a second embodiment of the data receiving apparatus according to the present invention;

FIG. 25 is a diagram showing an example of the structure of memory areas in the RAM 404 shown in FIG. 24;

FIGS. 26A and 26B are a flow chart showing a data receiving operation which is performed by the pager according to the second embodiment of the present invention;

FIG. 27 is a flow chart showing the data receiving operation which is performed by the pager according to the second embodiment of the present invention;

FIG. 28 is a flow chart showing the data receiving operation which is performed by the pager according to the second embodiment of the present invention;

FIG. 29 is a flow chart showing the data receiving operation which is performed by the pager according to the second embodiment of the present invention;

FIG. 30 is a timing chart showing a data transmitting and receiving operations which is performed by a DMA circuit 11 when the data receiving operation is performed;

FIG. 31 is a block diagram showing the structure of a circuit of a modification of the second embodiment of the present invention;

FIG. 32 is a diagram showing an example of the

structure of transmitted data which is employed by pager system "RCR STD-43";

FIG. 33 is a diagram showing the structure of one block of an interleaved block structure D2 when the frame speed is 1600 bps (phase "a");

FIG. 34 is a diagram showing the structure of one block of an interleaved block structure D2 when the frame speed is 3200 bps (a pair of phases "a" and "c"); and

FIG. 35 is a diagram showing the structure of one block of the interleaved block structure D2 when the frame speed is 6400 bps.

Best Mode of Carrying Out the Invention

A preferred embodiment of a data receiving apparatus and a method of reproducing received data according to the present invention will now be described with reference to the accompanying drawings. Note that the embodiments employ the data structure C and block structure D shown in FIG. 32.

(First Embodiment)

FIG. 1 is a block diagram showing the structures of circuits in a pager which is a first embodiment of a data receiving apparatus according to the present invention. The pager comprises an antenna 1, a receiver circuit 2, a decoder section 3, a control section 4, a deinterleaving circuit 5, an address comparison circuit 6, a display unit 7, a notifying section 8 and a power

supply circuit 9.

The antenna 1 receives data transmitted from a transmitting station of, for example, a pager service company in the format shown in FIG. 32 to supply the received data to the receiver circuit 2.

The receiver circuit 2 is connected to the decoder section 3 and arranged to be operated in response to a control signal supplied from the decoder section 3 so as to demodulate and wave-detect the received data. The receiver circuit 2 fetches the synchronization 1 (S1)C1 to select and output serial bit data in accordance with the 2-level FM or 4-level FM modulation method. That is, when the 2-level FM modulation is performed, only "d" is output. When 4-level FM modulation is performed, MSB signal of 4-level FM bit data is output to "d" and LSB signal is output to "e".

Data included in the frame pattern data obtained by fetching the synchronization 1 (S1)C1 and relating to the modulation method, is supplied to a level determining circuit 301 through the output "d", while data relating to the frame speed is supplied to a frame speed determining circuit 302. The decoder section 3 determines the frame pattern of the interleaved block structure D2 following the synchronization 2 (S2)C3 in response to a line selection signal "a" output from the level determining circuit 301, a shift clock signal "b" output from the frame speed determining circuit 302 and

a data trigger "c" output from the timing control circuit 303. Moreover, the decoder section 3 converts the detected digital data into 8-bit parallel data in accordance with the modulation method so as to supply the obtained 8-bit parallel data to a bus line "B".

The decoder section 3 includes the level determining circuit 301, the frame speed determining circuit 302, a timing control circuit 303 and a received data buffer circuit 304. Each of the level determining circuit 301 and frame speed determining circuit 302 has a buffer memory (not shown). The buffer memories store control data output from a CPU 401 of the control section 4 when initialization is performed, data included in the received frame type data which relates to the modulation method and data relating to the frame speed. Moreover, the buffer memories store control data output from the CPU 401 of the control section 4.

The level determining circuit 301 receives serial bit data "d" (data of the synchronization 1 (S1)C1) output from the receiver circuit 2 to determine the modulation method of the received data so as to generate the line selection signal "a".

The frame speed determining circuit 302 receives the serial data "d" (data of the synchronization 1 (S1)C1) output from the receiver circuit 2 so as to determine the frame type of the received data. Specifically, the frame speed determining circuit 302

determines the frame type among the following four types:

1. 1600bps 2-Level FM (Binary FSK Modulation/1600 bps)

2. 3200bps 2-Level FM (Binary FSK modulation/3200 bps)

3. 3200bps 4-Level FM (Quadruple FSK modulation/3200 bps)

4. 6400bps 4-Level FM (Quadruple FSK modulation/6400 bps)

After the frame speed determining circuit 302 has determined the frame type, it generates the shift clock signal "b".

The timing control circuit 303 has a buffer for temporarily storing timing control information obtained from the CPU 401 when the synchronizing signal portion D1 has been received. Thus, the timing control circuit 303 controls bit-synchronization and the frame-synchronization of the decoder section 3. Moreover, the timing control circuit 303 generates the data trigger "c" for controlling an output timing of 8-bit parallel data from the received data buffer circuit 304.

The received data buffer circuit 304 converts serial bit data (outputs "d" and "e") output from the receiver circuit 2 into 8-bit parallel data so as to output the 8-bit parallel data to the bus line "B". The received data buffer circuit 304 converts the above bit

data in unit of 64 bits in accordance with the line selection signal "a" output from the level determining circuit 301, the shift clock signal "b" output from the frame speed determining circuit 302 and the data trigger "c" output from the timing control circuit 303 so as to sequentially output 8-bit parallel data.

The control section 4 includes a CPU 401, a ROM 402 and a RAM 403 and controls the overall operation of the pager in accordance with a control program stored in the ROM 402.

The CPU 401 has a buffer memory 4011 for temporarily storing the frame pattern data read from, for example, the synchronization 1 (S1)C1, a buffer memory 4012 for temporarily storing data (cycle number, frame number and number of plural output operations) read from the frame information (F1)C2, a buffer memory 4013 for storing block information (BI)C4 and data (the start word of the address field (AF)C4, vector field (VF)C5,and own message data in the message field (MF)C6, and the message length of own message data in the message field (MF)C6) read from the vector field (VF) C5, a buffer memory 4014 for storing reproduced data in unit of one block so as to correct errors and a clock generator 4015 for generating clocks for use to adjust the timing of the receiving process and the like.

The CPU 401 controls circuit sections connected with each data by data and clocks contained in the above

one frame.

The ROM 402 stores various programs for operating the CPU 401 and ID information for storing information of the frequency bands which must be received by the own pager, frame data and address data, which are ID codes of the own pager, and phase data indicating the phase in which the ID codes are stored.

As shown in FIG. 13, the RAM 403 has a work area WA for use in an operation of the CPU 401, a data reading memory area RDA for use in reproducing the received data and a memory area MMA for use in a process for storing the received message data.

The memory area RDA is a memory area for temporarily storing 8-bit parallel data output from the decoder section 3 before it has been output to a deinterleaving circuit 5 to be described later. When the output timing to the deinterleaving circuit 5 has been detected under control of the CPU 401, the number of bits of data (16 bits if the frame speed is 3200 bps and 32 bits if the frame speed is 6400 bps) which can be reproduced is sequentially output to the deinterleaving circuit 5.

The deinterleaving circuit 5, for each phase, reproduces 16-bit data of 3200 bps (2-level FM), 16-bit data of 3200 bps (4-level FM) and 32-bit data of 6400 bps (4-level FM) in accordance with the corresponding frame pattern so as to output reproduced

data to the bus line "B".

The address comparison circuit 6 operates in accordance with the data trigger "c" output from the timing control circuit 303 and which compares and collates whether address data, which is included in the reproduced address field (AF)C5, coincides with address data of the own pager.

The display unit 7 is a circuit section formed by, for example, a liquid crystal panel, a display buffer or a driver so as to display information, such as a message, on a liquid crystal panel.

The notifying section 8 is composed of notifying means including, for example, an LED (Light Emission Diode) which is turned on or allowed to flicker to notify the receipt of message, a speaker which produces sound for notifying the same, a vibrator which is vibrated to notify the same.

The power supply circuit 9 supplies electric power to the overall circuits of the pager when a power switch (not shown) is switched on.

The decoder section 3 will now be described in detail. FIG. 2 is a circuit diagram showing the internal structure of the received data buffer circuit 304 in the decoder section 3. The received data buffer circuit 304 shown in FIG. 2 has eight registers 3042 consisting of registers Ra to Rh for, in unit of 8-bit from B0 to B7, sequentially storing serial bit data

output from the receiver circuit 2 through the outputs "d" and "e"; eight latches 3043 consisting of La to Lh respectively corresponding to the foregoing registers 3042; and a line selection circuit 3044.

A principle of the operation of the decoder section 3 to convert serial bit data to 64-bit data in 8-bit parallel will now be described. FIG. 3 shows correspondence between the inputs to the registers 3042 (Ra to Rh) and the outputs from the latches 3043 (La to Lh) with respect to the 64-bit data input to the received data buffer circuit 304 in one input operation.

As can be understood from table shown in FIG. 3, serial bit data supplied to B7 of the register Rh of the registers 3042 shown in FIG. 2 is, as 8-bit parallel data, output to D7 of the latch Lh of the latches 3043. Serial bit data supplied to B4 of the register Rd of the registers 3042 is, as 8-bit parallel data, output to D3 of the latch Le of the latches 3043.

FIGS. 4 to 12 show correspondence between the inputs to the registers 3042 (Ra to Rh) and the outputs from the latches 3043 (La to Lh) with respect to bit data in a range α among bit data in one block shown in FIGS. 32 to 35 in cases of frame types/rates 1600 bps (2-level FM: when phase "a" has been received), 3200 bps (2-level FM : when the pair of phases "a" and "c" has been received), 3200 bps (4-level FM : when the pair of phases "a" and "c" has been received) and 6400 bps

(4-level).

In the received data buffer circuit 304, the shift clock signal "b" output from the frame speed determining circuit 302 is supplied to each of the registers 3042, while the line selection signal "a" output from the level determining circuit 301 is supplied to the received data buffer circuit 304. The data trigger "c" output from the timing control circuit 303 is supplied to each of the latches 3043.

When 2-level FM bit data has been output from the receiver circuit 2, the registers 3042 (Ra to Rh), which are input registers, fetch 64-bit data through the output "d". When 4-level FM bit data has been output from the receiver circuit 2, the registers 3042 fetch MSB (upper bits) of 64-bit data through the output "d" and LSB (lower bits) through the output "e".

Thus-fetched bit data is controlled by the line selection signal "a" output from the level determining circuit 301, the shift clock signal "b" output from the frame speed determining circuit 302 and the data trigger "c" output from the timing control circuit 303 as follows so that bit data is output as 8-bit parallel data corresponding to the respective frame types/rates.

1. In a case where the frame type is 1600 bps (2-level FM: when phase "a" has been received"):

When bit data, the frame type of which is 1600 bps (2-level FM), has been fetched, the bit data

sequentially output from the receiver circuit 2 through the output "d" as W(word)0a1, W1a1, W2a1, W3a1, ..., in a direction indicated by an arrow β shown in FIG. 33 is, as shown in FIG. 4, fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rh) in the vertical directional order as W(word)0a1, W1a1, W2a1, W3a1, ..., W5a8, W6a8 and W7a8. When the data trigger "c" has been supplied, 64 bits are, in unit of 8-bit, output to the bus line B through D0 to D7 of the latches 3043 (La to Lh).

Since 8-bit parallel data of this frame type has been received in a single phase, the process for reproducing data is completed at this time. Thus, data is, as it is, output to the buffer memory 4014 through the bus line "B". Then, the CPU 401 performs an error correction process.

Moreover, since 8 bits × 8 columns, that is, 8-byte data, output from the received data buffer circuit 304 in one output operation uses only one phase, bit data in one block is converted into 8-bit parallel data for one block by performing the foregoing operation four times for each 64 bits in the case shown in FIG. 32.

2. In a case where the frame type is 3200 bps (2-level FM: when the pair of phases "a" and "c" has been received):

In the case where the frame type is 3200 bps (2-level FM), bit data in the phases "a" and "c" is

multiplexed and fetched. Therefore, paralleled data is allowed to pass through the RDA of the RAM 403, and then subjected to the so-called data reproducing process in the deinterleaving circuit 5 so that the received data is separated for each phase. Then, reproduced data is, through the bus line "B", stored in the buffer memory 4014, and then subjected to the error correction process in the CPU 401.

As for a portion in the range α which is indicated by α 1, bit data sequentially output from the receiver circuit 2 through the output "d" as W0a1, W0c1, W1a1, ..., in a direction indicated by an arrow β shown in FIG. 34 is, as shown in FIG. 5, fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rh) in the vertical directional order as W0a1, W0c1, W1a1, ..., W6c4, W7a4 and W7c4. When the data trigger "c" has been supplied, 64 bits are, in unit of 8-bit, output to the bus line "B" through D0 to D7 of the latches 3043 (La to Lh).

As for a portion in the range α which is indicated by α 2, bit data sequentially output from the receiver circuit 2 through the output "d" as W0a5, W0c5, W1a5, ..., in a direction indicated by an arrow β shown in FIG. 34 is, as shown in FIG. 6, fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rh) in the vertical directional order as W0a5, W0c5, W1a5, ..., W6c8, W7a8 and W7c8. When the data trigger "c" has been

supplied, 64 bits are, in unit of 8-bit, output to the bus line "B" through D0 to D7 of the latches 3043 (La to Lh).

3. In a case where the frame type is 3200 bps (4-level FM: when the pair of phases "a" and "c" has been received):

In the case where the frame type is 3200 bps (4-level FM), bit data in the phases "a" and "c" is multiplexed and fetched. Therefore, paralleled data is allowed to pass through the RDA of the RAM 403, and then subjected to the so-called data reproducing process in the deinterleaving circuit 5 so that received data is separated for each phase. Then, reproduced data is, through the bus line "B", stored in the buffer memory 4014, and then subjected to the error correction process in the CPU 401.

In this case, each one bit included in the phase "a" and the phase "c" is taken so that 2 bits (one symbol) are obtained. Therefore, serial bit data is supplied in such a manner that one bit data in the phase "a" and that in the phase "c", respectively are, as MSB and LSB, supplied in parallel to the received data buffer circuit 304 through the outputs d and e of the receiver circuit 2.

Therefore, data in the LSB of one symbol data is stored in the front portion from Ra to Rd of the registers 3042, while data in the MSB of the same is

stored in the rear portion from Re to Rh.

As for a portion in the range α which is indicated by α 1, bit data in the MSB sequentially output from the receiver circuit 2 through the output "d" as W0a1, W1a1, W2a1, ..., in a direction indicated by an arrow β shown in FIG.34 is, as shown in FIG. 7, fetched by B0 of the register 3042 (Re) to B7 of the register 3042 (Rh) in the vertical directional order as W0a1, W1a1, W2a1, ..., W5a4, W6a4 and W7a4. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D4 to D7 of the latches 3043 (La to Lh).

Simultaneously, bit data in the LSB sequentially output from the receiver circuit 2 through the output "e" as W0c1, W1c1, W2c1, ..., in a direction indicated by an arrow β shown in FIG. 34 is, as shown in FIG. 7, fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rd) in the vertical directional order as W0c1, W1c1, W2c1, ..., W5c4, W6c4 and W7c4. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D0 to D3 of the latches 3043 (La to Lh).

As for a portion in the range α which is indicated by α 2, bit data in the MSB sequentially output from the receiver circuit 2 through the output "d" as W0a5, W0c5, W1a5, ,..., in a direction indicated by an arrow β shown in FIG.34 is, as shown in FIG. 8, fetched by B0 of

the register 3042 (Re) to B7 of the register 3042 (Rh) in the vertical directional order as W0a5, W1a5, W2a5, ..., W5a8, W6a8 and W7a8. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D4 to D7 of the latches 3043 (La to Lh).

Simultaneously, bit data in the LSB sequentially output from the receiver circuit 2 through the output "e" as W0c5, W1c5, W2c5, ..., in a direction indicated by an arrow β shown in FIG. 34 is , as shown in FIG. 8, fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rd) in the vertical directional order as W0c5, W1c5, W2c5, ..., W5c8, W6c8 and W7c8. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D0 to D3 of the latches 3043 (La to Lh).

Since data of 8 bits × 8 columns, that is, 8-byte data, which is output from the received data buffer circuit 304 in one output operation uses the phases "a" and "c", bit data for one block is converted into 8-bit parallel data for one block by performing the foregoing operations by eight times for each 64-bit data as shown in FIG. 34.

4. In a case where the frame type is 6400 bps (4-level FM):

In the case where the frame type is 6400 bps (4-level FM), all of the phase "a", phase "b", phase "c"

and phase "d" are multiplexed and fetched. Therefore, paralleled data is allowed to pass through the RDA of the RAM 403, and then subjected to the so-called data reproducing process in the deinterleaving circuit 5 so that received data is separated for each phase. Then, reproduced data is, through the bus line "B", stored in the buffer memory 4014, and then subjected to the error correction process in the CPU 401.

In the case of 6400 bps (4-level FM), each one bit included in the phase "a" and the phase "b" is taken so that 2 bits (one symbol) are obtained. Moreover, each one bit included in the phase "c" and the phase "d" is taken so that 2 bits (one symbol) are obtained. Therefore, serial bit data is supplied in such a manner that one bit data in the phase "a" and that in the phase "c", are, MSB, and that in the phase "b" and that in the phase "d" are, as LSB, supplied through the outputs "d" and "e" of the receiver circuit 2.

Therefore, data in the LSB of one symbol data is stored in the front portion from Ra to Rd of the registers 3042, while data in the MSB of the same is stored in the rear portion from Re to Rh.

As for a portion in the range α which is indicated by α 1, bit data in the MSB sequentially output from the receiver circuit 2 through the output "d" as W0a1, W0c1, W1a1, ..., in a direction indicated by an arrow β shown in FIG. 35, is, as shown in FIG. 9, fetched by B0 of

the register 3042 (Re) to B7 of the register 3042 (Rh) in the vertical directional order as W0a1, W0c1, W1a1, ..., W6c2, W7a2 and W7c2. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D4 to D7 of the latches 3043 (La to Lh).

Simultaneously, bit data in the LSB sequentially output from the receiver circuit 2 through the output "e" as W0b1, W0d1, W1b1, ..., in a direction indicated by an arrow β shown in FIG. 35 is fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rd) in the vertical directional order as W0b1, W0d1, W1b1, ..., W6d2, W7b2 and W7d2. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D0 to D3 of the latches 3043 (La to Lh).

As for a portion in the range α which is indicated by α 2, bit data in the MSB sequentially output from the receiver circuit 2 through the output "d" as W0a3, W0c3, W1a3, ..., in a direction indicated by an arrow β shown in FIG. . 35, is, as shown in FIG. 10, fetched by B0 of the register 3042 (Re) to B7 of the register 3042 (Rh) in the vertical directional order as W0a3, W0c3, W1a3, ..., W6c4, W7a4 and W7c4. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D4 to D7 of the latches 3043 (La to Lh).

Simultaneously, bit data in the LSB sequentially output from the receiver circuit 2 through the output "e" as W0b3, W0d3, W1b3, ..., in a direction indicated by an arrow β shown in FIG. 35 is fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rd) in the vertical directional order as W0b3, W0d3, W1b3, ..., W6d4, W7b4 and W7d4. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D0 to D3 of the latches 3043 (La to Lh).

As for a portion in the range α which is indicated by α 3, bit data in the MSB sequentially output from the receiver circuit 2 through the output "d" as W0a5, W0c5, W1a5, ..., in a direction indicated by an arrow β shown in FIG. 35, is, as shown in FIG. 11, fetched by B0 of the register 3042 (Re) to B7 of the register 3042 (Rh) in the vertical directional order as W0a5, W0c5, W1a5, ..., W6c6, W7a6 and W7ct. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D4 to D7 of the latches 3043 (La to Lh).

Simultaneously, bit data in the LSB sequentially output from the receiver circuit 2 through the output "e" as W0b5, W0d5, W1b5, ..., in a direction indicated by an arrow β shown in FIG. 35 is fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rd) in the vertical directional order as W0b5, W0d5, W1b5, ...,

W6d6, W7b6 and W7d6. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D0 to D3 of the latches 3043 (La to Lh).

As for a portion in the range α which is indicated by α 4, bit data in the MSB sequentially output from the receiver circuit 2 through the output "d" as W0a7, W0c7, W1a7, ..., in a direction indicated by an arrow β shown in FIG. 35, is, as shown in FIG. 12, fetched by B0 of the register 3042 (Re) to B7 of the register 3042 (Rh) in the vertical directional order as W0a5, W0c5, W1a5, ..., W6c6, W7a6 and W7c6. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D4 to D7 of the latches 3043 (La to Lh).

Simultaneously, bit data in the LSB sequentially output from the receiver circuit 2 through the output "e" as W0b7, W0d7, W1b7, ..., in a direction indicated by an arrow β shown in FIG. 35 is fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rd) in the vertical directional order as W0b7, W0d7, W1b7, ..., W6d8, W7b8 and W7d8. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D0 to D3 of the latches 3043 (La to Lh).

Since data of 8 bits × 8 columns, that is, 8-byte data, which is output from the received data buffer

circuit 304 in one output operation uses all of the phases "a", "b", "c" and "d", bit data for one block is converted into 8-bit parallel data for one block by performing the foregoing operation by 16 times for each 64 bits as shown in FIG. 32.

The deinterleaving circuit 5 will now be described. The deinterleaving circuit 5 is separately provided from the decoder section 3 and controlled by the CPU 401 to reproduce the received interleaved block structure D2 in accordance with the received frame type so as to output the reproduced interleaved block structure D2 to the buffer memory 4014.

FIG. 14 is a block diagram showing an example of the structure of the deinterleaving circuit 5. The deinterleaving circuit 5 shown in FIG. 14 comprises shift registers 501A, 501B, 501C and 501D, rearranging circuits 502, 503 and 504 and a selector circuit 505.

Each of the shift registers 501A, 501B, 501C and 501D has a memory, the capacity of which is 8 bits, and receives data from the selector circuit 505 in unit of 8-bit. The shift registers 501A and 501B have output terminals connected to addresses 0 and 1 of the rearranging circuit 502 and to addresses 4 and 5 of the rearranging circuit 504. The shift registers 501C and 501D have output terminals connected to addresses 2 and 3 of the rearranging circuit 503 and to addresses 6 and 7 of the rearranging circuit 504.

The selector circuit 505 has an output terminal connected to the shift registers 501A, 501B, 501C and 501D and arranged to determine a rearranging circuit by selecting the address, to which data is input, the selection being performed under control of the CPU 401. The selector circuit 505 output data supplied from the RDA to each shift register corresponding to the output of the rearranging circuit.

The rearranging circuit 502 treats data, the frame type of which is 3200 bps (2-level FM), such that it fetches 1-byte data from each of the shift registers 501A and 501B to rearrange 2-byte data. Then, the rearranging circuit 502 sequentially output, to the bus line "B", reproduced data in unit of 1-byte, that is, in unit of 8-bit, in the total sum of 2 bytes.

The rearranging circuit 503 treats data, the frame type of which is 3200 bps (4-level FM), such that it fetches 1-byte data from each of the shift registers 501C and 501D to rearrange 2-byte data. Then, the rearranging circuit 503 sequentially output, to the bus line "B", two type data in unit of 1-byte, that is, in unit of 8-bit.

The rearranging circuit 504 treats data, the frame type of which is 6400 bps (4-level FM), such that it fetches 1-byte data from each of the shift registers 501A, 501B, 501C and 501D to rearrange 4-byte data to sequentially output 4-byte reproduced data in unit of

1-byte, that is, in unit of 8-bit, to the bus line "B".

The operation of the deinterleaving circuit 5 will now be described. FIGS. 15 to 17 are diagrams respectively showing the rearranging operations of the rearranging circuits 502, 503 and 504 provided to correspond to the frame types/rates. Referring to FIGS. 15 to 17, a portion of 8-bit data RD, stored in the shift registers 501A to 501D so as to be rearranged and output, which corresponds to four bits including D0 to D3 of the input data WR is referred to LSB, while a portion corresponding to four bits including D4 to D7 is referred to MSB.

1. In the case of 3200 bps (2-level FM):

As shown in FIG. 15, the rearranging circuit 502 is supplied with 8-bit data (D0 to D7) stored in the shift register 501A and 8-bit data (D0 to D7) stored in the shift register 501B by two supplying operations. Then, the rearranging operation is performed such that four odd-order bits (D0, D2, D4 and D6) of 8-bit data supplied to address 1 are rearranged to LSB of address 1 and four even-order bits (D1, D3, D5 and D7) are rearranged to LSB of address 0 so as to be reproduced and output to the bus line "B".

On the other hand, four odd-order bits (D0, D2, D4 and D6) of 8-bit data supplied to address 0 are rearranged to MSB of address 0 and four even-order bits (D1, D3, D5 and D7) are rearranged to MSB of address 1

so as to be reproducing and output to the bus line "B".

As described above, the rearranging circuit 502 is able to reproduce 16-bit (8 bits × 2) data.

2. In the case of 3200 bps (4-level FM):

As shown in FIG. 16, the rearranging circuit 503 is supplied with 8-bit data (D0 to D7) stored in the shift register 501C and 8-bit data (D0 to D7) stored in the shift register 501D by two supplying operations. Then, the rearranging operation is performed such that MSB (D4, D5, D6 and D7) of 8-bit data supplied to address 2 are rearranged to MSB of address 2 and LSB (D0, D1, D2 and D3) are rearranged to MSB of address 3 so as to be reproduced and output to the bus line "B".

On the other hand, MSB (D4, D5, D6 and D7) of 8-bit data supplied to address 3 are rearranged to LSB of address 2 and LSB (D0, D1, D2 and D3) are rearranged to LSB of address 3 so as to be reproduced and output to the bus line "B".

3. In the case of 6400 bps (4-level FM):

Addresses 4, 5, 6 and 7 of the rearranging circuit 504 are, as shown in FIG. 17, supplied with 8-bit data (D0 to D7) respectively stored in the shift registers 501A to 501D in four supplying operations. When the rearranging operation is performed, D5 and D7 in the MSB portion are fetched from input 8-bit data in each of addresses 4, 5, 6 and 7. Then, each of 2-bit data is assigned from LSB portion of address 4 which is output

to the bus line "B" so that 8-bit data at address 4 is formed.

Similarly, D4 and D6 in the MSB portion are fetched from input 8-bit data in each of addresses 4, 5, 6 and 7. Then, each of 2-bit data is assigned from LSB portion of address 5 which is output to the bus line "B" so that 8-bit data at address 5 is formed.

Similarly, D3 and D1 in the LSB portion are fetched from input 8-bit data in each of addresses 4, 5, 6 and 7. Then, each of 2-bit data is assigned from LSB portion of address 6 which is output to the bus line "B" so that 8-bit data at address 6 is formed.

Similarly, D2 and D0 in the LSB portion are fetched from input 8-bit data in each of addresses 4, 5, 6 and 7. Then, each of 2-bit data is assigned from LSB portion of address 7 which is output to the bus line "B" so that 8-bit data at address 7 is formed.

As described above, the rearranging circuit 504 is able to reproduce 6400 bps (4-level FM) 32-bit (8 bits × 4) of 8-bit parallel data.

The address comparison circuit 6 will now be described. FIG. 18 is a circuit diagram showing an example of the internal structure of the address comparison circuit 6. The address comparison circuit 6 has, for example, an address register 601 for previously storing the own address data (21 bits), a comparison circuit 602 for comparing received/reproduced address

data with address data which is stored in the address register 601 and a shift register 603 for outputting, to the bus line "B", an 8-bit coincidence signal "f", which is a result of the comparison performed by the comparison circuit 602.

The operation will now be described. The address field (AF)C5 of data reproduced by the deinterleaving circuit 5 has formatted address data which must be compared and collated with address data previously stored in the own pager.

When the comparison circuit 602 has, in unit of 8-bit, fetched data (data structure in the reproduced address field (AF)C5) supplied from the bus line "B" and which is a subject of comparison, the comparison circuit 602 compares the fetched data and address data supplied from the address register 601 (by using, for example, an EXOR circuit). By totaling the result of the comparison of each bit, a final result of the comparison is obtained (by using, for example, a NOR circuit). The result of the comparison is output to the shift register 603. The shift register 603 sequentially fetches the results of the comparison from the comparison circuit 602 so that the 8-bit coincidence signal "f" denoting the comparison result of the 8-byte address is output.

The overall operation of the circuit for receiving and reproducing data according to the first embodiment will now be described. FIGS. 19 to 22 are flow charts

of the main operation of the pager. FIG. 23 is a flow chart of the operation of the deinterleaving circuit 5.

The main operation of the pager will now be described. FIGS. 19 to 22 are flow charts of the operations of the CPU 401 and the decoder section 3 to be performed from a moment at which the power source of the pager has been turned on to a moment of completion of an operation for receiving data for one frame wherein the operations of the CPU 401 and the decoder section 3 are linked to each other. Note that the operation of the decoder section 3 is described as step R... and that of the CPU 401 is described as step C....

When a predetermined number of bit data has been stored in the RDA of the RAM 403, which can be reproduced by the deinterleaving circuit 5 and CPU 401 has detected the timing at which the deinterleaving circuit 5 can perform a reproducing process, the CPU 401 always output data to the deinterleaving circuit 5 through the bus line "B". The CPU 401 fetches data from the decoder section 3 to write this data to the RDA and performs an operation for correcting an error of data one preceding block stored in the buffer memory 4014 so as to read the contents.

Therefore, if address data included in the received address field (AF)C5 has been determined to be non-coincidence on the basis of the coincidence signal supplied from the address comparison circuit 6, control

is performed such that the operations of the decoder section 3 and the receiver circuit 2 are interrupted.

Referring to FIGS. 19 to 22, data receiving and reproducing processes will now be described. When the CPU 401 has detected at step C1 that the electric power has been supplied by the operation of a power supply switch (not shown), the CPU 401 allows electric power to be supplied to the respective circuit sections connected to the CPU 401 and initializes the sections. At this time, also the operation of the decoder section 3 is started when the initializing operation has been performed so that control data for controlling the received data buffer circuit 304 corresponding to each frame pattern is set to the frame speed determining circuit 302 and the level determining circuit 301. Then, the decoder section 3 is brought into a standby state at the frequency band and the phase set by ID-ROM (steps R1 and R2). In this standby state, the CPU 401 starts an internal timer (not shown) to perform intermittent reception in a period from 1.875 seconds (one frame) to 10 seconds at intervals of 30 seconds for two minutes until synchronization is detected when the synchronization 1 (S1)C1 of the synchronizing signal portion D1 is received (step C3). Then, synchronization detection is performed by receiving the synchronization 1 (S1)C1 until a predetermined time has been elapsed (steps C4 and C6).

If synchronization has been detected, the operation proceeds to step C5 so that the timer is reset, and frame pattern data set by the synchronization 1 (S1)C1 is stored in the buffer memory 4011. If no synchronization is detected in two minutes and the lapse of the predetermined time has been confirmed, the pager is moving or stays in an area outside the service zone. Therefore, the operation proceeds to step C7 in which the fact that the pager exists outside the service zone is displayed on display unit 7. Moreover, an out-of-zone notification interruption signal for interrupting out-of-zone notification, which is output by the notifying portion 8 when the pager exists outside the zone, is output.

When the decoder section 3 has received the synchronization 1 (S1)C1, the decoder section 3 fetches it and causes the level determining circuit 301 to store data included in frame pattern data set by the synchronization 1 (S1)C1 and relating to the modulation method (step R3). Moreover, the decoder section 3 causes the frame speed determining circuit 302 to store data included in the frame pattern data set by the synchronization 1 (S1)C1 and relating to the frame speed (step R4). The received frame pattern data is also output to the CPU 401.

The decoder section 3 continues the intermittent reception at steps R2, R3 and R6 until the out-of-zone

notification interruption signal is received by the CPU 401 at step C7. When the out-of-zone notification interruption signal has been received, the operation proceeds to step R7 in which the operation of the receiver circuit 2 is interrupted.

After step R4 has been performed, the decoder section 3 receives frame information (F1)C2 at step R5, and then output, to the CPU 401, the received cycle number, the received frame number and this timing information for obtaining the own frame from the frame information (F1)C2. The CPU 401, at step C8, recognizes the position of the own frame in accordance with the frame information 42B (FI) and timing information supplied from the decoder section 3 to interrupt operation of the receiver circuit 2 to the timing for the own frame comes. The process at step C8 is continued to the timing for the frame precedes to the own frame by one (step C9). The control of interrupting the operation of the receiver circuit 2 is performed by the decoder section 3 under control of the CPU 401 (step R8). The process at step R8 is repeatedly performed until a re-drive signal is input (step R9).

If the frame timing, which is preceding to the own frame by one, is detected at step C9, the CPU 401 re-drives the decoder section 3 at step C10. When the decoder section 3 is instructed to re-drive from the CPU 401 (step R9), it re-drives the decoder section 3

(step R10) in which the decoder section 3 waits for input of a re-drive control signal for the receiver circuit 2 from the CPU 401 (step R11). When the re-drive control signal for the receiver circuit 2 has been supplied from the CPU 401, the receiver circuit 2 is re-driven at step R12.

The CPU 401 re-drives the decoder section 3 (step C10), and then, at step C11, sets address data read from the ID-ROM of the ROM 402 to the address register of the address comparison circuit 6. At step C12, the CPU 401 determines an output timing of the final block of the frame, which is preceding to the own frame by one. When the timing of the final block has been detected, the CPU 401 outputs an operation control signal to the receiver circuit 2 (step C13).

When the receiver circuit 2 has been re-driven, the decoder section 3 establishes synchronization by the synchronization 1 (S1)C1 of the own frame received at step R13. Moreover, the decoder portion 3 causes the level determining circuit 301 to store data among frame pattern data of the own frame relating to the modulation method and that relating to the frame speed (step R16). Simultaneously, the received frame pattern data is also output to the CPU 401.

Then, the decoder section 3 fetches, decodes and outputs frame information (F1)C2 at step R14. Since the frame type data is, at step R13, also output to the CPU

401, the CPU 401 causes the buffer memory 4011 to re-store the frame type data at step C14. At step C15, whether or not the frames coincide with each other is determined in accordance with the decoded frame information (F1)C2. If non-coincidence is detected, the operation returns to step C8 in which frame timing, which is preceding to the own frame by one, is waited for. If coincidence is detected, the operation proceeds to step C16 in which the own frame is confirmed, continuous reception is controlled and the address of the rearranging circuit is determined by the deinterleaving circuit 5.

The decoder section 3 outputs frame information (F1)C2 to the CPU 401 at step R14, and then, at step R15, waits for input of an interruption signal which is generated when the frame non-coincidence is detected. If the interruption signal has been supplied, the operation returns to step R8 in which the operation of the receiver circuit 2 is interrupted. If the interruption is not supplied, the operation proceeds to step R16. At step R16, the synchronization 2 (S2)C3 is received, and then the timing control circuit 303 confirms synchronization of the reception of the interleaved block structure D2 and performs fine adjustment. At step R17, received data is rearranged by the received data buffer circuit 304 so that the rearranged data is output as 8-bit parallel data.

Then, the operation proceeds to step R18 in which block information (BI)C4, address field (AF)C5 and vector field (VF)C6 set by the synchronizing signal portion D1 are input and the reception is continued.

At step C16, the CPU 401 also performs a process for supplying a selection control signal for selecting any one of the rearranging circuits 502, 503 and 504 which is to be connected to the selector circuit 505 of the deinterleaving circuit 5 in accordance with the frame type of the subject frame by determining the address to be employed (the operation proceeds to step D1 shown in FIG. 23).

After the operation at step C16 has been completed, the CPU 401 determines at step C17 whether or not the received frame type is 1600 bps (2-level FM). If the frame type is 1600 bps (2-level FM), the operation proceeds to step S38 in which the start word of the address field (AF)C5 is read from the block information (BI)C4 so as to be stored in the buffer memory 4013. Then, the operation proceeds to step C39.

If a determination has been performed at step C17 that data is output with a frame type except 1600 bps (2-level FM), the operation proceeds to step C18 in which received data is sequentially stored in the RDA of the RAM 403 until the number of bits of data is stored to permit the reproducing process to be performed and the timing of the reproducing process comes (step C19).

When a determination has been performed that the number of bits of data, which permits the reproducing process can be performed, has been stored and the timing of the reproducing process has come, the operation proceeds to step C20 in which data is read from the RDA to supply data to the deinterleaving circuit 5. Thus, the deinterleaving circuit 5 starts performing the process for reproducing data (refer to step D4 shown in FIG. 23).

The operation of the deinterleaving circuit 5 shown in FIG. 23 will now be described. At step D1, the selector circuit 505 determines the address of the rearranging circuit for storing 8-bit data in accordance with the selection control signal for the rearranging circuit determined at step C16. Then, an operation for waiting for input of 8-bit parallel data starts (step D2). If input of 8-bit parallel data has been confirmed at step D3, the operation proceeds to step D4 in which the input 8-bit parallel data are sequentially stored in the shift register 501 (A to D). Then, 8-bit parallel data are output to the address of the rearranging circuits from the respective shift registers at step D5 as described with reference to FIGS. 15 to 17. Data reproduced by each of the rearranging circuits is, at step D6, again output to the bus line "B". After the reproducing process at step D6 has been completed, operations at steps C21, C25 and C35 are performed.

After the reproducing process at step D6 has been

completed, the CPU 401 stores this data in the buffer memory 4014 to subject the same to the error correction process. At step C21, the start word of the address field (AF)C5 is read in accordance with the block information (BI)C4 to store it in the buffer memory 4013. Then, the operation proceeds to step C22.

At step C22, the CPU 401 stores the received data in the RDA of the RAM 403. At step C23, the CPU 401 determines whether a predetermined number of bits of data, which permits the reproducing process can be performed, has been stored and the timing of the reproducing process has come. If the storage of the predetermined number bits of data and the reproducing timing are confirmed at step C23, the received data are sequentially read from the RDA so as to be output to the deinterleaving circuit 5, at step C24. When data has been supplied to the deinterleaving circuit 5 through the bus line "B", the deinterleaving circuit 5 reproduces data, the frame type of which is that except 1600 bps (2-level FM) and are stored in the shift register 501 (A to D) at step D3.

Then, when the reproduced data is fetched from the deinterleaving circuit 5 through the bus line "B", the CPU 401 stores this data in the buffer memory 4014 to subject the same to the error correction process. Then, the CPU 401 outputs address data included in the address field (AF)C5 to the address comparison circuit 6 (step

C25). At this time, the address comparison circuit 6 compares the received address data fetched through the bus line "B" at the timing of the data trigger "c" with the address data in the address register 601. Then, the coincidence signal "f" denoting the coincidence or non-coincidence is output to the CPU 401.

The CPU 401 instructs the decoder section 3 to fetch data. If the CPU 401 has detected coincidence of addresses because it has received the coincidence signal "f" from the address comparison circuit 6 at step C26, the operation proceeds to step C28. If the coincidence of addresses is not detected, the operation proceeds to step C27 in which the CPU 401 outputs an interruption signal to the decoder section 3. When the interruption signal has been supplied to the decoder section 3 from the CPU 401, the operation returns to step R8 in which the operation of the receiver circuit 2 is interrupted. If the coincidence signal "f" is not supplied, the operation proceeds to step R20. At steps R20 and R21, reception is continued until the interruption signal is received from the CPU 401.

At step C28, data of vector field (VF)C6 is read from the RDA following the address field (AF)C5 so that the start word and the number of words in the message field (MF)C7 are determined. At step C29, a process for interrupting the operation of the receiver circuit 2 until the start word of own message data appears is

performed. When the interruption control starts, only own message data can be fetched in accordance with the determined start word. Since the decoder section 3 receives the interruption signal at step R21, the decoder section 3 interrupts the operation of the receiver circuit 2 at step R22 and the above-mentioned state is maintained until the re-drive signal is received.

When the CPU 401 has confirmed the timing for receiving the start word of own message data at step C30, the CPU 401 outputs the re-drive signal to the decoder section 3 at step C31 in order to re-drive the receiver circuit 2. Thus, the receiver circuit 2 receives data. At step C32, the CPU 401 sequentially stores received data in the RDA through the decoder section 3. When the decoder section 3 has received the above-mentioned re-drive signal output at step C31 (step R23), the receiver circuit 2 is re-driven (step R24).

After data storage in the RDA has been started at step C32, the CPU 401 determines at step C23 whether a predetermined number of bits of data, which permits the reproducing process can be performed, has been stored and the timing of the reproducing process has come. If the storage of the predetermined number bits of data and the reproducing timing are confirmed at step C32, the received data (message data) are sequentially read from the RDA so as to be output to the deinterleaving circuit

5, at step C35. When the deinterleaving circuit 5 performs the data reproducing process, data in the next block is stored in the RDA. Then, the operation proceeds to step C35.

When data reproduced by the deinterleaving circuit 5 has been output to the bus line "B", idle blocks (IB)C8 is detected at step C35. When the idle blocks (IB)C8 is detected, an interruption signal is output to the decoder section 3 in order to interrupt the operation of the receiver circuit 2 to the timing for receiving the own frame. In order to control the reception notification at step C37, the CPU 401 causes the notifying section 8 to notify the reception and reproduces and displays a message in accordance with the received own message data, and then the operation returns to step C9. Thus, the CPU 401, at step C9, waits for the timing of the frame, which precedes to the own frame by one. When the receiver circuit 2 has been re-driven at step R24, the decoder section 3 continues the reception operation until the operation is interrupted by the CPU 401 at step C36 (steps R25 and R26). When the interruption signal has been received at step R26, the operation proceeds to step R27 in which the operation of the receiver circuit 2 is interrupted. Then, the decoder section 3 completes the receiving operation.

Thus, the operations of the CPU 401 and the decoder

section 3 have been described so that they are linked to each other to receive data with the frame pattern except 1600 bps (2-level FM) in accordance with a result of the determination performed at step C17. If the frame type of the received data is determined as 1600 bps (2-level FM) at step C17, the receiving operation, which is performed by the CPU 401, is shifted to step C38 in which an operation, in which the reproducing operation is not performed, is started.

At step C38, the block information (BI)C4 is fetched into the buffer memory 4014 so as to be subjected to the error correction process. Then, the start word of the address field (AF)C5 is stored. The CPU 401, at step C39, outputs address data, which is stored in the address field (AF)C5, to the address comparison circuit 6. Thus, the address comparison circuit 6 compares the received address data fetched through the bus line "B" at the timing of the supplied data trigger "c" with the address data in the address register 601. Then, the address comparison circuit 6 outputs the coincidence signal "f" to the CPU 401.

When the CPU 401 has detected the coincidence signal "f" denoting the coincidence of the addresses supplied from the address comparison circuit 6 at step C40, the CPU 401 shifts the operation to step C41. If the coincidence signal "f" is not detected, the CPU 401 shifts the operation to step C27 in which

an interruption signal is output to the decoder section 3. When the decoder section 3 has received the interruption signal from the CPU 401, the operation returns to step R8 in which the operation of the receiver circuit 2 is interrupted. If the coincidence signal "f" is not detected, the operation proceeds to steps R20 and R21 in which reception is continued until the interruption signal is supplied from the CPU 401.

At step C41, data of the vector field (VF)C6 is, following the address field (AF)C5, supplied from the receiver circuit 2 so that the start word of own message data and the number of words in the message field (MF)C7 are determined. At step C42, control is performed such that the operation of the receiver circuit 2 is interrupted until the start word of own message data is detected. When the interruption control has started, only own message can be fetched in accordance with the determined start word. Since the decoder section 3 receives the interruption signal at step R21, it interrupts the operation of the receiver circuit 2 at step R22 and maintains this state until the re-drive signal is supplied.

When the CPU 401 has confirmed timing for receiving the start word of own message data at step C43, the CPU 401 outputs the re-drive signal to the decoder section 3 in order to re-drive the receiver circuit 2 (step C44). Thus, the receiver circuit 2 receives data, and the CPU

401 sequentially reads own message data in unit of 8-bit (step C45) and detects the idle blocks (IB)C8 (step C46). When the re-drive signal output at step C31 has been supplied at step R23, the decoder section 3 re-drives the receiver circuit 2 (step R24).

If the idle blocks (IB)C8 has been detected at step C45, an interruption signal is output to the decoder section 3 in order to interrupt the operation of the receiver circuit 2 to the timing for receiving a next own frame (step C36). The CPU 401, at step C37, causes the notifying section 8 to perform the notification process and reproduces and displays the message in accordance with the received message data in order to control notification of reception. Then, the CPU 401 returns the operation to step C9. As described above, the CPU 401, at step C9, waits for timing for the frame, which is preceding to the own frame by one. After the receiver circuit 2 has been re-driven at step R24, the decoder section 3 continues the receiving operation until the operation is interrupted by the CPU 401 at step C36 (steps R25 and R26). When the interruption signal has been received at step R26, the operation proceeds to step R27 in which the operation of the receiver circuit 2 is interrupted. Then, the decoder section 3 completes the receiving operation.

As described above, according to the first embodiment, when information (synchronization 1 (S1)C1)

indicating the frame type has been received, the frame type of the data is determined. In accordance with the determined frame type, a suitable rearranging circuit is selected from the plural rearranging circuits. Therefore, load distribution to the hardware and software can be balanced. As a result, the size of the circuit and the load of the CPU can be reduced.

(Second Embodiment)

The first embodiment has the structure such that the data receiving operation is performed by the CPU 401 as follows. When a predetermined number of data bits have been stored in the RDA in the RAM 403, which can be reproduced and the timing for performing the reproducing process comes, a suitable rearranging circuit is selected from the plural rearranging circuits in the deinterleaving circuit 5 in accordance with the frame type of the received data. The addresses of the data reproduced by the selected rearranging circuit are subjected to a comparison processing. If the coincidence is detected, own data of the message field is fetched so that the reproducing process is performed.

However, according to the first embodiment, the CPU 401 controls the data transfer among the RAM 403, the deinterleaving circuit 5 and the address comparison circuit 6, complicated control of data transfer is required in addition to the main operation for reproducing data. Therefore, there sometimes arises

a problem in that the data processing rate is lowered.

Accordingly, a pager according to a second embodiment is provided with a DMA (Direct Memory Access) circuit 11. Thus, when the CPU 401 performs the data receiving operation, as shown in FIG. 30, the DMA circuit 11 controls data transfer among the CPU 401, the RAM 404, the deinterleaving circuit 5 and the BCH decoder 10 for performing the error correction process. Thus, load which must be borne by the CPU 401 for transferring data is intended to be reduced.

Referring to FIGS. 24 to 32, the second embodiment of the present invention will now be described. In the second embodiment, the data structure C and the block structure D shown in FIG. 32 are employed.

FIG. 24 is a block diagram showing the structure of circuits in the pager which is the second embodiment of the data receiving apparatus according to the present invention. The same elements as those of the pager according to the first embodiment and shown in FIG. 1 are indicated by the same reference numerals and the same elements are omitted from description.

The pager according to this embodiment comprises the antenna 1, the receiver circuit 2, the decoder section 3, the control section 4, the deinterleaving circuit 5, the address comparison circuit 6, the display unit 7, the notifying section 8, the power supply circuit 9, the BCH decoder 10, the DMA circuit 11 and

a key input section 12.

The control section 4 controls the overall operation of the pager in accordance with a control program stored in the ROM 402 and comprises the CPU 401, the ROM 402 and a RAM 404. The CPU 401 has the buffer memory 4011 for temporarily storing the frame pattern read from, for example, the synchronization 1 (S1)C1, the buffer memory 4012 for temporarily storing data (cycle number, frame number and number of plural output operations) read from the frame information (F1)C2, the buffer memory 4013 for storing the block information (BI)C4 and data read from the vector field (VF)C5 (the start word of the own message data and the number of words of message data in the address field (AF), the vector field (VF) and the message field (MF)) and the clock generator 4015 for generating clocks for use to adjust the timing of the receiving process and the like. The CPU 401 controls circuit sections connected to the CPU 401 by using the data contained in one frame and the clocks.

The RAM 404, as shown in FIG. 25, has a work area WA for enabling the CPU 401 to be operated, a memory area BDM (Block Data Memory) which is used to reproduce the received data and so that 11-block addresses of the received data for one frame supplied from the decoder section 3 at the time of performing the receiving operation are assigned in unit of block, and a memory

area MMA for storing the received message data.

The BDM stores data for one frame, which is being received and reproduced, by assigning the address.

Data thus-stored is, under control of the DMA circuit 11, to be described later, output to the deinterleaving circuit 5. Data reproduced by the deinterleaving circuit 5 is re-stored in the same storage address, and then output so as to be subjected to an error correction process in the BCH decoder 10.

In a case where the block data includes an address field, data subjected to the error correction process in the address comparison circuit 6 is again output so as to be subjected to a comparison of the address data is then subjected to the address comparison process. If the coincidence is detected, data is re-stored in the same address. If the non-coincidence is detected, data is not stored in the DBM and deleted.

The BCH decoder 10 corrects an error in data by using a 10-bit BCH code and even-number parity bits included in data for one block reproduced by the deinterleaving circuit 5, and then output the error bit number to the CPU 401.

The DMA (Direct Memory Access) circuit 11 controls data transfer among the CPU 401, the RAM 404, the deinterleaving circuit 5, the address comparison circuit 6 and the DMA circuit 11 through the bus line "B".

The key input section 12 is composed of a main

switch, cursor keys and memory keys to output signals denoting the operations of the key operations to the CPU 401.

The overall operation of the second embodiment will now be described.

FIGS. 26 to 29 are flow charts of the main operation of the pager. FIG. 30 is a timing chart of the operations in the DMA circuit 11 for reading and writing data between the BDM and the other circuits.

When the CPU 401 has detected at step C101 that the electric power has been supplied by the operation of a power supply switch (not shown), the CPU 401 allows electric power to be supplied to the respective circuit sections connected to the CPU 401 and initializes the sections. At this time, also the operation of the decoder section 3 is started when the initializing operation has been performed so that control data for controlling the received data buffer circuit 304 corresponding to each frame pattern is set to the frame speed determining circuit 302 and the level determining circuit 301. Then, the decoder section 3 is brought into a standby state at the frequency band and the phase set by ID-ROM (steps R101 and R102). In this standby state, the CPU 401 starts an internal timer (not shown) to perform intermittent reception in a period from 1.875 seconds (one frame) to 10 seconds at intervals of 30 seconds for two minutes until synchronization is

detected when the synchronization 1 (S1)C1 of the synchronizing signal portion D1 is received (step C103). Then, synchronization detection is performed by receiving the synchronization 1 (S1)C1 until a predetermined time has been elapsed (steps C104 and C106).

If synchronization has been detected, the operation proceeds to step C105 in which the timer is reset, and frame pattern data set by the synchronization 1 (S1)C1 is stored in the buffer memory 4011. If no synchronization is detected in two minutes and the lapse of the predetermined time has been confirmed, the pager is moving or stays in an area outside the service zone. Therefore, the operation proceeds to step C107 in which the fact that the pager exists outside the service zone is displayed on display unit 7. Moreover, an out-of-zone notification interruption signal for interrupting out-of-zone notification, which is output by the notifying portion 8 when the pager exists outside the zone, is output.

When the decoder section 3 has received the synchronization 1 (S1)C1, the decoder section 3 fetches it and causes the level determining circuit 301 to store data included in frame pattern data set by the synchronization 1 (S1)C1 and relating to the modulation method (step R103). Moreover, the decoder section 3 causes the frame speed determining circuit 302 to store

data included in the frame pattern data set by the synchronization 1 (S1)C1 and relating to the frame speed (step R104). The received frame pattern data is also output to the CPU 401.

The decoder section 3 continues the intermittent reception at steps R102, R103 and R106 until the out-of-zone notification interruption signal is received by the CPU 401 at step C107. When the out-of-zone notification interruption signal has been received, the operation proceeds to step R107 in which the operation of the receiver circuit 2 is interrupted.

After step R104 has been performed, the decoder section 3 receives frame information (F1)C2 at step R105, and then output, to the CPU 401, the received cycle number, the received frame number and this timing information for obtaining the own frame from the frame information (F1)C2. The CPU 401, at step C108, recognizes the position of the own frame in accordance with the frame information 42B (FI) and timing information supplied from the decoder section 3 to interrupt operation of the receiver circuit 2 until the timing for the own frame comes. The process at step C8 is continued to the timing for the frame which precedes to the own frame by one (step C109). The control of interrupting the operation of the receiver circuit 2 is performed by the decoder section 3 under control of the CPU 401 (step R108). The process at step R108 is

repeatedly performed until a re-drive signal is input (step R109).

If the frame timing, which is preceding to the own frame by one, is detected at step C109, the CPU 401 re-drives the decoder section 3 at step C110. When the decoder section 3 is instructed to re-drive from the CPU 401 (step R109), it re-drives the decoder section 3 (step R110) in which the decoder section 3 waits for input of a re-drive control signal for the receiver circuit 2 from the CPU 401 (step R111). When the re-drive control signal for the receiver circuit 2 has been supplied from the CPU 401, the receiver circuit 2 is re-driven at step R112.

The CPU 401 re-drives the decoder section 3 (step C110), and then, at step C111, sets address data read from the ID-ROM of the ROM 402 to the address register of the address comparison circuit 6. At step C112, the CPU 401 determines an output timing of the final block of the frame, which is preceding to the own frame by one. When the timing of the final block has been detected, the CPU 401 outputs an operation control signal to the receiver circuit 2 (step C113).

When the receiver circuit 2 has been re-driven, the decoder section 3 establishes synchronization by the synchronization 1 (S1)C1 of the own frame received at step R113. Moreover, the decoder portion 3 causes the level determining circuit 301 to store data among frame

pattern data of the own frame relating to the modulation method and that relating to the frame speed (step R116). Simultaneously, the received frame pattern data is also output to the CPU 401.

Then, the decoder section 3 fetches, decodes and outputs frame information (F1)C2 at step R114. Since the frame type data is, at step R113, also output to the CPU 401, the CPU 401 causes the buffer memory 4011 to re-store the frame type data at step C114. At step C115, whether or not the frames coincide with each other is determined in accordance with the decoded frame information (F1)C2. If non-coincidence is detected, the operation returns to step C108 in which frame timing, which is preceding to the own frame by one, is waited for. If coincidence is detected, the operation proceeds to step C116 in which the own frame is confirmed, continuous reception is controlled and the address of the rearranging circuit is determined by the deinterleaving circuit 5.

The decoder section 3 outputs frame information (F1)C2 to the CPU 401 at step R114, and then, at step R115, waits for input of an interruption signal which is generated when the frame non-coincidence is detected. If the interruption signal has been supplied, the operation returns to step R108 in which the operation of the receiver circuit 2 is interrupted. If the interruption is not supplied, the operation proceeds to

step R116. At step R116, the synchronization 2 (S2)C3 is received, and then the timing control circuit 303 confirms synchronization of the reception of the interleaved block structure D2 and performs fine adjustment. At step R117, received data is rearranged by the received data buffer circuit 304 so that the rearranged data is output as 8-bit parallel data. Then, the operation proceeds to step R118 in which block information (BI)C4, address field (AF)C5 and vector field (VF)C6 set by the synchronizing signal portion D1 are input and the reception is continued.

At step C116, the CPU 401 also performs a process for supplying a selection control signal for selecting any one of the rearranging circuits 502, 503 and 504 which is to be connected to the selector circuit 505 of the deinterleaving circuit 5 in accordance with the frame type of the subject frame by determining the address to be employed.

After the operation at step C116 has been completed, the CPU 401 determines at step C117 whether or not the received frame type is 1600 bps (2-level FM). If the frame type is 1600 bps (2-level FM), the operation proceeds to step C127 in which the start word of the address field (AF)C5 is read from the block information (BI)C4 so as to be stored in the buffer memory 4013. Then, the operation proceeds to step C128.

If a determination has been performed at step C117

that data is output with a frame type except 1600 bps (2-level FM), the operation proceeds to step C118 in which the 8-bit parallel data is stored in the BDA of the RAM 404 with the addresses being assigned.

When it is determined that the number of data bits, which permits the reproducing process can be performed, has been stored, the DMA circuit 11 sequentially reads the data from the BDM and supplies the data to the deinterleaving circuit 5. Thus, the deinterleaving circuit 5 performs the data reproducing process and re-stores the reproduced data at the read address. When the data of one block is reproduced, the data of one block are read from the BDM and are supplied to the BCH decoder 10. The error-corrected data of one block are re-stored at the read addresses.

Then, the CPU 401, at step C119, on the basis of the block information (BI)C4, reads the start word of each of the address field (AF)C5 and the vector field (VF)C6 of data subjected to the error correction process. Then, the operation proceeds to step C120.

Then, the CPU 401 instructs to perform a comparison of address data stored in the BDM of the RAM 404. The DMA circuit 11 reads address data included in the reproduced address field (AF)C5 which has been stored in the BDM so as to output the same to the address comparison circuit 6. The address comparison circuit 6, at the timing of the data trigger "c", compares the

address data received through the bus line "B" with the address data in the address register 601. Then, the address comparison circuit 6 outputs, to the CPU 401, a coincidence signal "f" denoting whether address data items coincide with each other.

The CPU 401 instructs the decoder section 3 to fetch data. Moreover, when the CPU 401 has detected the coincidence of addresses because it has received the coincidence signal "f" from the address comparison circuit 6 at step C120, it shifts the operation to step C121. If the address coincidence is not detected, the operation proceeds to step C123 in which an interruption signal is output to the decoder section 3. When the decoder section 3 has been supplied with the interruption signal from the CPU 401, the operation returns to step R108 in which the operation of the receiver circuit 2 is interrupted. If the coincidence signal "f" is not supplied, the operation proceeds to step R120 in which the receiving operation is continued.

At step C121, the start word and the number of words of own message data in the message field (MF)C7 are determined in accordance with vector data in the vector field (VF)C6. At step C122, data for one frame is sequentially fetched, and then storage address is assigned. Then, data is sequentially stored in the BDM of the RAM 404.

Simultaneously with the receiving operation

performed by the CPU 401, data which is sequentially stored in the BDM is repeatedly written to and read from both of the deinterleaving circuit 5 and the BCH decoder 10.

At step C124, the idle blocks (IB)C8 is detected. When the idle blocks (IB)C8 has been detected, an interruption signal is output in order to interrupt the operation of the receiver circuit 2 to the timing for receiving a next own frame. The CPU 401, at step C126, performs control of the reception notification by performing processes for reproducing and displaying message in accordance with the received message data subjected to the notifying process in the notifying section 8. Then, the operation returns to step C109. As described above, the CPU 401 waits for a frame timing which precedes to the own frame by one. Note that the receiving operation of the decoder section 3 is continued (step R121) until interruption of the operation is instructed from the CPU 401 at step C125. If the interruption signal is supplied at step R121, the operation proceeds to step R122 in which the operation of the receiver circuit 2 is interrupted. Then, the decoder section 3 completes the receiving operation.

The operations of the CPU 401 and the decoder section 3 have been described in which they are linked to each other to receive data with the frame pattern except 1600 bps in accordance with a result of the

determination performed at step C117. If the frame type of received data is detected as 1600 bps (2-level FM) at step C117, the receiving operation, which is performed by the CPU 401, is shifted to step C127 in which an operation, in which the reproducing operation is not performed, is started.

At step C127 block information (BI)C4 is output to the BCH decoder 10 so as to be subjected to the error correction process, and then stored in the BDM of the RAM 404. Then, the start words of each of the address field (AF)C5 and the vector field (VF)C6 are stored in the buffer memory 4013.

The CPU 401, at step C128, outputs address data, which is included in the address field (AF)C5, to the address comparison circuit 6. The address comparison circuit 6 compares the address data supplied through the bus line "B" at the timing of the data trigger "c" and the address data in the address register 601. Then, the address comparison circuit 6 outputs the coincidence signal "f" to the CPU 401.

At step C129, the CPU 401 detects the coincidence signal "f" supplied from the address comparison circuit 6. If the addresses coincide with each other, the operation proceeds to step C130. If the coincidence is not detected, the operation proceeds to step C123 in which an interruption signal is output to the decoder section 3. When the decoder section 3 has received the

interruption signal from the CPU 401, the operation returns to step R108 in which the operation of the receiver circuit 2 is interrupted. If the coincidence signal "f" is not detected, the operation proceeds to step R131 in which the receiving operation is continued.

At step C130, the start word and the number of words of own message data in the message field (MF)C7 are determined in accordance with data of the vector field (VF)C6.

The CPU 401 causes the receiver circuit 2 to continue the data receiving process in which data is sequentially stored in the BDM in unit of one block. Moreover, the CPU 401 causes the DMA circuit 11 to continue the data transfer processes (step C131). Then, own message data are sequentially read, and then the idle blocks (IB)C8 is detected (step C132).

If the idle blocks (IB)C8 is detected at step C132, the CPU 401 outputs an interruption signal to the decoder section 3 in order to interrupt the operation of the receiver circuit 2 to the timing for receiving a next own frame (step C125). In order to control the reception notification at step C125, the notification process is performed by the notifying section 8 and the message is reproduced and displayed in accordance with received own message data. Then, the operation returns to step C109. As described above, the CPU 401, at step C109, waits for the frame timing, which is preceding to

the own frame by one. When the interruption signal has been supplied to the decoder section 3 at step R121, the operation proceeds to step R122 in which the operation of the receiver circuit 2 is interrupted. Then, the decoder section 3 completes the receiving operation.

The operation, which is performed by the DMA circuit 11 will now be described with reference to a timing chart shown in FIG. 30. The timing chart shown in FIG. 30 shows the operation of the DMA circuit 11 for transfer data for one block (block #0) when data, the frame type of which is, for example, 6400 bps (4-level FM) has been received. Data, the frame type of which is 6400 bps (4-level FM), and which has been received by the receiver circuit 2 is decoded into parallel data by the decoder section 3 for each 8 bits. When parallel data has been output to the bus line "B", addresses are assigned and sequentially stored in the BDM formed in the RAM 404 under control of the CPU 401.

The DMA circuit 11, is turned on simultaneously with the reproducing process, sequentially makes accesses to data among 8-bit parallel data being stored in the BDM. The data of the block #0 having a predetermined number of bits which can be reproduced are sequentially read and supplied to the deinterleaving circuit 5. After the data reproducing process has been completed by the deinterleaving circuit 5, the reproduced data is again output to the BDM so as to be

written to the same address.

As described above, when data, the frame type of which is 6400 bps (4-level FM), has been received, the DMA circuit 11 repeatedly outputs and receives block data between the BDM and the deinterleaving circuit 5 until reproducing process for one block is performed four times.

In order to cause the BCH decoder 10 to BCH-decode (correct an error) data written back to the BDM by the DMA circuit 11, the CPU 401 causes the DMA circuit 11 to read data again from the BDM so as to output the same to the BCH decoder 10. After the BCH decoder 10 has completed the error correction process, corrected data is again output to the BDM so as to be written to the same address.

During the error correction process which is performed by the BCH decoder 10, the DMA circuit 11 makes an access to data in a next block (block #1) which is being stored in the BDM to follow an instruction from the CPU 401 to output the same to the deinterleaving circuit 5 so as to be reproduced. In the case shown in FIG. 30, a process is being performed with which data is output to the deinterleaving circuit 5 relating to a process for reproducing data (second time and third time) in the next blocks.

In a case where the corrected block is data (block #1 or block #1 and block #2) in the address field (AF)C5,

the CPU 401 reads address data in data which is written back to the BDM by the DMA circuit 11 and outputs the same to the address comparison circuit 6 so as to be compared with the address data of ID information. If the coincidence signal "f" from the address comparison circuit 6 is detected, the address data is written back to the BDM.

Simultaneously with the address comparison process which is performed by the address comparison circuit 6, the following process is repeatedly performed in the DMA circuit 11. The reproduced data (data of the block #3) is repeatedly transfered from the BDM to the BCH decoder 10 and the next data (data of the block #4) which is output from the decoder section 3 and stored in the BDM are accessed to be supplied to the deinterleaving circuit 5.

As described above, according to the second embodiment, the DMA circuit 11 for controlling data transfer among the CPU 401, the BDM of the RAM 404, the deinterleaving circuit 5, the address comparison circuit 6 and the BCH decoder 10 is provided in addition to the structure of the first embodiment so that the load which must be borne by the CPU 401 for transferring data is reduced.

FIG. 31 is a circuit diagram showing a modification of the second embodiment. As shown in FIG. 31, the structure according to this modification comprises

a receiver module 14 formed of a PC card having an interface 15 and a circuit substrate for a personal computer, and a portable data terminal 17 having an interface 16 for a PC card slot or the like.

Referring to FIG. 31, the receiver module 14 has the antenna 1, the receiver circuit 2, the decoder section 3, the buffer memories 4011 to 4014, the clock generator 4015, the ROM 402, the RAM 404, the deinterleaving circuit 5, the address comparison circuit 6, the BCH decoder 10, the DMA circuit 11 and the interface 15 capable of output and receiving data in the bus line "B". The portable data terminal 17 has the CPU 401 for controlling the data receiving and reproducing processes, the display unit 7, the notifying section 8 and a CPU 13 for controlling circuits in the portable data terminal 17.

Although both of the first embodiment and the second embodiment of the present invention have the structure such that the present invention is applied to a sole pager adapted to paging system STD-43, the present invention is not limited to this system. The present invention may be applied to any one of information communication terminal, data communication device connected to a personal computer and the like.

For example, the present invention may be applied to any pager adapted to a data communication method in which information about regulation of the data frame

speed or the modulation method can be output. In this case, even if a paging service company mixedly uses a plurality of paging systems, the pager according to the present invention may be applied.

C L A I M S

1. A data receiving apparatus comprising:

receiving means for receiving data;

plural reproducing means capable of reproducing received data having a format which can be recognized by said data receiving apparatus;

format data receiving means for receiving format data; and

selection means for selecting one of said plural reproducing means in accordance with the format data received by said format data receiving means.

2. A data receiving apparatus according to claim 1, wherein said format data denotes a data transmission rate.

3. A data receiving apparatus according to claim 2, further comprising control means for controlling a reproducing process rate of said selected reproducing means in accordance with the format data denoting the transmission rate received by said format data receiving means.

4. A data receiving apparatus according to claim 1, wherein said format data denotes a data modulation mode.

5. A data receiving apparatus according to claim 4, further comprising conversion means for converting data received by said one of plural receiving means into parallel data corresponding to the format data denoting the data modulation mode.

6. A data receiving apparatus according to any one of claims 5, wherein said conversion means comprises plural registers for used for converting received data into the parallel data and corresponding to data modulation modes.

7. A data receiving apparatus according to any one of claims 5, further comprising:

data storage means for dividing the parallel data output from said conversion means into data items of a predetermined unit and for sequentially storing divided data items;

reading means for reading the divided data items from said data storage means in a storing order and supplying read data items to said one of plural reproducing means selected by said selection means; and

storage control means for storing the parallel data output from said one of plural reproducing means in said data storage means at addresses of the divided data items read by said reading means.

8. A data receiving apparatus according to any one of claims 5, further comprising:

data storage means for storing data which is to be reproduced by one time by said one of plural reproducing means selected by said selection means;

detection means for detecting a data reproduction timing of said one of plural reproducing means selected by said selection means; and

storage control means for sequentially transferring the parallel data from said data storage means to said reproducing means and sequentially storing the parallel data output from said converting means to said data storage means.

9. A data receiving apparatus according to claim 1, wherein said format data includes first format data denoting a data transmission rate and second format data denoting a data modulation mode.

10. A data receiving apparatus according to claim 9, further comprising control means for controlling a reproducing process rate of said selected reproducing means in accordance with the first format data received by said format data receiving means.

11. A data receiving apparatus according to claim 10, further comprising conversion means for converting data received by said receiving means into parallel data corresponding to the second format data received by said format data receiving means.

12. A data receiving apparatus according to claim 11, wherein said conversion means comprises plural registers for used for converting received data into the parallel data and corresponding to data modulation modes.

13. A data receiving apparatus according to claim 11, further comprising:

data storage means for dividing the parallel data output from said conversion means into data items of

a predetermined unit and for sequentially storing divided data items;

reading means for reading the divided data items from said data storage means in a storing order and supplying read data items to said one of plural reproducing means selected by said selection means; and

storage control means for storing the parallel data output from said one of plural reproducing means in said data storage means at addresses of the divided data items read by said reading means.

14. A data receiving apparatus according to claim 11, further comprising:

data storage means for storing data which is to be reproduced by one time by said one of plural reproducing means selected by said selection means;

detection means for detecting a data reproduction timing of said one of plural reproducing means selected by said selection means; and

storage control means for sequentially transferring the parallel data from said data storage means to said reproducing means and sequentially storing the parallel data output from said converting means to said data storage means.

15. A data receiving apparatus according to claim 1, wherein said format data denotes a data interleaving mode.

16. A data receiving apparatus according to

claim 15, further comprising conversion means for converting data received by said receiving means into parallel data corresponding to the format data received by said format data receiving means.

17. A data receiving apparatus according to claim 16, wherein said conversion means comprises plural registers for used for converting received data into the parallel data and corresponding to data modulation modes.

18. A data receiving apparatus according to claim 16, further comprising:

data storage means for dividing the parallel data output from said conversion means into data items of a predetermined unit and for sequentially storing divided data items;

reading means for reading the divided data items from said data storage means in a storing order and supplying read data items to said one of plural reproducing means selected by said selection means; and

storage control means for storing the parallel data output from said one of plural reproducing means in said data storage means at addresses of the divided data items read by said reading means.

19. A data receiving apparatus according to claim 16, further comprising:

data storage means for storing data which is to be reproduced by one time by said one of plural reproducing means selected by said selection means;

detection means for detecting a data reproduction timing of said one of plural reproducing means selected by said selection means; and

storage control means for sequentially transferring the parallel data from said data storage means to said reproducing means and sequentially storing the parallel data output from said converting means to said data storage means.

20. A data receiving apparatus according to claim 1, further comprising format data storage means for storing the format data received by said format data receiving means until format data is received next.

21. A data receiving apparatus according to claim 1, further comprising:

ID code storage means for storing an ID code for specifying paging of said data receiving apparatus;

detection means for detecting the ID code from reproduced data while a reproducing process of said reproducing means continues; and

interrupting means for comparing a detected ID code with the ID code stored in said ID code storage means and for interrupting the reproducing process of said reproducing means when a coincidence is not detected.

22. A data receiving apparatus according to claim 1, which further comprises an interface for establishing a connection with an external device, and in which a receiving process of said data receiving apparatus is

performed in accordance with a control signal supplied from said external device through said interface.

23. A method of deinterleaving data in which data received by plural rearranging circuits are reproduced into data comprising the following steps of:

receiving format data; and

selecting one of said plural rearranging circuits in accordance with received format data.

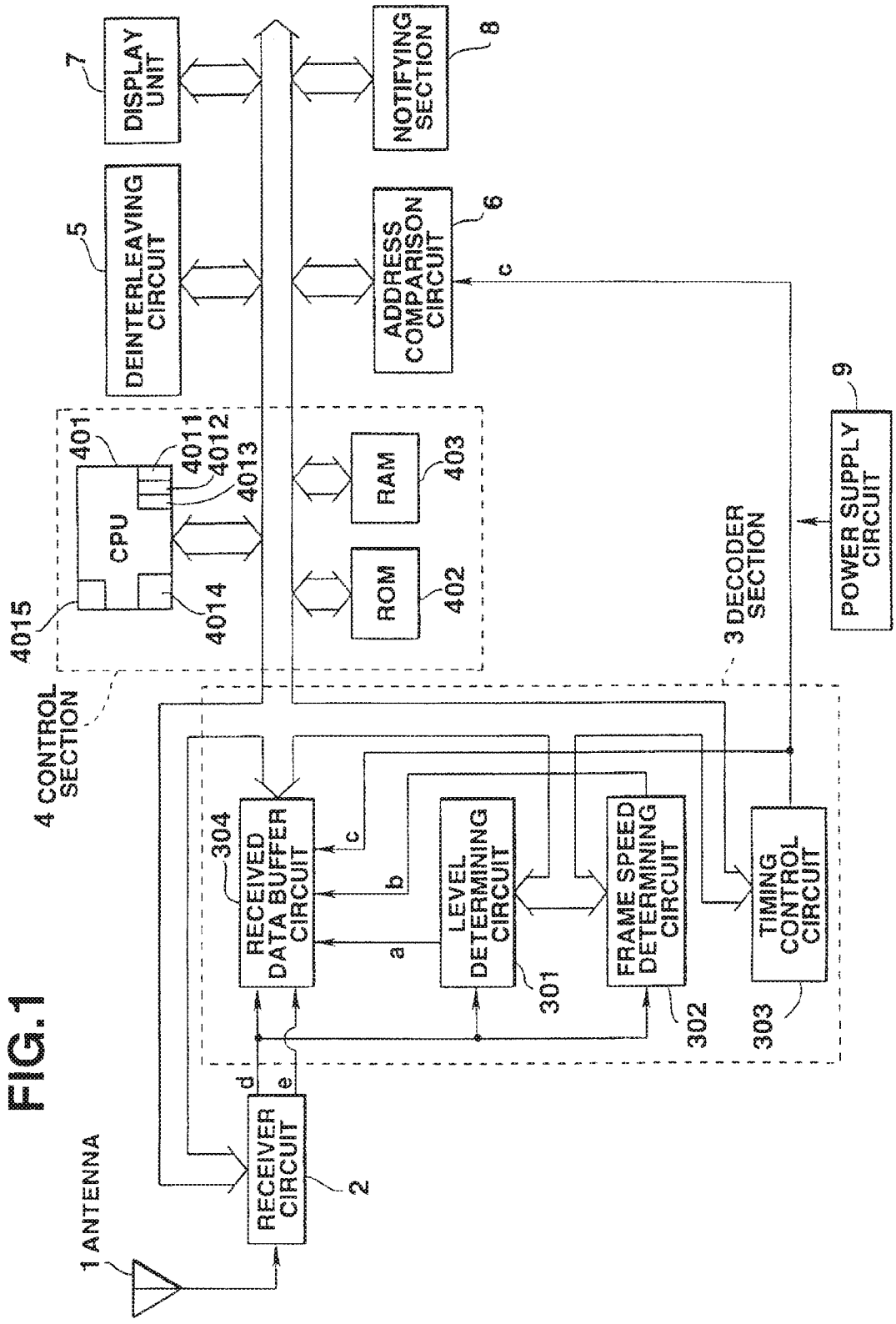

1 ANTENNA
RECEIVER CIRCUIT
2
4 CONTROL SECTION
4015
CPU
401
4011
4012
4013
4014
RAM
403
ROM
402
3 DECODER SECTION
RECEIVED DATA BUFFER CIRCUIT
304
LEVEL DETERMINING CIRCUIT
301
FRAME SPEED DETERMINING CIRCUIT
302
TIMING CONTROL CIRCUIT
303
a
b
c
d
e
DEINTERLEAVING CIRCUIT
5
ADDRESS COMPARISON CIRCUIT
6
DISPLAY UNIT
7
NOTIFYING SECTION
8
POWER SUPPLY CIRCUIT
9

FIG. 1

FIG.2

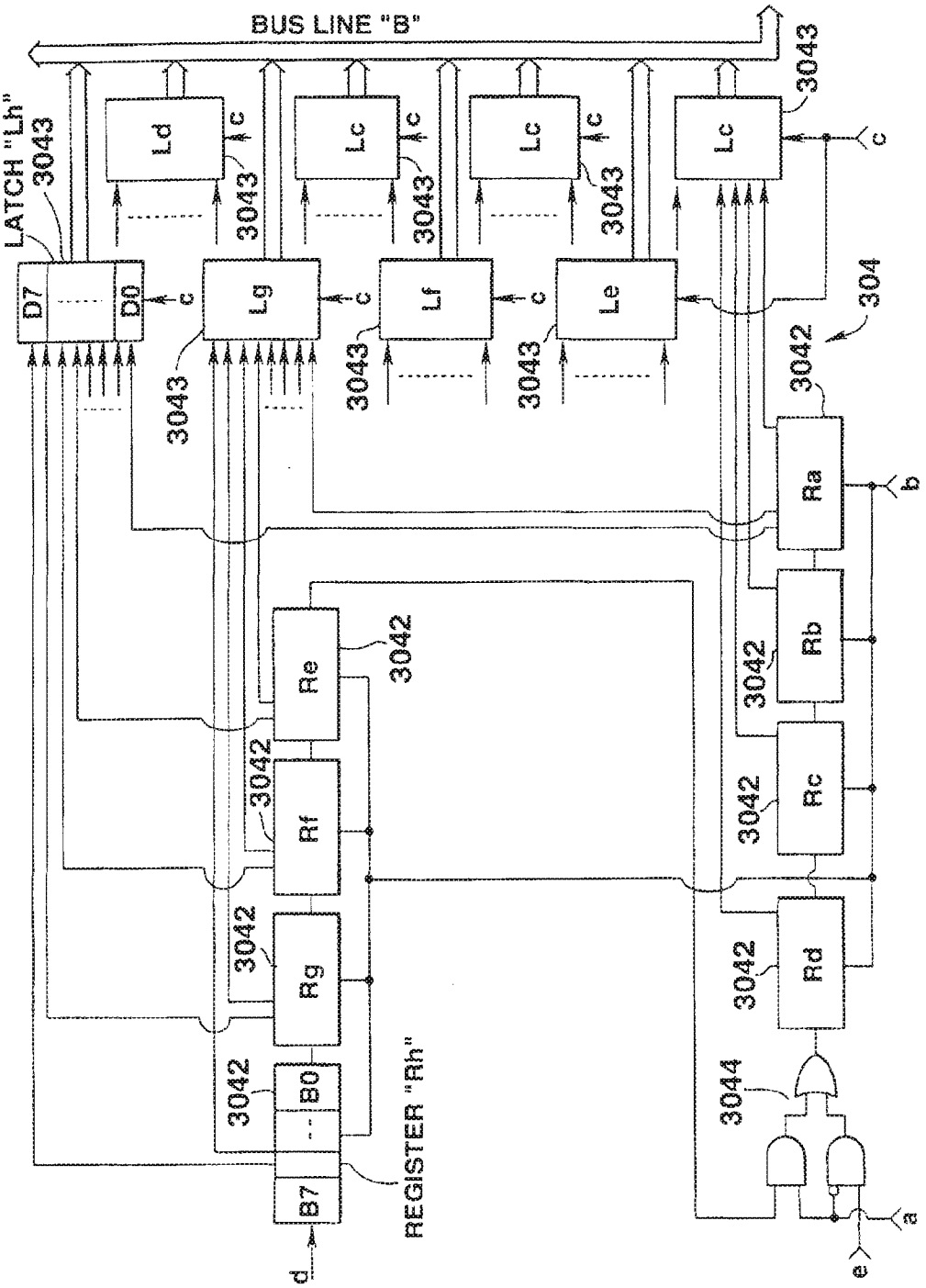

BUS LINE "B"
LATCH "Lh"
3043
Ld
Lc
Lg
Lf
Le
D7
D0
c
304
3042
Ra
Rb
Rc
Rd
Re
Rf
Rg
B0
B7
REGISTER "Rh"
3044
a
b
d
e

FIG.3

REGISTER		Rh	Rg	Rf	Re	Rd	Rc	Rb	Ra
	LATCH								
B7		LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
B6		LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
B5		LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
B4		LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
B3		LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
B2		LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
B1		LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
B0		LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0

FIG.4

REGISTER		Rh	Rg	Rf	Re	Rd	Rc	Rb	Ra
	LATCH								
B7		LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
		W7a8	W7a7	W7a6	W7a5	W7a4	W7a3	W7a2	W7a1
B6		LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
		W6a8	W6a7	W6a6	W6a5	W6a4	W6a3	W6a2	W6a1
B5		LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
		W5a8	W5a7	W5a6	W5a5	W5a4	W5a3	W5a2	W5a1
B4		LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
		W4a8	W4a7	W4a6	W4a5	W4a4	W4a3	W4a2	W4a1
B3		LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
		W3a8	W3a7	W3a6	W3a5	W3a4	W3a3	W3a2	W3a1
B2		LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
		W2a8	W2a7	W2a6	W2a5	W2a4	W2a3	W2a2	W2a1
B1		LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
		W1a8	W1a7	W1a6	W1a5	W1a4	W1a3	W1a2	W1a1
B0		LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0
		W0a8	W0a7	W0a6	W0a5	W0a4	W0a3	W0a2	W0a1

FIG.5

REGISTER		Rh	Rg	Rf	Re	Rd	Rc	Rb	Ra
	LATCH								
B7		LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
		W7c4	W3c4	W7c3	W3c3	W7c2	W3c2	W7c1	W3c1
B6		LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
		W7a4	W3a4	W7a3	W3a3	W7a2	W3a2	W7a1	W3a1
B5		LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
		W6c4	W2c4	W6c3	W2c3	W6c2	W2c2	W6c1	W2c1
B4		LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
		W6a4	W2a4	W6a3	W2a3	W6a2	W2a2	W6a1	W2a1
B3		LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
		W5c4	W1c4	W5c3	W1c3	W5c2	W1c2	W5c1	W1c1
B2		LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
		W5a4	W1a4	W5a3	W1a3	W5a2	W1a2	W5a1	W1a1
B1		LbD7	LbbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
		W4c4	W0c4	W4c3	W0c3	W4c2	W0c2	W4c1	W0c1
B0		LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0
		W4a4	W0a4	W4a3	W0a3	W4a2	W0a2	W4a1	W0a1

FIG.6

REGISTER	Rh	Rg	Rf	Re	Rd	Rc	Rb	Ra
	LATCH							
B7	LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
	W7c8	W3c8	W7c7	W3c7	W7c6	W3c6	W7c5	W3c5
B6	LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
	W7a8	W3a8	W7a7	W3a7	W7a6	W3a6	W7a5	W3a5
B5	LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
	W6c8	W2c8	W6c7	W2c7	W6c6	W2c6	W6c5	W2c5
B4	LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
	W6a8	W2a8	W6a7	W2a7	W6a6	W2a6	W6a5	W2a5
B3	LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
	W5c8	W1c8	W5c7	W1c7	W5c6	W1c6	W5c5	W1c5
B2	LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
	W5a8	W1a8	W5a7	W1a7	W5a6	W1a6	W5a5	W1a5
B1	LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
	W4c8	W0c8	W4c7	W0c7	W4c6	W0c6	W4c5	W0c5
B0	LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0
	W4a8	W0a8	W4a7	W0a7	W4a6	W0a6	W4a5	W0a5

FIG.7

REGISTER	Rh	Rf	Rf	Re	Rd	Rc	Rb	Ra
	LATCH							
B7	LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
	W7a4	W7a3	W7a2	W7a1	W7c4	W7c3	W7c2	W7c1
B6	LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
	W6a4	W6a3	W6a2	W6a1	W6c4	W6c3	W6c2	W6c1
B5	LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
	W5a4	W5a3	W5a2	W5a1	W5c4	W5c3	W5c2	W5c1
B4	LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
	W4a4	W4a3	W4a2	W4a1	W4c4	W4c3	W4c2	W4c1
B3	LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
	W3a4	W3a3	W3a2	W3a1	W3c4	W3c3	W3c2	W3c1
B2	LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
	W2a4	W2a3	W2a2	W2a1	W2c4	W2c3	W2c2	W2c1
B1	LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
	W1a4	W1a3	W1a2	W1a1	W1c4	W1c3	W1c2	W1c1
B0	LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0
	W0a4	W0a3	W0a2	W0a1	W0c4	W0c3	W0c2	W0c1
	MSB				LSB			

FIG.8

REGISTER		Rh	Rg	Rf	Re	Rd	Rc	Rb	Ra
	LATCH								
B7		LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
		W7a8	W7a7	W7a6	W7a5	W7c8	W7c7	W7c6	W7c5
B6		LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
		W6a8	W6a7	W6a6	W6a5	W6c8	W6c7	W6c6	W6c5
B5		LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
		W5a8	W5a7	W5a6	W5a5	W5c8	W5c7	W5c6	W5c5
B4		LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
		W4a8	W4a7	W4a6	W4a5	W4c8	W4c7	W4c6	W4c5
B3		LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
		W3a8	W3a7	W3a6	W3a5	W3c8	W3c7	W3c6	W3c5
B2		LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
		W2a8	W2a7	W2a6	W2a5	W2c8	W2c7	W2c6	W2c5
B1		LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
		W1a8	W1a7	W1a6	W1a5	W1c8	W1c7	W1c6	W1c5
B0		LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0
		W0a8	W0a7	W0a6	W0a5	W0c8	W0c7	W0c6	W0c5

MSB LSB

FIG.9

REGISTER		Rh	Rg	Rf	Re	Rd	Rc	Rb	Ra
	LATCH								
B7		LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
		W7c2	W3c2	W7c1	W3c1	W7d2	W3d2	W7d1	W3d1
B6		LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
		W7a2	W3a2	W7a1	W3a1	W7b2	W3b2	W7b1	W3b1
B5		LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
		W6c2	W2c2	W6c1	W2c1	W6d2	W2d2	W6d1	W2d1
B4		LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
		W6a2	W2a2	W6a1	W2a1	W6b2	W2b2	W6b1	W2b1
B3		LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
		W5c2	W1c2	W5c1	W1c1	W5d2	W1d2	W5d1	W1d1
B2		LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
		W5a2	W1a2	W5a1	W1a1	W5b2	W1b2	W5b1	W1b1
B1		LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
		W4c2	W0c2	W4c1	W0c1	W4d2	W0d2	W4d1	W0d1
B0		LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0
		W4a2	W0a2	W4a1	W0a1	W4b2	W0b2	W4b1	W0b1

MSB LSB

FIG.10

REGISTER		Rh	Rg	Rf	Re	Rd	Rc	Rb	Ra
	LATCH								
B7		LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
		W7c4	W3c4	W7c3	W3c3	W7d4	W3d4	W7d3	W3d3
B6		LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
		W7a4	W3a4	W7a3	W3a3	W7b4	W3b4	W7b3	W3b3
B5		LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
		W6c4	W2c4	W6c3	W2c3	W6d4	W2d4	W6d3	W2d3
B4		LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
		W6a4	W2a4	W6a3	W2a3	W6b4	W2b4	W6b3	W2b3
B3		LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
		W5c4	W1c4	W5c3	W1c3	W5d4	W1d4	W5d3	W1d3
B2		LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
		W5a4	W1a4	W5a3	W1a3	W5b4	W1b4	W5b3	W1b3
B1		LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
		W4c4	W0c4	W4c3	W0C3	W4d4	W0d4	W4d3	W0d3
B0		LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0
		W4a4	W0a4	W4a3	W0a3	W4b4	W0b4	W4b3	W0b3
		MSB				LSB			

FIG.11

REGISTER	Rh	Rg	Rf	Re	Rd	Rc	Rb	Ra
	LATCH							
B7	LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
	W7c6	W3c6	W7c5	W3c5	W7d6	W3d6	W7d5	W3d5
B6	LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
	W7a6	W3a6	W7a5	W3a5	W7b6	W3b6	W7b5	W3b5
B5	LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
	W6c6	W2c6	W6c5	W2c5	W6d6	W2d6	W6d5	W2d5
B4	LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
	W6a6	W2a6	W6a5	W2a5	W6b6	W2b6	W6b5	W2b5
B3	LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
	W5c6	W1c6	W5c5	W1c5	W5d6	W1d6	W5d5	W1d5
B2	LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
	W5a6	W1a6	W5a5	W1a5	W5b6	W1b6	W5b5	W1b5
B1	LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
	W4c6	W0c6	W4c5	W0c5	W4d6	W0d6	W4d5	W0d5
B0	LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0
	W4a6	W0a6	W4a5	W0a5	W4b6	W0b6	W4b5	W0b5
	MSB				LSB			

FIG.12

REGISTER	Rh	Rf	Rf	Re	Rd	Rc	Rb	Ra
	LATCH							
B7	LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
	W7c8	W3c8	W7c7	W3c7	W7d8	W3d8	W7d7	W3d7
B6	LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
	W7a8	W3a8	W7a7	W3a7	W7b8	W3b8	W7b7	W3b7
B5	LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
	W6c8	W2c8	W6c7	W2c7	W6d8	W2d8	W6d7	W2d7
B4	LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
	W6a8	W2a8	W6a7	W2a7	W6b8	W2b8	W6b7	W2b7
B3	LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
	W5c8	W1c8	W5c7	W1c7	W5d8	W1d8	W5d7	W1d7
B2	LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD6	LcD6
	W5a8	W1a8	W5a7	W1a7	W5b8	W1b8	W5b7	W1b7
B1	LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD6	LbD6
	W4c8	W0c8	W4c7	W0c7	W4d8	W0d8	W4d7	W0d7
B0	LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD6	LaD6
	W4a8	W0a8	W4a7	W0a7	W4b8	W0b8	W4b7	W0b7
	MSB				LSB			

FIG.13

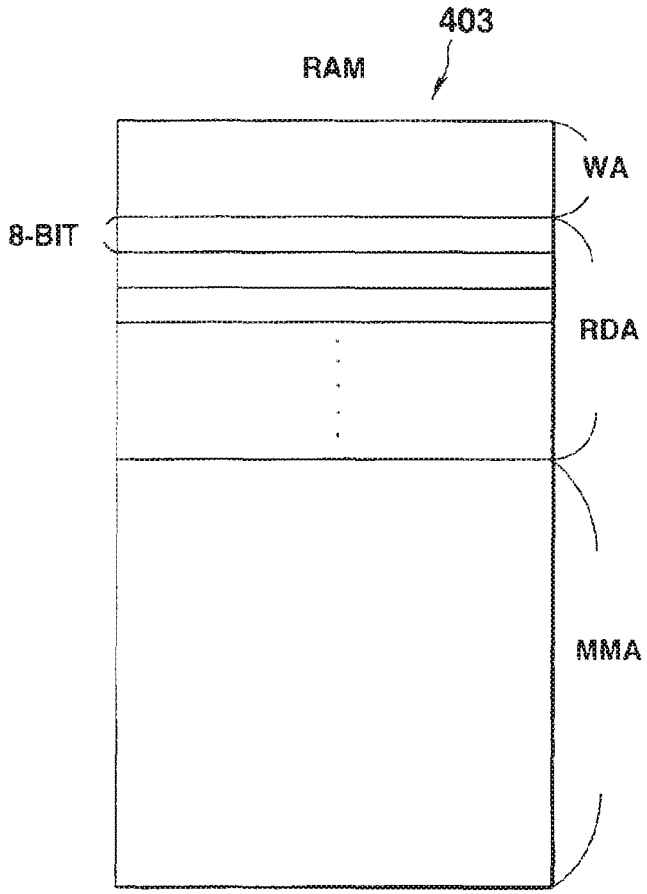


FIG.14

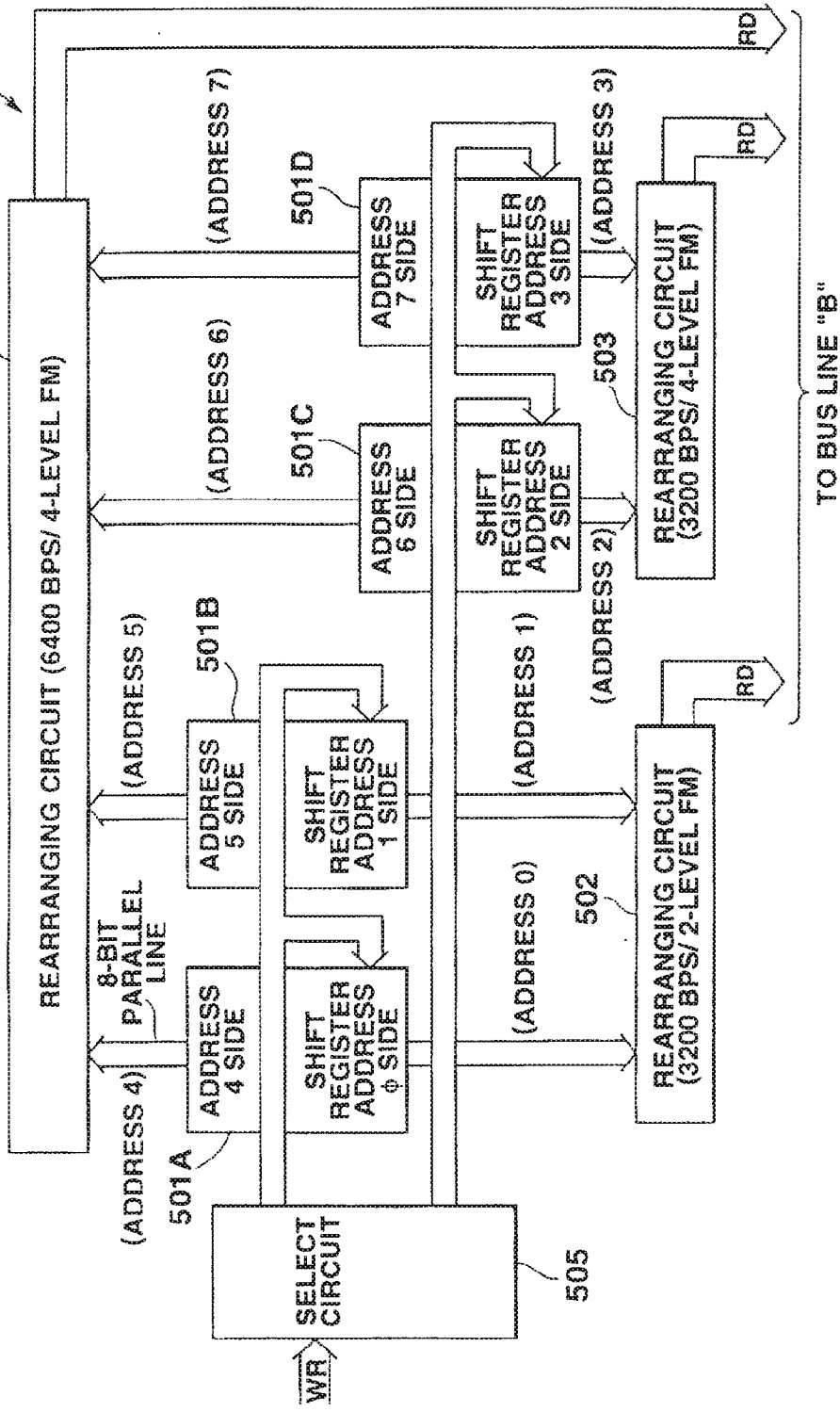

5
504
REARRANGING CIRCUIT (6400 BPS/ 4-LEVEL FM)
8-BIT PARALLEL LINE
(ADDRESS 4)
(ADDRESS 5)
(ADDRESS 6)
(ADDRESS 7)
(ADDRESS 0)
(ADDRESS 1)
(ADDRESS 2)
(ADDRESS 3)
501A
ADDRESS 4 SIDE
501B
ADDRESS 5 SIDE
501C
ADDRESS 6 SIDE
501D
ADDRESS 7 SIDE
SHIFT REGISTER ADDRESS ϕ SIDE
SHIFT REGISTER ADDRESS 1 SIDE
SHIFT REGISTER ADDRESS 2 SIDE
SHIFT REGISTER ADDRESS 3 SIDE
502
REARRANGING CIRCUIT (3200 BPS/ 2-LEVEL FM)
503
REARRANGING CIRCUIT (3200 BPS/ 4-LEVEL FM)
505
SELECT CIRCUIT
WR
RD
RD
RD
TO BUS LINE "B"

FIG.15

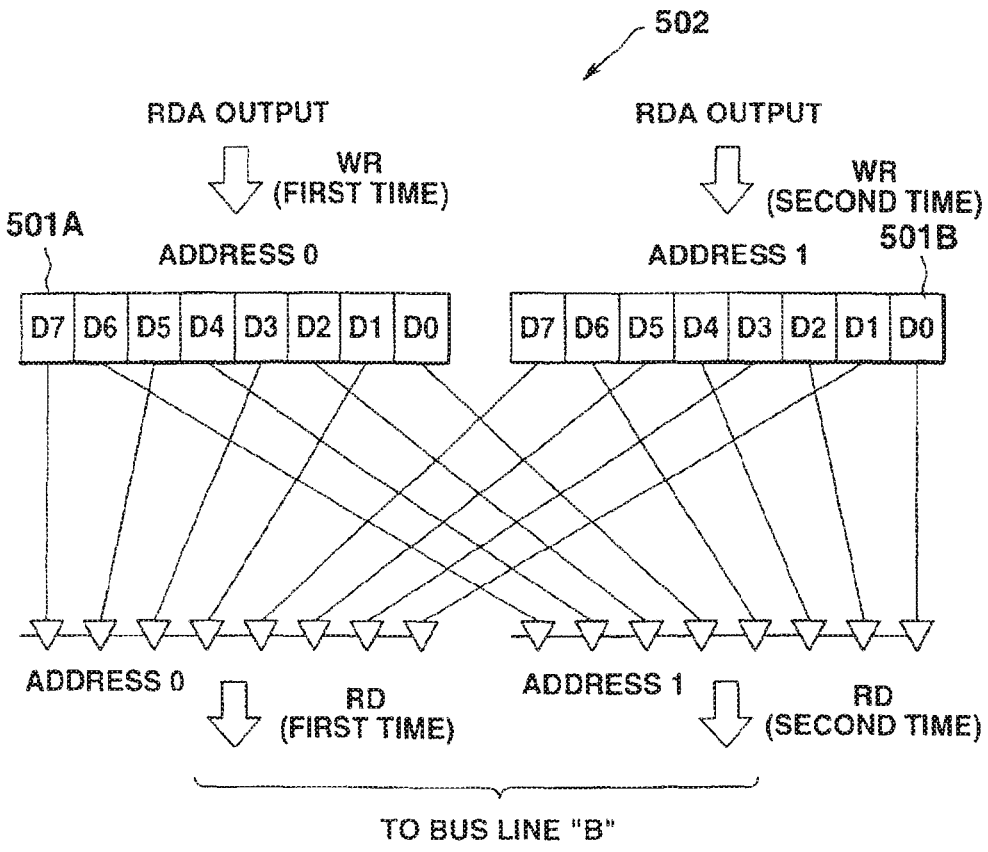

502
RDA OUTPUT
RDA OUTPUT
WR
(FIRST TIME)
WR
(SECOND TIME)
501A
501B
ADDRESS 0
ADDRESS 1
D7 D6 D5 D4 D3 D2 D1 D0
D7 D6 D5 D4 D3 D2 D1 D0
ADDRESS 0
ADDRESS 1
RD
(FIRST TIME)
RD
(SECOND TIME)
TO BUS LINE "B"

FIG.16

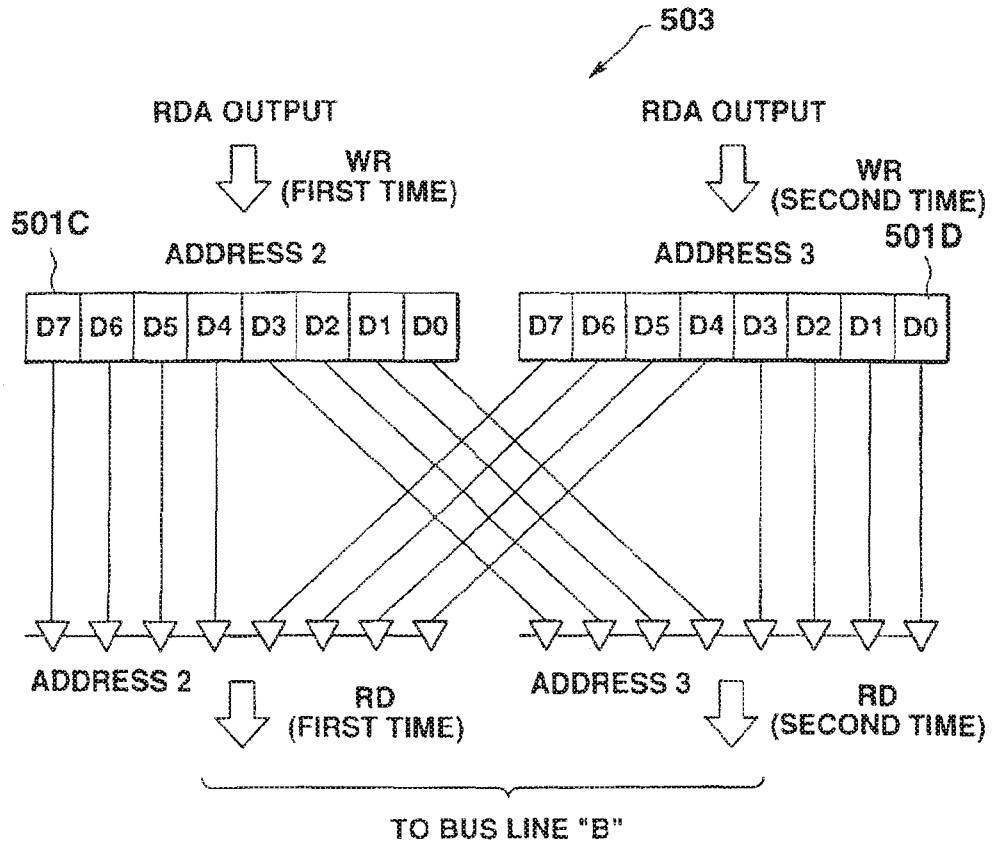

503
RDA OUTPUT
WR
(FIRST TIME)
RDA OUTPUT
WR
(SECOND TIME)
501C
ADDRESS 2
ADDRESS 3
501D
D7 D6 D5 D4 D3 D2 D1 D0
D7 D6 D5 D4 D3 D2 D1 D0
ADDRESS 2
RD
(FIRST TIME)
ADDRESS 3
RD
(SECOND TIME)
TO BUS LINE "B"

FIG.17

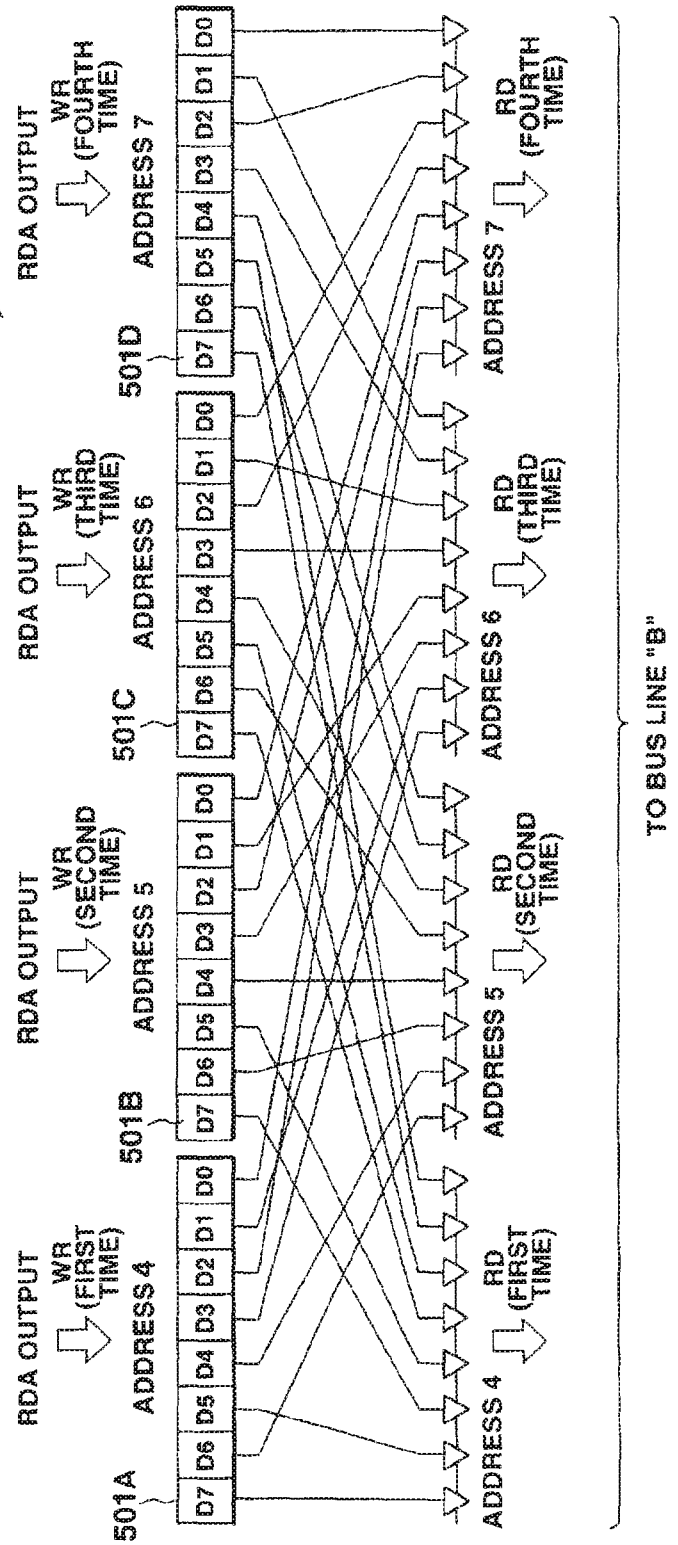


FIG.18

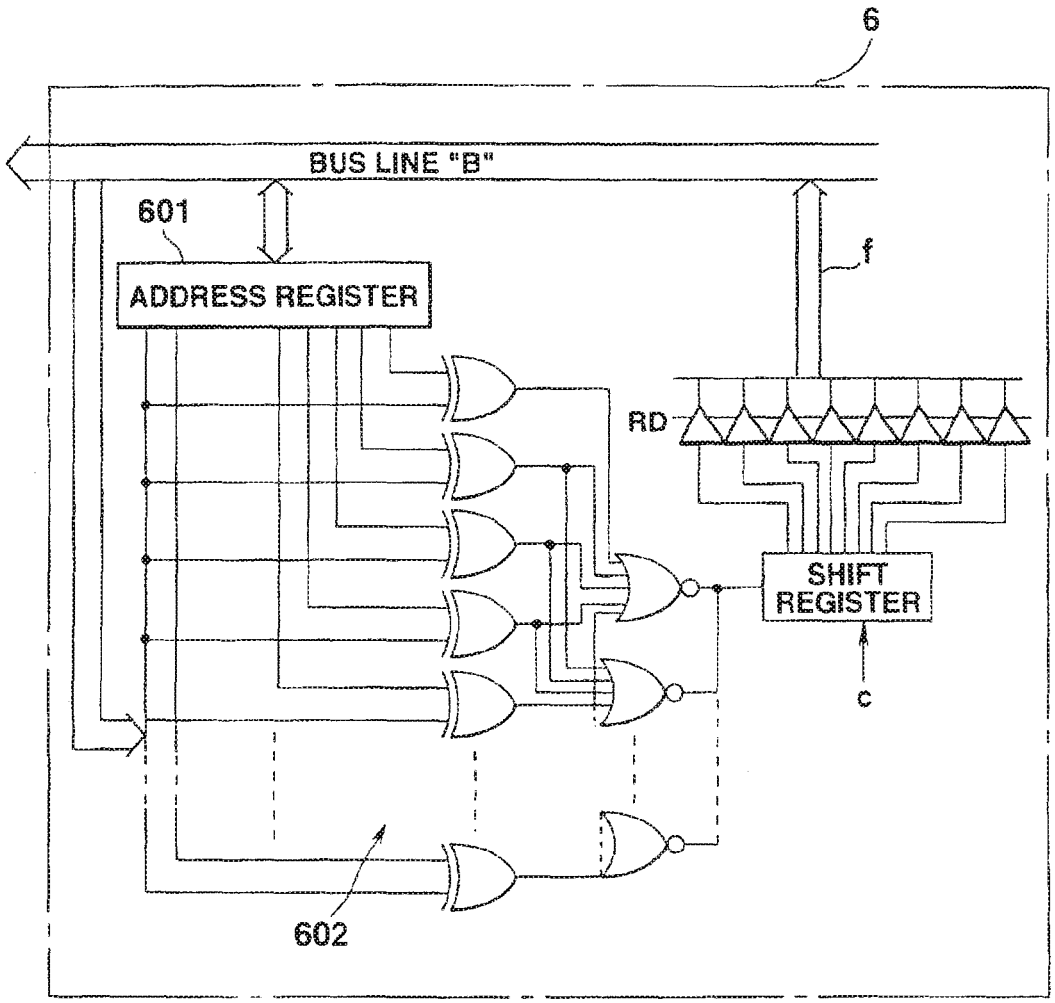


FIG.19A

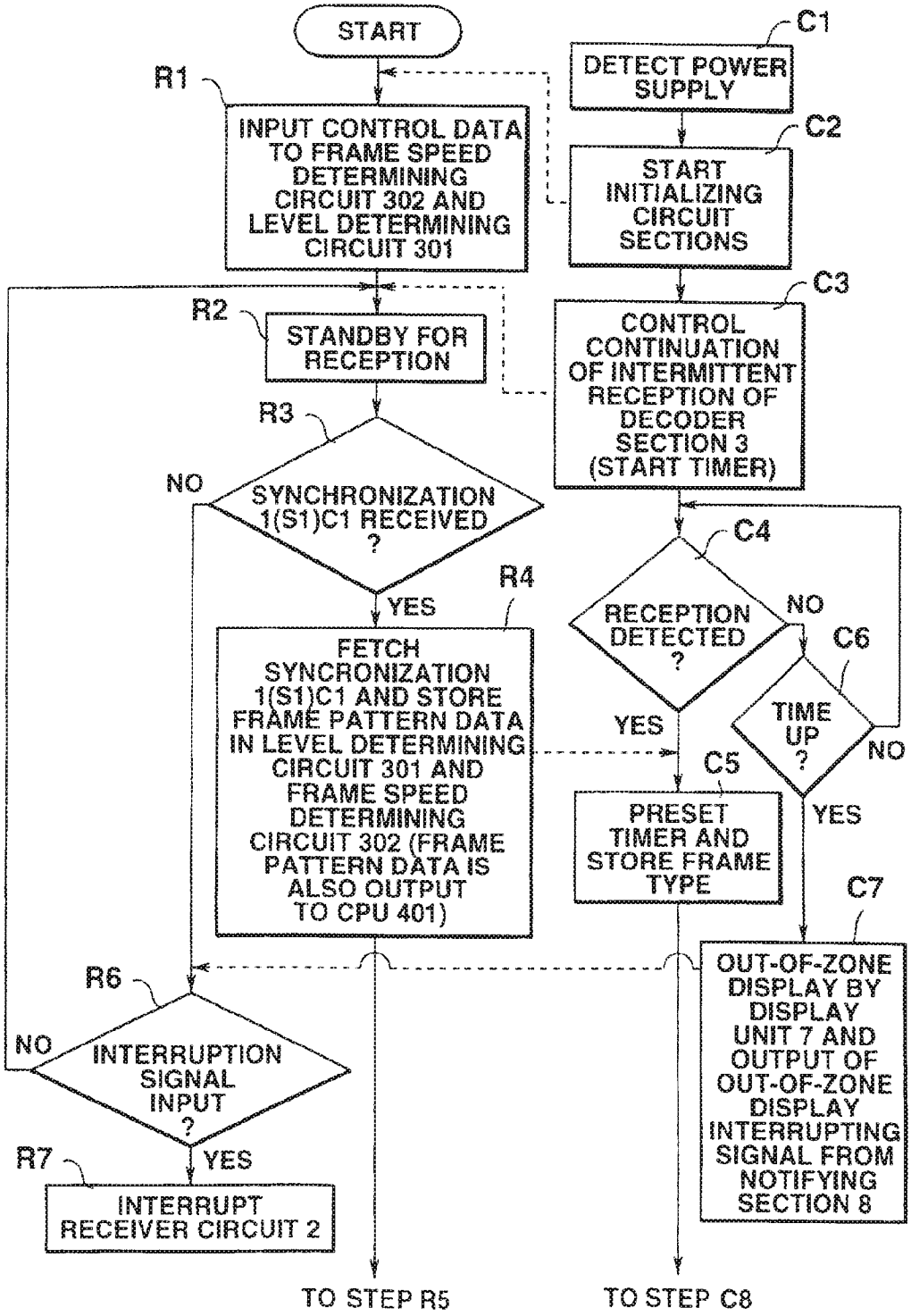


FIG.19B

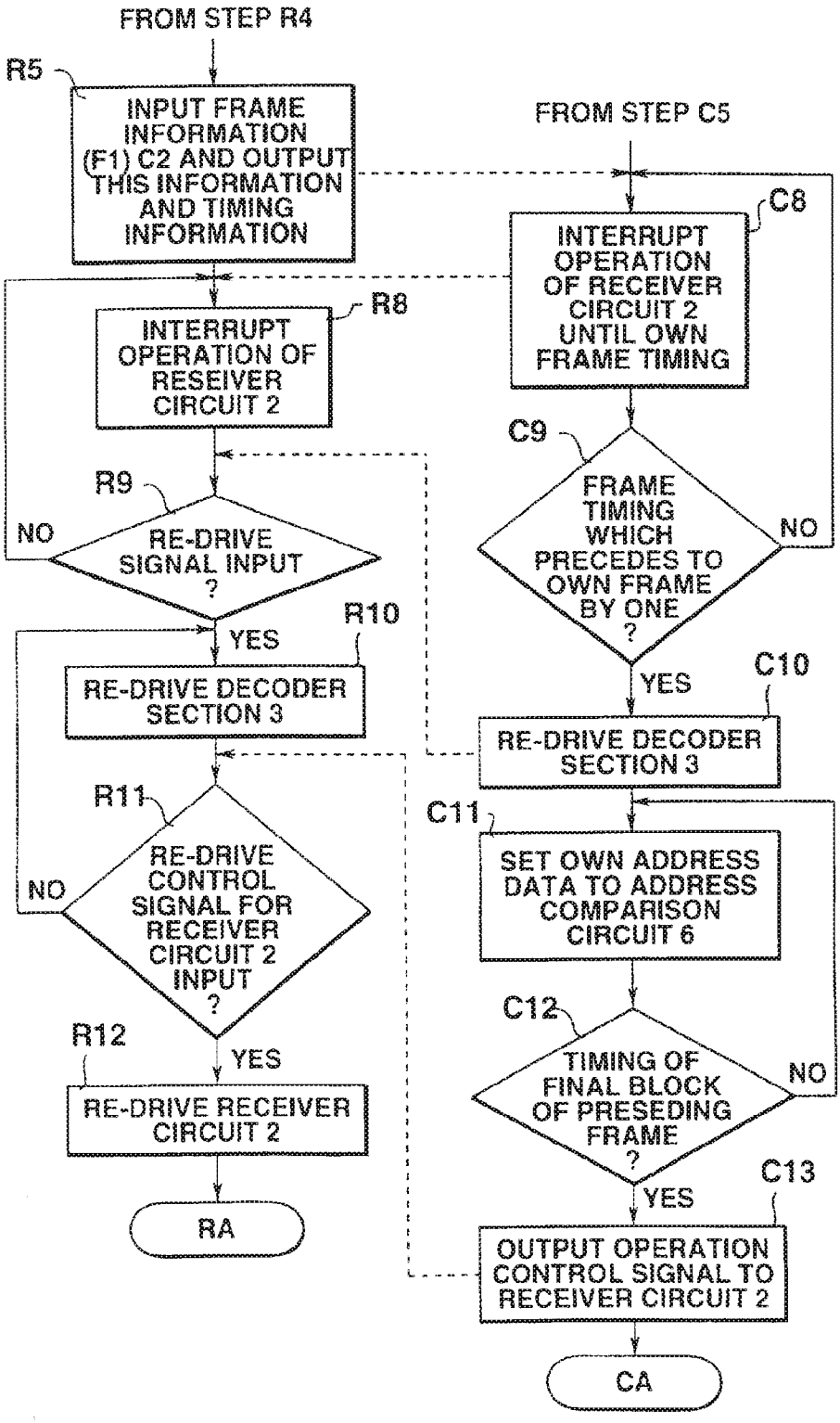

FROM STEP R4
R5
INPUT FRAME INFORMATION (F1) C2 AND OUTPUT THIS INFORMATION AND TIMING INFORMATION
R8
INTERRUPT OPERATION OF RESEIVER CIRCUIT 2
R9
RE-DRIVE SIGNAL INPUT ?
NO
YES
R10
RE-DRIVE DECODER SECTION 3
R11
RE-DRIVE CONTROL SIGNAL FOR RECEIVER CIRCUIT 2 INPUT ?
NO
R12
YES
RE-DRIVE RECEIVER CIRCUIT 2
RA
FROM STEP C5
C8
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2 UNTIL OWN FRAME TIMING
C9
FRAME TIMING WHICH PRECEDES TO OWN FRAME BY ONE ?
NO
YES
C10
RE-DRIVE DECODER SECTION 3
C11
SET OWN ADDRESS DATA TO ADDRESS COMPARISON CIRCUIT 6
C12
TIMING OF FINAL BLOCK OF PRESEDING FRAME ?
NO
YES
C13
OUTPUT OPERATION CONTROL SIGNAL TO RECEIVER CIRCUIT 2
CA

FIG.20

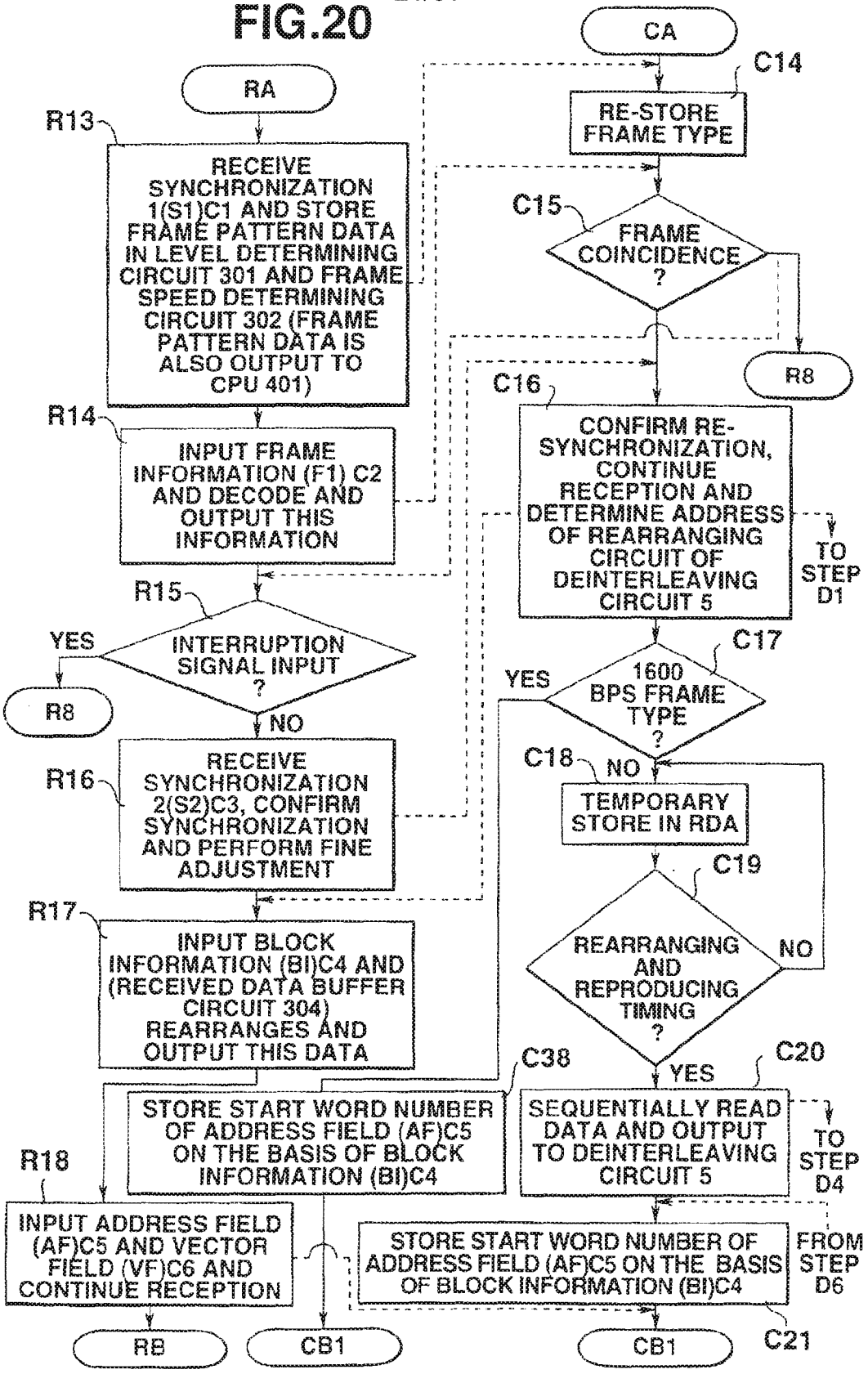

CA
C14
RE-STORE FRAME TYPE
C15
FRAME COINCIDENCE ?
R8
C16
CONFIRM RE-SYNCHRONIZATION, CONTINUE RECEPTION AND DETERMINE ADDRESS OF REARRANGING CIRCUIT OF DEINTERLEAVING CIRCUIT 5
TO STEP D1
C17
1600 BPS FRAME TYPE ?
YES
NO
C18
TEMPORARY STORE IN RDA
C19
REARRANGING AND REPRODUCING TIMING ?
NO
YES
C20
SEQUENTIALLY READ DATA AND OUTPUT TO DEINTERLEAVING CIRCUIT 5
TO STEP D4
C38
STORE START WORD NUMBER OF ADDRESS FIELD (AF)C5 ON THE BASIS OF BLOCK INFORMATION (BI)C4
FROM STEP D6
STORE START WORD NUMBER OF ADDRESS FIELD (AF)C5 ON THE BASIS OF BLOCK INFORMATION (BI)C4
C21
CB1
CB1
RA
R13
RECEIVE SYNCHRONIZATION 1(S1)C1 AND STORE FRAME PATTERN DATA IN LEVEL DETERMINING CIRCUIT 301 AND FRAME SPEED DETERMINING CIRCUIT 302 (FRAME PATTERN DATA IS ALSO OUTPUT TO CPU 401)
R14
INPUT FRAME INFORMATION (F1) C2 AND DECODE AND OUTPUT THIS INFORMATION
R15
INTERRUPTION SIGNAL INPUT ?
YES
R8
NO
R16
RECEIVE SYNCHRONIZATION 2(S2)C3, CONFIRM SYNCHRONIZATION AND PERFORM FINE ADJUSTMENT
R17
INPUT BLOCK INFORMATION (BI)C4 AND (RECEIVED DATA BUFFER CIRCUIT 304) REARRANGES AND OUTPUT THIS DATA
R18
INPUT ADDRESS FIELD (AF)C5 AND VECTOR FIELD (VF)C6 AND CONTINUE RECEPTION
RB
CB1

FIG.21A

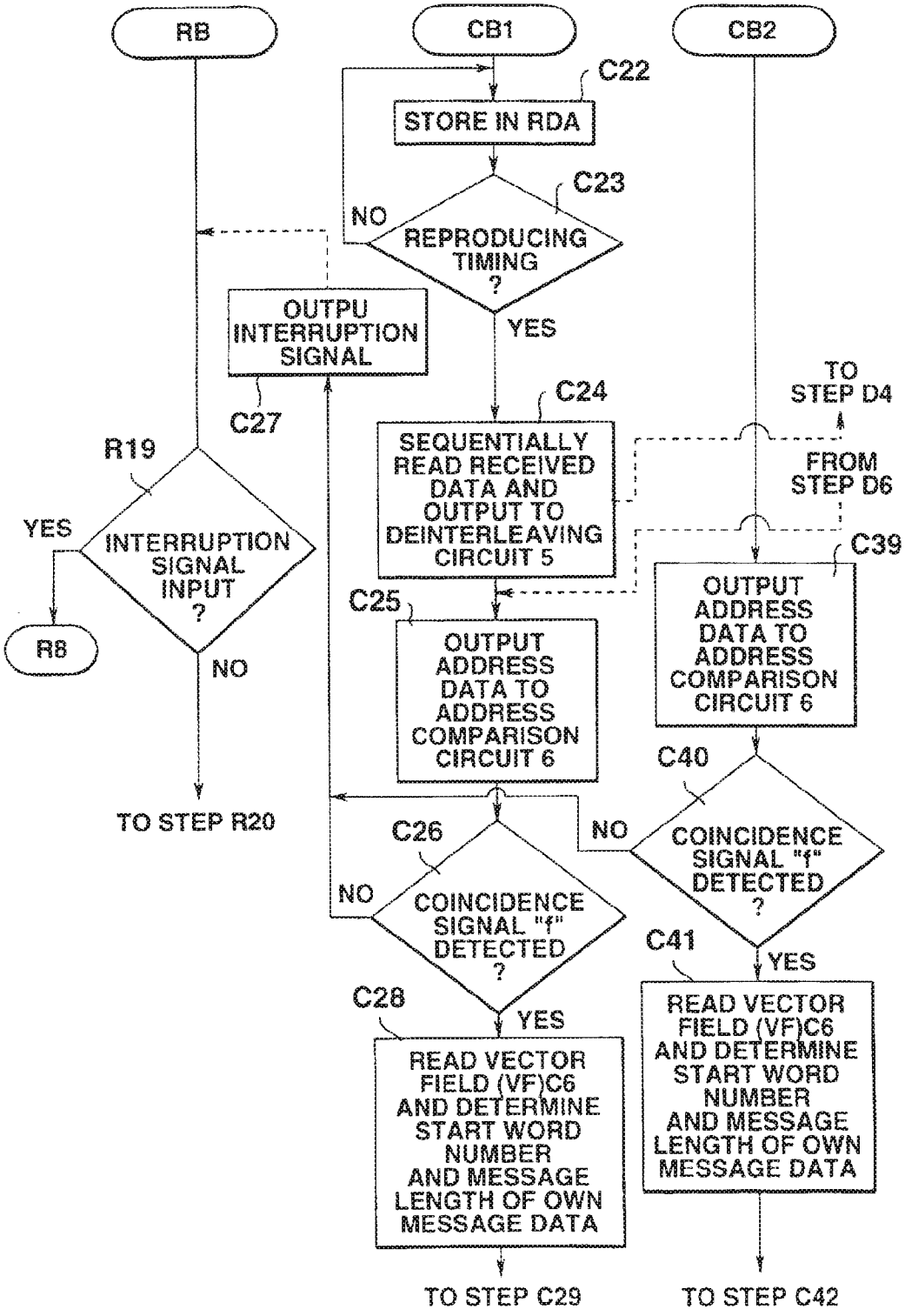

RB
CB1
CB2
C22
STORE IN RDA
C23
NO
REPRODUCING TIMING ?
YES
OUTPU INTERRUPTION SIGNAL
C27
C24
SEQUENTIALLY READ RECEIVED DATA AND OUTPUT TO DEINTERLEAVING CIRCUIT 5
TO STEP D4
FROM STEP D6
R19
YES
INTERRUPTION SIGNAL INPUT ?
R8
NO
TO STEP R20
C25
OUTPUT ADDRESS DATA TO ADDRESS COMPARISON CIRCUIT 6
C39
OUTPUT ADDRESS DATA TO ADDRESS COMPARISON CIRCUIT 6
C40
NO
COINCIDENCE SIGNAL "f" DETECTED ?
C26
NO
COINCIDENCE SIGNAL "f" DETECTED ?
C41
YES
C28
YES
READ VECTOR FIELD (VF)C6 AND DETERMINE START WORD NUMBER AND MESSAGE LENGTH OF OWN MESSAGE DATA
READ VECTOR FIELD (VF)C6 AND DETERMINE START WORD NUMBER AND MESSAGE LENGTH OF OWN MESSAGE DATA
TO STEP C29
TO STEP C42

FIG.21B

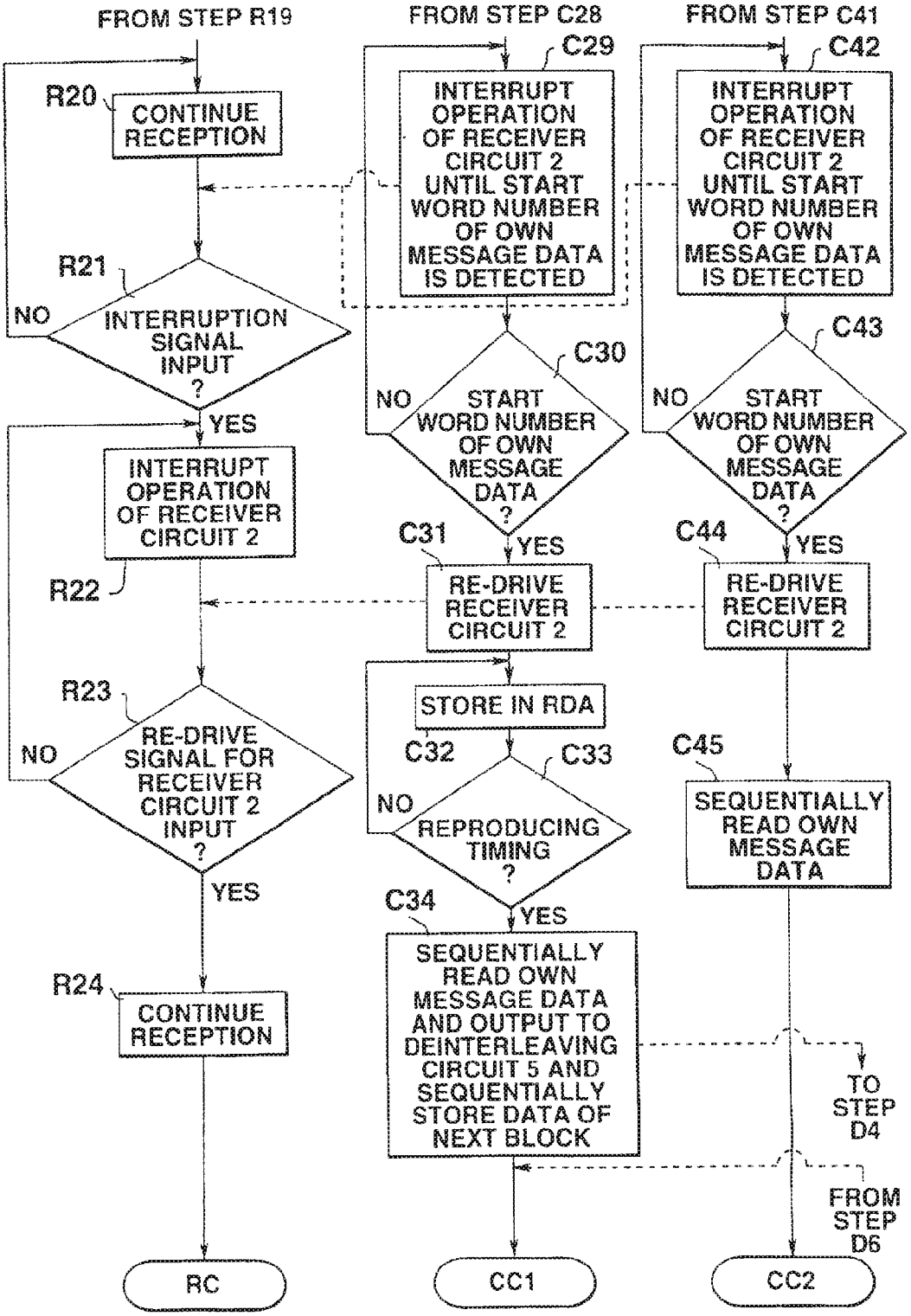

FROM STEP R19
FROM STEP C28
FROM STEP C41
R20
CONTINUE RECEPTION
C29
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2 UNTIL START WORD NUMBER OF OWN MESSAGE DATA IS DETECTED
C42
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2 UNTIL START WORD NUMBER OF OWN MESSAGE DATA IS DETECTED
R21
NO
INTERRUPTION SIGNAL INPUT ?
YES
C30
NO
START WORD NUMBER OF OWN MESSAGE DATA ?
C43
NO
START WORD NUMBER OF OWN MESSAGE DATA ?
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2
C31
YES
C44
YES
R22
RE-DRIVE RECEIVER CIRCUIT 2
RE-DRIVE RECEIVER CIRCUIT 2
R23
STORE IN RDA
C32
C33
C45
NO
RE-DRIVE SIGNAL FOR RECEIVER CIRCUIT 2 INPUT ?
NO
REPRODUCING TIMING ?
SEQUENTIALLY READ OWN MESSAGE DATA
YES
C34
YES
R24
CONTINUE RECEPTION
SEQUENTIALLY READ OWN MESSAGE DATA AND OUTPUT TO DEINTERLEAVING CIRCUIT 5 AND SEQUENTIALLY STORE DATA OF NEXT BLOCK
TO STEP D4
FROM STEP D6
RC
CC1
CC2

FIG.22

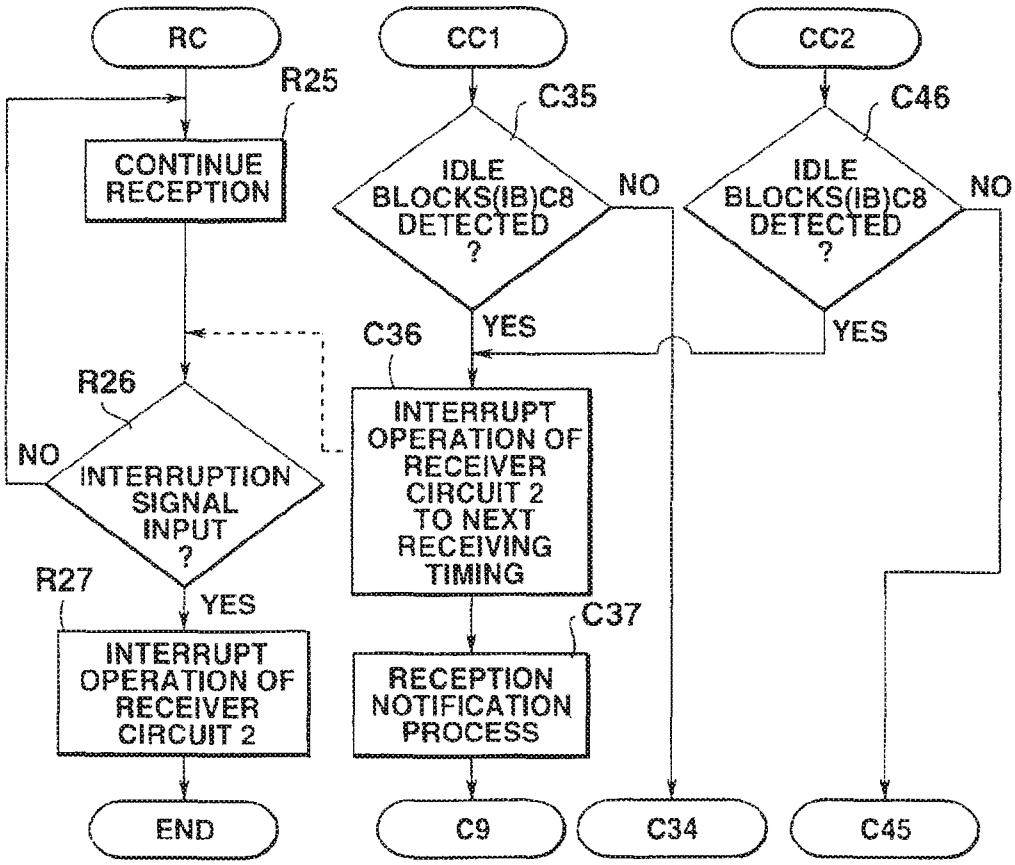
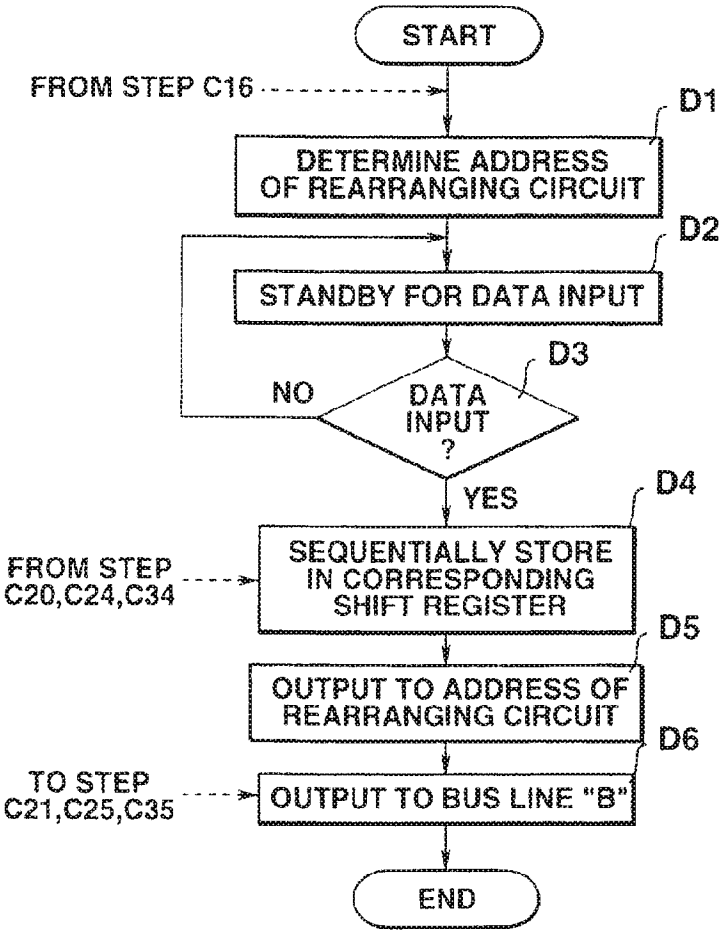

RC
R25
CONTINUE RECEPTION
R26
NO
INTERRUPTION SIGNAL INPUT ?
R27
YES
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2
END
CC1
C35
IDLE BLOCKS(IB)C8 DETECTED ?
NO
YES
C36
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2 TO NEXT RECEIVING TIMING
C37
RECEPTION NOTIFICATION PROCESS
C9
C34
CC2
C46
IDLE BLOCKS(IB)C8 DETECTED ?
NO
YES
C45

FIG.23


START
FROM STEP C16
D1
DETERMINE ADDRESS OF REARRANGING CIRCUIT
D2
STANDBY FOR DATA INPUT
D3
NO
DATA INPUT ?
YES
D4
FROM STEP C20,C24,C34
SEQUENTIALLY STORE IN CORRESPONDING SHIFT REGISTER
D5
OUTPUT TO ADDRESS OF REARRANGING CIRCUIT
D6
TO STEP C21,C25,C35
OUTPUT TO BUS LINE "B"
END

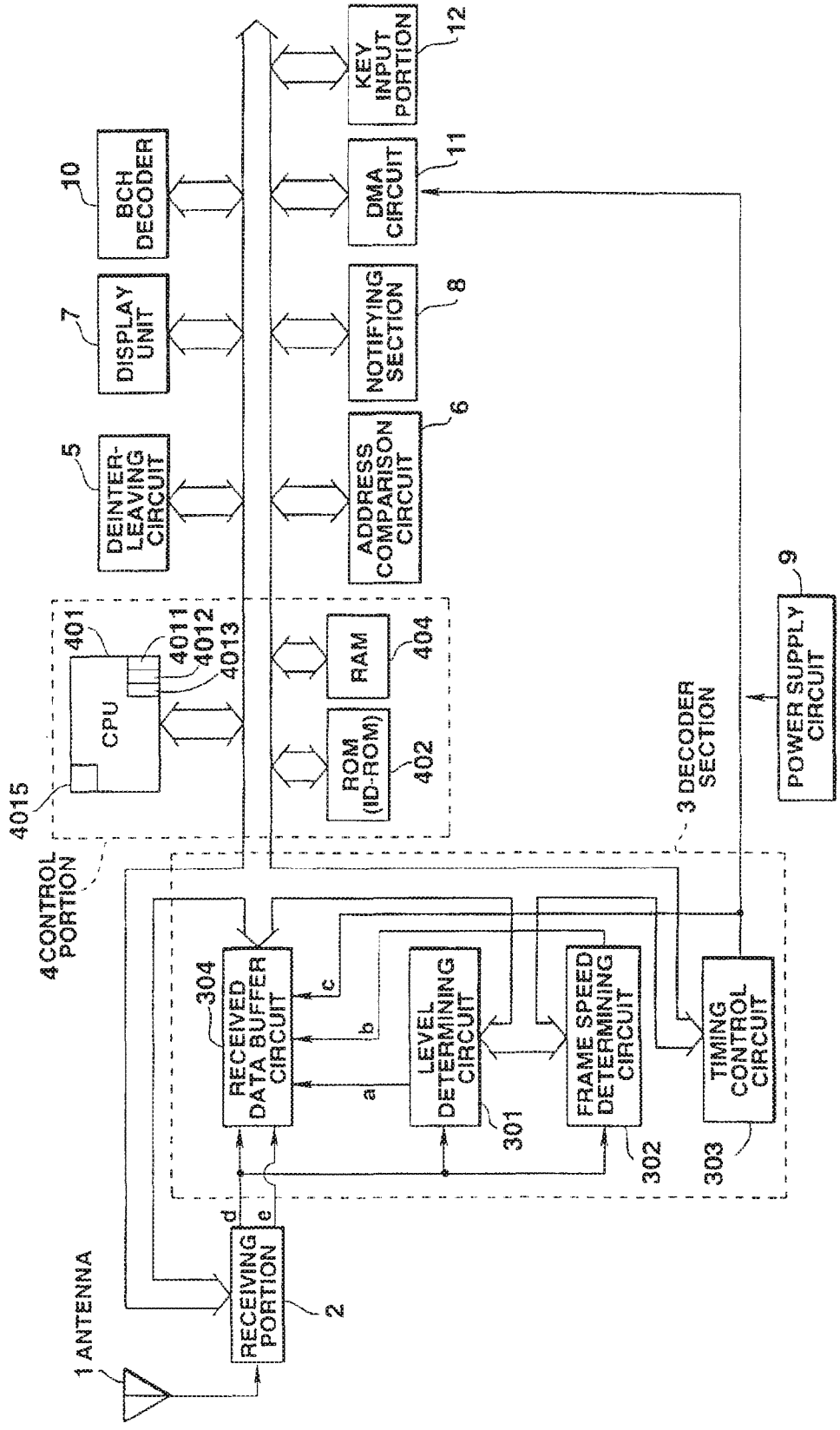

1 ANTENNA
RECEIVING PORTION
2
4 CONTROL PORTION
3 DECODER SECTION
RECEIVED DATA BUFFER CIRCUIT
304
LEVEL DETERMINING CIRCUIT
301
FRAME SPEED DETERMINING CIRCUIT
302
TIMING CONTROL CIRCUIT
303
a
b
c
d
e
CPU
401
4011
4012
4013
4015
ROM (ID-ROM)
402
RAM
404
DEINTER-LEAVING CIRCUIT
5
ADDRESS COMPARISON CIRCUIT
6
DISPLAY UNIT
7
NOTIFYING SECTION
8
POWER SUPPLY CIRCUIT
9
BCH DECODER
10
DMA CIRCUIT
11
KEY INPUT PORTION
12

FIG.24

FIG.25

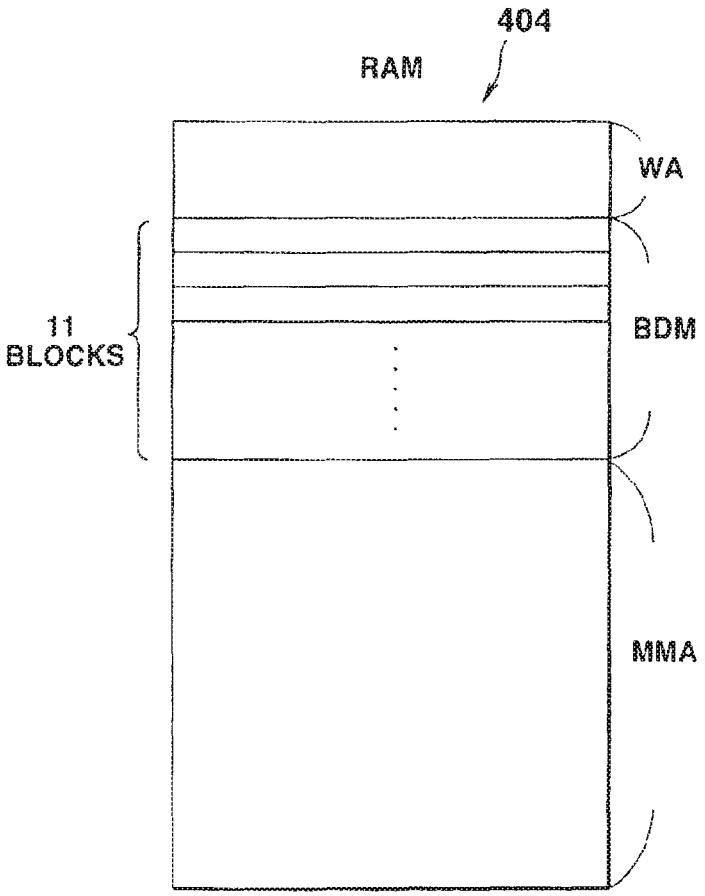


FIG.26A

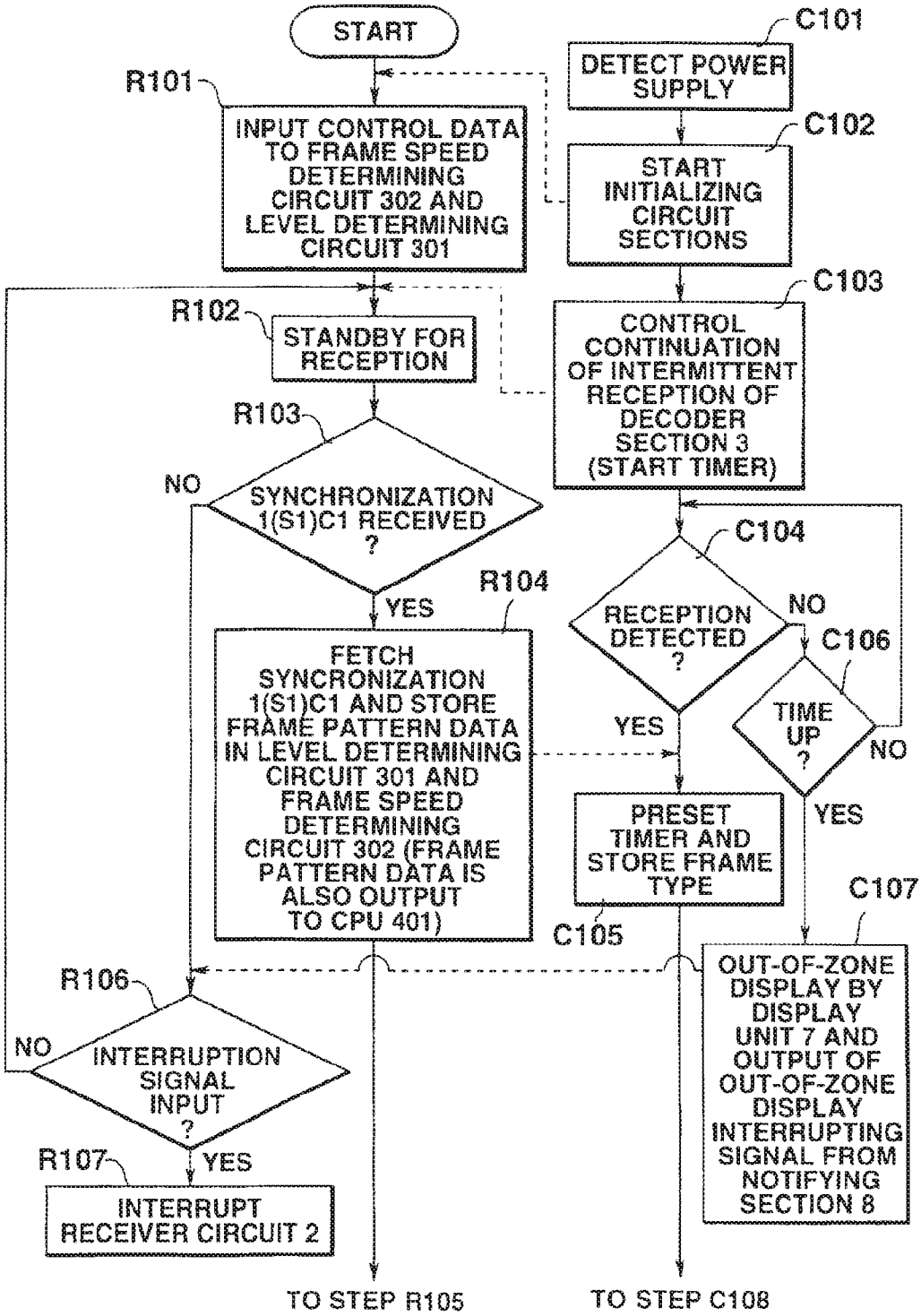
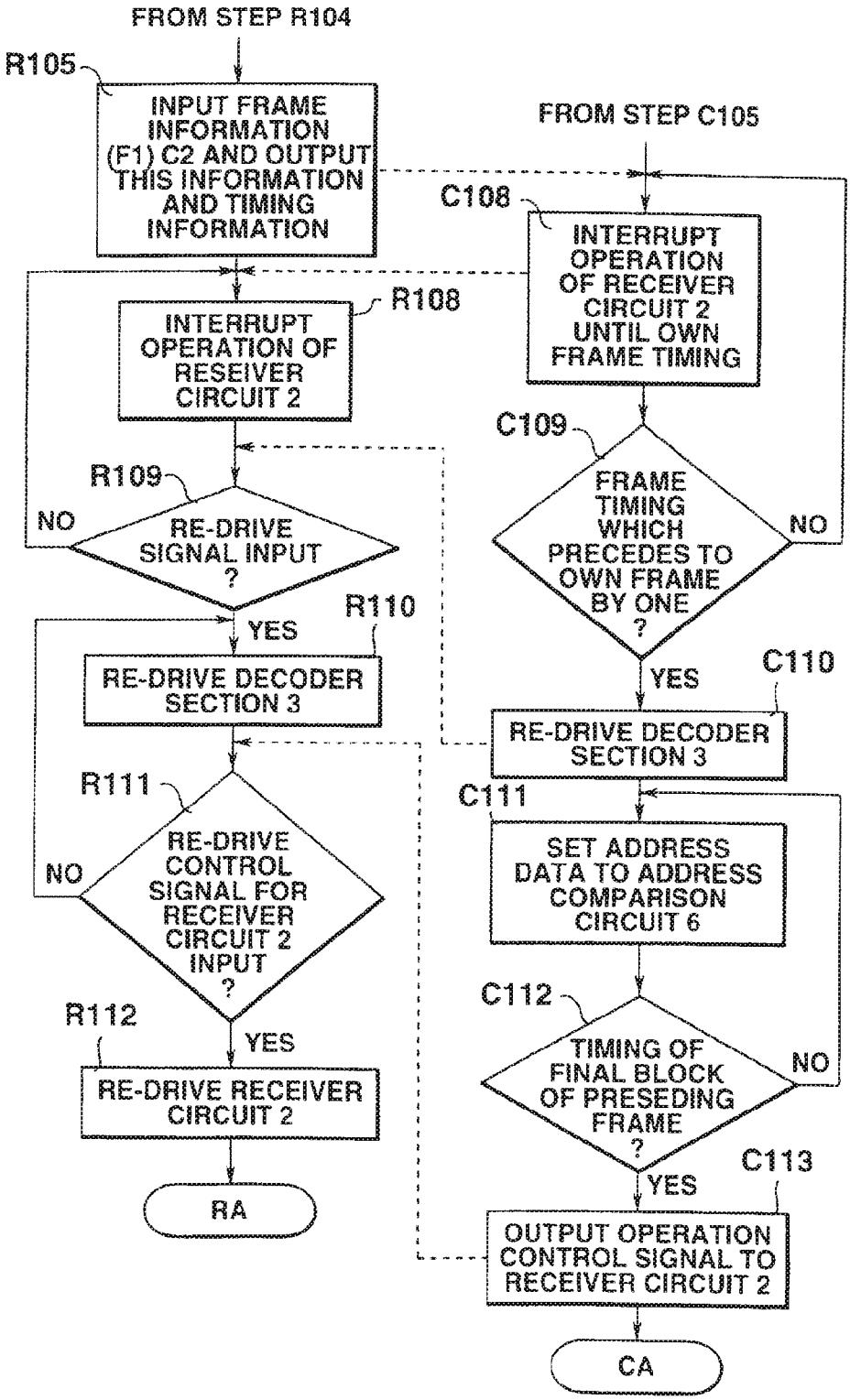

START
C101
DETECT POWER SUPPLY
R101
INPUT CONTROL DATA TO FRAME SPEED DETERMINING CIRCUIT 302 AND LEVEL DETERMINING CIRCUIT 301
C102
START INITIALIZING CIRCUIT SECTIONS
C103
CONTROL CONTINUATION OF INTERMITTENT RECEPTION OF DECODER SECTION 3 (START TIMER)
R102
STANDBY FOR RECEPTION
R103
SYNCHRONIZATION 1(S1)C1 RECEIVED ?
NO
YES
R104
FETCH SYNCRONIZATION 1(S1)C1 AND STORE FRAME PATTERN DATA IN LEVEL DETERMINING CIRCUIT 301 AND FRAME SPEED DETERMINING CIRCUIT 302 (FRAME PATTERN DATA IS ALSO OUTPUT TO CPU 401)
C104
RECEPTION DETECTED ?
NO
YES
C106
TIME UP ?
NO
YES
PRESET TIMER AND STORE FRAME TYPE
C105
C107
OUT-OF-ZONE DISPLAY BY DISPLAY UNIT 7 AND OUTPUT OF OUT-OF-ZONE DISPLAY INTERRUPTING SIGNAL FROM NOTIFYING SECTION 8
R106
INTERRUPTION SIGNAL INPUT ?
NO
R107
YES
INTERRUPT RECEIVER CIRCUIT 2
TO STEP R105
TO STEP C108

FIG.26B


FROM STEP R104
R105
INPUT FRAME INFORMATION (F1) C2 AND OUTPUT THIS INFORMATION AND TIMING INFORMATION
R108
INTERRUPT OPERATION OF RESEIVER CIRCUIT 2
R109
RE-DRIVE SIGNAL INPUT ?
NO
YES
R110
RE-DRIVE DECODER SECTION 3
R111
RE-DRIVE CONTROL SIGNAL FOR RECEIVER CIRCUIT 2 INPUT ?
NO
R112
YES
RE-DRIVE RECEIVER CIRCUIT 2
RA
FROM STEP C105
C108
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2 UNTIL OWN FRAME TIMING
C109
FRAME TIMING WHICH PRECEDES TO OWN FRAME BY ONE ?
NO
YES
C110
RE-DRIVE DECODER SECTION 3
C111
SET ADDRESS DATA TO ADDRESS COMPARISON CIRCUIT 6
C112
TIMING OF FINAL BLOCK OF PRESEDING FRAME ?
NO
YES
C113
OUTPUT OPERATION CONTROL SIGNAL TO RECEIVER CIRCUIT 2
CA

30/38

FIG.27

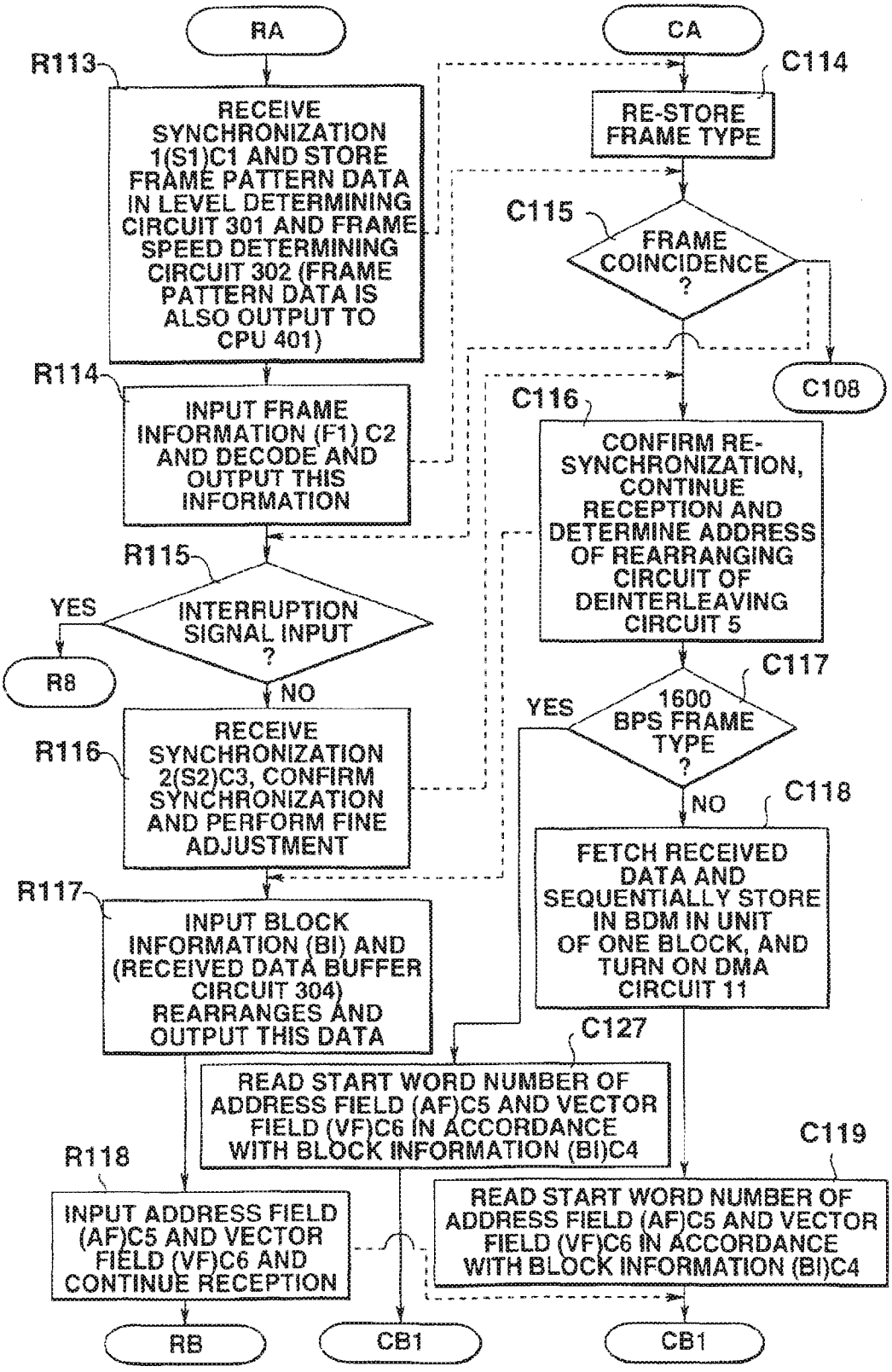


FIG.28

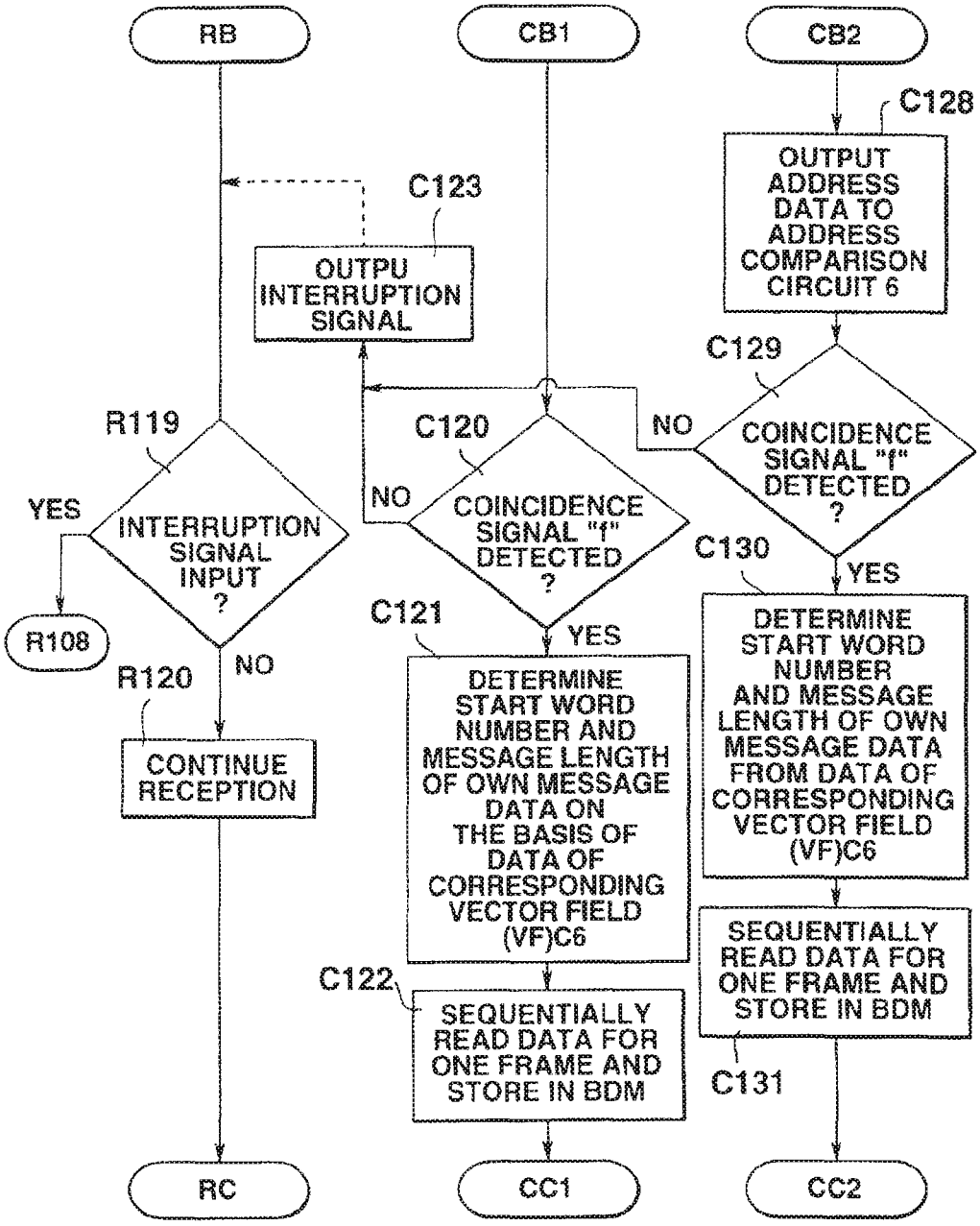

RB
CB1
CB2
C128
OUTPUT ADDRESS DATA TO ADDRESS COMPARISON CIRCUIT 6
C123
OUTPU INTERRUPTION SIGNAL
C129
COINCIDENCE SIGNAL "f" DETECTED ?
NO
YES
R119
INTERRUPTION SIGNAL INPUT ?
C120
COINCIDENCE SIGNAL "f" DETECTED ?
NO
YES
C130
YES
R108
C121
YES
DETERMINE START WORD NUMBER AND MESSAGE LENGTH OF OWN MESSAGE DATA ON THE BASIS OF DATA OF CORRESPONDING VECTOR FIELD (VF)C6
DETERMINE START WORD NUMBER AND MESSAGE LENGTH OF OWN MESSAGE DATA FROM DATA OF CORRESPONDING VECTOR FIELD (VF)C6
R120
NO
CONTINUE RECEPTION
C122
SEQUENTIALLY READ DATA FOR ONE FRAME AND STORE IN BDM
SEQUENTIALLY READ DATA FOR ONE FRAME AND STORE IN BDM
C131
RC
CC1
CC2

FIG.29

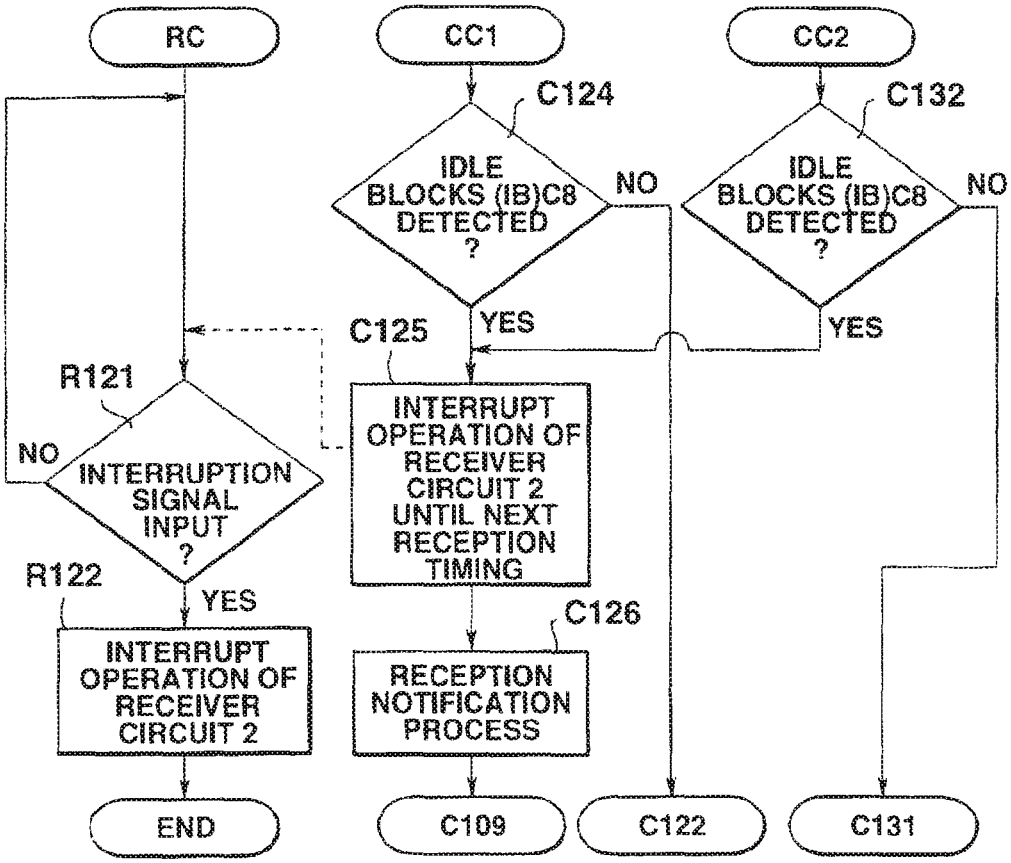

RC
CC1
CC2
C124
C132
IDLE BLOCKS (IB)C8 DETECTED ?
NO
YES
C125
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2 UNTIL NEXT RECEPTION TIMING
R121
INTERRUPTION SIGNAL INPUT ?
R122
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2
C126
RECEPTION NOTIFICATION PROCESS
END
C109
C122
C131

FIG.30

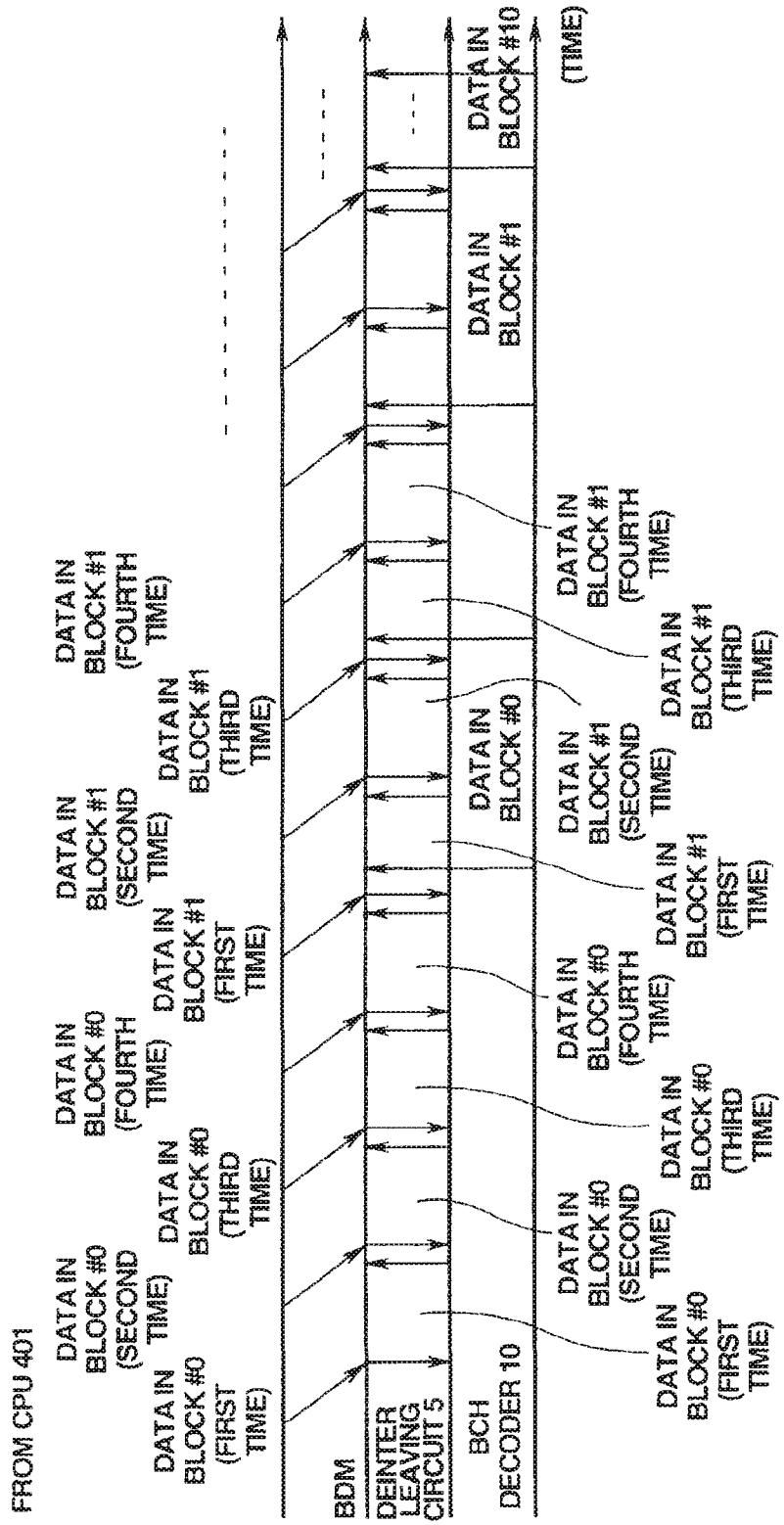

FROM CPU 401
BDM
DEINTER LEAVING CIRCUIT 5
BCH DECODER 10
DATA IN BLOCK #0 (FIRST TIME)
DATA IN BLOCK #0 (SECOND TIME)
DATA IN BLOCK #0 (THIRD TIME)
DATA IN BLOCK #0 (FOURTH TIME)
DATA IN BLOCK #1 (FIRST TIME)
DATA IN BLOCK #1 (SECOND TIME)
DATA IN BLOCK #1 (THIRD TIME)
DATA IN BLOCK #1 (FOURTH TIME)
DATA IN BLOCK #0
DATA IN BLOCK #1
DATA IN BLOCK #10
(TIME)

FIG.31

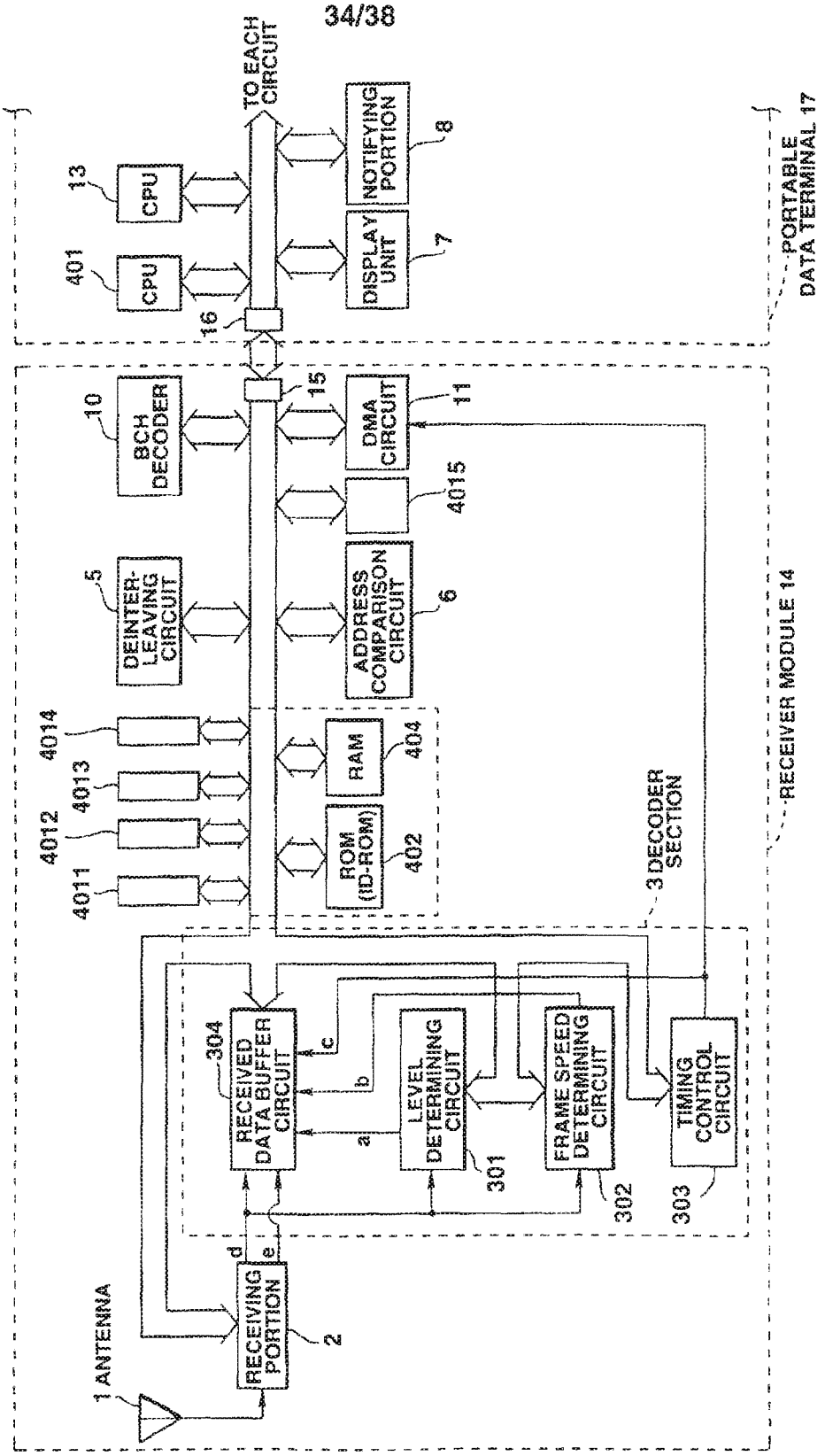

TO EACH CIRCUIT
NOTIFYING PORTION
8
DISPLAY UNIT
7
CPU
13
CPU
401
16
PORTABLE DATA TERMINAL 17
15
BCH DECODER
10
DMA CIRCUIT
11
4015
DEINTER-LEAVING CIRCUIT
5
ADDRESS COMPARISON CIRCUIT
6
4014
4013
4012
4011
RAM
404
ROM (ID-ROM)
402
3 DECODER SECTION
RECEIVER MODULE 14
RECEIVED DATA BUFFER CIRCUIT
304
LEVEL DETERMINING CIRCUIT
301
FRAME SPEED DETERMINING CIRCUIT
302
TIMING CONTROL CIRCUIT
303
a
b
c
d
e
RECEIVING PORTION
2
1 ANTENNA

FIG.32

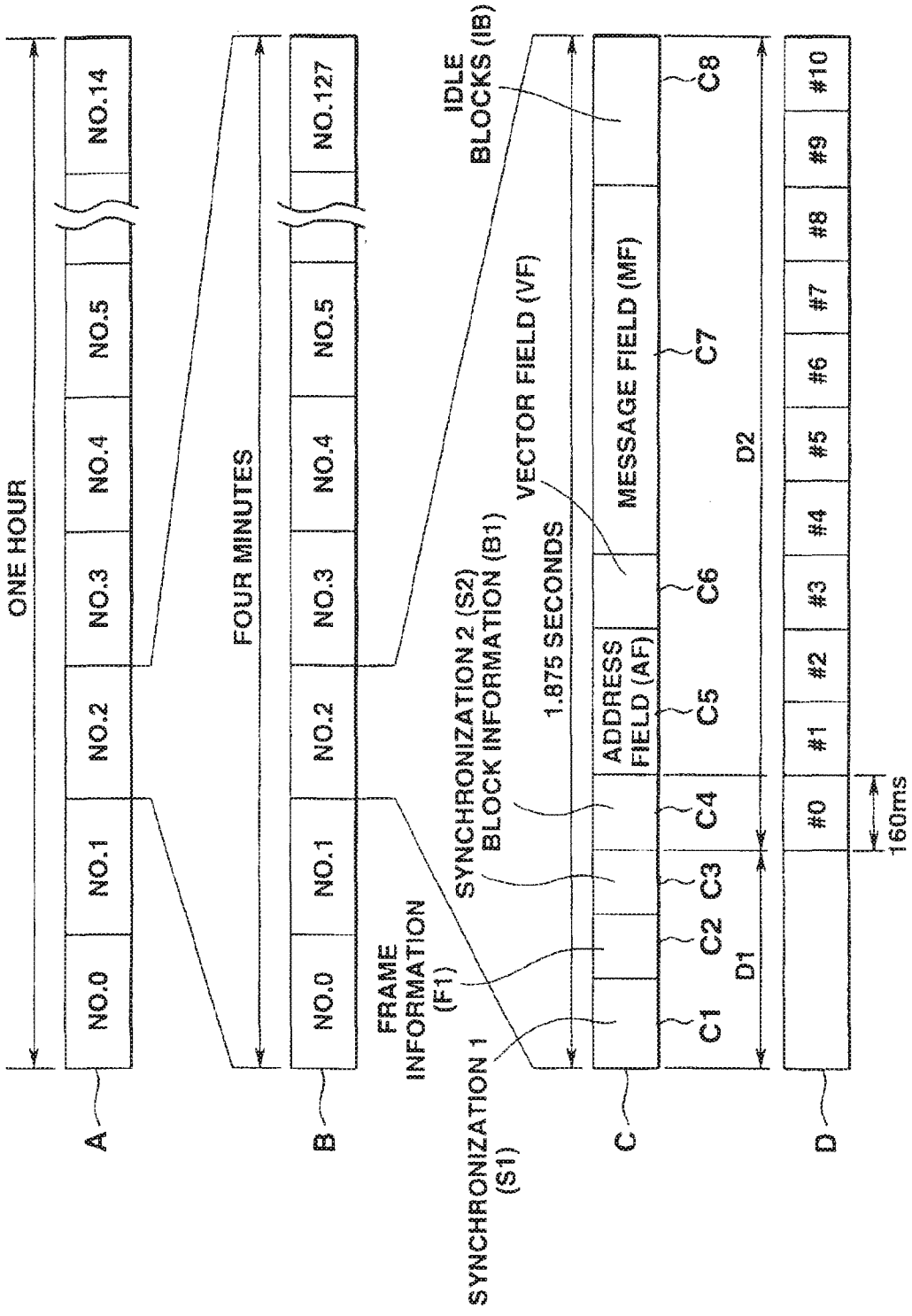

ONE HOUR
FOUR MINUTES
NO.0
NO.1
NO.2
NO.3
NO.4
NO.5
NO.14
NO.127
A
B
C
D
FRAME INFORMATION (F1)
SYNCHRONIZATION 1 (S1)
SYNCHRONIZATION 2 (S2) BLOCK INFORMATION (B1)
1.875 SECONDS
VECTOR FIELD (VF)
ADDRESS FIELD (AF)
MESSAGE FIELD (MF)
IDLE BLOCKS (IB)
C1
C2
C3
C4
C5
C6
C7
C8
D1
D2
#0
#1
#2
#3
#4
#5
#6
#7
#8
#9
#10
160ms

FIG.33

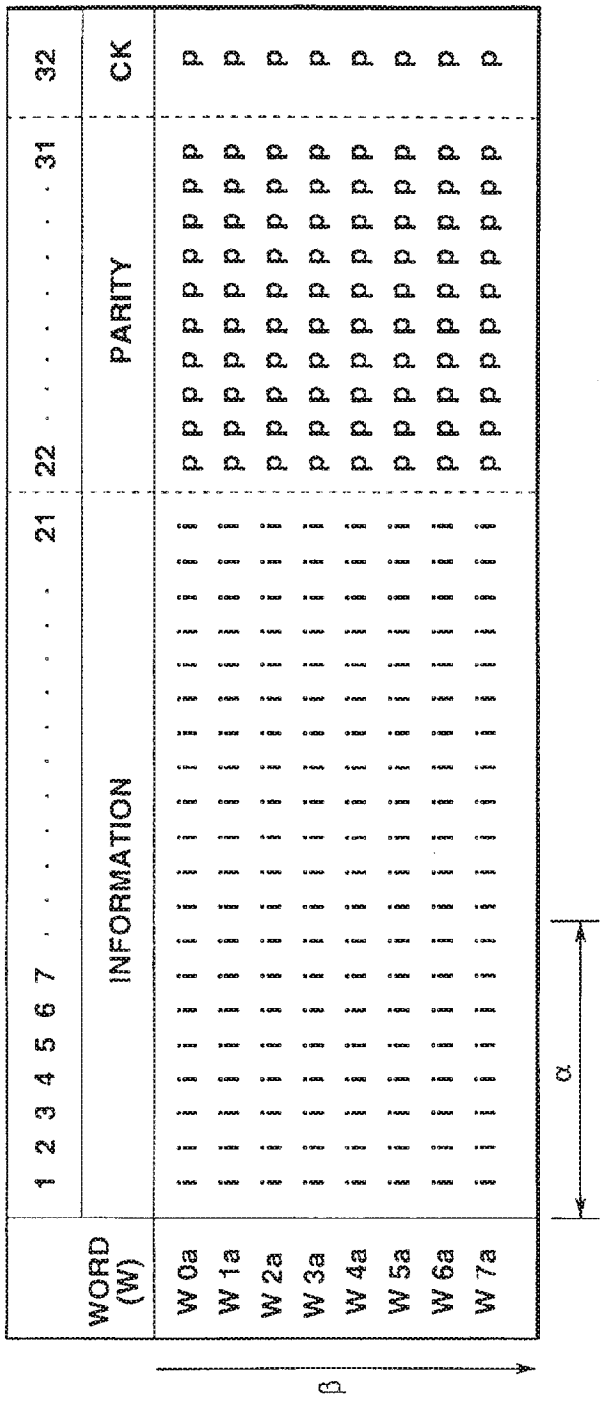

WORD (W)
1 2 3 4 5 6 7 21
INFORMATION
22 31
PARITY
32
CK
W 0a
W 1a
W 2a
W 3a
W 4a
W 5a
W 6a
W 7a
α
β

FIG.34

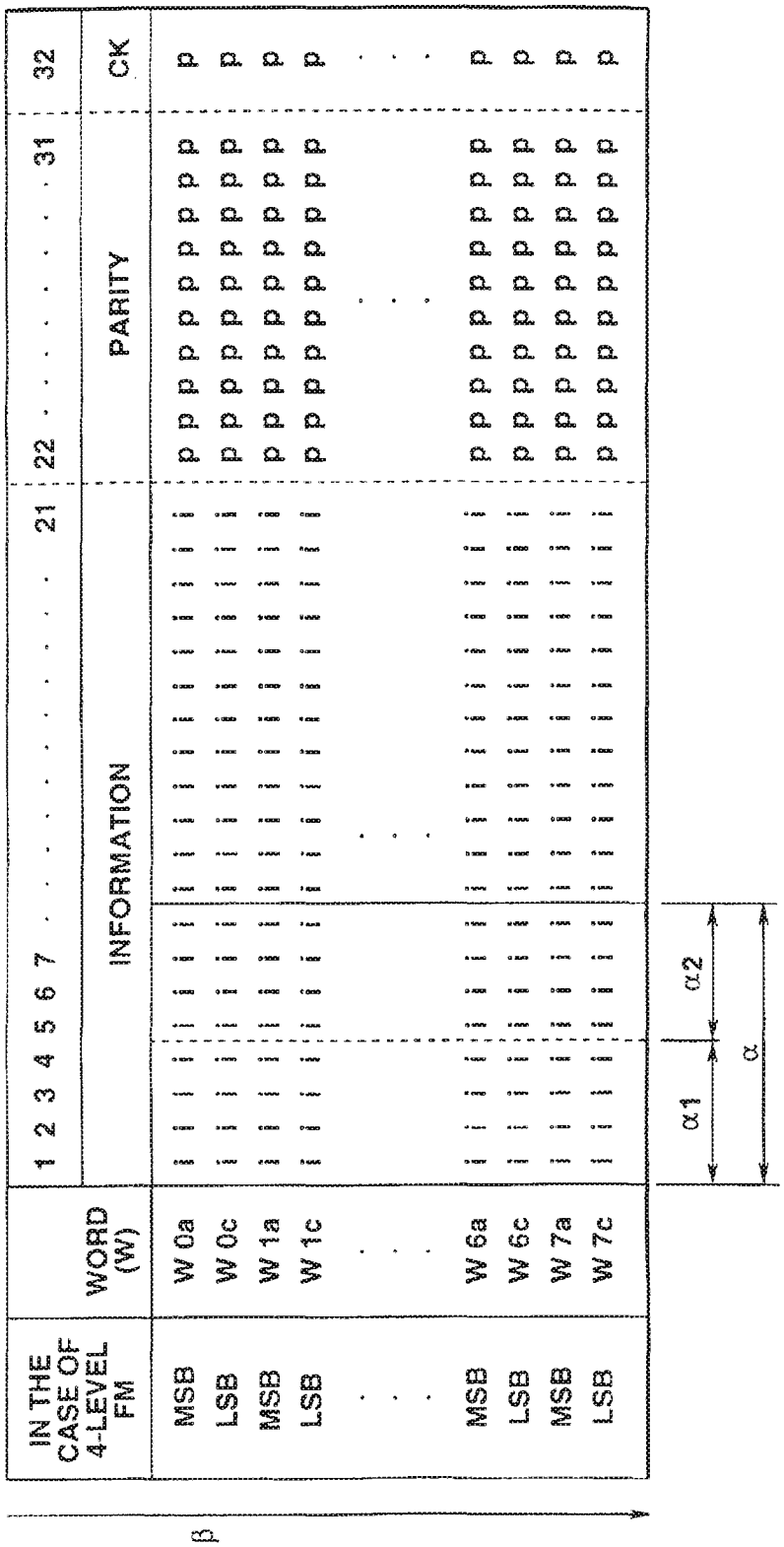
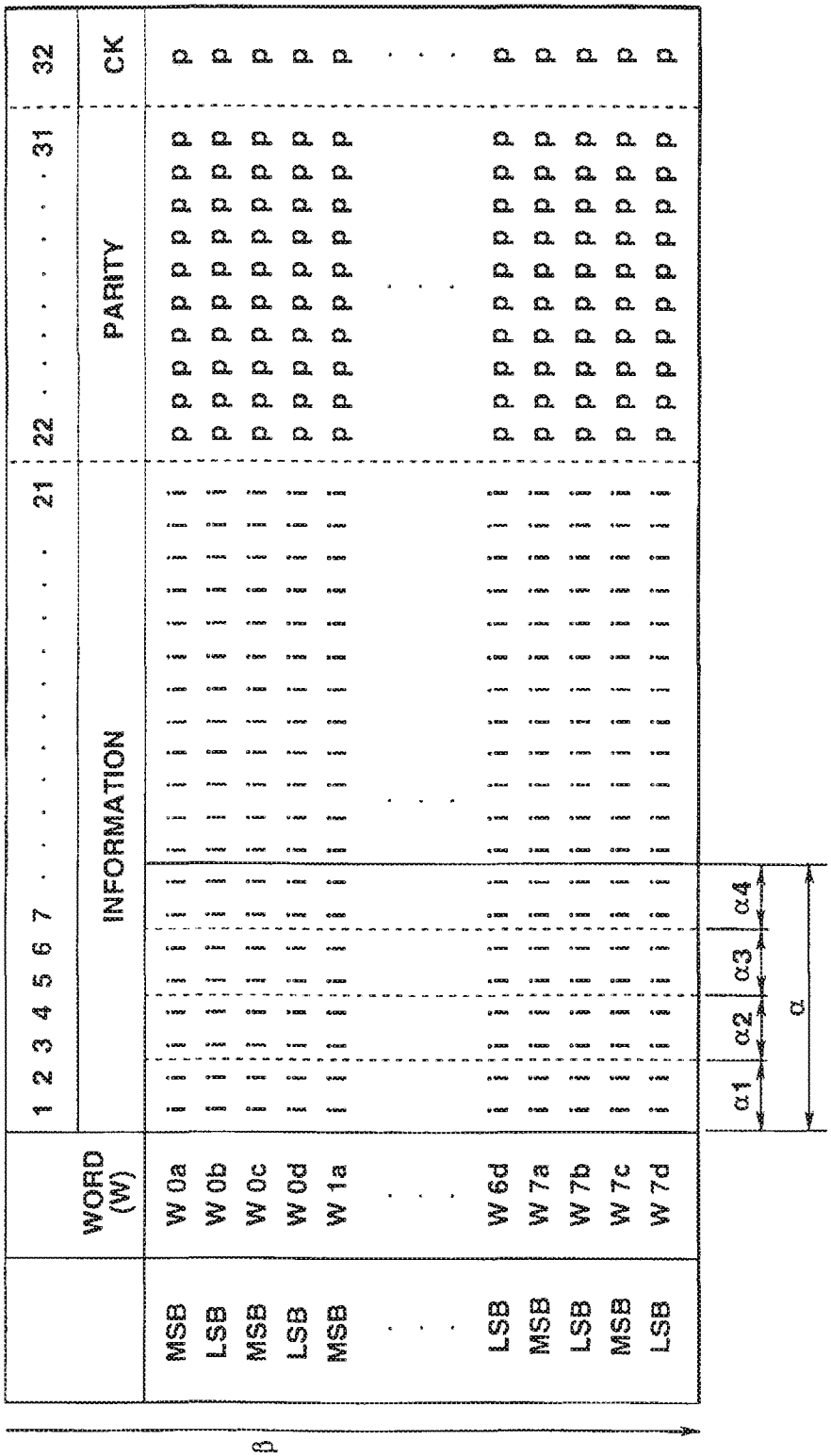

IN THE CASE OF 4-LEVEL FM
WORD (W)
INFORMATION
PARITY
CK
1 2 3 4 5 6 7 . . . . . 21 22 . . . . . 31 32
MSB
LSB
W 0a
W 0c
W 1a
W 1c
W 6a
W 6c
W 7a
W 7c
α1
α2
α
β

FIG.35


WORD (W)
INFORMATION
PARITY
CK
1 2 3 4 5 6 7 . . . 21 22 . . . . . 31 32
MSB LSB MSB LSB MSB . . . LSB MSB LSB MSB LSB
W 0a W 0b W 0c W 0d W 1a . . . W 6d W 7a W 7b W 7c W 7d
α1 α2 α3 α4 α
β

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/JP 96/03755

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04L1/12 H04Q7/18

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 264 205 A (NIPPON ELECTRIC CO) 20 April 1988	23
Y	see abstract	1-3,6-8
A	see column 2, line 5 - line 22 see column 5, line 5 - column 6, line 53; claims 6-11,13-16; figures 5-8	4,5,9-22

Y	WO 92 22162 A (BRITISH TELECOMM) 10 December 1992	4,5
A	see abstract see page 1, line 8 - page 3, line 6 see column 5, line 16 - column 7, line 6; figures 1,2	1-3,6,9

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4

Date of the actual completion of the international search	Date of mailing of the international search report
17 April 1997	06.05.97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Gries, T

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Inter nal Application No
PCT/JP 96/03755

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 117 500 A (DAVIS WALTER L ET AL) 26 May 1992	1-8
A	see abstract see column 3, line 35 - line 68; figures 1,3,4 see column 5, line 22 - column 6, line 10 see column 7, line 21 - line 46 see column 8, line 20 - column 11, line 37; claims	9-23
A	WO 90 08446 A (ATE CORP) 26 July 1990 see page 3, paragraph 1 - page 5, paragraph 1	1-22
A	US 5 168 493 A (NELSON LEONARD E ET AL) 1 December 1992 see page 2, line 4 - line 45; claims; figures	1-23
A	US 4 816 820 A (DAVIS WALTER L) 28 March 1989 see abstract see column 2, line 5 - line 28 see column 4, line 28 - column 5, line 7 see claims; figures	1-23
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4

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Inter nal Application No
PCT/JP 96/03755

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(51) International Patent Classification 6 :	A3	(11) International Publication Number: WO 98/37713
H04Q 7/20, H04L 1/12		(43) International Publication Date: 27 August 1998 (27.08.98)

(21) International Application Number: PCT/SE98/00197

(22) International Filing Date: 3 February 1998 (03.02.98)

(30) Priority Data:
08/801,386 20 February 1997 (20.02.97) US

(71) Applicant: TELEFONAKTIEBOLAGET LM ERICSSON (publ) [SE/SE]; S–126 25 Stockholm (SE).

(72) Inventors: LABONTE, Sylvain; 380, Raymond, St–Bruno de Montarville, Quebec J3V 2S7 (CA). TURCOTTE, Eric; Apartment 1B, 460, Abelard, Verdun, Quebec H3E 1B5 (CA).

(74) Agent: ERICSSON RADIO SYSTEMS AB; Common Patent Dept., S–164 80 Stockholm (SE).

(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(88) Date of publication of the international search report:
12 November 1998 (12.11.98)

(54) Title: SUPPORT OF MULTIPLE MODULATION LEVELS FOR A CELLULAR PACKET CONTROL CHANNEL

(57) Abstract

A D–AMPS+ cellular communications air interface (50) is presented wherein a packet data control channel (40, 60) and packet data traffic channel (42, 62) are supported in addition to the conventional digital control channel (20) and digital traffic channel (22, 64). In particular, the packet data control channel and packet data traffic channel support multiple modulation level operation (high versus low). Procedures are provided for mobile station selection, as well as re–selection (102, 110), of either the high or low–level modulation for the packet channels. Procedures are further provided for facilitating a fall–forward (158, 164, 190, 194) to the high–level modulation packet data control channel, or a fall–backward (222, 232, 254) to the low–level modulation packet data control channel with respect to both uplink and downlink packet data communications.

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INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/SE 98/00197

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04Q7/20 H04L1/12

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 92 22162 A (BRITISH TELECOMM) 10 December 1992 see page 2, line 1 - page 4, line 6	1-7,12, 17,22
P,X	WO 97 15131 A (ERICSSON TELEFON AB L M ;ERICSSON GE MOBILE INC (US)) 24 April 1997 see page 16, line 2 - page 18, line 12 see page 19, line 28 - page 20, line 19	1-7,12, 17,22
P,X	WO 97 44926 A (SIEMENS AG ;SPLETT ARMIN (DE)) 27 November 1997 see page 2, line 35 - page 4, line 9	1-7,12, 17,22
A	WO 95 07578 A (QUALCOMM INC) 16 March 1995 see page 3, line 13 - page 4, line 12 see page 14, line 36 - page 15, line 2	1-7,12, 17,22

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29 September 1998	05/10/1998

Name and mailing address of the ISA	Authorized officer
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Inte ional Application No
PCT/SE 98/00197

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(51) International Patent Classification 6 : G01R 31/08, H04H 27/10, H04L 27/10, 27/18, 5/16 — A1

(11) International Publication Number: **WO 98/59254**

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(21) International Application Number: PCT/US98/11107

(22) International Filing Date: 1 June 1998 (01.06.98)

(30) Priority Data:
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(54) Title: IMPROVED UNIVERSAL LAN POWER LINE CARRIER REPEATER SYSTEM AND METHOD

(57) Abstract

An improved local area network (LAN) to power line carrier (PLC) interface and protocol using FSK is described. This system provides improved data symmetry, higher data rates, lower bit error rates, improved synchronization and alignment of data, as well as improved carrier detection. The system provides high speed frequency shift key (FSK) modulation over the power line to achieve high data rates. Performance may be further improved by using a novel combination of FSK modulation and differential shift key (DFSK) modulation to provide an improved local area network (LAN) to power line carrier (PLC) interface and protocol using FSK and DFSK. DFSK is described and shown to provide improvements in the modulation and demodulation of data transferred over digital networks.

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IMPROVED UNIVERSAL LAN POWER LINE CARRIER REPEATER SYSTEM AND METHOD

Background of the Invention

Field of the Invention

This invention relates to Power Line Carrier (PLC) Local Area Network (LAN) repeaters in which LAN signal/data are transferred over the existing power lines of a building via power line carrier rather than through special cables which must be installed professionally. A PLC LAN repeater must (a) interface effectively with the LAN and its protocols, (b) achieve data rates over the power lines which are at least an order of magnitude faster than those of prior art PLC systems and (c) provide acceptable operation to a plurality of users. While many LAN (including Arcnet, Token Ring and RS-485) are in use and may be serviced by the instant invention, the Ethernet LAN will be examined to illustrate the interface and data rate requirements for this invention.

More specifically, this invention relates to systems for PLC LAN repeaters which employ a differential frequency shift key (DFSK) technique to increase data rates and noise immunity and system reliability. The use of DFSK technology improves the performance of PLC LAN repeaters by improving edge resolution; reducing the effective bandwidth requirements of the transmitted signal, thereby permitting increased data rate or narrower filter bandwidth; reducing the temperature coefficient and tuning requirements by AC coupling of the analog data; reducing startup transients in the data slicer; rejecting noise on the marking frequency; permitting special characters for compression or control purposes. This invention incorporates a number of other improvements over the existing technology, including: improved RF and IF filters to increase the data rate; synchronization of the data rate clock with the carrier frequency; a realignment bit every ninth bit; a group knowledge (ACK) which is frequency shift keyed (FSK) at a lower data rate; and carrier detection is accomplished without use of a Receive Signal Strength Indicator (RSSI), using special preamble and start characters. These improvements provide a complete modulation and demodulation system for PLC with significantly enhanced data quality.

Description of Related Art

The Ethernet IEEE 802.3 standard provides for mechanical and electrical standards and protocols for multiple users to share ("network") data transfer access to a common transmission medium or bus (the "ether" of a cable) but still maintain acceptable data access times and transmission rates. A user accesses the network through his node on the network, which is usually his computer/workstation with a hardware LAN interface physically connected to the network cable as the node. Proprietary network software (such as NetWare and Windows for Workgroups) runs with the workstation's operating system to manage the interface between the user's applications and the network. Individual users are provided unique ID/address codes so that only messages with the correct address preamble may be accepted and routed into their node/workstation while ignoring all others. The protocols also provide for detecting and managing collisions between the plurality of network users seeking simultaneous access to the network so that only one user may safely transmit data at a time. The software for implementing this Carrier Sense Multiple Access with Collision Detection protocol (CSMA/CD) is usually divided between firm embedded in the Ethernet interface cards and the proprietary workstation software.

IN a peer-to-peer network configuration, two or more workstations may be networked together. Each user may communicate with any other user with network protocols arbitrating data collisions when more than one user seeks to initiate communication at a time. In the Ethernet specification, when a collision is detected, each user interface backs off for a "random" time before reattempting access (CSMA/CD). In a client-file server configuration, each user communicates with the server as well as directly with other users. Arbitration takes place between the users and the server.

Since a large number of users results in frequent data transfers as well as collision arbitration, the data rate of Ethernet must be very high to accommodate acceptable transmission time delays. Consequently, the IEEE 802.3 standard provides for data transmission at the rate of 10Mbps in packets of no more than 1,500 bytes. Such speeds are three orders of magnitude beyond prior art PLC data communication/LAN technology.

In addition, Ethernet mechanical standards provide for bidirectional communications either by coaxial cable ("thin/thick net") or by dual sets of Unshielded Twisted Pairs (one for each direction of data flow) called UTP or "10baseT" cable. Coaxial interfaces utilize a transceiver to interface between the bidirectional digital data of one computer and the RF data modulated signals of the coax/thin net. The 10BaseT medium accommodates the bidirectional data more directly by using 2 sets of twisted pairs (one for transmit and one for receive data). To achieve 10Mbps data throughput an interface standard similar to RS-485 (CCITT V.11) is employed, which provides for balanced, isolated and low impedance transmitters and differential receivers. The RS-485 standard provides for up to 32 transmitters and receivers networked on the same data line. Both coaxial and UTP communications interfaces/LAN cards have been reduced to low cost, high performance commercial products sourced by many companies.

The problem with LAN systems such as Ethernet is the installation expense for the cables which can exceed $100 per "node" or user. Often the old commercial structures are prohibitively difficult to retrofit. Other companies are periodically requiring reconfiguration of office space to accommodate changing commercial needs and require a less expensive and more friendly method for connecting and reconfiguring workstations to their LAN. And there are limitations as to the length of cable one can use. The instant invention provides a cost effective alternative to special cable installation by "repeating" the network via power line carrier data transmission over the AC power lines of a premises.

RF LAN repeaters have been offered in the 900 MHz range where sufficient bandwidth is available to transmit the 10Mbps signals. However, the 900 MHz systems are not only prohibitively expensive (at $600-800 per node) but also exhibit propagation problems and interference in commercial buildings where LAN systems are most commonly used and the software for managing a large number of users has been unacceptable, which (in addition to high cost) has detracted seriously from their widespread proliferation.

Summary of the Invention

The instant invention, however, provides both the interface for the commercial LAN card/port as well as the PLC repeater system capable of transferring data packets at sufficiently high rates and with collision

detection/prevention firmware for transparency with respect to small and medium sized LAN systems at a competitive cost.

The PLC repeater/transreceiver comprises both a novel data transmitter and advanced data receiver with over 90 dB of gain, which together are capable of high bandwidth/data rate Frequency Shift Key (FSK) transmission data rates of DC to over 2 Mbps (million bits per second). RF PLC frequencies of 2-20 MHz combined with sufficient transmitter power and receiver sensitivity achieve adequate signal to noise ratios in AC power systems with high attenuation and noise. The over-90 dB sensitivity/RF range permits proper data transmission over the 3-phase power distribution system in industrial installations with capacitive loads and electrical equipment induced noise. The RF carrier frequencies in combination with the receiver sensitivity permit the signals to jump phases in residential 2-phase and industrial 3-phase distribution systems by means of the capacitance between phases in the wiring. The highly deviated (greater than 100kHz) FSK signal in combination with the high RF carrier frequency and 3 stages of RF and IF filtering in the receiver makes the data transmission very robust in the presence of electrical interference.

Multiple transceivers are capable of simultaneous operation at different RF carrier frequencies, permitting full duplex serial communication as well as multiple networks operating without interference on the same power line bus.

The LAN interface comprises 2 subsystems: (1) a bidirectional LAN card or port interface (a) for receiving (and storing in buffers) outgoing data packets in the LAN system format from a user's workstation for transmission to other LAN users and (b) for returning data packets in the LAN format to the same workstation card/port from other users, and (2) an asynchronous serial data transceiver (with data buffering) which (a) drives the PLC data transmitter with the outgoing data packets stored in the buffer by the port interface and (b) receives incoming data from the PLC data receiver originating from other users. The serial data transceiver is controlled by a system controller with firmware (i) to arbitrate collisions on the power line data bus with other users and (ii) to manage the bidirectional transfer of data packets: OUTGOING from LAN interface to serial data transceiver and INCOMING from serial data transceiver back to LAN interface. Commercial controllers are available for managing the entire repeater which contain both the asynchronous PLC serial port and some LAN interface ports such as RS-232 and RS-485, as well as parallel ports.

A relatively simple and low cost PLC LAN repeater networks workstations through their standard serial ports using software such as NetWare Lite. The PLC LAN repeater consists of a low cost but competent microcontroller with (1) an RS-232D port (115.2Kbaud) for connecting a built-in serial port to the users and (2) an asynchronous serial communications port which connects to the PLC transceiver. The onboard controller firmware manages the storage and retransmission of data packets in addition to collision arbitration and detection on the PLC bus. The PLC LAN repeater thus converts a two-user RS-232 peer-to-peer network into a more-than-two user network (like RS-485) without the user having to by a (more expensive and less common) RS-485 type of interface. The data rate for PLC bus could be 10 times higher than the limited 115.2 Kbaud of the conventional serial port, making this kind of PLC bus network capable of handling much larger data traffic than is possible with an ordinary RS-232 serial port network.

Alternatively, personal computers (PCs), printers and other electronic devices can be networked together using this invention through standard parallel ports using standard interface protocol software and controllers, including but not limited to Windows 95.

The proliferation of embedded controllers in a plethora of electrical/electronic equipment can be effectively networked with control maintenance/security systems via PLC LAN repeater subsystems also embedded in the equipment, which repeaters network the serial port of the embedded controllers to a PLC LAN bus via the existing power cord of the equipment and the power distribution system of a premises. The inventors have applied this same concept of embedded PLC LAN repeater to many types of computers and related products, modems, industrial control systems and utility metering equipment. The instant invention facilitates the higher data rates and transmission integrity required by these systems.

For LANs using the RS-485 ports, a high-speed 485 interface is provided together with a controller for converting the data to PLC transceiver compatible rates and format.

A more complex configuration for Ethernet illustrates the scope of application of the universal repeater and utilizes a commercial Ethernet interface chip in combination with a microcontroller with global high-speed communications port for servicing the PLC transceiver. This provides a transparent PLC repeater which connects to the standard Ethernet ports of a workstation and, with NO additional software or hardware, permits multiple users to network over the existing power lines of a premises.

The versatility of configurations also supports Token Ring and Arcnet protocols, chiefly because the PLC transceiver is competent enough to handle sufficiently high data rates to permit transparent operation for smaller segments of the network.

Objects

Accordingly, it is an object of the invention to provide an advanced method and system of high data rate power line carrier transmission which supports the data rates required by local area networks.

It is an object to provide a method and system of interfacing power line carrier repeaters with conventional network cables or cards to convert LAN data to PLC repeater acceptable data and to convert PLC repeater data to LAN data.

It is a further object to provide a method and system of arbitrating multiple PLC LAN repeaters to permit efficient and exclusive access to a particular frequency/channel of the power line medium.

It is an object to provide a PLC transceiver which sends data with a bandwidth of DC to over 2 Mbps and which is therefore able to transfer wideband analog signals/data of DC to over 1 MHz bandwidth.

It is an object to provide an embedded PLC network repeater system capable of being interfaced with embedded controllers in equipment for networking said equipment with automation, control and diagnostics systems and general network services.

It is a further object of this invention to provide an embedded PLC network repeater system having an improved modulation technique, known as Differential Frequency Shift Key (DFSK) in conjunction with Frequency Shift Key (FSK) which is able to trigger data state changes with much improved resolution.

A still further object of this invention is to provide an embedded PLC network repeater system having a DFSK modulation technique which by centering more energy around the carrier frequency minimizes the effective bandwidth required for a given data rate.

A further object of this invention is to provide an embedded PLC network repeater system employing improved RF and IF filters to provide wider and flatter pass bands while maintaining system data reliability with changing data compositions.

Another object of this invention is to provide an embedded PLC network repeater system employing a realignment bit at the end of each data byte to aid the re-synchronization of the receiver, thereby permitting increased data rates.

Another object of this invention is to provide an embedded PLC network repeater system with improved carrier detection and acknowledgment techniques.

An additional object of this invention is to provide an improved modulation and demodulation technique, known as Differential Frequency Shift Key (DFSK), for all networking media or electronic communications systems, including RF and wired media.

Additional objects, advantages and novel features of this invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art upon examination of the following or may be learned by the practice of this invention. The objects and advantages of this invention may be realized and attained by means of the instruments and combinations particularly pointed out in the appended claims.

These and other objects of the invention are achieved by an electronics system, which in its present preferred embodiment employs an innovative Differential Frequency Shift Key (DFSK) modulation technique to improve the reliability and achievable data rates of Local Area Network (LAN) communication between digital computer workstations across Power Lines or Power Line Carrier (PLC) mediums. While the preferred embodiment of the system is designed to operate at data rates of up to 2 million bits per second (2Mbps), even higher data rates are possible with some envisioned enhancements, and very high noise, jitter, temperature, and voltage drift immunity.

Brief Description of the Drawings

Figure 1 is a diagram of a PLC LAN repeater network.

Figure 2 is a block diagram of a PLC LAN repeater.

Figure 3 is a schematic of a LAN to Repeater Interface.

Figure 4 is a schematic of a PLC Repeater Transceiver.

Figure 5 is a schematic of a standard quadrature detector for the demodulation of FSK carrier signals.

Figure 6 is an illustration of the voltage output from the quadrature detector buffer amplifier 5-54 (V_{quad} 5-59), showing the variance of the voltage level with frequency change.

Figure 7a shows the schematic of a DC-coupled FSK data comparator. Figure 7b shows the ideal operation of the DC-coupled FSK data comparator. Figure 7c shows the operation of the DC-coupled FSK data comparator when there is signal drift.

Figures 8a, 8b, and 8c illustrate the operation and disadvantages of the traditional FSK data slicer 8-70.

Figure 9a illustrates the DFSK data detector of the preferred embodiment of the invention which overcomes the limitations of prior detectors. Figure 9b shows the nature of DFSK V_{quad} signals as they are detected by a quadrature detector. Figure 9c shows the effect of temperature or data composition on the operation of the DFSK data detector. Figure 9d depicts a further modification/enhancement of the DFSK demodulator.

Figure 10 illustrates a comparison of the frequency spectrum of FSK with DFSK modulation and illustrates the improved bandwidth requirements of DFSK over FSK.

Figure 11 illustrates the implementation of DFSK modulation using a 5-state digital state machine.

Figure 12 illustrates a state machine improvement where the data rate is synchronized with the carrier frequency.

Figure 13 is a MC13158 receiver data book chart for the RSSI response which shows a limiting characteristic RSSI detection schemes and protocols based on RSSI signals.

Figure 14 illustrates several improvements achieved with the Acknowledge Comparator.

Figure 15 depicts a typical V_{quad} data and FSK ACK Data waveform which illustrates how DFSK permits the compatible use of FSK to produce special characters for group acknowledgment in a network.

Detailed Description of the Preferred Embodiment

A universal local area network (LAN) power line carrier (PLC) repeater system and method is described which provides: (1) a competent LAN repeater interface for converting high-speed LAN data to PLC serial data and high-speed PLC serial data to LAN data, (2) a high-speed PLC data transceiver for exchanging PLC data with other repeaters, and (3) a control system and method for controlling the interface and transceiver to arbitrate data communications on the PLC bus among the plurality of PLC repeaters. In the following description, the Ethernet LAN PLC repeater is set forth in specific detail in order to provide a thorough understanding of the invention in a non-trivial application. It will be apparent to one of ordinary skill in the art that these specific details are beyond what is necessary to practice the present invention. In other instances, well-known circuits, interfaces and software structures have not been shown in detail in order not to unnecessarily obscure the present invention.

Reference is first made to Figure 1 in which a plurality of workstations are networked together by means of PLC repeater s and the AC power system of a premises. Workstation 1-1 with its corresponding LAN card is connected via UTP 1-2 to LAN-PLC repeater 1-3 to the AC power line 1-4 of a premises which constitutes a PLC LAN bus in addition to distributing AC power to the various appliances, equipment and workstations (1-1, 1-7, 1-10) of the premises. Data from workstation 1-1 is repeated onto the PLC LAN bus 1-4 in proper format for LAN-PLC repeater 1-5 to receive said data and repeat it in LAN format via UTP 1-6 to workstation 1-7 and its corresponding LAN card. Workstations 1-1, 1-7 and 1-10 are operated by commercial LAN software which, at a minimum, supports a peer-to-peer configuration of users, thus permitting messages and files to be transferred between any two peers of the network. The LAN PLC repeater permits said data to be transferred between workstations "transparently," that is, without any additional effort or special instructions/software on the part of the workstation and its operating system. Therefore, workstation 1-7 receives the data originating from workstation 1-1 and confirms receipt thereof back to 1-1 via UTP 1-6, repeaters 1-5, AC power bus 1-4, repeater 1-3 and UTP 1-2.

While two workstations networked together peer-to-peer constitute the minimum configuration of a network and do not require sophisticated network arbitration, many commercial network products assume that additional workstations, represented by 1-10, may be connected to the network, seeking network access simultaneous with other workstations and requiring CSMA/CD. In a PLC LAN repeater, arbitration protocols peculiar to the PLC environment need to be serviced transparently to the workstations/users.

Figure 1 also illustrates a segmented bus configuration comprising both a conventional hard-wired LAN bus segment 1-12 network and a PLC LAN interface 1-11. In this example, the LAN bus 1-12 networks physically proximate workstations together (not illustrated), while the PLC bus segment 1-4 could network physically less proximate or more mobile workstations 1-1, 1-7 and 1-10 to the network via PLC-LAN interface 1-11. Interface 1-11 is also a "repeater" similar in hardware to repeater 1-3, but may include software/firmware which identifies and repeats only those LAN packets/data addressed to workstations 1-1, 1-7 and 1-10 on the PLC LAN segment 1-4, thereby reducing the data traffic load on said PLC segment 1-4. In large networks involving many workstations, a plurality of PLC LAN segments 1-4, each operating on its exclusive PLC frequency and serviced by its respective PLC-LAN interface 1-11, may be networked together by means of the instant invention, while sharing the AC power distribution bus through frequency domain multiple access or other multiple techniques such as code division multiple access.

Referring still to Figure 1, other communication devices besides workstations may be represented by workstations 1-1, 1-7 and 1-10. For example, embedded microcontrollers 1-1 and 1-7 with communication ports could be networked through embedded repeaters 1-3 and 1-5 with a host controller 1-10 which monitors/controls the operation of the equipment hosting said microcontrollers. A relatively simple network communication and arbitration protocol could be administered by said host repeater 1-8. Such protocols have been developed for applications such as utility meter reading and industrial control systems.

Figure 2 is a block diagram of a LAN PLC Repeater 1-3. The LAN connection 1-2 to repeater 1-3 is made at RJ-45 connector 2-1, which is operably connected via connections 2-2 and isolator 2-3 to the differential transmit and receive ports 2-4 of LAN interface IC 2-5. Network Interface Controller (NIC) 2-5 (data sheets may be found in National Semiconductor's Local Area Network Databook, incorporated by reference) is a generic, multiple-sourced part which is common to most sophisticated LAN networks and contains the hardware registers, connections and logic/firmware to transmit and receive high bit rate LAN signals with standardized preambles, packet sizing and CSMA/CD collision arbitration. A standard RAM (Random Access Memory) 2-6 sufficient size is operably connected to NIC 2-5 via memory address and data bus 2-7 to store incoming and outgoing data packets: (1) incoming packets which have been received from LAN connection 1-2 and are waiting to be transmitted further by μC 2-9 and (2) outgoing packets which were received by μC 2-9 and are waiting to be transmitted back through LAN connection 2-1 to the network 1-2 or LAN card of a workstation 1-1. The repeater is controlled by μC 2-9, which is operably connected to NIC 2-5 via control, data and address lines 2-8, permitting the μC 2-9 to setup and control the NIC 2-5 and transfer data packets bidirectionally into/out of the packet buffer 2-6. In addition, μC 2-9 has communication ports, both parallel and serial, for communicating LAN data with wired and/or PLC interfaces. Some

commercial μC's, such as the Intel 83C152 (an 8031 derivative, data sheets for which may be found in Intel's Bit Embedded Microcontroller Handbook, incorporated by reference) contain high-speed Global Serial Channels (GSC) 2-10 which are capable of 0.1 – 10 Mbps serial data transfer with CDMA/CD protocol registers and firmware at a reasonable cost, which facilitates data I/O for a high-speed PLC transceiver (2-11 through 2-17 or Figure 4), which is operably connected to the global series channel 2-10. Transmit data TXD from the incoming packet buffer 2-6 modulates an RF carrier at modulator 2-11 which drives transmitter 2-12, which transmitter is operably connected to the power line bus 1-4 via Filter 2-13 and RF coupler 2-14. Transmitter 2-12 is turned ON by transmit enable TXE only when data is transmitted, thus reducing the RF traffic on the AC line 1-4 during latent periods. Data receiver 2-16 is operably connected to AC bus 1-4 via RF coupler 2-14 and filter 2-15. Data-modulated RF from similar repeaters carried by power line 1-4 is received by the receiver 2-16, buffer by high-speed comparator 2-17 and transferred as RXD to global serial port receiver 2-10where μC 2-9 screens the preamble for ID codes/addresses and arbitrates the data for transmission on to the LAN interface. Unique ID codes repeater addresses may be either manually entered by dipswitch or automatically assigned by network supervisory software under automatic or user control. For example, manual entry ID code switches 2-22 operably connect to a port of the μC 2-9 via lines 2-21, and may be used to uniquely identify address and security bytes in preambles and/or determine arbitration backoff delay times, etc. Factory-burned ID codes can also be obtained with specialty or ASIC designs.

Figure 2 also illustrates alternate LAN and data sources for the PLC repeater. The μC 2-9 provides a standard serial comm port 2-20 which connects to a serial port interface 2-19 and connector 2-18, configuring repeater 1-3 into an RS-232D LAN repeater, in which the PLC data transceiver operates at substantially higher data rates (than the 115.2Kbaud RS-232D) to unburden the AC power bus 1-4 LAN. (The Network Interface Controller and associated parts would be removed, if unused in this alternate embodiment.) IN some network configurations, parallel port interface components could be operably connected in place of serial components 2-18 and 2-19 to a parallel port on μC2-9. Alternately, the GSC port 2-10 could be operably connected to an RS-485 LAN via a 2-19 interface like the LTC490, while the μC serial port 2-20 TxD and RxD lines could be operably connected to the TXD and RXD I/O 2-11 and 2-17 of the PLC transceiver. In its simplest embodiment, the TxD and RxD lines 2-20 may be operably connected to TXD and RXD lines 2-10, providing a repeater requiring μC; PLC transmitter 2-12 and receiver 2-16 have been operated simultaneously on different carrier frequencies to provide full duplex serial operation, if required by the LAN application. Alternately, the transmitter in a no μC system may be enabled only when data is transmitted, to permit PLC LAN operation with a single frequency.

Figure 3 presents a detailed working schematic of the LAN interface and 10 Mbps to 1 Mbps converter. J1 2-1 is the RJ-45 connector to the LAN line/card of a workstation. U3 2-3 is the Isolator/Filter for Ethernet 10Mbps lines. U1 2-5 is the NIC chip, a National DP83902A, the complete specs for which are found in National Semiconductor's Local Area Network Databook, already incorporated by reference, which also contains comprehensive documentation on the Ethernet IEEE 802.3 standard. Several Network Interface Controllers are available from various manufacturers for Ethernet as well as other popular network standards, such as Arcnet and Token Ring, which may be operably connected to μC U6 2-9 in place of Ethernet NIC 2-5 and the corresponding connectors 2-1 through 2-4.

Referring still to Figure 3, an 8Kbyte RAM packet buffer U5 2-6 is operably connected via address latch U7 3-27 to the memory address and data ports of NIC 2-5. The size of buffer 2-6 may be enlarged or reduced somewhat to accommodate network data capacity, system operation and budgetary constraints. Repeater μC U6 2-9 is operably interfaced with NIC U1 2-5 via latches, U13, U14 3-25 & 3-26 and PAL U15 3-28. The timing diagrams and PAL 3-28 logic diagram are appended herewith in Appendix B. Additional functions 20 MHz clock 3-29, 10 MHz divider 3-30, status drivers 3-31 and status indicators D1, D2 and D3. While one enabling embodiment has been represented, those skilled in the art will appreciate that other approaches and simplifications can be implemented without departing from the method presented herein.

Referring to Figure 3 again, the μC 2-9 may contain masked ROM firmware or may be operably connected with external EPROM U9 3-9 for development purposes. A pseudo-code listing follows:

LAN PLC REPEATER PSEDUO-CODE FLOW SHEET

```
RESET ON POWER UP
STARTUP SEQUENCE
'Initialize µC sets up the communications registers for Manchester
'Encoding with CSMA/CD. A 16-bit CRC is selected and the preamble
'is set to 8 bits. The serial rate is set to 1.25Mbps.
INITIAZLIE µC
        GMOD Register
                Select Manchester Encoding
                Select CSMA/CD
                Enable CRC, Select 16-bit CRC
                Set preamble to 8 bits
        Baud Register
                Set serial rate at 1.25 Mbps
        Disable all interrupts
        Enable receiver
        Set transmit status register to normal operation
        Set address mask registers to don't care state
        Initialize SLOTTM (slot time register) to 2µs
'Initialize NIC divides the 8K buffer into 2 Xmit buffers and 20
'256 byte pages for the receive ring. Data is handled a byte at 'time and the FIFO to receive buffer ring occurs 8
bytes at a time.
'The CRC is appended by the transmitter. The receiver rejects 'errored packets. All valid packets are received.
INITIALIZE NIC
        Setup 8K xmit/rcvr buffer
        Setup 2 Xmit buffers of 1536 bytes each
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        Set remaining 5120 bytes as receive buffer ring
        SETUP NIC REGISTERS:
            Data Configuration Register
                Byte wide DMA transfer
                Normal operation
                FIFO set to 8 bytes
            Transmit Configuration Register
                CRC appended by transmitter
                Normal operation
                Normal backoff
            Receive Configuration Register
                Reject packets with receive errors
                Reject packets with fewer than 64 bytes
                Accept broadcast packets
                Accept all packets (promiscuous mode)
                Buffer packets to memory
    'The μC Receive Routine keeps track of the current NIC transmit
    'buffer then loads that buffer data as it is received in the
    'μC Receive FIFO.
    RECEIVE Routine: (μC ROUTINE for μC to send data to NIC)
        Choose free NIC transmit buffer
        IF NIC transmit buffers full, THEN
            Discard receiver and GOTO TRANSMIT
        Check Receive FIFO for Not Empty (NE) flag on μC
        Read byte from Receive FIFO
        Check Receive FIFO NE flag on μC
        IF FIFO Empty, THEN validate byte (No collision packet byte)
            IF transmit pending, THEN
                Restart backoff
            ELSE GOTO RECEIVE ROUTINE:
        ELSE GOTO READ ROUTINE (Valid Data Packet)

        READ ROUTINE: Write byte to NIC transmit buffer
            Read FIFO NE flag
            IF NE flag asserted, THEN GOTO READ ROUTINE
            ELSE write last data byte to NIC transmit RAM
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```
                    (Packet has been read and written to NIC)
                Check receiver for receiver errors
                IF no errors, THEN
                    Instruct NIC to transmit Packet
                ELSE discard packet
                GOTO TRANSMIT
'The μC Transmit Routine checks its Global Serial Channel (GSC) for
'a not busy state.  If the GSC is not busy then the μC reads packet
'data from the NIC and loads the TX FIFO.
TRANSMIT ROUTINE:  (routine for μC to get data from NIC)
    IF NIC has received a valid packet, THEN
        IF Global Serial Channel (GSC) is not busy, THEN
            Get pointer to received packet
            Read 2 bytes from NIC
            Save 1st byte (this is a pointer to the next received packet)
            Read 2 bytes from NIC
            Save these bytes in variable ByteCount

            LOOP
                Wait TX FIFO Not Full (NF Flag)
                Read 1 byte from NIC
                Write 1 byte to μC TX FIFO
                Decrement ByteCount
            ENDLOOP (When ByteCount is zero)
    ELSE GOTO RECEIVE ROUTINE
```

An additional routine services AC PLC bus collision avoidance and access arbitration. The method requires each repeater (with data to send) seeking access to a particular frequency or channel of the AC LAN bus (1) to listen to the bus traffic and, upon detecting the termination of a third party transmission, (2) to wait a minimum of 20 μs plus a random additional time (in 5 μs increments) before transmitting a short access request. (3) Following the access request, the receiver listens for 15 μs and, upon detecting no other carrier, the repeater μC begins data transmission with confidence. The dipswitch 2-22 may be used to provide a unique backoff or wait time for each repeater in addition to providing a unique IC code/address.

The universal interface capabilities of the controller 2-9 with its parallel and serial ports provides the capability for embedding the PLC repeater in computers and equipment with embedded controllers which already

connect to the AC power system of a premises, thereby networking the equipment with other similarly equipped devices and users simply by connecting the AC power. The physical size of such system and its associated cost could be reduced by utilizing the existing embedded controller and its serial port as the repeater controller and merely interfacing it to a compatible embedded PLC transceiver. The embedded controller would require the addition of appropriate network arbitration and control software/firmware. State-of-the-art design and manufacturing techniques reduce size and cost of repeater systems to attractive marketing levels.

Referring now to Figure 4, a versatile PLC data transmitter and receiver are shown which provide DC to 2 Mbps data rates. No Manchester or other encoding is required. Wideband data or analog signals may be transferred in original form. The data interface of the transceiver comprise four data lines: a transmit data input line GTXD, a transmitter enable input line TXE, a receive data output line GRXD and a carrier detect output line CARDET. These lines correspond to their counterparts at the Global Serial Channel 2-10 of the μC 2-9. GTXD data voltage levels are coupled to varactor diode D7, which is capacitively coupled to the frequency determining components C18 and C22 at the low-impedance port of oscillator 2-11, of which transistor Q3 4-33 forms the active element. Changes in reverse voltage across D7 result in corresponding inverse changes in the junction capacitance of D7 which change the resonant frequency of oscillation determined by L3 and the combination of C18 with the other capacitors C19 through C24. Driving the low-impedance port of oscillator 2-11 at the collector of Q3 4-33 minimizes the negative impact of differentiated DC voltage shifts on the delicate bias of Q3 4-33, which DC sifts correspond to differentiated data coupled through capacitors C19 and C22. The output of Q3 drives a class D output stage 2-12, which efficiently drives the power line through filter 2-13 and RF coupler 2-14. The several stages of transmitter drivers buffer the oscillator 2-11 from AC line capacitance and load changes. A class A transmitter output may be employed to reduce harmonics but with decreased efficiency. The transmitter enable TXE circuit 4-34 connects to the base of Q3 4-33 through D6 to turn the oscillator 2-11 off. The circuit of 4-34 may be configured as an inverter (for operation from a controller) or as a resetable monostable multivibrator (for enabling the transmitter only when data is presented to the data input).

Figure 4 also shows a data receiver 2-16 which is coupled by 2-14 RF coupler and filter 2-15 to the AC power bus. The filter 2-15 selects only the desired frequencies and matches the impedance of the AC line to that of the receiver input pin 1. The receiver 2-16 is a high performance superhetrodyne design with local oscillator, mixer, 2 stages of IF gain/filtering and limiter with quadrature detector, providing over 90 dB of RF gain with DC to 2 Mbps data response (Philips SA 636 version). The receiver 2-16 local oscillator supports either (1) crystals, (2) LC oscillators or (3) external oscillator/synthesizers. Use of a synthesizer permits controller 2-9 selection of LO frequencies for FDMA and frequency hopping configurations. Receiver 2-16 has both a data output and a competent FSI (Field Strength Indicator) output, which are buffered by high speed comparators 4-35 and 4-36 such as LM319 or LM360. It should be noted that an analog buffer can be connected to the demodulated signal output (pin9) of the receiver 2-16 for recovery of Wideband analog or composite analog/digital signals. The FSI CARDET output supports the RF carrier detect input of the repeater controller 2-9 for performing AC bus arbitration. The CARDET and GRXD buffered comparator outputs may be connected together in a wired AND configuration to provide

data output only when BOTH the carrier is present AND data is present. The receiver 2-16 is so selective that multiple receivers and transmitters may be used simultaneously in a repeater to increase data rate, increase channels or network together AC power line LAN segments. The transmitter and receiver are fully capable of RF LAN operation which, in conjunction with the competent collision avoidance and arbitration, would provide competent RF LAN segments for many applications.

It should be noted that alternative commercial components of competent specifications can be used for the components specified herein. Although this invention has been illustrated in relation to a particular embodiment, it should not be considered so limited except by the appended claims.

Alternative embodiments of the PLC transceiver hardware can provide significant improvements in data rate while increasing system reliability. These alternatives employ a different modulation technique than the FSK described previously, where detection was done by analog comparator DC threshold adjustments in reference to an analog demodulated FSK data waveform. This previously described FSK modulation technique produced a waveform which at high data rate exhibits a ramping/semi-sinusoidal characteristic (instead of the ideal DC square waves produced at low data rates). The alternative embodiment, described following, uses a Differential Frequency Shift Key (DFSK) in conjunction with the FSK modulation technique. DFSK produces sharp data edges for triggering the data detector and further permits AC coupling of said data edges, improved speed of data demodulation, and increased data reliability – less subject to system temperature coefficients, while minimizing the required effective bandwidth for a given data rate by centering more energy around the carrier frequency.

Further improvements are incorporated in this alternative transceiver embodiment, including: improvements in RF and IF filters to provide wider and flatter pass bands while maintaining reliability with changing data compositions, an introduction of a realignment bit in the data to provide the means for allowing the receiver to re-synchronizing with each in-coming byte, improvements in carrier detection and acknowledgment, and an improved controller.

These improvements permit a dramatic improvement in data rate and bit error rate across the PLC interface, from previous speeds of 100 to 350 Kbps to 1-3 Mbps. The following discussion describes prior modulation circuits, their characteristics and the current best mode of the invention utilizing the DFSK modulation techniques.

Figure 5 illustrates a standard quadrature detector for demodulation of FSK carrier signals. The IF limited output 5-51 of a receiver IF section (for example as shown on Figure 4 at U1 2-16 pin 11) drives directly the first input 5-56 of a quadrature detector 5-50 (which is typically an analog Gilbert cell multiplier). Said IF limiter also drives loosely, through a small-valued, high-impedance capacitor C1 5-55, a quadrature tank circuit composed of an inductor L 5-56, an capacitor C 5-57 and a resistor R 5-58. The capacitor C1 5-55 is typically a small value, such as 5pF in order to avoid swamping the transfer function of the quadrature tank circuit. The typical values of L 5-56, C 5-57 and R 5-58 depend on the carrier frequency. For example: for a 10.7 MHz system L 5-56 would typically be 1.5μH, C 5-57 would typically be 139pF, and R 5-58 would typically be 2.2KΩ; while for a 20 MHz system L 5-56 would typically be 1.5μH, C 5-57 would typically be 39pF and R 5-58 would typically be 4.7kΩ. The

quadrature tank circuit drives the second input 5-52 of the quadrature detector 5-50. The quadrature detector 5-50 is a multiplier which produces an output voltage QuadOut 5-53 that is the product of the two sine wave input signals. The double frequency output component of QuadOut 5-53 is filtered and amplified by the detector buffer amplifier 5-54, leaving the phase differential component V_{QUAD} 5-59 which varies in magnitude according to the frequency difference between the IF frequency received from a transmitter 5-51 and the quadrature tank resonant frequency determined by L 5-56 and C 5-57, as described in Figure 6. V_{REF} 5-66 is maintained at a voltage between the V_{QUAD} 5-59 FSK 1 and 0 levels, by the diodes D1 5-61 and D2 5-62. Comparator/Data Slicer 5-60 outputs data 5-64 at logic levels to a deserializer. The quality of the Data Slicer 5-60 is determined by how well it defines or recovers from V_{QUAD} 5-59 the edges of each data bit. Indeed, the quality of a complete modulation and demodulation system is determined by how faithfully data is transferred from the data transmitter to the data receiver. Prior data slicers exhibit two significant problems that are overcome by the present invention: (1) sensitivity to voltage drifts in V_{QUAD} 5-59, and (2) sensitivity to high data rates and data composition, as illustrated in the discussion and figures that follow.

Figure 6 illustrates that V_{QUAD} 5-59, the output of the quadrature detector buffer amplifier 5-54, varies lineraly with IF frequency within a 400KHz range. The attractive feature of this type of demodulator is that V_{QUAD} 5-59 is a DC level signal directly related to frequency, i.e., a 200KHz IF signal f_0 produces a +400 mV V_{QUAD} 5-59 signal and a +200 Khz IF signal f_1 produces a -400 mV V_{QUAD} 5-59 for low to intermediate data rates. The comparator 5-60 reference voltage V_{REF} 5-66 is maintained at a voltage corresponding to the virtual center frequency f_c between f_1 and f_0. Figure 6 also shows V_{QUAD} drift as a DC offset to the quadrature detector transfer characteristic at f_c about V_{REF}. V_{QUAD} drift is caused by the sum of temperature coefficient and long term frequency drifts of the transmitter and the receiver local oscillator in addition to the temperature coefficient and mechanical vibration drifts of the quadrature coil L 5-56 and capacitor C 5-57. The temperature coefficient drifts of quadrature detector 5-50, buffer 5-54 and comparator 5-60 are minor because V_{QUAD} is in the 400 mV range.

The prior DC coupled data slicer illustrated in Figure 7a may be less sensitive to data composition but is likely to be very sensitive to V_{QUAD} drifts. A second prior data slicer circuit, shown in Figure 8a, can track temperature coefficient and drift changes for low data rates, but no for high data rates or mixed data compositions.

At higher data rates, the V_{QUAD} buffer 5-54 slew rate combined with the time domain response limitations due to the bandwidth of the IF filters produce lower amplitude V_{QUAD} output signals are shown in Figure 7b. A lower data rate 3-bit long (0 0 0) V_{QUAD} signal is compared to a higher data rate single bit V_{QUAD} signal (0 1 0). While t1 through t3 is the period of a single high data rate bit, t1 through t7 is the period of a 3-bit long V_{QUAD} signal. At the higher data rate, the peak amplitude of V_{QUAD} at t2 and t4 is significantly lower than for the 3-bit long V_{QUAD} signal peak at t4 (and t10). The variation in V_{QUAD} peak voltage with data composition is significant enough to foil the operation of the V_{REF} bias circuit of Figure 5, but not that of Figure 7a, which illustrates a prior DC coupled data comparator with fixed reference (V_{REF}) as set by resistors R1 7-67 and R2 7-66. R1 7-67 and R2 7-66 are typically set to 1 kΩ. But while the DC coupled comparator of Figure 7a is able to slice the data from higher data rate or mixed data composition V_{QUAD} 7-68 signals illustrated in Figure 7b, it yet experiences significant data edge and bit

width symmetry difficulties when encountering temperature coefficient and signal drifts. Figure 7c illustrates the negative effects of V_{QUAD} 7-68 drift on the data 7-69 signal. The width of the 0 bit is totally truncated form t1 to t3, while the width of the 1 bit is expanded accordingly.

Figures 8a through 8c illustrate the operation and disadvantages of the FSK data slicer 8-70 with tracking reference V_{REF} 8-71 provided by diodes D1 8-73 and D2 8-74 and hold capacitor C_{hold} 8-75. D1 8-73 and D2 8-74 become forward biased during the positive and negative peaks of the FSK V_{QUAD} 8-72 signal and ensure that C_{hold} 8-75 is charged to the peak FSK V_{QUAD} voltage value less the diode forward voltage drop (about 40 mV). Thus, if the gain of buffer 5-54 is adjusted to provide an 800 mV peak-to-peak V_{QUAD} signal to D1 8-73 and D2 8-74, C_{hold} 8-75 will be charged by D1 8-73 and D2 8-74 after a few lower data rate alternating bit cycles to an intermediate value of V_{REF} halfway between the 0-rail and 1-rail of V_{QUAD} 8-72 that ideally provides adequate comparator 8-70 "slicing" of data from V_{QUAD} 8-72, as illustrated in Figure 8b. However, as illustrated in Figure 8c, when lower amplitude high data rate signals are used (for which the peak amplitude of V_{QUAD} 8-72 is reduced below the forward voltage drop of D1 8-73 and D2 8-74) or when long strings of 1's or 0's present in the data, the slicer V_{REF} 8-71 begins to drift off of the ideal center voltage and causes corresponding data edge and width distortions as shown in Figure 8c. The width of high data rate bits at t2-t9 are significantly distorted. And while the string of 1's at t9 to t13 may have readjusted V_{REF} for a time, at t12 other drift factors such as diode D2 8-74 leakage or comparator 8-70 input bias currents have started changing the charge on C_{hold} 8-75 with the attendant drift of V_{REF} 8-71/

Figure 9a illustrates a DFSK data detector 9-77 which overcomes the limitations of prior detectors. Both comparator inputs 9-78 and 9-79 are DC biased identically by means of R1 9-80 and R2 9-81 through R3 9-82 and R4 9-83 to V_{REF} 9-88 and the V_{QUAD} 9-84 DFSK signal illustrated in Figure 9b is AC coupled to the inverting comparator 9-85 input (V_{QUAD} 9-78) through capacitor C3 9-86. C2 9-87 bypasses or filters V_{REF} 9-88 from the AC signals at both inputs 9-78 and 9-79 of the comparator 9-85 passed to V_{REF} 9-88 through R3 9-82 and R4 9-83. R3 9-82 (from the DFSK V_{QUAD} 9-78 signal) and through R4 9-83 (from the V_{+REF} 9-79 noninverting input of comparator 9-85).

Figure 9b illustrates the nature of DFSK V_{QUAD} signals as they are detected by a quadrature detector. Differential frequency signals may be characterized by a short decrease in frequency to represent a falling edge (or high to low logic level change) in data. The term "differential frequency shift key" arises because the DFSK V_{QUAD} data looks like the derivative or differential of the FSK data described in Figures 6, 7 and 8. A DFSK modulation technique will be described in Figure 11. Figure 9b represents the signals at the inverting input (V_{QUAD} 9-78), noninverting input V_{+REF} 9-79 (the dashed lined) and data output of data slicer comparator 9-85 of Figure 9a. The inverting input signals V_{QUAD} 9-78 comprise a DC component equal to V_{REF} 9-88 and an AC component equal to V_{QUAD}'s DFSK component. Thus, at t0 the carrier frequency is f_0, V_{QUAD} 9-84 is at its median level, and V_{QUAD} 9-78 is at V_{REF} 9-88, its DC level provided by R3 9-82. AT t1 to t4 a DFSK falling data edge signal is detected as a positive pulse at V_{QUAD} 9084 and transferred through C3 9-86 to V_{QUAD} 9-78. Meanwhile, at t0 V_{REF} 9-79 is more positive than V_{REF} 9-88 due to the voltage divider action of hysteresis resistor R_H 9-89 with R4 9-83 and the logic level 1 data output voltage of the comparator 9-85. R_H 9-89 and R4 9-89 and R4 9-83 are judiciously selected to provide sufficient

hysteresis to permit noise reduction of half the V_{QUAD} 9-84 peak signal level or 200 mV (since the peak value of V_{QUAD} 9-78 is about 400 mV). Therefore, when the V_{QUAD} 9-78 signal rises at t2 to V_{+REFO}, comparator 9-85 output state toggles to logic 0 with a corresponding change in V_{-REF} 9-79 to V_{+REF}. At t4 V_{QUAD} 9-78 returns V_{REF} 9-88 until t5, when a negative going V_{QUAD} 9-78 voltage (1 level data edge) DFSK transition starts. At t6 V_{QUAD} 9-78 drops to the V_{-REF} voltage, the comparator 9-85 data output again toggles from 0 to 1 logic level with a corresponding to a change in V_{-REF} 9-79 to V_{+REFO}, where the reference input of the comparator waits until the next 0 level t1 to t4 type V_{QUAD} 9-78 signal is detected.

Because the DFSK signal defines the edges of each data level change, there is no temperature drift or data composition component that foils the operation of the comparator 9-85 DATA output 9-90, as illustrated in Figure 9c. The time constant of C3 9-86 and R3 9-82 is selected to be long enough to pass DFSK V_{QUAD} to the inverting input of comparator 9-85 (V_{QUAD} 9-78) but short enough to reject short term DC drifts present V_{QUAD} 9-84 due to data composition changes and to adjust quickly to the transient DC change from noise to preamble exhibited upon initial receipt of a packet. The time-constant value (τ=R3 9-82 x C3 9-86) can be about 5 μs for data rats in the megabit range. Hysteresis in the comparator circuit (provided by R_H 9-89 and R4 9-83) provides the same noise rejection characteristics as ordinary FSK and in the instant circuit may be 400 mV total for an 800 mV peak-to-peak V_{QUAD} 9-84 signal. (input offset drifts in comparators are typically below the millivolt level, while signal levels are hundreds of millivolts.) Typically, in the current best mode of the invention C3 9-86 is 470 pF; C2 9-97 is .1 μF; R1 9-80 is 1 kΩ; R2 9-87 is 1 kΩ; R3 9-82 is 10 kΩ; R4 9-83 is 33 kΩ; and R_H 9-89 is 470 Ω.

A further modification to the DFSK demodulation scheme provides for peak detection of the demodulated data pulses, since the time location of DFSK peaks tend to be more stable with variation in real media amplitude and phase attenuation characteristics. A peak detector is illustrated in Figure 9d. The peak detector consists of two sets of analog voltage comparators 9-91, 9-92, 9-93 and 9-94, one set of which (9-93 and 9-94) detects the level of the peaks of the demodulated data signal (through C3 9-95 and R3 9-96) and another set of which (9-91 and 9-92) detects the zero-slope of the peaks by differentiating the demodulated signal (through C5 9097 and R5 9-98). The time constant of C3 9-95 and R3 9-96 is selected to be longer than the data time constant (τ = 470 pF x 10 kΩ · 4.7 μs), while the time constant of C5 9-97 and R5 9-98 (τ = 68 pF x 1 kΩ = 68 ns) is selected to be short with respect to the raw data waveform V_{QUAD} Bias and reference levels for the comparators are provided by R1 9-99, R2 9-100, R6 9-101, R7 9-102, R8 9-103, and R9 9-104 providing the upper and lower peak detection reference voltages DU 9-105 and DL 9-106 for AC-coupled data VD, permitting peak detection to be performed by comparators 9-93 and 9-94. R6 9-101 and R7 9-102 provide ZU 9-107 and ZL 9-108, the upper and lower references for zero slope detection by comparators 9-91 and 9-92. The open collector outputs of the comparators require pull-up resistors (R11 9-109, R12 9-110, and R13 9-111) and may be connected in a wired-NOR configuration, which for comparators 9-91 and 9-92 provides a 1 output for zero-slope signals. The peak and zero-slope outputs are then logically ANDed by NAND gates 9-112 and 9-113 to provide trigger pulses corresponding to the positive and negative peaks of the demodulated data signal. The positive peak pulse triggers the "0" state of the RS flip flop comprising gates 9-114 and 9-115 while the negative peak pulse triggers the "1" state of said RS

flip flop. In the current best mode of the invention the components have the following values: C5 9-97 is 68 pF; C2 9-116 is .1 μF; C3 9-95 is 470 pF; R1 9-99 is 1 kΩ; R2 9-100 is 1 kΩ; R3 9-96 is 10kΩ; R5 9-98 is 1kΩ; R6 9-101 is 8.2Ω; R8 9-103 is 75Ω' R9 9-104 is 75Ω; R11 9-109 is 470Ω; R12 9-110 is 1kΩ; and R13 is 1kΩ. It should be noted that digital signal processing hardware and firmware can provide many of the demodulation and data detection functions described herein, but at the higher cost of DSP chips and A/D converter interfaces.

Figure 10 compares the frequency spectrum of FSK and DFSK modulation and illustrates the beneficial bandwidth consumption characteristic of DFSK over FSK. AT low data rates (Figure 10a) FSK is designed to produce a fixed shift or deviation determined by the two frequencies assigned to the '1' and '0' data bits, the deviation (difference) of which is determined by the demodulator transfer function or curve (illustrated in Figure 10 as f_0 and f_1). The power of the FSK transmission is divided equally (for data with equal averages of 1's and 0's) between the two frequencies. At high data rates (Figure 10b) FSK exhibits sidebands spaced from the center f_c. At high data rates (Figure 10d) DFSK exhibits sidebands of the same width as with FSK, but the magnitude of the sidebands is suppressed by as much as 10dB compared to FSK, requiring less filtering of transmitter sidebands and better propagation through receiver filters.

DFSK modulation of a carrier is easily implemented with a 5-state digital state machine (driven by a 4 x f_c clock) as illustrated in Figure 11a, because (1) only one carrier/clock frequency need be generated or synthesized (as opposed to two with FSK) and (2) the rising and falling edges of the data are used to skip or add a state to the state machine, producing a higher or lower differential frequency shift, respectively. In the case of the normal unmodulated carrier f_c (with 50/50 duty cycle), the state sequence for one carrier cycle is 1,2,3,4 with states 1 and 2 producing a high level and 3 and 4 producing a low level. A falling data edge '0' causes the state machine to add a fifth state 2' between states 2 and 3, producing the sequence of 1,2,2',3,4 and resulting in a lower differential frequency shift corresponding to falling edge '0'. Similarly, a rising data edge '1' causes the state machine to skip state 2, producing the sequence 1,3,4 and resulting in a higher differential frequency shift corresponding to rising edge '1'. Thus, the DFSK state machine and modulation technique effectively has 3 symbols: (1) the rising edge of data, (2) the falling edge of data, and (3) no data edges or state changes, which further distinguishes DFSK from other modulation techniques (FSK, QFSK, PSK, QPSK, etc.) that have 2 or 4 or more (even numbers) symbols, but not 3. It should be noted here that the 5-state digital state machine in practice employs more states to permit setup, synchronization and timing of data with carrier. Also, the assignment of data logic states to higher or lower differential frequency shifts may be reversed from the example herein without changing the substance of the invention.

Additional state machine modifications illustrated in Figure 11b permit selection of alternate data rates while keeping carrier frequency fixed by selecting a preset number n of carrier cycles per bit. A presetable divide by n counter may be added to the state machine to provide a data clock which is presetable submultiple of carrier frequency. Thus, a 6 MHz carrier would provide bit rates corresponding to n as follows: 1200 kbps for n=5, 600 kbps for n=10, 300 kbps for n=20, and 150 kbps for n=40. Selection of bit rate without changing carrier frequency by system controllers permits negotiation of bit rate for servicing a variety of device types on a network

as well as accommodating varying power line propagation characteristics. For example, a lowest cost light switch node may be implemented with 150 kbps monolithic filters and no data rate negotiability, while a moderate price point printer node may be operated at 1200 kbps with discrete wideband filters and have negotiability designed into its controller. By initiating operation of the network at 150 kbps, the n for the printer and the switch would start at 40, but as soon as the device type and node address were broadcast for a printer node, the bit rate would be negotiated upward from n=40 to n=20 until n=5 or until the bit error rate became unacceptable for the conditions of the power line medium at that time, whereupon the n and corresponding data rate would back off to an acceptable selection.

An addition advantage of the DFSK modulator is that the state machine can be configured and instructed by a data controller to produce special DFSK characters for control or compression purposes. For example, two lower differential frequency shifts could be executed in sequence to represent a string of 1's while two higher differential frequency shifts in sequence could represent a string of 0's. This feature is not possible with FSK. The state machine has no limitations on its agility regarding which states it adds or skips, as instructed. The demodulator data slicer would require some additional comparator(s) and logic/circuitry to detect successive DFSK pulses of like polarity.

An additional modification to the carrier generation and modulation state machine includes increasing the number of states to permit Multiple DFSK techniques. For example, subdividing the original 5 states by 2 doubles the number of states to 10 half-states (with a corresponding doubling of clock frequency to 8 x f_c) and permits increasing the number of symbols by 2 by skipping or adding 1 or 2 half-states. Corresponding modifications to the receiver demodulator are required to detect the differing responses to the 1 and 2 half-state symbols. Since a 1 half-state shift produces half the differential frequency shift of a 2 half-state shift, a quadrature detector produces pulses of half the amplitude for the 1 half-state shift with reference to a 2 half-state shift, which is the normal shift for standard DFSK.

A further modification to the carrier generation and modulation state machine includes modulation shaping methods that more consistently define data edges at high bit rates, which modifications either prefix or append to data symbols (a) single whole shifts or (b) 1 or 2 half-state shifts which precompensate the quadrature detector's analog data output waveform for more accurate data slicing of each data bit sequence/combination.

DFSK, while discussed in this specification, primarily in a PLC application has many similar applications in other electronic communication system, including but not limited to: RF, wired, telephone line and the equivalent. Moreover, while this discussion of DFSK implies a workstation computer device, this technology can be applied, and should be considered within the scope of this patent, to any other electronic devices with communication capabilities, including but not limited to controllers, personal computers, fax machines, printers and telephonic systems.

Figure 12 illustrates the improvement in data bit timing accuracy achieved if the data rate is synchronized with the carrier frequency f_c and clock. Figure 12 shows two data bits of identical length or rate, XMIT DATA and XMIT DATA', but shifted in phase in reference to the CARRIER modulator. XMIT DATA falling edge X0 (and X0') and rising edge X1 meet the set up windows (low state) for the modulator state machine, while the rising edge X1'

of XMIT DATA misses the setup window of the modulator state machine, delaying execution of the modulation for rising edge 1 to 1', to the next CARRIER cycle and producing a corresponding time delay/shift in rising edge RCVR DATA R1 vs. R1'. Received data bit width changes of 1 carrier cycle produce significant data errors at the high data rates of the instant invention, while prior system data rates, being at least an order of magnitude lower, have not observed this error source as significant. It should be especially noted that both rising and falling edges of data are sensitive to data synchronization with the carrier modulator and that the variation in bit width data error is especially exacerbated by data rates that are not related to the carrier frequency by an even multiple of carrier cycles. Therefore, synchronization of both data rate and phase with the carrier modulator eliminates synchronization granularity/jitter in the modulated carrier, enabling high data rates.

Another improvement that increases the reliability of detecting/receiving the bits in each byte provides a realignment bit at the end of each byte. The realignment bit resynchronizes the receiver's deserializer sampling clock with each incoming data byte to prevent clock timing skews between the transmitter data clock and the deserializer (receiver) clock, permitting low-cost clock references. This differs significantly from other packet transmission schemes such as Ethernet, which employ 20,00000 MHZ (1ppm) accurate clocks for tracking a 1500-byte-long packet. While the realignment bit improvement is similar in concept to RS-232 start and stop bits, it differs significantly from RS-232 in that (1) the polarity alternates from that of the last data bit of the byte to further distinguish its edge from the last bit, and (2) only one realignment bit per byte is required, effectively reducing the overall data rate throughput by only 11% (as compared with 25% for RS-232). This improvement permits reliable data transfers at higher data rates well beyond the 11% hit as well as increasing the maximum packet size, while still permitting the use of low-cost clock references/crystals.

Figure 13 illustrates another limiting characteristic of prior techniques using RSSI detection schemes and protocols based on RSSI signals. Figure 13 shows an MC13158 receiver data book chart for the RSSI response. In networks involving RF carrier transmissions, each node has a transmitter and a receiver, the operation of which is determined by the fundamental protocol of the network (client-server, peer-to-peer, etc.). For data transmission, only one transmitter at a time is permitted to be active on the medium and then only when the respective node has data to send. When not transmitting, each node's receiver is active, producing valid data or spurious noise depending on whether a valid transmission is present on the medium. Prior network arbitration protocols have used the presence or absence of carrier as detected by receiver RSSI circuits to determine (1) that the data output of a receiver is valid or spurious, or (2) that the medium is clear of other transmissions, permitting a node's transmitter access to the medium. In each instance the response time of the RSSI circuit limits the responsiveness of system protocols as illustrated in Figure 13. The response time exceeds 4 μs for rise time t_r (presence of carrier) and exceeds 25 μs for fall time t_f (absence of carrier) for stronger signals, varying down to 6 μs for weak signals. Since the length of a byte at 2 Mbps is 4 μs, the six times variation between rise and fall times and the long length of the fall time (exceeding 6 data bytes) create bandwidth consuming protocol delays for send/receive and intergap spacing operations when the RSSI signal is used to arbitrate transmissions.

Then there are two other problems related to the nose level of the medium, and particularly that of the power line: (1) medium noise pulses trigger counterfeit RSSI signals and false arbitration attempts and (2) the signal-to-noise ratio on the medium changes from one environment to another and at different times of the day, making it difficult for an RSSI comparator circuit to adjust its reference to remain sensitive to normally attenuated signals while ignoring false triggers.

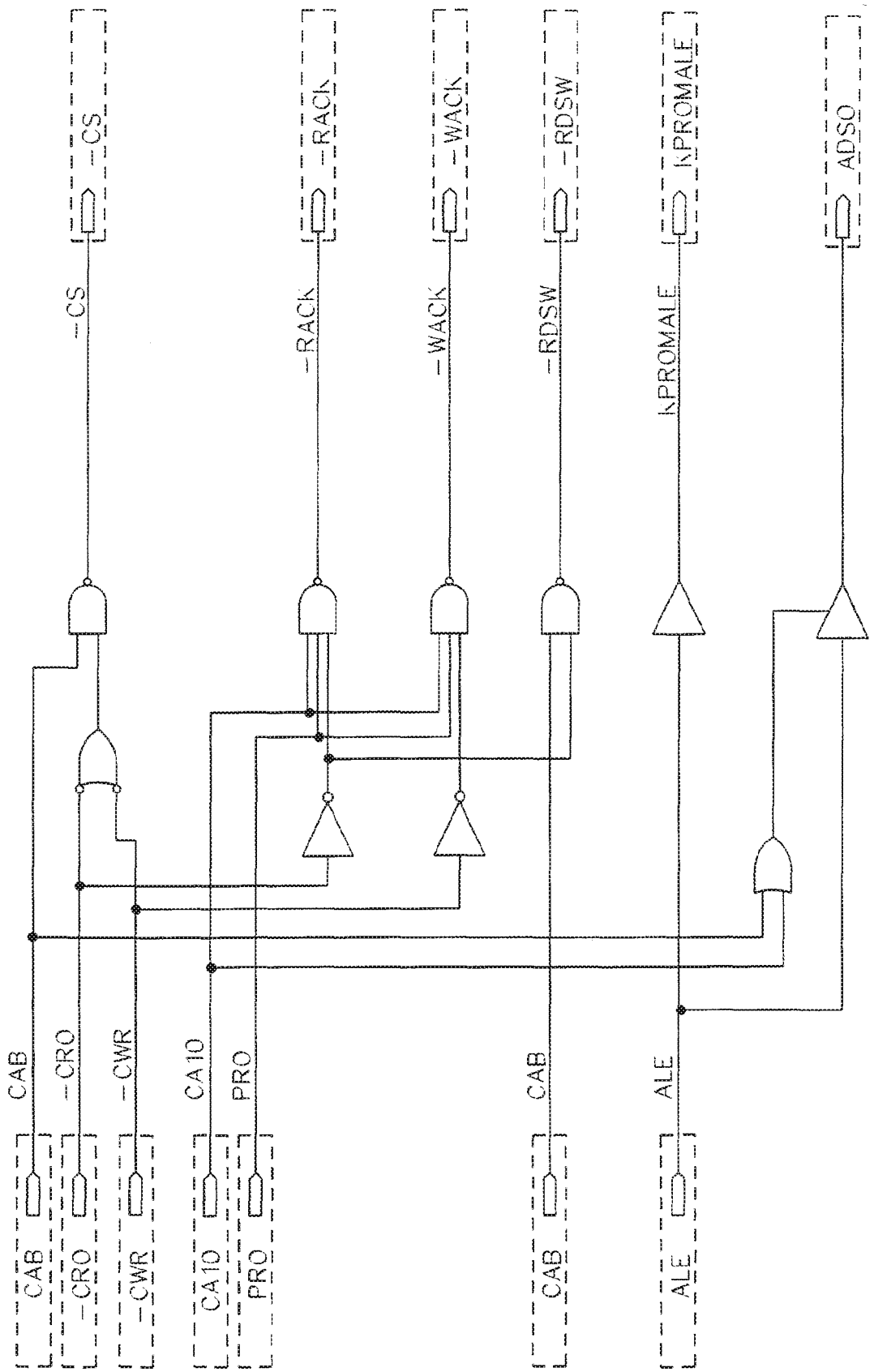
To overcome RSSI technique and circuit limitations and improve reliability of power line network arbitration the present preferred embodiment of the invention avoids the use of the RSSI signal altogether, relying instead on (1) validation of distinct data preambles to test for adequate signal-to-noise ratios and (2) special modulation symbols called FSK ACK (for Frequency Shift Key Acknowledgment) for permitting multiple nodes to acknowledge (respond) simultaneously to group polls by a network master. If the signal to noise ratio is at least 12 dB, a favorable bit error rate results in detection of valid packet preamble and start byte, packet length byte, unique node address, data payload and CRC, which together assure the reception of an accurate packet. Distinctive preamble and start bytes are chosen to permit competent comparison logic to distinguish preambles from power line noise. For example, sending a series of alternating ones and zeros (AAH) followed by a 31H (i.e., 1010101010010001) produces an acceptably unique combination for differentiating the start code from noise. Packet length bytes also provide reliable anticipation of the packet length and the end of the packet for arbitrating the next transmission by other network nodes with minimal intergap spacing. Similarly, the special FSK ACK packet described in Figure 15 permits discrimination against normal data as well as power line noise.

In relation to the detection of special FSK ACK symbols, Figure 14a illustrates several improvements over prior techniques, which are achieved by substantially increasing the IF frequency: (1) the demodulator linear frequency range is doubled, dramatically decreasing the sensitivity to the AC coupled DFSK data comparator to the temperature coefficient and mechanical tuning drifts; (2) the FSK ACKnowledgment signal detection is more robust by setting the corresponding comparator reference near a demodulator output "rail" which is also further from the DFSK carrier and noise; and (3) the IF filter is designed for flatter pass band and sharper skirts with substantially less expensive components. Extending the linear range of the quadrature demodulator transfer function (for IF frequency vs. V_{QUAD} voltage out) permits a wider range of temperature coefficient/mechanical drift and tolerance on parts from the transmitter to the receiver. Extending the frequency range of the demodulator rails also extends the FSK ACK frequency range, which is judiciously placed near or onto a rail, providing a more robust deviation in FSK ACK frequency from the DFSK carrier to help discriminate against noise in the carrier range. A DC coupled comparator (FSK data slicer) may then be employed because the rail tends to act as a limiter on V_{QUAD} as it responds to the FSK ACK frequency, permitting the FSK ACK comparator reference to be placed in the linear range next to a rail with sufficient margin to accommodate temperature coefficient drifts and noise, as illustrated in Figure 14b. Another reason the FSK comparator works well for FSK ACK detection is that the data rate of an FSK ACK signal is designed to be much lower than for DFSK data. Placing the IF at a substantially higher frequency also provides the advantage of making IF filter design more practical for obtaining wider and flatter pass bands (and sharper skirts for rejection of out of band interference) with economical commercial components.

Figure 15 illustrates how DFSK permits the compatible use of FSK to produce special characters that may be used for group acknowledgment of requests for status of slave devices in a network. At t1 to t3 normal DFSK operation at the end of a packet is illustrated with corresponding DFSK DATA. During t3 to t4 the carrier of the master drops and the noise level of the medium creates false DATA which is rejected as invalid data by the receive data controller because it does not meet the start of packet requirements for a data packet nor does it meet the FSK ACK requirements for an ACK packet. But at t4 an FSK ACK packet begins in which the unmodulated DFSK carrier is employed as one frequency f0 for a byte (t4 to t5) and the second FSK ACK frequency acts as f1 for several bytes (t5 to t6). From t6 to t7 the ACK packet returns to f0 for the length of a byte, following which carrier transmission ceases and the data and ACK signals detect the noise level of the medium at t8 to t11. No realignment bit is required in the ACK packets. By reducing the data rate (from bits to bytes or to the lowest bit rate of the network) of the ACK protocol, at least two transmissions of equal strength may be detected simultaneously, which can occur when several remote devices in a network group respond simultaneously to a group poll. Frequencies must be within 10 kHz, which for a 5 MHZ carrier is a reasonable 0.2% (2000 PPM). Commercial crystals are available with 50 ppm tolerances at low cost. It may also be noted that the judicious use of the FSK ACK symbols and protocol avoids the use of the unreliable RSSI signal for group ACKs as described herein.

Because the FSK, ACK signal permits discrimination against normal data as well as medium noise, this advantage permits an FSK ACK packet to be employed, modified or unchanged, for other signaling applications in a network or control system. For example, in a master/slave network, the FSK ACK could provide an interrupt when a slave node requires the services of a master, which reduces polling frequency. The slave node's own address could be appended to the end of the DFSK trailer on the FSK ACK packet, reducing polling operations. Or in a peer to peer system, the FSK ACK could be used to notify other users of its intent to broadcast on the medium or to pass tokens. Changing the length of the FSK portions of the FSK ACK packet could provide control or identification data to other network devices.

It is to be understood that the above described embodiments of the invention are merely indicative of the inventors' current best mode of the invention and are illustrative of numerous and varied other embodiments which may constitute applications of the principles of the invention. Such other embodiments may be readily devised by those skilled in the art without departing from the spirit or scope of this invention and it is our intent that they be deemed within the scope of our invention.



ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
1	C	rackl	[,130]		130	<,0> <,0>	83902A Read Strobe to -ACK Low (2*bcyc + 30) only 2 wait states allowed
2	C	rackh	[,30]		30	<,0>	83902A Read Strobe to -ACK High
3	C	ackdv	[,55]		55	<,0>	83902A Acknowledge Low to Data Valid
4	C	rdz	[15,70]	15	70	<54.67,0.33>	83902A Read Strobe to Data TRI-STATE
5	C	ww	[50,]	50		<0,>	83902A Write Strobe Width from -ACK
6	C	rwds	[20,]	20		<0,>	83902A Register Write Data Setup
7	C	rwdh	[21,]	21		<0,>	83902A Register Write Data Hold
8	C	wackh	[,30]		30	<,0>	83902A Write High to -ACK High
9	C	wackl	[,130]		130	<,0>	83902A Write Low to -ACK Low
10	C	rsrs	[10,]	10		<0,>	83902A Register Select to Read Setup
11	C	rsrh	[0,]	0		<2.77,>	83902A Register Select Hold from Read
12	C	rswh	[0,]	0		<1.87,>	83902A Register Select Hold from Write
13	C	rsws	[15,]	15		<0,>	83902A Register Select to Write Setup (assumes ADS0 high when RA lines)
14	C	bch	[20,]	20		<5,>	83902A Bus Clock High Time
15	C	bcl	[20,]	20		<5,>	83902A Bus Clock Low Time
16	C	asds	[,30]		30	<,0>	83902A Address Strobe to Data Strobe (bcl+10)
17	C	bcrl	[,43]		43	<,0>	83902A Bus Clock to Read Strobe Low
18	C	bcrh	[,40]		40	<,0>	83902A Bus Clock to Read Strobe High
19	C	avrh	[132,]	132		<0,>	83902A Address Valid to Read Strobe High

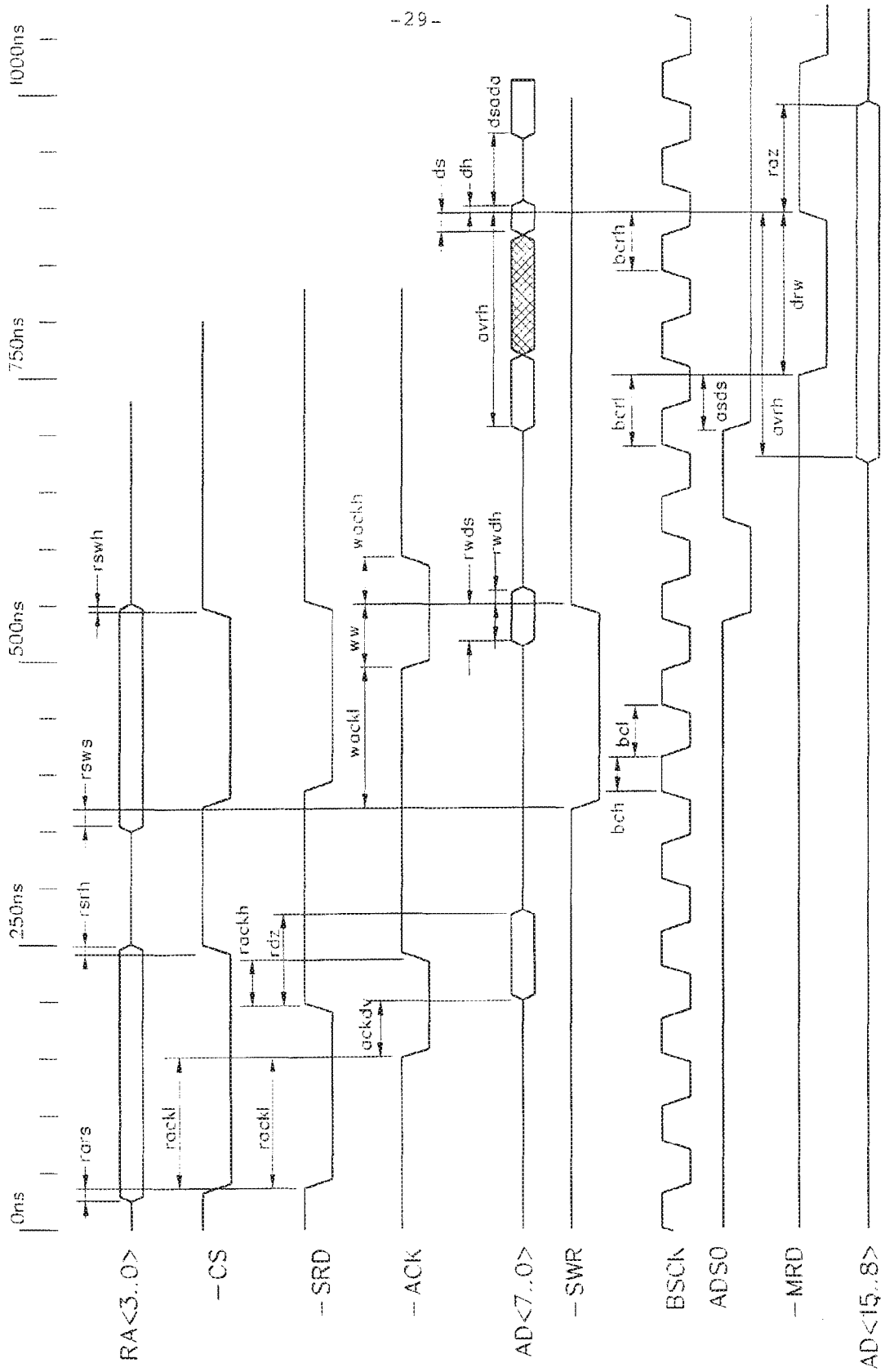
ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
20	C	avrh	[132,]	132		<0,>	83902A Address Valid to Read Strobe High
21	C	ds	[22,]	22		<0,>	83902A Data Setup to Read Strobe High
22	C	drw	[85,]	85		<12,>	83902A DMA Read Strobe Width Out
23	C	dh	[0,]	0		<3,>	83902A Data Hold from Read Strobe High
24	C	dsada	[40,]	40		<0,>	83902A Data Strobe to Address Active
25	C	raz	[90,]	90		<0,>	Memory Read High to Address TRI-STATE

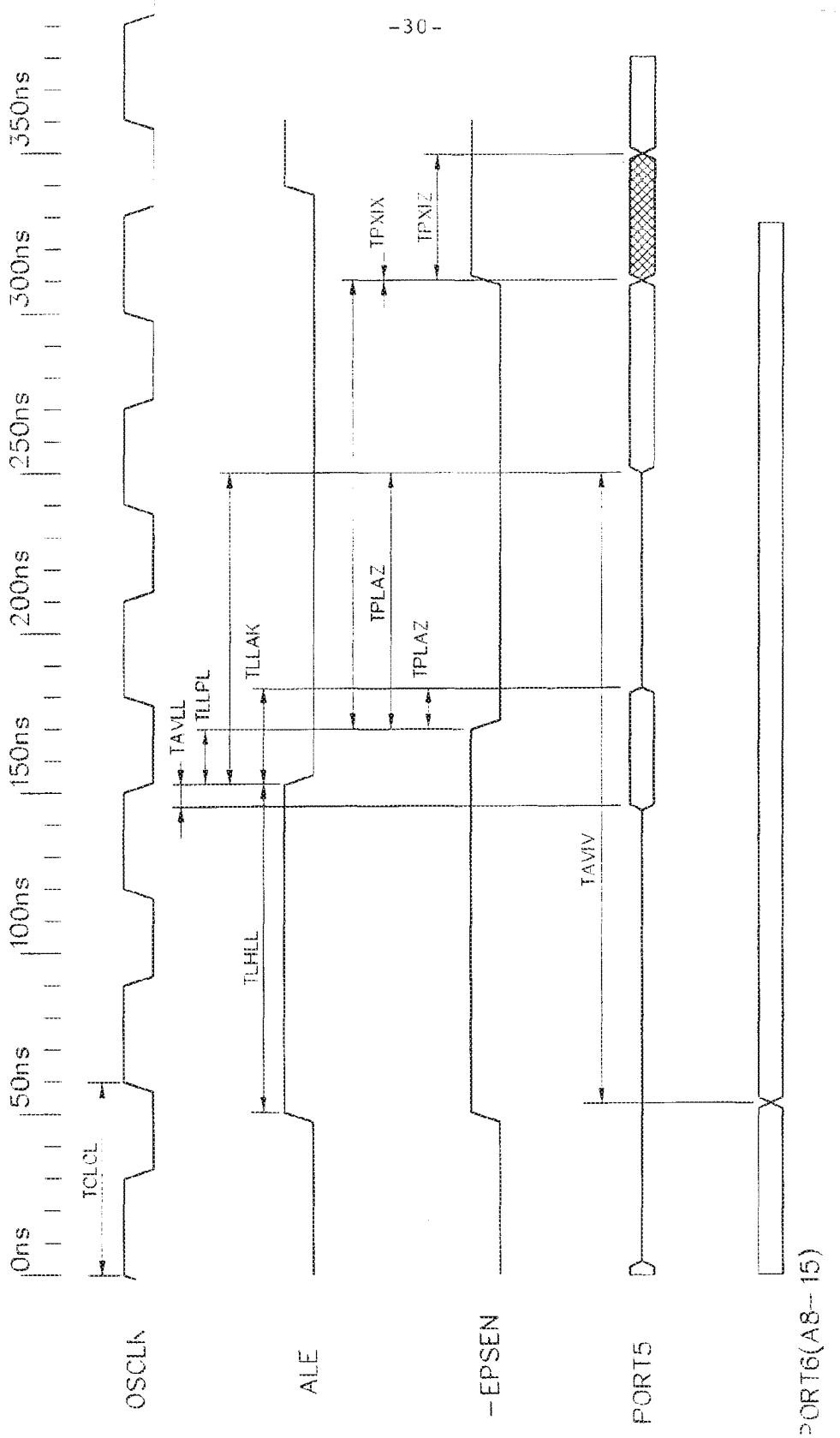
ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
1	C	TLHLL	[min(((2*TCLCL)-40)),]	81.21		<21.49,>	8X152 ALE PULSE WIDTH
2	C	tLL	[50,]	50		<52.70,>	8764 Chip DeSelect Width (87C64-1)
3	V	TCLCL	[60.61,]	60.61			8X152 OSCILLATOR CLOCK PERIOD
4	C	TCLCL	[60.61,]	60.61		<0,>	8x152 OSCILLATOR CLOCK PERIOD
5	C	TAVLL	[min((TCLCL-55)),]	5.61		<0,>	8X152 Address Valid to ALE Low
6	C	tAL	[25,]	25		<-19.39,>	8764 Address to -CE Latch Set-up
7	C	TLLAX	[min((TCLCL-35)),]	25.61		<5,>	8X152 Address Hold After ALE Low
8	C	tLA	[30,]	30		<0.61,>	8764 Address Hold from -CE Latch
9	C	TLLIV	[,min(((4*TCLCL)-100))]		142.42	<,45.41>	8X152 ALE Low to Valid Instruction In
10	C	tACL	[,150]		150	<,52.99>	8764 CE Latch Access Time
11	C	TLLPL	[min((TCLCL-40)),]	20.61		<0,>	8X152 ALE Low to -EPSEN Low
12	C	tCOE	[30,]	30		<-9.39,>	8764 ALE/-CE to Output Enable
13	C	TPLPH	[min(((3*TCLCL)-45)),]	136.82		<0,>	-EPSEN Pulse Width

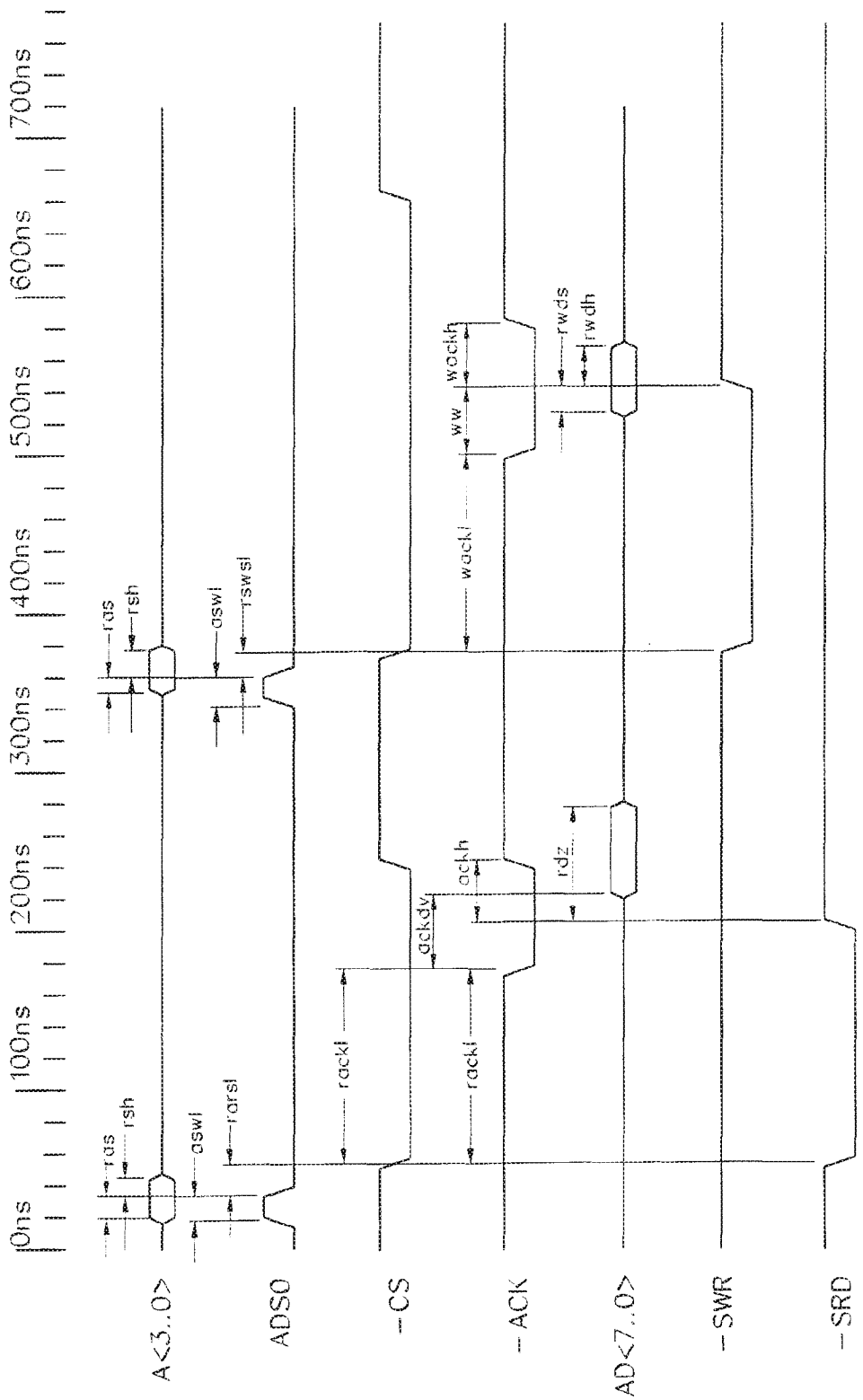
ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
1	C	TLHLL	[min(((2*TCLCL)-40)),]	81.21		< 21.49, >	8X152 ALE PULSE WIDTH
2	V	TCLCL	[60.61,]	60.61			8X152 OSCILLATOR CLOCK PERIOD
3	C	TCLCL	[60.61,]	60.61		< 0, >	8x152 OSCILLATOR CLOCK PERIOD
4	C	TAVLL	[min((TCLCL-55)),]	5.61		< 0, >	8X152 Address Valid to ALE Low
5	C	TLLAX	[min((TCLCL-35)),]	25.61		< 5, >	8X152 Address Hold After ALE Low
6	C	TLLIV	[,min(((4*TCLCL)-100))]		142.42	< ,45.41 >	8X152 ALE Low to Valid Instruction In
7	C	TLLPL	[min((TCLCL-40)),]	20.61		< 0, >	8X152 ALE Low to -EPSEN Low
8	C	TPLPH	[min(((3*TCLCL)-45)),]	136.82		< 0, >	-EPSEN Pulse Width
9	C	TPLIV	[,min(((3*TCLCL)-105))]		76.82	< ,0.4 >	8X152 -EPSEN Low to Valid Instruction In
10	C	TPLAZ	[,10]		10	< ,0 >	8X152 -EPSEN Low to Address Float
11	C	TPXIX	[0,]	0		< 0, >	8X152 Input Instruction Hold After -EPSEN
12	C	TPXIZ	[,min(((5*TCLCL)-25))]		278.03	< ,242.43 >	8X152 Input Instruction Float After - EPSEN
13	C	TAVIV	[,min(((5*TCLCL)-105))]		198.03	< ,0 >	8X152 Address to Valid Instruction In

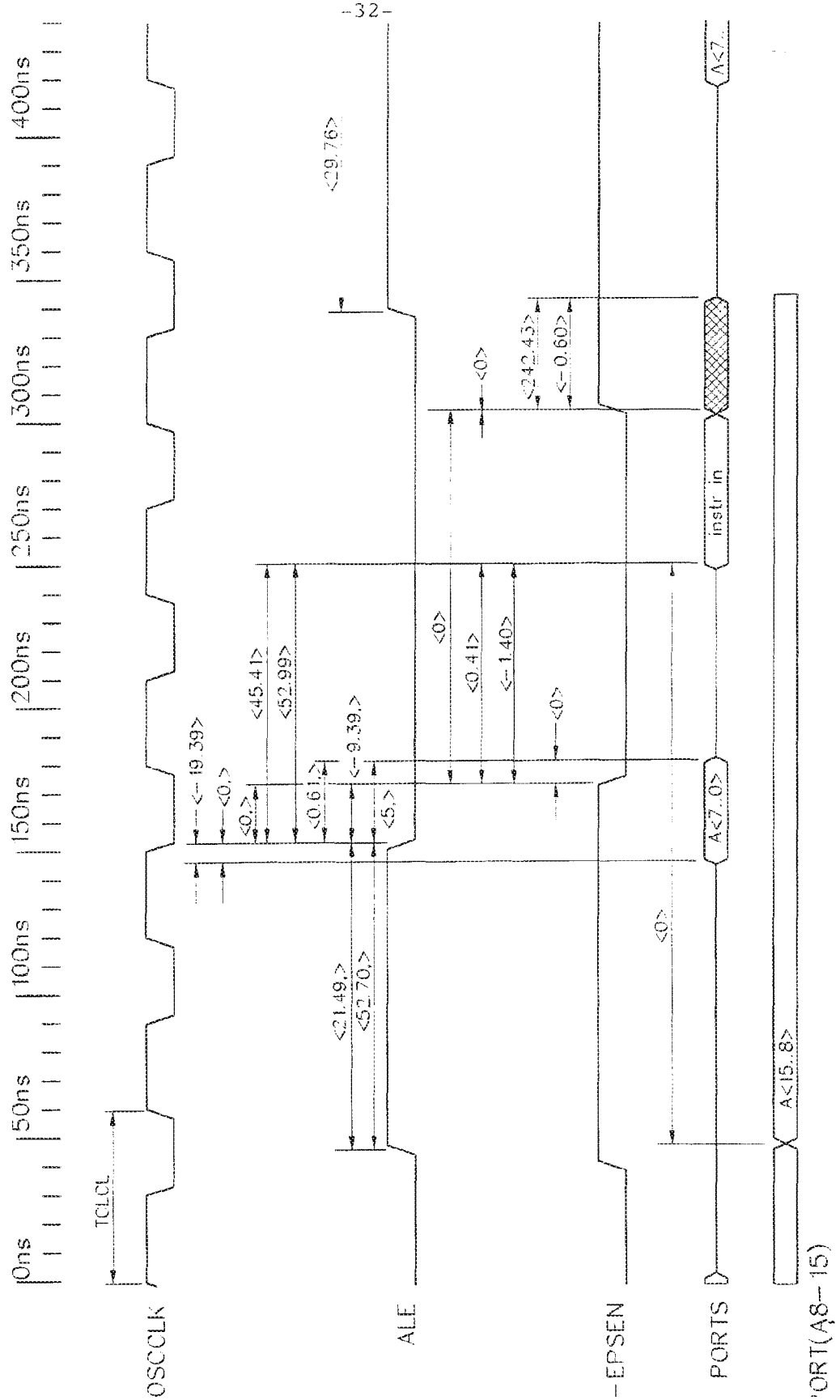
ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
1	C	TLHLL	[min(((2*TCLCL)-40)),]	81.21		<0,>	8X152 ALE PULSE WIDTH
2	V	TCLCL	[60.61,]	60.61			8X152 OSCILLATOR CLOCK PERIOD
3	C	TCLCL	[60.61,]	60.61		<0,>	8x152 OSCILLATOR CLOCK PERIOD
4	C	TAVLL	[min((TCLCL-55)),]	5.61		<0,>	8X152 Address Valid to ALE Low
5	C	TLLAX	[min((TCLCL-35)),]	25.61		<0,>	8X152 Address Hold After ALE Low
6	C	TLLDV	[,max(((8*TCLCL)-150)))]			<,>	8X152 ALE Low to Valid Data In
7	C	TAVDV	[,max(((9*TCLCL)-165)))]			<,>	8X152 Address to Valid Data In
8	C	TWHLH	[min((TCLCL-40)),max((TCLCL+40)))]	20.61		<0,>	-RD or -WR High to ALE High
9	C	TLLWL	[min(((3*TCLCL)-50)),max(((3*TCLCL)	131.82		<0,><0,>	8X152 ALE Low to -RD or -WR Low
10	C	TRLRH	[min(((6*TCLCL)-100)),]	263.64		<0,>	8X152 -RD Pulse Width
11	C	TRLDV	[,max(((5*TCLCL)-165)))]			<,>	8X152 -RD Low to Valid Data In
12	C	TRHDZ	[,max((2*TCLCL)-70))]			<,>	8X152 Data Float after -RD
13	C	TRLAZ	[,0]		0	<,0>	8X152 -RD Low to Address Float
14	C	TRHDX	[0,]	0		<0,>	8X152 Data Hold after -RD
15	C	TAVWL	[min(((4*TCLCL)-130)),]	112.42		<25.01,>	8X152 Address to -RD or -WR Low

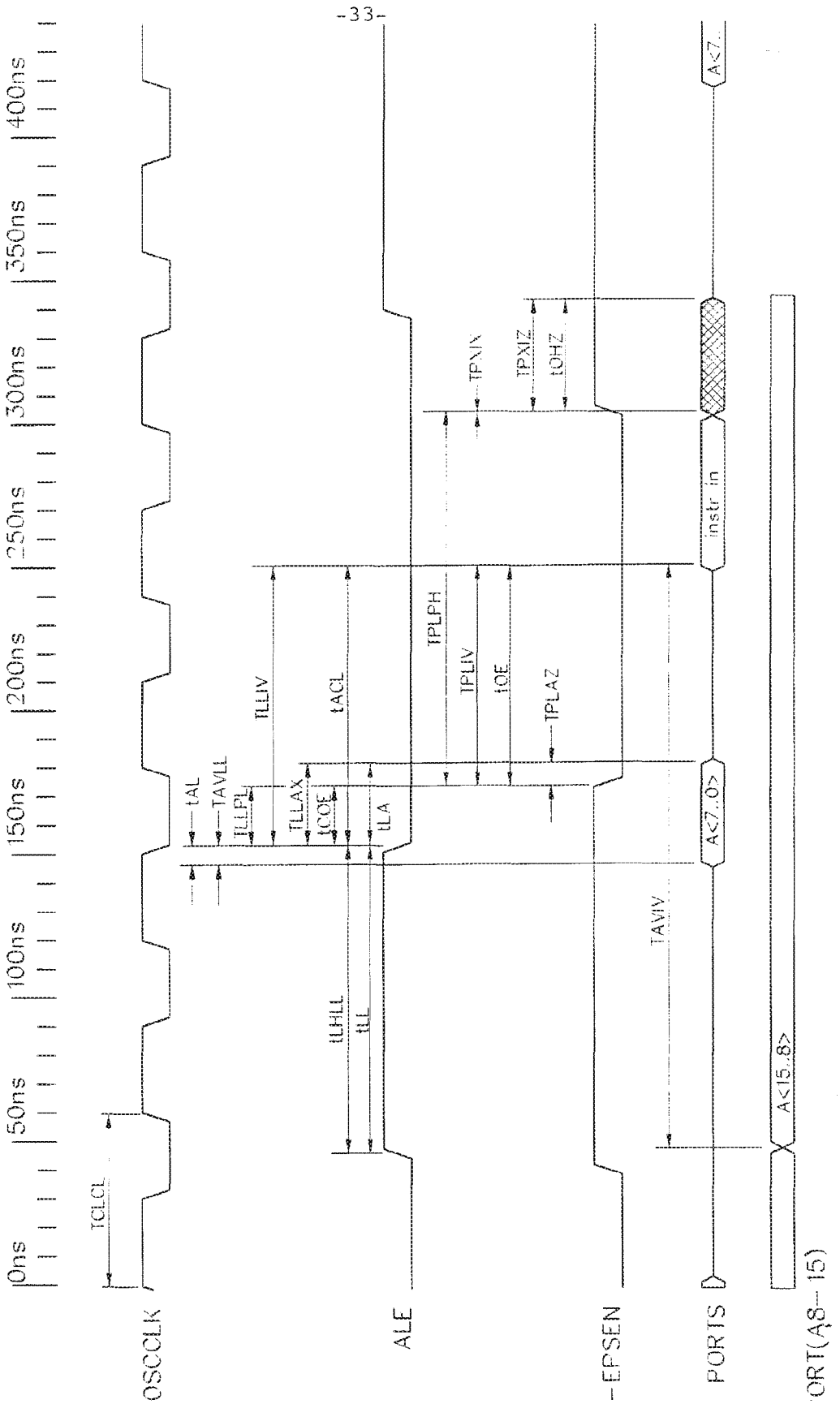
ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
16	C	TWLWH	[min(((6*TCLCL)-100)),]	263.64		<0,>	8X152 -WR Pulse Width

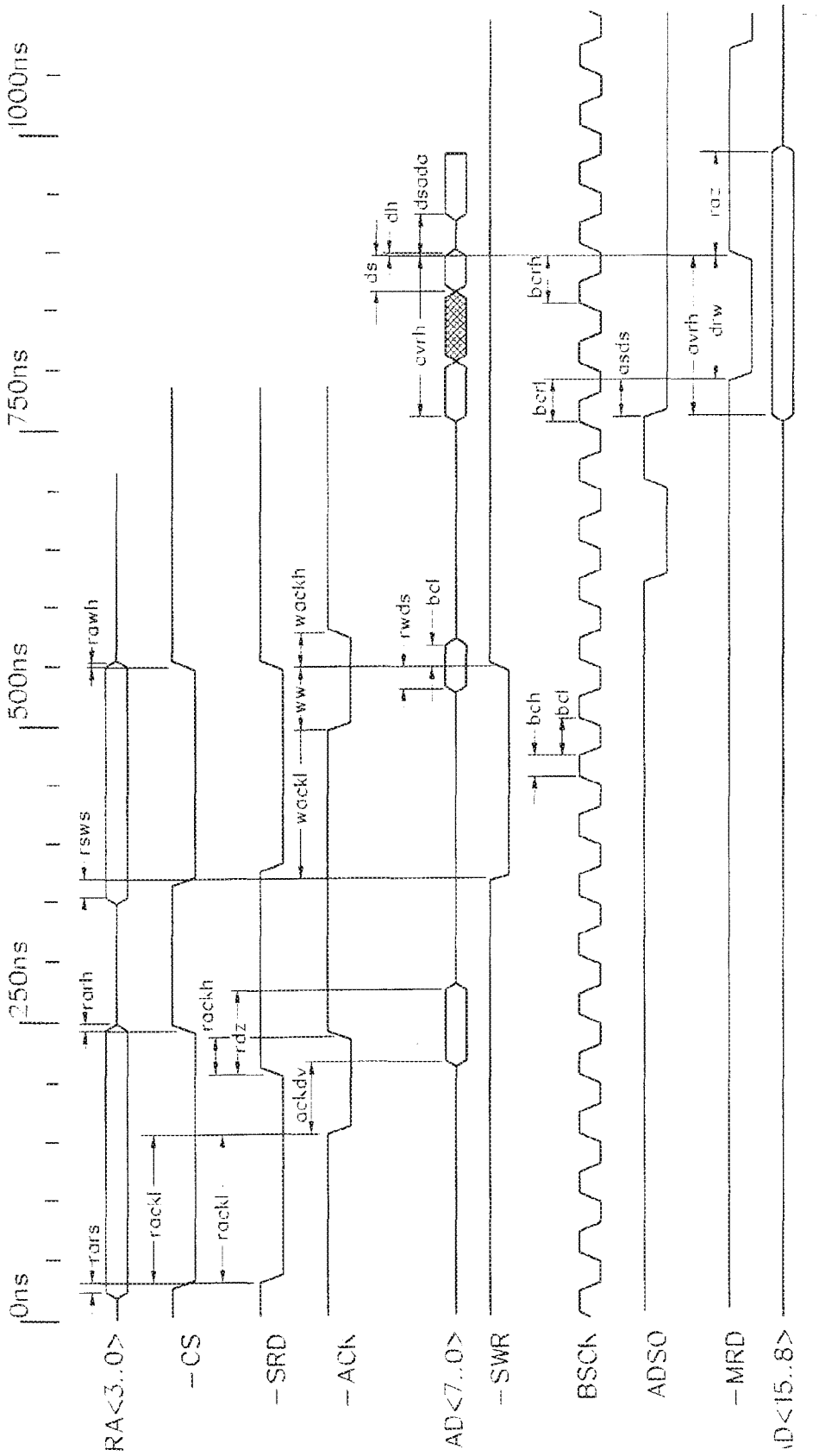


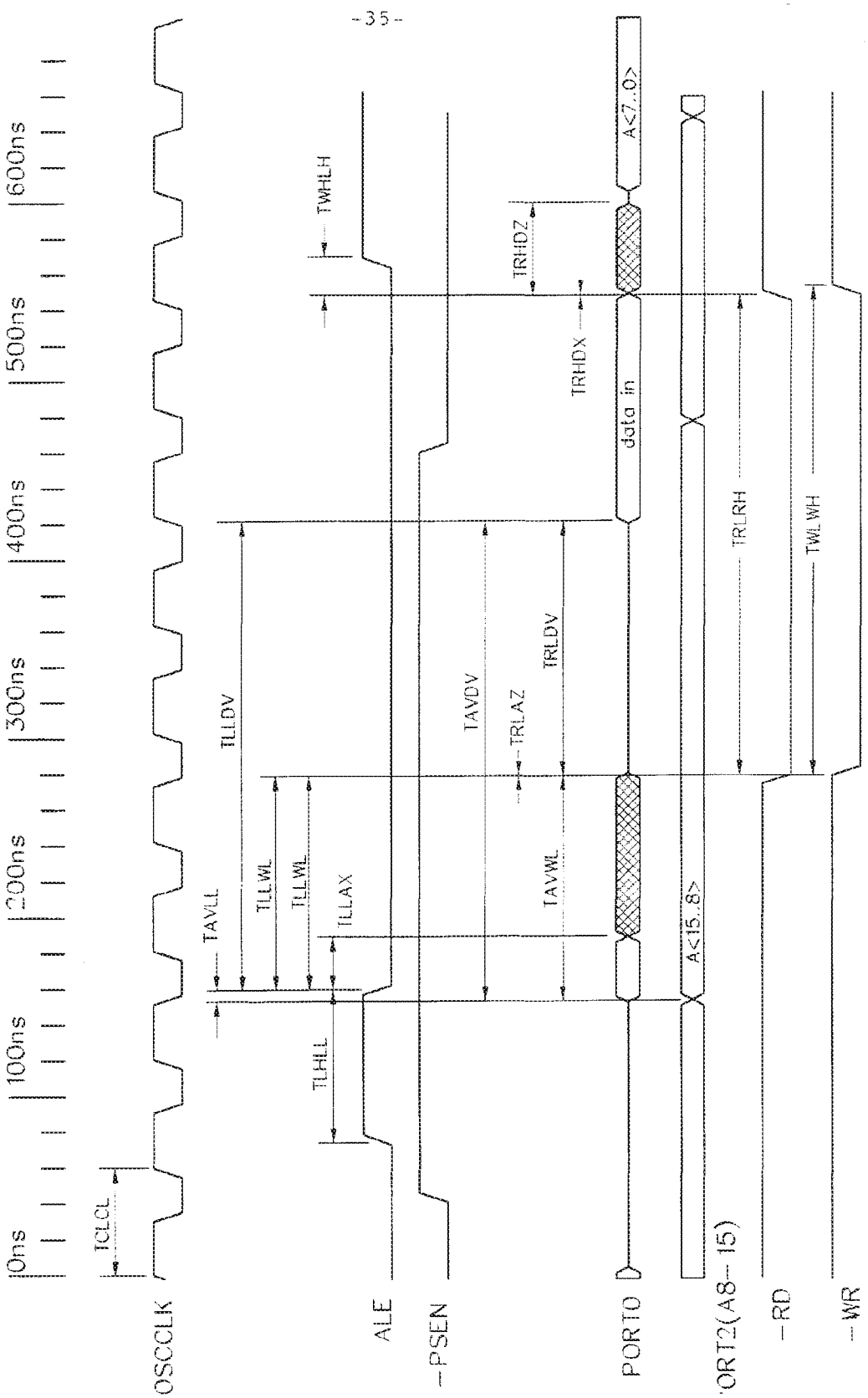












WHAT IS CLAIMED IS:

1. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, each comprising:

a. an interface, connecting said repeater to an AC power line;

b. a transceiver, electrically connected to said coupler for receiving data from said coupler, wherein said transceiver further comprises:

i. a data modulator to convert digital data to analog data;

ii. a transmitter to receive the analog data from said data modulator and prepare the analog data for transmission on the power lines;

iii. a transmit filter receiving the analog data from said transmitter and filtering the resulting analog signal to transmission on the power lines;

iv. a receiver filter receiving an analog signal from the power lines;

v. a receiver receiving the filtered analog signal from said receiver filter and demodulating and digitizing said analog signal, wherein said demodulation incorporates frequency shift key (FSK) and differential frequency shift key (DFSK) technology; and

vi. a data buffer receiving said digitized data from said receiver;

c. controller, electronically connected to said transceiver, receiving data from said data buffer and sending data to said data modulator, to provide digital control to said transceiver; and

d. an interface electrically connected to said controller for transferring digital data to a computer.

2. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said transceiver further comprises:

a. a re-synchronizer to synchronize data received by said receiver.

3. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said transceiver receiver further comprises:

a. a DSFK data detector.

4. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said transceiver receiver further comprises:

a. an acknowledge signal created from a FSK carrier signal.

5. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said transceiver receiver further comprises:

a. a DFSK edge detector.

6. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said transceiver receiver further comprises:

a. a DFSK peak detector.

7. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said controller further comprises:

a. a serializer/deserializer to serialize and deserialize the data as well as insert realignment bits and CRC logic.

8. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, comprising:

a. a means for coupling between a local area network and an AC power line for transmitting and receiving data;

b. a means for modulating a transmission carrier with network data and demodulating a transmission carrier to recover network data, said means including a means for performing differential frequency shift key modulation;

c. a means for providing noise immunity to the transferred data; and

d. a means for providing synchronization of the transferred data.

9. A local area network repeater system for transmitting and receiving network data between repeater, comprising a controller, wherein said controller includes a state machine which permits the selection of a wide range of data rates without requiring the modification of carrier frequency.

10. A local area computer network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, each comprising:

means for coupling a local area network interface to a local area computer network or network segment for transmitting a bi-directional network data stream, said data stream having a bitrate of up to 2 megabits per second and a data bandwidth approximately equal to said bitrate;

means for frequency shift key modulating a transmission carrier with said network data stream and demodulating said frequency shift key modulated transmission carrier to recover network data, said frequency shift key modulated transmission carrier having an instantaneous frequency bandwidth which is not substantially greater than the greater of either about twice said data bandwidth or the frequency deviation of said frequency shift key modulation, said means comprising a receiver chip which utilizes at least one stage of gain and filter, and said means providing at least about 90 decibels of gain;

means for coupling bi-directional network data between said network interface and said carrier modulation and demodulation means; and

means for coupling said transmission carrier to an AC power line to produce a power line carrier signal having a frequency in the range from about 2 to about 20 megahertz.

11. A local area network repeater system as recited in claim 1 wherein said local area network interface comprises a network interface selected from the following:

Ethernet network interface controller means;

Token ring network interface controller means;

Arcnet network interface controller means;

RS-232 interface controller means;

RS-485 network interface controller means;

Serial data, open standard interface; and

Parallel data interface.

12. A local area network repeater system as recited in claim 1 wherein said transmission carrier modulation and demodulation means further comprises transmission means selected from the following:

Time domain multiple access means wherein carrier data modulation and transmission is alternated with carrier data demodulation and data reception, said modulation and demodulation carriers operating on the same frequency; and

Frequency domain multiple access means wherein said carrier data modulation and transmission utilizes one carrier frequency and said carrier data demodulation and reception utilizes a second frequency.

13. A local area network repeater system as recited in claim 1 further comprising repeater controller means for performing control functions selected from among the following:

initializing and controlling said network interface means, as required to permit transparent repeating of network data over the AC power line;

monitoring said data modulated transmission carriers and arbitrating data transmissions to permit only one repeater at a time to transmit a carrier of a particular frequency onto the AC power line; and

attaching and removing data preambles and addresses; reformatting data, encrypting and decrypting data, and providing alternate data communications ports.

14. A repeater system for transmission of high frequency computer data signals through an AC power line, the system comprising a plurality of repeaters, each repeater comprising:

means for coupling input signals and output signals to a signal port;

carrier modulation means for frequency shift key modulating a transmission carrier with said input signals to produce a modulated signal having a bitrate of up to 2 megabits per second and a data bandwidth approximately equal to said bitrate, said modulated signal having an instantaneous bandwidth which is not substantially greater than the greater of either about twice said data bandwidth or the frequency deviation of said frequency shift key modulation;

demodulation means for demodulating said modulated signal to recover said output signals, said modulation means further comprising means for changing the resonant frequency produced by an oscillator in response to an input signal by driving an output port of the oscillator;

said demodulation means further comprising means for providing at least about 90 decibels of gain;

means for coupling bi-directional signals between said signal port and said carrier modulating and demodulation means; and

means for coupling said transmission carrier to the AC power line to produce a power line carrier signal having a frequency in the range from about 2 to about 20 megahertz.

15. A method for power line carrier data transmission, said method comprising the steps of:

generating a carrier signal at a frequency in the range of from about 2 to 20 megahertz;

frequency shift key modulating said carrier signal to provide a modulated carrier signal having a data bitrate of up to 2 megabits per second and a data bandwidth approximately equal to said bitrate, said modulated carrier signal having an instantaneous bandwidth which is not substantially greater than the greater of either about twice said data bandwidth or the frequency deviation of said frequency shift key modulation; and

coupling the frequency shift key modulated carrier signal onto an ac power line.

16. The method of claim 8, further comprising the steps of:

coupling the modulated carrier signal off of the AC power line; and

demodulating the carrier signal.

17. The method of claim 8, wherein said modulating step comprises modulating the carrier signal to correspond to a digital data signal.

18. The method of claim 8, wherein said modulating step comprises modulating the carrier signal to correspond to an analog data signal.

19. The method of claim 8, wherein said modulating step comprises buffering with multi-stage transmitter drivers.

20. The method of claim 9, wherein said demodulating step comprises filtering the carrier signal in stages.

21. The method of claim 8, further comprising the collision avoidance steps of:

listening for traffic on the AC power line; and

selecting between (a) transmitting an access request after detecting termination of a transmission, and (b) beginning data transmission after detecting no other traffic.

22. An embedded PLC communications system comprising a plurality of networked communications devices, each of said communications devices comprising:

an embedded microcontroller having a communication port;

carrier modulation means for frequency shift key modulating a transmission carrier with data signals from said communication port to produce a modulated carrier, said modulated carrier having a bitrate of up to 2 megabits per second and a data bandwidth approximately equal to said bitrate, said modulated carrier having an instantaneous bandwidth which is not substantially greater than the greater of either about twice said data bandwidth or the frequency deviation of said frequency shift key modulation; and

a receiver comprising a demodulator for demodulating said modulated carrier to recover corresponding data signal, said receiver comprising at least one intermediate frequency gain and filtering stage utilizing an intermediate frequency in the range from about 2 to about 20 megahertz and providing a receiver gain of at least about 90 decibels;

means for coupling said data signals between said communication port and said carrier modulation means; and

means for coupling said modulated carrier to an AC power line.

23. The system of claim 17, further comprising network arbitration and control means.

24. The system of Claim 17, wherein said means for coupling said transmission carrier to an AC power line comprises an existing AC power cord.

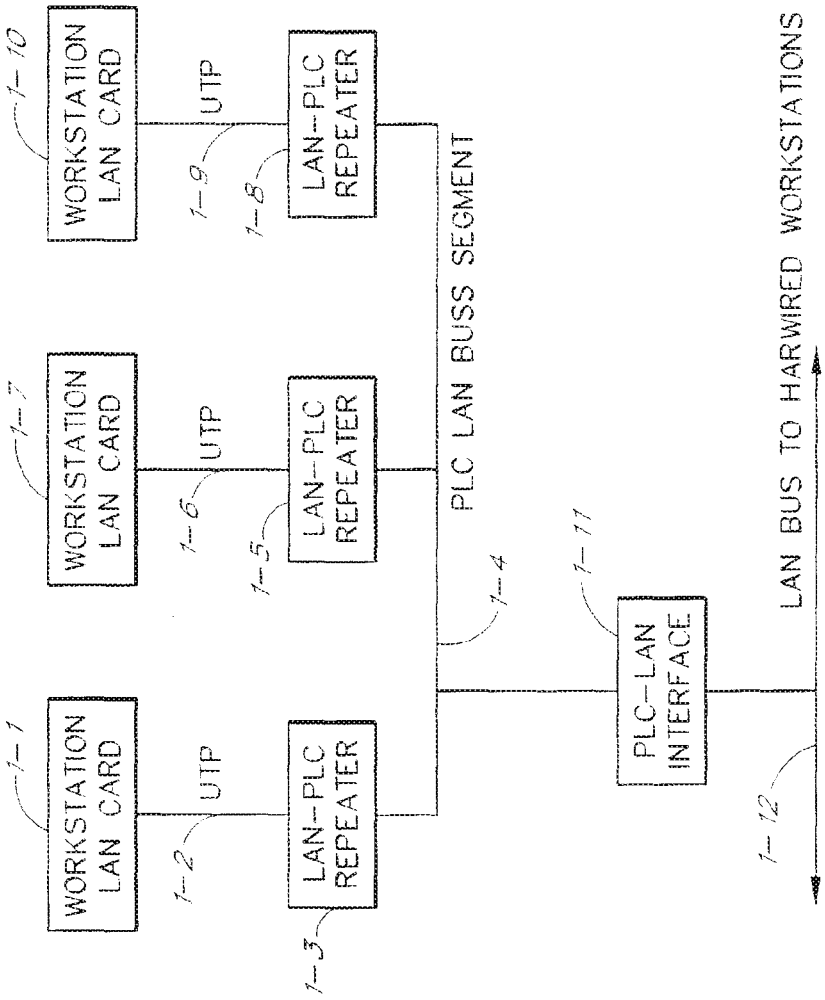

WORKSTATION LAN CARD
1-1
UTP
1-2
LAN-PLC REPEATER
1-3
WORKSTATION LAN CARD
1-7
UTP
1-6
LAN-PLC REPEATER
1-5
WORKSTATION LAN CARD
1-10
UTP
1-9
LAN-PLC REPEATER
1-8
PLC LAN BUSS SEGMENT
1-4
PLC-LAN INTERFACE
1-11
LAN BUS TO HARWIRED WORKSTATIONS
1-12

FIG. 1

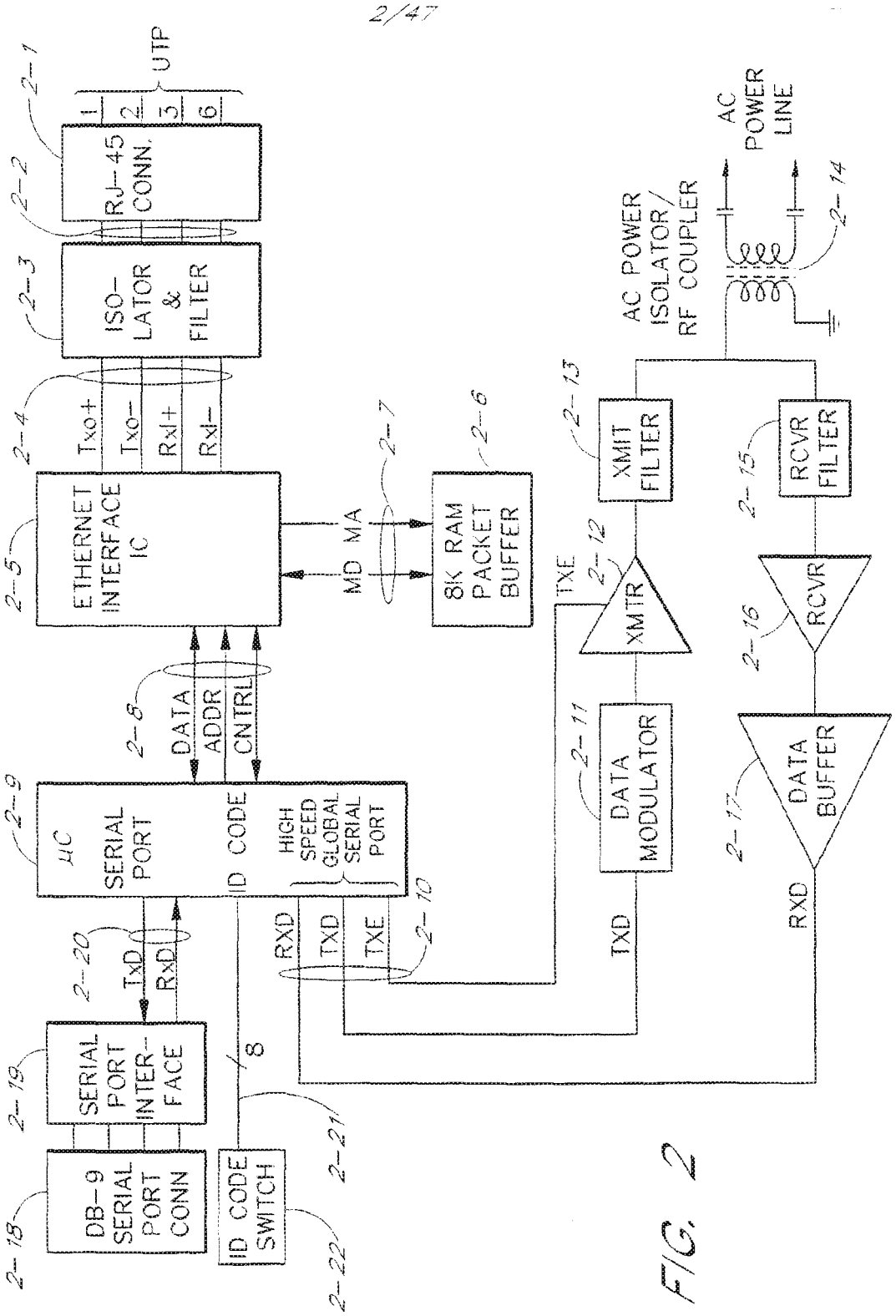

2-1
UTP
1
2
3
6
2-2
RJ-45 CONN.
2-3
ISO-LATOR & FILTER
2-4
Txo+
Txo-
Rxi+
Rxi-
2-5
ETHERNET INTERFACE IC
MD MA
2-7
2-6
8K RAM PACKET BUFFER
2-8
DATA
ADDR
CNTRL
2-9
µC SERIAL PORT
ID CODE
HIGH SPEED GLOBAL SERIAL PORT
2-10
RXD
TXD
TXE
2-11
DATA MODULATOR
2-12
XMTR
2-13
XMIT FILTER
AC POWER ISOLATOR/ RF COUPLER
AC POWER LINE
2-14
2-15
RCVR FILTER
2-16
RCVR
2-17
DATA BUFFER
2-20
TXD
RXD
2-19
SERIAL PORT INTER-FACE
2-18
DB-9 SERIAL PORT CONN
8
2-21
ID CODE SWITCH
2-22

FIG. 2

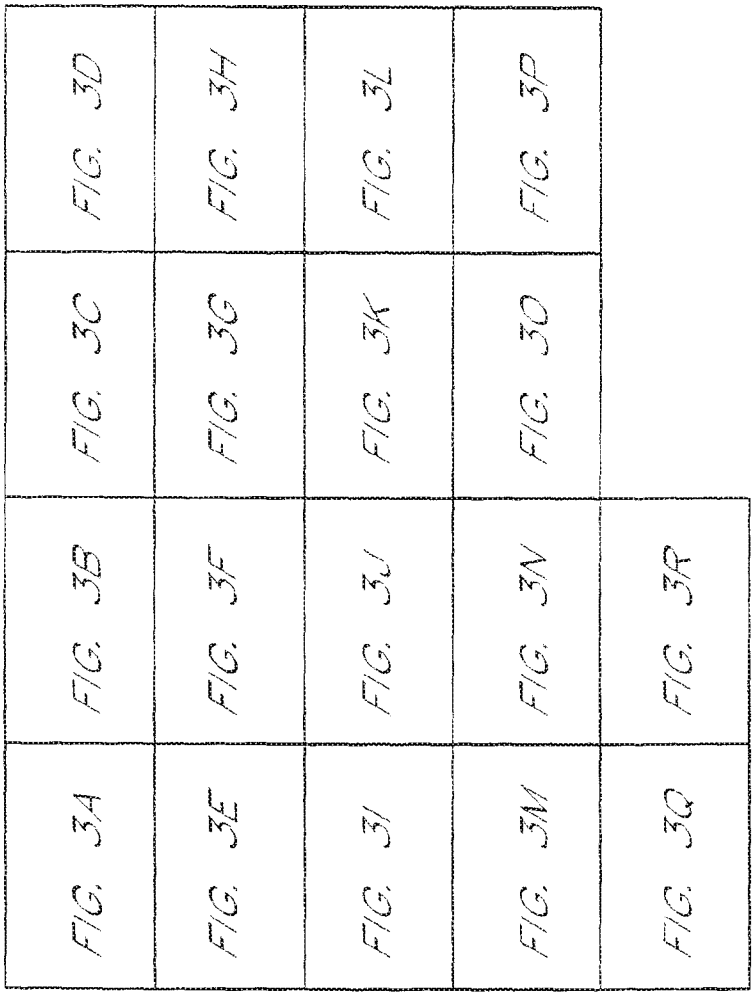


FIG. 3A
FIG. 3B
FIG. 3C
FIG. 3D
FIG. 3E
FIG. 3F
FIG. 3G
FIG. 3H
FIG. 3I
FIG. 3J
FIG. 3K
FIG. 3L
FIG. 3M
FIG. 3N
FIG. 3O
FIG. 3P
FIG. 3Q
FIG. 3R

FIG. 3

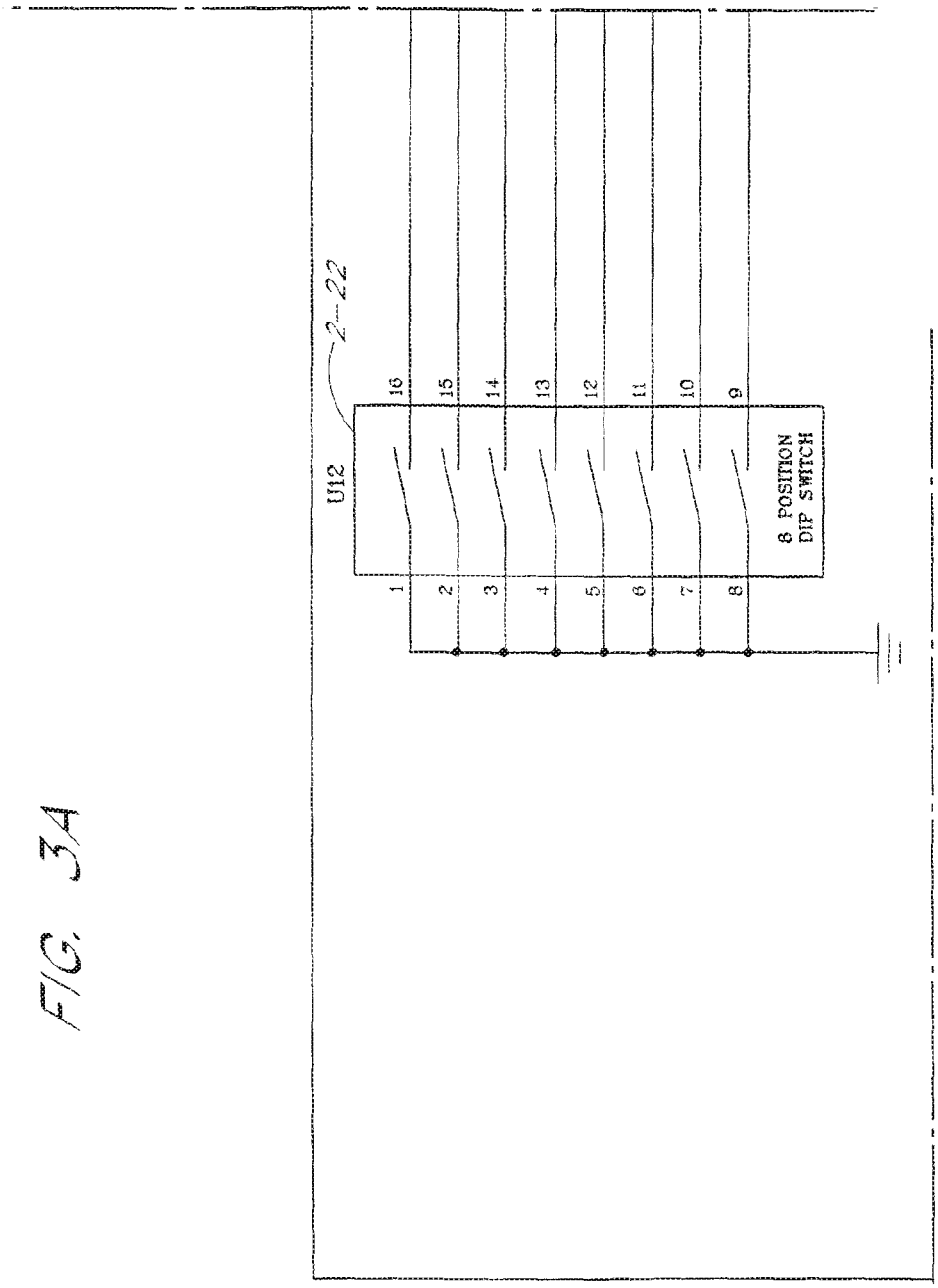
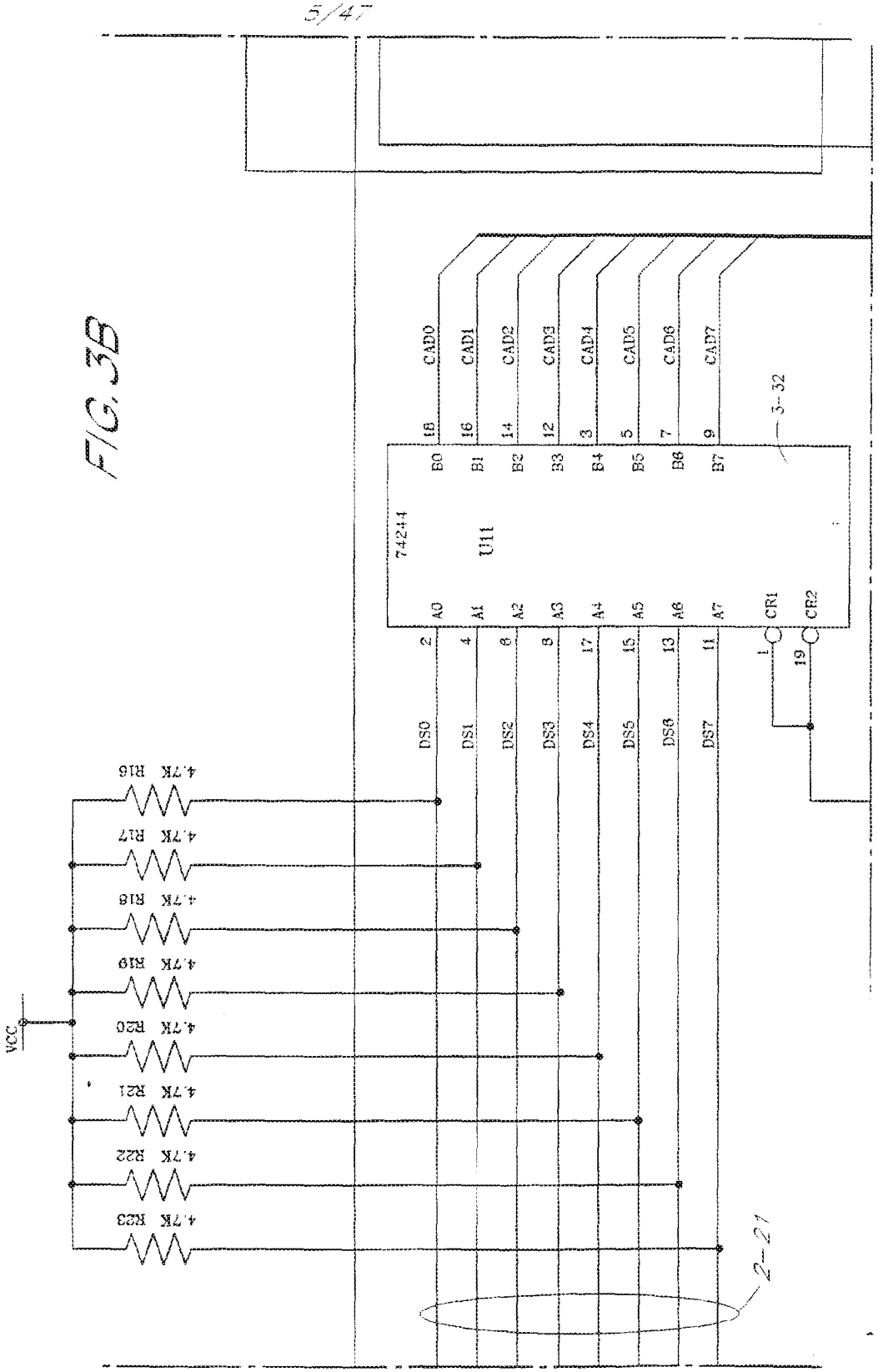


FIG. 3A

FIG. 3B


74244
U11
CAD0
CAD1
CAD2
CAD3
CAD4
CAD5
CAD6
CAD7
B0
B1
B2
B3
B4
B5
B6
B7
A0
A1
A2
A3
A4
A5
A6
A7
CR1
CR2
DS0
DS1
DS2
DS3
DS4
DS5
DS6
DS7
3-32
2-21
VCC
4.7K R16
4.7K R17
4.7K R18
4.7K R19
4.7K R20
4.7K R21
4.7K R22
4.7K R23

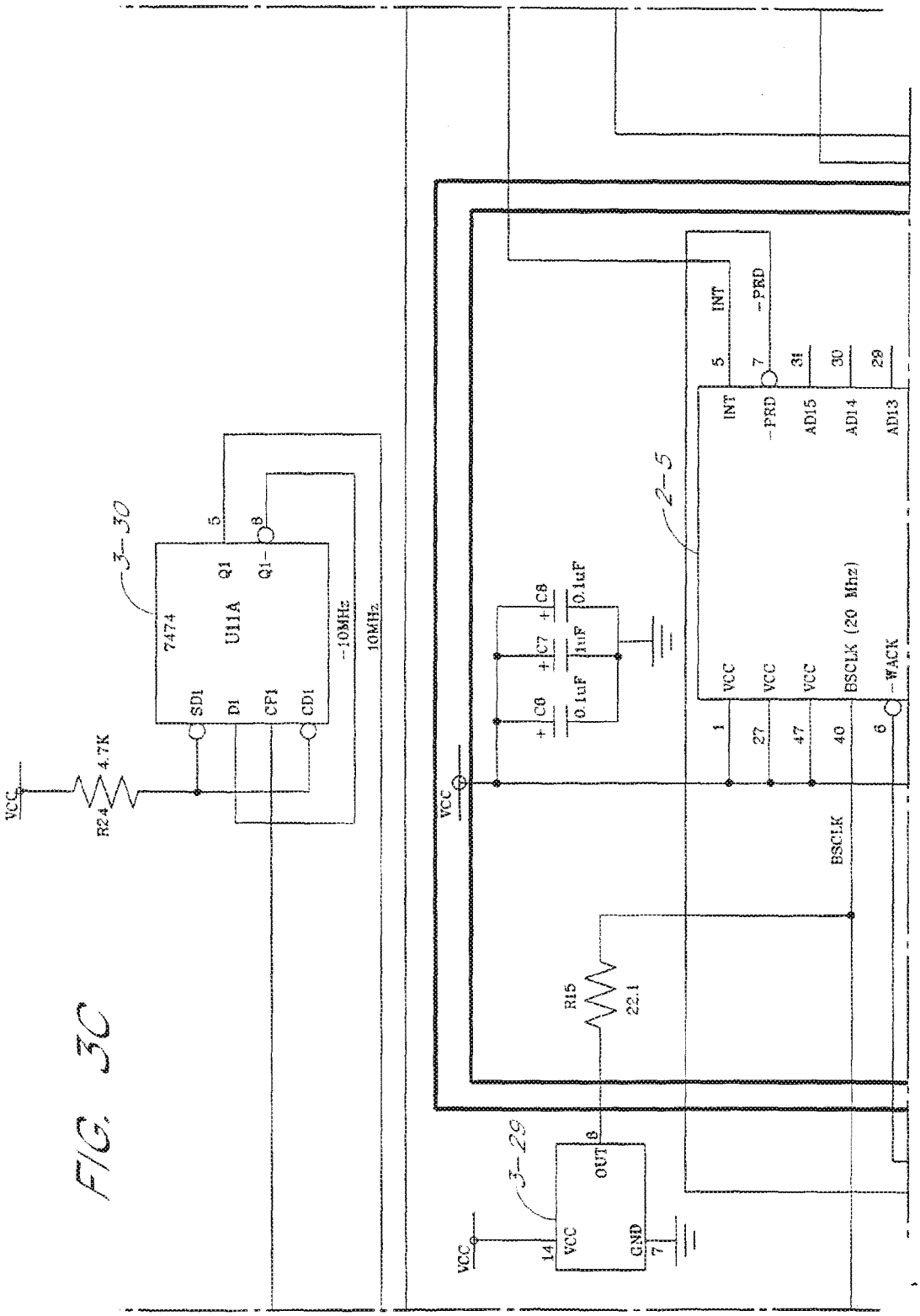

3-30
7474
U11A
Q1
Q1-
SD1
D1
CP1
CD1
10MHz
--10MHz
R24
4.7K
VCC
2-5
INT
-PRD
AD15
AD14
AD13
VCC
BSCLK (20 Mhz)
-WACK
BSCLK
C6
C7
C8
0.1uF
1uF
R15
22.1
3-29
OUT
GND
14
7

FIG. 3C

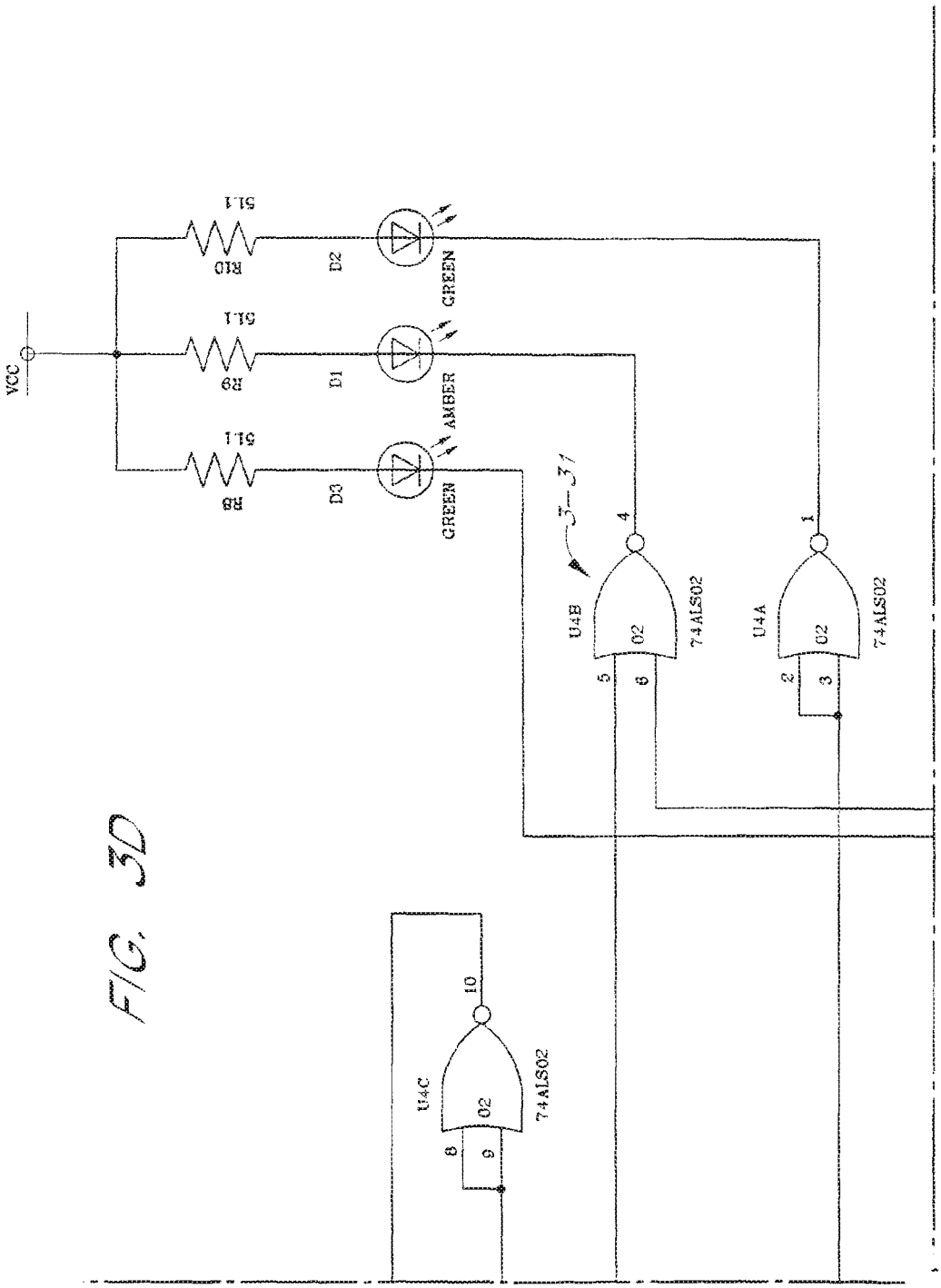

VCC
R10
510
D2
GREEN
R9
510
D1
AMBER
R8
510
D3
GREEN
U4B
74ALS02
U4A
74ALS02
U4C
74ALS02

FIG. 3D

8/47

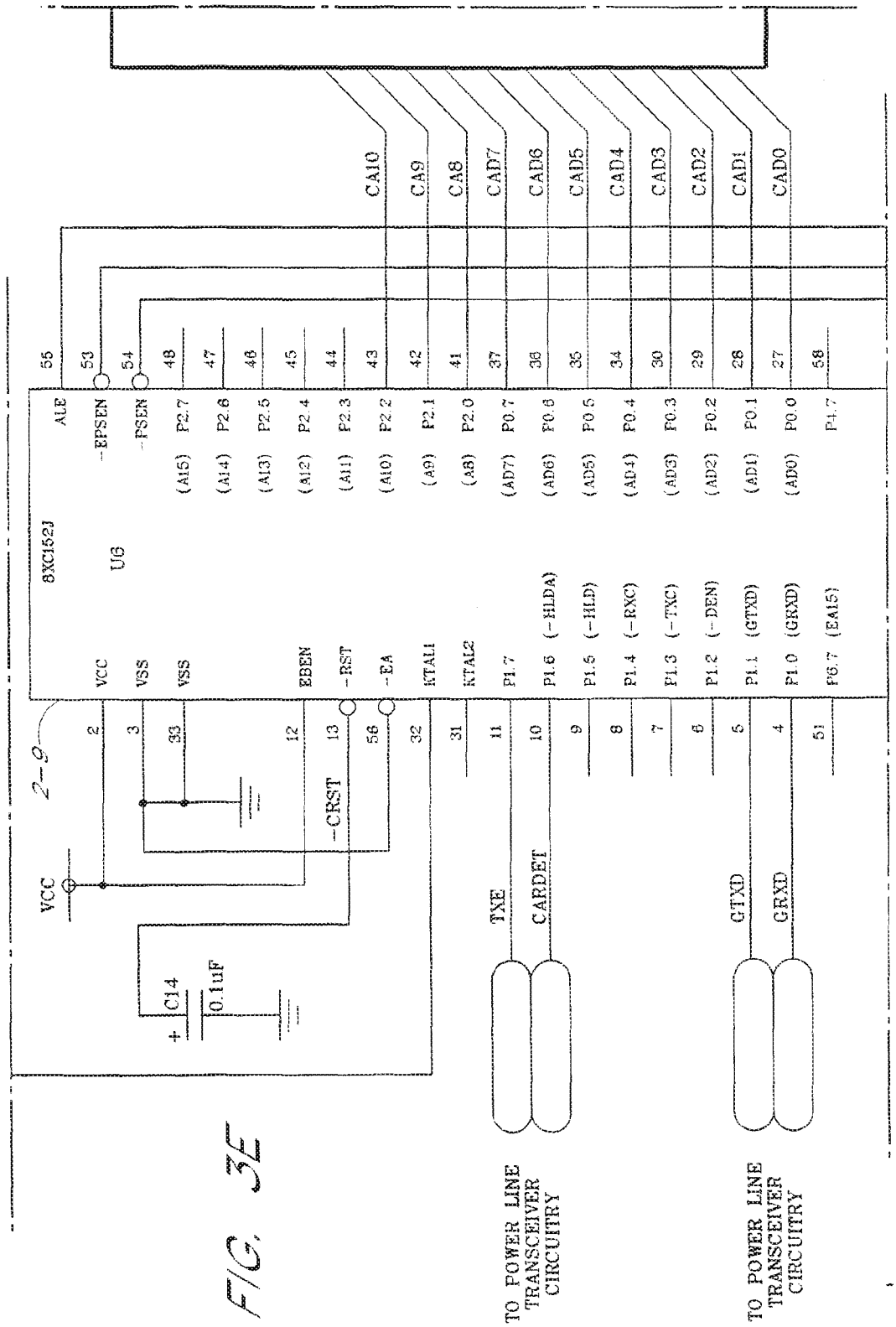

8XC152J
U6
VCC
VSS
VSS
EBEN
-RST
-EA
XTAL1
XTAL2
P1.7
P1.6 (-HLDA)
P1.5 (-HLD)
P1.4 (-RXC)
P1.3 (-TXC)
P1.2 (-DEN)
P1.1 (GTXD)
P1.0 (GRXD)
P6.7 (EA15)
ALE
-EPSEN
-PSEN
P2.7 (A15)
P2.6 (A14)
P2.5 (A13)
P2.4 (A12)
P2.3 (A11)
P2.2 (A10)
P2.1 (A9)
P2.0 (A8)
P0.7 (AD7)
P0.6 (AD6)
P0.5 (AD5)
P0.4 (AD4)
P0.3 (AD3)
P0.2 (AD2)
P0.1 (AD1)
P0.0 (AD0)
P4.7
CA10
CA9
CA8
CAD7
CAD6
CAD5
CAD4
CAD3
CAD2
CAD1
CAD0
2-9
VCC
C14
0.1uF
-CRST
TXE
CARDET
GTXD
GRXD
TO POWER LINE TRANSCEIVER CIRCUITRY
TO POWER LINE TRANSCEIVER CIRCUITRY

FIG. 3E

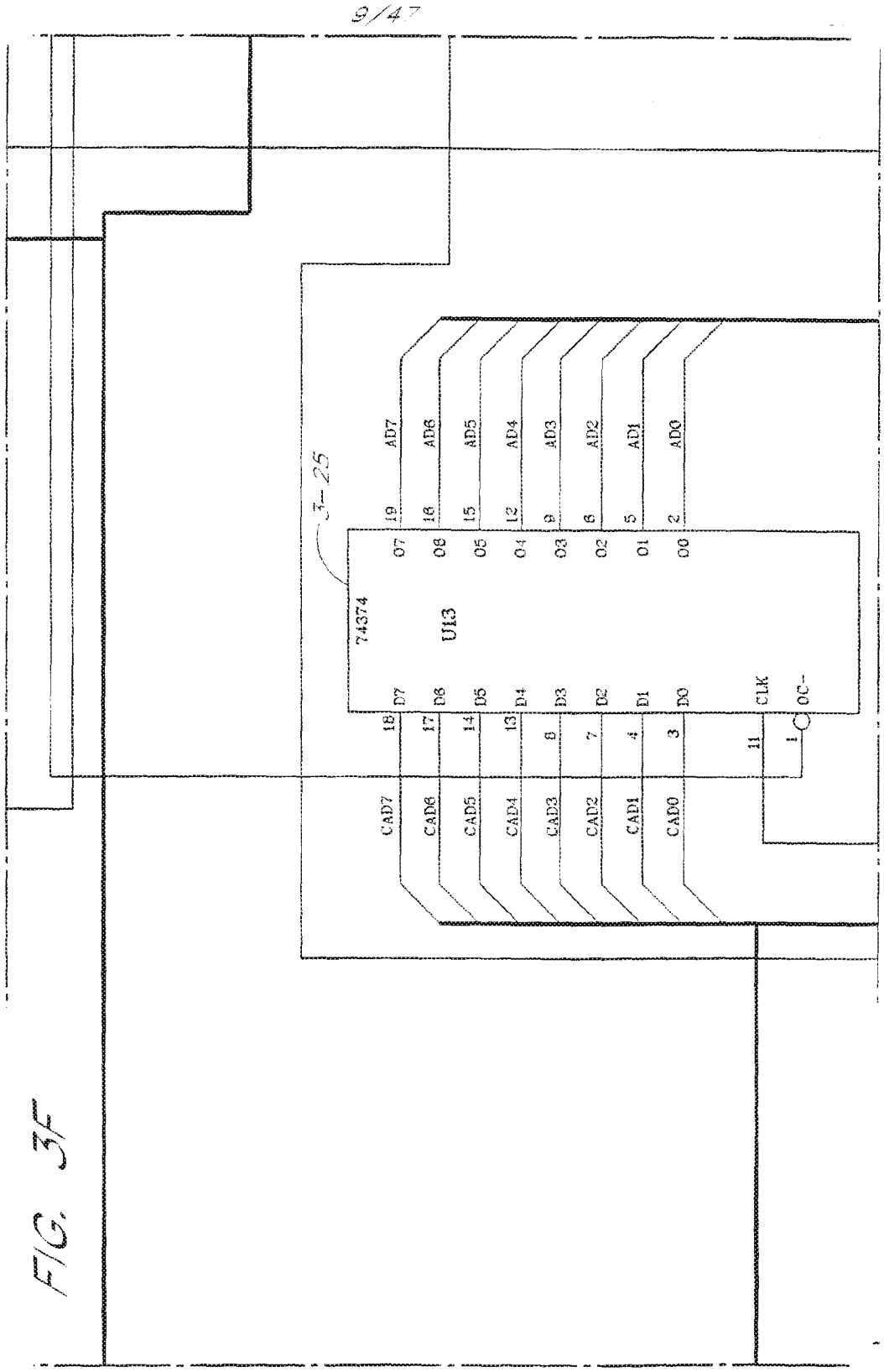

3-25
74374
U13
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
19
18
15
12
9
8
5
2
O7
O6
O5
O4
O3
O2
O1
O0
D7
D6
D5
D4
D3
D2
D1
D0
CLK
OC-
18
17
14
13
8
7
4
3
11
1
CAD7
CAD6
CAD5
CAD4
CAD3
CAD2
CAD1
CAD0

FIG. 3F

10/47

FIG. 3G

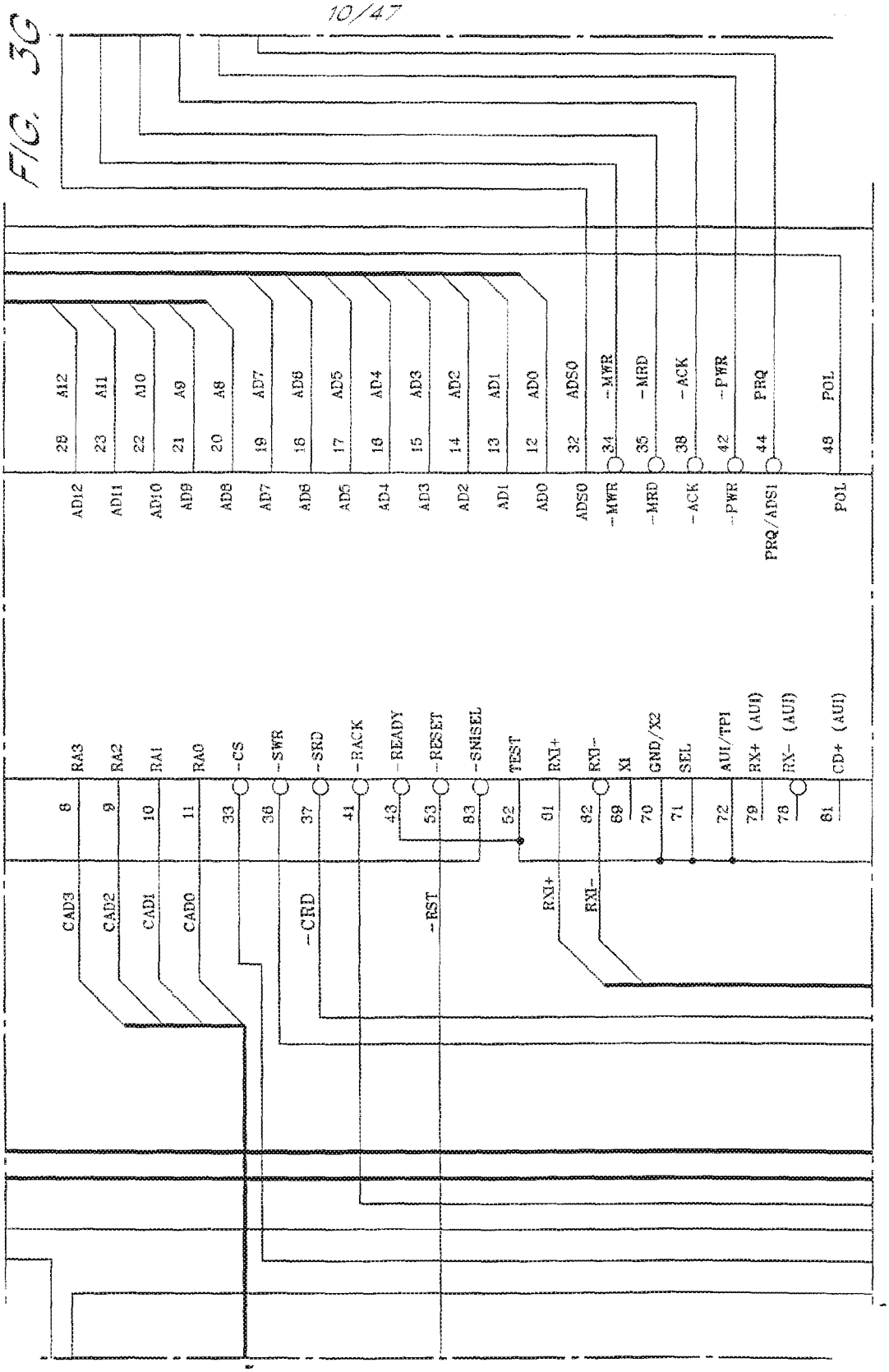
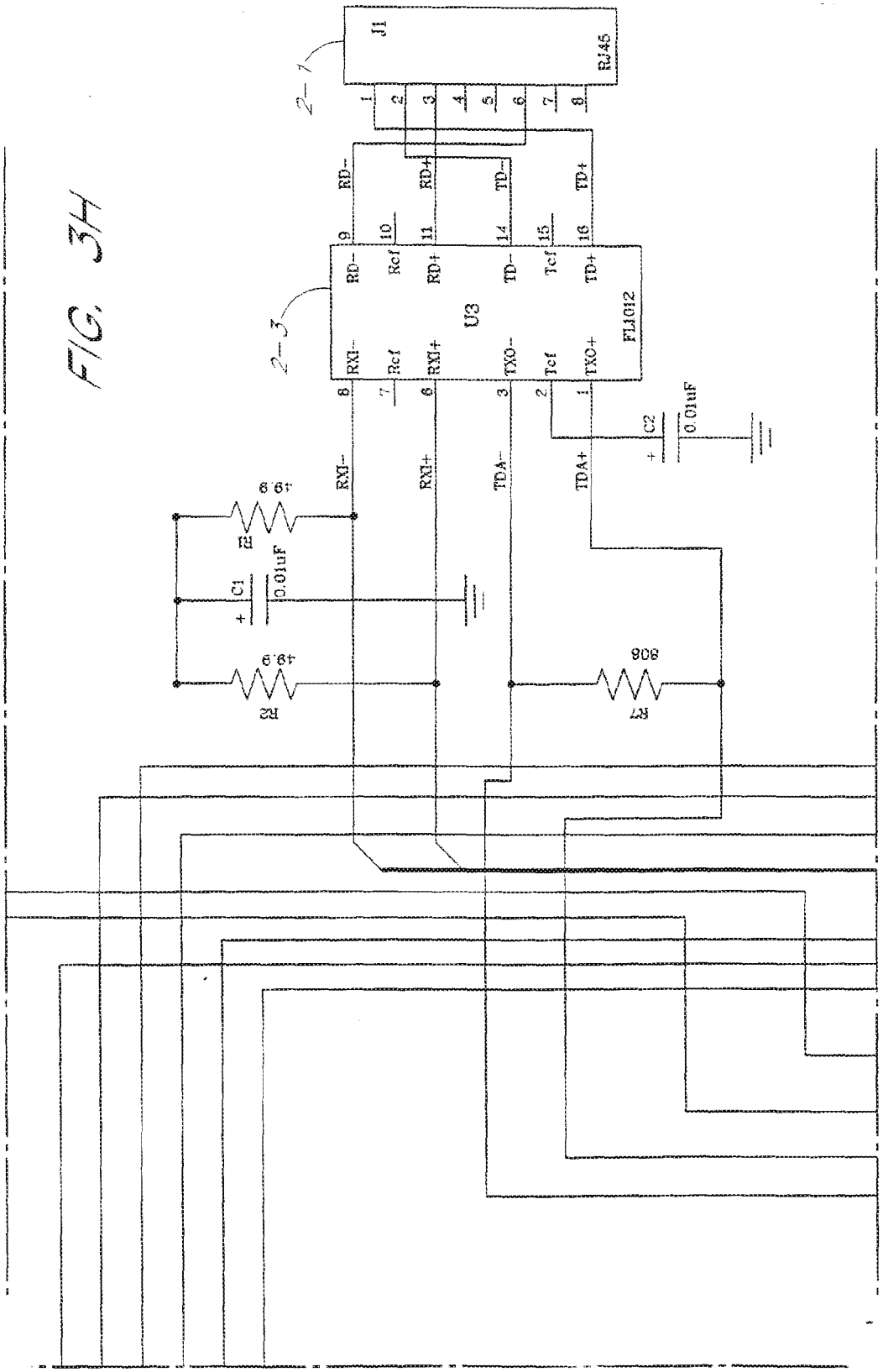

28 A12
23 A11
22 A10
21 A9
20 A8
19 AD7
16 AD6
17 AD5
18 AD4
15 AD3
14 AD2
13 AD1
12 AD0
32 ADS0
34 -MWR
35 -MRD
38 -ACK
42 -PWR
44 PRQ
48 POL
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
ADS0
-MWR
-MRD
-ACK
-PWR
PRQ/ADS1
POL
8 RA3
9 RA2
10 RA1
11 RA0
33 -CS
36 -SWR
37 -SRD
41 -RACK
43 -READY
53 -RESET
83 -SNISEL
52 TEST
81 RXI+
82 RXI-
69 XI
70 GND/X2
71 SEL
72 AUI/TPI
79 RX+ (AUI)
78 RX- (AUI)
61 CD+ (AUI)
CAD3
CAD2
CAD1
CAD0
-CRD
-RST
RXI+
RXI-

FIG. 3H


J1
RJ45
2-1
2-3
U3
FL1012
RD-
RD+
TD-
TD+
Ref
RXI-
RXI+
TXO-
TXO+
TDA-
TDA+
C1
C2
0.01uF
R1
R2
R7
49.9
806

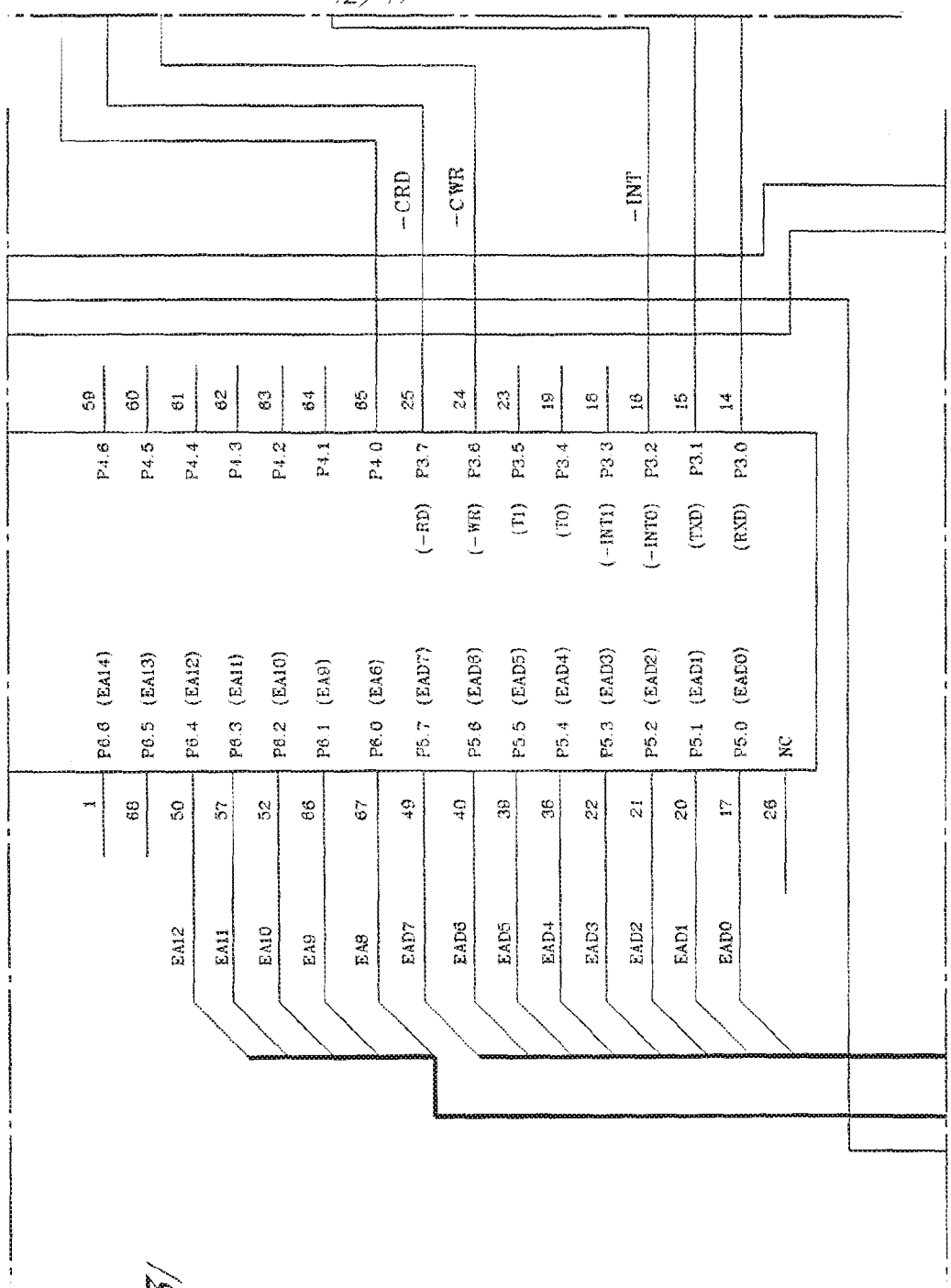

-CRD
-CWR
-INT
59 P4.6
60 P4.5
61 P4.4
62 P4.3
63 P4.2
64 P4.1
65 P4.0
25 P3.7 (-RD)
24 P3.6 (-WR)
23 P3.5 (T1)
19 P3.4 (T0)
18 P3.3 (-INT1)
16 P3.2 (-INT0)
15 P3.1 (TXD)
14 P3.0 (RXD)
1 P6.6 (EA14)
68 P6.5 (EA13)
50 P6.4 (EA12)
57 P6.3 (EA11)
52 P6.2 (EA10)
66 P6.1 (EA9)
67 P6.0 (EA8)
49 P5.7 (EAD7)
40 P5.6 (EAD6)
38 P5.5 (EAD5)
36 P5.4 (EAD4)
22 P5.3 (EAD3)
21 P5.2 (EAD2)
20 P5.1 (EAD1)
17 P5.0 (EAD0)
26 NC
EA12
EA11
EA10
EA9
EA8
EAD7
EAD6
EAD5
EAD4
EAD3
EAD2
EAD1
EAD0

FIG. 3

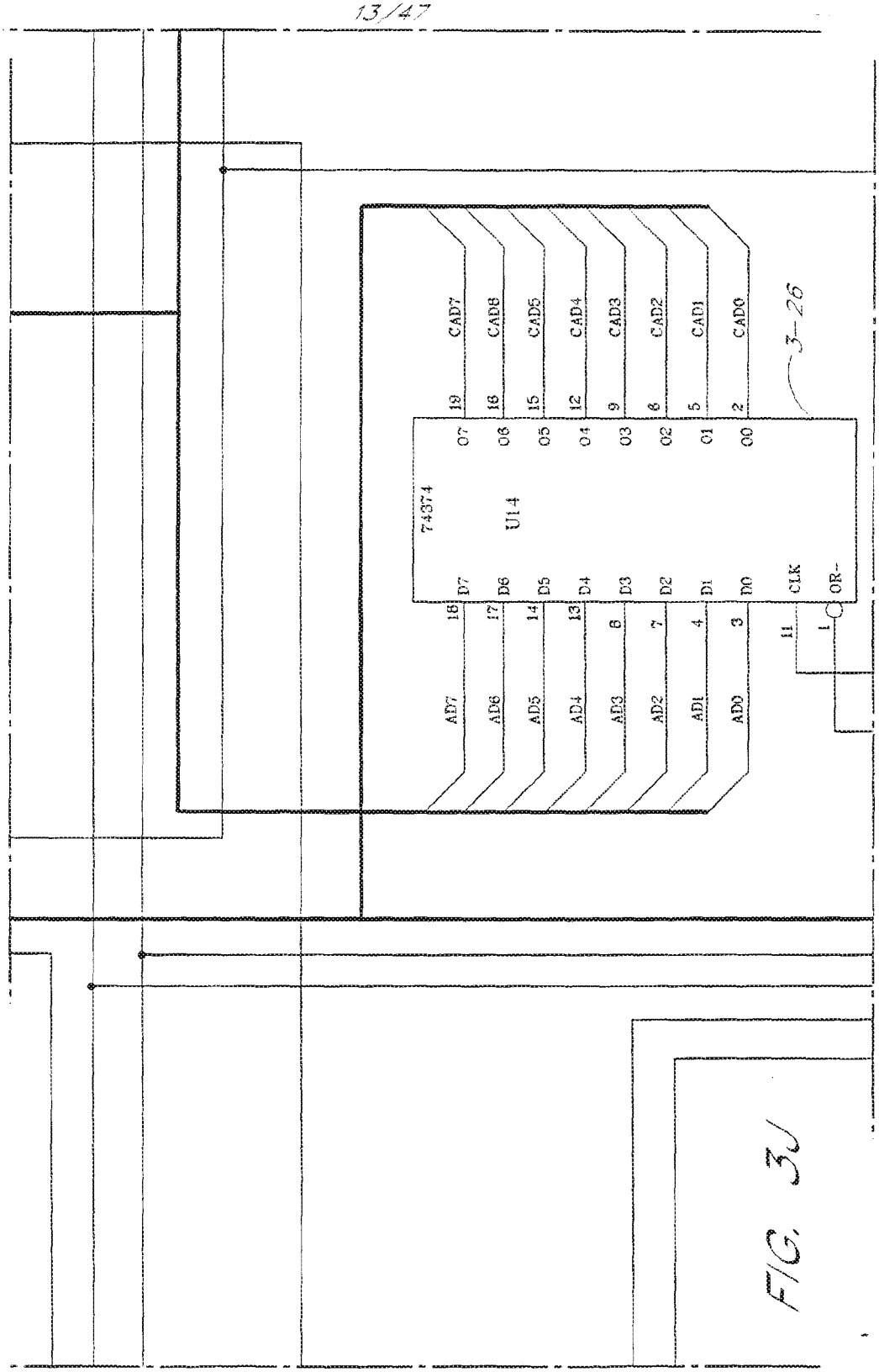

CAD7
CAD6
CAD5
CAD4
CAD3
CAD2
CAD1
CAD0
19
18
15
12
9
8
5
2
O7
O6
O5
O4
O3
O2
O1
O0
74374
U14
D7
D6
D5
D4
D3
D2
D1
D0
CLK
OR-
18
17
14
13
8
7
4
3
11
1
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
3-26

FIG. 3J

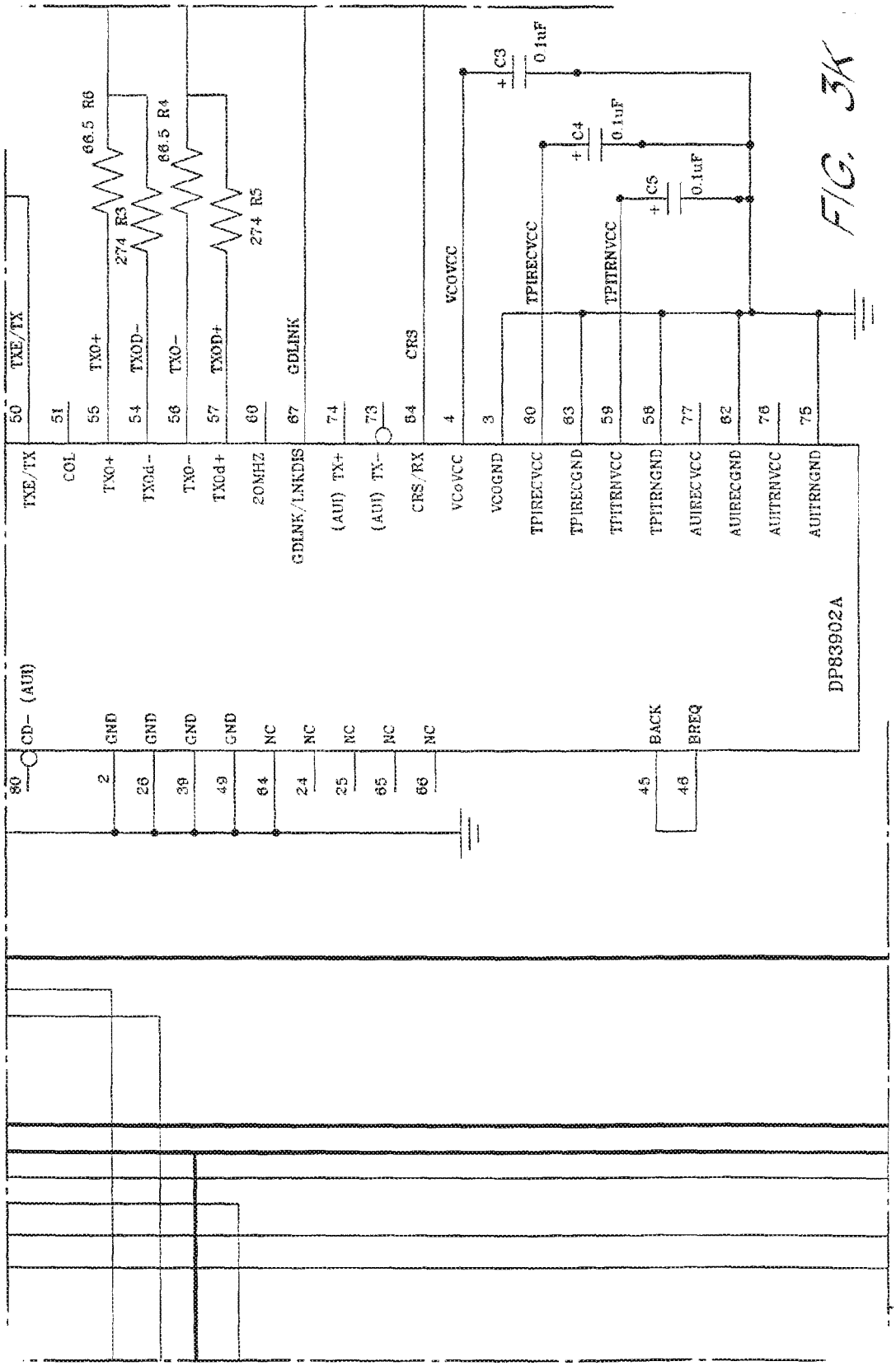
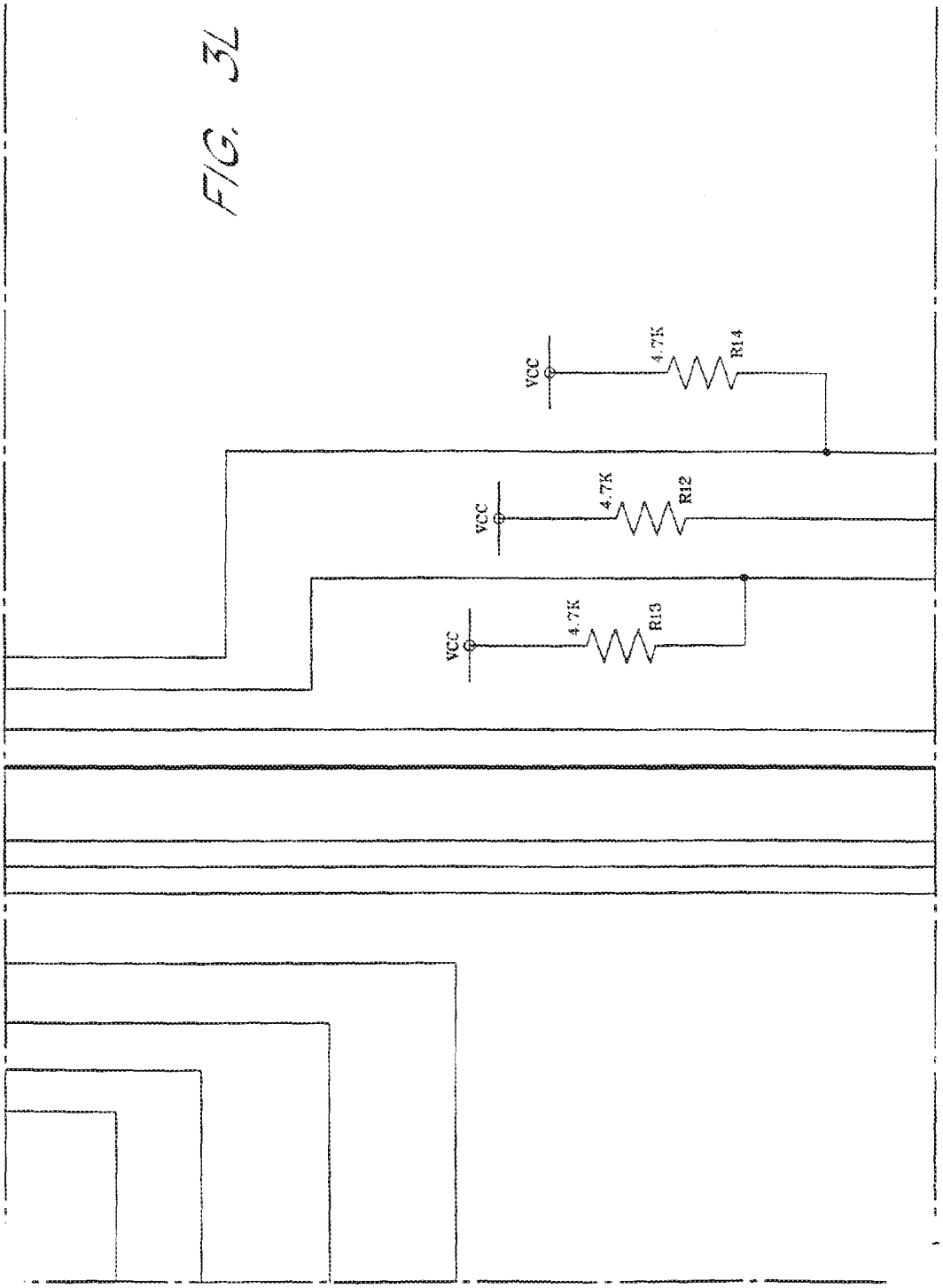

DP83902A
TXE/TX
COL
TXO+
TXOd-
TXO-
TXOd+
20MHZ
GDLNK/LNKDIS
(AUI) TX+
(AUI) TX-
CRS/RX
VCOVCC
VCOGND
TPIRECVCC
TPIRECGND
TPITRNVCC
TPITRNGND
AUIRECVCC
AUIRECGND
AUITRNVCC
AUITRNGND
CD- (AUI)
GND
NC
BACK
BREQ
66.5 R6
66.5 R4
274 R3
274 R5
C3
C4
C5
0.1uF

FIG. 3K

FIG. 3L



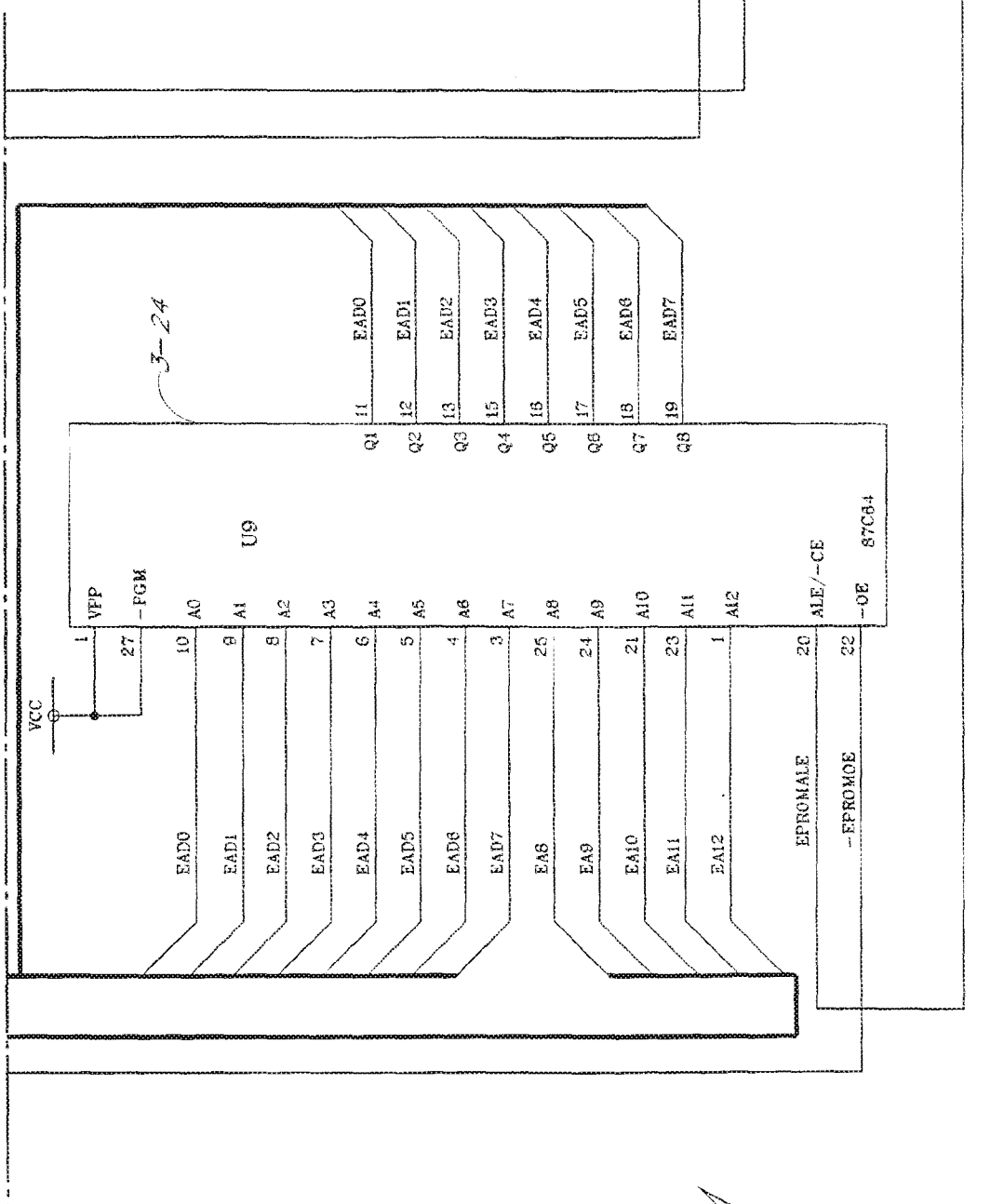

3-24
U9
VPP
-PGM
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
ALE/-CE
-OE
87C64
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
EAD0
EAD1
EAD2
EAD3
EAD4
EAD5
EAD6
EAD7
EA8
EA9
EA10
EA11
EA12
EPROMALE
-EPROMOE
VCC

FIG. 3M

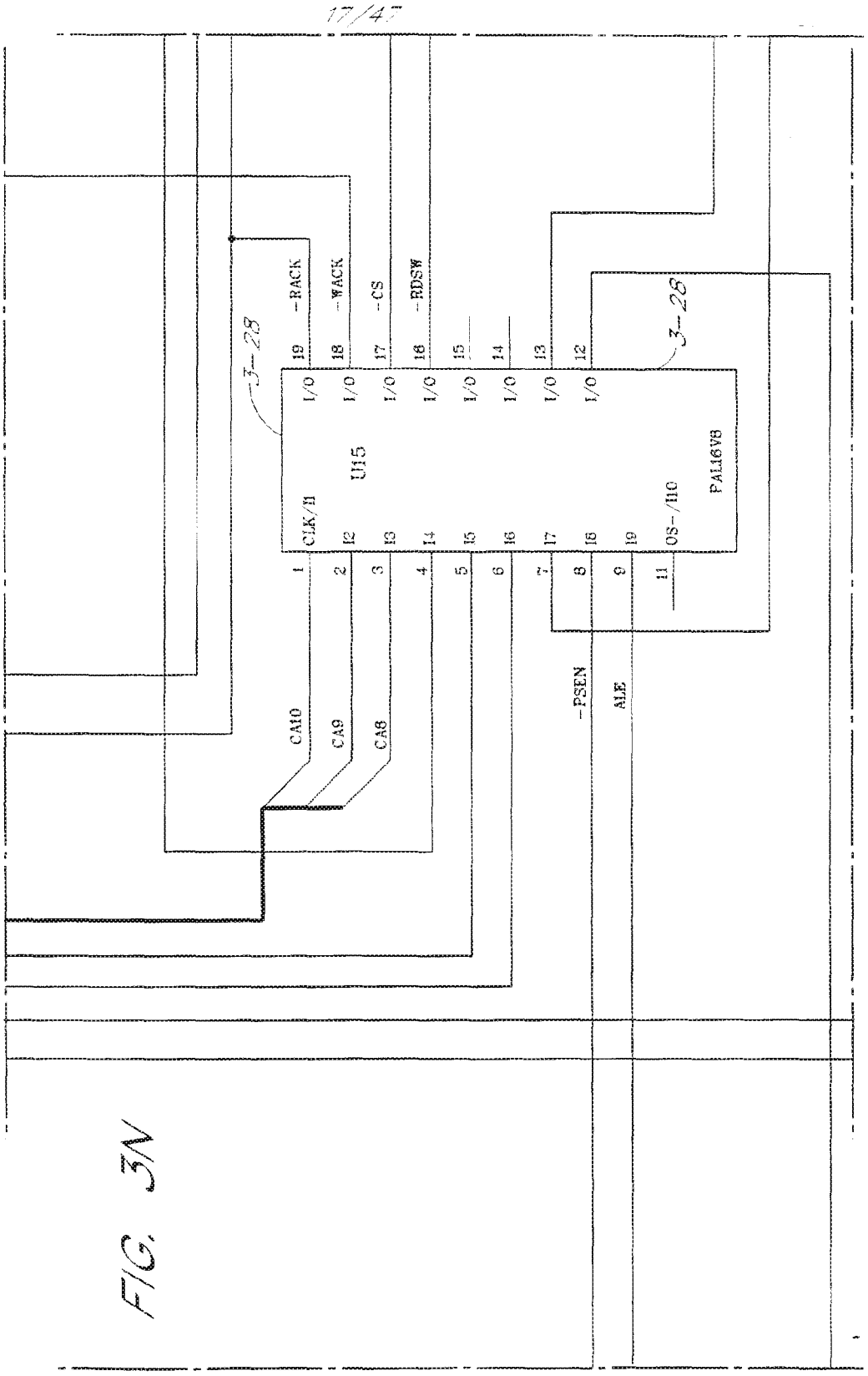

-RACK
-WACK
-CS
-RDSW
3-28
3-28
I/O
U15
PAL16V8
CLK/I1
OS-/IIO
CA10
CA9
CA8
-PSEN
ALE

FIG. 3N

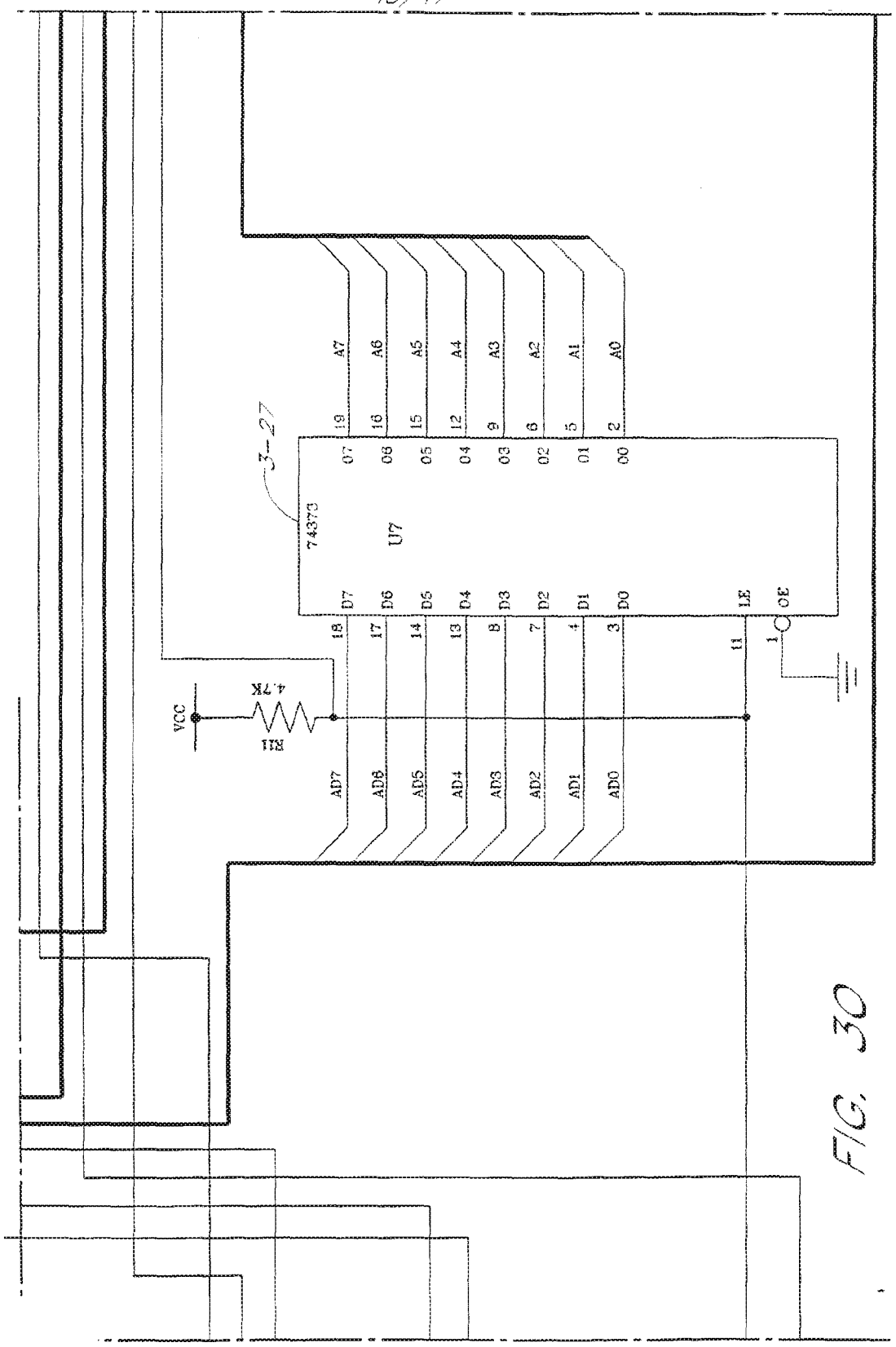
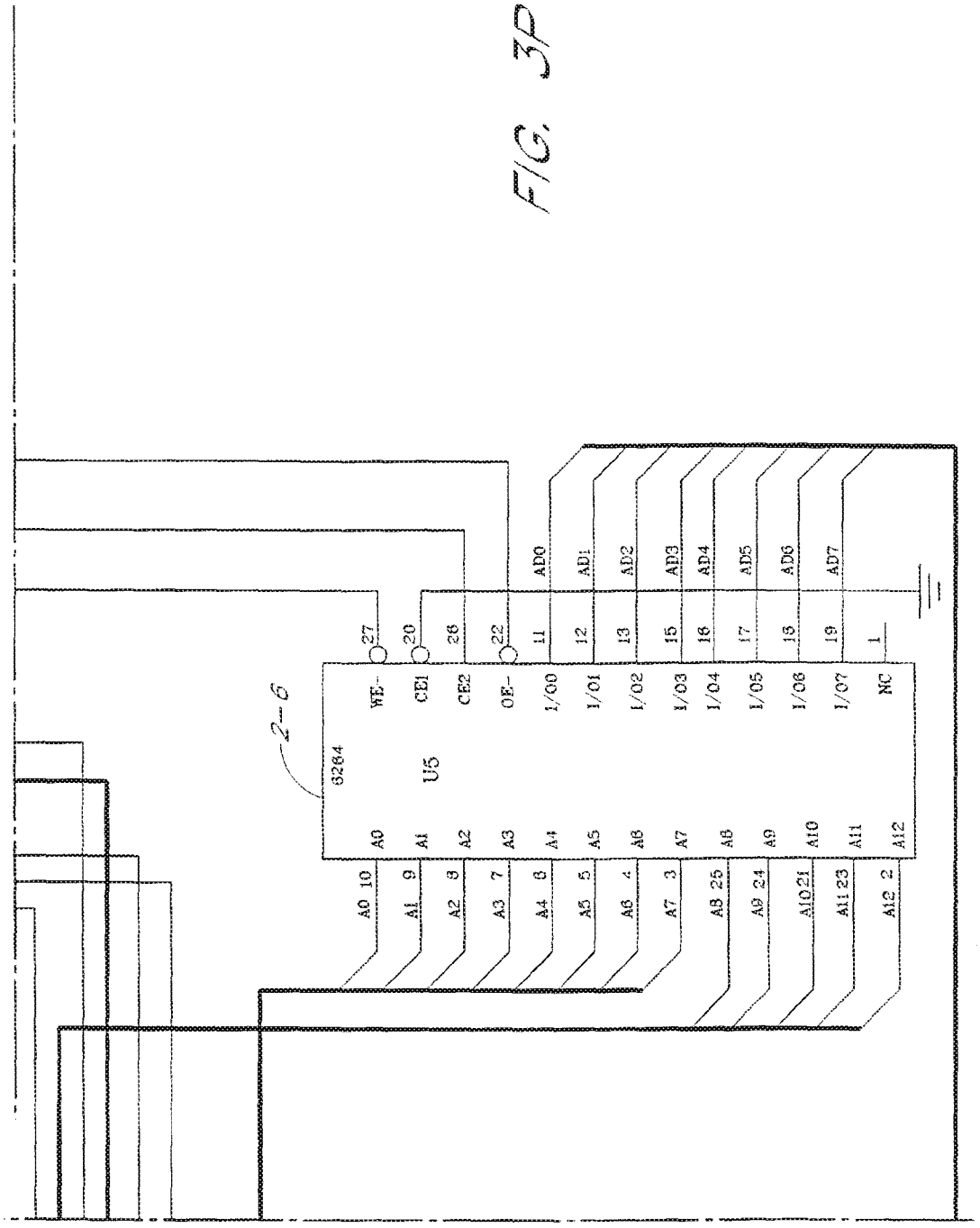

A7
A6
A5
A4
A3
A2
A1
A0
19
16
15
12
9
6
5
2
3-27
74373
U7
O7
O6
O5
O4
O3
O2
O1
O0
D7
D6
D5
D4
D3
D2
D1
D0
LE
OE
18
17
14
13
8
7
4
3
11
1
VCC
4.7K
R11
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0

FIG. 30

FIG. 3P


U5
6264
WE-
CE1
CE2
OE-
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
NC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
27
20
26
22
11
12
13
15
16
17
18
19
1
10
9
8
7
6
5
4
3
25
24
21
23
2

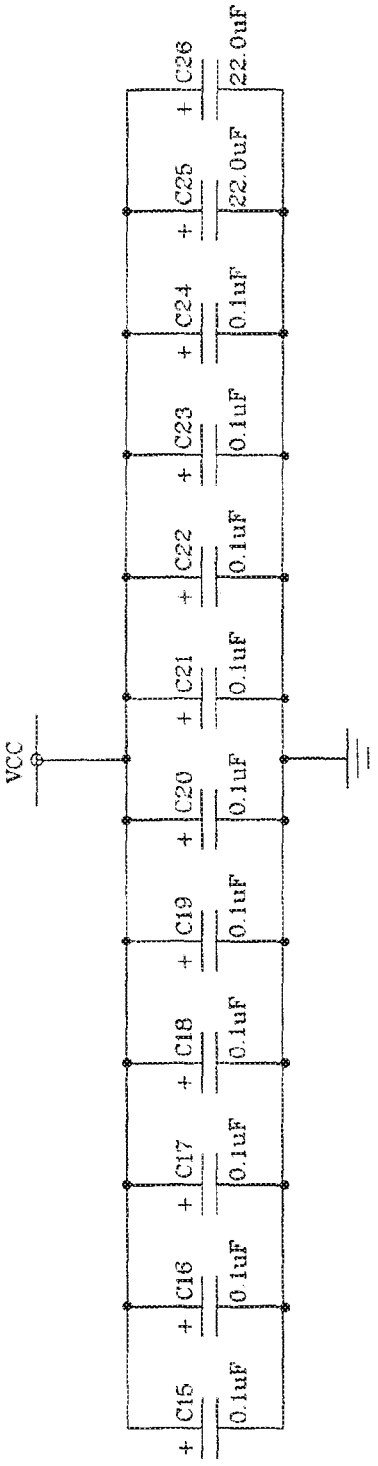

VCC
C15 0.1uF
C16 0.1uF
C17 0.1uF
C18 0.1uF
C19 0.1uF
C20 0.1uF
C21 0.1uF
C22 0.1uF
C23 0.1uF
C24 0.1uF
C25 22.0uF
C26 22.0uF

FIG. 3Q

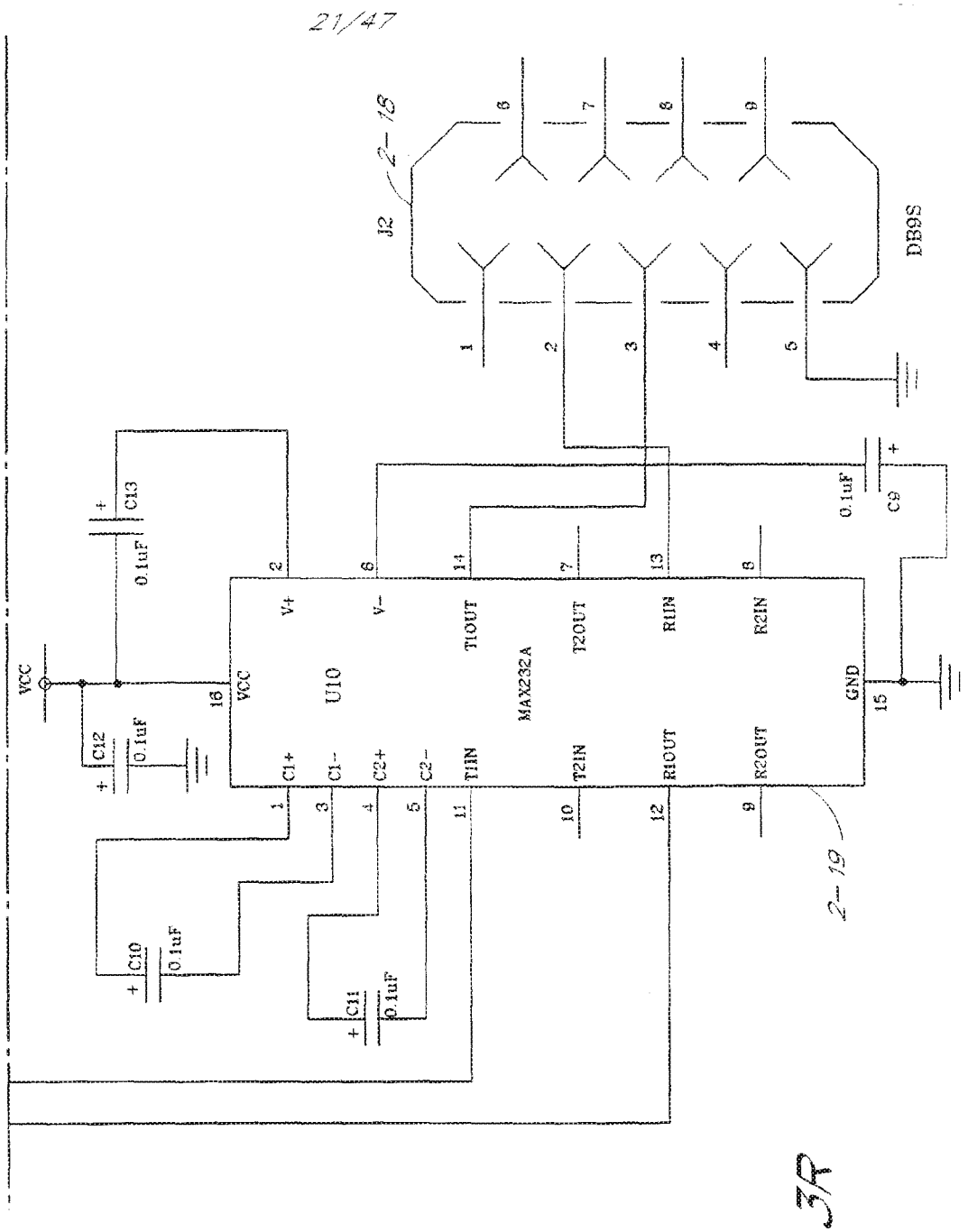

J2
2-18
DB9S
1
2
3
4
5
6
7
8
9
C13
0.1uF
C9
0.1uF
C12
0.1uF
C10
0.1uF
C11
0.1uF
VCC
U10
MAX232A
V+
V-
T1OUT
T2OUT
R1IN
R2IN
GND
C1+
C1-
C2+
C2-
T1IN
T2IN
R1OUT
R2OUT
2-19

FIG. 3B

FIG. 4A	FIG. 4B	FIG. 4C
FIG. 4D	FIG. 4E	FIG. 4F

FIG. 4

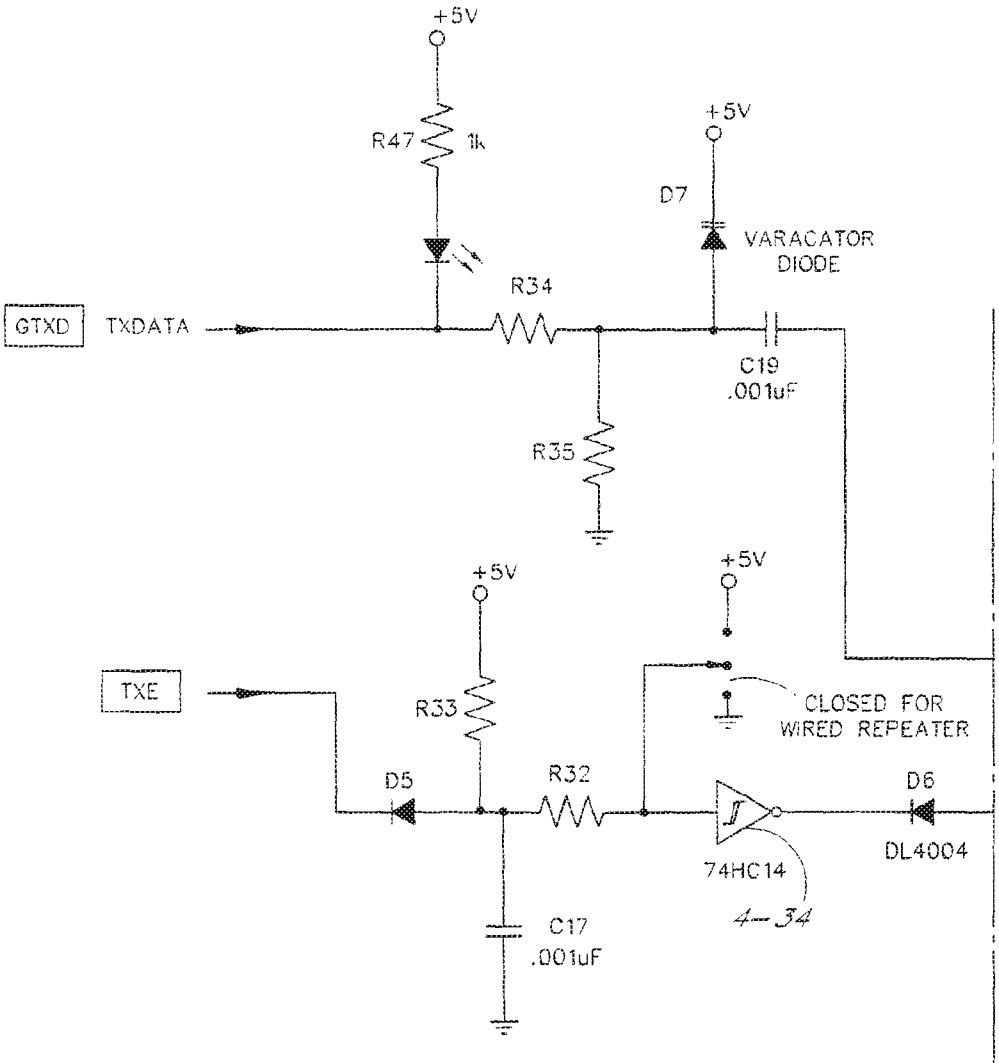


FIG. 4A

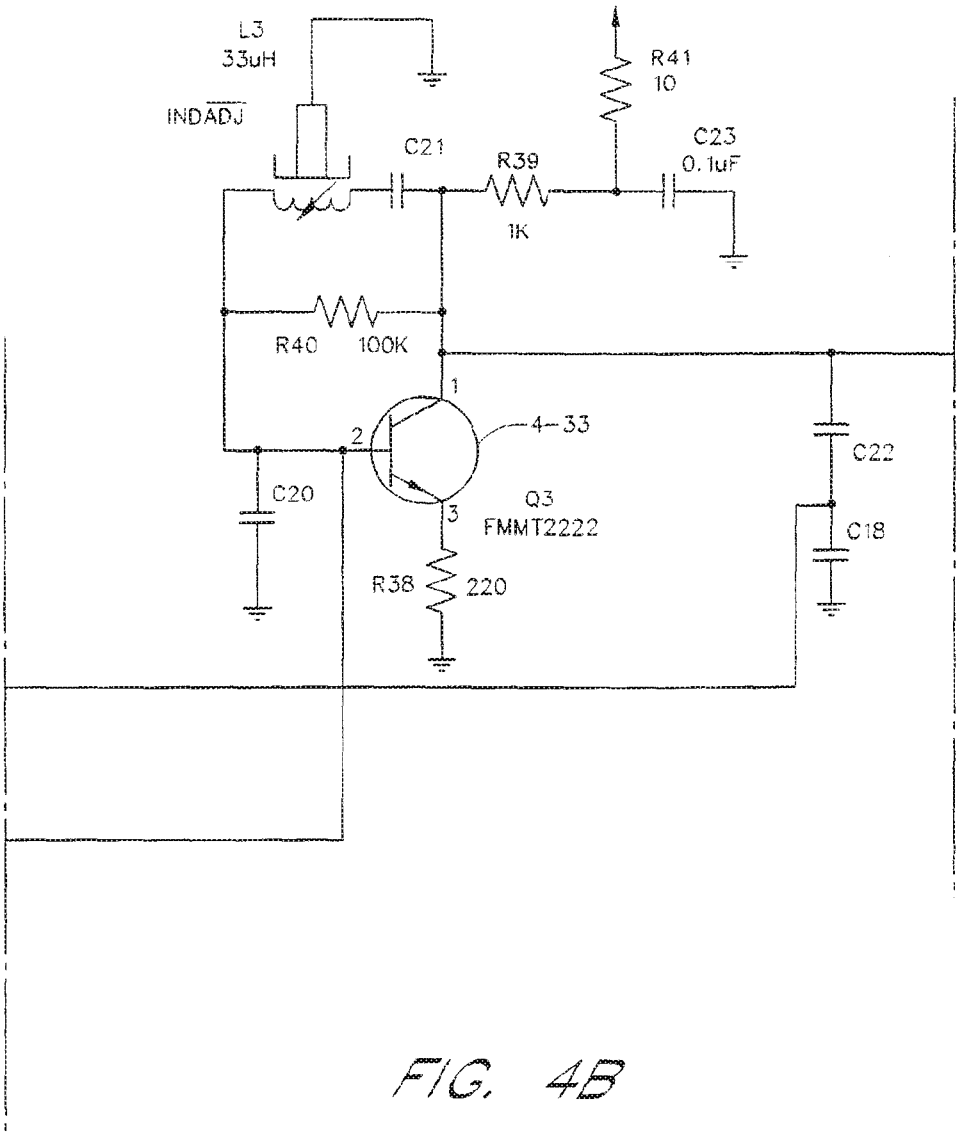

L3
33uH
INDADJ
C21
R39
1K
R41
10
C23
0.1uF
R40
100K
1
2
3
4-33
Q3
FMMT2222
C20
R38
220
C22
C18

FIG. 4B

FIG. 4C

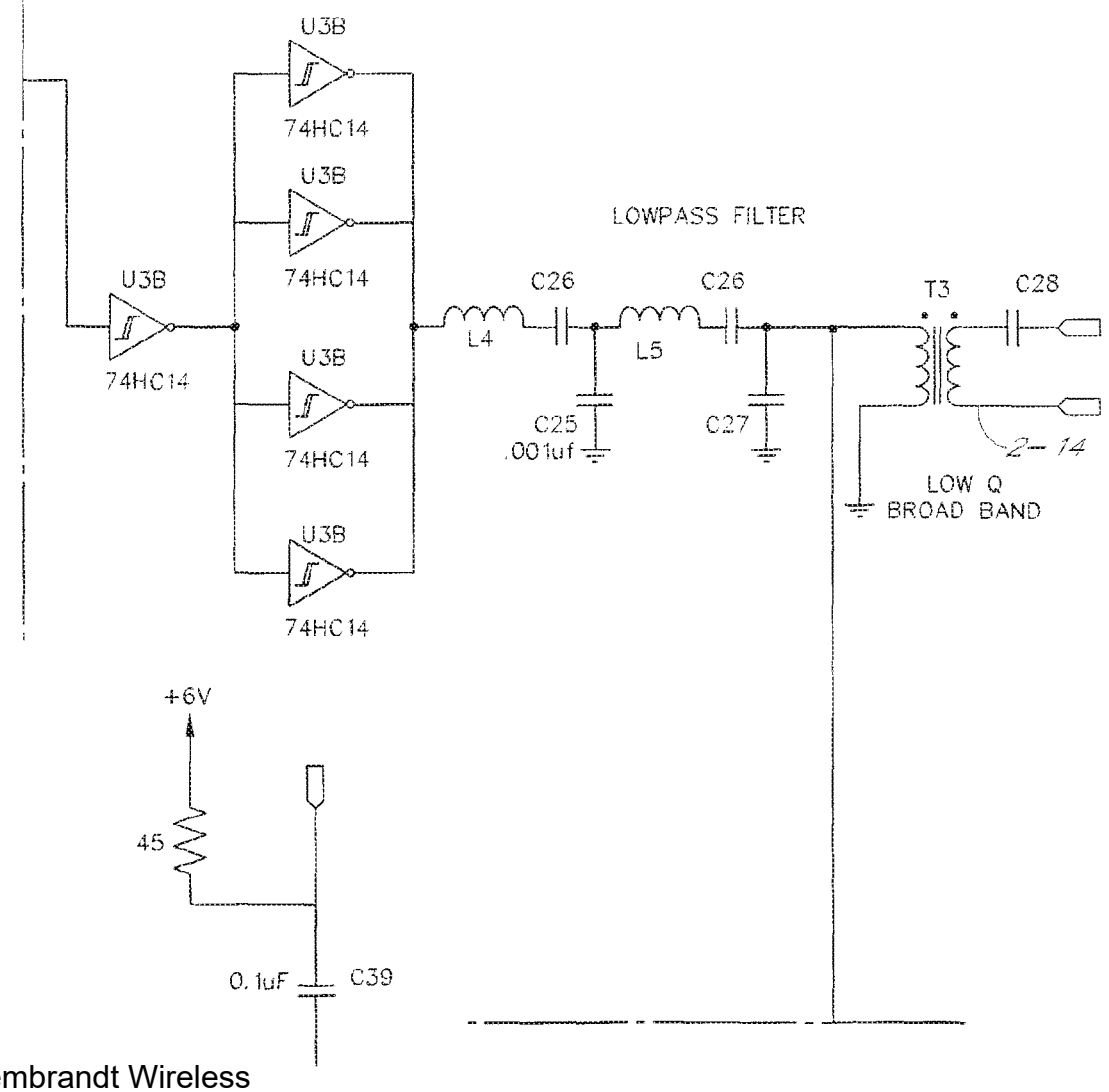
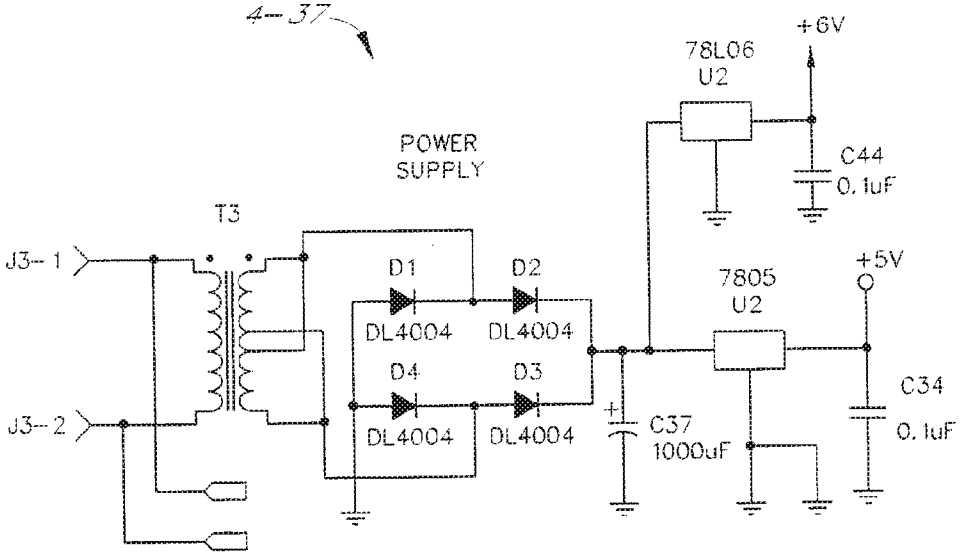


FIG. 4D


4-37
POWER SUPPLY
T3
J3-1
J3-2
D1
DL4004
D2
DL4004
D4
DL4004
D3
DL4004
78L06
U2
+6V
C44
0.1uF
7805
U2
+5V
C37
1000uF
C34
0.1uF

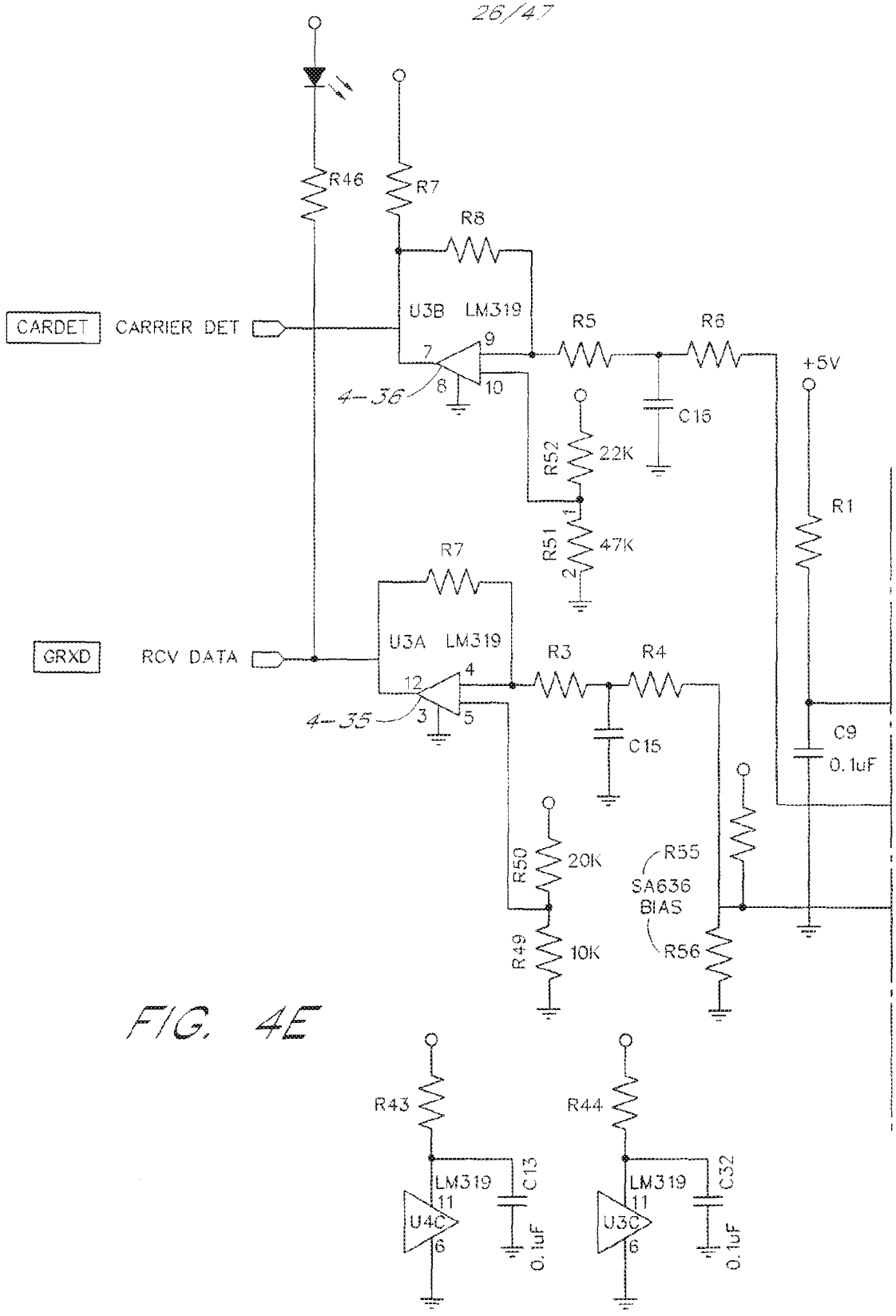

R46
R7
R8
CARDET
CARRIER DET
U3B LM319
7
9
8
10
4-36
R5
R6
+5V
C16
R52
22K
R51
47K
2
1
R1
R7
GRXD
RCV DATA
U3A LM319
12
4
3
5
4-35
R3
R4
C15
C9
0.1uF
R50
20K
R55
SA636
BIAS
R56
R49
10K
R43
R44
LM319
11
U4C
6
C13
0.1uF
LM319
11
U3C
6
C32
0.1uF

FIG. 4E

27/47

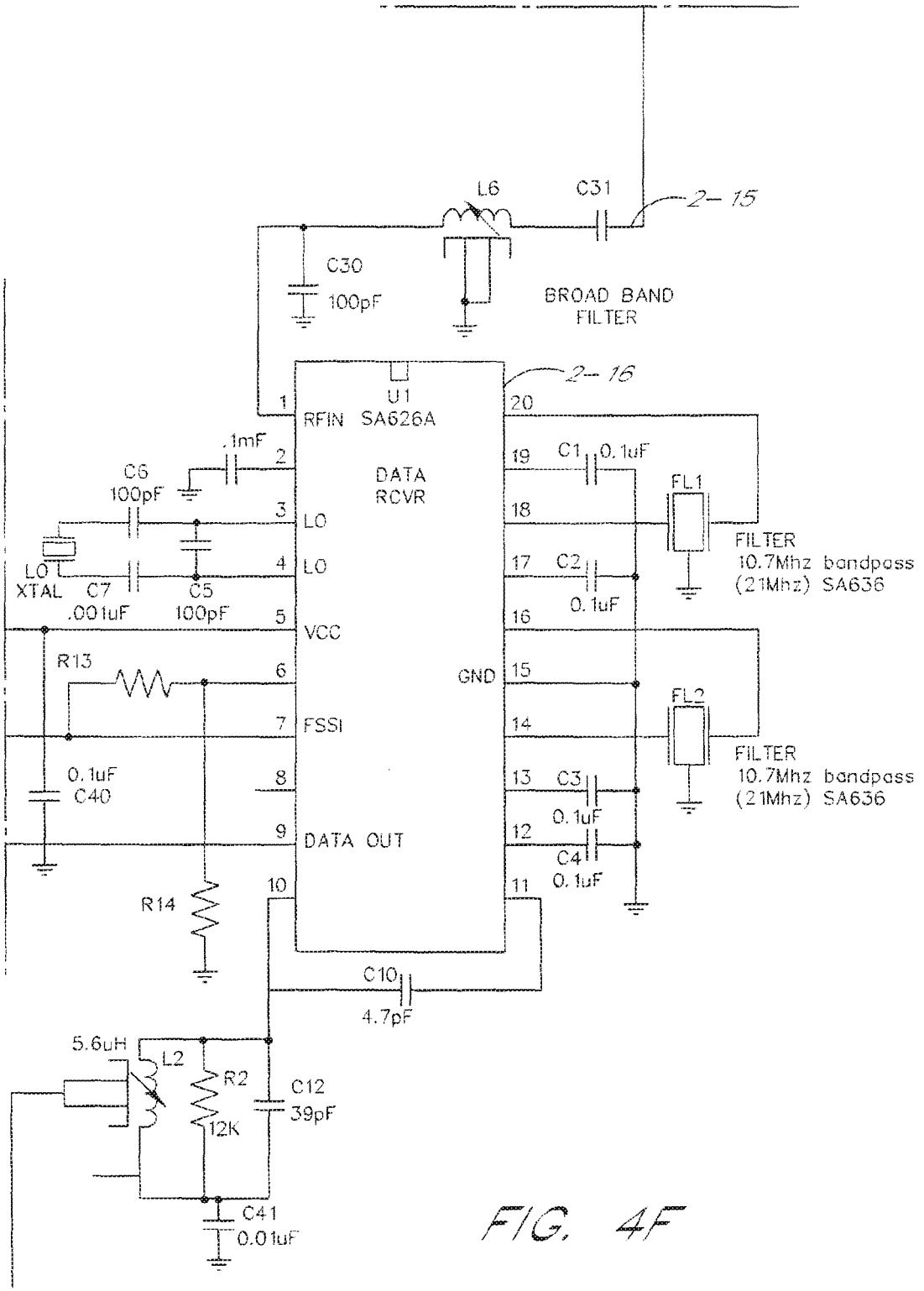

L6
C31
2-15
C30
100pF
BROAD BAND
FILTER
2-16
U1
RFIN SA626A
DATA
RCVR
.1mF
C6
100pF
LO
XTAL
C7
.001uF
C5
100pF
VCC
R13
FSSI
0.1uF
C40
DATA OUT
R14
C10
4.7pF
5.6uH
L2
R2
12K
C12
39pF
C41
0.01uF
C1
0.1uF
FL1
FILTER
10.7Mhz bandpass
(21Mhz) SA636
C2
0.1uF
GND
FL2
FILTER
10.7Mhz bandpass
(21Mhz) SA636
C3
0.1uF
C4
0.1uF

FIG. 4F

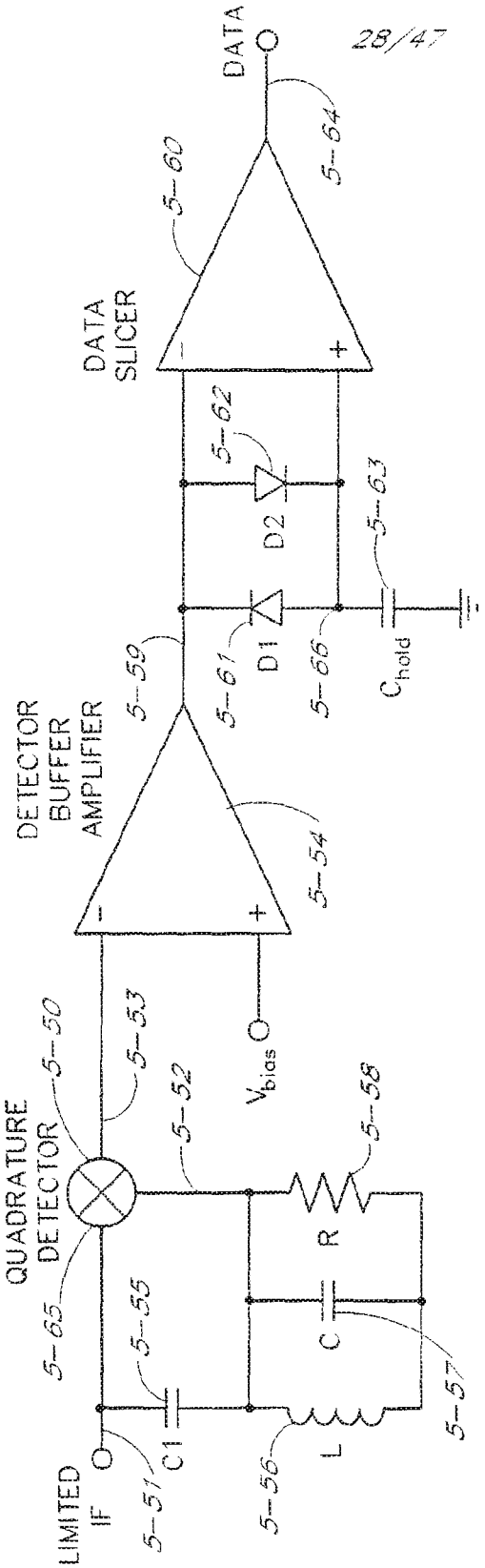


FIG. 5

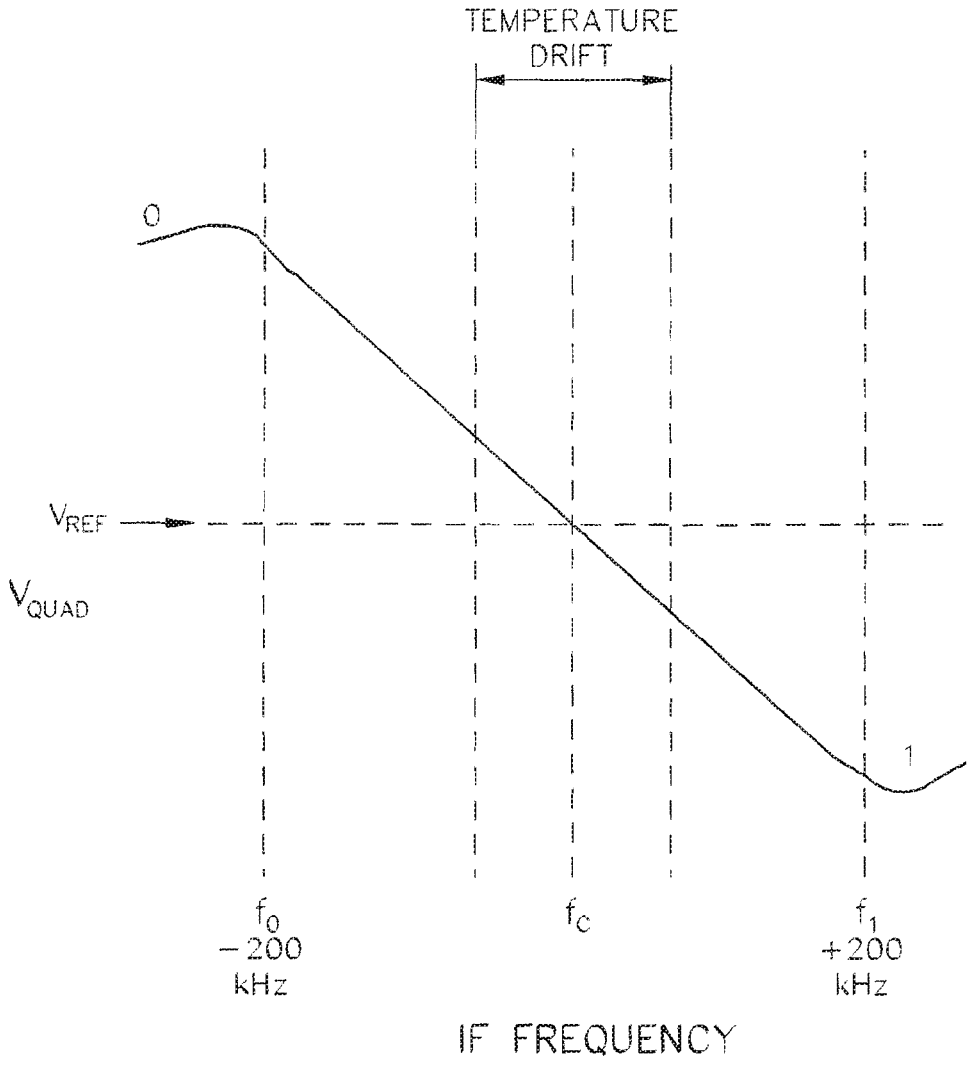
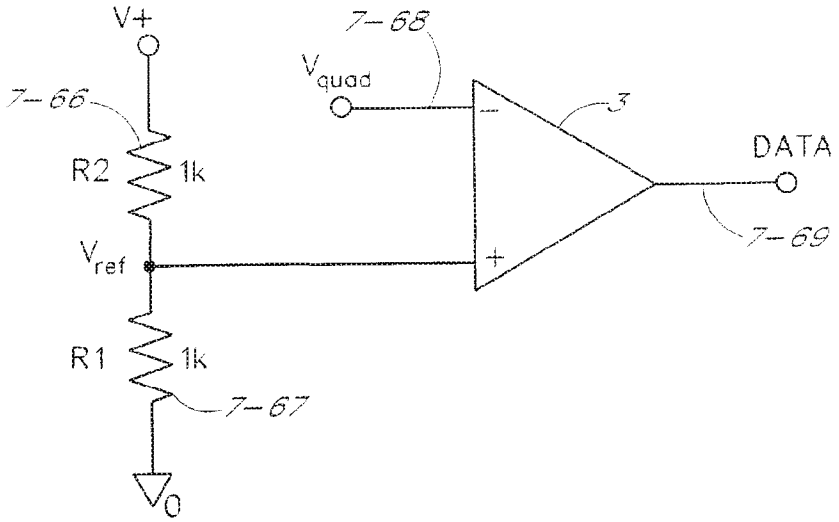

TEMPERATURE
DRIFT
0
1
V_{REF}
V_{QUAD}
f_0
−200
kHz
f_c
f_1
+200
kHz
IF FREQUENCY

FIG. 6



DC-coupled FSK data comparator

FIG. 7A

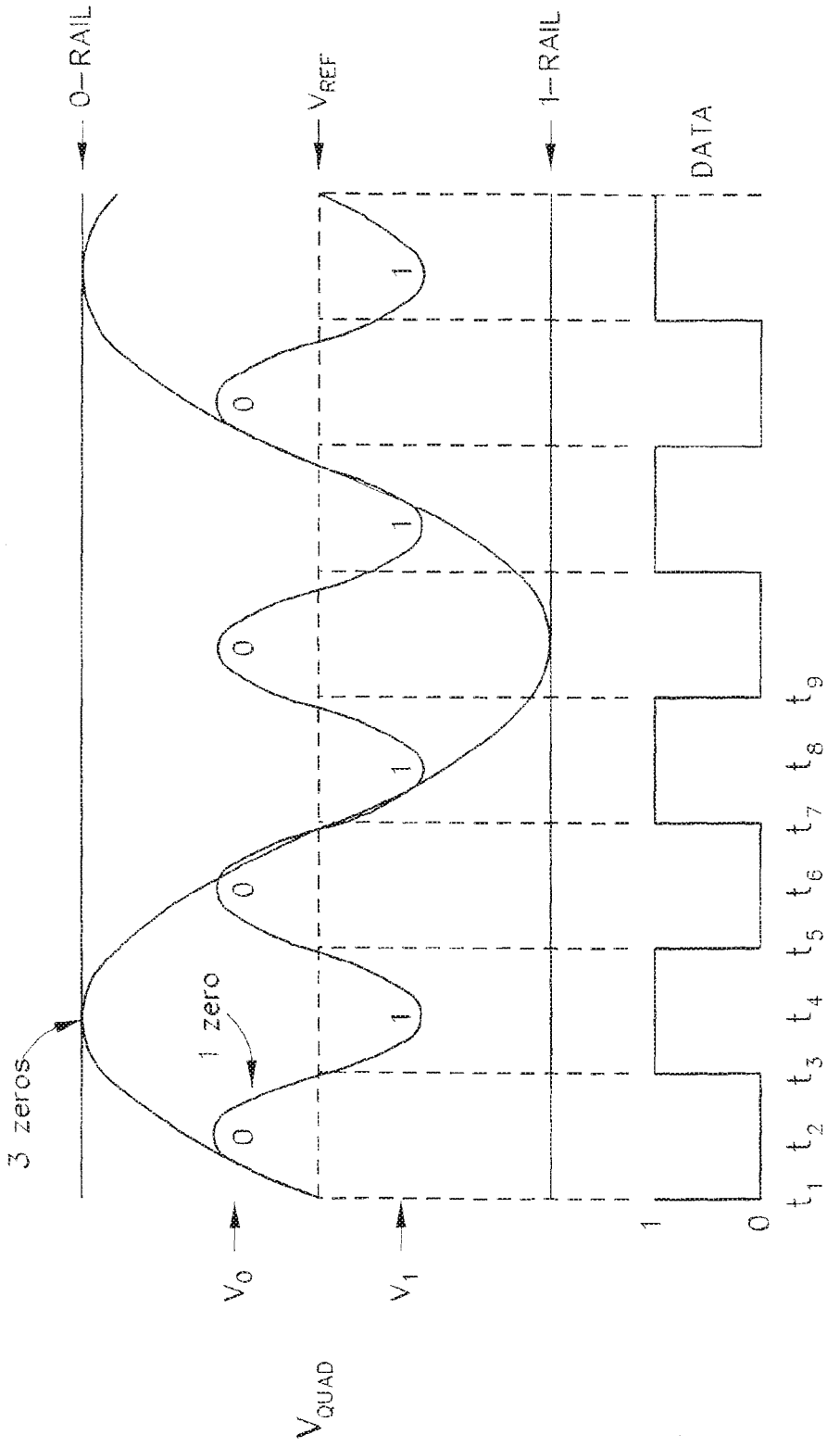

0-RAIL
V_{REF}
1-RAIL
DATA
3 zeros
1 zero
0
1
V_0
V_1
V_{QUAD}
t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8 t_9
TIME
IDEAL OPERATION

FIG. 7B

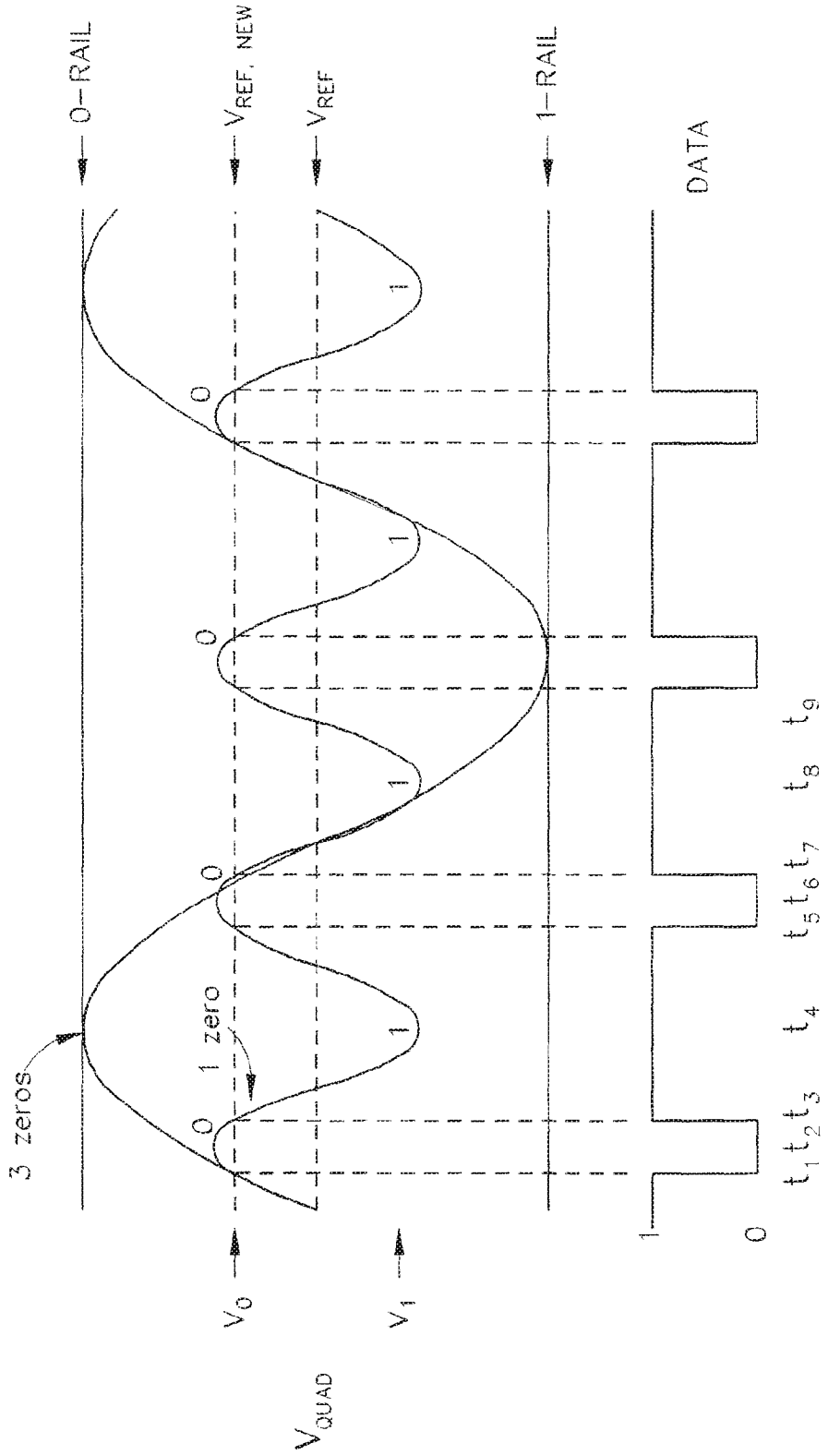
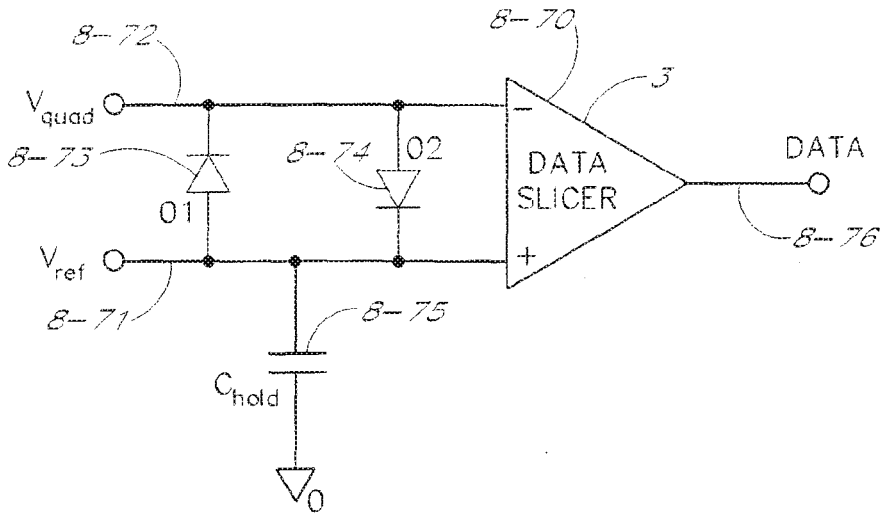


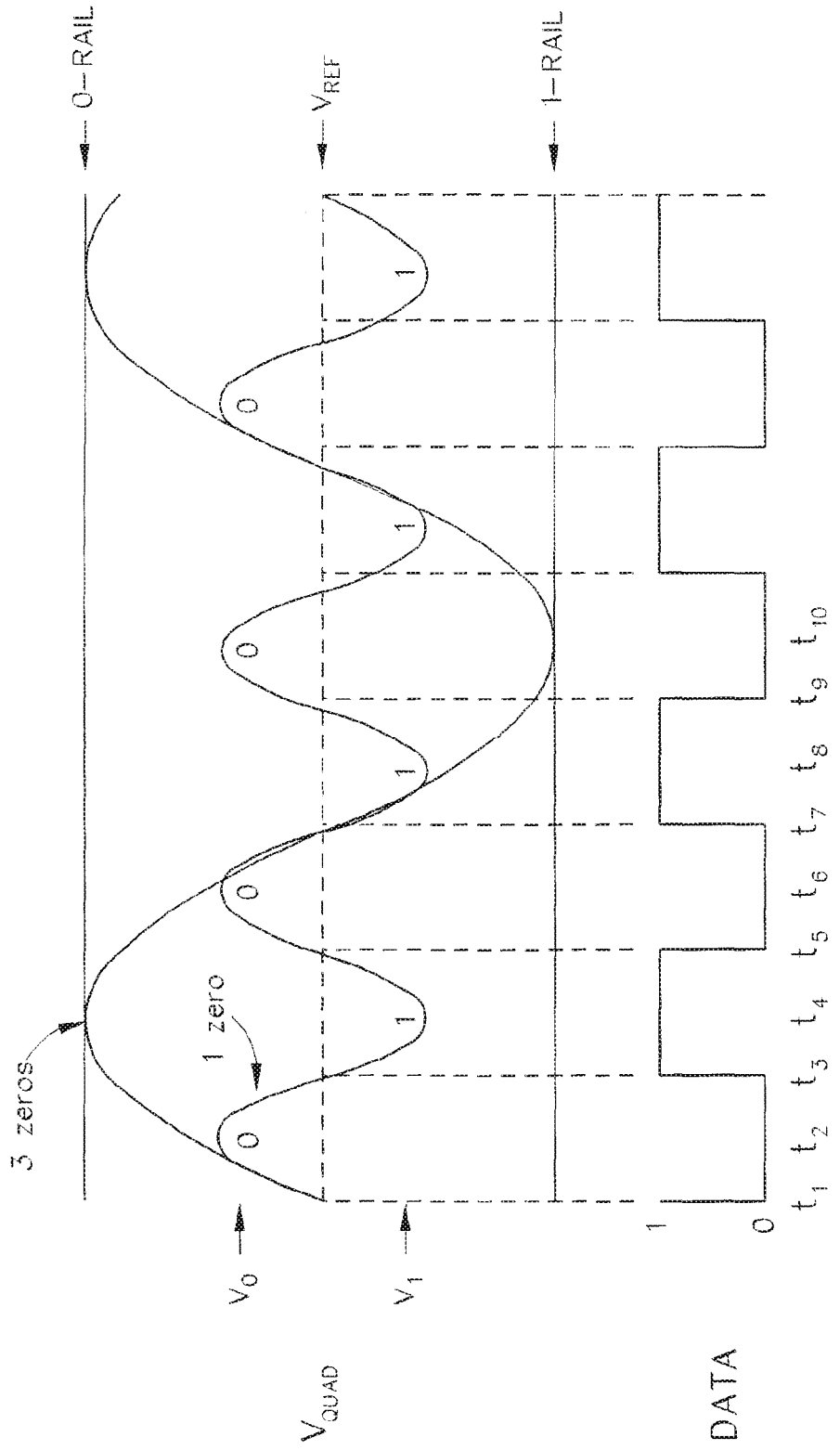
FIG. 7C

OPERATION WITH SIGNAL DRIFT



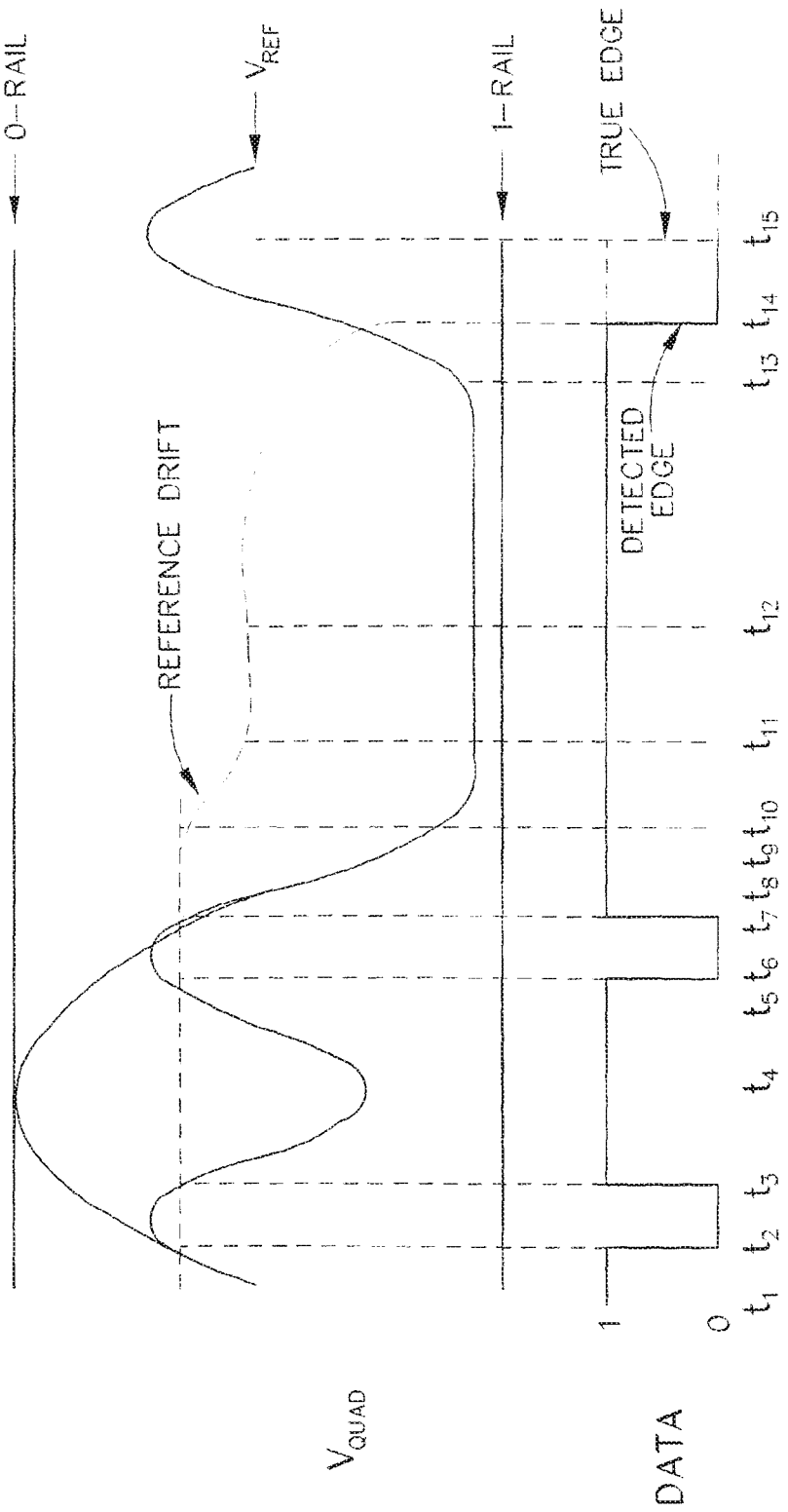
SLICER WITH TRACKING REFERENCE

FIG. 8A



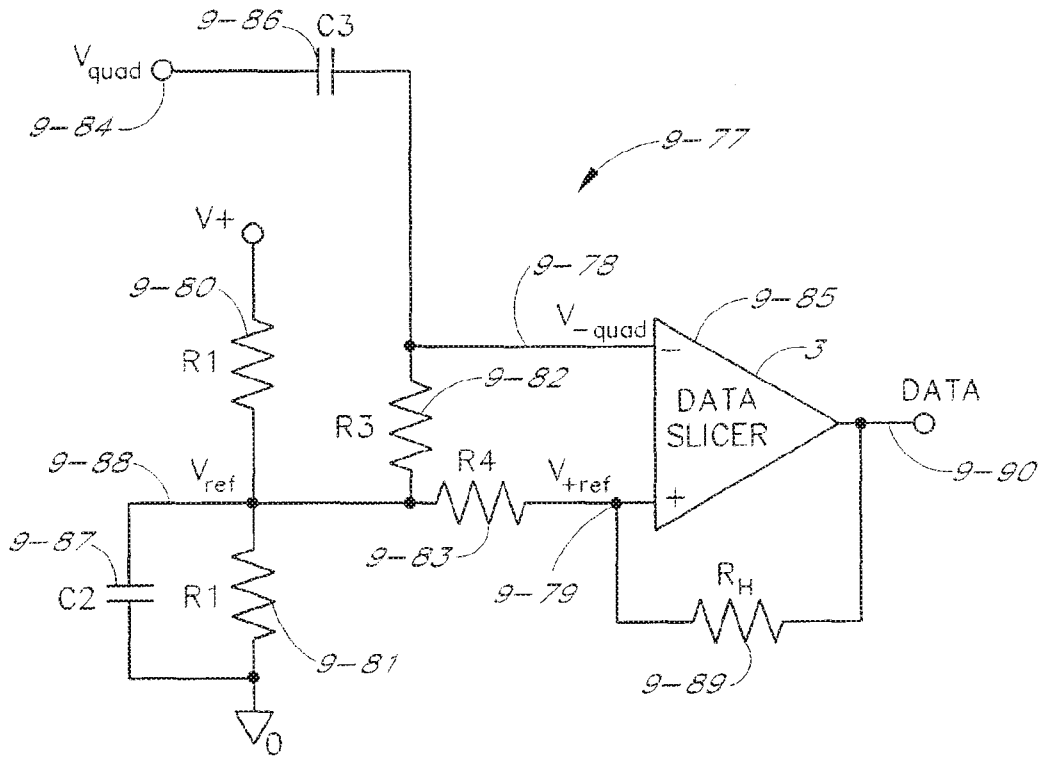
IDEAL OPERATION

FIG. 8B



OPERATION WITH REFERENCE DRIFT

FIG. 8C



AC-COUPLED SIGNAL

FIG. 9A

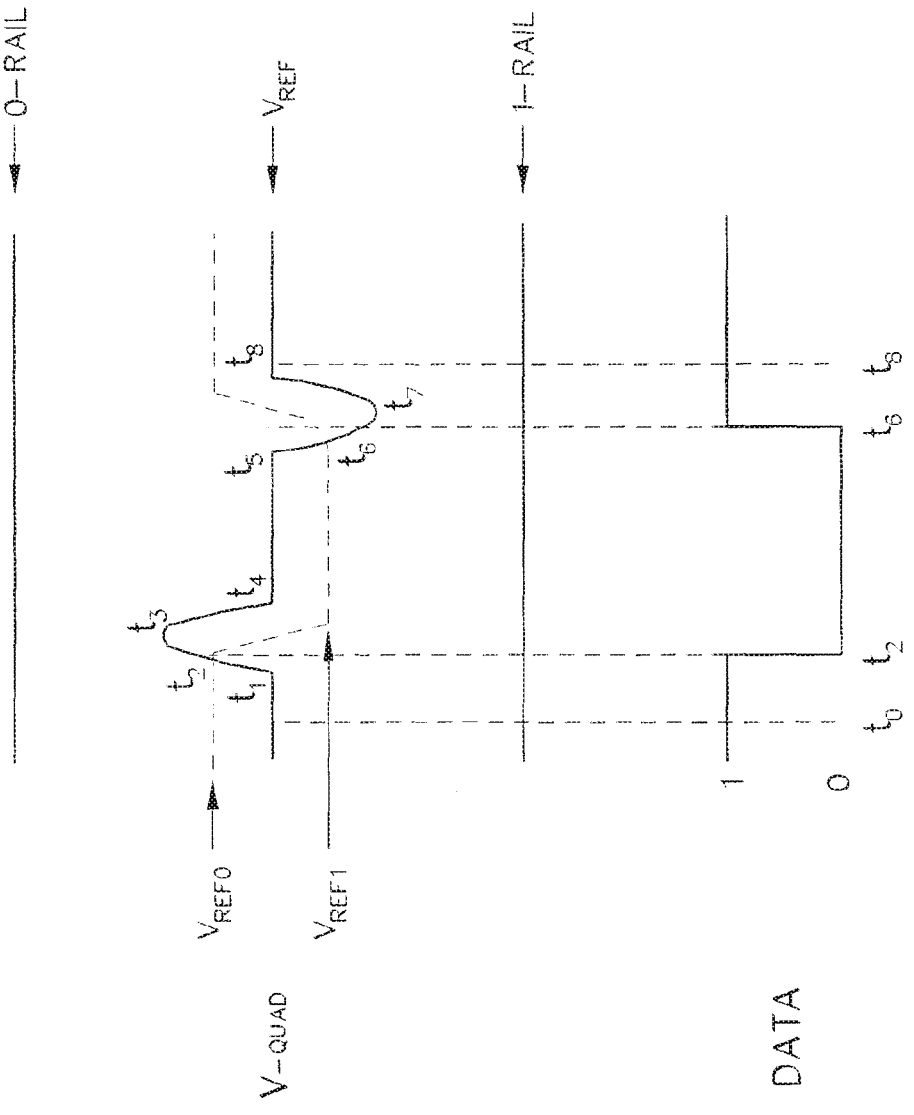

0-RAIL
VREF
1-RAIL
t8
t7
t5
t6
t4
t3
t2
t1
t0
t6 t8
t0 t2
VREF0
VREF1
V-QUAD
DATA
1
0
DFSK

FIG. 9B

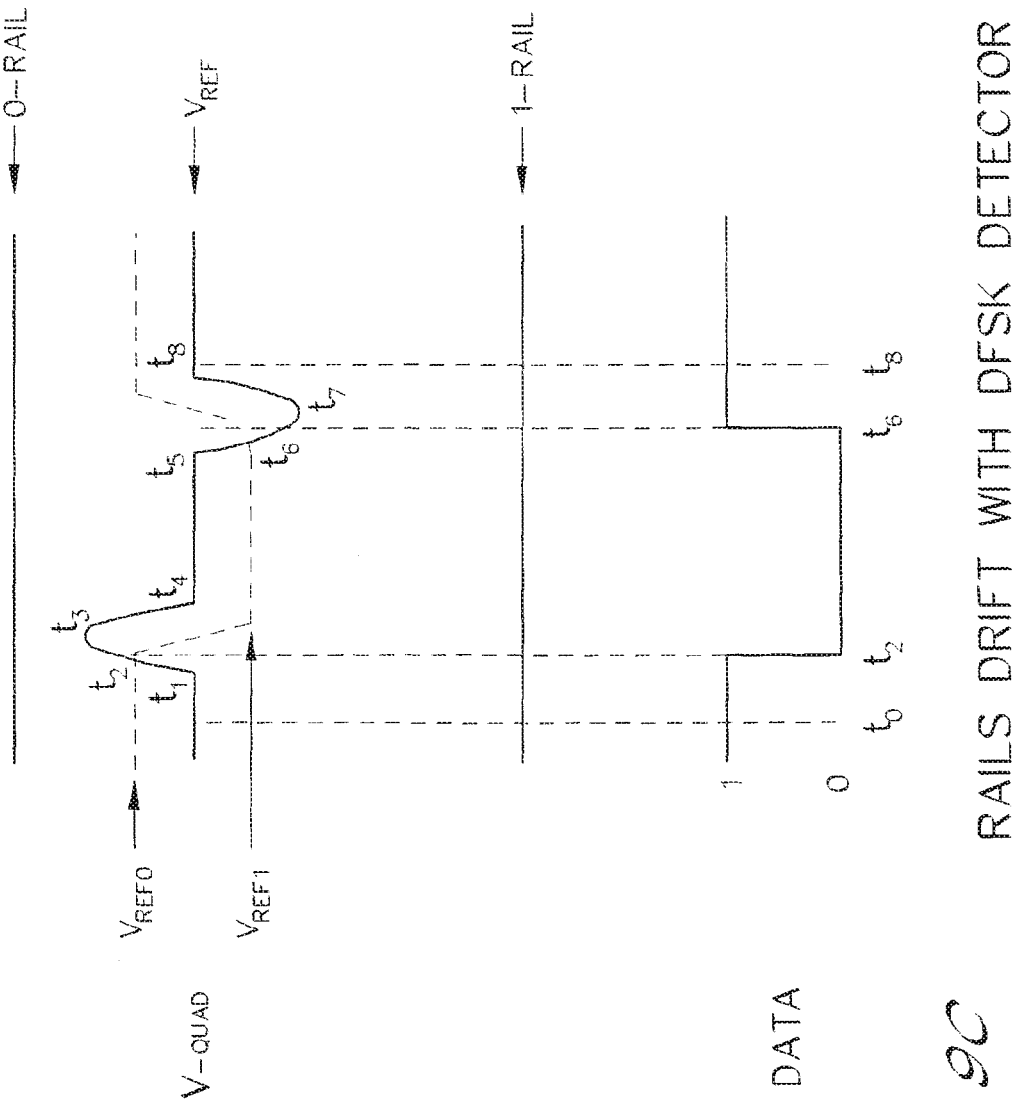
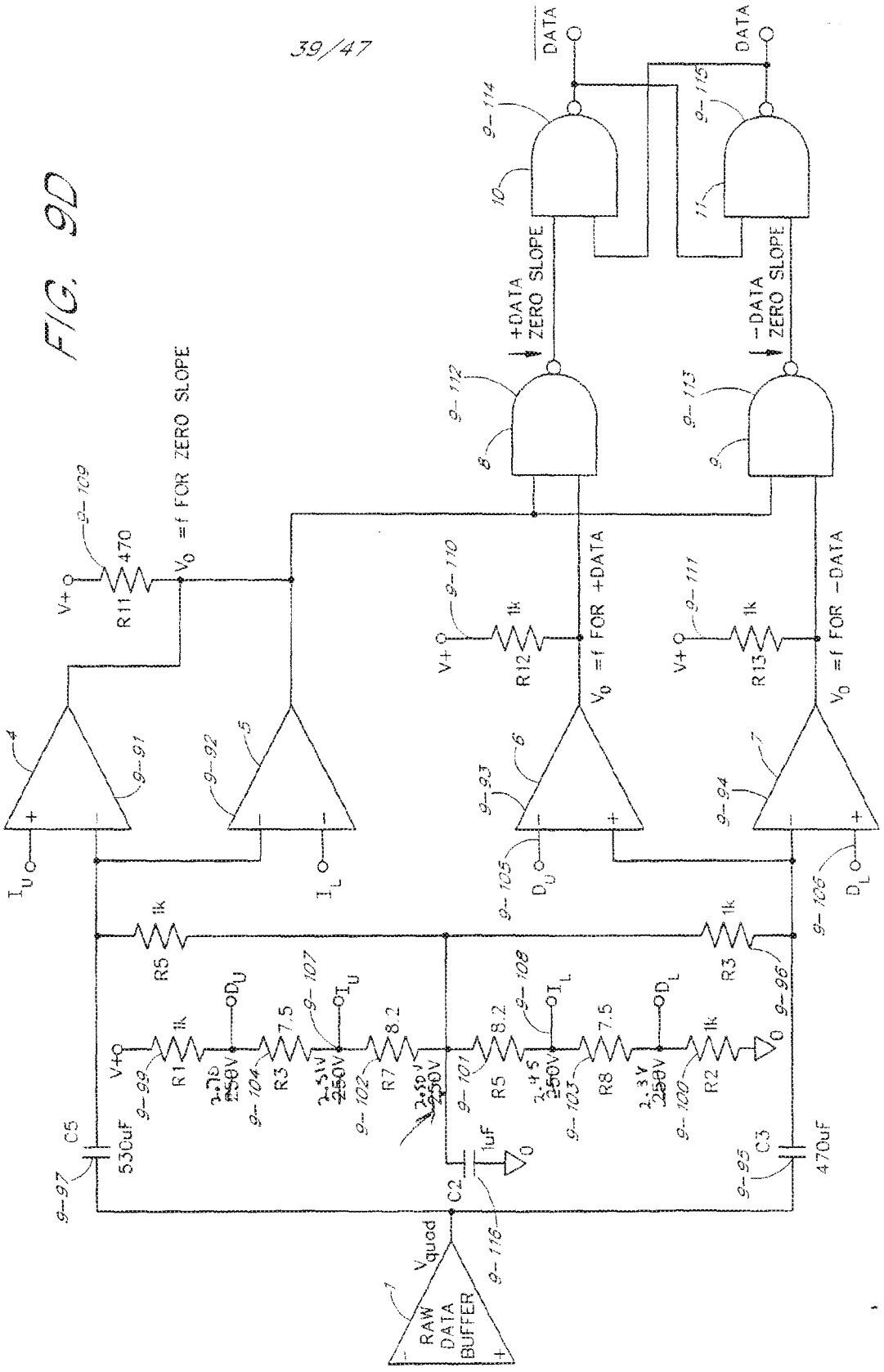


FIG. 9C

RAILS DRIFT WITH DFSK DETECTOR

39/47

FIG. 9D


DATA
DATA
9-114
9-115
10
11
+DATA ZERO SLOPE
-DATA ZERO SLOPE
9-112
9-113
8
9
V+
9-109
R11 470
V_0 = f FOR ZERO SLOPE
9-110
R12 1k
V_0 = f FOR +DATA
9-111
R13 1k
V_0 = f FOR -DATA
4
9-91
9-92
5
6
9-93
7
9-94
I_U
I_L
D_U
D_L
9-105
9-106
R5 1k
R3 1k
R1 1k
9-99
9-104
R3 7.5
9-107
9-102
R7 8.2
9-101
R5 8.2
9-108
9-103
R8 7.5
R2 1k
9-100
9-96
C5 530uF
9-97
C2 1uF
C3 470uF
9-95
V_{quad}
9-116
1
RAW DATA BUFFER

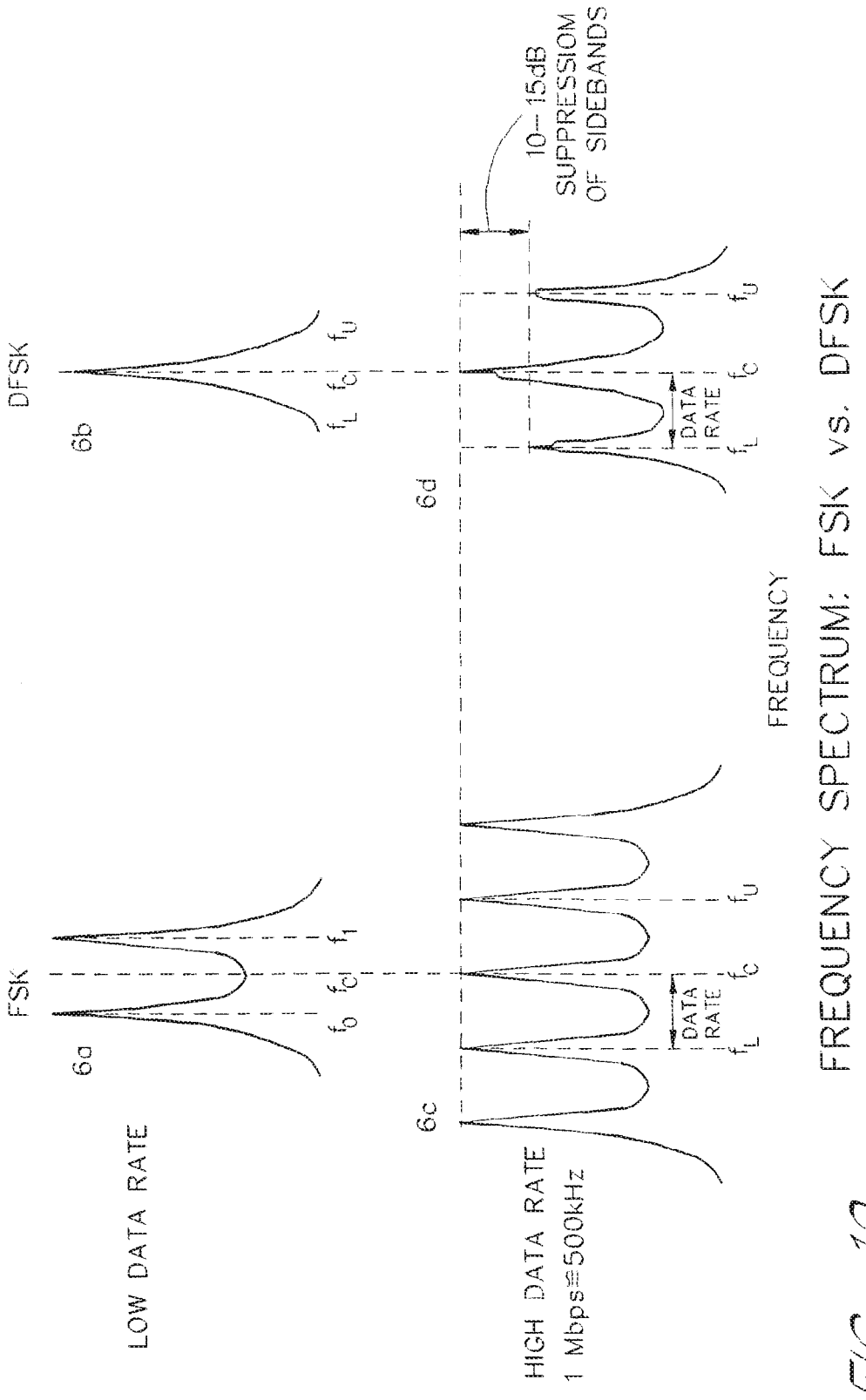

FREQUENCY SPECTRUM: FSK vs. DFSK
FREQUENCY
LOW DATA RATE
HIGH DATA RATE
1 Mbps≅500kHz
FSK
DFSK
6a
6b
6c
6d
f_0 f_c f_1
f_L f_c f_U
DATA RATE
10— 15dB SUPPRESSION OF SIDEBANDS

FIG. 10

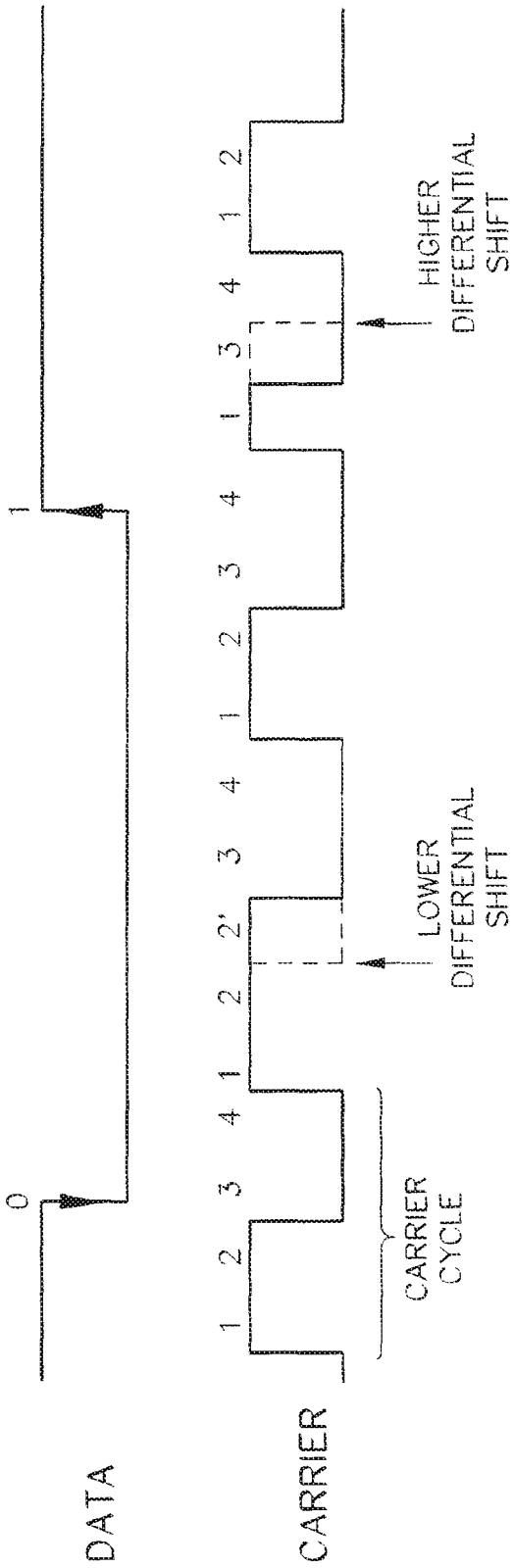


FIG. 11a

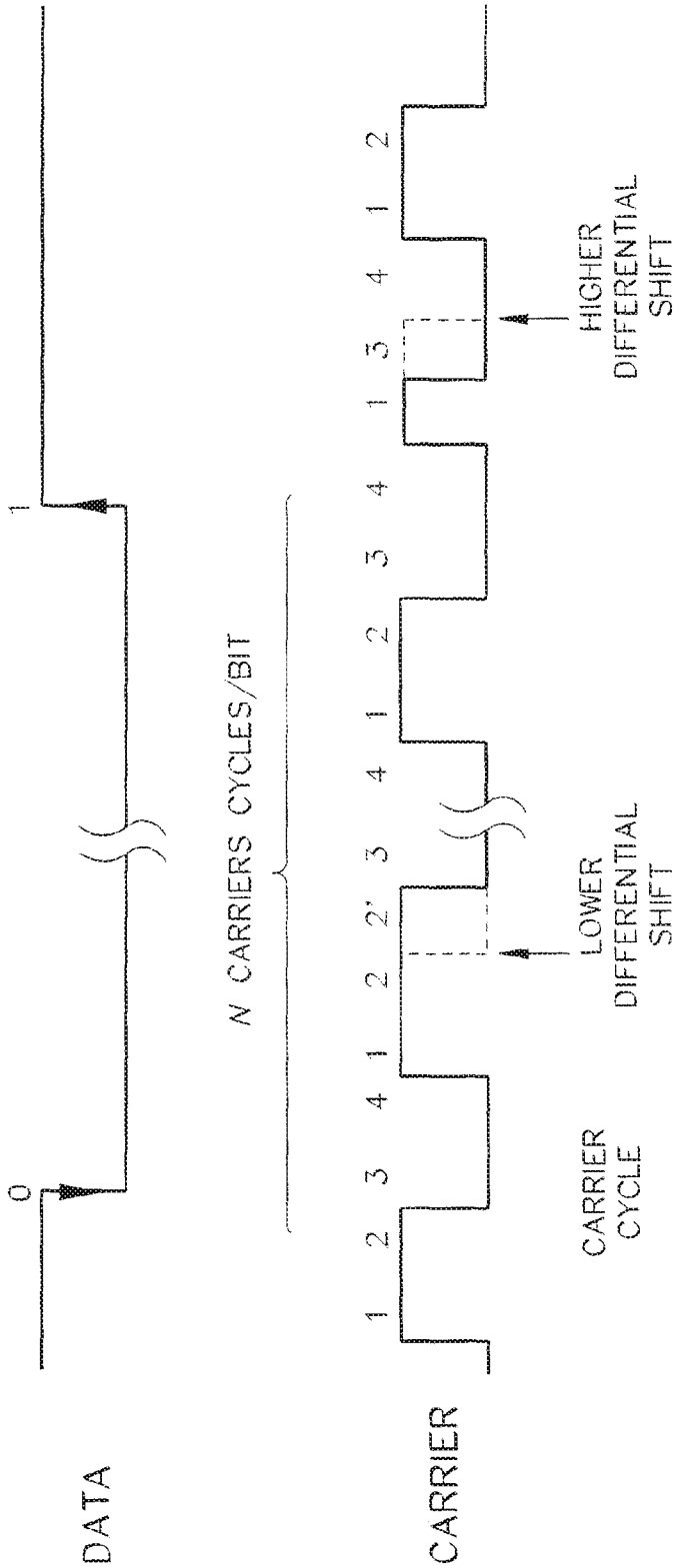


FIG. 11B

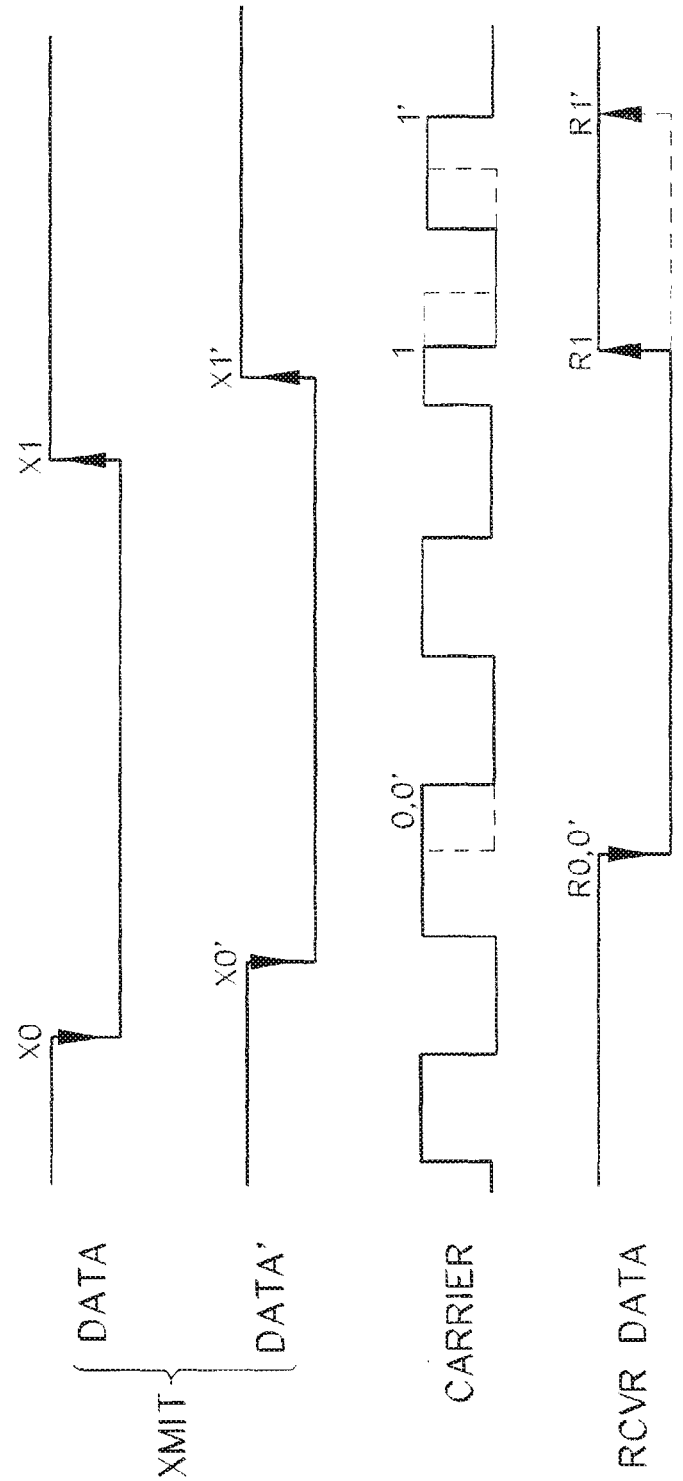


FIG. 12

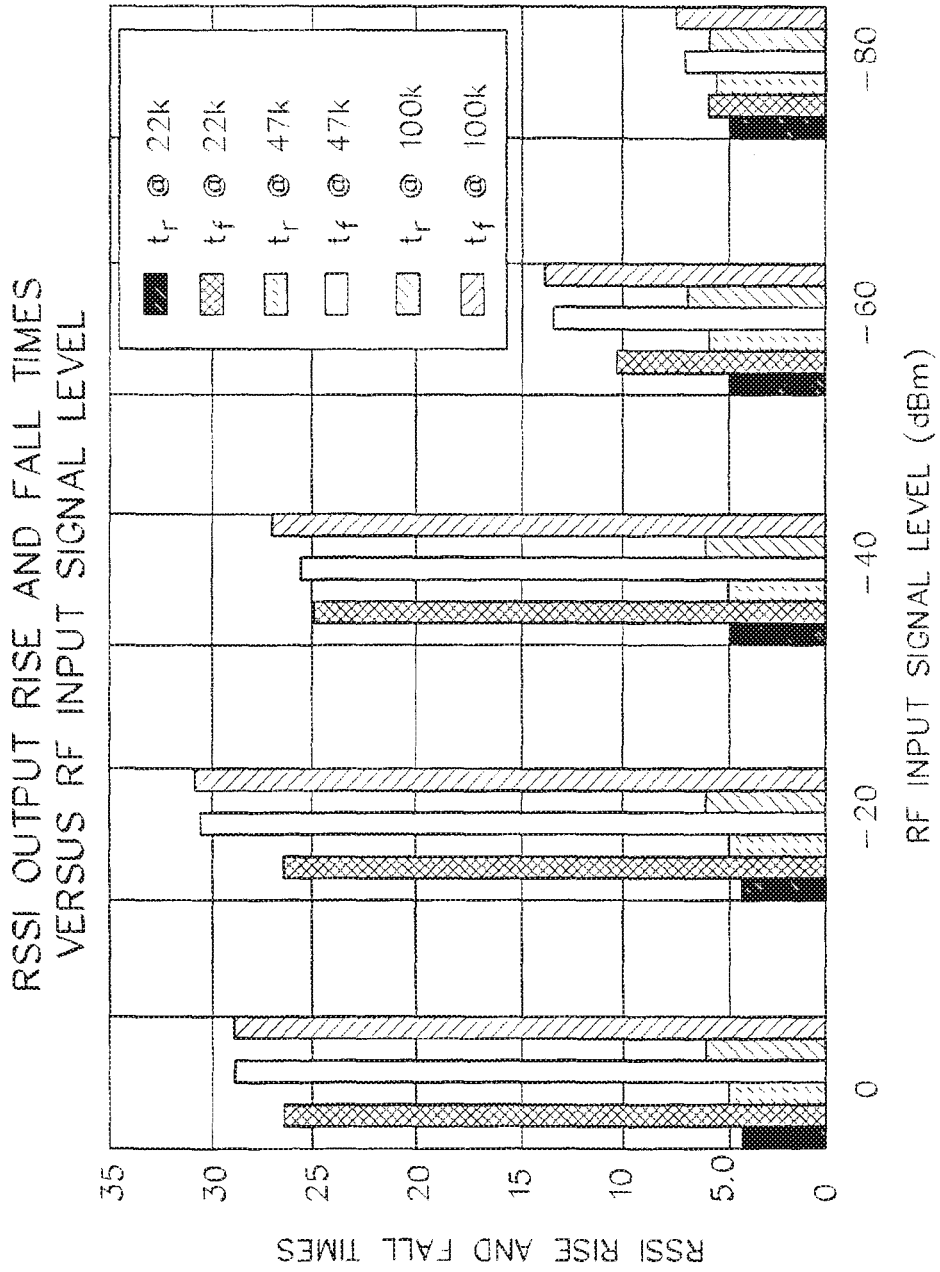
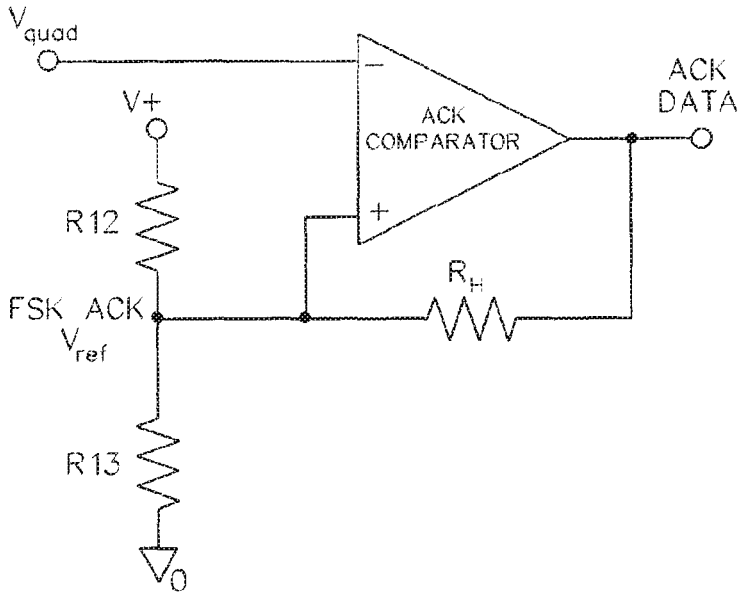

RSSI OUTPUT RISE AND FALL TIMES
VERSUS RF INPUT SIGNAL LEVEL
t_r @ 22k
t_f @ 22k
t_r @ 47k
t_f @ 47k
t_r @ 100k
t_f @ 100k
RSSI RISE AND FALL TIMES
0
5.0
10
15
20
25
30
35
0
-20
-40
-60
-80
RF INPUT SIGNAL LEVEL (dBm)

FIG. 13



ACK COMPARATOR

FIG. 14A

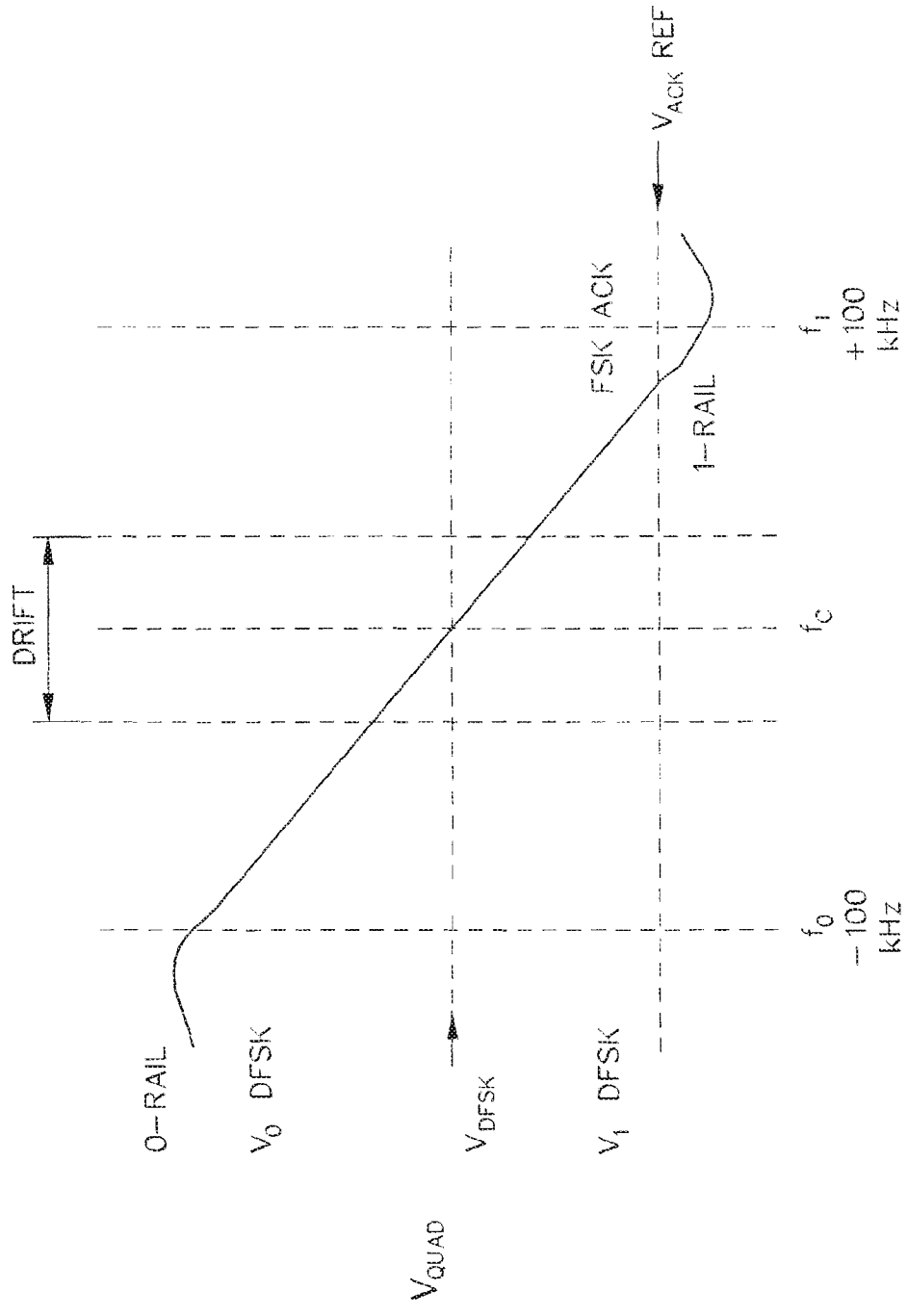

V_{ACK} REF
FSK ACK
1-RAIL
f_1 +100 kHz
f_c
f_0 -100 kHz
IF FREQUENCY
DRIFT
0-RAIL
V_0 DFSK
V_{DFSK}
V_1 DFSK
V_{QUAD}

FIG. 14B

47/47

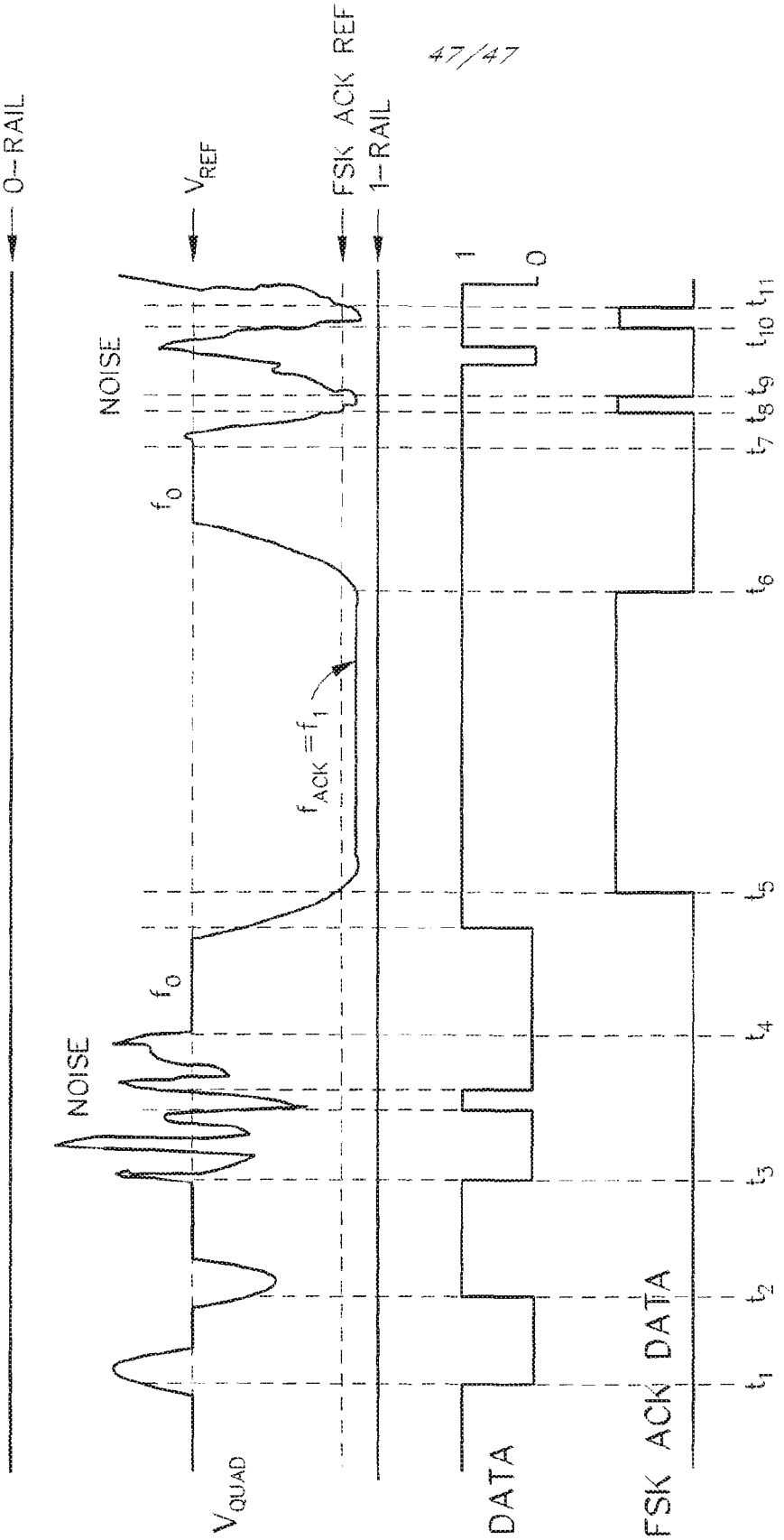


FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/11107

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G01R 31/08; H04H 27/10; H04L 27/10, 27/18, 5/16

US CL :Please See Extra Sheet.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 370/204, 205, 282, 284; 455/3.3, 403; 375/223, 244, 271, 272, 283, 303, 323, 329,330, 331, 332, 334, 346, 347, 350, 355

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4,580,276 A (ANDRUZZI et al) 01 April 1986, Fig. 2, Fig 4, and col. 8, lines 40-68.	1-24
Y	US 4,716,376 A (DAUDELIN) 29 December 1987, col. 1, line 65 to col.2, line 2.	1-24
Y	US 5,305,008 A (TURNER et al) 19 April 1994, col 10, line 47-56.	8
Y	US 4,001,692 A (FENWICK et al) 04 JAN 1977, col. 2, lines 5-7.	9

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
26 AUGUST 1998

Date of mailing of the international search report
0 1 OCT 1998

Name and mailing address of the ISA/US
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Authorized officer
STEVEN NGUYEN

Telephone No. (703) 308-8848

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/11107

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

370/204, 205, 282, 284; 455/3.3, 403; 375/223, 244, 271, 272, 283, 303, 323, 329,330, 331, 332, 334, 346, 347, 350, 355

Electronic Acknowledgement Receipt

EFS ID:	33623254
Application Number:	90013809
International Application Number:	
Confirmation Number:	7821
Title of Invention:	SYSTEM AND METHOD OF COMMUNICATION USING AT LEAST TWO MODULATION METHODS
First Named Inventor/Applicant Name:	8457228
Customer Number:	6449
Filer:	Michael Vincent Battaglia/Keiko Shelton
Filer Authorized By:	Michael Vincent Battaglia
Attorney Docket Number:	3277-0114US-RXM2
Receipt Date:	05-SEP-2018
Filing Date:	12-SEP-2016
Time Stamp:	16:45:59
Application Type:	Reexam (Patent Owner)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Foreign Reference	F1_CA1081848.pdf	5984533 7fec4551dbf3ffb79ecda6be6f2ceb40b39b4f3b	no	52

Warnings:

Information:					
2	Foreign Reference	F2_CA2236686.pdf	1303344 59e567daa4e029ad0e4198e53bc910aece66e954	no	13
Warnings:					
Information:					
3	Foreign Reference	F3_EP0496427.pdf	1937713 96696f957131df73196d4fb184584482e835cea0	no	14
Warnings:					
Information:					
4	Foreign Reference	F4_EP0562875.pdf	18521678 336b820e7154b4c0c1900ff383c74a11fac1f074	no	179
Warnings:					
Information:					
5	Foreign Reference	F5_EP0584865.pdf	1856956 0632c4b8618eb0c014687ef226f9ea72085f5d3b	no	15
Warnings:					
Information:					
6	Foreign Reference	F6_EP0700175.pdf	310765 02d4161fbd77c55cd1630deecb7522aa18df5495	no	3
Warnings:					
Information:					
7	Foreign Reference	F7_EP0730251.pdf	3072760 c66b28e6976cb821030824b70325b550e5197c9c	no	27
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Information:					
8	Foreign Reference	F8_EP0772923.pdf	425994 2545df579c891782f09349c077f5595b84206bef	no	4
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Information:					

9	Foreign Reference	F9_EP0774850.pdf	4249608 4d97b640fe1cef860e47b342b9b29dd0e6b06118	no	38
Warnings:					
Information:					
10	Foreign Reference	F10_EP_0845916.pdf	2081461 29d1509a8fd4d9d3eec44abf3203c64961cbbd45	no	16
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Information:					
11	Foreign Reference	F11_EP0869649.pdf	1279554 75fee8493d9d075073658fb49299e06d6fb10407	no	10
Warnings:					
Information:					
12	Foreign Reference	F12_JPS59113515.pdf	526393 396ebac00c0e77aba31f0c8f9b661f3028201e17	no	5
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Information:					
13	Foreign Reference	F13_MX9603371A.pdf	2960446 b9b4a9b9424f97f8a3bc9cc156b56b11929 5a3d8	no	48
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14	Foreign Reference	F14_WO_198302379.pdf	6411008 fd421d5e5f9667851090034463ec44a6978 9ac24	no	51
Warnings:					
Information:					
15	Foreign Reference	F15_WO_199105427.pdf	576869 608fe582af68242b21d34b4d2df2444ac1f7feef	no	12
Warnings:					
Information:					

16	Foreign Reference	F16_WO_199400943.pdf	2680335 b0933c2f07b4150e1ec1a1f25443d4348a544283	no	29
Warnings:					
Information:					
17	Foreign Reference	F17_WO_199419892.pdf	1844189 636b9b999f26678ac287d9d95a1d9ad2294fecb7	no	16
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Information:					
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Information:					
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Information:					
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Information:					
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Information:					

23	Non Patent Literature	1.pdf	4130685 0eb4cc1290e7d7984f3edc396f75d83b0a1df549	no	422
Warnings:					
Information:					
24	Non Patent Literature	2_Part1.pdf	25109453 048fab68153f6b2a9f22aad52f690acf8c250014	no	184
Warnings:					
Information:					
25	Non Patent Literature	2_Part2.pdf	25150179 890cf17d2c0d7ab7546300f94441e43d041353f4	no	188
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26	Non Patent Literature	2_Part3.pdf	10744884 b8b30049824ef265eddfb904fe0371e8a3a1df48	no	87
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Information:					
27	Non Patent Literature	3.pdf	1027893 de178e35e0944ddb4ae83031b45d3624e4f3d4a6	no	9
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Information:					
28	Non Patent Literature	4.pdf	517942 a71ac954e249368b0a3240ae7f472405ec874e11	no	4
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Information:					
29	Non Patent Literature	5.pdf	667915 277fe5b45ce841bf5d047c5a09b55fe5f05f9d5d	no	6
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30	Non Patent Literature	6.pdf	8907334 47fc4253c33be37db9d4a59c16526e5f894801c9	no	12
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Information:					
33	Non Patent Literature	9.pdf	2471355 72b690a6a6c713fae7498eda333d59252a870ee5	no	20
Warnings:					
Information:					
34	Non Patent Literature	10.pdf	3573445 a8c72dbeb8a3d000d7f46ce68679ff911fe12752	no	11
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Information:					
35	Non Patent Literature	11.pdf	272763 04efea948de4659de6e4873496b2f19c541d18bb	no	31
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Information:					
36	Non Patent Literature	12_A.pdf	25160903 0bc16a10b4dc6bd46cbf70f0869cdd93241107a3	no	192
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Information:					

37	Non Patent Literature	12_B.pdf	25129954 dcc76ae34014f7bb4aca3ae6e08f6fd7e20e2b40	no	198
Warnings:					
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38	Non Patent Literature	12_C.pdf	25136224 65cc048288d069b11733e20a67dc63434b553628	no	201
Warnings:					
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39	Non Patent Literature	12_D.pdf	25118573 12f886806beaba8e27c164481cd3667127e8a6fe	no	191
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40	Non Patent Literature	12_E.pdf	25145984 08d0508ec2c2bd03e118092b23afb06e0cb37a9f	no	185
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41	Non Patent Literature	12_F.pdf	8165248 9e80acfe9b95535b5e96ec82ce909e2acb11fdb8	no	53
Warnings:					
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42	Non Patent Literature	13.pdf	1091699 09151fe50821b284c5c85a9f5368879da199222b	no	5
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43	Non Patent Literature	14.pdf	1001729 88e608410d88c5ecc440ccf4bae8d5b2a64e822f	no	5
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44	Non Patent Literature	15.pdf	1464628 59a2d8674ee40258509b8ec3679ddc9e35da0894	no	24
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45	Non Patent Literature	16.pdf	2174497 45c0ae16a430864adc48d8007ddeb8d98ca5f44e	no	24
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46	Non Patent Literature	17.pdf	2383951 a4a8e3b80c1bfacc2296112e50b90049ba83098b	no	23
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47	Non Patent Literature	18_A.pdf	1281826 e8bd5b6fad67d46d0889ed7bc41f12d5f4d6ba43	no	16
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48	Non Patent Literature	18_B.pdf	781621 9d8629e49561e012a4226f473e916f1079476a4a	no	10
Warnings:					
Information:					
49	Non Patent Literature	18_C.pdf	1979097 1917c7d7f151b896a66a637ec84e785087a9d4a1	no	22
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50	Non Patent Literature	18_D.pdf	920650 133fd136ee6fa4246250e63a63f4aac61377ba5b	no	11
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51	Non Patent Literature	18_E.pdf	757818 4885b538ff94b31668f59303ea8e82edcf17236e	no	11
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52	Non Patent Literature	19.pdf	975028 d67c55a865cfd6f0cc43a386faa2599fd56af026	no	5
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54	Non Patent Literature	21.pdf	370019 b53c4b22144c966b5bee8ac94ede112c50d4ce3c	no	3
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Reexamination	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/013,809	8457228
	Certificate Date	Certificate Number

Requester Correspondence Address: ☐ **Patent Owner** ☑ **Third Party**

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LITIGATION REVIEW ☑	SLW (examiner initials)	2016-10-06T00:00:00 (date)
Case Name		Director Initials
IPR2015 - 00555		
IIPR2014-00889		
IPR2014-00890		
IPR2014-00891		
IPR2014-00892		
IPR2014-00893		
IPR2014-00895		

COPENDING OFFICE PROCEEDINGS	
TYPE OF PROCEEDING	**NUMBER**
Ex Parte Reexaminaiton	90/013808

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/013,809	8457228
	Examiner	Art Unit
	SCOTT L WEAVER	3992

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/02/2017	10/18/2018							
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CLAIM		DATE								
Final	Original	03/02/2017	10/18/2018							
	43									
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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	90013809
Filing Date	2016-09-12
First Named Inventor	Bremer (U.S. Patent No. 8,457,228)
Art Unit	3992
Examiner Name	Scott L. WEAVER
Attorney Docket Number	3277-114US-RXM2

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	2	5436901		1995-07-25	Koopman	
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	20	4807253		1989-02-21	Haganauer	
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	31	5363408		1994-11-08	Paik et al.	
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	Art Unit	3992
	Examiner Name	Scott L. WEAVER
	Attorney Docket Number	3277-114US-RXM2

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Attorney Docket Number	3277-114US-RXM2

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	1	P802.11 Draft Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specification.	
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	Examiner Name	Scott L. WEAVER
	Attorney Docket Number	3277-114US-RXM2

	32	"Lucent Technologies' New IEEE 802.11 Compliant WaveLan(R) Family Sets the Standard in Reliability, Efficiency for Wireless LANs."	

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EXAMINER SIGNATURE

Examiner Signature	/Scott L. Weaver/	Date Considered	10/18/2018

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Attorney Docket Number	3277-114US-RXM2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Michael V. Battaglia/	Date (YYYY-MM-DD)	2018-09-05
Name/Print	Michael V. Battaglia	Registration Number	64,932

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ART UNIT *3992* .

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

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REEXAMINATION OF U.S. PATENT 8,457,228

FINAL OFFICE ACTION

I. ACKNOWLEDGMENTS

This final office action is responsive to the Remarks filed on August 14, 2017 in response to the non-final action mailed on May 3, 2017.

On Sep. 12, 2016, third-party requester **("Requester")** filed a request **("Request")** for *ex parte* reexamination of claim 21 of US Patent # 8,457,228 **("228 patent")** issued to Bremer. The '228 patent issued on June 4, 2013, and was filed on August 4, 2011 and assigned application number 13/198,568 **(" '568 application").** On October 17, 2016, the Office mailed an order granting reexamination of claim 21 of the 228 patent. A non-final action was mailed on May 3, 2017.

II. INFORMATION DISCLOSURE STATEMENT

An information disclosure statement was submitted by the Requester on Sep. 12, 2016 (Sep 2016 IDS). The Sep 2016 IDS is in compliance with the provisions of 37 C.F.R. § 1.97. Accordingly, the Sep 2016 IDS has been considered by the Examiner and was made of record in the Order Granting Request for Ex Parte Reexamination.

An IDS was submitted by patent owner on September 5, 2018, (Sept 2018 IDS) the initialed IDS is attached to this office action. With respect to the IDS (Sept 2018 IDS) the "degree of consideration to be given to such information will be normally limited by the degree to which the party filing the information citation has explained the content and relevance of the information" in accordance with MPEP §§ 2256 and in "the same manner as other documents in Office search files are considered by the Examiner while conducting a search of the prior art in a proper field of search." In accordance with MPEP § 609.05(b).

Patent Owner's remarks submitted in relation to the (Sept 2018 IDS) have only been considered to the extent they explain the content and relevance of documents listed on the accompanying 1449 forms. Only those documents listed on the 1449 forms, in compliance with Rules 97 and 98, have been expressly considered by the examiner. Moreover, expunged or unavailable documents referred to in Patent Owner's IDS remarks, if any, have not been considered.

III. PRIORITY CLAIMS

The '228 patent is a continuation of US Patent Application 12/543,910 filed on Aug. 19, 2009, now patent US 8,023,580 ('580 Patent).

The '580 patent is a continuation of US Patent Application 11/774,803, filed on Jul. 9, 2007, now patent US 7,675,965, which is continuation of US Patent Application 10/412,878, filed on Apr. 14, 2003, now patent US 7,248,626, which is continuation-in-part of application 09/205,205, filed on Dec. 4, 1998, now patent US 6,614,838.

Application 09/205,205 claims priority to US provisional application 60/067,562 filed on Dec. 5, 1997.

There is no claim to foreign priority.

Because the effective filing date of the **'228** patent is not on or after March 16, 2013, the AIA First Inventor to File ("AIA-FITF") provisions do not apply. Instead, the earlier 'First to Invent' provisions apply.

Based upon a review of the '228 patent and prosecution history, the Examiner finds that there are no prior or concurrent *ex parte* or supplemental reexaminations for the '228 patent.

A co-pending request for ex parte reexamination (90/013,808) of the '580 patent has been filed on September 12, 2016.

IV. PRIOR ART

A. References Cited in the Request

1. U.S. Patent No. **5,982,807**, to **Snell,** J., filed on Mar. 17, 1997 and issued on Nov. 9, 1999, ("**Snell**").

2. U.S. Patent No. **6,075,814**, filed on May 9, 1997 and issued on Jun. 13, 2000, to **Yamano** et al. ("**Yamano**").

3. "Using the PRISM™ Chip Set for Low Data Rate Applications," Andren, C. et al., Harris Semiconductor Application Note No. AN9614, March 1996 ("**Harris AN9614**").

4. "HSP3824 Direct Sequence Spread Spectrum Baseband Processor," Harris Semiconductor File No. 4064.4, Oct. 1996 ("**Harris 4064.4**").

5. **Kamerman, A**., "Throughput Density Constraints for Wireless LANs Based on DSSS," IEEE 4th International Symposium on Spread Spectrum Techniques and Applications Proceedings, Mainz, Germany, Sept. 22-25, 1996, pp. 1344-1350 vol.3 ("**Kamerman**").

6. **Upender** et al., "Communication Protocols for Embedded Systems," Embedded Systems Programming, Vol. 7, Issue 11, November 1994. - ("**Upende**r").

B. References Cited in 2014IPR-00892

1. U.S. Patent No. 5,706,428, to Boer et al. filed on Mar. 14, 1996 and issued Jan.6, 1998 ("**Boer**")

IV. CLAIM INTERPRETATION

During re-examination, claims are given the broadest reasonable interpretation consistent with the specification and limitations in the specification are not read into the claims. See MPEP § 2111 et seq.

A. Lexicographic Definitions

A first exception occurs when there is lexicographic definition in the specification. After a review of the original specification, the prosecution history, and unless expressly noted otherwise below, the examiner is unable to locate any lexicographic definitions (either express or implied) with reasonable clarity, deliberateness, and precision and therefore concludes that Applicants are not their own lexicographer. See MPEP §2111.01 IV.

B. 35 U.S.C. § 112 6th Paragraph

A second exception is when a claimed phrase is interpreted in accordance with 35 U.S.C. § 112 6th paragraph. See MPEP § 2181 *et seq.* The statute, 35 U.S.C. § 112, ¶6 states:

> An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.
>
> -- 35 U.S.C. § 112 6th Paragraph.

To invoke 35 U.S.C. § 112 6th paragraph, a claimed phrase must be an element in a claim for a combination. Claim 21 of the '228 patent depends from independent claim 1, claim 21 thus includes all limitations of the claim from which it depends and reads as follows:

> **1.** A master communication device configured to communicate with one or more slave transceivers according to a master/slave relationship in which a slave communication from a slave device to the master communication device occurs in response to a master communication from the master communication device to the slave device,
> the master communication device comprising:

a master **transceiver** configured to transmit a first message over a communication medium from the master transceiver to the one or more slave transceivers, wherein **the first message** comprises:

first information modulated according to a first modulation method,

second information, including a payload portion, modulated according to the first modulation method,

wherein the second information comprises data intended for one of the one or more slave transceivers and

first message address information that is indicative of the one of the one or more slave transceivers being an intended destination of the second information; and

said master transceiver configured to transmit a second message over the communication medium from the master transceiver to the one or more slave transceivers wherein the second message comprises:

third information modulated according to the first modulation method,

wherein the third information comprises information that is indicative of an impending change in modulation to a second modulation method, and

fourth information, including a payload portion, transmitted after transmission of the third information,

the fourth information being modulated according to the second modulation method, the second modulation method being of a different type than the first modulation method, wherein the fourth information comprises data intended for a single slave transceiver of the one or more slave transceivers, and

second message address information that is indicative of the single slave transceiver being an intended destination of the fourth information; and

wherein the second modulation method results in a higher data rate than the first modulation method.

21. The master communication device as in claim **1,** wherein **the first information that is included in the first message comprises the first message address data.**

The limitations of claim 21 including the limitations of claim 1 comprise a single means, i.e., a transceiver. According to 35 U.S.C. 112 6th paragraph, only limitations or elements in a claim

for a combination may invoke 112 6th paragraph, the Examiner concludes that claim 21 does **not invoke 35 USC 112 6th paragraph.**

C. Sources.

Except for either (a) any lexicographic definitions noted in § IV.A of this Office action; or (b), any entire claim phases that *invoke* 35 U.S.C. § 112 6th paragraph as noted in § IV.B of this Office action; the **following interpretations are adopted under the broadest reasonable interpretation standard (BRI)**. The scope of claim 21 is the same regardless of whether claim terms are interpreted under the BRI or *Phillips* standard. The following provided as *express notice* of how particular terms are being interpreted under the broadest reasonable interpretation standard. These interpretations are only a guide to claim terminology since claim terms must be interpreted in context of the surrounding claim language. In accordance with *In re Morris*, 127 F.3d 1048, 1056, 44 USPQ2d 1023, 1029 (Fed. Cir. 1997), **the following "sources" support a broadest reasonable interpretation of the claims. The following list is not intended to be exhaustive**:

1. Modulation -- the process by which some characteristic of a carrier is varied in accordance with a modulation wave (IPR2014-00892, Pap. 46 at p. 7; Request, p. 19; IEEE170-1964 - IEEE Standard Definitions of Terms for Modulation Systems, 1964, page 6).

2. **First and Second 'Modulation Method'**– modulation methods that are incompatible with one another (IPR2014-00892), Pap. 46 at p. 13, Request, pp. 12-13 and pp. 19-23).

3. **Transceiver** – Term for a combination transmitter/receiver (Snell, col. 1, lines 34-36); a radio that can send and receive messages (Merriam-Webster.com).

D. Product-by-Process Claims

A third exception is for product-by-process claims, claim 21 is a product claim.[1]

In accordance with an absence of remarks with respect to the product by process issue Section IV.D. Office Action of May 3, 2017, it is understood the claims are not directed to a product by process.

[1] "Product claims are claims that are directed to either machines, manufactures, or compositions of matter." MPEP § 2103 I C.

V. CLAIM REJECTIONS - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A.) Claim 21 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art (APA) in view of Boer and further in view of Yamano.

Claim 1 was reviewed (IPR 2014-00892) and it was found that there was a reasonable likelihood that petitioner would prevail in challenging claim 1 for obviousness over APA and Boer[2], a Final Written Decision was entered on September 24, 2015 (IPR2014-00892, Paper 46), as such, Claim 1 is rejected for the reasons indicated in the Final Written Decision entered on September 24, 2105 (IPR2014-00892, Paper 46) as obvious over APA and Boer.

> While the APA in view of Boer was deemed an appropriate rejection on claim 1 including the limitations that the first message include first message address information that is indicative of the one of the one or more slave transceivers being an intended destination of the second information; The APA in view of Boer did not teach as pertains to claim 21 "The master communication device as in claim 1, wherein the first information that is included in the first message comprises the first message address data."
>
> Yamano teaches that packets can be advantageously addressed for an intended destination. Yamano discloses transmitting a "first message" *(e.g.,* data packet including a preamble and main body) that includes "first message address information that is indicative" *(e.g.,* "destination address" in the preamble) of the transceiver that is the "intended destination of the second information."
>
> *"Packet 700* includes a *preamble 701* and a *main body 702."* Yamano at 19:63-64.
>
> "For example, *preamble 701* can include information which identifies: (1) a version or type field for the preamble, (2) ***packet source and destination addresses,*** (3) the line code (i.e., the modem protocol being used), (4) the data rate, (5) error control parameters, (6) packet length and (7) a timing value for the expected reception slot of a subsequent packet." Yamano at 20:1-7.

[2] IPR2014-00892

Yamano also discloses that the preamble precedes the main body (containing data), as shown in Figure 8. Yamano teaches that the first message comprises first message address information that is indicative of the one of the one or more slave transceivers being an intended destination of the second information. *See, e.g.,* Yamano at 19:63-64, 20:1-7, 20:54-59, Fig. 8.

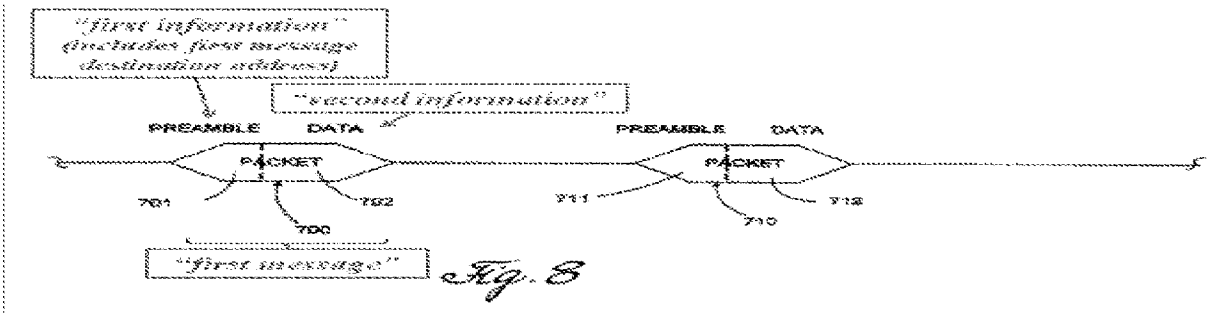

Fig. 8

Yamano at Fig. 8 (annotated).

Yamano expressly teaches that including a destination address in the preamble portion of the data packet, which precedes the data portion, will advantageously reduce processing requirements of receiving devices because the receiving device can filter out packets which it does not need to demodulate. Yamano at 20:54-59 ("When the preamble in a burst-mode packet *includes the destination address of the packet,* the receiver circuits can monitor the destination address of the packet, and in response, filter packets which do not need to be demodulated, thereby reducing the processing requirements of the receiver circuits."). (Yamano at 19:63-20:7, Fig. 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Yamano' s teaching of including a destination address in the preamble portion of a data packet in implementing the modified Boer APA data packet to advantageously specify which receiver the data is intended for and to beneficially reduce the processing requirements at the receiving device, as taught by Yamano. "When the preamble in a burst-mode packet *includes the destination address of the packet,* the receiver circuits can monitor the destination address of the packet, and in response, filter packets which do not need to be demodulated, thereby reducing the processing requirements of the receiver circuits." Yamano at 20:54-59.

In the following rejections under 35 USC §103, all limitations are interpreted **under a broadest reasonable interpretation**, see section IV.C. above.[3] The scope of claim 21 is the same

[3] Examiners are unaware of any requirement that there should be a single Broadest Reasonable Interpretation (BRI). If Patent owner is aware of any statue, rules, or case law requiring such, examiners request Patent Owner present such authority in the next response. The broadest reasonable interpretation does not mean the broadest possible

regardless of whether claim terms are interpreted under the BRI or *Phillips* standard. The scope is the same because for example claim 21 is a product claim. Claims 21 only explicitly recites one structure. A review of the claims, specification, and prosecution history in light of Patent Owner remarks finds insufficient evidence that Patent Owner has indicated a particular interpretation that requires other structures. Accordingly the Examiners conclude that the interpretations would result in same scope.

21. The master communication device as in claim 1, wherein the first information that is included in the first message comprises the first message address data.

Snell in view of Yamano and further in view of Kamerman as recited above disclose that the **first information that is included in the first message comprises the first message address** as indicated in the rejection of claim 1 above with reference to the first message address of the destination, therefore the first message address data is included in the actual message when transmitted by the master to the slave transceiver.

Yamano expressly teaches that including a destination address in the preamble portion of the data packet, which precedes the data portion, will advantageously reduce processing requirements of receiving devices because the receiving device can filter out packets which it does not need to demodulate. Yamano at 20:54-59 ("When the preamble in a burst-mode packet *includes the destination address of the packet*, the receiver circuits can monitor the destination address of the packet, and in response, filter packets which do not need to be demodulated, thereby reducing the processing requirements of the receiver circuits.").

C.) Claim 21 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Snell in view of Harris 4064.4, further in view of Harris AN9614, further in view of Yamano and further in view of Kamerman.

1. A master communication device configured to communicate with one or more slave transceivers according to a master/slave relationship in which a slave communication from a slave device to the master communication device occurs in response to a master communication from the master communication device to the slave device,

---

interpretation. Rather, the meaning given to a claim term must be consistent with the ordinary and customary meaning of the term (unless the term has been given a special definition in the specification), and must be consistent with the use of the claim term in the specification and drawings. Further, the broadest reasonable interpretation of the claims must be consistent with the interpretation that those skilled in the art would reach. (MPEP) § 2111. The scope of the claim 21 is same regardless of whether claim terms are interpreted under the BRI or *Phillips* standard.

> Snell discloses a master communication device (transceiver 30) that serves as an access point for communicating data with other transceivers connected to a wireless local area network (WLAN) and is configured to communicate with one or more slave transceivers (end users connect to LAN through transceivers) according to a master/slave relationship in which a slave communication from a slave device to the master communication device occurs in response to a master communication from the master communication device to the slave device. *See, e.g.*, Snell at 1:34-46,1:47-50,1:55-57, 2:27-30, 4:42-47, 5:18-21; Harris AN9614 at 3.
>
> Snell at 4:42-47 ("Referring to FIG. 1, a ***wireless transceiver 30*** in accordance with the invention is first described. The *transceiver 30 may be readily used for WLAN applications* in the 2.4 GHZ ISM band in accordance with the proposed IEEE 802.11 standard. Those of skill in the art will readily recognize other applications for the transceiver 30 as well."
>
> "In a typical WLAN, ***an access point provided by a transceiver*****, that is, a combination transmitter and receiver,** connects to the wired network from a fixed location. Accordingly, the access transceiver receives, buffers, and transmits data between the WLAN and the wired network. *A single access transceiver can support a small group of collocated users within a range of less than about one hundred to several hundred feet. The* ***end users connect to the WLAN through transceivers*** which are typically implemented as PC cards in a notebook computer, or ISA or PCI cards for desktop computers. Of course the transceiver may be integrated with any device, such as a hand-held computer." Snell at 1:34-46.

With respect to the 'slave communication from a slave device to the master communication device occurring in response to a master communication from the master communication device to the slave device', Snell teaches the master (access point transceiver) communicates with slave transceivers on the WLAN via **polled protocol**. A **polled protocol** is a master/slave protocol as confirmed by the '228 patent, '228 patent at 4:30-34 where the slave is given permission to transmit on the network.

> Snell incorporates by reference Harris AN9614[4], which discloses that the communications between transceivers can operate according to a polled (*i.e.*,

[4] Snell expressly incorporates by reference "the entire disclosure" of Harris AN9614 (Snell at 5:2-7). *See Harari v. Lee,* 656 F.3d 1331, 1335-36 (Fed. Cir. 2011) ("the entire '579 application disclosure was incorporated by the broad and unequivocal language: 'The disclosures of the two applications are hereby incorporate[d] by reference.'"); *see also Advanced Display Sys., Inc. v. Kent State Univ.,* 212 F.3d 1272, 1282 (Fed.Cir.2000) ("material not explicitly contained in the single, prior art document may still be considered **for purposes of anticipation** if that material is incorporated by reference into the document.").

master/slave) protocol, which is a master/slave communication system.[5] *See e.g.*, Harris AN9614 at 3.

"[T]he controller can keep adequate time to operate either a polled or a time allocated scheme. In these modes, the radio is powered off most of the time and only awakens when communications is expected. This station would be awakened periodically to listen for a beacon transmission. The beacon serves to reset the timing and to alert the radio to traffic. If traffic is waiting, the radio is instructed when to listen and for how long. In **a polled scheme**, the remote radio can respond to the poll with its traffic if it has any. With these techniques, the average power consumption of the radio can be reduced by more than an order of magnitude while meeting all data transfer objectives." Harris AN9614 at 3.

the master communication device comprising:
a master transceiver configured to transmit a first message over a communication medium from the master transceiver to the one or more slave transceivers,

An access point (wireless transceiver 30, figure 1, 4:42-47 corresponds to a master communication device) connected to a LAN (WLAN), the transceiver communicates with one or more transceivers connected to the LAN, communication on the LAN to and from external networks is provided through the access point as in typical LAN (1:34-46).

Snell discloses the "transceiver" 30 that serves as an access point for communicating "data intended for one of the one or more [other] transceivers" connected to a wireless local area network (WLAN). Snell's transceiver transmits data packets intended for another transceiver, where the communication may switch on-the-fly between a "first modulation method" *(e.g.,* BPSK) and a "second modulation method" *(e.g.,* QPSK) that is "of a different type than the first modulation method." *Id* at 2:61-63

For example, Snell discloses a "transceiver" (a master transceiver 30 with respect to an access point in a local area network) that serves as an access point for communicating data with other transceivers connected to a wireless local area network (WLAN) (end user transceivers connected to the WLAN are slave transceivers). Snell 1:34-46, 1:47-50, 4:42-47, 5:18-21.

"In a typical WLAN, *an access point provided by a transceiver,* that is, a combination transmitter and receiver, connects to the wired network from a fixed location. Accordingly, the **access transceiver receives, buffers, and transmits data between the**

[5] A polled protocol is a master/slave protocol, as confirmed by the '228 patent. '228 patent at 4:30-34. *See also* IPR2014-00892, Pap. 46 at 16 ("In [a polling] protocol, a centrally assigned master periodically sends a polling message to the slave nodes, giving them explicit permission to transmit on the network."); '228 Prosecution History at 352; IPR2014-00892, Ex.1323 (Goodman Declaration) Para124.

WLAN and the wired network. *A single access transceiver can support a small group of collocated users within a range of less than about one hundred to several hundred feet. The end users connect to the WLAN through transceivers...*" Snell at 1:34-46.

Snell references processors enabling the disclosed transceiver functions and incorporates by reference Harris AN9614 and Harris 4064.4. (Snell at 5:8-17, 5:31-33)

"Like the HSP3824 baseband processor, the high data rate baseband processor 40 of the invention contains all of the functions necessary for a full or half duplex packet baseband *transceiver*." Snell at 5:18-21.

"The PRISM 1 chip set provides all the functions necessary for full or half duplex, direct sequence spread spectrum *packet communications* at the 2.4 to 2.5 GHz ISM radio band." Snell at 1:55-57.

See also, e.g., Snell at 2:27-30 ("It is another object of the invention to provide *a spread spectrum transceiver* and associated method to permit operation at higher data rates and which may switch on-the-fly between different data rates and/or formats."); Snell at 1:47-50 ("The assignee of the present invention has developed and manufactured a set of integrated circuits for a WLAN under the mark PRISM 1 which is compatible with the proposed IEEE 802.11 standard."); Snell at 4:42-47 ("Referring to FIG. 1, a *wireless transceiver 30* in accordance with the invention is first described. The *transceiver 30 may be readily used for WLAN applications* in the 2.4 GHZ ISM band in accordance with the proposed IEEE 802.11 standard. Those of skill in the art will readily recognize other applications for the transceiver 30 as well."

Treating Harris 4064.4 and Harris AN9614 as independent references from Snell, one of ordinary skill in the art at the time the invention was made would have been motivated and found it obvious and straightforward to use Harris 4064.4' s teachings of modulating the preamble and header portions of a data packet using DBPSK modulation and modulating the payload portion of the data packet using DBPSK or DQPSK modulation (as indicated by the SIGNAL field in the header portion) to advantageously provide for switching between DBPSK and DQPSK modulation types in implementing an IEEE 802.11 system *(see* Harris 4064.4 at 1, 3) such as disclosed in Snell. Harris 4064.4 is incorporated by reference into Snell (Snell at 5: 13-17), both references are directed to the PRISM chipset and HSP 3824 baseband processor (Harris 4064.4 at l; Snell at 1:47-63, 5:8-17,5 :31-33), and Harris 4064.4 is a publication of Harris Corporation, the same original assignee of Snell.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Harris 4064.4 with the teachings of Snell, in light of the foregoing including Snell's express direction to apply the teachings of Harris 4064.4, and further because, in combination, each element (Harris 4064.4's teaching of modulating

the preamble and header portions of a data packet using DBPSK modulation and modulating the payload portion of the data packet using DBPSK or DQPSK modulation and Snell's communication system for transmitting data packets modulated using different modulation methods) performs the same function as it would separately, yielding nothing more than predictable results. *KSR,* 550 U.S. at 417. One of ordinary skill in the art would have thus recognized that this combination (yielding the claimed limitation) would have worked as expected and for these reasons, would have been motivated and found it obvious and straightforward to use Harris 4064.4's teachings in implementing Snell's communication system.

One of ordinary skill in the art would have additionally been motivated and found it obvious and straightforward to use Harris AN9614's teaching of a polled (master/slave) protocol in implementing the communication system taught by Snell (in light of Harris 4064.4). Harris AN96l 4 is incorporated by reference into Snell (Snell at 5 :2-7), both references are directed to the PRISM chipset and HSP 3824 baseband processor (Harris AN9614 at 1, 2; Snell at 1:47-63, 5:8-17, 5:31-33), and Harris AN9614 is a publication of Harris Corporation, the same original assignee of Snell. Moreover, AN9614 expressly teaches that it is beneficial to use a polled (master/slave) protocol because "the average power consumption of the radio can be reduced by more than an order of magnitude while meeting all data transfer objectives." Harris AN9614 at 3.

Polling (master/slave) enables this reduction in power consumption because "the system can be set at its sleep mode most of the time to achieve low power consumption. It only needs to operate at full power consumption during the transmission of a packet or during the expected window for received packets." Harris AN9614 at 3. In addition to Snell's express suggestion to apply Harris AN9614's disclosures, one of ordinary skill in the art would have been motivated to use Harris AN9614's teaching of a polled (master/slave) protocol in implementing Snell's communication system (implemented in light of Harris 4064.4, *see supra)* because a polled (master/slave) communication system advantageously provides a simple protocol that has good determinacy *(e.g.,* a reduction in collisions). It would have been routine for one of ordinary skill in the art to use a polled (master/slave) protocol in implementing Snell's communication system (as implemented in light of Harris 4064.4), as master/slave communication systems were common and well-known in the art *(see* '228 patent at 3: 64- 5:7), and thus implementing a polled (master/slave) protocol in Snell's transceiver (which serves as an access point to support communications with multiple other transceivers - Snell at I :34-46) would involve nothing more than using common and known techniques to improve a similar system in the same way to yield predictable results. *KSR,* 550 U.S. at 416. One of ordinary skill in the art would have thus recognized that this combination (yielding the claimed limitation) would have worked as expected. For these reasons, one of ordinary skill in the art would have been motivated and found it obvious and straightforward to implement a polled (master/slave) protocol in implementing Snell's system (as implemented in light of Harris 4064.4).

wherein the first message comprises:
first information modulated according to a first modulation method,

Snell discloses that the master transceiver transmits a first message (PLCP header and PLCP preamble, figure 3 annotated below) which comprises first information modulated according to a first modulation method (BPSK), *See, e.g.,* **Snell at Abstract, 1:34-46, 1:47-50, 1:55-57, 1:58-61, 2:27-30, 2:56-59, 2:61-3:5, 4:42-47, 5:18-2, 6:35-36, 6:52-59, 6:64-66, 7:1-2, 7:5-14,** 7:6- **8, Figs. 2, 3; Harris AN9614 at 3; Harris 4064.4 at 14, 15, 16, Fig. 10.**

second information, including a payload portion, modulated according to the first modulation method,

Snell discloses that the master transceiver transmits second information, including a payload portion (MPDU, figure 3), modulated according to the first modulation method (BPSK), *See, e.g.,* **Snell at Abstract, 1:34-46, 1:47-50, 1:55-57, 1:58-61, 2:27-30, 2:56-59, 2:61-3:5, 4:42-47, 5:18-2, 6:35-36, 6:52-59, 6:64-66, 7:1-2, 7:5-14,** 7:6- **8, Figs. 2, 3; Harris AN9614 at 3; Harris 4064.4 at 14, 15, 16, Fig. 10.**

wherein the second information comprises data intended for one of the one or more slave transceivers and

Snell discloses that the second information (MPDU) comprises data intended for one of the one or more slave transceivers. *See, e.g.,* **Snell at Abstract, 1:34-46, 1:47-50, 1:55-57, 1:58-61, 2:27-30, 2:56-59, 2:61-3:5, 4:42-47, 5:18-2, 6:35-36, 6:52-59, 6:64-66, 7:1-2, 7:5-14,** 7:6- **8, Figs. 2, 3; Harris AN9614 at 3; Harris 4064.4 at 14, 15, 16, Fig. 10.**

With reference to Figure 3 (annotated below) which depicts a message from the master transceiver, a first message includes a PLCP header and PLCP preamble, the MPDU corresponds to second information which is transmitted to the respective slave transceiver.

Snell discloses the transceiver transmitting a "first message" comprising "first information" *(e.g.,* PLCP preamble and PLCP header) "modulated according to a first modulation method" *(e.g.,* BPSK) and "second information, including a payload portion" *(e.g.,* MPDU data) "modulated according to the first modulation method" *(e.g.,* BPSK) (as depicted in Figure 3 below). Snell alternatively discloses modulating the "first information" *(e.g.,* PLCP preamble and PLCP header) and "second information, including a payload portion" *(e.g.,* MPDU data) according to DBPSK which also is a "first modulation method."

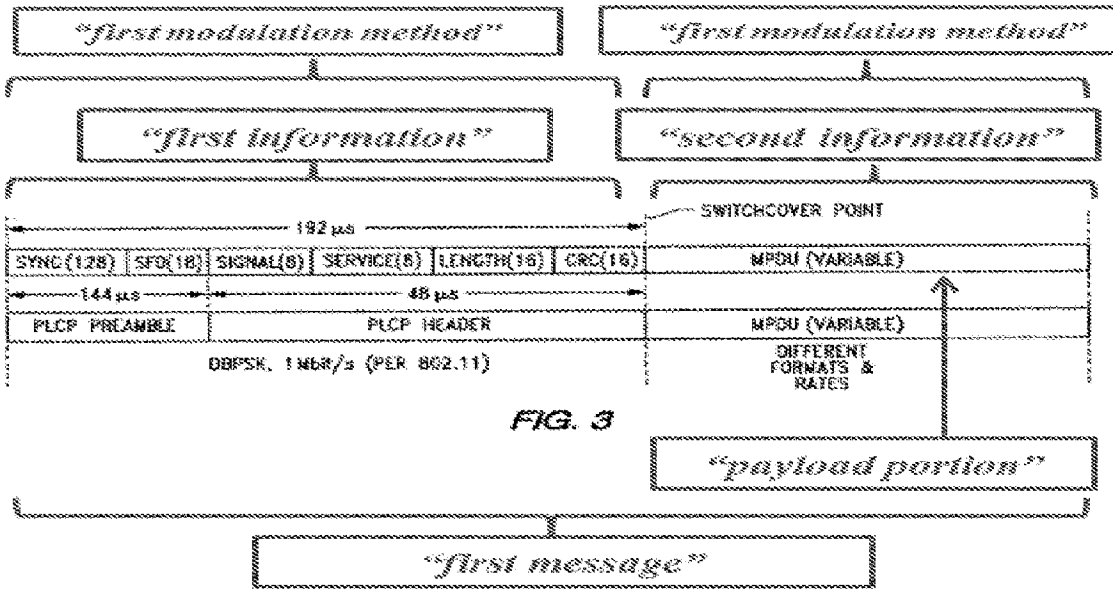

FIG. 3

Snell at Fig. 3 (annotated).

"The ***header may always be BPSK.***" Snell at 6:35-36.

Snell discloses that the "**SIGNAL" in the PLCP header indicates** (*e.g.*, using "OAh") the **modulation type** (*e.g.*, BPSK) **used for modulating the MPDU data portion.**

"Now relating to the PLCP header 91, the SIGNAL is:

0Ah	1 Mbit/s BPSK,
14h	2 Mbit/S QPSK,
37h	5.5 Mbit/s BPSK, and
6Eh	11 Mbit/s QPSK.

"

Snell at 6:52-59.

"SIGNAL is indicated by 2 control bits and then formatted as described." Snell at 7:1-2.

"MPDU is serially provided by Interface 80 and is the variable data scrambled for normal operation. The reference phase for the first symbol of the MPDU is the output phase of the last symbol of the header for Diff Encoding. The last symbol of the header into the scrambler 51 must be followed by the first bit of the MPDU. The **variable data may be modulated and demodulated in different formats than the header portion to thereby increase the data rate,** and while a switchover as indicated by the switchover point in FIG. 3, occurs on-the-fly." Snell at 7:5-14.

"The modulator preferably comprises means for *operating in one of a biphase PSK (BPSK) modulation mode at a first data rate defining a first format,* and a quadrature PSK (QPSK) mode at a second data rate defining a second format." Snell at 2:56-59.

"In particular, the HSP3824 baseband processor manufactured by Harris Corporation *employs quadrature or bi-phase phase shift keying (QPSK or BPSK) modulation schemes."* Snell at 1:58-61.

See also, e.g., Snell at Abstract ("The modulator and demodulator are each preferably operable *in one of a bi-phase PSK (BPSK) mode* at a first data rate and *a quadrature PSK (QPSK) mode* at a second data rate. These formats may also be switched on-the-fly in the demodulator."), 2: 15-17 ("**Moreover, a WLAN application, for example, may require a change between *BPSK and QPSK* during operation,** that is, on-the-fly.").

*"**The PLCP preamble and PLCP header are always** **at 1 Mbit/s, *Diff encoded,*** scrambled and spread with an 11 chip barker." Snell at 6:64-66.

"The modulator may also preferably include header modulator means for modulating data packets to include *a header at a predetermined modulation and a third data rate defining a third format .... The third format is preferably differential BPSK."* Snell at 2:61-3:5. "The reference phase for the first symbol of the *MPDU* is the output phase of the last symbol of the header/or *Diff Encoding."* Snell at 7:6-8.

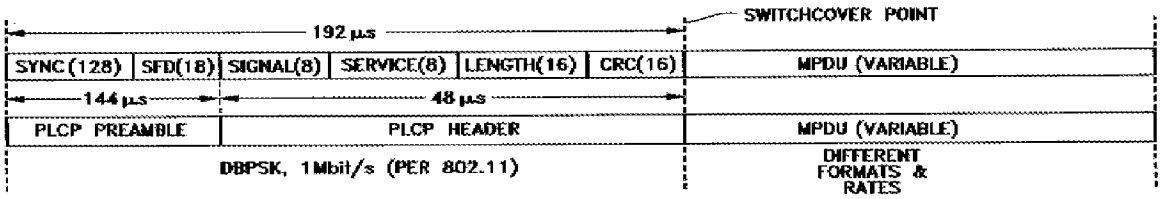

FIG. 3

Snell Figure 3

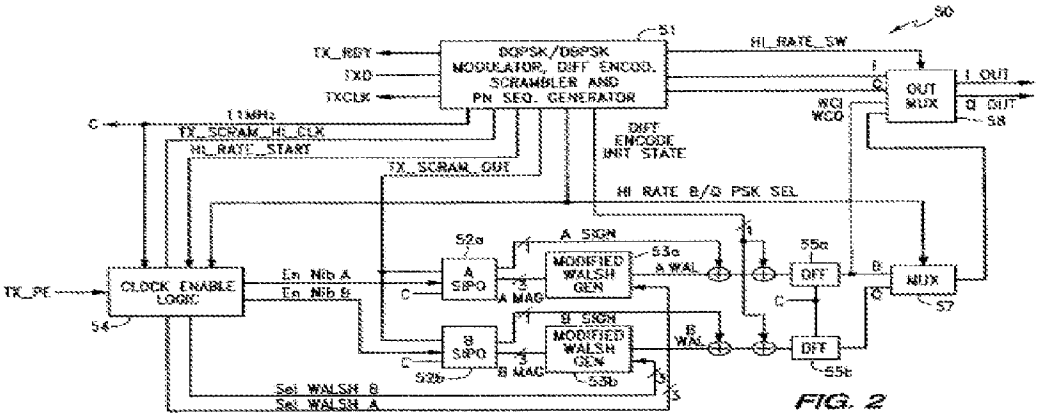

FIG. 2

Snell Figure 2

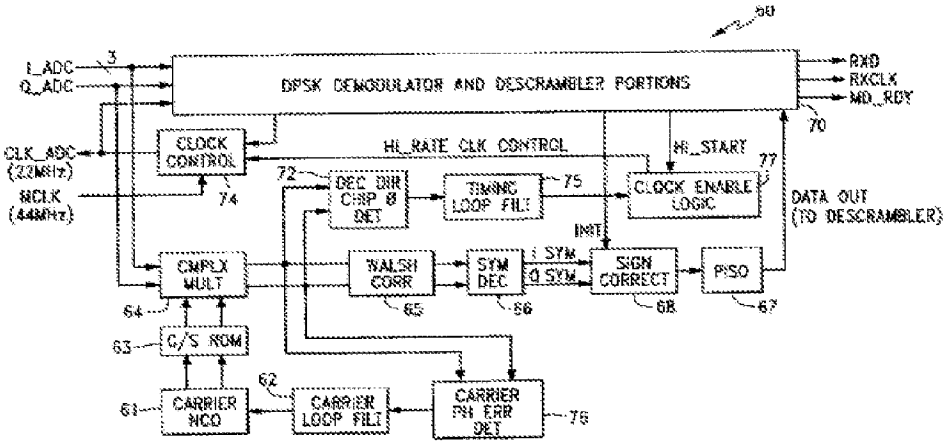

FIG. 5

Snell Figure 5

Snell incorporates by reference Harris 4064.4,[6] which teaches:
"The preamble and header are always transmitted as DBPSK waveforms while the ***data packets can be configured to be either DBPSK* or DQPSK**." Harris 4064.4 at 14.

"The *preamble is always transmitted as a DBPSK* waveform with a programmable length of up to 256 symbols long." Harris 4064.4 at 15.

[6] Snell expressly incorporates by reference "the entire disclosure" of Harris 4064.4 (Snell at 5:8-17, 5:31-33). *See Harari v. Lee,* 656 F.3d 1331, 1335-36 (Fed. Cir. 2011) ("the entire '579 application disclosure was incorporated by the broad and unequivocal language: 'The disclosures of the two applications are hereby incorporate[d] by reference."'); *see also Advanced Display Sys., Inc. v. Kent State Univ.,* 212 F.3d 1272, 1282 (Fed.Cir.2000) ("material not explicitly contained in the single, prior art document may still be considered for purposes of anticipation if that material is incorporated by reference into the document.").

"Signal Field (8 Bits) - This field indicates whether the data packet that follows the header is modulated as DBPSK or DQPSK. In mode 3 the HSP3824 receiver looks at the signal field to determine whether it needs to switch from DBPSK demodulation into DQPSK demodulation at the end of the always DBPSK preamble and header fields." Harris 4064.4 at 15.

"Mode 3 - In this mode the preamble is programmable up to 256 bits (all l's). The header in this mode is using all available fields. *In mode 3 the signal field defines the modulation type of the data packet (DBPSK* or DQPSK) so the receiver does not need to be preprogrammed to anticipate one or the other. In this mode the device checks the Signal field for the data packet modulation and it switches to DQPSK if it is defined as such in the signal field. *Note that the preamble and header are always DBPSK* the modulation definition applies only for the data packet." Harris 4064.4 at 16.

See also, e.g., Harris 4064.4 at 14 ("The HSP3824 transmitter is designed as a Direct [7] Sequence Spread Spectrum DBPSK/DQPSK modulator."), Harris 4064.4 at 14 ("The modulator is capable of switching rate automatically in the case where the preamble and header information are DBPSK modulated, and the data is DQPSK modulated."), Harris 4064.4 at FIGURE 10.

first message address information that is indicative of the one of the one or more slave transceivers being an intended destination of the second information; and

Snell does not expressly disclose *the first message comprises first message address information that is indicative of the one of the one or more slave transceivers being an intended destination of the second information.*

Yamano teaches that packets can be advantageously addressed for an intended destination.
Yamano discloses transmitting a "first message" *(e.g.,* data packet including a preamble and main body) that includes "first message address information that is indicative" *(e.g.,* "destination address" in the preamble) of the transceiver that is the "intended destination of the second information."

"Packet 700 includes a *preamble 701* and a *main body 702."* Yamano at 19:63-64.

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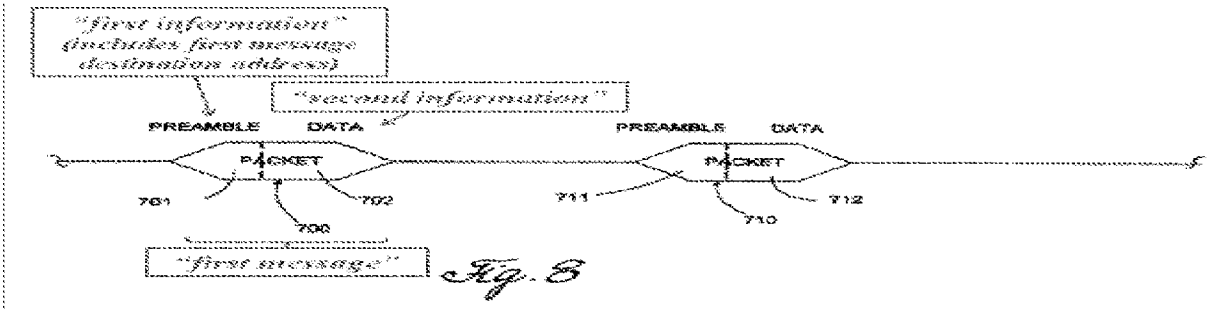
[7] Snell expressly incorporates by reference "the entire disclosure" of Harris 4064.4 (Snell at 5:8-17, 5:31-33). *See Harari v. Lee,* 656 F.3d 1331, 1335-36 (Fed. Cir. 2011) ("the entire '579 application disclosure was incorporated by the broad and unequivocal language: 'The disclosures of the two applications are hereby incorporate[d] by reference."'); *see also Advanced Display Sys., Inc. v. Kent State Univ.,* 212 F.3d 1272, 1282 (Fed.Cir.2000) ("material not explicitly contained in the single, prior art document may still be considered for purposes of anticipation if that material is incorporated by reference into the document.").

"For example, *preamble 701* can include information which identifies: (1) a version or type field for the preamble, (2) ***packet source and destination addresses,*** (3) the line code (i.e., the modem protocol being used), (4) the data rate, (5) error control parameters, (6) packet length and (7) a timing value for the expected reception slot of a subsequent packet." Yamano at 20:1-7.

Yamano also discloses that the preamble precedes the main body (containing data), as shown in Figure 8. Yamano teaches that the first message comprises first message address information that is indicative of the one of the one or more slave transceivers being an intended destination of the second information. *See, e.g.,* Yamano at 19:63-64, 20:1-7, 20:54-59, Fig. 8.



Yamano at Fig. 8 (annotated).

Snell and Yamano are in the same field of art, with both relating to transmitting data packets over a network *(see, e.g.,* Snell at 1:55-58, 2:61-63, 2:66-3:3, 5:18-21, 6:48-63, Fig. 3; Yamano at 1: 1-29, 19:54-20:33, Fig. 8), at varying rates *(see, e.g.,* Snell at 2: 15-17, 6:52-59; Yamano at 19:54-56). Yamano expressly teaches that including a destination address in the preamble portion of the data packet, which precedes the data portion, will advantageously reduce processing requirements of receiving devices because the receiving device can filter out packets which it does not need to demodulate. Yamano at 20:54-59 ("When the preamble in a burst-mode packet *includes the destination address of the packet,* the receiver circuits can monitor the destination address of the packet, and in response, filter packets which do not need to be demodulated, thereby reducing the processing requirements of the receiver circuits.").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Yamano' s teaching of including a destination address in the preamble portion of a data packet in implementing Snell's data packet implemented in light of Harris 4064.4 and Harris AN9614 comprising preamble, header, and MPDU data portions to advantageously specify which receiver the data is intended for and to beneficially reduce the processing requirements at the receiving device, as taught by Yamano. "When the preamble in a burst-mode packet *includes the destination address of the packet,* the receiver circuits can monitor the destination address of the packet, and in

response, filter packets which do not need to be demodulated, thereby reducing the processing requirements of the receiver circuits." Yamano at 20:54-59.

In addition, Snell teaches structuring its data packet to include a preamble, header, and MPDU data portion *(see, e.g.,* Snell at 6:35-36, 6:64-66, 7:5-14, Fig. 3), and Yamano teaches structuring its data packet to also include a preamble and data portion, and to place the destination address in the preamble portion (Yamano at 19:63-20:7, Fig. 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a destination address in the preamble portion of a data packet, as taught by Yamano, in implementing Snell's system implemented in light of Harris 4064.4 and Harris AN9614 for transmitting data packets between transceivers, as Snell teaches that its data packet already includes a preamble portion-and in combination, each element (Yamano' s teaching of placing a destination address in the preamble and Snell's teaching of a system for communicating data packets modulated according to different modulation methods between transceivers) performs the same function as it would separately, yielding nothing more than predictable results. *KSR Int'l Co. v. Teleflex Inc.,* 550 U.S. 398, 417 (2007). One of ordinary skill in art at the time the invention was made would have thus recognized that this combination (yielding the claimed limitation) would have worked as expected. For these reasons, a person of ordinary skill would have been motivated and found it obvious and straightforward to use the teachings of Yamano including a destination address in the preamble of a data packet in implementing Snell's communication system.

Snell in view of Harris 4064.4, in further view of Harris AN9614 and further in view of Yamano thus teach that the first message comprises first message address information that is indicative of the one of the one or more slave transceivers being an intended destination of the second information. *See, e.g.,* Snell at 6:35-36, 6:64-66, 7:5-10, Fig. 3; Harris 4064.4 at 14; Yamano at 19:63-64, 20:1-7, 20:54-59, Fig. 8.

said master transceiver configured to transmit a second message over the communication medium from the master transceiver to the one or more slave transceivers wherein the second message comprises:

third information modulated according to the first modulation method,
wherein the third information comprises information that is indicative of an impending change in modulation to a second modulation method, and

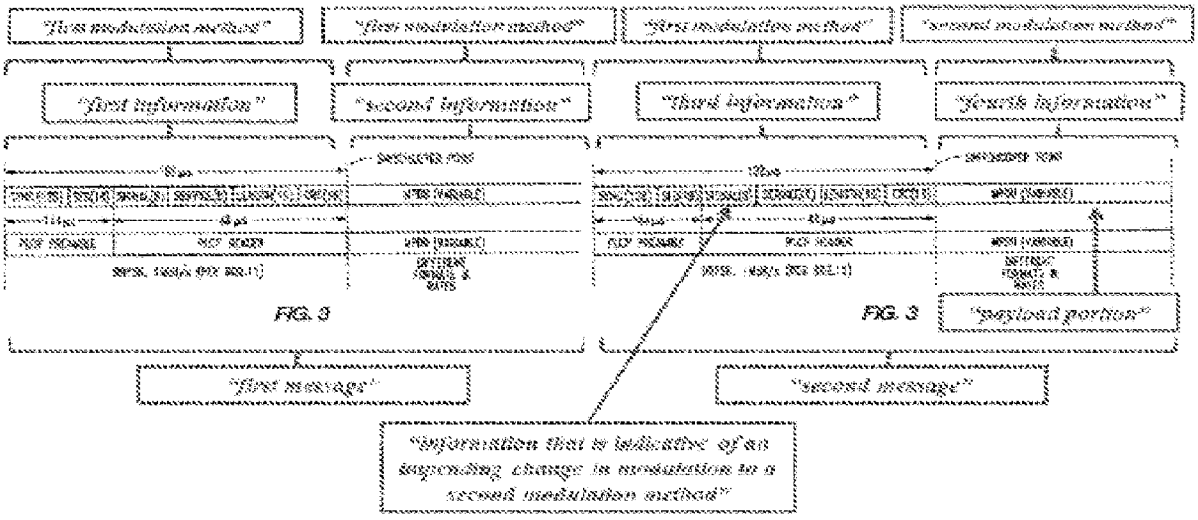
fourth information, including a payload portion, transmitted after transmission of the third information,
the fourth information being modulated according to the second modulation method,
the second modulation method being of a different type than the first modulation method,

wherein the fourth information comprises data intended for a single slave transceiver of the one or more slave transceivers, and

As noted above, Snell discloses that the transceiver transmits data packets to multiple different end user slave transceivers, as such multiple messages of format shown in figure 3 are provided to the slave transceivers and where the communication may switch on-the-fly between a "first modulation method" *(e.g.,* BPSK) and a "second modulation method" *(e.g.,* QPSK) that is "of a different type than the first modulation method." **Snell thus teaches transmitting a "first message" and a "second message" as shown in annotated Figure 3 below.** *See, e.g.,* Snell at 1:34-46, 1:47-50, 1:55-57, 2:27-30, 2:61-3:5, 4:42-47, 5:18-2, 6:35-36, 6:52-59, 6:64-66, 7:1-2, 7:5-14, Fi s. 2, 3, 5; Harris AN9614 at 3; Harris 4064.4 at**14-16, Fig. 10**

For example, Snell discloses a "transceiver" that serves as an access point for communicating "data intended for a [transceiver]" connected to a wireless local area network (WLAN). *See* claim 1 preamble.

Snell also discloses that the transceiver transmits data packets to another transceiver, where the communication may switch on-the-fly between a "first modulation method" *(e.g.,* BPSK) and a "second modulation method" *(e.g.,* QPSK) that is "of a different type than the first modulation method." Snell thus teaches transmitting a "first message" and a "second message" as shown in annotated Figure 3 below.



Snell Figure 3 Annotated (page 54 Request)

Snell teaches communicating multiple data packets with the ability to "switch on-the-fly between different data rates and/or formats" as noted above, based on this disclosure, a person of ordinary skill in the art would have understood that Snell teaches that a series of packets may be sent that switch from using a first modulation method to using a second modulation method for the payload portion of the data packet. For example, the "first message" in Snell comprises "first information" *(e.g.,* PLCP preamble and PLCP

header) that is "modulated according to a first modulation method" *(e.g.,* BPSK) where the "first information" *(e.g.,* "SIGNAL" field in PLCP header) indicates *(e.g.,* using "OAh") the modulation type *(e.g.,* BPSK) used for modulating "second information" *(e.g.,* MPDU data). In the "first message," the "SIGNAL" field in the PLCP header uses a code *(e.g.,* "OAh") that indicates that the "second information" *(e.g.,* MPDU data) is modulated "according to the first modulation method" *(e.g.,* BPSK at 1 Mbit/s).

Snell's transceiver can transmit a "second message" comprising "third information" *(e.g.,* PLCP preamble and PLCP header) "modulated according to the first modulation method" *(e.g.,* BPSK) where the "third information comprises information" *(e.g.,* "SIGNAL" field in PLCP header) "that is indicative of an impending change in modulation" *(e.g.,* using "l 4h") "to a second modulation method" *(e.g.,* QPSK) used for modulating "fourth information." For example, in the "second message," the "SIGNAL" field in the PLCP header uses a code *(e.g.,* "14h") that indicates that the "fourth information" *(e.g.,* MPDU data) is modulated "according to the second modulation method" *(e.g.,* QPSK at 2 Mbit/s), wherein the "second modulation method" is of a "different type than the first modulation method." This "SIGNAL" is "indicative of an impending change" from the "first modulation method" to the "second modulation method" because it is indicating a change from, for example, QPSK modulation to BPSK modulation. In addition, transmitting the data using the "second modulation method"- QPSK-results in a data rate of 2 Mbit/s which is higher than transmitting the data using the "first modulation method " BPSK at 1 Mbit/s.

"The modulator may also preferably include header modulator means for modulating *data packets."* Snell at 2:61-63.

"The PRISM 1 chip set provides all the functions necessary for full or half duplex, direct sequence spread spectrum, *packet communications* at the 2.4 to 2.5 GHz ISM radio band." Snell at 1:55-57.

"It is another object of the invention to provide a spread spectrum transceiver and associated method to permit operation at higher data rates and *which may switch on-the-fly between different data rates and/or formats."* Snell at 2:27-30.

"The variable data may be modulated and demodulated in different formats than the header portion to thereby increase the data rate, and *while a switchover as indicated by the switchover point in FIG. 3, occurs on-the-fly."* Snell at 7: 10-14.

"The *header* may always be *BPSK."* Snell at 6:35-36.

"Now relating to the *PLCP header* 91, *the SIGNAL* is:

0Ah	1 Mbit/s BPSK,
14h	2 Mbit/S QPSK,
37h	5.5 Mbit/s BPSK, and
6Eh	11 Mbit/s QPSK.

"

SIGNAL is indicated by 2 control bits and then formatted as described." Snell at 7:1-2.

"MPDU is serially provided by Interface 80 and *is the variable data* scrambled for normal operation. The reference phase for the first symbol of the MPDU is the output phase of the last symbol of the header for Diff Encoding. The last symbol of the header into the scrambler 51 must be followed by the first bit of the MPDU. *The variable data may be modulated and demodulated in different formats* than the header portion to thereby increase the data rate, and while a switchover as indicated by the switchover point in FIG. 3, occurs on-the-fly." Snell at 7:5-14.

Snell describes that the "first modulation method" may be BPSK and the "second modulation method" may be QPSK, which is of a different "type" than the first modulation method, and alternatively describes that the "first modulation method" may be differential BPSK ("DBPSK") and that the "second modulation method" may be differential QPSK ("DQPSK"), which is also of a different "type" than the first modulation method.

Thus, Snell alternatively describes modulating the "first information" *(e.g.,* PLCP preamble and PLCP header) according to a "first modulation method" *(e.g.,* DBPSK) and "second information" *(e.g.,* MPDU data) according to either a "first modulation method" *(e.g.,* DBPSK) or "second modulation method" *(e.g.,* QBPSK).

"The PLCP preamble and PLCP header are always at 1 Mbit/s, *Diff encoded,* scrambled and spread with an 11 chip barker." Snell at 6:64-66.

"The modulator may also preferably include header modulator means for modulating data packets to include *a header at a predetermined modulation and a third data rate defining a third format .... The third format is preferably differential BPSK."* Snell at 2:61-3:5.

"The reference phase for the first symbol of the *MPDU* is the output phase of the last symbol of the header/or *Diff Encoding."* Snell at 7:6-8. *See also, e.g.,* Snell at Figs. 2, 3, 5.

Snell incorporates by reference Harris 4064.4, 17 which discloses: *"The preamble and header are always transmitted as DBPSK* waveforms while the *data packets can be configured to be either DBPSK or DQPSK."* Harris 4064.4 at 14.

"The *preamble is always transmitted as a DBPSK* waveform with a programmable length of up to 256 symbols long." Harris 4064.4 at 15.

"Signal Field (8 Bits) - This field indicates whether the data packet that follows the header is modulated as DBPSK or DQPSK. In mode 3 the HSP3824 receiver looks at the signal field to determine whether it needs to switch from DBPSK demodulation into DQPSK demodulation at the end of the always DBPSK preamble and header fields." Harris 4064.4 at 15.

"Mode 3 - In this mode the preamble is programmable up to 256 bits (all l's). The header in this mode is using all available fields. *In mode 3 the signal field defines the modulation type of the data packet (DBPSK* or *DQPSK)* so the receiver does not need to be preprogrammed to anticipate one or the other. In this mode the device checks the Signal field for the data packet modulation and it switches to DQPSK if it is defined as such in the signal field. *Note that the preamble and header are always DBPSK* the modulation definition applies only for the data packet." Harris 4064.4 at 16.

See also, e.g., Harris 4064.4 at 14 ("The HSP3824 transmitter is designed as a Direct Sequence Spread Spectrum *DBPSKIDQPSK* modulator."), Harris 4064.4 at 14 ("The modulator is capable of switching rate automatically in the case where the preamble and header information are DBPSK modulated, and the data is *DQPSK* modulated."), Harris 4064.4 at FIGURE 10.

Kamerman *discloses transmitting a first message including second information modulated at a first modulation method and transmitting a second message including fourth information modulated at a second modulation method.* *See, e.g.,* **Kamerman at 6, 11, 12.**

For example, Kamerman discloses an automatic rate selection scheme for falling forward from a "first modulation method" *(e.g.,* BPSK) corresponding to a lower data rate *(e.g.,* 1 Mbit/s) to a "second modulation method" *(e.g.,* QPSK) corresponding to a higher data rate *(e.g.,* 2 Mbit/s) after a number of successive correctly acknowledge packet transmissions, for instance, where there is a low load in neighbor cells and a reliable connection.

"Then there is looked to *automatic rate control* to keep the co-channel interference at a tolerable level." Kamerman at 6.

"IEEE 802.11 DS specifies bit rates of 1 and 2 Mbps. The allowable SNR and CSIR values for reliable transmission of data packets are dependent on the bit rate." Kamerman at 11.

"IEEE 802.11 DS specifies BPSK and QPSK, in addition there could be applied proprietary modes with M-PSK and QAM schemes that provide higher bit rates by encoding more bits per symbol. ... An automatic rate selection scheme based on the reliability of the individual uplink and downlink could be applied. The basic rate adaptation scheme could be: after unacknowledged packet transmissions the rate falls back, and *after a number (e.g. JO) of successive correctly acknowledged packet transmissions the bit rate goes up."* Kamerman at 11.

"At lower load in the neighbor cells the highest bit rate can be used more often. At higher load the transmissions from the access point to stations at the outer part of the cells, will be done often at fall back rates due to mutilation of transmissions by interference. In practice the network load for LANs at nowadays client-server applications is very bursty, with sometimes transmission bursts over an individual links and low activity during the major part of the time. *Therefore the higher bit rate can be used during the most of the time, and at high load in the neighbor cells (as will evoked by test applications) there will be switched to fall back rates in the outer part of the cell."* Kamerman at 11.

"The application of proprietary bit rates of 3 and 4 Mbps in addition to the basic 1 and 2 Mbps, can be combined with an automatic rate selection. This automatic rate selection *gives fall forward at reliable connections* and fall back at strong co-channel interference." Kamerman at 12

It was well-known in the art, as demonstrated by Kamerman, to transmit a first data packet where the data is modulated using a first modulation method, such as BPSK (corresponding to a lower data transfer rate), and to next transmit a second data packet where the data is modulated using a second modulation method, such as QPSK (corresponding to a higher data transfer rate).

One of ordinary skill in the art at the time the invention was made would have been motivated and found it obvious and straight forward to use **Kamerman**'s teaching of transmitting a first data packet where the data is modulated using a first modulation method and next transmitting a second data packet where the data is modulated using a second modulation method in implementing Snell's system for communicating data packets modulated according to different modulation methods (modified by the teaching of Yamano, as discussed above) to advantageously maximize the data transfer rate and adapt to changing channel conditions (as also taught by Kamerman). In particular, Kamerman expressly teaches that it is beneficial to transmit the data of a first data packet using a first modulation method corresponding to a lower data transfer rate *(e.g.,* BPSK modulation at 1 mbps) during higher load conditions when a more robust signal is needed due to "mutilation of transmissions by interference," and to next transmit the data of a second data packet using a second modulation method corresponding to a higher data transfer rate *(e.g.,* QPSK modulation at 2 mbps) *(i.e.,* falling forward) to maximize the data transfer rate during lower load conditions when the connection is more reliable. *See*

Kamerman at 6 ("Then there is looked to *automatic rate control* to keep the co-channel interference at a tolerable level."), 11 ("The basic rate adaptation scheme could be: after unacknowledged packet transmissions the rate falls back, and *after a number (e.g. 10) of successive correctly acknowledged packet transmissions the bit rate goes up."),* 11 *("At lower load in the neighbor cells the highest bit rate can be used more often.* At higher load the transmissions from the access point to stations at the outer part of the cells, will be done at fallback rates due to mutilation of transmissions by interference. In practice the network load for LANs at nowadays client-server applications is very bursty, with sometimes transmission bursts over an individual links and low activity during the major part of the time. Therefore the higher bit rate can be used during the most of the time, and at high load in the neighbor cells ... there will be switched to fall back rates in the outer part of the cell."), 12 ("This automatic rate selection gives fall forward at reliable connections and fall back at strong co-channel interference. Therefore it gives adaptation of the bit rate to the interference as it occurs in time depending on positions as load.").

Moreover, Snell and Kamerman are in the same field of art, with both relating to communications between transceivers that use BPSK and QPSK modulation methods to transfer data at different rates according to the draft IEEE 802.11 standard available at that time. *See, e.g.,* Snell at 1:47-63 ("The assignee of the present invention has developed and manufactured a set of integrated circuits for a WLAN under the mark PRISM 1 *which is compatible with the proposed IEEE 802.11 standard .... "),* 5:31-33 ("The present invention provides an extension of the PRISM 1 product from 1 *Mbit/s BPSK and 2 Mbit/s QPSK .. . "*); Kamerman at 6 ("This paper considers the critical parameters for *wireless LANs that operate conform to the IEEE 802.11 DSSS (direct sequence spread spectrum) standard ... "),* 11 ("IEEE 802.11 DS specifies bit rates of 1 and 2 Mbps.", 11 ("IEEE 802.11 DS specifies BPSK and QPSK ... ").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Kamerman' s teaching of transmitting a first data packet where the data is modulated using a first modulation method and next transmitting a second data packet where the data is modulated using a second modulation method in implementing Snell's system (modified in light of Yamano) for communicating data packets modulated according to different modulation methods, as both Snell and Kamerman are directed to IEEE 802.11 systems utilizing BPSK and QPSK modulation corresponding, respectively, to a lower and higher data transfer rates-and in combination, each element (Kamerman's teaching of transmitting a first data packet where the data is modulated using a first modulation method and next transmitting a second data packet where the data is modulated using a second modulation method and Snell's system for communicating data packets modulated according to different modulation methods) performs the same function as it would separately, yielding nothing more than predictable results. *KSR,* 550 U.S. at 417. One of ordinary skill in the art would have thus recognized that this combination (yielding the claimed limitation) would have worked as expected and would have been motivated and found it obvious and straightforward to use Kamerman' s

teaching of transmitting a first data packet where the data is modulated using a first modulation method and next transmitting a second data packet where the data is modulated using a second modulation method in implementing Snell's system (modified in light of Yamano) for communicating data packets modulated according to different modulation methods.

second message address information that is indicative of the single slave transceiver being an intended destination of the fourth information; and

Snell in view of Yamano discloses that the second message comprises second message address information that is indicative of the single slave transceiver being an intended destination of the fourth information. *See, e.g.,* Snell at 1:55-57, 2:61-63, 6:35-36, 6:64-66, 7:5-14, Fig. 3; Harris 4064.4 at 14; Yamano at 19:63-64, 20:1-7, 20:54-59, Fig. 8.

For example, Snell discloses transmitting a "second message" including a PLCP preamble and PLCP header, and MPDU data, as shown in Figure 3 below.

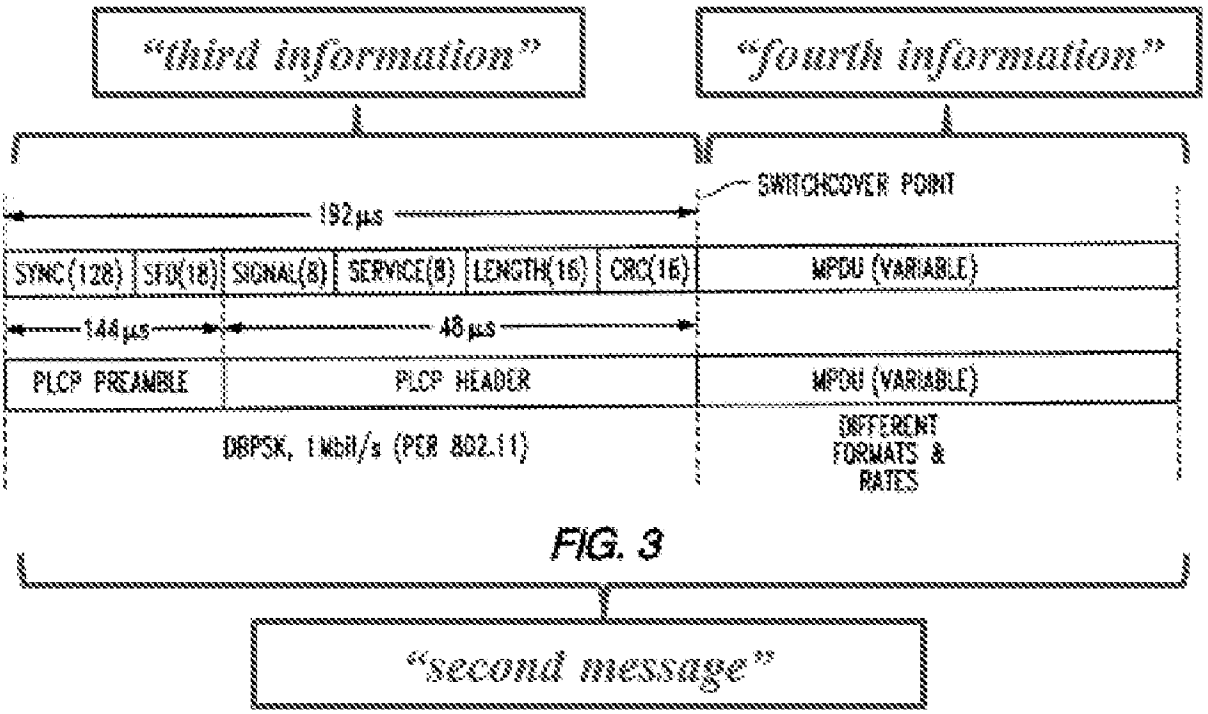


FIG. 3

Snell at Fig. 3 (annotated).

"The modulator may also preferably include header modulator means for modulating *data packets*" Snell at 2:61-63.

"The PRISM 1 chip set provides all the functions necessary for full or half duplex, direct sequence spread spectrum, *packet communications* at the 2.4 to 2.5 GHz ISM radio band." Snell at 1:55-57.

"The *header* may always be BPSK." Snell at 6:35-36.

"The *PLCP preamble and PLCP header* are always at 1 Mbit/s, Diff encoded, scrambled and spread with an 11 chip barker." Snell at 6:64-66.

"*MPDU* is serially provided by Interface 80 and *is the variable data* scrambled for normal operation. The reference phase for the first symbol of the MPDU is the output phase of the last symbol of the header for Diff Encoding. The last symbol of the header into the scrambler 51 must be followed by the first bit of the MPDU. *The variable data* may be modulated and demodulated in different formats than the header portion to thereby increase the data rate, and while a switchover as indicated by the switchover point in FIG. 3, occurs on-the-fly." Snell at 7:5-14.

Snell incorporates by reference Harris 4064.4,[19] which discloses:

"The *preamble and header* are always transmitted as DBPSK waveforms while the *data packets* can be configured to be either DBPSK or DQPSK." Harris 4064.4 at 14.

Yamano discloses that the second message comprises second message address information that is indicative of the single slave transceiver being an intended destination of the fourth information. *See, e.g.,* Yamano at 19:63-64, 20:1-7, 20:54-59, Fig. 8.

For example, Yamano discloses that a packet includes a preamble and main body, and that the preamble can include a destination address.

"Packet 700 includes a *preamble 701* and a *main body 702."* Yamano at 19:63-64.

"For example, *preamble 701* can include information which identifies: (1) a version or type field for the preamble, (2) *packet source and destination addresses,* (3) the line code (i.e., the modem protocol being used), (4) the data rate, (5) error control parameters, (6) packet length and (7) a timing value for the expected reception slot of a subsequent packet." Yamano at 20:1-7 (emphasis added).

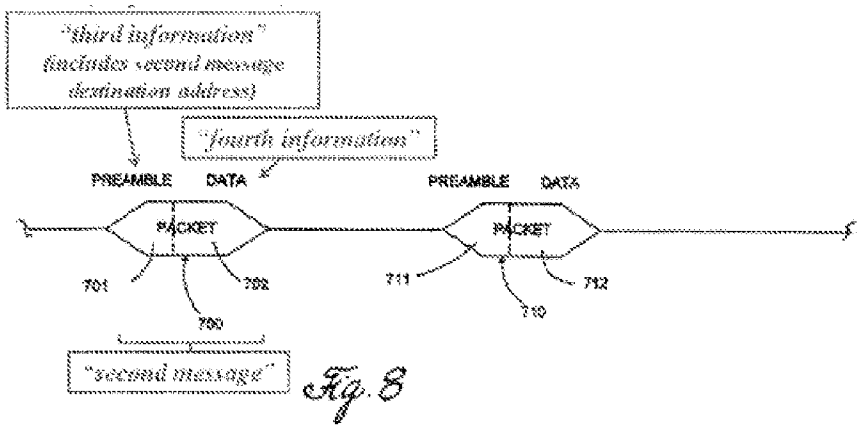


Fig. 8

Yamano at Figure 8 (annotated).

"When the preamble in a burst-mode packet *includes the destination address of the packet,* the receiver circuits can monitor the destination address of the packet, and in response, filter packets which do not need to be demodulated, thereby reducing the processing requirements of the receiver circuits." Yamano at 20:54-59.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Yamano' s teaching of including a destination address in the preamble portion of a data packet in implementing Snell's data packet comprising preamble, header, and MPDU data portions to advantageously specify which receiver the data is intended for and to beneficially reduce the processing requirements at the receiving device, as taught by Yamano. "When the preamble in a burst-mode packet *includes the destination address of the packet,* the receiver circuits can monitor the destination address of the packet, and in response, filter packets which do not need to be demodulated, thereby reducing the processing requirements of the receiver circuits." Yamano at 20:54-59.

In addition, Snell teaches structuring its data packet to include a preamble, header, and MPDU data portion *(see, e.g.,* Snell at 6:35-36, 6:64-66, 7:5-14, Fig. 3), and Yamano teaches structuring its data packet to also include a preamble and data portion, and to place the destination address in the preamble portion (Yamano at 19:63-20:7, Fig. 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a destination address in the preamble portion of a data packet, as taught by Yamano, in implementing Snell's system for transmitting data packets between transceivers, as Snell teaches that its data packet already includes a preamble portion-and in combination, each element (Yamano' s teaching of placing a destination address in the preamble and Snell's teaching of a system for communicating data packets modulated according to different modulation methods between transceivers) performs the same

function as it would separately, yielding nothing more than predictable results. *KSR Int'l Co. v. Teleflex Inc.,* 550 U.S. 398, 417 (2007). One of ordinary skill in art at the time the invention was made would have thus recognized that this combination (yielding the claimed limitation) would have worked as expected. For these reasons, a person of ordinary skill would have been motivated and found it obvious and straightforward to use the teachings of Yamano including a destination address in the preamble of a data packet in implementing Snell's communication system.

wherein the second modulation method results in a higher data rate than the first modulation method.

Snell discloses that the second modulation method results in a higher data rate than the first modulation method. *See, e g.* , Snell at 5:31-33, 6:52-59, 6:64-66, 7:1-2, 7:5-14, Fig. 3; Harris 4064.4 at 16 (Table 7).

For example, Snell discloses that the second modulation method *(e.g.,* QPSK, or alternatively, DQPSK) results in a higher data rate *(e.g.,* 2 Mbit/s) than the first modulation method *(e.g.,* BPSK, or alternatively, DBPSK) which results in a data rate of 1 Mbit/s.
"The present invention provides an extension of the PRISM 1 product from *1 Mbit/s BPSK and 2 Mbit/s QPSK* to 5.5 Mbit/s BPSK and 11 Mbit/s QPSK." Snell at 5:31-33

"The PLCP preamble and PLCP header are always at *1 Mbit/s,* Diff encoded, scrambled and spread with an 11 chip barker." Snell at 6:64-66.

"Now relating to the PLCP header 91, the SIGNAL is:

0Ah	1 Mbit/s BPSK,
14h	2 Mbit/S QPSK,
37h	5.5 Mbit/s BPSK, and
6Eh	11 Mbit/s QPSK.

"

Snell at 6:52-59

"SIGNAL is indicated by 2 control bits and then formatted as described." Snell at 7:1-2.

"MPDU is serially provided by Interface 80 and is the variable data scrambled for normal operation. The reference phase for the first symbol of the MPDU is the output phase of the last symbol of the header for Diff Encoding. The last symbol of the header into the scrambler 51 must be followed by the first bit of the MPDU. The variable data may be modulated and demodulated in different formats than the header portion to thereby increase the data rate, and while a switchover as indicated by the switchover point in FIG. 3, occurs on-the-fly." Snell at 7:5-14. *See also, e.g.,* Snell at Fig. 3; Harris 4064.421 at 16 (Table 7).

21. The master communication device as in claim 1, wherein the first information that is included in the first message comprises the first message address data.

Snell modified in view of Harris 4064.4, in view of Harris AN 9614, in view of Yamano and further in view of Kamerman as recited above disclose that the first information that is included in the first message comprises the first message address as indicated in the rejection of claim 1 above with reference to the first message address of the destination, therefore the first message address data is included in the actual message when transmitted by the master to the slave transceiver.

Yamano expressly teaches that including a destination address in the preamble portion of the data packet, which precedes the data portion, will advantageously reduce processing requirements of receiving devices because the receiving device can filter out packets which it does not need to demodulate. Yamano at 20:54-59 ("When the preamble in a burst-mode packet *includes the destination address of the packet*, the receiver circuits can monitor the destination address of the packet, and in response, filter packets which do not need to be demodulated, thereby reducing the processing requirements of the receiver circuits.").

D.) Claim 21 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Snell in view of Harris 4064.4, further in view of the Admitted Prior Art, further in view of Upender, further in view of Yamano and further in view of Kamerman.

1. A master communication device configured to communicate with one or more slave transceivers according to a master/slave relationship in which a slave communication from a slave device to the master communication device occurs in response to a master communication from the master communication device to the slave device,
the master communication device comprising:
a master transceiver configured to transmit a first message over a communication medium from the master transceiver to the one or more slave transceivers,

Snell discloses a master communication device (transceiver 30) that serves as an access point for communicating data with other transceivers connected to a wireless local area network (WLAN) and is configured to communicate with one or more slave transceivers (end users connect to LAN through transceivers) according to a master/slave relationship in which a slave communication from a slave device to the master communication device occurs in response to a master communication from the master communication device to the slave device. *See, e.g.,* Snell at 1:34-46,1:47-50,1:55-57, 2:27-30, 4:42-47, 5:18-21; Harris AN9614 at 3.

Snell at 4:42-47 ("Referring to FIG. 1, a ***wireless transceiver 30*** in accordance with the invention is first described. The *transceiver 30 may be readily used for WLAN applications* in the 2.4 GHZ ISM band in accordance with the proposed IEEE 802.11 standard. Those of skill in the art will readily recognize other applications for the transceiver 30 as well."

"In a typical WLAN, ***an access point provided by a transceiver*****, that is, a combination transmitter and receiver,** connects to the wired network from a fixed location. Accordingly, the access transceiver receives, buffers, and transmits data between the WLAN and the wired network. *A single access transceiver can support a small group of collocated users within a range of less than about one hundred to several hundred feet. The* ***end users connect to the WLAN through transceivers*** which are typically implemented as PC cards in a notebook computer, or ISA or PCI cards for desktop computers. Of course the transceiver may be integrated with any device, such as a hand-held computer." Snell at 1:34-46.

"Like the HSP3824 baseband processor, the high data rate baseband processor 40 of the invention contains all of the functions necessary for a full or half duplex packet baseband *transceiver*." Snell at 5:18-21.

"The PRISM 1 chip set provides all the functions necessary for full or half duplex, direct sequence spread spectrum *packet communications* at the 2.4 to 2.5 GHz ISM radio band." Snell at 1:55-57.

See also, e.g., Snell at 2:27-30 ("It is another object of the invention to provide *a spread spectrum transceiver* and associated method to permit operation at higher data rates and which may switch on-the-fly between different data rates and/or formats."); Snell at 1:47-50 ("The assignee of the present invention has developed and manufactured a set of integrated circuits for a WLAN under the mark PRISM 1 which is compatible with the proposed IEEE 802.11 standard."); Snell at 4:42-47 ("Referring to FIG. 1, a *wireless transceiver 30* in accordance with the invention is first described. The *transceiver 30 may be readily used for WLAN applications* in the 2.4 GHZ ISM band in accordance with the proposed IEEE 802.11 standard. Those of skill in the art will readily recognize other applications for the transceiver 30 as well."

Snell incorporates by reference Harris AN9614[8], which discloses that the communications between transceivers can operate according to a polled (*i.e.*,

[8] Snell expressly incorporates by reference "the entire disclosure" of Harris AN9614 (Snell at 5:2-7). *See Harari v. Lee,* 656 F.3d 1331, 1335-36 (Fed. Cir. 2011) ("the entire '579 application disclosure was incorporated by the broad and unequivocal language: 'The disclosures of the two applications are hereby incorporate[d] by reference.'"); *see also Advanced Display Sys., Inc. v. Kent State Univ.,* 212 F.3d 1272, 1282 (Fed.Cir.2000) ("material not explicitly contained in the single, prior art document may still be considered for purposes of anticipation if that material is incorporated by reference into the document.").

master/slave) protocol, which is a master/slave communication system.[9] *See e.g.*, Harris AN9614 at 3.

"[T]he controller can keep adequate time to operate either a polled or a time allocated scheme. In these modes, the radio is powered off most of the time and only awakens when communications is expected. This station would be awakened periodically to listen for a beacon transmission. The beacon serves to reset the timing and to alert the radio to traffic. If traffic is waiting, the radio is instructed when to listen and for how long. In **a polled scheme**, the remote radio can respond to the poll with its traffic if it has any. With these techniques, the average power consumption of the radio can be reduced by more than an order of magnitude while meeting all data transfer objectives." Harris AN9614 at 3.

With respect to the 'slave communication from a slave device to the master communication device occurring in response to a master communication from the master communication device to the slave device',

Applicants' Admitted Prior Art[10] discloses a communication device capable of communication according to a master/slave relationship in which a slave communication from a slave to a master occurs in response to a master communication from the master to the slave. *See, e.g.,* **'228 at 3:64- 5:7, Figs. 1, 2.**

For example, the '228 patent discloses a prior art system with master and tributary (slave) transceivers, as shown in Figures 1 and 2 (depicted below).

[9] A polled protocol is a master/slave protocol, as confirmed by the '228 patent. '228 patent at 4:30-34. *See also* IPR2014-00892, Pap. 46 at 16 ("In [a polling] protocol, a centrally assigned master periodically sends a polling message to the slave nodes, giving them explicit permission to transmit on the network."); '228 Prosecution History at 352; IPR2014-00892, Ex.1323 (Goodman Declaration) Para124.

[10] In IPR2014-00892, the Board found that the '228's disclosed multipoint communication systems or master/slave systems, depicted in '228 patent, Figures 1and2 and 3:64-5:7 is material that may be used as prior art against the patent under §103. IPR2014-00892, Pap. 46 (Final Written Decision) at 13-14; *see Pharmastem Therapeutics, Inc. v. Viacell, Inc.,* 491 F.3d 1342, 1362 (Fed. Cir. 2007) ("Admissions in the specification regarding the prior art are binding on the patentee for purposes of a later inquiry into obviousness."); *Constant v. Advanced Micro-Devices, Inc.,* 848 F.2d 1560, 1570 (Fed.Cir.1988) ("A statement in the patent that something is in the prior art is binding on the applicant and patentee for determinations of anticipation and obviousness."). As explained in Section 111.E, a POSIT A would have been motivated and found it obvious and straightforward to use the Applicant's Admitted Prior Art of a master/slave communication system *(see* '228 patent at 3:64-5:7, Figs. 1, 2) in implementing Snell's communication system (as implemented in light of Harris 4064.4).

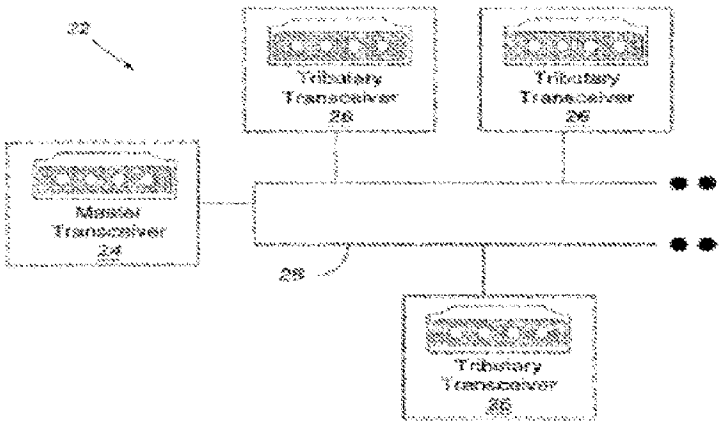


FIG. 1
Prior Art

'228 at Fig. 1.

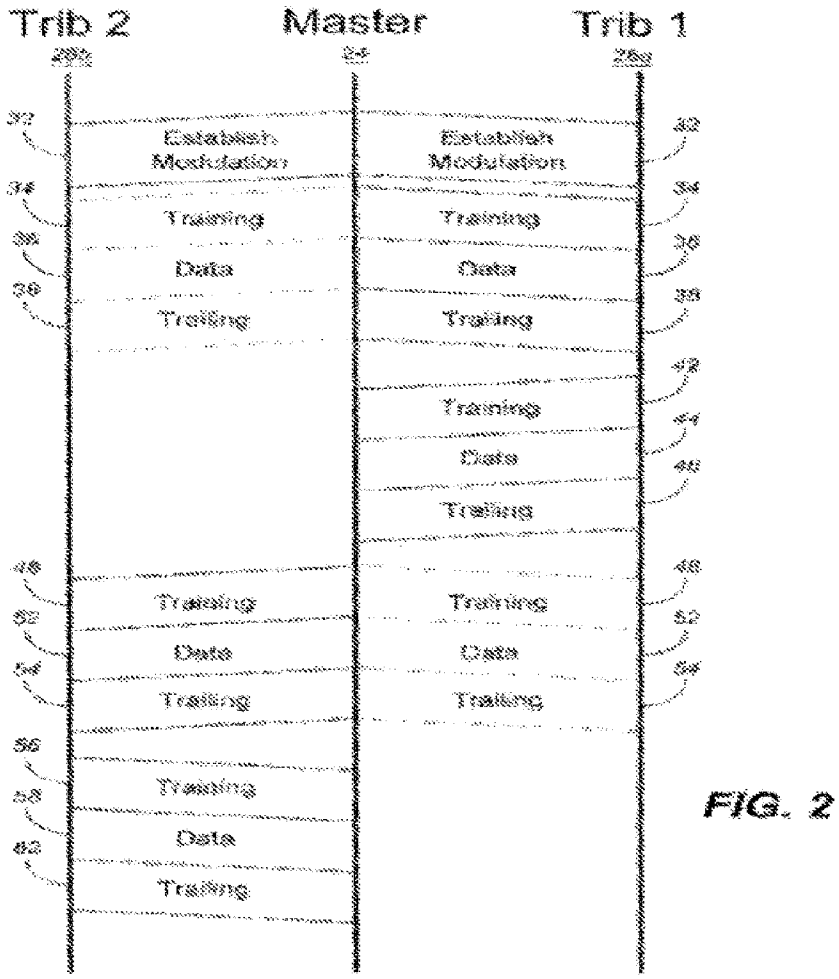


FIG. 2

'228 at FIG 2.

> "With reference to *FIG. 1, a prior art multipoint communication system 22 is shown to comprise a master modem or transceiver 24, which communicates with a plurality of tributary modems (tribs) or transceivers 26-26 over communication medium 28.* Note that all tribs 26-26 are identical in that they share a common modulation method with the master transceiver 24. Thus, before any communication can begin in multipoint system 22, the master transceiver and the tribs 26-26 must agree on a common modulation method. If a common modulation method is found, the master transceiver 24 and a single trib 26 will then exchange sequences of signals that are particular subsets of all signals that can be communicated via the agreed upon common modulation method. These sequences are commonly referred to as training signals and can be used for the following purposes: 1) to confirm that the common modulation method is available, 2) to establish received signal level compensation, 3) to establish time recovery and/or carrier recovery, 4) to permit channel equalization and/or echo cancellation, 5) to exchange parameters for optimizing performance and/or to select optional features, and 6) to confirm agreement with regard to the foregoing purposes prior to entering into data communication mode between the users. In a multipoint system, the address of the trib with which the master is establishing communication is also transmitted during the training interval. At the end of a data session a communicating pair of modems will typically exchange a sequence of signals known as trailing signals for the purpose of reliably stopping the session and confirming that the session has been stopped. In a multipoint system, failure to detect the end of a session will delay or disrupt a subsequent session. Referring now to FIG. 2, an exemplary multipoint communication session is illustrated through use of a ladder diagram. *This system uses polled multipoint communication protocol. That is, a master controls the initiation of its own transmission to the tribs and permits transmission from a trib only when that trib has been selected.* At the beginning of the session, the master transceiver 24 establishes a common modulation as indicated by sequence 32 that is used by both the master 24 and the tribs 26a, 26b for communication. Once the modulation scheme is established among the modems in the multipoint system, The master transceiver 24 transmits a training sequence 34 that includes the address of the trib that the master seeks to communicate with. In this case, the training sequence 34 includes the address of trib 26a. As a result, trib 26b ignores training sequence 34. After completion of the training sequence 34, master transceiver 24 transmits data 36 to trib 26a followed by trailing sequence 38, which signifies the end of the communication session. Similarly, with reference to FIG. 8, the sequence 170 illustrates a Type A modulation training signal, followed by a Type A modulation data signal. Note that trib 26b ignores data 36 and trailing sequence 38 as it was not requested for communication during training sequence 34. At the end of trailing sequence 38, trib 26a transmits training sequence 42 to initiate a communication session with master transceiver 24. *Because master transceiver 24 selected trib 26afor communication as part of training sequence 34, trib 26a is the only modem that will return a transmission.* Thus, trib 26a transmits data 44 destined for master transceiver 24 followed by trailing sequence 46 to terminate the communication session.

The foregoing procedure is repeated except master transceiver identifies trib 26b in training sequence 48. In this case, trib 26a ignores the training sequence 48 and the subsequent transmission of data 52 and trailing sequence 54 because it does not recognize its address in training sequence 48. Master transceiver 24 transmits data 52 to trib 26b followed by trailing sequence 54 to terminate the communication session. Similarly, with reference to FIG. 8, sequence 172 illustrates a Type A modulation signal, with notification of a changes to Types B, followed by a Types B modulation data signal. To send information back to master transceiver 24, trib 26b transmits training sequence 56 to establish a communication session. *Master transceiver 24 is conditioned to expect data only from trib 26b because trib 26b was selected as part of training sequence 48.* Trib 26b transmits data 58 to master transceiver

wherein the first message comprises:
first information modulated according to a first modulation method,

Snell discloses that the master transceiver transmits a first message (PLCP header and PLCP preamble, figure 3 annotated below) which comprises first information modulated according to a first modulation method (BPSK), *See, e.g.,* **Snell at Abstract, 1:34-46, 1:47-50, 1:55-57, 1:58-61, 2:27-30, 2:56-59, 2:61-3:5, 4:42-47, 5:18-2, 6:35-36, 6:52-59, 6:64-66, 7:1-2, 7:5-14,** 7:6- **8, Figs. 2, 3; Harris AN9614 at 3; Harris 4064.4 at 14, 15, 16, Fig. 10.**

second information, including a payload portion, modulated according to the first modulation method,

Snell discloses that the master transceiver transmits second information, including a payload portion (MPDU, figure 3), modulated according to the first modulation method (BPSK), *See, e.g.,* **Snell at Abstract, 1:34-46, 1:47-50, 1:55-57, 1:58-61, 2:27-30, 2:56-59, 2:61-3:5, 4:42-47, 5:18-2, 6:35-36, 6:52-59, 6:64-66, 7:1-2, 7:5-14,** 7:6- **8, Figs. 2, 3; Harris AN9614 at 3; Harris 4064.4 at 14, 15, 16, Fig. 10.**

wherein the second information comprises data intended for one of the one or more slave transceivers and

Snell discloses that the second information (MPDU) comprises data intended for one of the one or more slave transceivers. *See, e.g.,* **Snell at Abstract, 1:34-46, 1:47-50, 1:55-57, 1:58-61, 2:27-30, 2:56-59, 2:61-3:5, 4:42-47, 5:18-2, 6:35-36, 6:52-59, 6:64-66, 7:1-2, 7:5-14,** 7:6- **8, Figs. 2, 3; Harris AN9614 at 3; Harris 4064.4 at 14, 15, 16, Fig. 10.**

With reference to Figure 3 (annotated below) which depicts a message from the master transceiver, a first message includes a PLCP header and PLCP preamble, the MPDU corresponds to second information which is transmitted to the respective slave transceiver.

Snell discloses the transceiver transmitting a "first message" comprising "first information" (*e.g.*, PLCP preamble and PLCP header) "modulated according to a first modulation method" (*e.g.*, BPSK) and "second information, including a payload portion" (*e.g.*, MPDU data) "modulated according to the first modulation method" (*e.g.*, BPSK) (as depicted in Figure 3 below). Snell alternatively discloses modulating the "first information" (*e.g.*, PLCP preamble and PLCP header) and "second information, including a payload portion" (*e.g.*, MPDU data) according to DBPSK which also is a "first modulation method."

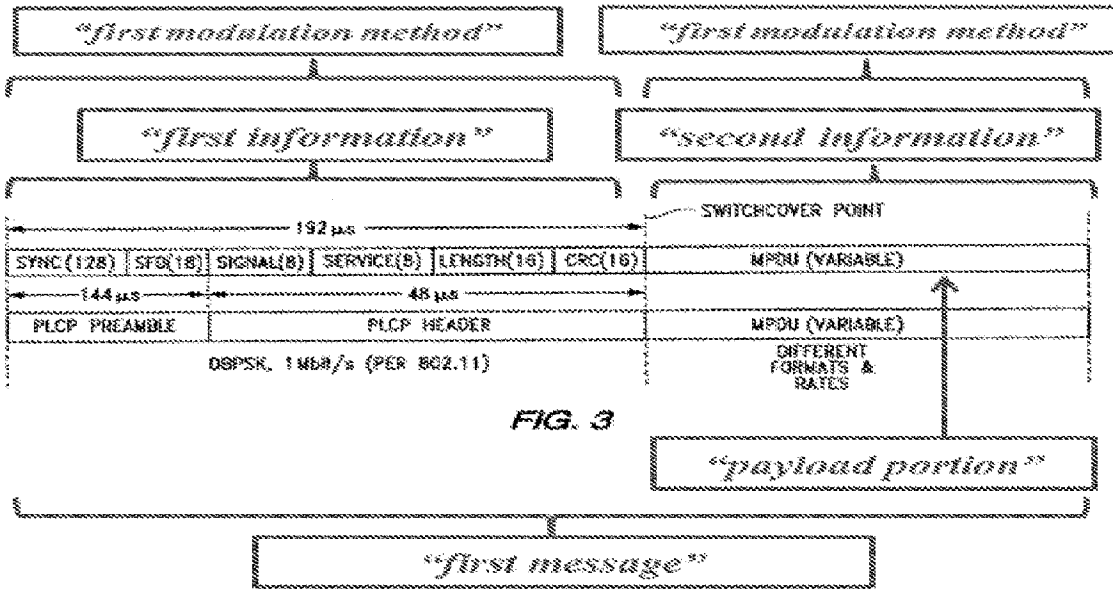


FIG. 3

Snell at Fig. 3 (annotated).

"The ***header may always be BPSK.***" Snell at 6:35-36.

Snell discloses that the "**SIGNAL" in the PLCP header indicates** (*e.g.*, using "0Ah") the **modulation type** (*e.g.*, BPSK) **used for modulating the MPDU data portion**.

"Now relating to the PLCP header 91, the SIGNAL is:

0Ah	1 Mbit/s BPSK,
14h	2 Mbit/S QPSK,
37h	5.5 Mbit/s BPSK, and
6Eh	11 Mbit/s QPSK.

"

Snell at 6:52-59.

"SIGNAL is indicated by 2 control bits and then formatted as described." Snell at 7:1-2.

"MPDU is serially provided by Interface 80 and is the variable data scrambled for normal operation. The reference phase for the first symbol of the MPDU is the output phase of the last symbol of the header for Diff Encoding. The last symbol of the header into the scrambler 51 must be followed by the first bit of the MPDU. The **variable data may be modulated and demodulated in different formats than the header portion to thereby increase the data rate,** and while a switchover as indicated by the switchover point in FIG. 3, occurs on-the-fly." Snell at 7:5-14.

"The modulator preferably comprises means for *operating in one of a biphase PSK (BPSK) modulation mode at a first data rate defining a first format,* and a quadrature PSK (QPSK) mode at a second data rate defining a second format." Snell at 2:56-59.

"In particular, the HSP3824 baseband processor manufactured by Harris Corporation *employs quadrature or bi-phase phase shift keying (QPSK or BPSK) modulation schemes."* Snell at 1:58-61.

See also, e.g., Snell at Abstract ("The modulator and demodulator are each preferably operable *in one of a bi-phase PSK (BPSK) mode* at a first data rate and *a quadrature PSK (QPSK) mode* at a second data rate. These formats may also be switched on-the-fly in the demodulator."), 2: 15-17 ("**Moreover, a WLAN application, for example, may require a change between *BPSK and QPSK* during operation,** that is, on-the-fly.").

*"**The PLCP preamble and PLCP header are always** **at 1 Mbit/s, *Diff encoded,*** scrambled and spread with an 11 chip barker." Snell at 6:64-66.

"The modulator may also preferably include header modulator means for modulating data packets to include *a header at a predetermined modulation and a third data rate defining a third format .... The third format is preferably differential BPSK."* Snell at 2:61-3:5. "The reference phase for the first symbol of the *MPDU* is the output phase of the last symbol of the header/or *Diff Encoding."* Snell at 7:6-8.

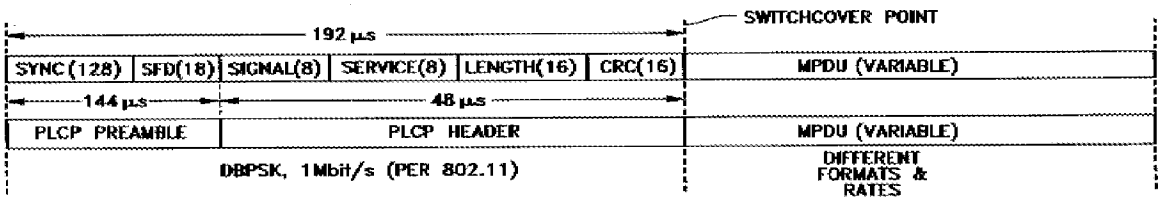
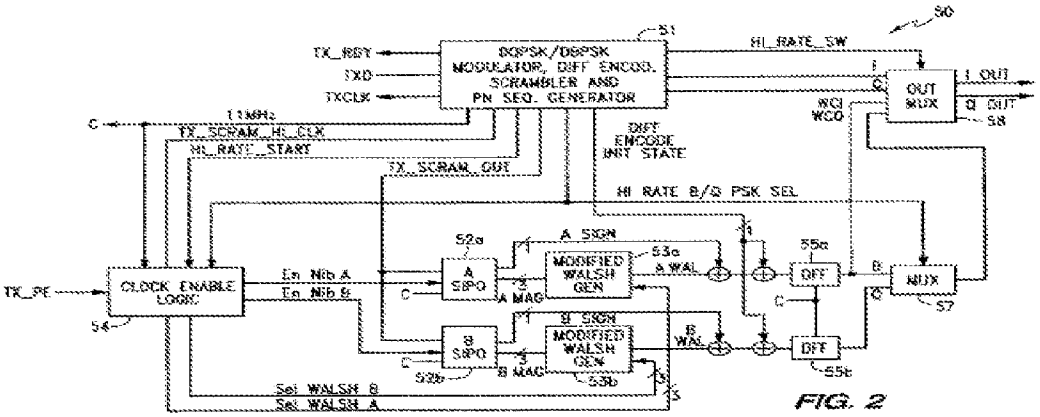
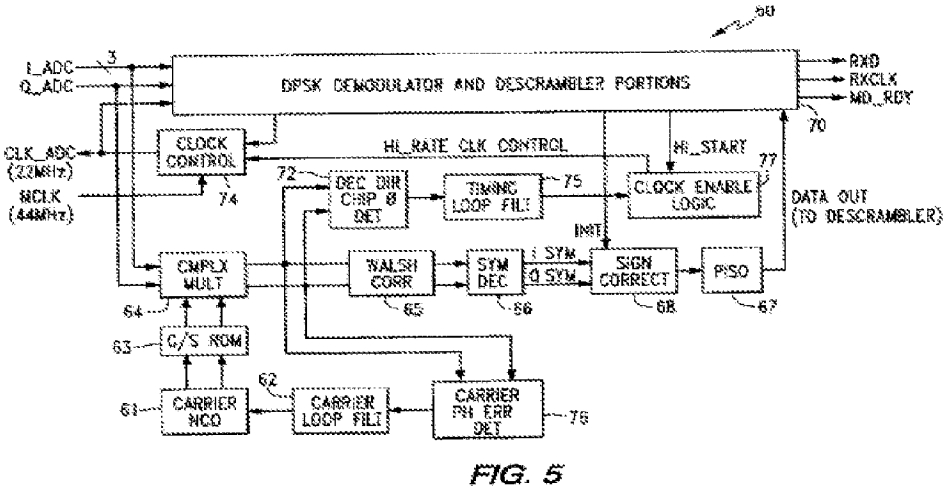


FIG. 3

Snell Figure 3



Snell Figure 2



Snell Figure 5

Snell incorporates by reference Harris 4064.4,[11] which discloses:

"The preamble and header are always transmitted as DBPSK waveforms while the ***data packets can be configured to be either DBPSK* or DQPSK**." Harris 4064.4 at 14.

"The *preamble is always transmitted as a DBPSK* waveform with a programmable length of up to 256 symbols long." Harris 4064.4 at 15.

[11] Snell expressly incorporates by reference "the entire disclosure" of Harris 4064.4 (Snell at 5:8-17, 5:31-33). *See Harari v. Lee,* 656 F.3d 1331, 1335-36 (Fed. Cir. 2011) ("the entire '579 application disclosure was incorporated by the broad and unequivocal language: 'The disclosures of the two applications are hereby incorporate[d] by reference."'); *see also Advanced Display Sys., Inc. v. Kent State Univ.,* 212 F.3d 1272, 1282 (Fed.Cir.2000) ("material not explicitly contained in the single, prior art document may still be considered for purposes of anticipation if that material is incorporated by reference into the document.").

"Signal Field (8 Bits) - This field indicates whether the data packet that follows the header is modulated as DBPSK or DQPSK. In mode 3 the HSP3824 receiver looks at the signal field to determine whether it needs to switch from DBPSK demodulation into DQPSK demodulation at the end of the always DBPSK preamble and header fields." Harris 4064.4 at 15.

"Mode 3 - In this mode the preamble is programmable up to 256 bits (all l's). The header in this mode is using all available fields. *In mode 3 the signal field defines the modulation type of the data packet (DBPSK* or DQPSK) so the receiver does not need to be preprogrammed to anticipate one or the other. In this mode the device checks the Signal field for the data packet modulation and it switches to DQPSK if it is defined as such in the signal field. *Note that the preamble and header are always DBPSK* the modulation definition applies only for the data packet." Harris 4064.4 at 16.

See also, e.g., Harris 4064.4 at 14 ("The HSP3824 transmitter is designed as a Direct [12] Sequence Spread Spectrum DBPSK/DQPSK modulator."), Harris 4064.4 at 14 ("The modulator is capable of switching rate automatically in the case where the preamble and header information are DBPSK modulated, and the data is DQPSK modulated."), Harris 4064.4 at FIGURE 10.

To the extent that it is deemed that Harris 4064.4 should be treated as independent reference from Snell, one of ordinary skill in the art at the time the invention was made would have been motivated and found it obvious and straightforward to use Harris 4064.4' s teachings of modulating the preamble and header portions of a data packet using DBPSK modulation and modulating the payload portion of the data packet using DBPSK or DQPSK modulation (as indicated by the SIGNAL field in the header portion) to advantageously provide for switching between DBPSK and DQPSK modulation types in implementing an IEEE 802.11 system *(see* Harris 4064.4 at 1, 3) such as disclosed in Snell. Harris 4064.4 is incorporated by reference into Snell (Snell at 5: 13-17), both references are directed to the PRISM chipset and HSP 3824 baseband processor (Harris 4064.4 at l; Snell at 1:47-63, 5:8-17, 5:31-33), and Harris 4064.4 is a publication of Harris Corporation, the same original assignee of Snell.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Harris 4064.4 with the teachings of Snell, in light of the foregoing including Snell's express direction to apply the teachings of Harris 4064.4, and further because, in

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[12] Snell expressly incorporates by reference "the entire disclosure" of Harris 4064.4 (Snell at 5:8-17, 5:31-33). *See Harari v. Lee,* 656 F.3d 1331, 1335-36 (Fed. Cir. 2011) ("the entire '579 application disclosure was incorporated by the broad and unequivocal language: 'The disclosures of the two applications are hereby incorporate[d] by reference."'); *see also Advanced Display Sys., Inc. v. Kent State Univ.,* 212 F.3d 1272, 1282 (Fed.Cir.2000) ("material not explicitly contained in the single, prior art document may still be considered for purposes of anticipation if that material is incorporated by reference into the document.").

combination, each element (Harris 4064.4's teaching of modulating the preamble and header portions of a data packet using DBPSK modulation and modulating the payload portion of the data packet using DBPSK or DQPSK modulation and Snell's communication system for transmitting data packets modulated using different modulation methods) performs the same function as it would separately, yielding nothing more than predictable results. *KSR,* 550 U.S. at 417. One of ordinary skill in the art would have thus recognized that this combination (yielding the claimed limitation) would have worked as expected and for these reasons, would have been motivated and found it obvious and straightforward to use Harris 4064.4's teachings in implementing Snell's communication system.

One of ordinary skill in the art would have additionally been motivated and found it obvious and straightforward to use Harris AN9614's teaching of a polled (master/slave) protocol in implementing the communication system taught by Snell (in light of Harris 4064.4). Harris AN9614 is incorporated by reference into Snell (Snell at 5 :2-7), both references are directed to the PRISM chipset and HSP 3824 baseband processor (Harris AN9614 at 1, 2; Snell at 1:47-63, 5:8-17, 5:31-33), and Harris AN9614 is a publication of Harris Corporation, the same original assignee of Snell. Moreover, AN9614 expressly teaches that it is beneficial to use a polled (master/slave) protocol because "the average power consumption of the radio can be reduced by more than an order of magnitude while meeting all data transfer objectives." Harris AN9614 at 3. Polling (master/slave) enables this reduction in power consumption because "the system can be set at its sleep mode most of the time to achieve low power consumption. It only needs to operate at full power consumption during the transmission of a packet or during the expected window for received packets." Harris AN9614 at 3. In addition to Snell's express suggestion to apply Harris AN9614's disclosures, one of ordinary skill in the art would have been motivated to use Harris AN9614's teaching of a polled (master/slave) protocol in implementing Snell's communication system (implemented in light of Harris 4064.4, *see supra)* because a polled (master/slave) communication system advantageously provides a simple protocol that has good determinacy *(e.g.,* a reduction in collisions). It would have been routine for one of ordinary skill in the art to use a polled (master/slave) protocol in implementing Snell's communication system (as implemented in light of Harris 4064.4), as master/slave communication systems were common and well-known in the art *(see* '228 patent at 3: 64- 5:7), and thus implementing a polled (master/slave) protocol in Snell's transceiver (which serves as an access point to support communications with multiple other transceivers - Snell at I :34-46) would involve nothing more than using common and known techniques to improve a similar system in the same way to yield predictable results. *KSR,* 550 U.S. at 416. One of ordinary skill in the art would have thus recognized that this combination (yielding the claimed limitation) would have worked as expected. For these reasons, one of ordinary skill in the art would have been motivated and found it obvious and straightforward to implement a polled (master/slave) protocol in implementing Snell's system (as implemented in light of Harris 4064.4).

It would have further been obvious to one of ordinary skill in the art at the time the invention was made and one would have been motivated and found it obvious and straightforward to use the Applicant's Admitted Prior Art of a master/slave communication system *(see* '228 patent at

3:64-5:7, Figs. 1, 2) in implementing Snell's communication system because a polled (master/slave) communication system was a popular communication protocol with recognized benefits prior to the earliest claimed priority date.

Snell is in the same field of art as the Admitted Prior Art, with both relating to a communication system among transceivers. *See, e.g.,* Snell at 1 :34-46; Harris AN9614 at 3 *(see also* Snell at 5 :2-7); '228 patent at 3:64-4:1. Snell further incorporates by reference Harris AN9614 (Snell at 5:2-7), which is an application note for the Harris PRISM chipset and HSP3824 baseband processor described in Snell. Harris AN9614 at 1 ("Using the *PRISM™ Chip Set ... "),* 2 *("The HSP3824* performs the baseband demodulation function."); Snell at 5:30-32 *("The present invention provides an extension of the PRISM I product ... "),* 5: 11-13 *("The conventional Harris PRISM I chip set includes* a low data rate DSS baseband processor available under the designation *HSP3824).* Harris AN9614 expressly teaches that the communications between Snell's transceivers may operate according to a "polled" (master/slave) protocol. *See, e.g.,* Harris AN96 I 4 ("the controller can keep adequate time to operate either a *polled* or time allocated *scheme.").* Similarly, the admitted prior art in the '228 patent also describes using a *"polled* multipoint communication protocol," which is a master/tributary *(i.e.,* master/slave) system. '228 patent at 4:30-33. As shown in Fig. 1 below, the admitted prior art of the '228 patent discloses a master transceiver 24 that communicates with a plurality of tributary transceivers 26. '228 patent at 3:64-4:3, Fig. 1.

Upender is in the same field of art as Snell, with both relating to protocols for communications over a network. *See, e.g.,* Upender at 7 ("let's examine various *commonly available media access protocols"),* 7 *("In this protocol,* a centrally assigned master sends a polling message to the slave nodes, giving them explicit permission *to transmit on the network.").* Upender further confirms that a person of ordinary skill in the art would be motivated to use a master/slave protocol in implementing the teachings of Snell (as implemented in light of Harris 4064.4). Upender discusses a finite list of well-known communications protocols applicable for use in a network setting, including a polled (master/slave) protocol, and expressly teaches benefits of using a polled (master/slave) protocol. For example, Upender teaches that *"[p]olling is one of the more popular protocols* for embedded systems *because of it simplicity and determinacy.* In this protocol, a centrally assigned master periodically polls the slave nodes for information." Upender at 7; *see also* IPR2014-00892, Pap. 46 at 16-17 (citing Upender at 7 and finding that "Upender teaches that master/slave protocols were widely used and a good choice for simple systems"); '228 Prosecution History at 352-353August 26, 2016;IPR2014-00892, Ex. 1323 (Declaration of David Goodman) 1-125. While Upender discloses tradeoffs of using a master/slave protocol as compared with other communication protocols *(see* Upender at 11, Table 1),

Upender expressly teaches that a protocol for a particular application should be selected in light of the respective costs and benefits of available protocols, noting that the discussion of the strengths and weaknesses of the different protocols "should allow you to select the best protocol to match your needs". Upender at 10-11; *see also* IPR2014-00892, Pap. 46 at 17 (citing Upender at 10-11 and finding that Upender does not "teach away" from using the master/slave protocol);

'228 Prosecution History at 353. Upender's express teaching that a polled (master/slave) protocol is advantageous for its "simplicity and determinacy," would have motivated one of ordinary skill to use such a protocol in implementing Snell's communication system, particularly in any system in which simplicity and determinacy are important considerations. Upender at 7; *see also* IPR2014-00892, Pap. 46 at 16-18; '228 Prosecution History at 352-354. Upender further teaches that a polled (master/slave) protocol is *"ideal for a centralized data-acquisition system* where peer-to-peer communication and global prioritization are not required," such as Snell's centralized data-acquisition system comprising an access point transceiver supporting a group of transceivers which does not require communicating using peer-to-peer communication or global prioritization. *See* Snell at 1:34-46.

In addition, the Admitted Prior Art demonstrates that polled (master/slave) protocols were well-known *(see* '228 patent at 3:64-4:1), as also further confirmed by Upender *(see* Upender at 7 ("let's examine various *commonly available media access protocols"),* 7 *("polling [(master/slave)} is one of the more popular protocols"),* and thus implementing a polled (master/slave) protocol in Snell's transceiver (as implemented in light of Harris 4064.4), which serves as an access point to support communications with multiple other transceivers and is also operable according to a polled (master/slave) protocol, would involve nothing more than using common and known techniques to improve a similar system in the same way to yield predictable results. *KSR,* 550 U.S. at 416. One of ordinary skill would have thus recognized that this combination (yielding the claimed limitation) would have worked as expected. For these reasons, one of ordinary skill would have been motivated and found it obvious and straightforward to implement the admitted prior art of a master/slave communication system in implementing Snell's system (as implemented in light of Harris 4064.4).

first message address information that is indicative of the one of the one or more slave transceivers being an intended destination of the second information; and

> **Snell does not expressly disclose** *the first message comprises first message address information that is indicative of the one of the one or more slave transceivers being an intended destination of the second information.*
>
> Yamano teaches that packets can be advantageously addressed for an intended destination. Yamano discloses transmitting a "first message" *(e.g.,* data packet including a preamble and main body) that includes "first message address information that is indicative" *(e.g.,* "destination address" in the preamble) of the transceiver that is the "intended destination of the second information."
>
> *"Packet 700* includes a *preamble 701* and a *main body 702."* Yamano at 19:63-64.
>
> "For example, *preamble 701* can include information which identifies: (1) a version or type field for the preamble, (2) ***packet source and destination addresses,*** (3) the line code (i.e., the modem protocol being used), (4) the data rate, (5) error control parameters,

(6) packet length and (7) a timing value for the expected reception slot of a subsequent packet." Yamano at 20:1-7.

Yamano also discloses that the preamble precedes the main body (containing data), as shown in Figure 8. Yamano teaches that the first message comprises first message address information that is indicative of the one of the one or more slave transceivers being an intended destination of the second information. *See, e.g.,* Yamano at 19:63-64, 20:1-7, 20:54-59, Fig. 8.

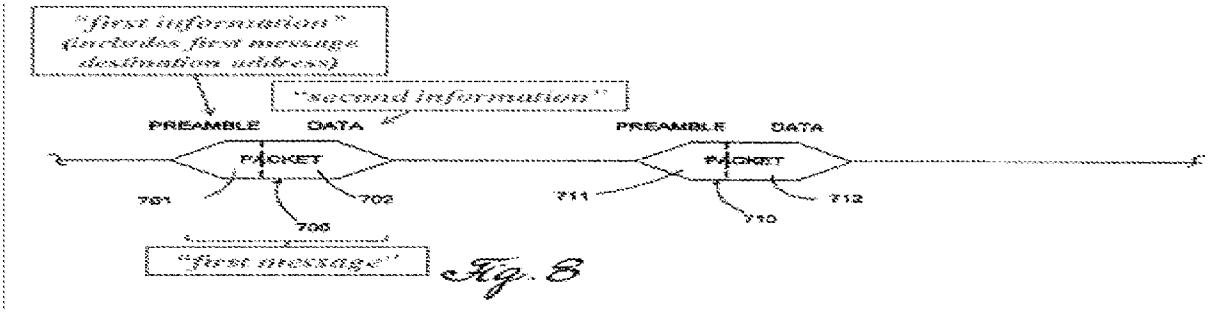


Fig. 8

Yamano at Fig. 8 (annotated).

Snell and Yamano are in the same field of art, with both relating to transmitting data packets over a network *(see, e.g.,* Snell at 1:55-58, 2:61-63, 2:66-3:3, 5:18-21, 6:48-63, Fig. 3; Yamano at 1: 1-29, 19:54-20:33, Fig. 8), at varying rates *(see, e.g.,* Snell at 2: 15-17, 6:52-59; Yamano at 19:54-56). Yamano expressly teaches that including a destination address in the preamble portion of the data packet, which precedes the data portion, will advantageously reduce processing requirements of receiving devices because the receiving device can filter out packets which it does not need to demodulate. Yamano at 20:54-59 ("When the preamble in a burst-mode packet *includes the destination address of the packet,* the receiver circuits can monitor the destination address of the packet, and in response, filter packets which do not need to be demodulated, thereby reducing the processing requirements of the receiver circuits.").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Yamano' s teaching of including a destination address in the preamble portion of a data packet in implementing Snell's data packet implemented in light of Harris 4064.4 and Harris AN9614 comprising preamble, header, and MPDU data portions to advantageously specify which receiver the data is intended for and to beneficially reduce the processing requirements at the receiving device, as taught by Yamano. "When the preamble in a burst-mode packet *includes the destination address of the packet,* the receiver circuits can monitor the destination address of the packet, and in response, filter packets which do not need to be demodulated, thereby reducing the processing requirements of the receiver circuits." Yamano at 20:54-59.

In addition, Snell teaches structuring its data packet to include a preamble, header, and MPDU data portion *(see, e.g.,* Snell at 6:35-36, 6:64-66, 7:5-14, Fig. 3), and Yamano teaches structuring its data packet to also include a preamble and data portion, and to place the destination address in the preamble portion (Yamano at 19:63-20:7, Fig. 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a destination address in the preamble portion of a data packet, as taught by Yamano, in implementing Snell's system implemented in light of Harris 4064.4 and Harris AN9614 for transmitting data packets between transceivers, as Snell teaches that its data packet already includes a preamble portion-and in combination, each element (Yamano' s teaching of placing a destination address in the preamble and Snell's teaching of a system for communicating data packets modulated according to different modulation methods between transceivers) performs the same function as it would separately, yielding nothing more than predictable results. *KSR Int'l Co. v. Teleflex Inc.,* 550 U.S. 398, 417 (2007). One of ordinary skill in art at the time the invention was made would have thus recognized that this combination (yielding the claimed limitation) would have worked as expected. For these reasons, a person of ordinary skill would have been motivated and found it obvious and straightforward to use the teachings of Yamano including a destination address in the preamble of a data packet in implementing Snell's communication system.

Snell in view of Harris 4064.4 and Harris AN9614 in view of Yamano thus teach that the first message comprises first message address information that is indicative of the one of the one or more slave transceivers being an intended destination of the second information. *See, e.g.,* Snell at 6:35-36, 6:64-66, 7:5-10, Fig. 3; Harris 4064.4 at 14; Yamano at 19:63-64, 20:1-7, 20:54-59, Fig. 8.

said master transceiver configured to transmit a second message over the communication medium from the master transceiver to the one or more slave transceivers wherein the second message comprises:

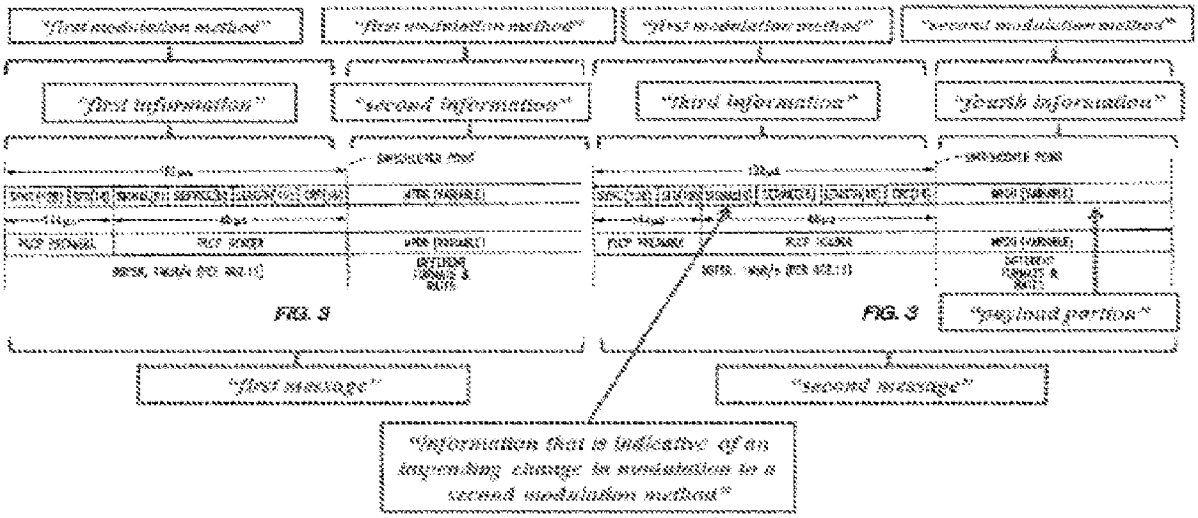
third information modulated according to the first modulation method,
wherein the third information comprises information that is indicative of an impending change in modulation to a second modulation method, and

fourth information, including a payload portion, transmitted after transmission of the third information,
the fourth information being modulated according to the second modulation method,
the second modulation method being of a different type than the first modulation method,
wherein the fourth information comprises data intended for a single slave transceiver of the one or more slave transceivers, and

As noted above, Snell discloses that the transceiver transmits data packets to multiple different end user slave transceivers, as such multiple messages of format shown in figure 3 are provided to the slave transceivers and where the communication may switch on-the-fly between a "first modulation method" *(e.g.,* BPSK) and a "second modulation method" *(e.g.,* QPSK) that is "of a different type than the first modulation method." **Snell thus teaches transmitting a "first message" and a "second message" as shown in annotated Figure 3 below.** *See, e.g.,* Snell at 1:34-46, 1:47-50, 1:55-57, 2:27-30, 2:61-3:5, 4:42-47, 5:18-2, 6:35-36, 6:52-59, 6:64-66, 7:1-2, 7:5-14, Fi s. 2, 3, 5; Harris AN9614 at 3; Harris 4064.4 at**14-16, Fig. 10**

For example, Snell discloses a "transceiver" that serves as an access point for communicating "data intended for a [transceiver]" connected to a wireless local area network (WLAN). *See* claim 1 preamble.

Snell also discloses that the transceiver transmits data packets to another transceiver, where the communication may switch on-the-fly between a "first modulation method" *(e.g.,* BPSK) and a "second modulation method" *(e.g.,* QPSK) that is "of a different type than the first modulation method." Snell thus teaches transmitting a "first message" and a "second message" as shown in annotated Figure 3 below.



Snell Figure 3 Annotated (page 54 Request)

Snell teaches communicating multiple data packets with the ability to "switch on-the-fly between different data rates and/or formats" as noted above, based on this disclosure, a person of ordinary skill in the art would have understood that Snell teaches that a series of packets may be sent that switch from using a first modulation method to using a second modulation method for the payload portion of the data packet. For example, the "first message" in Snell comprises "first information" *(e.g.,* PLCP preamble and PLCP header) that is "modulated according to a first modulation method" *(e.g.,* BPSK) where the "first information" *(e.g.,* "SIGNAL" field in PLCP header) indicates *(e.g.,* using "OAh") the modulation type *(e.g.,* BPSK) used for modulating "second information"

(e.g., MPDU data). In the "first message," the "SIGNAL" field in the PLCP header uses a code *(e.g.,* "OAh") that indicates that the "second information" *(e.g.,* MPDU data) is modulated "according to the first modulation method" *(e.g.,* BPSK at 1 Mbit/s).

Snell's transceiver can transmit a "second message" comprising "third information" *(e.g.,* PLCP preamble and PLCP header) "modulated according to the first modulation method" *(e.g.,* BPSK) where the "third information comprises information" *(e.g.,* "SIGNAL" field in PLCP header) "that is indicative of an impending change in modulation" *(e.g.,* using "l 4h") "to a second modulation method" *(e.g.,* QPSK) used for modulating "fourth information." For example, in the "second message," the "SIGNAL" field in the PLCP header uses a code *(e.g.,* "14h") that indicates that the "fourth information" *(e.g.,* MPDU data) is modulated "according to the second modulation method" *(e.g.,* QPSK at 2 Mbit/s), wherein the "second modulation method" is of a "different type than the first modulation method." This "SIGNAL" is "indicative of an impending change" from the "first modulation method" to the "second modulation method" because it is indicating a change from, for example, QPSK modulation to BPSK modulation. In addition, transmitting the data using the "second modulation method"- QPSK-results in a data rate of 2 Mbit/s which is higher than transmitting the data using the "first modulation method " BPSK at 1 Mbit/s.

"The modulator may also preferably include header modulator means for modulating *data packets."* Snell at 2:61-63.

"The PRISM 1 chip set provides all the functions necessary for full or half duplex, direct sequence spread spectrum, *packet communications* at the 2.4 to 2.5 GHz ISM radio band." Snell at 1:55-57.

"It is another object of the invention to provide a spread spectrum transceiver and associated method to permit operation at higher data rates and *which may switch on-the-fly between different data rates and/or formats."* Snell at 2:27-30.

"The variable data may be modulated and demodulated in different formats than the header portion to thereby increase the data rate, and *while a switchover as indicated by the switchover point in FIG. 3, occurs on-the-fly."* Snell at 7: 10-14.

"The *header* may always be *BPSK."* Snell at 6:35-36.

"Now relating to the *PLCP header* 91, *the SIGNAL* is:

0Ah	1 Mbit/s BPSK,
14h	2 Mbit/S QPSK,
37h	5.5 Mbit/s BPSK, and
6Eh	11 Mbit/s QPSK.

"

SIGNAL is indicated by 2 control bits and then formatted as described." Snell at 7:1-2.

"MPDU is serially provided by Interface 80 and *is the variable data* scrambled for normal operation. The reference phase for the first symbol of the MPDU is the output phase of the last symbol of the header for Diff Encoding. The last symbol of the header into the scrambler 51 must be followed by the first bit of the MPDU. *The variable data may be modulated and demodulated in different formats* than the header portion to thereby increase the data rate, and while a switchover as indicated by the switchover point in FIG. 3, occurs on-the-fly." Snell at 7:5-14.

Snell describes that the "first modulation method" may be BPSK and the "second modulation method" may be QPSK, which is of a different "type" than the first modulation method, and alternatively describes that the "first modulation method" may be differential BPSK ("DBPSK") and that the "second modulation method" may be differential QPSK ("DQPSK"), which is also of a different "type" than the first modulation method.

Thus, Snell alternatively describes modulating the "first information" *(e.g.,* PLCP preamble and PLCP header) according to a "first modulation method" *(e.g.,* DBPSK) and "second information" *(e.g.,* MPDU data) according to either a "first modulation method" *(e.g.,* DBPSK) or "second modulation method" *(e.g.,* QBPSK).

"The PLCP preamble and PLCP header are always at 1 Mbit/s, *Diff encoded,* scrambled and spread with an 11 chip barker." Snell at 6:64-66.

"The modulator may also preferably include header modulator means for modulating data packets to include *a header at a predetermined modulation and a third data rate defining a third format .... The third format is preferably differential BPSK."* Snell at 2:61-3:5.

"The reference phase for the first symbol of the *MPDU* is the output phase of the last symbol of the header/or *Diff Encoding."* Snell at 7:6-8. *See also, e.g.,* Snell at Figs. 2, 3, 5.

Snell incorporates by reference Harris 4064.4, 17 which discloses: *"The preamble and header are always transmitted as DBPSK* waveforms while the *data packets can be configured to be either DBPSK or DQPSK."* Harris 4064.4 at 14.

"The *preamble is always transmitted as a DBPSK* waveform with a programmable length of up to 256 symbols long." Harris 4064.4 at 15.

"Signal Field (8 Bits) - This field indicates whether the data packet that follows the header is modulated as DBPSK or DQPSK. In mode 3 the HSP3824 receiver looks at the signal field to determine whether it needs to switch from DBPSK demodulation into DQPSK demodulation at the end of the always DBPSK preamble and header fields." Harris 4064.4 at 15.

"Mode 3 - In this mode the preamble is programmable up to 256 bits (all l's). The header in this mode is using all available fields. *In mode 3 the signal field defines the modulation type of the data packet (DBPSK* or *DQPSK)* so the receiver does not need to be preprogrammed to anticipate one or the other. In this mode the device checks the Signal field for the data packet modulation and it switches to DQPSK if it is defined as such in the signal field. *Note that the preamble and header are always DBPSK* the modulation definition applies only for the data packet." Harris 4064.4 at 16.

See also, e.g., Harris 4064.4 at 14 ("The HSP3824 transmitter is designed as a Direct Sequence Spread Spectrum *DBPSKIDQPSK* modulator."), Harris 4064.4 at 14 ("The modulator is capable of switching rate automatically in the case where the preamble and header information are DBPSK modulated, and the data is *DQPSK* modulated."), Harris 4064.4 at FIGURE 10.

Kamerman *discloses transmitting a first message including second information modulated at a first modulation method and transmitting a second message including fourth information modulated at a second modulation method.* *See, e.g.,* **Kamerman at 6, 11, 12.**

For example, Kamerman discloses an automatic rate selection scheme for falling forward from a "first modulation method" *(e.g.,* BPSK) corresponding to a lower data rate *(e.g.,* 1 Mbit/s) to a "second modulation method" *(e.g.,* QPSK) corresponding to a higher data rate *(e.g.,* 2 Mbit/s) after a number of successive correctly acknowledge packet transmissions, for instance, where there is a low load in neighbor cells and a reliable connection.

"Then there is looked to *automatic rate control* to keep the co-channel interference at a tolerable level." Kamerman at 6.

"IEEE 802.11 DS specifies bit rates of 1 and 2 Mbps. The allowable SNR and CSIR values for reliable transmission of data packets are dependent on the bit rate." Kamerman at 11.

"IEEE 802.11 DS specifies BPSK and QPSK, in addition there could be applied proprietary modes with M-PSK and QAM schemes that provide higher bit rates by encoding more bits per symbol. ... An automatic rate selection scheme based on the reliability of the individual uplink and downlink could be applied. The basic rate adaptation scheme could be: after unacknowledged packet transmissions the rate falls back, and *after a number (e.g. JO) of successive correctly acknowledged packet transmissions the bit rate goes up."* Kamerman at 11.

"At lower load in the neighbor cells the highest bit rate can be used more often. At higher load the transmissions from the **access point** to stations at the outer part of the cells, will be done often at fall back rates due to mutilation of transmissions by interference. In practice the network load for LANs at nowadays client-server applications is very bursty, with sometimes transmission bursts over an individual links and low activity during the major part of the time. *Therefore the higher bit rate can be used during the most of the time, and at high load in the neighbor cells (as will evoked by test applications) there will be switched to fall back rates in the outer part of the cell."* Kamerman at 11.

"The application of proprietary bit rates of 3 and 4 Mbps in addition to the basic 1 and 2 Mbps, can be combined with an automatic rate selection. This automatic rate selection *gives fall forward at reliable connections* and fall back at strong co-channel interference." Kamerman at 12

It was well-known in the art, as demonstrated by Kamerman, to transmit a first data packet where the data is modulated using a first modulation method, such as BPSK (corresponding to a lower data transfer rate), and to next transmit a second data packet where the data is modulated using a second modulation method, such as QPSK (corresponding to a higher data transfer rate).

One of ordinary skill in the art at the time the invention was made would have been motivated and found it obvious and straight forward to use Kamerman's teaching of transmitting a first data packet where the data is modulated using a first modulation method and next transmitting a second data packet where the data is modulated using a second modulation method in implementing Snell's system for communicating data packets modulated according to different modulation methods (further modified by the teaching of Yamano, as discussed above) to advantageously maximize the data transfer rate and adapt to changing channel conditions (as also taught by Kamerman). In particular, Kamerman expressly teaches that it is beneficial to transmit the data of a first data packet using a first modulation method corresponding to a lower data transfer rate *(e.g.,* BPSK modulation at 1 mbps) during higher load conditions when a more robust signal is needed due to "mutilation of transmissions by interference," and to next transmit the data of a second data packet using a second modulation method corresponding to a higher data transfer rate *(e.g.,* QPSK modulation at 2 mbps) *(i.e.,* falling forward) to maximize the data transfer rate during lower load conditions when the connection is more

reliable. *See* Kamerman at 6 ("Then there is looked to *automatic rate control* to keep the co-channel interference at a tolerable level."), 11 ("The basic rate adaptation scheme could be: after unacknowledged packet transmissions the rate falls back, and *after a number (e.g. 10) of successive correctly acknowledged packet transmissions the bit rate goes up."),* 11 *("At lower load in the neighbor cells the highest bit rate can be used more often.* At higher load the transmissions from the access point to stations at the outer part of the cells, will be done at fallback rates due to mutilation of transmissions by interference. In practice the network load for LANs at nowadays client-server applications is very bursty, with sometimes transmission bursts over an individual links and low activity during the major part of the time. Therefore the higher bit rate can be used during the most of the time, and at high load in the neighbor cells ... there will be switched to fall back rates in the outer part of the cell."), 12 ("This automatic rate selection gives fall forward at reliable connections and fall back at strong co-channel interference. Therefore it gives adaptation of the bit rate to the interference as it occurs in time depending on positions as load.").

Moreover, Snell and Kamerman are in the same field of art, with both relating to communications between transceivers that use BPSK and QPSK modulation methods to transfer data at different rates according to the draft IEEE 802.11 standard available at that time. *See, e.g.,* Snell at 1:47-63 ("The assignee of the present invention has developed and manufactured a set of integrated circuits for a WLAN under the mark PRISM 1 *which is compatible with the proposed IEEE 802.11 standard .... "),* 5:31-33 ("The present invention provides an extension of the PRISM 1 product from 1 *Mbit/s BPSK and 2 Mbit/s QPSK .. . "*); Kamerman at 6 ("This paper considers the critical parameters for *wireless LANs that operate conform to the IEEE 802.11 DSSS (direct sequence spread spectrum) standard ... "),* 11 ("IEEE 802.11 DS specifies bit rates of 1 and 2 Mbps.", 11 ("IEEE 802.11 DS specifies BPSK and QPSK ... ").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Kamerman' s teaching of transmitting a first data packet where the data is modulated using a first modulation method and next transmitting a second data packet where the data is modulated using a second modulation method in implementing Snell's system (modified in light of Yamano) for communicating data packets modulated according to different modulation methods, as both Snell and Kamerman are directed to IEEE 802.11 systems utilizing BPSK and QPSK modulation corresponding, respectively, to a lower and higher data transfer rates-and in combination, each element (Kamerman's teaching of transmitting a first data packet where the data is modulated using a first modulation method and next transmitting a second data packet where the data is modulated using a second modulation method and Snell's system for communicating data packets modulated according to different modulation methods) performs the same function as it would separately, yielding nothing more than predictable results. *KSR,* 550 U.S. at 417. One of ordinary skill in the art would have thus recognized that this combination (yielding the claimed limitation) would have worked as expected and would

have been motivated and found it obvious and straightforward to use Kamerman' s teaching of transmitting a first data packet where the data is modulated using a first modulation method and next transmitting a second data packet where the data is modulated using a second modulation method in implementing Snell's system (modified in light of Yamano) for communicating data packets modulated according to different modulation methods.

second message address information that is indicative of the single slave transceiver being an intended destination of the fourth information; and

Snell in view of Yamano discloses that the second message comprises second message address information that is indicative of the single slave transceiver being an intended destination of the fourth information. *See, e.g.,* Snell at 1:55-57, 2:61-63, 6:35-36, 6:64-66, 7:5-14, Fig. 3; Harris 4064.4 at 14; Yamano at 19:63-64, 20:1-7, 20:54-59, Fig. 8.

For example, Snell discloses transmitting a "second message" including a PLCP preamble and PLCP header, and MPDU data, as shown in Figure 3 below.

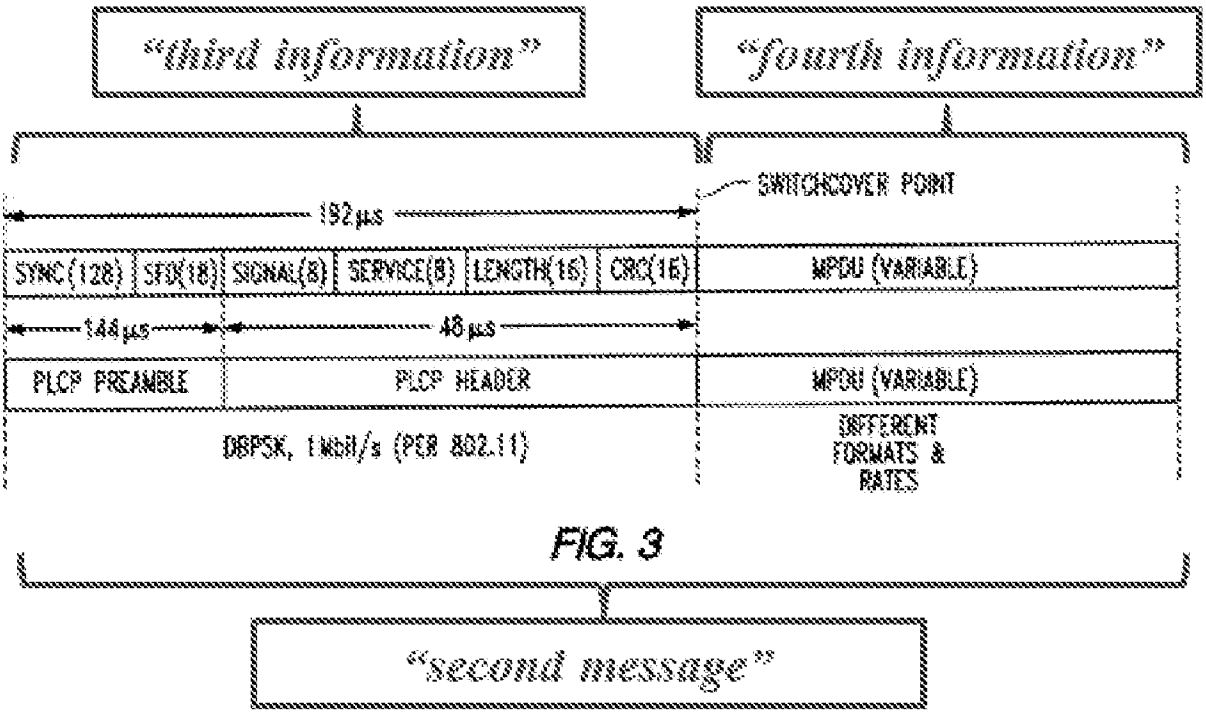


FIG. 3

Snell at Fig. 3 (annotated).

"The modulator may also preferably include header modulator means for modulating *data packets*" Snell at 2:61-63.

"The PRISM 1 chip set provides all the functions necessary for full or half duplex, direct sequence spread spectrum, *packet communications* at the 2.4 to 2.5 GHz ISM radio band." Snell at 1:55-57.

"The *header* may always be BPSK." Snell at 6:35-36.

"The *PLCP preamble and PLCP header* are always at 1 Mbit/s, Diff encoded, scrambled and spread with an 11 chip barker." Snell at 6:64-66.

"*MPDU* is serially provided by Interface 80 and *is the variable data* scrambled for normal operation. The reference phase for the first symbol of the MPDU is the output phase of the last symbol of the header for Diff Encoding. The last symbol of the header into the scrambler 51 must be followed by the first bit of the MPDU. *The variable data* may be modulated and demodulated in different formats than the header portion to thereby increase the data rate, and while a switchover as indicated by the switchover point in FIG. 3, occurs on-the-fly." Snell at 7:5-14.

Snell incorporates by reference Harris 4064.4,[19] which discloses:

"The *preamble and header* are always transmitted as DBPSK waveforms while the *data packets* can be configured to be either DBPSK or DQPSK." Harris 4064.4 at 14.

Yamano discloses that the second message comprises second message address information that is indicative of the single slave transceiver being an intended destination of the fourth information. *See, e.g.,* Yamano at 19:63-64, 20:1-7, 20:54-59, Fig. 8.

For example, Yamano discloses that a packet includes a preamble and main body, and that the preamble can include a destination address.

"Packet 700 includes a *preamble 701* and a *main body 702."* Yamano at 19:63-64.

"For example, *preamble 701* can include information which identifies: (1) a version or type field for the preamble, (2) *packet source and destination addresses,* (3) the line code (i.e., the modem protocol being used), (4) the data rate, (5) error control parameters, (6) packet length and (7) a timing value for the expected reception slot of a subsequent packet." Yamano at 20:1-7 (emphasis added).

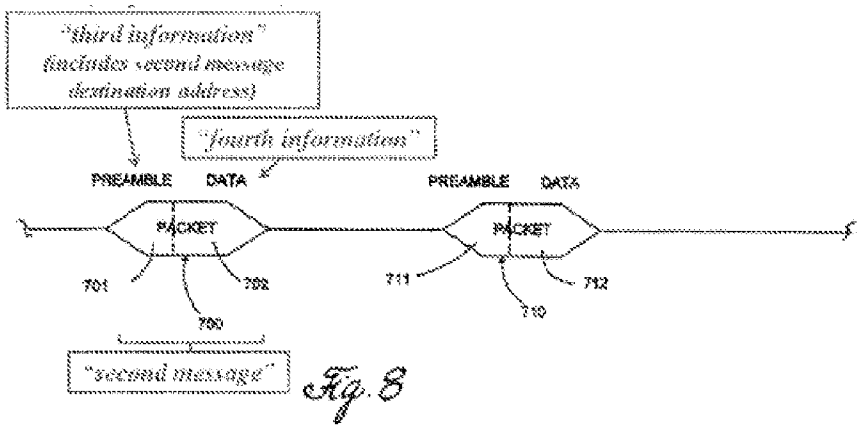


Fig. 8

Yamano at Figure 8 (annotated).

"When the preamble in a burst-mode packet *includes the destination address of the packet,* the receiver circuits can monitor the destination address of the packet, and in response, filter packets which do not need to be demodulated, thereby reducing the processing requirements of the receiver circuits." Yamano at 20:54-59.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Yamano' s teaching of including a destination address in the preamble portion of a data packet in implementing Snell's data packet comprising preamble, header, and MPDU data portions to advantageously specify which receiver the data is intended for and to beneficially reduce the processing requirements at the receiving device, as taught by Yamano. "When the preamble in a burst-mode packet *includes the destination address of the packet,* the receiver circuits can monitor the destination address of the packet, and in response, filter packets which do not need to be demodulated, thereby reducing the processing requirements of the receiver circuits." Yamano at 20:54-59.

In addition, Snell teaches structuring its data packet to include a preamble, header, and MPDU data portion *(see, e.g.,* Snell at 6:35-36, 6:64-66, 7:5-14, Fig. 3), and Yamano teaches structuring its data packet to also include a preamble and data portion, and to place the destination address in the preamble portion (Yamano at 19:63-20:7, Fig. 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a destination address in the preamble portion of a data packet, as taught by Yamano, in implementing Snell's system for transmitting data packets between transceivers, as Snell teaches that its data packet already includes a preamble portion-and in combination, each element (Yamano' s teaching of placing a destination address in the preamble and Snell's teaching of a system for communicating data packets modulated according to different modulation methods between transceivers) performs the same

function as it would separately, yielding nothing more than predictable results. *KSR Int'l Co. v. Teleflex Inc.,* 550 U.S. 398, 417 (2007). One of ordinary skill in art at the time the invention was made would have thus recognized that this combination (yielding the claimed limitation) would have worked as expected. For these reasons, a person of ordinary skill would have been motivated and found it obvious and straightforward to use the teachings of Yamano including a destination address in the preamble of a data packet in implementing Snell's communication system.

wherein the second modulation method results in a higher data rate than the first modulation method.

Snell discloses that the second modulation method results in a higher data rate than the first modulation method. *See, e g.* , Snell at 5:31-33, 6:52-59, 6:64-66, 7:1-2, 7:5-14, Fig. 3; Harris 4064.4 at 16 (Table 7).

For example, Snell discloses that the second modulation method *(e.g.,* QPSK, or alternatively, DQPSK) results in a higher data rate *(e.g.,* 2 Mbit/s) than the first modulation method *(e.g.,* BPSK, or alternatively, DBPSK) which results in a data rate of 1 Mbit/s.
"The present invention provides an extension of the PRISM 1 product from *1 Mbit/s BPSK and 2 Mbit/s QPSK* to 5.5 Mbit/s BPSK and 11 Mbit/s QPSK." Snell at 5:31-33

"The PLCP preamble and PLCP header are always at *1 Mbit/s,* Diff encoded, scrambled and spread with an 11 chip barker." Snell at 6:64-66.

"Now relating to the PLCP header 91, the SIGNAL is:

0Ah	1 Mbit/s BPSK,
14h	2 Mbit/S QPSK,
37h	5.5 Mbit/s BPSK, and
6Eh	11 Mbit/s QPSK.

"

Snell at 6:52-59

"SIGNAL is indicated by 2 control bits and then formatted as described." Snell at 7:1-2.

"MPDU is serially provided by Interface 80 and is the variable data scrambled for normal operation. The reference phase for the first symbol of the MPDU is the output phase of the last symbol of the header for Diff Encoding. The last symbol of the header into the scrambler 51 must be followed by the first bit of the MPDU. The variable data may be modulated and demodulated in different formats than the header portion to thereby increase the data rate, and while a switchover as indicated by the switchover point in FIG. 3, occurs on-the-fly." Snell at 7:5-14. *See also, e.g.,* Snell at Fig. 3; Harris 4064.421 at 16 (Table 7).

21. The master communication device as in claim 1, wherein the first information that is included in the first message comprises the first message address data.

Snell modified in view of Harris 4064.4, in view of Applicants admitted prior art (APA) , in view of Upender, in view of Yamano and further in view of Kamerman as recited above disclose that the first information that is included in the first message comprises the first message address as indicated in the rejection of claim 1 above with reference to the first message address of the destination, therefore the first message address data is included in the actual message when transmitted by the master to the slave transceiver.

Yamano expressly teaches that including a destination address in the preamble portion of the data packet, which precedes the data portion, will advantageously reduce processing requirements of receiving devices because the receiving device can filter out packets which it does not need to demodulate. Yamano at 20:54-59 ("When the preamble in a burst-mode packet *includes the destination address of the packet*, the receiver circuits can monitor the destination address of the packet, and in response, filter packets which do not need to be demodulated, thereby reducing the processing requirements of the receiver circuits.").

VII. RESPONSE TO ARGUMENTS

Patent Owner Argues:

I. The Office has not identified a substantial new question of patentability ("SNQ") because the art identified in its alleged SNQs (and relied on to support its grounds of rejection) is cumulative to art previously presented in a number of the IPRs challenging the '228 Patent and fully considered by the PTAB and during prosecution of the '228 Patent. *See infra* at § II.A.; Akl, at Paragraphs 41-70, asserting that Snell (including Harris AN9614), Yamano and Kamerman, are cumulative to Boer, APA, and Siwiak.

The arguments have been considered but are not persuasive.

In summary, it is only necessary that the prior art or publication raise an SNQ for at least one claim. See MPEP 2242. As noted in the October 2016 Decision on Request (Order), the references were newly cited and/or viewed in a new light and raised an SNQ for at least claim 21. Accordingly reexamination was ordered. For support the Examiner notes the following:

The SNQ was determined with respect to claim 21 which by dependency includes all limitations of claim 1 from which claim 21 depends, taking into consideration the written decision and explanation from the board in not instituting a review of claim 21. Yamano was considered to show the placing of a message address data (information) in a header of a message, such was related to the comment made in IPR 2014 00892 (IPR892) with

respect to the petitioners proposal failing to convince the board that the rejection would prevail on claim 21.

The ex parte reexamination statute sets forth the universe of references that can be used to raise a SNQ [35 U.S.C. § 303(a) (patents and printed publications)]. In addition to a newly-discovered reference, a previously applied reference can raise a SNQ if the previously applied reference is presented in a "new light". Section 303(a) makes this explicit — "[t]he existence of a substantial new question of patentability is not precluded by the fact that a patent or printed publication was previously cited by or to the PTO or considered by the PTO."

Considering Yamano alone or in combination with previously cited references was proper as during original prosecution the reference was not reviewed with "any reasonably detailed analysis," nor was it applied as a principal prior art reference, nor was the issue forming the basis of rejection during reexamination the same as that examined during original prosecution. Thus the reference was not "old" art and raised a valid SNQ.

It is not enough for a reference to be "new," the reference must also be non-cumulative to the technological teachings previously considered by the PTO during prosecution. Therefore, even a newly discovered reference may not raise a SNQ if the reference merely is cumulative to similar prior art already fully considered by the PTO in a previous examination (and previous reexaminations) [MPEP § 2242]. This is an important point when determining whether to file a reexamination request or what references to use. In the instant proceeding, the Yamano reference was not deemed cumulative to any art considered and thus the combinations with previously cited art was considered as being in a new light. Siwiak was not deemed cumulative as the reference was not considered on the merits during a review by the board (555 IPR, paper 20, page 6), nor during prosecution of the application which became the '228 patent. The prosecution history shows no discussion of Siwiak of record in the 13/198,568 application, the reference was merely cited without discussion on the merits of such document with respect to a particular claim.

In re Swanson provides some guidance on what constitutes a "new light" for old art. For example, an SNQ based on previously applied art could arise because the examiner in the original examination misunderstood the actual technical teaching, because the examiner failed to consider a portion of the reference that contained the now cited teaching, or if the examiner applied the reference to a different limitation or claim than the reference is currently being applied. But a reference does not raise an SNQ if the examiner in the original examination understood the actual technical teaching, but got it "wrong" in the rejection. This is a subtle but critical distinction.

In IPR 2014-00892 (IPR 892) the board with respect to claim 21, indicated petitioner had not convinced the board such a rejection would prevail, the proposed rejection had not

addressed reasoning why one of ordinary skill would place "message address data" (see C.2/L.36 of the '228 patent via amendment filed October 19, 2012 amending paragraph 8 of the specification, adding claim 42 (patent claim 21)) in the message header of the primary reference as proposed by petitioner. The decision noted "the Petition's "conclusory allegation of design choice does not provide the required articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." (IPR2014-00892, Pap. 8 at 14-15 (IPR 892 Decision)). The IPR892 decision by the board considered the petitioners proposed rejection did not show the placement of address data in the message header as so addressed by petitioner with respect to claim 21 (page 14, IPR 892 Decision). Boer in view of APA was however determined to adequately teach including "message address information" (claim 1, amendment filed February 5, 2013) in the first message of Boer via Boer 6:28-31 ("The C-MST 132 determines if an incoming message is addressed to its own station, using a destination address included in the DATA field 214 of the MESSAGE 200 (FIGURE 4 of Boer).

The Order granting the Request for reexamination considered Yamano new in light of Yamano teaching placing the 'header with address' which was as noted in the decision above, and therefore also not cumulative to the cited art nor the Siwiak reference (IPR 2014 -00555). Combinations with Yamano were considered new for teaching placing an address in the header.

II. The Office has not identified any SNQ to support its § 102(e) rejection or its rejection "A" under § 103(a), and thus these rejections are *ultra vires* and must be withdrawn for this reason alone, as only new questions are subject to reexamination. *See infra* at § II.B.

The argument has been considered but is not persuasive. The patent owner argument is not relevant to a 102 rejection. The presence or absence of an SNQ is a criteria applied only to determine whether or not a reasonable examiner would consider the references pertinent and thus order reexamination. See MPEP 2242. The statutes applied by the Examiner in the first office action are chosen to most clearly and completely address the patentability of the claims. MPEP 2262. In the instant situation the Patent Owner appears to be arguing that the Examiner does not have the authority to apply rejections not recited in the request, the argument is not relevant: regardless that an SNQ was not identified directly with respect to rejections under 102(e) (section V. Office action) and the 103 rejection based on Boer/APA/Yamano (section VI. A. of Office action)...it is not improper to provide a rejection which is not proposed in a request in considering MPEP 2258.01.

> **2258.01 Use of Previously Cited/Considered Art in Rejections**
> **In the examining stage of a reexamination proceeding, the examiner will consider whether the claims are subject to rejection based on art**. Before making such a rejection, the examiner should check the patent's file history to ascertain whether the art that will provide the basis for the rejection was previously cited/considered in an earlier concluded Office examination of the patent (e.g., in the examination of the application for the patent). For the sake of

expediency, such art is referred to as "old art" throughout, since the term "old art" was coined by the Federal Circuit in its decision of *In re Hiniker*, 150 F.3d 1362, 1365-66, 47 USPQ2d 1523, 1526 (Fed. Cir. 1998).
If the rejection to be made by the examiner will be based on a combination of "old art" and art newly cited during the reexamination proceeding, the rejection is proper, and should be made. See *In re Hiniker*, 150 F.3d at 1367, 47 USPQ2d at 1527.

III. The multiple alleged reasonable claim constructions compel a finding of indefiniteness and termination of the reexamination proceeding. *See infra* at§ III. (Page 46 Remarks)

No indefinite-ness rejection is of record in the office action, the office action merely provides explanation of reasonable interpretations for each rejection. The Office is required by statute, case law, and the MPEP to utilize the "broadest reasonable interpretation consistent with the specification" standard during reexamination proceedings.

37 CFR 1.555(b) states:

A prima facie case of unpatentability of a claim pending in a reexamination proceeding is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

Note also MPEP 2111 states:

During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." The Federal Circuit's en banc decision in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316, 75 USPQ2d 1321, 1329 (Fed. Cir. 2005) expressly recognized that the USPTO employs the "broadest reasonable interpretation" standard:
The Patent and Trademark Office ("PTO") determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364[, 70 USPQ2d 1827, 1830] (Fed. Cir. 2004). Indeed, the rules of the PTO require that application claims must "conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description." 37 CFR 1.75(d)(1).

See also *In re Suitco Surface, Inc.*, 603 F.3d 1255, 1259, 94 USPQ2d 1640, 1643 (Fed. Cir. 2010); *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000).

Because applicant has the opportunity to amend the claims during prosecution, giving a claim its broadest reasonable interpretation will reduce the possibility that the claim, once issued, will be interpreted more broadly than is justified. *In re Yamamoto,* 740 F.2d 1569, 1571 (Fed. Cir. 1984); *In re Zletz,* 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow."); *In re Prater,* 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969)

See further response to the remarks directed toward claim construction in section IV. below.

IV. (Page 50 Remarks) The Office has not based its rejections on the broadest *reasonable* claim construction and thus has not identified where in the cited art a number of the claim limitations, when properly construed, are disclosed or suggested. *See infra* at§ IV; Akl, at Paragraphs 18-27.

The Examiners disagree. In summary, as noted in the May 2017 Non Final Action, for each of the examined claims the claim language is written in bold and the Examiner's interpretations are written directly after the language with citations to the sections of the prior art and the interpretation of the language onto the prior art. For example in the May 2017 Non Final Action, p. 14, the Examiner sates the BRI of "data intended for one of the one or more slave transceivers" can reasonably be interpreted as "PLCP headers."

The 102(e) single means claim rejection which ignores all claim limitations which were suggested as intended use, has been withdrawn upon further consideration.

Ex parte Schulhauser, Appeal 2013-007847 (PTAB April 28, 2016), precedential provides that if a condition precedent in a **method claim** is not met, the conditional steps recited in the claim are not required to be performed. As such, **the broadest reasonable interpretation of such a method claim does not include the conditional steps**. Therefore, the conditional steps in a method need not be found in the prior art in order to deny patentability of a method claim. In contrast, if the same steps are part of a system claim having a programmed processor performing the steps, the system claim is interpreted more narrowly to include all of the steps. The Board reasoned that since there is a structure (i.e., a processor) tied to the steps in a system claim, the structure is present in the system regardless of whether the condition is met and the conditional function is actually performed.

The broadest reasonable interpretation of a system claim having structure that performs a function, which only needs to occur if a condition precedent is met, still requires structure for performing the function should the condition occur. This interpretation of the system

claim differs from the method claim because the structure (i.e., a processor programmed to perform an algorithm for carrying out the recited function should the recited condition be met) is present in the system regardless of whether the condition is met and the function is actually performed. See also 2111.04 Contingent Limitations

The term "configured to" is used to describe programming or structure required to perform a specified function, it cannot be ignored by the Examiner when applying the prior art. The subject matter of claim 21 (including the limitations of claim 1) is an apparatus claim and does recite the transmitting and modulating in positive tense, not in a conditional or optional manner. In this apparatus claim, the transceiver is not recited as optionally transmitting if a condition is met but rather states the transceiver is configured to transmit (positively does transmit) and the first information is modulated (positively is modulated), the wherein clause is also not just merely stating an inherent result but gives purpose to the limitations in the claim, the second modulation method is used in the transmitted modulated second message.

With respect to patent owners remarks directed toward the **prosecution history and federal circuit claim construction**, during examination the prosecution history is entitled to little weight under the broadest reasonable interpretation standard. See *Tempo Lighting, Inc. v. Tivoli, LLC*, 742 F.3d 973, 978 (Fed. Cir. 2014) ("This court also observes that the PTO is under no obligation to accept a claim construction proffered as a prosecution history disclaimer, which generally only binds the patent owner.").

The Patent Owner asserts that the Office's refusal to recognize and utilize the claim construction as affirmed by the Federal Circuit is contrary to law. As noted above, the Examiner is required by law to perform the instant Reexamination according to the "broadest reasonable interpretation consistent with the specification." Furthermore, the patent owner's general statement that the Federal Circuit "affirmed" the claim constructions is repeated many times throughout the Amendment and throughout the Akl Declaration. However, *Markman v Westview Instruments*, stated "[w]hen a court construes the claims of the patent, it 'is as if the construction fixed by the court had been incorporated in the specification.'" The Federal Circuit dismissed such an argument stating:

> Markman involved an infringement suit in the district court. This is a distinction with a difference. Patents in infringement suits are presumed valid by statute. 35 USC 282 (1994). No such presumption attaches before the PTO. It is the PTO's duty to assure that the statutory requirements for patentability are met....It would be inconsistent with the role assigned to the PTO in issuing a patent to require it to interpret claims in the same manner as judges who, post issuance, operate under the assumption that the patent is valid.

See also *In re Morris,* 127 F.3d 1048,1054-55, 44 USPQ2d 1023,1027-28 (Fed. Cir. 1997) (The court held that the PTO is not required, in the course of prosecution, to

interpret claims in applications in the same manner as a court would interpret claims in an infringement suit. Rather, the PTO applies to verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, **taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in applicant's specification**.").

With respect to the ***modulation methods***; Claims 43-46 of the '288 disclosure recite that different modulation methods correspond to for example phase modulation, amplitude modulation, quadrature amplitude modulation, discrete multi-tone modulation. Claims 43-46 also indicate "at least one of" the first or second methods is the named modulation type in the respective claim 43-46. Considering 'at least one' includes not only 'one' but also 'both of the first and second modulation methods', it is clear from this portion of the prosecution history and disclosure including the claims that patent owner intended one or both of the first and second modulation methods to reasonably be considered as a variant of phase modulation, or quadrature modulation, or quadrature amplitude modulation, or discrete multi-tone modulation. As such, two different variants of for example phase modulation such as the QPSK and BPSK taught by the art relied on in the rejections is a reasonable interpretation of different type of modulation methods and is consistent with the disclosure of the '288 patent.

Also, in considering the specification description of the instant '228 patent under reexamination, the description provides modulation methods as including for example, QAM and CAP, which are based on 'amplitude modulation', (C2/L1-10) thus the description suggests it would be reasonable to consider 'variations' of amplitude modulations as being of different modulation methods. The claim does not recite the particular modulation method nor are variants of modulation 'families' excluded by the language of the claim or specification description.

Such a "broadest reasonable interpretation consistent with the specification" is further required in Reexamination proceedings as well. Note 2258(G) states:

Original patent claims will be examined only on the basis of prior art patents or printed publications applied under the appropriate parts of 35 U.S.C. 102 and 103. See MPEP § 2217....During reexamination... claims are given the broadest reasonable interpretation consistent with the specification and limitations in the specification are not read into the claims (*In re Yamamoto*, 740 F.2d 1569, 222 USPQ 934 (Fed. Cir. 1984)).

Thus, the "'broadest reasonable construction' rule applies to reexaminations as well as initial examinations", where "construing claims broadly during prosecution is not unfair to the applicant...because the applicant has the opportunity to amend the claims to obtain more precise claim coverage." *In re American Academy of Science Tech Center,* 70 USPQ2d 1827, 1830, 367 F3d 1359, 1364 (Fed. Cir. 2004).25 "[I]t is important that or the district court and the PTO can consider different evidence....

[accordingly, different results between the two forums may be entirely reasonable....[a]nd, if the district court determines a patent is not invalid, the PTO should continue its reexamination because, of course, the two forums have different standards of proof for determining invalidity. *Ethicon Inc. v. Quigg*, 849 F.2d 1422, 1428-9, 7 USPQ2d 1152, 1157 (Fed. Cir. 1988).

"Finally, American Academy points to an inconsistency between the Board's construction of the term "user computer" and that of the district court in American Academy's litigation against Novell. In the district court litigation, the court construed "user computer" to refer to a computer that serves one user at a time. However, the Board is required to use a different standard for construing claims than that used by district courts. We have held that it is error for the Board to "appl[y] the mode of claim interpretation that is used by courts in litigation, when interpreting the claims of issued patents in connection with determinations of infringement and validity." *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989); accord *In re Morris*, 127 F.3d 1048,1054 (Fed. Cir. 1997) fit would be inconsistent with the role assigned to the PTO in issuing a patent to require it to interpret claims in the same manner as judges who, post-issuance, operate under the assumption the patent is valid."). Instead, as we explained above, the PTO is obligated to give claims their broadest reasonable interpretation during examination. Under that standard, it was proper for the Board to construe "user computer" to encompass the mainframes and minicomputers of the cited prior art." Id.

The litigation history shows patent owner considered "variants" of one 'family' of modulation methods as 'at least two types of modulation methods' because (Bluetooth EDR uses variants of PSK modulation).

See Case No. 2:13-cv-00213 THIRD AMENDED COMPLAINT FOR PATENT INFRINGEMENT (Paragraphs 14 and 21) therein:

> ...[t]he infringing acts include, but are not limited to, the manufacture, use, sale, importation, and/or offer for sale of products practicing the following Bluetooth standards: Version 2.0 + EDR, Version 2.1 + EDR, Version 3.0 + HS, Version 4.0, and Version 4.1 ("Bluetooth Standards"). **Each of these Bluetooth Standards supports Enhanced Data Rate ("EDR") mode, thereby using at least two modulation methods.**

With respect to **the Master/Slave** interpretation: Patent Owner suggests the 'master' in the master/slave network requires the device to function in a multi-point architecture (such as would also be known in the art as an 'access point'). A multi-point architecture is described in the '228 patent C.1/L58-60, however, claim 2 of the '228 patent further limits claim 1 to be of a multi-point architecture, therefore it would not be unreasonable to interpret the master device of claim 1 as merely one of at least two devices clustered together such as in an in ad-hoc network where the device which initiates the communication is the 'controlling' device which merely requests response from another device (slave), and is thus designated a 'master'. Claims 1 and 21 do not recite a multi-

point architecture. Applicant argues definition of "**master**" as being limited to: In the context of wireless protocols, this refers to a device that controls the operation of a network. The argument is not persuasive, in the context of the claim language in which the term is applied and which is intended to present the boundaries of the invention, the requirement by the claim language includes only that a "master"...communicates with at least a single slave transceiver, the claim does not require any more than one other 'slave' device in its communication functions. The 'slave' device' is deemed a slave in the claim in accordance with the requirement that the slave responds to the master. Furthermore, the APA was deemed appropriate to teach the Master Slave feature in IPR892, and the portions of the Harris AN9614 teaching document relied on the rejections clearly show the master 'controls' by at least …'instructing' the radio (client/slave/) … in "either mode" … as to when to listen and for how long (control) …and to "respond to the poll".

> [T]he controller can keep adequate time to operate **either a polled or a time allocated scheme. In these modes**, the radio is powered off most of the time and only awakens when communications is expected. This station would be awakened periodically to listen for a beacon transmission. **The beacon serves to reset the timing and to alert the radio** to traffic. If traffic is waiting, the **radio is instructed when to listen and for how long**. In a polled scheme, the remote radio can **respond to the poll** with its traffic if it has any... Harris AN9614 at 3. [emphasis added].

V. Harris AN9614 and Harris 4064.4 (collectively "Harris Documents") are not prior art and therefore could not be incorporated by reference into Snell or used as references against the '228 Patent, as their earliest publication date in the record is the date Snell issued as a patent, *i.e.*, November 9, 1999 (after the '228 priority date of December 5, 1997). *See infra* at§ VI.A.-C; Akl, at 71-77.

The argument is not persuasive, the 'Harris documents' were supplied in the file of the Snell application by the applicants of the Snell patent before the Snell application issued as a patent, the documents were received in the Snell application on March 17, 1997. Snell is a 102(e) reference for examination purposes. Each of the Harris AN9614 and Harris file no 4064.4 incorporated by reference are included in the Snell application papers. Harris File no. 4063.4 listed as 'other publication' on Snell is also of record in the Snell application file. A reissue application 10/005,483 of Snell '807 also included the Harris Documents as listed under "other publications" in Snell '807. The documents each have a copyright date 1996. Snell specifically recites the literature by title as incorporated by reference and refers to 'the publication'. A public availability notice is found on the File number 4064.4 page 3, which indicates:

> "For additional information on the PRISM chip set, call 724-7800 to access Harris' AnswerFAX system. When prompted, key in the four-digit document number (File #) of the datasheets you wish to receive. The four-digit file numbers are shown in Typical Application Diagram, and correspond to the appropriate circuit" ,

showing that the documents whose file numbers are found on the data sheets were available to the interested public and especially those persons concerned with the art, such as those attempting to use the Harris chip set to which the documents apply.

Also see MPEP 2128.02 in accordance with the notice of routine practice noted above.

> 2128.02 Date Publication Is Available as a Reference
> I. DATE OF ACCESSIBILITY CAN BE SHOWN THROUGH EVIDENCE OF ROUTINE BUSINESS PRACTICES
> Evidence showing routine business practices can be used to establish the date on which a publication became accessible to the public. Specific evidence showing when the specific document actually became available is not always necessary. *Constant v. Advanced Micro-Devices,Inc.,* 848 F.2d 1560, 7 USPQ2d 1057 (Fed. Cir.), *cert. denied,* 988 U.S. 892 (1988) (Court held that evidence submitted by Intel regarding undated specification sheets showing how the company usually treated such specification sheets was enough to show that the sheets were accessible by the public before the critical date.); *In re Hall,* 781 F.2d 897, 228 USPQ 453 (Fed. Cir. 1986) (Librarian's affidavit establishing normal time frame and practice for indexing, cataloging and shelving doctoral theses established that the thesis in question would have been accessible by the public before the critical date.).

The Harris documents are all publicly available to those with interest of such documents prior to the earliest suggested priority date of December 5, 1997. The '228 patent claims continuity to the '8,023,580 patent as well as the 6,614,838 patent among others and as such should recite identical specifications less the reference to continuity data. The '228 patent application (13/198,568) contains an amendment amending the specification of the '228 patent (see C.2/L.36 of the '228 patent via amendment filed October 19, 2012 amending paragraph 8 of the specification, adding claim 42 (patent claim 21)).

VI. The material Snell attempted to incorporate by reference <u>is not the material the Office now relies on</u> to support its rejections. Thus, even assuming portions of the Harris Documents were legally incorporated by reference, the <u>specific material</u> the Office is relying on was not incorporated by reference. *See infra* at§ VI.D.; Akl, at Para 71-77.

In order to reduce issues related to the content of files which are incorporated into Snell and listed as other publications, the remaining rejections including the Harris documents rely on such documents for secondary teachings which are at the least especially relevant to Snell because Snell specifically points to each such document in the Snell disclosure and further directs the subject matter of the Snell invention directly to the subject matter of the incorporated and disclosed documents. The essential subject matter of a claimed invention must be pointed out, the references are incorporated into the Snell patent, the claims of Snell are not relied on in the rejection, the patent is assumed valid for examination purposes.

VII. The alleged Admitted Prior Art cannot serve as a basis for rejecting claim 21 *(e.g.,* because it is not the work of another). *See infra* at§ VII.

The argument is not persuasive, the evidence of record supports that the features of the APA relied on in the rejections are by another. For example the '228 Patent states that the teachings are known in the art, the Admitted Prior Art (APA) was considered proper for teaching certain aspects well known in the art via reference to IPR 892 and multiple other Inter parte reviews on various claims of the '228 patent and '580 patent. The concept of master slave is well known prior art used in Wireless LAN wherein an access point is a 'master' to devices connected thereto to form an infrastructure network.

VIII. The Anticipation Rejection is improper because the art relied on to support it does not disclose the claimed (i) master/slave relationship, (ii) the two different types of modulation methods, or (iii) the first and second messages. *See infra* at § VIII; Akl, at Para 78-123.

The argument is moot – the anticipation rejection based on **intended use** is withdrawn, see the response to arguments of section IV above.

However, with respect to the arguments directed to terms at issue with patent owner and requester, in addition to the response to remarks in section IV. above,

(i) the **master slave** relationship;

the master/slave relationship is disclosed by Snell in at least use of master (access point) transceiver to communicate with other wireless transceivers on a wireless LAN, and was also well known as evidenced by the APA and as noted in the May 2017 Non Final Action, for example at p. 11, Snell is disclosing a "polled protocol," in an 802.11 LAN; and

(ii) the **different modulation** types;

With respect to patent owners intentions suggested via the prosecution history, the prosecution history is entitled to little weight under the broadest reasonable interpretation standard. See *Tempo Lighting, Inc. v. Tivoli, LLC,* 742 F.3d 973, 978 (Fed. Cir. 2014) ("This court also observes that the PTO is under no obligation to accept a claim construction proffered as a prosecution history disclaimer, which generally only binds the patent owner.").

Considering claims 43-46 of the '288 disclosure recite that different modulation methods correspond to for example Phase modulation, amplitude modulation, quadrature amplitude modulation, discrete multi-tone modulation. These claims indicate "at least one of" the first and second methods is the named modulation type in the respective claim. Considering 'at least one' includes not only 'one' but also "both" the first and second modulation methods, it is clear that patent owner intended both the first and second modulation methods to reasonably be considered as different variants (types) of phase modulation, or quadrature modulation, or quadrature amplitude modulation, or discrete

multitone modulation. As such, two different variations (types) of, for example, phase modulation such as the QPSK and BPSK taught by the art relied on in the rejections is a reasonable interpretation for different types of modulation methods as claimed and is consistent with the disclosure of the '288 patent and the finding by the board in the IPR892 decision.

Also, in considering the specification description of the instant '228 patent under reexamination, the description provides modulation methods as including for example, QAM and CAP, which are based on 'amplitude modulation', (C2/L1-10) thus the description suggests it would be reasonable to consider 'variations' of amplitude modulations as being of different modulation methods. The claim does not recite the particular modulation method nor are variants of modulation 'families' excluded by the language of the claim or specification description.

Furthermore, the litigation history contradicts the suggested modulation methods being tied to different families as suggested being the sole intent of different modulation methods in that patent owner previously considered "variants" of one family of modulation methods as 'at least two types of modulation methods (Bluetooth EDR uses variants of PSK modulation). See Case No. 2:13-cv-00213 THIRD AMENDED COMPLAINT FOR PATENT INFRINGEMENT Paragraphs 14 and 21.

> ...[t]he infringing acts include, but are not limited to, the manufacture, use, sale, importation, and/or offer for sale of products practicing the following Bluetooth standards: Version 2.0 + EDR, Version 2.1 + EDR, Version 3.0 + HS, Version 4.0, and Version 4.1 ("Bluetooth Standards"). **Each of these Bluetooth Standards supports Enhanced Data Rate ("EDR") mode, thereby using at least two modulation methods**.

Further, with respect to the patent owners suggested reliance on prosecution history of parent applications related to the file of the '228 patent, the '228 patent corresponds to application 13/198,568 filed August 4, 2011 as a continuation application of 12/543,910, the prosecution history of the parent application 12/543,910 is not of record in the 13/198,568 application as the instant application is not a file wrapper continuation of 12/543,910. The '228 patent application (13/198,568) contains a unique amendment amending the specification of the application corresponding to the '228 patent (see C.2/L.36 of the '228 patent via amendment filed October 19, 2012 amending paragraph 8 of the specification, adding claim 42 (patent claim 21)). Such amendment does not appear to be of record in each of the other patents related by continuity.

(iii) the first and second messages are clearly taught by a sequence of messages with a defined format, common operational functioning of devices connected in a network requires sequences of messages in order to communicate on the network.

IX. All of the rejections based on § 103(a) are improper because one of ordinary skill in the art would not have adapted/combined the references as the Office proposes for at least the

following reasons: (i) the peer-to-peer systems of Boer and Snell are fundamentally different than the claimed master/slave system; (ii) the "polled scheme" of Harris AN9614 was in the context of a single low data rate scheme as opposed to Snell's relied-on higher data rate scheme; (iii) Upender would have discouraged adapting Snell or Boer to a master/slave system; and (iv) the problem identified and solved by Gordon Bremer was not recognized in the cited prior art. See infra at § V & IX.A; Akl, at 78-99, 124-79.

The argument has been considered but is not persuasive. The Patent Owner argument suggests the references cannot be constructively combined, however, "[t]he test for obviousness is not whether the features of a secondary references may be bodily incorporated into the structure of the primary reference.... Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art." In re Keller, 642 F.2d 413, 425 (CCPA 1981).

The Boer/APA rejection was deemed to render claim 1 unpatentable in IPR892, therefore the master slave functionality of such system is clear, the decision was made final, claim 1 was canceled. Snell is a master slave system merely even by virtue of the transceiver being referenced as an access point for transmitting between local area devices to wired network as per the background of the Snell disclosure. Snell is also argued by patent owner as being substantially similar to Boer, therefore the adaptation of Snell to function as a master slave system if not explicitly already considered to teach a master slave system by virtue of the suggested utilization of the transceiver as an access point, would have been an expected use of the Snell system as evidenced by the use of the disclosed and incorporated processing circuitry which is explicitly recited as including polling. Snell utilizes the Harris Prism Chipset, the documents referenced by Snell explicitly teach use of such chip in a master slave environment with reference to the paragraph reading:

> [T]he controller can keep adequate time to operate **either a polled or a time allocated scheme. In these modes**, the radio is powered off most of the time and only awakens when communications is expected. This station would be awakened periodically to listen for a beacon transmission. The **beacon serves to reset the timing and to alert the radio to traffic. If traffic is waiting, the radio is instructed when to listen and for how long.** In a **polled scheme**, the remote radio can **respond to the poll** with its traffic if it has any. With these techniques, the average power consumption of the radio can be reduced by more than an order of magnitude while meeting all data transfer objectives.

Thus the Harris document provides clear exemplary language of master/slave relation as required by the claim language and argued in the remarks which suggest the master controls, which is shown in Harris by the 'instructing' the radio (client/slave/) which occurs … in "either mode" and further controlling … 'as to when to listen and for how long' … as well as in the radio being controlled to "respond to the poll".

With respect to the claimed master slave system being different from the peer to peer systems, APA was deemed to teach use as a master slave system, further, claim 1 is not limited to a multipoint network as importing such limitation into claim 1 would be unduly limiting in considering the further limiting feature of claim 2. Upender was deemed appropriate to provide motivation for modifying a system to function as a master slave system in IPR 892.

The problem recognized, as argued by the patent owner, is not required by claim limitations of claim 1 and 21 alone, the rejection is only required to teach the limitations of each claim which the specific rejection is applied to. Nonetheless the variable data rates of the receiving devices is well established in each reference relied on in the rejection though the claims are not specific to what constitutes higher and lower differing data rates.

X. All of the rejections based on § 103(a) also are improper because one of ordinary skill in the art would not have adapted Boer or Snell to a master/slave system and then combined it with Yamano as the Office proposes because moving address information from the Data Link Layer to the Physical Layer Preamble would have resulted in an inoperable system and removed error detection functionality with respect to the address value. In addition, the skilled artisan would have recognized that doing so would have been a "serious design blunder." ***See infra*** **at§ IX.B.; Akl, at PP 78-99, 124-79.**

The argument with respect to Boer/APA and Snell is not persuasive. The Patent Owner argument suggests the references cannot be constructively combined, however, "[t]he test for obviousness is not whether the features of a secondary references may be bodily incorporated into the structure of the primary reference.... Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art." In re Keller, 642 F.2d 413, 425 (CCPA 1981).

IPR 892 found claim 1 unpatentable in view of Boer and APA. Claim 1 recites the first message ...includes '**message address information**', therefore Boer and APA teach the message address information of claim 1, the decision was final, claim 1 was canceled. The board noted the petitioner had not addressed reasoning why one of ordinary skill would place "**the message address data**" in claim 21, of the first message in claim 1, in a message header of the primary reference applied to claim 1. The claim limitations of claim 21 do not require the placing of such 'address data' in a header of the claimed first message ('address data' is referenced in 2:36 of the '228 patent via amendment filed October 19, 2012 amending paragraph 8 of the specification, adding claim 42 (patent claim 21)). Claim 21 requires the first message to include the first message address data. Yamano teaches placing message address data in a preamble of a header, the preamble portion of the data packet, which precedes the data portion. The Yamano data packet (message) is not broken down in illustration as far as the Boer/APA or Snell message packet in that Yamano shows the packet includes the preamble portion and data portion. One of ordinary skill in the art would know that the address data in the Yamano preamble

portion could not replace the required data of the PLCP preamble in each preamble portion of the message in either Boer or Snell as such a portion of the message packet in either is reserved for specific use as noted by applicants arguments and similarly in the file no. 4064.4 data sheets. Modification of Boer or Snell in combination with Yamano would not require to move the message address information (claimed as being in the first message) or message address data (of the message address information of claim 1) to the physical layer or PLCP, nor does the claim 21 limitation require such placement. Boer taught the header portion as 218 in figure 4, including 206, 208, 210, 212, that header was modulated in a first format, that header portion is part of 'first message information' in the rejection, movement of any 'message address data' if required would be from the payload portion 214 of the message of Boer for the very reason Yamano stated in the rejection above. *"Packet 700* includes a *preamble 701* and a *main body 702."* Yamano at 19:63-64. ...preamble precedes the main body (the body containing the payload data), as shown in Figure 8. Yamano teaches that the first message comprises first message address information that is indicative of the one of the one or more slave transceivers being an intended destination of the second information. *See, e.g.,* Yamano at 19:63-64, 20:1-7, 20:54-59, Fig. 8. Yamano expressly teaches that including a destination address in the preamble portion of the data packet, which precedes the data portion**,** will advantageously reduce processing requirements of receiving devices because the receiving device can filter out packets which it does not need to demodulate. Yamano at 20:54-59 ("When the preamble in a burst-mode packet *includes the destination address of the packet,* the receiver circuits can monitor the destination address of the packet, and in response, filter packets which do not need to be demodulated, thereby reducing the processing requirements of the receiver circuits."). (Yamano at 19:63-20:7, Fig. 8).

XI. Further, all of the rejections based on § 103(a) are improper because one of ordinary skill in the art would not have adapted Boer or Snell to a master/slave system and then combined it with Yamano as the Office proposes because adding a destination address to the preamble of Snell or Boer would have frustrated their goals of increasing the data rate and remaining compliant with IEEE 802.11. *See infra* at§ IX.B.; Akl, at PP 78-99, 124-79.

The Patent Owner argument suggests the references cannot be constructively combined, however, "[t]he test for obviousness is not whether the features of a secondary references may be bodily incorporated into the structure of the primary reference.... Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art." In re Keller, 642 F.2d 413, 425 (CCPA 1981).

The response addressing arguments in section X. directly above are also applicable to the remarks in this section XI., the destination address is not moved to the physical layer preamble of Boer or Snell for reasons noted in the remarks addressing section X. above, and the goals of increasing data rate are not claimed nor is compliance with 802.11 standards, nonetheless one of ordinary skill would know that the address data in the Yamano preamble portion could not replace the required data of the PLCP preamble in each preamble portion of the message in either Boer or Snell as such a portion of the message packet in either is reserved for specific use as noted by applicants arguments and

similarly in the file no. 4064.4 data sheets. Yamano teaches 'the first message address data' is included in the first message, the rejections make clear that it would be obvious to include the address data as well as the address information which is already included in the first message of claim 1.

XII. Rejection A is improper because it would not have been obvious to (i) adapt Boer to a master/slave system, or (ii) move destination address data to the preamble of Boer. Rejection A is additionally improper because (1) the Office relies improperly on portions of the '228 Patent as disclosing the claimed "master/slave relationship" and (2) the cited references do not disclose and would not have suggested the claimed "the second modulation method [that is] of a different type than the first modulation method." ***See infra*** **at§§ IX & X; Akl, at PP 180-85.**

The Patent Owner argument suggests the references cannot be constructively combined, however, "[t]he test for obviousness is not whether the features of a secondary references may be bodily incorporated into the structure of the primary reference.... Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art." In re Keller, 642 F.2d 413, 425 (CCPA 1981).

The argument with respect to Boer/APA/Yamano is not persuasive. The IPR 892 decision found claim 1 unpatentable in view of Boer and APA. Claim 1 recites the first message ...includes '**message address information**', therefore Boer and APA teach the message address information of claim 1. The rejection had not addressed reasoning why one of ordinary skill would place "**the message address data**" of the first message in claim 1 in a message header of the primary reference. The claim limitations do not require the placing of such 'address data' in a header of the claimed first message ('address data' is referenced in 2:36 of the '228 patent via amendment filed October 19, 2012 amending paragraph 8 of the specification, adding claim 42 (patent claim 21)). Nonetheless Yamano teaches placing message address data in a first message via preamble of a header, the preamble portion of the data packet, which precedes the data portion, and provides motivation for doing so as noted above in response to arguments of section X. The response to arguments section IV. above addresses the manner in which a broadest reasonable interpretation of the master slave relationship and the modulation methods are viewed in the office action rejections.

XIII. Rejections B and C are improper because it would not have been obvious to (i) adapt Snell to a master/slave system, or (ii) move destination address data to the preamble of Snell. Rejections B and C are also improper because the cited references do not disclose and would not have suggested any of the following three claim limitations: (1) the "master/slave relationship," (2) "the second modulation method [that is] of a different type than the first modulation method," and (3) the "first message" and "second message." ***See infra*** **at§§ IX & XI; Akl, at PP 186-206.**

Rejection B was withdrawn in order to reduce redundancy and any issues raised by documentation issues related to incorporation by reference.

The arguments with respect to rejection C. are not persuasive, master slave adaption and the modulation method issues are addressed above in response to remarks sections IV and VIII. The first and second messages are clearly taught by a sequence of messages with defined format, and common operational functioning of devices connected in a network requires sequences of messages in order to communicate on the network.

XIV. Rejection D is improper because it would not have been obvious to (i) adapt Snell to a master/slave system, or (ii) move destination address data to the preamble of Snell. Rejection D is also improper because (1) the Office relies improperly on portions of Harris AN9614 and the '228 Patent as disclosing the claimed "master/slave relationship" and (2) the cited references do not disclose and would not have suggested the claimed "the second modulation method [that is] of a different type than the first modulation method." ***See infra*** **at § § IX & XII; Akl, at PP 207-215.**

The arguments with respect to rejection D. have been considered but are not persuasive.

With respect to the Master Slave relationship (XIV.i.), in addition to comments above, Snell explicitly recites Master Slave operation in as much as the limitations of claim 21 (including 1) require of the Master salve relationship. The claims require the slave to respond to a communication from the master. Snell utilizes the Harris Prism Chipset, the documents referenced by Snell in the Snell disclosure explicitly teach use of such chip in a master slave environment with reference to at least the paragraph reading:

> [T]he controller can keep adequate time to operate **either a polled or a time allocated scheme. In these modes**, the radio is powered off most of the time and only awakens when communications is expected. This station would be awakened periodically to listen for a beacon transmission. The **beacon serves to reset the timing and to alert the radio to traffic. If traffic is waiting, the radio is instructed when to listen and for how long.** In a **polled scheme**, the remote radio can **respond to the poll** with its traffic if it has any. With these techniques, the average power consumption of the radio can be reduced by more than an order of magnitude while meeting all data transfer objectives.

Thus the Harris document teaches that there is clearly a master/slave relationship as required by the claim language and argued in the remarks which suggest the master controls, which is shown in Harris by the 'instructing' the radio (client/slave/) which occurs … in "either mode" and further controlling … 'as to when to listen and for how long' … as well as in the radio being controlled to "respond to the poll".

With respect to the requirement for moving a destination to the preamble of Snell (XIV. ii.), the argument is not persuasive, the claim (21) requires the first message to include

the address information (claim 1) and the address data (claim 21). Yamano teaches inclusion of address data which is address information for particular advantages of reducing processing requirements. The limitations of claim 21 do not require the placing of 'address data' in a header of the claimed first message ('address data' is referenced in 2:36 of the '228 patent via amendment filed October 19, 2012 amending paragraph 8 of the specification, adding claim 42 (patent claim 21)). Yamano teaches placing message address data in a preamble of a header, the preamble portion of the data packet, which precedes the data portion. The Yamano data packet (a first message) is not broken down in illustration as far as the Snell message packet in that Yamano shows the packet includes the preamble portion and data portion. One of ordinary skill in the art would know that the address data in the Yamano preamble portion could not replace the required data of the PLCP preamble in each preamble portion of the message in Snell as such a portion of the message packet in Snell is reserved for specific use as noted similarly in the rejection reciting the fields in Snell and with reference to the same fields in file no. 4064.4 data sheets. Modification of Snell in combination with Yamano would not require to move the message address information (claimed as being in the first message) or message address data (of the message address information of claim 1) to the physical layer or PLCP, nor does the claim 21 limitation require such placement in a header, but rather merely requires to include the message address data in the first message.

With respect to (XIV. 1.), the master/slave relationship is disclosed in at least use of master (access point) transceiver to communicate with other wireless transceivers on a wireless LAN was well known as evidenced by the APA. With respect to **the Master/Slave** interpretation: Patent Owner suggests the 'master' in the master/slave network requires the device to function in a multi-point architecture (such as would also be known in the art as an access point). A multi-point architecture is described in the '228 patent C.1/L58-60, however, claim 2 of the '228 patent further limits claim 1 to be of a multi-point architecture, therefore it would not be unreasonable to interpret the master device of claim 1 as merely one of at least two devices clustered together such as in an in ad-hoc network where the device which initiates the communication is the 'controlling' device which merely requests response from another device (slave), and is thus designated a 'master'. Claim 21 including claim 1 does not recite a multi-point architecture. Applicant argues definition of "**master**" as being limited to: In the context of wireless protocols, this refers to a device that controls the operation of a network. The argument is not persuasive, in the context of the claim language in which the term is applied and which is intended to present the boundaries of the invention, the requirement by the claim language includes only that a "master"...communicates with at least a single slave transceiver, the claim does not require any more than one other 'slave' device in its communication functions. The 'slave' device' is deemed a slave in the claim in accordance with the requirement that the slave responds to the master. Furthermore, the APA was deemed appropriate to teach the Master Slave feature in IPR892, and the portions of the Harris documents relied on the rejection clearly show the master controls …'instructing' the radio (client/slave/) … in "either mode" … as to when to listen and for how long (control) …and to "respond to the poll".

With respect to (XIV. 2.), the reference explicitly recites two 'variants' of PSK modulation and the arguments do not show how the disclosure limits the modulation methods to exclude such an interpretation of modulation methods from including merely different variants of particular modulation. See the response to remarks in section IV above for further explanation of why the office action interpretation is deemed proper in this proceeding.

VIII. Conclusion

Patent owner's Amendment necessitated any new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL. See** MPEP § 706.07(a).

Service of Papers

After the filing of a request for reexamination by a third party requester, any document filed by either the patent owner or the third party requester must be served on the other party (or parties where two or more third party requester proceedings are merged) in the reexamination proceeding in the manner provided in 37 CFR 1.248. See 37 CFR 1.550(f).

Extensions of Time

Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 CFR 1.550(c).

Amendment in Reexamination Proceedings

Patent owner is notified that any proposed amendment to the specification and/or claims in this reexamination proceeding must comply with 37 CFR 1.530(d)-(j), must be formally presented pursuant to 37 CFR 1.52(a) and (b), and must contain any fees required by 37 CFR 1.20(c).

Submissions

In order to insure full consideration of any amendments, affidavits or declarations or other documents as evidence of patentability, such documents must be submitted in response to the first Office action on the merits (which does not result in a close of prosecution). Submissions after the second Office action on the merits, which is intended to be a final action, will be governed by the requirements of 37 CFR 1.116, after final rejection and by 37 CFR 41.33 after appeal, which will be strictly enforced.

Notification of Concurrent Proceedings

The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a), to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving the Patent under reexamination throughout the course of this reexamination proceeding. Likewise, if present, the third party requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286.

Conclusion

This *ex parte* reexamination proceeding has been filed by a third party requester, or has been merged with another proceeding filed by a third party requester. Accordingly, the parties to this reexamination proceeding are reminded that, in accordance with 37 CFR 1.550(f), any document filed by either the patent owner or the third party requester must be served on the other party in the reexamination proceeding (or parties, where two or more third party requester proceedings are merged), **in the manner provided by 37 CFR 1.248**. If the document filed with the Office does not include a proper certificate of service, the document may be refused consideration by the Office. See MPEP 2220 and 2266.03.

37 CFR 1.550(f) provides:

> *"The reexamination requester will be sent copies of Office actions issued during the ex parte reexamination proceeding. After filing of a request for ex parte reexamination by a third party requester, any document filed by either the patent owner or the third party requester must be served on the other party in the reexamination proceeding in the manner provided by § 1.248. The document must reflect service or the document may be refused consideration by the Office."*

All correspondence relating to this ex parte reexamination proceeding should be directed:

By Mail to: Mail Stop Ex Parte Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand: Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Registered users of EFS-Web may alternatively submit such correspondence via the electronic filing system EFS-Web, at https://efs.uspto.gov/efile/myportal/efs-registered. EFS-Web offers the benefit of quick submission to the particular area of the Office that needs to act on the correspondence. Also, EFS-Web submissions are "soft scanned" (i.e., electronically uploaded) directly into the official file for the reexamination proceeding, which offers parties the opportunity to review the content of their submissions after the "soft scanning" process is complete.

Any inquiry concerning this communication or earlier communications from the examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

/Scott L. Weaver/
Primary Examiner, Art Unit 3992

Conferees:

/Ovidio Escalante/

/Hetul Patel/
Supervisory Patent Examiner, Art Unit 3992

Office Action in Ex Parte Reexamination	Control No. 90/013,809	Patent Under Reexamination 8457228	
	Examiner SCOTT L WEAVER	Art Unit 3992	AIA Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

a. ☑ Responsive to the communication(s) filed on 03 May 2017.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

b. ☑ This action is made FINAL.

c. ☐ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire 2 month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☑ Information Disclosure Statement, PTO/SB/08.
3. ☐ Interview Summary, PTO-474.
4. ☐ _____.

Part II SUMMARY OF ACTION

1a. ☑ Claims 21 are subject to reexamination.
1b. ☑ Claims 1-20 and 22-52 are not subject to reexamination.
2. ☐ Claims _____ have been canceled in the present reexamination proceeding.
3. ☐ Claims _____ are patentable and/or confirmed.
4. ☑ Claims 21 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ The drawings, filed on _____ are acceptable.
7. ☐ The proposed drawing correction, filed on _____ has been (7a) ☐ approved (7b) ☐ disapproved.
8. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the certified copies have
   1 ☐ been received.
   2 ☐ not been received.
   3 ☐ been filed in Application No. _____.
   4 ☐ been filed in reexamination Control No. _____.
   5 ☐ been received by the International Bureau in PCT application No. _____.
   * See the attached detailed Office action for a list of the certified copies not received.
9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. ☐ Other: _____

cc: Requester (if third party requester)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In *Ex Parte* Reexamination of	:	Group Art Unit: 3992
Gordon F. BREMER	:	
Patent No.: 8,457,228	:	Control No.: 90/013,809
Issued: June 4, 2013	:	

Reexam Request Filed: September 12, 2016

For: SYSTEM AND METHOD OF COMMUNICATION USING AT LEAST TWO MODULATION METHODS

Mail Stop *Ex Parte* Reexam
ATTN: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO FINAL OFFICE ACTION

In this above-referenced reexamination of claim 21 of U.S. Patent No. 8,457,228 ("the '228 Patent"), the Office issued a final Office action on November 5, 2018 ("FOA"). This Response to the FOA is timely-filed, i.e., within the two-month period from the mailing date of the FOA. Thus, this Response includes a request to extend the shortened statutory period for an additional two months, i.e., to March 5, 2019. *See* MPEP § 2265(VII).

Notice of Expiration of U.S. Patent No. 8,457,228

Rembrandt submits this response to notify the Office that the '228 Patent expired on December 5, 2018, a fact that impacts the reexamination in that it requires a claim construction under *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316, 75 USPQ2d 1321, 1329 (Fed. Cir. 2005), and one consistent with the Federal Circuit's previous construction of claim 21 of the '228 Patent and claims 2 and 59 of its parent, U.S. Patent No. 8,023,580 ("the '580 Patent"). The Office's present construction under the broadest reasonable interpretation cannot stand.

In view of the '228 Patent's expiration, Rembrandt requests that the Office (1) construe claim 21, including the "at least two types of modulation methods" limitations, under *Phillips*, (2) confirm the patentability of claim 21 under that construction, and (3) issue a NIRC consistent with this determination, as the Office has now done in the parent case U.S. Patent No. 8,023,580 (also under reexamination).

The proper claim construction of the '228 Patent under *Phillips* is a question of law that was finally and conclusively resolved in Rembrandt's favor by the Federal Circuit in *Rembrandt Wireless Technologies v. Samsung Electronics Co.*, 853 F.3d 1370, 1375-77 (Fed. Cir. 2017) -- an appeal brought by Samsung (the Requestor of this reexamination). The criticisms raised by the Office to Rembrandt's construction of "different types" were raised by the Requestor and were rejected by the Federal Circuit. As a result, the proper construction of the '228 Patent under *Phillips* is now settled law, and the Office is required to apply the Federal Circuit's claim construction going forward in this matter. *See, e.g., In re CSB-System International*, 832 F.3d 1335, 1341 (Fed. Cir. 2016 ("When a patent expires during a reexamination proceeding, the PTO should thereafter apply the *Phillips* standard for claim construction."). The court in *CSB-System* cited *Facebook, Inc. v. Pragmatus AV, LLC*, 582 Fed. Appx. 864, 868-69 (Fed. Cir. 2014) and noted that the court in *Facebook* "appl[ied] the *Phillips* standard when patent expired after the Board's reexamination decision pending appeal to the Federal Circuit." 832 F.3d at 1341; MPEP § 2258(I)(G) ("In a reexamination proceeding involving claims of an expired patent, claim construction pursuant to the principle set forth by the court in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316, 75 USPQ2d 1321, 1329 (Fed. Cir. 2005) … should be applied since the expired claim are not subject to amendment. …").

In the related district court litigation, *Rembrandt Wireless Technologies v. Samsung Electronics Co.*, 853 F.3d 1370, 1375-77 (Fed. Cir. 2017), both the district court and the Federal Circuit applied a *Phillips* claim construction and determined that the limitation "modulation method [] of a different type" in claim 21 required at least two "different families of modulation techniques, such as the FSK family of modulation methods and the QAM family of modulation methods." *Id.* at 1377. The Office in this reexamination and the Board in the related IPRs refused to construe "modulation method [] of a different type" to require at least two "different families of modulation techniques." Instead, it construed the claims under an alleged "broadest reasonable interpretation" and determined that their construction did not require at least two "different families of modulation techniques." Given that the '228 Patent has expired, application of the broadest reasonable interpretation is no longer proper and cannot stand. Thus, Rembrandt respectfully requests that the outstanding rejections be reconsidered in light of the expiration of the '228 Patent and of the proper construction of "at least two different types" to require at least two "different families of modulation techniques," as Rembrandt previously requested prior to the '228 Patent's expiration. *See, e.g.,* Rembrandt's August 14, 2017 Response to the May 3, 2017 non-final Office action ("August 14 Response"), at 50-52, 59-69; Claim Construction Order (Exhibit C to Response) and Akl Declaration, ¶¶ 18-27 (submitted with and cited in the Response).

Additionally, Rembrandt submits the Declaration of Dr. Christopher R. Jones (Ex. 2714 in IPR2014-00892) (attached as Ex. A), in which Dr. Jones explains why the modulation methods disclosed in Boer do not satisfy the limitations of claim 21 that require different modulation types (ones that are not in the same family), when properly construed under *Phillips*.

Jones Decl. ¶¶ 28-41, 44, & 55-62. Dr. Jones' testimony regarding Boer would apply with at least equal force to the disclosure of BPSK and QPSK in Snell and Harris.

The Office's NIRC in the Reexamination of the Parent Patent No. 8,023,580

In a NIRC dated December 21, 2018, the Office confirmed the patentability of all the claims under reexamination in the parent patent, U.S. Patent No. 8,023,580 ("the '580 Patent"), which also expired on December 5, 2018. The NIRC acknowledges that "the broadest reasonable interpretation of claim terms is no longer proper for the claims" in the '580 reexamination. *Id.* at 2. It further acknowledges that the claim limitations "including the 'at least two types of modulation methods' or 'different types of modulation method,' should be interpreted under Phillips v. AWH Corp., 415 F.3d 1303, 1316 … (Fed. Cir. 2005)." *Id.*

The NIRC then explains that the Federal Circuit had "applied a Phillips claim construction and determined that the limitation 'modulation of a different type' in claims 2 and 59 required at least two 'different families of modulation techniques, such as the FSK family of modulation methods and the QAM family of modulation methods.'" *Id.* The same holds true for claim 21 of the '228 Patent, as the Federal Circuit determined. *See Rembrandt Wireless Technologies v. Samsung Electronics Co.*, 853 F.3d 1370, *passim* (Fed. Cir. 2017) (construing the term in both the '580 and '228 Patents). Based on that construction, the Office concluded: "Because the prior art on the record does not teach different types of modulation methods as different families of modulation techniques such as the FSK family of modulation methods and the QAM family of modulation methods, claims 2 and 59 [of the '580 Patent] are confirmed." *Id.* For the same reason, the Office should confirm the patentability of claim 21 of the '228 Patent, as the prior art of record in the '228 reexamination does not teach the different types of

modulation methods required when construed as it must be construed under *Phillips* and Federal Circuit law.

Conclusion

Given the expiration of the '228 Patent, the Federal Circuit's claim construction under *Phillips* of different types of modulation methods, and the Office's determination in the '580 reexamination, Rembrandt respectfully requests that the Office withdraw its rejections of claim 21 in the '228 reexamination and issue a NIRC, consistent with its action it the '580 reexamination.

Any fee required for this submission may be charged to Counsel's Deposit Account Number 02-2135.

Respectfully submitted,

Date: December 21, 2018 By: /Michael V. Battaglia/

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Attorney for Petitioner
Rembrandt Wireless Technologies, LP

cc: Nancy J. Linck, Ph.D.
Counsel for Rembrandt Wireless Technologies, LP

Exhibit A

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD.;
SAMSUNG ELECTRONICS AMERICA, INC.;
SAMSUNG TELECOMMUNICATIONS AMERICA, LLC; and
SAMSUNG AUSTIN SEMICONDUCTOR, LLC;
Petitioner

v.

REMBRANDT WIRELESS TECHNOLOGIES, LP
Patent Owner

Case No. IPR2014-00892
Patent 8,457,228

DECLARATION OF DR. CHRISTOPHER R. JONES

TABLE OF CONTENTS

Page

I. INTRODUCTION

1. I have been retained by Pepper Hamilton LLP as Counsel for Patent Owner, Rembrandt Wireless Technologies, LP ("Patent Owner"), to provide opinions on certain issues concerning *Inter Partes* Review No. IPR2014-00892 of U.S. Patent No. 8,457,228 ("the '228 Patent," Ex. 1301).

2. I am aware that the Petition (Paper 2) filed in the above-identified proceeding requested review of various claims of the '228 Patent and that the Board instituted this proceeding on a subset of the challenged claims. Specifically, I understand that the Petitioner challenged Claims 1-3, 5, and 10-21 of the '228 Patent, and that the Patent Trial and Appeal Board ("the Board") has instituted trial for Claims 1-3, 5, and 10-20 of the '228 Patent ("the instituted claims"). I am also aware that Petitioner submitted with the Petition a declaration of David Goodman, Ph.D. ("the Goodman Report," Ex. 1323). I have been asked to analyze the '228 Patent, the Petition and the art cited therein, the Goodman Report, and the Institution Decision dated December 10, 2014 ("the Institution Decision," Paper 8) as they relate to certain issues concerning the instituted claims.

3. My observations and opinions, as set forth below, are based upon my training, education, and experience, as well as my review of the above-referenced documents. I make these statements based upon facts and matters within my own

knowledge or on information provided to me by others. All such facts and matters are true to the best of my knowledge and belief.

4. I am being compensated at my standard consulting rate of $350 per hour. My compensation is not dependent on the outcome of this case.

II. BACKGROUND AND QUALIFICATIONS

5. I received my Ph.D. in Electrical Engineering from the University of California, Los Angeles ("UCLA") in 2003, and my Master of Science (MS) degree in Electrical Engineering from UCLA in 1996. I graduated *magna cum laude* with a Bachelor of Science degree in Electrical Engineering from UCLA in 1995, and was awarded a prize for most outstanding graduating senior in the electrical engineering department.

6. From 2004 to 2009, I worked for Jet Propulsion Laboratory (JPL) in Pasadena, CA as a senior member of the technical staff. In that capacity, I served as the Principal Investigator for the Mars Technology Program on "Coding Systems for High Data Rate Mars Links." I am an author of the Consultative Committee for Space Data Systems (CCSDS) international standard for Low Density Parity Check Codes for deep space telecommunications links. After leaving JPL in 2009, I occasionally contracted with JPL on the Mars MAVEN project and have produced a forward error correction codec to be used in flight on the mission, which launched in November 2013. In addition, I am the co-founder

of Chilicon Power, LLC, a power electronics company that designs and manufactures grid-interactive inverters for photovoltaic modules. The devices Chilicon Power manufactures employ a unique modulation. I designed this modulation for Chilicon's devices in order to mitigate the jamming and erasure conditions present in power line communication channels. Prior to founding Chilicon Power, I was the Chief Technical Officer of Mojix, Inc. in Santa Monica, California between 2009 and 2010, and the Vice President of Advanced Technology for Mojix between 2006 and 2009. Using signal processing techniques from patents that I co-invented, Mojix develops receivers able to received passive RFID tag communications across a distance of more than 1000 feet. I was an early employee of Broadcom Corp. and share inventor credentials on DOCSIS Cable Modem, Direct Broadcast Satellite technologies, and advanced forward error correction technologies.

7. I have authored and co-authored numerous peer-reviewed journal articles, as well as conference papers, on topics concerning field programmable gate array applications, parallel concatenated coding, low density parity check coding, coding applications to the NASA deep space network, and coding applications for Mars in-situ communication. I am the inventor or co-inventor of 35 U.S. patents relating to cable modem, direct broadcast satellite, forward error correction, radio frequency identification, waveform and modulation, and grid

interactive power inverter technologies, and have three other patent applications pending. I have particular expertise in the area of modulation and coding and hold numerous patents on the topic of mutual information optimized pulse-amplitude modulation (PAM), quadrature amplitude modulation (QAM), and phase shift keyed (PSK) constellations for use with capacity approaching codes. PAMs, QAMs, and PSKs can be understood as a 'next generation' of traditional modulations in that they close the majority of the remaining efficiency gap to the ultimate Shannon capacity in applications such as cable modem, direct broadcast satellite, and terrestrial cellular communication.

8. I have founded a registered S-corporation in California named Constellation Designs, Inc. that holds 3 granted US patents, has one pending US application and multiple foreign filings related to capacity-optimized phase and amplitude modulations.

9. A complete list of my publications, patents, and pending applications is included in my curriculum vitae, which is attached hereto as Exhibit A.

10. By virtue of the above experience, I have gained a detailed understanding of the technology that is at issue in this proceeding. My experience with communications systems, and waveforms and modulation techniques used therein, is directly relevant to the subject matter of the '228 Patent. I am also particularly familiar with the '228 Patent as a result of an expert report that I

provided on behalf of the Patent Owner in the related district court litigation involving the '228 Patent, captioned *Rembrandt Wireless Technologies, LP v. Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Telecommunications America, LLC, Samsung Austin Semiconductor, LLC, Blackberry, Corp., and Blackberry, Ltd.*, United States District Court, Eastern District of Texas, Case No. 2:13-CV-213-JRG-RSP.

11. I believe I am qualified to provide opinions about how one of ordinary skill in the art in December 1997 would have interpreted and understood the '228 Patent and the art relied upon by the Petitioner.

III. RELEVANT LEGAL STANDARDS

12. I understand from Counsel that in an *inter partes* review proceeding, claim terms of an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. I also understand that under that standard, there is a heavy presumption that a claim term carries its plain and ordinary meaning, as would be understood by one of ordinary skill in the art at the time of the invention. A claim term will not receive its plain and ordinary meaning, however, if the patentee sets forth a special definition for the term that is clearly stated in the patent specification or file history.

13. It is my understanding that an invention is unpatentable if the differences between the invention and the prior art are such that the subject matter

of the invention as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art. I further understand that obviousness is determined by evaluating: (1) the scope and content of the prior art, (2) the differences between the prior art and the claim, (3) the level of ordinary skill in the art, and (4) secondary considerations of non-obviousness. To establish obviousness based on a combination of the elements disclosed in the prior art, it is my understanding that a petitioner must identify a specific combination that teaches all limitations of the claimed invention and establish that a person of ordinary skill in the art at the time of the claimed invention would have found it obvious to make that combination.

14. To guard against hindsight and an unwarranted finding of obviousness, I understand that an important component of any obviousness inquiry is whether the petitioner has identified any teaching, suggestion, or motivation that would have prompted a person of ordinary skill in the art to make the claimed combination and have a reasonable expectation of success in doing so. I understand that this test should not be rigidly applied, but can be an important tool to avoid the use of hindsight in the determination of obviousness.

15. I further understand that the teaching, suggestion, or motivation may be found explicitly or implicitly: (1) in the prior art; (2) in the knowledge of those of ordinary skill in the art that certain references, or disclosures in those references,

are of special interest or importance in the field; or (3) from the nature of the problem to be solved. Additionally, I understand that the legal determination of the motivation to combine references allows recourse to logic, judgment, and common sense. In order to resist the temptation to read into prior art the teachings of the invention in issue, however, it should be apparent that the "common sense" should not be conflated with what appears obvious in hindsight.

16. I understand that if the teachings of a prior art reference would lead a person of ordinary skill in the art to make a modification that would render another prior art device inoperable, then such a modification would generally not be obvious. I also understand that if a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.

17. I understand that it is improper to combine references where the references teach away from their combination. I understand that a reference may be said to teach away when a person of ordinary skill in the relevant art, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the patentee. In general, a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the patentee. I understand that a reference teaches away, for

example, if (1) the combination would produce a seemingly inoperative device, or (2) the references leave the impression that the product would not have the property sought by the patentee. I also understand that a reference does not teach away if it merely expresses a general preference for an alternative invention, but does not criticize, discredit, or otherwise discourage investigation into the invention claimed. Finally, I understand that dependent claims contain all of the limitations of the claims from which they depend.

IV. SUMMARY OF MY STUDY

18. I have been asked to render an opinion as to the meaning of certain claim terms to a person of ordinary skill in the art and as to whether the instituted claims are invalid in view of the Petitioner's proposed combination of the alleged Admitted Prior Art ("APA") and U.S. Patent No. 5,706,428 of Boer *et al*. ("Boer," Ex. 1304).[1]

[1] The scope of my opinions expressed in this Declaration address claim construction of various terms, as well as whether the combination of the APA and Boer, as proposed by the Petitioner, meets the recitations of the instituted claims as the claims should be construed from the perspective of a person having ordinary skill in the art. I understand that the Patent Owner also relies on the opinions in the Declaration of Dr. Phillip Koopman as they relate to whether one of ordinary skill

19. In forming the opinions contained herein, I have read the '228 Patent and have considered its disclosure from the perspective of a person of ordinary skill in the art in December 1997, including those portions of the '228 Patent that are relied upon by the Petitioner as representing APA. I have also read Boer and considered its disclosure from the perspective of a person of ordinary skill in the art in December 1997. I have also read and considered *inter alia* the Petition for *Inter Partes* Review of the '228 Patent, the Goodman Report, the Patent Owner's Preliminary Response (Paper No. 6), and the Institution Decision (Paper No. 8). I am also familiar with a large number of other prior art references in the field of the invention, including but not limited to the other references provided by the Petitioner in this proceeding. By way of example, I have read an article published in Embedded Systems Programming Magazine, entitled "Communication Protocols for Embedded Systems" and authored by Bhargav Upender and Phillip Koopman, which was submitted by the Petitioner in the instant proceeding as Exhibit 1322.

20. In my opinion, even if a person having ordinary skill in the art would have been motivated to combine APA and Boer, as proposed by the Petitioner, one

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in the art would have been motivated to combine the APA and Boer as proposed by the Petitioner.

would have failed to arrive at the inventions recited in the claims of the '228 Patent, as discussed in detail below.

V. DEFINITION OF PERSON OF ORDINARY SKILL IN THE ART

21. I understand that analysis regarding claim construction and the teachings of the asserted prior art should be performed from the perspective of a person of ordinary skill in the art as of December 5, 1997, which is the filing date of the earliest application to which the '228 Patent claims priority.

22. It is my opinion that one of ordinary skill in the art at the relevant time would have had a bachelor's degree in electrical engineering that included coursework in communications systems and networking, and two years of work experience in electronic communications. In determining this hypothetical "ordinary" level of skill, I considered the sophistication of the technology and the type of problems generally encountered in the field (and typical solutions to those problems), as well as the education level of active workers in the field.

23. Based on my education, qualifications, and experience, I believe that I am qualified to provide opinions about how one of ordinary skill in the art in December 1997 would have understood the prior art and the '228 Patent. My opinions set forth in this declaration are consistent with these understandings.

24. For example, in 1997 I was working at Broadcom Corporation on fundamental cable modem technologies (of which I am listed as a co-inventor).

These technologies utilized a variety of modulations including, binary phase shift keying (BPSK), quadrature (or quaternary) phase shift keying (QPSK), and QAM. I had a master's degree at the time and I had obtained my bachelor's degree 2 years earlier. My master's thesis was focused on compression technologies, specifically a lossless compression technique called "arithmetic coding." My doctoral work was centered on forward error correction for communication systems and enabled me to contribute fundamentally to the development of cable modem technologies as evidenced by my co-inventor credentials on many foundational cable modem patents.

25. I disagree with the Petitioner's definition of a person of ordinary skill in the art. The Petition and the Goodman Report allege that the hypothetical person of ordinary skill in the art would have had "a Master's Degree in Electrical Engineering that included coursework in communications systems and networking, and *at least* five years of experience designing network communication systems." (Paper 2 at 8; Ex. 1323 at ¶61.) However, neither the Petition nor the Goodman Report provides any basis for its allegation as to the level of ordinary skill. Petitioner's proposed definition does not appear to be supported by any evidence, and in fact, fails to provide any rationale as to how a *minimum* level of "at least five years of experience" indicates what is "ordinary." In my opinion, the Petitioner's definition not only includes those that are over-qualified by failing to

cap the level of work experience (e.g., a person with a Master's and *more than 15 years of experience* would be "ordinary" under Petitioner's definition), but it also overstates the typical characteristic of the ordinary-skilled artisan.

VI. SUMMARY OF THE '228 PATENT

26. As indicated above, I understand that the Board has instituted trial for Claims 1-3, 5, 10-20 ("the instituted claims"), of which Claim 1 is independent.

27. Gordon Bremer is listed as the sole inventor of the '228 Patent, which as noted above claims priority to a provisional application filed on December 5, 1997. *See* Exhibit 2701. The Abstract indicates that the '228 Patent is generally directed to systems in which a master device may communicate using different types of modulation methods with other network devices according to a master/slave relationship in which communication from a slave to a master occurs in response to a communication from the master to a slave. (Ex. 1301, Abstract). The '228 Patent is a continuation of U.S. Patent Application No. 12/543,910, which matured into U.S. Patent No. 8,023,580 ("the '580 Patent," Ex. 2718) both the '228 and '580 Patents claim priority to U.S. Provisional Patent Application No. 60/067,562.

28. I believe that a key feature highlighted by the Patentee is the use of the word "types" in many of the claims that are the subject of these proceedings. Specifically, independent claim 1 (and its dependent claims) utilizes the specifier

"types" in reference to modulation methods in order to narrow the claims from the broader term "different." A "different type" means not just changing the number of bits per symbol for a given modulation method (e.g., changing from 1 bit per symbol of binary (B) PSK to 2 bits per symbol of quadrature (Q) PSK), but that modulation methods of a different family are used, for example, from one duration of the transmission to the next (e.g., frequency shift keying (FSK), followed by PSK). As discussed in the sections below, use of the word "type," through its addition in the claims of the '580 patent, was important to the scope of the claim language.

VII. CLAIM CONSTRUCTION

29. I provide my opinions below as to the meaning of the terms first and second "modulation methods" and "types" of modulation methods, as used in independent claim 1in accordance with my understanding of the broadest reasonable construction standard applicable to these proceedings (*see* above at para. 12).

A. First and Second "Modulation Methods"

30. I believe that the proper construction of the term "first modulation method" is "a first method for varying one or more characteristics of a carrier in accordance with information to be communicated," and the proper construction for

the term "second modulation method" is "a second method for varying one or more characteristics of a carrier in accordance with information to be communicated."

31. Based upon my relevant experience, "modulation method" is a term that is generally recognized in the electronic communications arts to mean a technique for varying one or more characteristics of a carrier wave in a predetermined manner to convey information. This definition is supported by the following publications, which describe "modulation" consistent with this common understanding at the time of the invention of the '228 Patent:

- *The IEEE Standard Dictionary of Electrical and Electronics Terms*, 6th Ed. (1996) defines "modulation" as "[t]he process by which some characteristic of a carrier is varied in accordance with a modulating wave." *See* Ex. 1320 (p. 662);
- The *Modern Dictionary of Electronics* (6th ed., 1997) defines "modulation" as "[t]he controlled variation of frequency, phase and/or amplitude of a carrier wave of any frequency in order to transmit a message" and "[t]he process, or results of the process, whereby some characteristic of one signal is varied in accordance with another signal. The modulated signal is called the carrier and may be modulated in three fundamental ways: by varying the amplitude

(amplitude modulation) by varying the frequency (frequency modulation) or by varying the phase (phase modulation).") *See* Ex. 2704 at 663;

- The *Microsoft Press Computer Dictionary* (3rd ed., 1997) – "The process of changing or regulating the characteristics of a carrier wave vibrating at a certain amplitude (height) and frequency (timing) so that the variations represent meaningful information." *See* Ex. 2716, p. 313; and
- D.K. Sharma, et al., *Analog & Digital Modulation Techniques: An Overview* 551 (2010) indicates that "[m]odulation is the process of varying some parameter of a periodic waveform in order to use that signal to convey a message." *See* Ex. 2717, p. 551 and Table 1.

Table-1: Type of Modulation Techniques

Sr. No.	Modulation Techniques	Type	Notation
01	Analog Modulation Techniques	(i) Amplitude Modulation	A.M.
		(ii) Frequency Modulation	F.M.
		(iii) Phase Modulation	P.M.
02	Digital Modulation Techniques	(i) Amplitude Shift Keying	A.S.K.
		(ii) Frequency Shift Keying	F.S.K.
		(iii)Phase Shift Keying	P.S.K.

32. The '228 Patent uses the term "modulation" consistent with this well-known meaning as a method for varying characteristics of a carrier wave. For example, at column 2, lines 3-10, the '228 Patent provides various examples of carrier wave modulation techniques:

> For example, some applications (e.g., internet access) require high performance modulation, such as quadrature amplitude modulation (QAM), carrier [*sic*] amplitude and phase modulation (CAP)[2], or discrete multitone (DMT) modulation, while other applications (e.g., power monitoring and control) require only modest data rates and therefore a low performance modulation method.

33. QAM is Quadrature Amplitude Modulation and consists of discretely varying the amplitude of two orthogonal phases of a carrier wave.

34. CAP is Carrierless Amplitude and Phase modulation. This modulation is similar to QAM, but does not explicitly use quadrature phases in the modulator to build the constellation. CAP is a variant of QAM in that CAP can be thought of as combining two "carrierless" pulse-amplitude modulated signals to

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[2] The reference to Carrier Amplitude Modulation appears to be a typographical error in the '228 Patent. A person of ordinary skill in the art would understand that CAP is an acronym for Carrierless Amplitude and Phase modulation, as discussed otherwise herein.

create a QAM signal in which the phase of the carrier is reset at the beginning of each symbol.

35. DMT is Discrete Multitone Modulation and uses a plurality of orthogonal carrier waves to transmit information. Each of these orthogonal carrier waves may be modulated with PSK or QAM in order to convey information.

36. Persons having ordinary skill in the art would have appreciated that the modulation methods described above are carrier wave modulation techniques. Indeed, all of the modulations in the '228 Patent are similar in that they share the common attribute that information is related through alteration of a carrier wave. This is important because it allows all tribs to demodulate the first portion of the modulated carrier (because it is a carrier wave modulation) and then optionally demodulate the second portion of modulation depending on whether or not the modulation is changed to a different, more spectrally efficient modulation that the trib may or may not be capable of demodulating.

37. Indeed, in light of the definition of "modulation" provided in *The IEEE Standard Dictionary of Electrical and Electronics Terms* (which is cited above and also relied upon in the Petition at page 13 and the Goodman Report at ¶88), it is my opinion that there appears to be no significant difference between my proposed construction and the Petitioner's, with the lone caveat being that one of

ordinary skill in the art would appreciate that modulation does not randomly or indiscriminately vary the characteristics of a carrier wave.

B. "Types" of Modulation Methods

38. Instituted independent claim 1 requires that the first and second are of a different "type." As noted above, I am aware that during prosecution of the '580 patent, claims were amended to recite "at least two types of modulation methods, . . . wherein the second modulation method is of a different type than the first modulation method . . . ." Ex. 2719 at 07/23 (underlining original indicating amendments to the claim language). Concurrent with this amendment to the claims, the applicant indicated that "the language of independent claim 1 has been clarified to refer to **two *types* of modulation methods, *i.e.*, different families of modulation techniques**, such as the FSK family of modulation methods and the QAM family of modulation methods." Ex. 2719 at 20 (bold and underlining added, italics original). In light of the applicant's express definition for "types" presented during prosecution of the related application, it is my understanding that this claim term is therefore to be construed according to the special definition provided by the applicant (*i.e.*, "different families of modulation techniques").

39. As indicated by the definition of "modulation" provided by the *Modern Dictionary of Electronics* (6th ed., 1997)[3], a person having ordinary skill in the art would understand that a carrier *wave* is fully characterized by its frequency, phase, and amplitude (e.g., for a sine wave, $A(t) = A\sin(2\pi f t + \phi)$, were A denotes amplitude, *f* denotes frequency, and ϕ denotes phase of the wave).

40. As such, the fundamental characteristic(s) of the carrier waveform that are varied in order to convey information with the carrier wave is limited to one or more of the wave's frequency, phase, and amplitude.

41. Accordingly, carrier wave modulations can be classified into distinct *types* or *families* based on changes to the fundamental characteristics of the waveform – amplitude, frequency, and phase of the carrier wave.

42. I note that Petitioner's expert, Dr. Goodman, has focused only on the difference between modulations and not on the concept of modulation type as it is

[3] "The process, or results of the process, whereby some characteristic of one signal is varied in accordance with another signal. The modulated signal is called the carrier and may be modulated in three fundamental ways: by varying the amplitude (amplitude modulation) by varying the frequency (frequency modulation) or by varying the phase (phase modulation)." Ex. 2704 at 663.

used in the '228 patent. The modifier "type" is a narrowing constraint added in the '228 Patent claims.

43. In my opinion, it also would not have been obvious to one of ordinary skill in December 1997 to mix types of modulations because the implementation resources within a radio transceiver would have generally been greater to support the different modulation types. Rather, I believe that ordinary-skilled artisans at the time of the '228 Patent would have avoided multiple types of modulation within the same transceiver because it would have oftentimes increased the cost of implementation and would have been viewed as having little benefit as compared to targeting a specific modulation type for an end-channel requirement.

44. That multiple modulation "types" are a key distinction in the invention described in the '228 Patent is further supported by the provisional application (Ex. 2701) to which the '228 Patent claims priority. The provisional application indicates that the Patentee's teachings "cannot be properly met by a single modulation. A high performance modulation, such as QAM, CAP or DMT, that is initially optimized for high performance and will continue to be improved, will demand state-of-the art implementation devices that are relatively costly. This is true even if such a high performance modulation is "degraded" to operate at its lowest data rate and with its poorest acceptable performance. A low performance

modulation, such as FSK, PAM or DSB, may implemented in much, much less expensive devices." Ex. 2701 at 4.

45. The provisional application also provides a specific example of what it would mean to "degrade" a high performance modulation to operate at its lowest data rate. "Without embedded modulations, all tribs must possess substantially all the transceiver features and cost of a full performance Pinnacle. That is, with the usual 64 kbaud (640 kbps), IP/PPP/PMAP/P-CAP protocol Pinnacle, all tribs must be capable of transmitting and receiving 64 kbaud. *Only minor cost reductions can be achieved by restricting a lower cost trib to fewer bits per symbol… saving some cost in the AFE and the DSP. An example cost reduction may be from $50 to $40.* With embedded modulation, Type B tribs can be, say, 16 kbps FSK modems without need for any protocol such as above. It is estimated that such a modem core can be implemented for a cost of perhaps $5." Ex. 2701 at 6.

46. In light of the above passages of the priority provisional, the '228 Patent thereby provides that operating at fewer bits per symbol to degrade the performance of a modulation method (though the modulation method remains the same) may be insufficient to obtain the beneficial outcomes (e.g., cost savings) that can be obtained by using multiple "types" of modulation in accordance with the Patentee's teachings.

47. Thus, in the context of the '228 Patent, Boer's restriction of a transceiver to DBPSK modulation as compared DQPSK modulation would result in only a 'minor' cost reduction by reducing the bits per symbol of the differential PSK modulation from two bits per symbol to one, and would be insufficient to obtain the benefits provided by the '228 Patent, which are described as being enabled through the use of different "types" of modulation. Accordingly, Dr. Goodman's proposed definition for different "types" of modulation methods as being "incompatible" is inconsistent with the '228 Patent, and is therefore improper.

VIII. THE PRIOR ART OF THE INSTITUTED GROUNDS

48. I understand Petitioner alleges that the combination of alleged Admitted Prior Art and U.S. Patent No. 5,706,428 to Boer *et al*. renders the instituted claims obvious. Below, I provide a brief summary of the relied-upon art.

A. The Alleged Admitted Prior Art ("APA")

49. Petitioner alleges that the '228 Patent describes certain prior art systems including a multipoint communication system including a master transceiver and a plurality of tributary transceivers. Petitioner alleges that the description of a system having a master modem and plurality of identical tributary modems all communicating via a common modulation method constitutes prior art. *See* Paper 2 at 15-17; *see also* Ex. 1301, 3:64 – 4:3.

50. The Petitioner relies on the described system as evidence of the existence of common modulation master/slave systems prior to the invention of the claimed subject matter of the '228 Patent.

B. U.S. Patent No. 5,706,428 to Boer *et al.* ("Boer")

51. U.S. Patent No. 5,706,428 issued to Jan Boer *et al*. on January 6, 1998, and is entitled "Multirate Wireless Data Communication System." Boer purportedly provides a wireless local area network (LAN) that "includes first stations adapted to operate at a 1 or a 2 Mbps data rate and second stations adapted to operate at a 1, 2, 5, or 8 Mbps data rate." (Ex. 1304, Abstract.

52. Figure 1 of Boer, which is reproduced below, depicts a wireless LAN 10 that includes an access point 12 and multiple mobile stations 18, 22. *Id*. at 2:7-37. The access point 12 has antennas 16, 17 for transmitting and receiving messages over a wireless communication channel. *Id*. at 2:5-15. Each of the mobile stations 18, 22 are depicted in Figure 1 of Boer as also having two antennas. Boer discloses that some mobile stations 18-1, 18-2 are "capable of transmitting and receiving messages selectively at a data rate of 1 Mbps (Megabit per second) or 2 Mbps…," (*Id*. at 2:34-41) while other mobile stations 22-1, 22-2 "can operate at a 1 Mbps or a 2 Mbps data rate . . . and in addition can also operate at two higher data rates, namely 5 Mbps and 8 Mbps." *Id*. at 2:19-21. When the mobile stations 18, 22 are "operating at the 1 Mbps data rate, DBPSK (differential

binary phase shift keying) modulation of the RF carrier is utilized, and when operating at the 2 Mbps data rate DQPSK (differential quadrature phase shift keying) modulation of the RF carrier is utilized." *Id.* at 2: 23-27 (emphasis added). *See also* 2:37-39. When the mobile stations 22 operate at the higher data rates, the "5 and 8 Mbps data rates utilize PPM/DQPSK (pulse position modulation – differential quadrature phase shift keying)…" *Id.* at 2:41-43 (emphasis added).

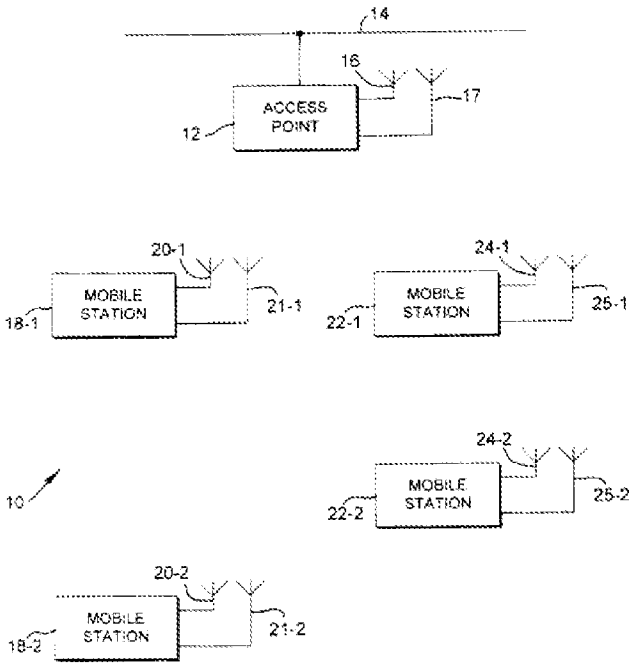

FIG.1

53. As shown below in Figure 4, a typical message 200 used in Boer's LAN 10 contains a preamble 216, a header 218 (which contains *inter alia* an 8-bit signal field 206 and an 8-bit service field), and a data field 214, "which comprises a variable number of data 'octets', that is 8-bit segments, sometimes referred to as 'bytes'." *Id.* at 3:42-55.

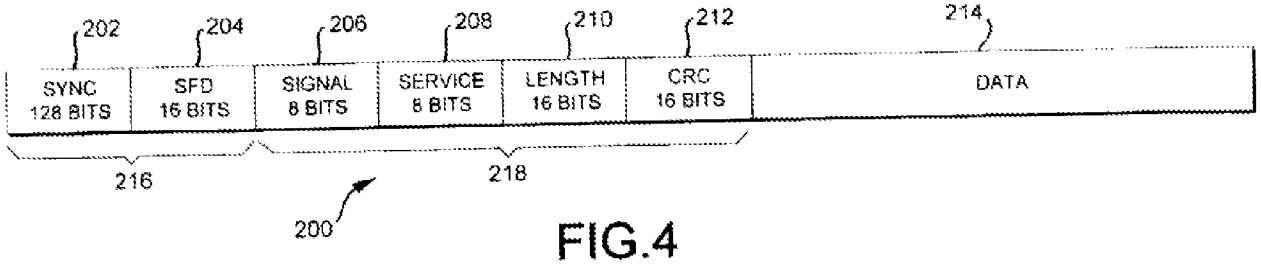

FIG.4

54. "[T]he preamble 216 and header 218 are always transmitted at the 1 Mbps rate using DBPSK modulation." (*Id.* at 3:56-58.) "The subsequent DATA field 214, however, may be transmitted at a selected one of the four possible rates 1, 2, 5, and 8 Mbps using modulation and coding discussed hereinabove." *Id.* at 3:57-62 (emphasis added). "The SIGNAL field 206 has a first predetermined value if the DATA field 214 is transmitted at the 1 Mbps rate and a second predetermined value if the DATA field 214 is transmitted at the 2, 5, or 8 Mbps rates." *Id.* at 4:4-7. "The SERVICE field 208 has a first predetermined value (typically all zero bits) for the 1 and 2 Mbps rates, and a second predetermined value for the 5 Mbps rate and a third predetermined value for the 8 Mbps rate." *Id.* at 4:8-11. The stations 18, which are adapted to operate at 1 and 2 Mbps rates only, ignore the SERVICE field 208. *Id.* at 4:12-13.

IX. THE BOER '428 PATENT DOES NOT USE A MODULATION OF A DIFFERENT TYPE FOR THE SECOND MODULATION

55. All of Boer's rates operate using phase shift keying (PSK) modulation. As noted above, Boer states:

> When operating at the 1 Mbps data rate DBPSK (differential binary phase shift keying) modulation of the RF carrier is utilized and when operating at the 2 Mbps data rate DQPSK (differential quadrature phase shift keying) modulation of the RF carrier is utilized. Ex. 1304 at 2:23-27.

> At the 5 Mbps data rate there are used 1 out of 8 possible PPM positions whereby there are 5 encoded bits per symbol interval (3 position bits plus 2 bits for quadrature phase information). At the 8 Mbps data rate the I- and Q-components are used separately. Thus there are 3 position bits for the I-component, 3 position bits for the Q-component and 2 bits for quadrature phase information. Ex. 1304 at 2:44-51.

56. Differential BPSK (DBPSK) and Differential QPSK (DQPSK) are both examples of differential phase shift keying (DPSK), which requires only differential, instead of absolute, phase measurement at the receiver in order to ascertain the information conveyed by the modulated carrier wave. In particular, the receiver can measure the relative phase difference between waveforms received during successive transmission intervals. DBPSK employs two different phase levels (i.e., two different waveforms with half-cycle phase shifts of the carrier wave) to convey one bit per symbol and DQPSK employs four different phase levels (i.e., four different waveforms with quarter-cycle phase shifts of the carrier wave) to convey two bits per symbol.

57. In my opinion, DBPSK and DQPSK are not different types of modulation methods. Rather, DBPSK and DQPSK are both in the phase family of modulation methods. This is so because in both DBPSK and DQPSK the characteristic of the carrier wave that is modulated is its phase. Moreover, as noted

above, DBPSK and DQPSK cannot be considered different "types" of modulation within the meaning of the '228 Patent because the '228 Patent provides that merely restricting the differential PSK modulation from two bits per symbol to one bit per symbol would be insufficient to obtain the benefits provided by the Patentee's teachings.

58. Further, in my opinion, pulse position modulation (PPM) as utilized in Boer (i.e., as PPM/DQPSK) is not a carrier wave modulation technique and does not fall under the construction of the term "modulation" as "varying one or more characteristics of a carrier signal in accordance with information to be communicated." Therefore PPM/DQPSK is not a different type of modulation than DQPSK.[4] It is my opinion that, in the context of the '228 patent, the use of the term "modulation" within the term "pulse position modulation" is a misnomer. Because the PPM portion of the PPM/DQPSK technique *does not vary the carrier*

[4] Claims 1 and 15 refer to modulation methods being of "a different type." The parties have also sought to construe the terms "The second modulation method *being of a different type* than the first modulation method" and *different type* of modulation method" (emphasis added). The specification and file history do not include any discussion or analysis of "sameness" or "same types". Therefore to be precise, my opinions focus on the meaning of "different" rather than "same."

amplitude, the carrier phase, or the carrier frequency, one of skill in the art would recognize that the PPM portion of the PPM/DQPSK technique is not modulating the carrier wave. Rather, PPM is an "encoding" (or coding) technique within the context of Boer, a characterization which Boer similarly utilizes to describe the use of PPM in PPM/DQPSK. *See e.g.,* Ex. 1304 at 4:45-48 ("Thus a station 18 will not defer if, when it wishes to transmit, it senses a transmission involving a *PPM type coding* as well as DSSS coding. such as is used for the 5 and 8 Mbps transmissions of a station 22." (emphasis added)).

59. The PPM-encoding technique employed by Boer in combination with DQPSK modulation creates 8 time slots in which carrier phase modulated symbols can be placed for transmission. Since 8 time slots correspond to 2^3 possible time locations, 3 bits of information can be conveyed in choosing the time slot for transmission. The underlying type of carrier wave modulation is independent of the time slot selected and remains phase modulation. I also note that these 3 bits of information come at the expense of 8 time slots that could have otherwise been filled with an unbroken stream of DBPSK and DQPSK symbols. So the throughput increases logarithmically in the number of slots, but simultaneously decreases linearly in the number of slots. In general, if there are N slots then the throughput, for a constant symbol time, is changed by a factor of $(\log_2 N)/N$.

60. In the PPM-encoded DQPSK modulation used in Boer, PPM does not change the underlying type of carrier wave modulation from one point in time to the next. Rather, the underlying type of carrier wave modulation remains phase modulation (as noted above, DQPSK modulates the phase of the carrier wave). PPM as used in combination with DQPSK simply allows encoding additional bits in the transmitted signal by providing time slots (8 time slots in Boer) in which the signal is transmitted so as to change the throughput without changing the type of carrier wave modulation. Though changing the "start and stop time" of the information (i.e., selecting a slot for a phase-modulated carrier wave as in PPM/DQPSK) may increase the number of bits transmitted by the DQPSK modulation method, this increase is due to encoding rather than through varying one of the fundamental characteristic(s) that define the information-varying aspect of the carrier waveform (i.e., the wave's frequency, phase, and amplitude).

61. In other words, PPM as used in Boer (i.e., PPM/DQPSK) is an encoding technique—not a modulation method that expresses information through alteration of a carrier wave. Other encoding techniques that can be applied to PSK modulation to convey different amounts of information per channel usage are known in the art. For example, a repetition code operates as its name implies: the symbols are literally repeated in order to improve reliability in the presence of noise. As another example, forward error correcting coding may be applied to

modulated symbols. Under such as approach, the total number of modulated symbols is increased by a proportion equal to 1/R where R is the 'rate' of the code and varies between 1 and 0. For example, a rate 1/3 code expands the amount of transmitted information by a factor of 3. Similar to these encoding techniques, PPM used in Boer is independent of the underlying carrier wave modulation method used to modulate the symbols.

62. Accordingly, it is my opinion that even if one of ordinary skill in the art would have been motivated to combine APA and Boer as suggested by the Petitioner, one would have failed to arrive at the invention recited in independent claim 1 (and instituted claims which depend therefrom), at least because Boer fails to disclose or suggest utilizing different types of modulation methods.

63. All of the statements made in this declaration of my own knowledge are true, and all statements made on information and belied are believed to be true. These statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code.

Dated: February 17, 2015 Signature: 

EXHIBIT A

Dr. Christopher R. Jones – Curriculum Vitae

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(Rev. Sept 2014)

Employment

- 2010-*Present* Co-Founder, Chilicon Power LLC, Los Angeles, CA
- 2010-*Present* Co-Founder, Constellation Designs, Los Angeles, CA.
- 2004-2009 Senior Technical Staff, Jet Propulsion Laboratory, Pasadena, CA.
- 2009-2010 Chief Technical Officer, Mojix Corporation, Santa Monica, CA.
- 2006-2009 Vice President Advanced Technology, Mojix Corporation, Santa Monica, CA.
- 1997-2002 VLSI Engineer, Broadcom Corporation, Irvine, CA.

Testifying / Deposition

- Nov. 2013. 6 hour deposition on behalf of Space Systems Loral

Consulting Relationships / Engagements

- 2012 Research Expert: Oracle Corp, Redwood Shores Headquarters, CA; Purpose: Retained to support IPR re-exam on patents related to memory caching.
- 2008-2012 Research Expert: GPNE Corp; Purpose: Develop opinions and conclusions related to infringement of digital communication patents held by employer. Employer is not Tivo, Verizon, Motorola, or General Instrument, nor is employer a competitor to Tivo, Verizon, Motorola, or General Instrument.
- 2011 Research Expert: ATMEL Corp, 2325 Orchard Parkway San Jose, 95131
- 2010-2012 Research Expert: Tivo Corp, 2160 Gold Street P.O. Box 2160 Alviso, CA 95002
- 2012-2013 Testifying Expert: Space Systems Loral, 3825 Fabian Way Palo Alto, CA 94303
- 2013 Research Expert: Ericsson Corp related to LTE technologies
- 2014 Testifying Expert: Campbell Company related to power line communication for traffic lights
- 2013-2014 Research Expert: Rembrandt Technologies on Blue Tooth infringement issues

Professional Activity

- Nov 2013 MAVEN Mars Satellite System Advanced FEC Communication Payload for Obiter to Lander to Earth Relay
- Aug 2011 LDPC Codec for JPL Mission: Mars Atmospheric and Volatile Evolution (MAVEN)
- Jan 2005-*Present* Principal Investigator : Mars Technology Program, "Coding Systems for High Data Rate Mars Links," 3 Yrs / $1.8 million Mars Technology Program Task.
- Sept 2007 Session Chair, Information Theory Workshop, Lake Tahoe, CA.
- 2004-2006 Author : Low Density Parity Check Codes for Use in Near-Earth and Deep Space Applications, Consultative Committee for Space Data Systems (CCSDS) standards body
- July 2005,06,07 Instructor : UCLA Short Course on LDPC Codes.
- 2003-2004 Working Group Member : IEEE 802.11 Wireless LAN High Throughput Study Group (TGN/802.11n)
- 2001-*Present* Peer Reviewer : *IEEE Transactions on Communications*, *IEEE Transactions on Signal Processing*, *IEEE Communications Letters*, *IEEE* Conferences
- 1999-2001 Integrated Circuits BCM4500/94500. Direct broadcast satellite integrated transceiver SOC.
  - First Broadcom socket in Echostar/DISH network set-top box
  - First Broadcom parallel concatenated (turbo) code implementation

- Constituent code design/selection
- Codec algorithmic definition
- High throughput VLSI encoder implementation

- 1998 Integrated Circuit BCM6010. Very high rate Digital Subscriber Line (VDSL) transceiver
  - FEC functional verification, module synthesis
- 1997 Integrated Circuit BCM3137. Burst demodulator for cable modem headend
  - First MCNS compliant cable modem headend ASIC.
  - Digital ASIC engineer
- 1997 Data Over Cable System Specification Media Access Controller TDMA timing recovery
  - MCNS Media Access Controller (MAC) FPGA prototype
  - System verification of upstream time division synchronizaton
- 1995-1996 Run-Time Reconfigurable FPGA platform and algorithms for video communication

Education

- Fall 2003 **Ph.D. Electrical Engineering**, University of California Los Angeles.
  Dissertation : *Constructions, Applications, and Implementations of Low-Density Parity-Check Codes*
- Fall 1996 **M.S. Electrical Engineering**, University of California Los Angeles.
  Thesis : *Low Complexity Adaptive Arithmetic Coding*
- Spring 1995 **B.S. Electrical Engineering**, University of California Los Angeles.
  Magna Cum Laude (GPA 3.81).

Awards

- 2013 Award for 25 most influential papers at FCCM "Configurable Computing Solutions for Automatic Target Recognition" http://tcfpga.org/fccm20/fccm20.html
- 2007 NASA B-Level Ranger Award : Codes and Codecs for Mars InSitu Communication Links
- 2006 NASA C-Level : Testbed Demonstration of Coding Systems for High Data-Rate Mars Links
- 2007 NASA Tech Brief Award NPO 45032: Pilotless Frame Synchronization Using LDPC Code Constraints
- 2007 NASA Tech Brief Award NPO 44810: New Constellations for Communications Signalling: Design Methodolgy and Method and Apparatus for the New Signalling Scheme
- 2006 NASA Tech Brief Award NPO 43949: ARA Type Protograph Codes
- 2006 NASA Tech Brief Award NPO 42063: Protograph Based LDPC Codes with Minimum Distance Linearly Growing with Block Size
- 2006 NASA Tech Brief Award NPO 42042: Protograph Based LDPC Codes Constructed from Simple Loop-Free Encoding Modules
- 2006 NASA Tech Brief Award NPO 43112: Pilotless Iterative Symbol Timing Recovery via LDPC Code Constraint Feedback
- 2005 NASA Achievement Award: ARA-Type Code Construction and Standardization.
- 2004 NASA achievement award: Low-Density Parity-Check Decoder.
- 1995 UCLA Electrical Engineering: Most outstanding graduating senior.
- 1994 UCLA Electrical Engineering: Eta Kappa Nu.
- 1994 UCLA Electrical Engineering: Tau Beta Pi.

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- D. Divsalar, S. Dolinar, C. Jones, "Short Protograph-Based LDPC Codes," *MILCOM*, Oct. 2007, Orlando, FL, USA.
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- "Methods and Apparatuses for Signaling with Geometric Constellations," US Patent 8,265,175 (Issued Sep. 11, 2012).
- "Rate-compatible protograph LDPC code families with linear minimum distance," US Patent 8,239,746 (Issued Aug. 7, 2012). (Alternate codes to those described in 8,117,523).
- "Systems and Methods for Secure Supply Chain Management and Inventory Control," US Patent 8,332,656 (Issued Dec. 11, 2012).
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- "Methodology and Method and Apparatus for Signaling with Capacity Optimized Constellations," US Patent 7,978,777 (Issued Jul. 12, 2011).
- "Methods to Compensate for Noise in a Wireless Communication System," US Patent 7,821,954 (Issued Oct. 26, 2010).
- "Compensating for Noise in a Wireless Communication System," US Patent 7,843,847 (Issued Nov. 30, 2010).
- "ARA Type Protograph Codes," US Patent 7,343,539 (Issued Mar. 11, 2008).
- "Encoders for Block-Circulant LDPC Codes," US Patent 7,499,490 (Issued Mar. 3, 2009)
- "Decoding Low Density Parity Check Codes," US Patent 7,340,671 (Issued Mar. 4, 2008)
- "Parallel concatenated code with soft-in soft-out interactive turbo decoder," US Patent 7,570,700 (Issued Aug. 4, 2009).
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- "Data packet fragmentation in a wireless communication system," US Patent 7,512,154 (Issued Mar. 31, 2009).
- "Synchronization module using a Viterbi slicer for a turbo decoder," US Patent 7,499,507 (Issued Mar. 3, 2009).
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- "Method and apparatus for performing calculations for forward (alpha) and reverse (beta) metrics in a map decoder," US Patent 7,012,975 (Issued Mar. 14, 2006).
- "Network data transmission synchronization system and method," US Patent 6,965,616 (Issued Nov. 15, 2005).
- "Burst receiver for cable modem system," US Patent 6,961,314 (Issued Nov. 1, 2005).
- "Cable modem apparatus and method," US Patent 6,650,624 (Issued Nov. 18, 2003).

Pending US Patent Applications

- "MACHINE VISION RFID EXCITER TRIGGERING SYSTEM," US Application 20090322489 (Published Dec. 31, 2009).
- "RFID SYSTEMS USING DISTRIBUTED EXCITER NETWORK," US Application 20090146792 (Published Jun. 11, 2009).
- "SYSTEMS AND METHODS FOR JOINT BEAMFORMING AND PREAMBLE DETECTION," US Application 13/307,819 (Published Jul. 26, 2012).

EXHIBIT B

MATERIALS CONSIDERED

1. U.S. Patent 8,457,228 (Ex. 1301) and its file history
2. U.S. Provisional Patent App. No. 60/067,562, dated December 5, 1997 (Ex. 2701)
3. U.S. Patent 5,706,426 to Boer (Ex. 1304)
4. Declaration of David Goodman dated June 4, 2014 (Ex. 1323)
5. Patent Owner's Preliminary Response (Paper 6)
6. Institution Decision (Paper 8)
7. COMPREHENSIVE DICTIONARY OF ELECTRICAL ENGINEERING 397 (CRC Press LLC 1999) (Ex. 2703).
8. Transcript of Deposition of David Goodman, Ph.D. and Exhibits in IPR2014-00518 and IPR2014-00519 (November 7, 2014) (Ex. 2711, filed herewith)
9. MODERN DICTIONARY OF ELECTRONICS, SIXTH ED., REVISED AND UPDATED 663 (Butterworth-Heinemann 1997) (Ex. 2715, filed herewith)
10. MICROSOFT PRESS COMPUTER DICTIONARY, THIRD ED. 313 (MICROSOFT PRESS 1997) (Ex. 2616, filed herewith)
11. D.K. Sharma, et al., "Analog & Digital Modulation Techniques: An Overview," TECHNIA – International Journal of Computing Science and Communication Technologies, vol. 3, n. 1, 551-61 (July 2010) (Ex. 2717, filed herewith)
12. Filings from *Inter Partes* Review, IPR2014-00892
13. Filings from *Inter Partes* Review, IPR2014-00893
14. Filings from *Inter Partes* Review, IPR2014-00895
15. Filings from *Inter Partes* Review, IPR2014-00518

16. Filings from *Inter Partes* Review, IPR2014-00519

17. U.S. Patent 8,023,580 (Ex. 2718) and its file history (Ex. 2719)

Electronic Acknowledgement Receipt

EFS ID:	34679609
Application Number:	90013809
International Application Number:	
Confirmation Number:	7821
Title of Invention:	SYSTEM AND METHOD OF COMMUNICATION USING AT LEAST TWO MODULATION METHODS
First Named Inventor/Applicant Name:	8457228
Customer Number:	6449
Filer:	Michael Vincent Battaglia/Keiko Shelton
Filer Authorized By:	Michael Vincent Battaglia
Attorney Docket Number:	3277-0114US-RXM2
Receipt Date:	21-DEC-2018
Filing Date:	12-SEP-2016
Time Stamp:	17:22:07
Application Type:	Reexam (Patent Owner)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		response.pdf	111182 9891969472788dbbe36c4324dfbb4baf6e53e13a	yes	6

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Reexam Certificate of Service	6	6
	Reexam Response to Final Rejection	1	5
Warnings:			
Information:			

2	Trans Letter filing of a response in a reexam	Exhibit_A.pdf	1970123 970549b463d71ca38635f8dc0ad8b7f55778cbca	no	42

Warnings:	
Information:	
Total Files Size (in bytes):	2081305

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

CERTIFICATE OF SERVICE

It is hereby certified that on this 21st day of December, 2018, the foregoing **RESPONSE TO FINAL OFFICE ACTION** was served, by first-class U.S. Mail, on the attorney of record for the third-party Requesters Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc., at the following address:

J. Steven Baughman, Esq.
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IPRM – Floor 43
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800 Boylston Street
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/Michael V. Battaglia/
Michael V. Battaglia
Reg. No. 64,932

cc: Nancy J. Linck, Ph.D.
Counsel for Rembrandt Wireless Technologies, LP

Litigation Search Report CRU 3999

Reexam Control No. 90/013,809

TO: SCOTT WEAVER Location: CRU Art Unit: 3992 Date: 01/02/2019	From: MANUEL SALDANA Location: CRU 3999 REM4C71 Phone: (571) 272-7740 MANUEL.SALDANA@uspto.gov

Search Notes

Litigation was found for US Patent Number: **8,457,228**

(OPEN) Samsung Electronics Co. Ltd. Vs. Rembrandt Wireless Technologies, LP	IPR2014-00889
(OPEN) Samsung Electronics Co. Ltd. Vs. Rembrandt Wireless Technologies, LP	IPR2014-00890
(OPEN) Samsung Electronics Co. Ltd. Vs. Rembrandt Wireless Technologies, LP	IPR2014-00891
(CLOSED) Samsung Electronics Co. Ltd. Vs. Rembrandt Wireless Technologies, LP	IPR2014-00892
(CLOSED) Samsung Electronics Co. Ltd. Vs. Rembrandt Wireless Technologies, LP	IPR2014-00893
(CLOSED) Samsung Electronics Co. Ltd. Vs. Rembrandt Wireless Technologies, LP	IPR2014-00895
(OPEN) Samsung Electronics Co. Ltd. Vs. Rembrandt Wireless Technologies, LP	IPR2015-00555

1) I performed a KeyCite Search in Westlaw, which retrieves all history on the patent including any litigation.

2) I performed a search on the patent in Lexis CourtLink for any open dockets or closed cases.

United States Patent Trial and Appeals Board

US Patent Trial and Appeals Board - Alexandria
(Alexandria)

IPR2014-00889

Samsung Electronics Co. Ltd. Vs. Rembrandt Wireless Technologies, LP

This case was retrieved from the court on Wednesday, June 08, 2016

Header

Case Number: **IPR2014-00889**

Date Filed: **06/04/2014**

Date Full Case Retrieved: **06/08/2016**

Status: **Open**

Misc: **Civil**

Summary

Court Case Status: Not Instituted

Case Type: IPR: Inter partes review

Date of Decision to Institute Case: 12/10/2014

Technical Center Number: 2600

Patent Application Number: 13198568

Patent Number: 8457228

Participants

Litigants

Samsung Electronics Co. Ltd.

Petitioner

Rembrandt Wireless Technologies, LP

PatentOwner

Proceedings

File Date	Details	Document Type	Paper/ Exhibit	Filed By	Public?

			No.		
06/04/2014	Power of Attorney	Power of Attorney	1	Petitioner	Yes
06/04/2014	Petition for Inter Partes Review of U.S. Patent No. 8,457,228	Petition	2	Petitioner	Yes
06/04/2014	Patent 8457228	Exhibit	1001	Petitioner	Yes
06/04/2014	Complaint	Exhibit	1002	Petitioner	Yes
06/04/2014	Amended Complaint	Exhibit	1003	Petitioner	Yes
06/04/2014	Draft 801.22 Std	Exhibit	1004	Petitioner	Yes
06/04/2014	802.11 Std	Exhibit	1005	Petitioner	Yes
06/04/2014	Boer US5706428	Exhibit	1006	Petitioner	Yes
06/04/2014	Patent 5,537,398 siwiak	Exhibit	1007	Petitioner	Yes
06/04/2014	Information Disclosure Statement	Exhibit	1008	Petitioner	Yes
06/04/2014	228 Application as Filed	Exhibit	1009	Petitioner	Yes
06/04/2014	228 4.30.2012 OA	Exhibit	1010	Petitioner	Yes
06/04/2014	10.19.2012 OA Response	Exhibit	1011	Petitioner	Yes
06/04/2014	First Notice of Allowance	Exhibit	1012	Petitioner	Yes
06/04/2014	Request for Continued Examination	Exhibit	1013	Petitioner	Yes
06/04/2014	2nd Notice of Allowance	Exhibit	1014	Petitioner	Yes
06/04/2014	Infringement Contentions	Exhibit	1015	Petitioner	Yes
06/04/2014	Rembrandt Markman Brief	Exhibit	1016	Petitioner	Yes
06/04/2014	580 App as Filed	Exhibit	1017	Petitioner	Yes
06/04/2014	580 Office Action Summary	Exhibit	1018	Petitioner	Yes
06/04/2014	580 3.1.2011 Reply	Exhibit	1019	Petitioner	Yes
06/04/2014	Rembrandt Tutorial Reference	Exhibit	1020	Petitioner	Yes
06/04/2014	IEEE Dictionary	Exhibit	1021	Petitioner	Yes
06/04/2014	Commuications Dictionary Master Slave	Exhibit	1022	Petitioner	Yes
06/04/2014	O'Hara Declaration	Exhibit	1023	Petitioner	Yes
06/04/2014	Goodman Declaration	Exhibit	1024	Petitioner	Yes
06/18/2014	Notice of Filing Date Accorded to Petition	Notice of Filing Date Accorded to Petition	3	Board	Yes
06/20/2014	Power of Attorney	Power of Attorney	4	Potential Patent Owner	Yes
06/20/2014	Related Matters	Notice	5	Potential Patent Owner	Yes
09/18/2014	PO Preliminary Response	Preliminary Response	6	Patent Owner	Yes
09/18/2014	Exhibit 2401	Exhibit	2401	Patent Owner	Yes
09/18/2014	Exhibit 2402	Exhibit	2402	Patent Owner	Yes

09/18/2014	Exhibit 2403	Exhibit	2403	Patent Owner	Yes
09/18/2014	Exhibit 2404	Exhibit	2404	Patent Owner	Yes
09/18/2014	Exhibit 2405	Exhibit	2405	Patent Owner	Yes
09/18/2014	Exhibit 2406	Exhibit	2406	Patent Owner	Yes
09/18/2014	Exhibit 2407	Exhibit	2407	Patent Owner	Yes
09/18/2014	Exhibit 2408	Exhibit	2408	Patent Owner	Yes
09/18/2014	Exhibit 2409	Exhibit	2409	Patent Owner	Yes
09/18/2014	Exhibit 2410	Exhibit	2410	Patent Owner	Yes
09/18/2014	Exhibit 2411	Exhibit	2411	Patent Owner	Yes
09/18/2014	Exhibit 2412	Exhibit	2412	Patent Owner	Yes
09/18/2014	Exhibit 2413	Exhibit	2413	Patent Owner	Yes
10/31/2014	Supplemental Mandatory Notice	Notice	7	Patent Owner	Yes
12/10/2014	Decision - Denying Institution of Inter Partes Review 37 C.F.R. 42.108	Institution Decision	8	Board	Yes
12/10/2014	Patent Owner's Supplemental Mandatory Notice Information Under 37 C.F.R. 42.8	Notice	9	Patent Owner	Yes
03/10/2015	IPR2014-00889 - Refund request	Refund Request	10	Petitioner	Yes
03/23/2015	Notice of Refund	Notice	11	Board	Yes

United States Patent Trial and Appeals Board

US Patent Trial and Appeals Board - Alexandria
(Alexandria)

IPR2014-00895

Samsung Electronics Co. Ltd. Vs. Rembrandt Wireless Technologies, LP

This case was retrieved from the court on Wednesday, June 08, 2016

Docket

Case Number: **IPR2014-00895**

Date Filed: **06/04/2014**

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Status: **Closed**

Misc: **Civil**

Summary

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06/04/2014	Patent No. US8457228	Exhibit	1501	Petitioner	Yes
06/04/2014	Complaint	Exhibit	1502	Petitioner	Yes
06/04/2014	Amended Complaint	Exhibit	1503	Petitioner	Yes
06/04/2014	Boer US5706428	Exhibit	1504	Petitioner	Yes
06/04/2014	Patent US6614838	Exhibit	1505	Petitioner	Yes
06/04/2014	838 June 28 2001 Office Action Summary	Exhibit	1506	Petitioner	Yes
06/04/2014	Oct 1 2001 Response	Exhibit	1507	Petitioner	Yes
06/04/2014	228 Application as Filed	Exhibit	1508	Petitioner	Yes
06/04/2014	228 4.30.2012 Office Action Summary	Exhibit	1509	Petitioner	Yes
06/04/2014	10.19.2012 OA Response	Exhibit	1510	Petitioner	Yes
06/04/2014	228 Notice of Allowance and Fees Due	Exhibit	1511	Petitioner	Yes
06/04/2014	228 Request for Continued Examination Transmittal	Exhibit	1512	Petitioner	Yes
06/04/2014	228 2nd Notice of Allowance and Fees Due	Exhibit	1513	Petitioner	Yes
06/04/2014	Infringement Contentions	Exhibit	1514	Petitioner	Yes
06/04/2014	Rembrandt Markman Brief	Exhibit	1515	Petitioner	Yes
06/04/2014	580 Application as Filed	Exhibit	1516	Petitioner	Yes
06/04/2014	580 Office Action Summary	Exhibit	1517	Petitioner	Yes
06/04/2014	580 3.1.2011 Reply	Exhibit	1518	Petitioner	Yes
06/04/2014	Rembrandt Tutorial Reference	Exhibit	1519	Petitioner	Yes
06/04/2014	IEEE Dictionary	Exhibit	1520	Petitioner	Yes
06/04/2014	Commuications Dictionary Master Slave	Exhibit	1521	Petitioner	Yes
06/04/2014	Mears Declaration and Upender	Exhibit	1522	Petitioner	Yes
06/04/2014	Draft 802.11 Std	Exhibit	1523	Petitioner	Yes
06/04/2014	Cafarella US5809060	Exhibit	1524	Petitioner	Yes
06/04/2014	Bialkowiski US5574910	Exhibit	1525	Petitioner	Yes
06/04/2014	Goodman Declaration	Exhibit	1526	Petitioner	Yes
06/18/2014	Notice of Filing Date Accorded to Petition	Notice of Filing Date Accorded to Petition	3	Board	Yes
06/20/2014	Power of Attorney	Power of Attorney	4	Potential Patent Owner	Yes
06/20/2014	Related Matters	Notice	5	Potential	Yes

				Patent Owner	
09/18/2014	PO Preliminary Response	Preliminary Response	6	Patent Owner	Yes
09/18/2014	Exhibit 2901	Exhibit	2901	Patent Owner	Yes
09/18/2014	Exhibit 2902	Exhibit	2902	Patent Owner	Yes
09/18/2014	Exhibit 2903	Exhibit	2903	Patent Owner	Yes
09/18/2014	Exhibit 2904	Exhibit	2904	Patent Owner	Yes
09/18/2014	Exhibit 2905	Exhibit	2905	Patent Owner	Yes
09/18/2014	Exhibit 2906	Exhibit	2906	Patent Owner	Yes
09/18/2014	Exhibit 2907	Exhibit	2907	Patent Owner	Yes
10/31/2014	Supplemental Mandatory Notice	Notice	7	Patent Owner	Yes
12/10/2014	Decision - Institution of Inter Partes Review - 37 C.F.R. 42.108	Institution Decision	8	Board	Yes
12/10/2014	Scheduling Order	Notice	9	Board	Yes
12/10/2014	Patent Owner's Supplemental Mandatory Notice Information Under 37 C.F.R. 42.8	Notice	10	Patent Owner	Yes
12/16/2014	Patent Owner's List of Proposed Motions	Notice	11	Patent Owner	Yes
12/16/2014	Petitioner's List of Proposed Motions	Notice	12	Petitioner	Yes
12/19/2014	ORDER Conduct of Proceeding	Notice	13	Board	Yes
01/06/2015	Supplemental Mandatory Notice	Notice	14	Petitioner	Yes
01/09/2015	Supplemental Mandatory Notice	Notice	15	Petitioner	Yes
01/30/2015	PO Supplemental Mandatory Notice	Notice	16	Patent Owner	Yes
02/17/2015	Patent Owner's Response	Opposition	17	Patent Owner	Yes
02/17/2015	Exhibit 2908	Exhibit	2908	Patent Owner	Yes
02/17/2015	Exhibit 2909	Exhibit	2909	Patent Owner	Yes
02/17/2015	Exhibit 2910	Exhibit	2910	Patent Owner	Yes
02/17/2015	Exhibit 2911	Exhibit	2911	Patent Owner	Yes
02/17/2015	Exhibit 2912	Exhibit	2912	Patent Owner	Yes
02/17/2015	Exhibit 2913	Exhibit	2913	Patent	Yes

				Owner	
02/17/2015	Exhibit 2914	Exhibit	2914	Patent Owner	Yes
02/17/2015	Exhibit 2915	Exhibit	2915	Patent Owner	Yes
02/17/2015	Exhibit 2916	Exhibit	2916	Patent Owner	Yes
02/17/2015	Exhibit 2917	Exhibit	2917	Patent Owner	Yes
02/17/2015	Exhibit 2918	Exhibit	2918	Patent Owner	Yes
02/17/2015	Exhibit 2919	Exhibit	2919	Patent Owner	Yes
03/02/2015	Power of Attorney	Power of Attorney	18	Petitioner	Yes
03/20/2015	Petitioners_ Motion to Withdraw As Counsel (IPR2014-00895)	Motion	19	Petitioner	Yes
03/20/2015	Petitioners_ Motion to Change Designation of Lead Counsel (IPR2014-00895)	Motion	20	Petitioner	Yes
03/20/2015	Power of Attorney	Power of Attorney	21	Petitioner	Yes
03/25/2015	Petitioner's Unopposed Motion for Pro Hac Vice Admission of Brian P. Biddinger	Motion	22	Petitioner	Yes
03/26/2015	Order Conduct of Proceedings	Order	23	Board	Yes
03/27/2015	DECISION - Petitioner's Motion for Pro Hac Vice Admission of Mr. Biddinger	Notice	24	Board	Yes
04/07/2015	Petitioners' Supplemental Mandatory Notice	Notice	25	Petitioner	Yes
04/13/2015	Order - Conduct of the Proceeding - 37 CFR 42.5	Order	26	Board	Yes
04/23/2015	Petitioners' Reply In Support of Its Petition for IPR Review	Reply	27	Petitioner	Yes
04/23/2015	Deposition Transcript of Philip J. Koopman, Jr., Ph.D., dated January 13, 2015	Exhibit	1527	Petitioner	Yes
04/23/2015	Data Network Evaluation Criteria Handbook, dated June 2009	Exhibit	1528	Petitioner	Yes
04/23/2015	Order Granting Motion for Fees and Costs, dated August 29, 2012.	Exhibit	1529	Petitioner	Yes
04/23/2015	Deposition Transcript of Dr. Christopher Jones, dated January 7, 2015	Exhibit	1530	Petitioner	Yes
04/23/2015	Illustration of DBPSK modulation drawn by Dr. Christopher Jones at deposition, January 7, 2015	Exhibit	1531	Petitioner	Yes
04/23/2015	Illustration of 5 Mbps PPM/DQPSK modulation drawn by Dr. Christopher Jones at deposition, January 7, 2015	Exhibit	1532	Petitioner	Yes
04/23/2015	Illustration of 8 Mbps PPM/DQPSK modulation drawn by Dr. Christopher Jones at deposition, January 7, 2015	Exhibit	1533	Petitioner	Yes
04/23/2015	Illustration by Dr. Christopher Jones drawn	Exhibit	1534	Petitioner	Yes

	at deposition, January 7, 2015				
04/23/2015	Illustration by Dr. Christopher Jones drawn at deposition, January 7, 2015	Exhibit	1535	Petitioner	Yes
04/23/2015	Illustration by Dr. Christopher Jones drawn at deposition, January 7, 2015	Exhibit	1536	Petitioner	Yes
04/23/2015	Illustration by Dr. Christopher Jones drawn at deposition, January 7, 2015	Exhibit	1537	Petitioner	Yes
04/23/2015	Illustration by Dr. Christopher Jones drawn at deposition, January 7, 2015	Exhibit	1538	Petitioner	Yes
04/23/2015	U.S. Patent No. 5,450,404	Exhibit	1539	Petitioner	Yes
04/23/2015	U.S. Patent No. 5,436,901	Exhibit	1540	Petitioner	Yes
04/23/2015	U.S. Patent No. 5,535,212	Exhibit	1541	Petitioner	Yes
04/23/2015	Order Granting Toshiba America Information Systems Motion to Unseal Court Orders, dated June 27, 2013	Exhibit	1542	Petitioner	Yes
04/23/2015	Lab-Volt, Pulse Modulation and Sampling, Telecommunications Communications Technologies - January 2010	Exhibit	1543	Petitioner	Yes
04/23/2015	WIRELESS COMMUNICATION SYSTEMS - Cambridge University Press 2010	Exhibit	1544	Petitioner	Yes
05/29/2015	Power of Attorney	Power of Attorney	28	Patent Owner	Yes
05/29/2015	PO Supplemental Mandatory Notice	Notice	29	Patent Owner	Yes
06/05/2015	Order - Conduct of Proceeding - 37 CFR 42.5	Order	30	Board	Yes
06/11/2015	PO Identification of Information to be Stricken	Motion	31	Patent Owner	Yes
06/11/2015	Exhibit 3001 - Transcript of June 3, 2015 Conference Call	Exhibit	3001	Patent Owner	Yes
06/15/2015	PO Request for Oral Argument	Notice	32	Patent Owner	Yes
06/15/2015	Petitioners' Request for Oral Hearing	Notice	33	Petitioner	Yes
06/15/2015	PO Motion to Exclude	Motion	34	Patent Owner	Yes
06/15/2015	Ex. 2920 - PO Objections to Evidence Submitted with Reply	Exhibit	2920	Patent Owner	Yes
06/17/2015	Order Trial Hearing Notice	Notice	35	Board	Yes
06/17/2015	Power of Attorney	Power of Attorney	36	Patent Owner	Yes
06/17/2015	Patent Owner Supplemental Mandatory Notice	Notice	37	Patent Owner	Yes
06/18/2015	Petitioners' Response to PO's Identification of Matter to be Stricken from Petitioners' Reply	Reply	38	Petitioner	Yes
07/02/2015	Petitioner's Opposition to Patent Owner's Motion to Exclude Evidence	Opposition	39	Petitioner	Yes

07/02/2015	Wireless Communication Systems	Exhibit	1545	Petitioner	Yes
07/02/2015	Declaration of Meera Nair	Exhibit	1546	Petitioner	Yes
07/13/2015	PO Reply in support of Motion to Exclude	Reply	40	Patent Owner	Yes
07/17/2015	Petitioners' Updated Exhibit List - July 17, 2015	Notice	41	Petitioner	Yes
07/17/2015	Petitioners' Demonstratives	Exhibit	1547	Petitioner	Yes
07/29/2015	Order - re Request for Conference Call	Order	42	Board	Yes
09/16/2015	Record of Oral Hearing	Notice	43	Board	Yes
09/24/2015	Final Written Decision	Final Decision	44	Board	Yes

United States Patent Trial and Appeals Board

US Patent Trial and Appeals Board - Alexandria
(Alexandria)

IPR2015-00555

Samsung Electronics Co. Ltd. Vs. Rembrandt Wireless Technologies, LP

This case was retrieved from the court on Friday, January 08, 2016

Header

Case Number: **IPR2015-00555**

Date Filed: **01/09/2015**

Date Full Case Retrieved: **01/08/2016**

Status: **Open**

Misc: **Civil**

Summary

Court Case Status: Not Instituted

Case Type: IPR: Inter partes review

Date of Decision to Institute Case: 6/19/2015

Technical Center Number: 2600

Patent Application Number: 13198568

Patent Number: 8457228

Participants

Litigants

Samsung Electronics Co. Ltd.

Petitioner

Rembrandt Wireless Technologies, LP

PatentOwner

Proceedings

File Date	Details	Document Type	Paper/ Exhibit	Filed By	Public?

			No.		
01/09/2015	Petition for Inter Partes Review of U.S. Patent No. 8,457,228	Petition	1	Petitioner	Yes
01/09/2015	Power of Attorney	Power of Attorney	2	Petitioner	Yes
01/09/2015	Motion for Joinder to IPR2014-00892	Motion	3	Petitioner	Yes
01/09/2015	U.S. Patent No. 8,457,228	Exhibit	1301	Petitioner	Yes
01/09/2015	Complaint	Exhibit	1302	Petitioner	Yes
01/09/2015	Amended Complaint	Exhibit	1303	Petitioner	Yes
01/09/2015	U.S. Patent No. 5,706,428 (Boer)	Exhibit	1304	Petitioner	Yes
01/09/2015	U.S. Patent No. 6,614,838	Exhibit	1305	Petitioner	Yes
01/09/2015	'838 June 28, 2001 Office Action Summary	Exhibit	1306	Petitioner	Yes
01/09/2015	Oct. 1, 2001 Response	Exhibit	1307	Petitioner	Yes
01/09/2015	'228 Application (as filed)	Exhibit	1308	Petitioner	Yes
01/09/2015	'228 April 30, 2012 Office Action Summary	Exhibit	1309	Petitioner	Yes
01/09/2015	October 19, 2012 Response to Office Action	Exhibit	1310	Petitioner	Yes
01/09/2015	'228 Notice of Allowance and Fees	Exhibit	1311	Petitioner	Yes
01/09/2015	'228 Request for Continued Examination	Exhibit	1312	Petitioner	Yes
01/09/2015	'228 Second Notice of Allowance and Fees	Exhibit	1313	Petitioner	Yes
01/09/2015	Infringement Contentions	Exhibit	1314	Petitioner	Yes
01/09/2015	Rembrandt's Markman Brief	Exhibit	1315	Petitioner	Yes
01/09/2015	'580 Application (as filed)	Exhibit	1316	Petitioner	Yes
01/09/2015	'580 Office Action Summary	Exhibit	1317	Petitioner	Yes
01/09/2015	'580 March 1, 2011 Reply	Exhibit	1318	Petitioner	Yes
01/09/2015	Rembrandt Tutorial Reference	Exhibit	1319	Petitioner	Yes
01/09/2015	IEEE Dictionary	Exhibit	1320	Petitioner	Yes
01/09/2015	Communications Dictionary	Exhibit	1321	Petitioner	Yes
01/09/2015	Mears Declaration and Upender	Exhibit	1322	Petitioner	Yes
01/09/2015	Goodman Declaration (Case IPR2014-00892)	Exhibit	1323	Petitioner	Yes
01/09/2015	U.S. Patent No. 5,537,398 (Siwiak)	Exhibit	1324	Petitioner	Yes
01/09/2015	Goodman Supplemental Declaration	Exhibit	1325	Petitioner	Yes
01/12/2015	Supplemental Mandatory Notice	Notice	4	Petitioner	Yes
01/29/2015	Notice of Filing Date Accorded	Notice of Filing Date Accorded to Petition	5	Board	Yes

01/30/2015	Power of Attorney	Power of Attorney	6	Potential Patent Owner	Yes
01/30/2015	Related Matters	Notice	7	Potential Patent Owner	Yes
02/02/2015	Order - Conduct of the Proceeding - 37 CFR 42.5	Order	8	Board	Yes
02/16/2015	PO Opposition to Joinder	Opposition	9	Patent Owner	Yes
02/16/2015	Ex. 2001 - Defs' Invalidity Contentions	Exhibit	2001	Patent Owner	Yes
02/16/2015	Ex. 2002 - Trial Transcript	Exhibit	2002	Patent Owner	Yes
02/26/2015	Petitioner's Reply to Opposition to Motion for Joinder	Reply	10	Petitioner	Yes
03/02/2015	Power of Attorney	Power of Attorney	11	Petitioner	Yes
03/20/2015	Petitioners_ Motion to Withdraw As Counsel (IPR2015-00555)	Motion	12	Petitioner	Yes
03/20/2015	Petitioners_ Motion to Change Designation of Lead Counsel (IPR2015-00555)	Motion	13	Petitioner	Yes
03/20/2015	Power of Attorney	Power of Attorney	14	Petitioner	Yes
03/25/2015	Petitioner's Unopposed Motion for Pro Hac Vice Admission of Brian P. Biddinger	Motion	15	Petitioner	Yes
03/27/2015	Order - re Petitioner's Motion to Withdraw Counsel	Order	16	Board	Yes
03/27/2015	DECISION - Petitioner's Motion for Pro Hac Vice Admission of Mr. Biddinger	Notice	17	Board	Yes
04/07/2015	Petitioners' Supplemental Mandatory Notice	Notice	18	Petitioner	Yes
04/29/2015	Patent Owner's Preliminary Response	Preliminary Response	19	Patent Owner	Yes
04/29/2015	Ex. 2003 - D. Ct. Claim Construction	Exhibit	2003	Patent Owner	Yes
04/29/2015	Ex. 2004 - Comp. Dict. of E.E.	Exhibit	2004	Patent Owner	Yes
04/29/2015	Ex. 2005 - Mod. Dict. of Elec.	Exhibit	2005	Patent Owner	Yes
04/29/2015	Ex. 2006 - Proakis I	Exhibit	2006	Patent Owner	Yes
04/29/2015	Ex. 2007 - Proakis II	Exhibit	2007	Patent Owner	Yes
04/29/2015	Ex. 2008 - Gast	Exhibit	2008	Patent Owner	Yes
06/19/2015	Decision Denial of Institution of Inter Partes Revew Denial of Motion for Joinder	Institution Decision	20	Board	Yes
06/29/2015	Petitioners' Request for Refund of Post-Institution Fees	Notice	21	Petitioner	Yes
06/30/2015	Notice of Refund	Notice	22	Board	Yes

United States Patent Trial and Appeals Board

US Patent Trial and Appeals Board - Alexandria
(Alexandria)

IPR2014-00893

Samsung Electronics Co. Ltd. Vs. Rembrandt Wireless Technologies, LP

This case was retrieved from the court on Wednesday, June 08, 2016

Docket

Case Number: **IPR2014-00893**

Date Filed: **06/04/2014**

Date Full Case Retrieved: **06/08/2016**

Status: **Closed**

Misc: **Civil**

Summary

Court Case Status: Final Decision

Case Type: IPR: Inter partes review

Date of Decision to Institute Case: 12/10/2014

Technical Center Number: 2600

Patent Application Number: 13198568

Patent Number: 8457228

Participants

Litigants

Samsung Electronics Co. Ltd.

Petitioner

Rembrandt Wireless Technologies, LP

PatentOwner

Proceedings

File Date	Details	Document Type	Paper/Exhibit	Filed By	Public?

			No.		
06/04/2014	Power of Attorney	Power of Attorney	1	Petitioner	Yes
06/04/2014	Petition for Inter Partes Review of U.S. Patent No. 8,457,228	Petition	2	Petitioner	Yes
06/04/2014	Patent US8,457,228	Exhibit	1401	Petitioner	Yes
06/04/2014	Complaint	Exhibit	1402	Petitioner	Yes
06/04/2014	Amended Complaint	Exhibit	1403	Petitioner	Yes
06/04/2014	Boer US5706428	Exhibit	1404	Petitioner	Yes
06/04/2014	Patent US6614838	Exhibit	1405	Petitioner	Yes
06/04/2014	838 June 28 2001 Office Action Summary	Exhibit	1406	Petitioner	Yes
06/04/2014	Oct 1 2001 Response	Exhibit	1407	Petitioner	Yes
06/04/2014	228 Application as Filed	Exhibit	1408	Petitioner	Yes
06/04/2014	228 4.30.2012 Office Action Summary	Exhibit	1409	Petitioner	Yes
06/04/2014	10.19.2012 OA Response	Exhibit	1410	Petitioner	Yes
06/04/2014	228 Notice of Allowance and Fees	Exhibit	1411	Petitioner	Yes
06/04/2014	Request for Continued Examination Transmittal	Exhibit	1412	Petitioner	Yes
06/04/2014	2nd Notice of Allowance and Fees	Exhibit	1413	Petitioner	Yes
06/04/2014	Infringement Contentions	Exhibit	1414	Petitioner	Yes
06/04/2014	Rembrandt Markman Brief	Exhibit	1415	Petitioner	Yes
06/04/2014	580 Application as Filed	Exhibit	1416	Petitioner	Yes
06/04/2014	580 Office Action Summary	Exhibit	1417	Petitioner	Yes
06/04/2014	580 3.1.2011 Reply	Exhibit	1418	Petitioner	Yes
06/04/2014	Rembrandt Tutorial Reference	Exhibit	1419	Petitioner	Yes
06/04/2014	IEEE Dictionary	Exhibit	1420	Petitioner	Yes
06/04/2014	Commuications Dictionary Master Slave	Exhibit	1421	Petitioner	Yes
06/04/2014	Mears Declaration and Upender	Exhibit	1422	Petitioner	Yes
06/04/2014	Goodman Declaration	Exhibit	1423	Petitioner	Yes
06/18/2014	Notice of Filing Date Accorded to Petition	Notice of Filing Date Accorded to Petition	3	Board	Yes
06/20/2014	Power of Attorney	Power of Attorney	4	Potential Patent Owner	Yes
06/20/2014	Related Matters	Notice	5	Potential Patent Owner	Yes
09/18/2014	PO Preliminary Response	Preliminary Response	6	Patent Owner	Yes

09/18/2014	Exhibit 2801	Exhibit	2801	Patent Owner	Yes
09/18/2014	Exhibit 2802	Exhibit	2802	Patent Owner	Yes
09/18/2014	Exhibit 2803	Exhibit	2803	Patent Owner	Yes
09/18/2014	Exhibit 2804	Exhibit	2804	Patent Owner	Yes
09/18/2014	Exhibit 2805	Exhibit	2805	Patent Owner	Yes
09/18/2014	Exhibit 2806	Exhibit	2806	Patent Owner	Yes
09/18/2014	Exhibit 2807	Exhibit	2807	Patent Owner	Yes
10/31/2014	Supplemental Mandatory Notice	Notice	7	Patent Owner	Yes
12/10/2014	Decision - Institution of Inter Partes Review 37 C.F.R. 42.108	Institution Decision	8	Board	Yes
12/10/2014	Scheduling Order	Notice	9	Board	Yes
12/10/2014	Patent Owner's Supplemental Mandatory Notice Information Under 37 C.F.R. 42.8	Notice	10	Patent Owner	Yes
12/16/2014	Patent Owner's List of Proposed Motions	Notice	11	Patent Owner	Yes
12/16/2014	Petitioner's List of Proposed Motions	Notice	12	Petitioner	Yes
12/19/2014	ORDER Conduct of Proceeding	Notice	13	Board	Yes
01/06/2015	Supplemental Mandatory Notice	Notice	14	Petitioner	Yes
01/09/2015	Supplemental Mandatory Notice	Notice	15	Petitioner	Yes
01/30/2015	PO Supplemental Mandatory Notice	Notice	16	Patent Owner	Yes
02/17/2015	Patent Owner's Response	Opposition	17	Patent Owner	Yes
02/17/2015	Exhibit 2808	Exhibit	2808	Patent Owner	Yes
02/17/2015	Exhibit 2809	Exhibit	2809	Patent Owner	Yes
02/17/2015	Exhibit 2810	Exhibit	2810	Patent Owner	Yes
02/17/2015	Exhibit 2811	Exhibit	2811	Patent Owner	Yes
02/17/2015	Exhibit 2812	Exhibit	2812	Patent Owner	Yes
02/17/2015	Exhibit 2813	Exhibit	2813	Patent Owner	Yes
02/17/2015	Exhibit 2814	Exhibit	2814	Patent Owner	Yes
02/17/2015	Exhibit 2815	Exhibit	2815	Patent	Yes

				Owner	
02/17/2015	Exhibit 2816	Exhibit	2816	Patent Owner	Yes
02/17/2015	Exhibit 2817	Exhibit	2817	Patent Owner	Yes
02/17/2015	Exhibit 2818	Exhibit	2818	Patent Owner	Yes
02/17/2015	Exhibit 2819	Exhibit	2819	Patent Owner	Yes
03/02/2015	Power of Attorney	Power of Attorney	18	Petitioner	Yes
03/20/2015	Petitioners_ Motion to Withdraw As Counsel (IPR2014-00893)	Motion	19	Petitioner	Yes
03/20/2015	Petitioners_ Motion to Change Designation of Lead Counsel (IPR2014-00893)	Motion	20	Petitioner	Yes
03/20/2015	Power of Attorney	Power of Attorney	21	Petitioner	Yes
03/25/2015	Petitioner's Unopposed Motion for Pro Hac Vice Admission of Brian P. Biddinger	Motion	22	Petitioner	Yes
03/26/2015	Order Conduct of Proceedings	Order	23	Board	Yes
03/27/2015	DECISION - Petitioner's Motion for Pro Hac Vice Admission of Mr. Biddinger	Notice	24	Board	Yes
04/07/2015	Petitioners' Supplemental Mandatory Notice	Notice	25	Petitioner	Yes
04/13/2015	Order - Conduct of the Proceeding - 37 CFR 42.5	Order	26	Board	Yes
04/23/2015	Petitioners' Reply In Support of Its Petition for IPR Review	Reply	27	Petitioner	Yes
04/23/2015	Deposition Transcript of Philip J. Koopman, Jr., Ph.D.	Exhibit	1424	Petitioner	Yes
04/23/2015	Data Network Evaluation Criteria Handbook, DOT/FAA/AR-09/24 Final Report, dated June 2009	Exhibit	1425	Petitioner	Yes
04/23/2015	Order Granting Motion for Fees and Costs dated August 29, 2012	Exhibit	1426	Petitioner	Yes
04/23/2015	Deposition Transcript of Dr. Christopher Jones, dated January 7, 2015	Exhibit	1427	Petitioner	Yes
04/23/2015	Illustration of DBPSK modulation drawn by Dr. Christopher Jones at deposition in IPR2014-518 and IPR2014-519, January 7, 2015	Exhibit	1428	Petitioner	Yes
04/23/2015	Illustration of 5 Mbps PPM/DQPSK modulation drawn by Dr. Christopher Jones at deposition in IPR2014-518 and IPR2014-519, January 7, 2015	Exhibit	1429	Petitioner	Yes
04/23/2015	Illustration of 8 Mbps PPM/DQPSK modulation drawn by Dr. Christopher Jones at deposition, January 7, 2015	Exhibit	1430	Petitioner	Yes
04/23/2015	Illustration by Dr. Christopher Jones drawn at deposition, January 7, 2015	Exhibit	1431	Petitioner	Yes

04/23/2015	Illustration by Dr. Christopher Jones drawn at deposition, January 7, 2015	Exhibit	1432	Petitioner	Yes
04/23/2015	Illustration by Dr. Christopher Jones drawn at deposition, January 7, 2015	Exhibit	1433	Petitioner	Yes
04/23/2015	Illustration by Dr. Christopher Jones drawn at deposition, January 7, 2015	Exhibit	1434	Petitioner	Yes
04/23/2015	Illustration by Dr. Christopher Jones drawn at deposition, January 7, 2015	Exhibit	1435	Petitioner	Yes
04/23/2015	U.S. Patent No. 5,450,404	Exhibit	1436	Petitioner	Yes
04/23/2015	U.S. Patent No. 5,436,901	Exhibit	1437	Petitioner	Yes
04/23/2015	U.S. Patent No. 5,535,212	Exhibit	1438	Petitioner	Yes
04/23/2015	Order Granting Toshiba America Information Systems Motion to Unseal Court Orders dated June 27, 2013.	Exhibit	1439	Petitioner	Yes
04/23/2015	Lab-Volt, Pulse Modulation and Sampling (PAM/PWM/PPM), Telecommunications Communications Technologies, at page V (Jan. 2010)	Exhibit	1440	Petitioner	Yes
04/23/2015	WIRELESS COMMUNICATION SYSTEMS - Cambridge University Press 2010	Exhibit	1441	Petitioner	Yes
05/29/2015	Power of Attorney	Power of Attorney	28	Patent Owner	Yes
05/29/2015	PO Supplemental Mandatory Notice	Notice	29	Patent Owner	Yes
06/05/2015	Order - Conduct of Proceeding - 37 CFR 42.5	Order	30	Board	Yes
06/11/2015	PO Identification of Information to be Stricken	Motion	31	Patent Owner	Yes
06/11/2015	Exhibit 3001 - Transcript of June 3, 2015 Conference Call	Exhibit	3001	Patent Owner	Yes
06/15/2015	PO Request for Oral Argument	Notice	32	Patent Owner	Yes
06/15/2015	Petitioners' Request for Oral Hearing	Notice	33	Petitioner	Yes
06/15/2015	PO Motion to Exclude	Motion	34	Patent Owner	Yes
06/15/2015	Ex. 2820 - PO Objections to Evidence Submitted with Reply	Exhibit	2820	Patent Owner	Yes
06/17/2015	Order Trial Hearing Notice	Notice	35	Board	Yes
06/17/2015	Power of Attorney	Power of Attorney	36	Patent Owner	Yes
06/17/2015	Patent Owner Supplemental Mandatory Notice	Notice	37	Patent Owner	Yes
06/18/2015	Petitioners' Response to PO's Identification of Matter to be Stricken from Petitioners' Reply	Reply	38	Petitioner	Yes
07/02/2015	Petitioner's Opposition to Patent Owner's Motion to Exclude Evidence	Opposition	39	Petitioner	Yes
07/02/2015	Wireless Communication Systems	Exhibit	1442	Petitioner	Yes

07/02/2015	Declaration of Meera Nair	Exhibit	1443	Petitioner	Yes
07/13/2015	PO Reply in support of Motion to Exclude	Reply	40	Patent Owner	Yes
07/17/2015	Petitioners' Updated Exhibit List - July 17, 2015	Notice	41	Petitioner	Yes
07/17/2015	Petitioners' Demonstratives	Exhibit	1444	Petitioner	Yes
07/29/2015	Order - re Request for Conference Call	Order	42	Board	Yes
09/16/2015	Record of Oral Hearing	Notice	43	Board	Yes
09/24/2015	Final Written Decision	Final Decision	44	Board	Yes

United States Patent Trial and Appeals Board

US Patent Trial and Appeals Board - Alexandria
(Alexandria)

IPR2014-00892

Samsung Electronics Co. Ltd. Vs. Rembrandt Wireless Technologies, LP

This case was retrieved from the court on Wednesday, June 08, 2016

Header

Case Number: **IPR2014-00892**

Date Filed: **06/04/2014**

Date Full Case Retrieved: **06/08/2016**

Status: **Closed**

Misc: **Civil**

Summary

Court Case Status: Final Decision

Case Type: IPR: Inter partes review

Date of Decision to Institute Case: 12/10/2014

Technical Center Number: 2600

Patent Application Number: 13198568

Patent Number: 8457228

Participants

Litigants

Samsung Electronics Co. Ltd.

Petitioner

Rembrandt Wireless Technologies, LP

PatentOwner

Proceedings

File Date	Details	Document Type	Paper/ Exhibit	Filed By	Public?

			No.		
06/04/2014	Power of Attorney	Power of Attorney	1	Petitioner	Yes
06/04/2014	Petition for Inter Partes Review of U.S. Patent No. 8,457,228	Petition	2	Petitioner	Yes
06/04/2014	Patent 8,457,228	Exhibit	1301	Petitioner	Yes
06/04/2014	Complaint	Exhibit	1302	Petitioner	Yes
06/04/2014	Amended Complaint	Exhibit	1303	Petitioner	Yes
06/04/2014	Boer US5706428	Exhibit	1304	Petitioner	Yes
06/04/2014	Patent No. US 6,614,838	Exhibit	1305	Petitioner	Yes
06/04/2014	838 June 28 2001 Office Action Summary	Exhibit	1306	Petitioner	Yes
06/04/2014	Oct 1 2001 Response	Exhibit	1307	Petitioner	Yes
06/04/2014	228 Application as Filed	Exhibit	1308	Petitioner	Yes
06/04/2014	228 4.30.2012 Office Action Summary	Exhibit	1309	Petitioner	Yes
06/04/2014	10.19.2012 OA Response	Exhibit	1310	Petitioner	Yes
06/04/2014	228 Notice of Allowance and Fees	Exhibit	1311	Petitioner	Yes
06/04/2014	Request for Continued Examination Transmittal	Exhibit	1312	Petitioner	Yes
06/04/2014	2nd Notice of Allowance and Fees	Exhibit	1313	Petitioner	Yes
06/04/2014	Infringement Contentions	Exhibit	1314	Petitioner	Yes
06/04/2014	Rembrandt Markman Brief	Exhibit	1315	Petitioner	Yes
06/04/2014	580 Application as Filed	Exhibit	1316	Petitioner	Yes
06/04/2014	580 Office Action Summary	Exhibit	1317	Petitioner	Yes
06/04/2014	580 3.1.2011 Reply	Exhibit	1318	Petitioner	Yes
06/04/2014	Rembrandt Tutorial Reference	Exhibit	1319	Petitioner	Yes
06/04/2014	IEEE Dictionary	Exhibit	1320	Petitioner	Yes
06/04/2014	Communications Dictionary Master Slave	Exhibit	1321	Petitioner	Yes
06/04/2014	Mears Declaration and Upender	Exhibit	1322	Petitioner	Yes
06/04/2014	Goodman Declaration	Exhibit	1323	Petitioner	Yes
06/18/2014	Notice of Filing Date Accorded to Petition	Notice of Filing Date Accorded to Petition	3	Board	Yes
06/20/2014	Power of Attorney	Power of Attorney	4	Potential Patent Owner	Yes
06/20/2014	Related Matters	Notice	5	Potential Patent Owner	Yes
09/18/2014	PO Preliminary Response	Preliminary Response	6	Patent Owner	Yes

09/18/2014	Exhibit 2701	Exhibit	2701	Patent Owner	Yes
09/18/2014	Exhibit 2702	Exhibit	2702	Patent Owner	Yes
09/18/2014	Exhibit 2703	Exhibit	2703	Patent Owner	Yes
09/18/2014	Exhibit 2704	Exhibit	2704	Patent Owner	Yes
09/18/2014	Exhibit 2705	Exhibit	2705	Patent Owner	Yes
09/18/2014	Exhibit 2706	Exhibit	2706	Patent Owner	Yes
09/18/2014	Exhibit 2707	Exhibit	2707	Patent Owner	Yes
10/31/2014	Supplemental Mandatory Notice	Notice	7	Patent Owner	Yes
12/10/2014	Decision - Institution of Inter Partes Review 37 C.F.R. 42.108	Institution Decision	8	Board	Yes
12/10/2014	Scheduling Order	Notice	9	Board	Yes
12/10/2014	Patent Owner's Supplemental Mandatory Notice Information Under 37 C.F.R. 42.8	Notice	10	Patent Owner	Yes
12/16/2014	Patent Owner's List of Proposed Motions	Notice	11	Patent Owner	Yes
12/16/2014	Petitioners List of Proposed Motions	Notice	12	Petitioner	Yes
12/19/2014	ORDER Conduct of Proceeding	Notice	13	Board	Yes
12/23/2014	Petitioner Request for Rehearing	Rehearing Request	14	Petitioner	Yes
01/06/2015	Supplemental Mandatory Notice	Notice	15	Petitioner	Yes
01/09/2015	Supplemental Mandatory Notice	Notice	16	Petitioner	Yes
01/27/2015	DECISION Request for Rehearing	Notice	17	Board	Yes
01/30/2015	PO Supplemental Mandatory Notice	Notice	18	Patent Owner	Yes
02/17/2015	Patent Owner's Response	Opposition	19	Patent Owner	Yes
02/17/2015	Exhibit 2708	Exhibit	2708	Patent Owner	Yes
02/17/2015	Exhibit 2709	Exhibit	2709	Patent Owner	Yes
02/17/2015	Exhibit 2710	Exhibit	2710	Patent Owner	Yes
02/17/2015	Exhibit 2711	Exhibit	2711	Patent Owner	Yes
02/17/2015	Exhibit 2712	Exhibit	2712	Patent Owner	Yes
02/17/2015	Exhibit 2713	Exhibit	2713	Patent Owner	Yes

02/17/2015	Exhibit 2714	Exhibit	2714	Patent Owner	Yes
02/17/2015	Exhibit 2715	Exhibit	2715	Patent Owner	Yes
02/17/2015	Exhibit 2716	Exhibit	2716	Patent Owner	Yes
02/17/2015	Exhibit 2717	Exhibit	2717	Patent Owner	Yes
02/17/2015	Exhibit 2718	Exhibit	2718	Patent Owner	Yes
02/17/2015	Exhibit 2719	Exhibit	2719	Patent Owner	Yes
03/02/2015	Power of Attorney	Power of Attorney	20	Petitioner	Yes
03/20/2015	Petitioners_ Motion to Withdraw As Counsel (IPR2014-00892)	Motion	21	Petitioner	Yes
03/20/2015	Petitioners_ Motion to Change Designation of Lead Counsel (IPR2014-00892)	Motion	22	Petitioner	Yes
03/20/2015	Power of Attorney	Power of Attorney	23	Petitioner	Yes
03/25/2015	Petitioner's Unopposed Motion for Pro Hac Vice Admission of Brian P. Biddinger	Motion	24	Petitioner	Yes
03/26/2015	Order Conduct of Proceedings	Order	25	Board	Yes
03/27/2015	DECISION - Petitioner's Motion for Pro Hac Vice Admission of Mr. Biddinger	Notice	26	Board	Yes
04/07/2015	Petitioners' Supplemental Mandatory Notice	Notice	27	Petitioner	Yes
04/13/2015	Order - Conduct of Proceeding - 37 CFR 42.5	Order	28	Board	Yes
04/23/2015	Petitioners' Reply In Support of Its Petition for IPR Review	Reply	29	Petitioner	Yes
04/23/2015	Deposition Transcript of Philip J. Koopman, Jr., Ph.D., dated January 13, 2015	Exhibit	1324	Petitioner	Yes
04/23/2015	Data Network Evaluation Criteria Handbook, dated June 2009	Exhibit	1325	Petitioner	Yes
04/23/2015	Order Granting Motion for Fees and Costs, dated August 29, 2012.	Exhibit	1326	Petitioner	Yes
04/23/2015	Deposition Transcript of Dr. Christopher Jones, dated January 7, 2015	Exhibit	1327	Petitioner	Yes
04/23/2015	Illustration of DBPSK modulation drawn by Dr. Christopher Jones at deposition, January 7, 2015	Exhibit	1328	Petitioner	Yes
04/23/2015	Illustration of 5 Mbps PPM/DQPSK modulation drawn by Dr. Christopher Jones at deposition, January 7, 2015	Exhibit	1329	Petitioner	Yes
04/23/2015	Illustration of 8 Mbps PPM/DQPSK modulation drawn by Dr. Christopher Jones at deposition, January 7, 2015	Exhibit	1330	Petitioner	Yes
04/23/2015	Illustration by Dr. Christopher Jones drawn at deposition, January 7, 2015	Exhibit	1331	Petitioner	Yes

04/23/2015	Illustration by Dr. Christopher Jones drawn at deposition, January 7, 2015	Exhibit	1332	Petitioner	Yes
04/23/2015	Illustration by Dr. Christopher Jones drawn at deposition, January 7, 2015	Exhibit	1333	Petitioner	Yes
04/23/2015	Illustration by Dr. Christopher Jones drawn at deposition, January 7, 2015	Exhibit	1334	Petitioner	Yes
04/23/2015	Illustration by Dr. Christopher Jones drawn at deposition, January 7, 2015	Exhibit	1335	Petitioner	Yes
04/23/2015	U.S. Patent No. 5,450,404	Exhibit	1336	Petitioner	Yes
04/23/2015	U.S. Patent No. 5,436,901	Exhibit	1337	Petitioner	Yes
04/23/2015	U.S. Patent No. 5,535,212	Exhibit	1338	Petitioner	Yes
04/23/2015	Order Granting Toshiba America Information Systems Motion to Unseal Court Orders, dated June 27, 2013.	Exhibit	1339	Petitioner	Yes
04/23/2015	Telecommunications Communications Technologies, at page V - January 2010	Exhibit	1340	Petitioner	Yes
04/23/2015	WIRELESS COMMUNICATION SYSTEMS - Cambridge University Press 2010	Exhibit	1341	Petitioner	Yes
05/29/2015	Power of Attorney	Power of Attorney	30	Patent Owner	Yes
05/29/2015	PO Supplemental Mandatory Notice	Notice	31	Patent Owner	Yes
06/05/2015	Order - Conduct of Proceeding - 37 CFR 42.5	Order	32	Board	Yes
06/11/2015	PO Identification of Information to be Stricken	Motion	33	Patent Owner	Yes
06/11/2015	Exhibit 3001 - Transcript of June 3, 2015 Conference Call	Exhibit	3001	Patent Owner	Yes
06/15/2015	PO Request for Oral Argument	Notice	34	Patent Owner	Yes
06/15/2015	Petitioners' Request for Oral Hearing	Notice	35	Petitioner	Yes
06/15/2015	PO Motion to Exclude	Motion	36	Patent Owner	Yes
06/15/2015	Ex. 2720 - PO Objections to Evidence Submitted with Reply	Exhibit	2720	Patent Owner	Yes
06/17/2015	Order Trial Hearing Notice	Notice	37	Board	Yes
06/17/2015	Power of Attorney	Power of Attorney	38	Patent Owner	Yes
06/17/2015	Patent Owner Supplemental Mandatory Notice	Notice	39	Patent Owner	Yes
06/18/2015	Petitioners' Resonse to PO's Identification of Matter to be Stricken from Petitioners' Reply	Reply	40	Petitioner	Yes
07/02/2015	Petitioner's Opposition to Patent Owner's Motion to Exclude Evidence	Opposition	41	Petitioner	Yes
07/02/2015	Wireless Communication Systems	Exhibit	1342	Petitioner	Yes
07/02/2015	Declaration of Meera Nair	Exhibit	1343	Petitioner	Yes

07/13/2015	PO Reply in support of Motion to Exclude	Reply	42	Patent Owner	Yes
07/17/2015	Petitioners' Updated Exhibit List - July 17, 2015	Notice	43	Petitioner	Yes
07/17/2015	Petitioners' Demonstratives	Exhibit	1344	Petitioner	Yes
07/29/2015	Order - re Request for Conference Call	Order	44	Board	Yes
09/16/2015	Record of Oral Hearing	Notice	45	Board	Yes
09/24/2015	Final Written Decision	Final Decision	46	Board	Yes

United States Patent Trial and Appeals Board

US Patent Trial and Appeals Board - Alexandria
(Alexandria)

IPR2014-00891

Samsung Electronics Co. Ltd. Vs. Rembrandt Wireless Technologies, LP

This case was retrieved from the court on Wednesday, June 08, 2016

Docket

Case Number: **IPR2014-00891**

Date Filed: **06/04/2014**

Date Full Case Retrieved: **06/08/2016**

Status: **Open**

Misc: **Civil**

Summary

Court Case Status: Not Instituted

Case Type: IPR: Inter partes review

Date of Decision to Institute Case: 12/10/2014

Technical Center Number: 2600

Patent Application Number: 13198568

Patent Number: 8457228

Participants

Litigants

Samsung Electronics Co. Ltd.

Petitioner

Rembrandt Wireless Technologies, LP

PatentOwner

Proceedings

File Date	Details	Document Type	Paper/ Exhibit	Filed By	Public?

			No.		
06/04/2014	Power of Attorney	Power of Attorney	1	Petitioner	Yes
06/04/2014	Petition for Inter Partes Review of U.S. Patent No. 8,457,228	Petition	2	Petitioner	Yes
06/04/2014	Patent 8,457,228	Exhibit	1201	Petitioner	Yes
06/04/2014	Complaint	Exhibit	1202	Petitioner	Yes
06/04/2014	Amended Complaint	Exhibit	1203	Petitioner	Yes
06/04/2014	Draft 802.11 Std	Exhibit	1204	Petitioner	Yes
06/04/2014	802.11 Std	Exhibit	1205	Petitioner	Yes
06/04/2014	Boer US5706428	Exhibit	1206	Petitioner	Yes
06/04/2014	Information Disclosure Statement	Exhibit	1207	Petitioner	Yes
06/04/2014	Patent No. 6614838	Exhibit	1208	Petitioner	Yes
06/04/2014	838 June 28 2001 Office Action Summary	Exhibit	1209	Petitioner	Yes
06/04/2014	Oct 1 2001 Response	Exhibit	1210	Petitioner	Yes
06/04/2014	228 Application as Filed	Exhibit	1211	Petitioner	Yes
06/04/2014	228 4.30.2012 Office Action Summary	Exhibit	1212	Petitioner	Yes
06/04/2014	228 10.19.2012 OA Response	Exhibit	1213	Petitioner	Yes
06/04/2014	228 1st Notice of Allowance and Fees	Exhibit	1214	Petitioner	Yes
06/04/2014	228 Request for Continued Examination Transmittal	Exhibit	1215	Petitioner	Yes
06/04/2014	228 2nd Notice of Allowance and Fees	Exhibit	1216	Petitioner	Yes
06/04/2014	Infringement Contentions	Exhibit	1217	Petitioner	Yes
06/04/2014	Rembrandt Markman Brief	Exhibit	1218	Petitioner	Yes
06/04/2014	580 Application as Filed	Exhibit	1219	Petitioner	Yes
06/04/2014	580 Office Action Summary	Exhibit	1220	Petitioner	Yes
06/04/2014	580 3.1.2011 Reply	Exhibit	1221	Petitioner	Yes
06/04/2014	Rembrandt Tutorial Reference	Exhibit	1222	Petitioner	Yes
06/04/2014	IEEE Dictionary	Exhibit	1223	Petitioner	Yes
06/04/2014	Commuications Dictionary Master Slave	Exhibit	1224	Petitioner	Yes
06/04/2014	O'Hara Declaration	Exhibit	1225	Petitioner	Yes
06/04/2014	Cafarella US5809060	Exhibit	1226	Petitioner	Yes
06/04/2014	Bialkowiski US5574910	Exhibit	1227	Petitioner	Yes
06/04/2014	Goodman Declaration	Exhibit	1228	Petitioner	Yes
06/18/2014	Notice of Filing Date Accorded to Petition	Notice of Filing Date Accorded to Petition	3	Board	Yes
06/20/2014	Power of Attorney	Power of Attorney	4	Potential	Yes

				Patent Owner	
06/20/2014	Related Matters	Notice	5	Potential Patent Owner	Yes
09/18/2014	PO Preliminary Response	Preliminary Response	6	Patent Owner	Yes
09/18/2014	Exhibit 2601	Exhibit	2601	Patent Owner	Yes
09/18/2014	Exhibit 2602	Exhibit	2602	Patent Owner	Yes
09/18/2014	Exhibit 2603	Exhibit	2603	Patent Owner	Yes
09/18/2014	Exhibit 2604	Exhibit	2604	Patent Owner	Yes
09/18/2014	Exhibit 2605	Exhibit	2605	Patent Owner	Yes
09/18/2014	Exhibit 2606	Exhibit	2606	Patent Owner	Yes
09/18/2014	Exhibit 2607	Exhibit	2607	Patent Owner	Yes
09/18/2014	Exhibit 2608	Exhibit	2608	Patent Owner	Yes
09/18/2014	Exhibit 2609	Exhibit	2609	Patent Owner	Yes
09/18/2014	Exhibit 2610	Exhibit	2610	Patent Owner	Yes
09/18/2014	Exhibit 2611	Exhibit	2611	Patent Owner	Yes
09/18/2014	Exhibit 2612	Exhibit	2612	Patent Owner	Yes
09/18/2014	Exhibit 2613	Exhibit	2613	Patent Owner	Yes
10/31/2014	Supplemental Mandatory Notice	Notice	7	Patent Owner	Yes
12/10/2014	Decision - Denying Institution of Inter Partes Review 37 C.F.R. 42.108	Institution Decision	8	Board	Yes
12/10/2014	Patent Owner's Supplemental Mandatory Notice Information Under 37 C.F.R. 42.8	Notice	9	Patent Owner	Yes
03/10/2015	IPR2014-00891 - Refund request	Refund Request	10	Petitioner	Yes
03/19/2015	Notice of Refund	Notice	11	Board	Yes

United States Patent Trial and Appeals Board

US Patent Trial and Appeals Board - Alexandria
(Alexandria)

IPR2014-00890

Samsung Electronics Co. Ltd. Vs. Rembrandt Wireless Technologies, LP

This case was retrieved from the court on Wednesday, June 08, 2016

Header

Case Number: **IPR2014-00890**

Date Filed: **06/04/2014**

Date Full Case Retrieved: **06/08/2016**

Status: **Open**

Misc: **Civil**

Summary

Court Case Status: Not Instituted

Case Type: IPR: Inter partes review

Date of Decision to Institute Case: 12/10/2014

Technical Center Number: 2600

Patent Application Number: 13198568

Patent Number: 8457228

Participants

Litigants

Samsung Electronics Co. Ltd.

Petitioner

Rembrandt Wireless Technologies, LP

PatentOwner

Proceedings

File Date	Details	Document Type	Paper/ Exhibit	Filed By	Public?

			No.		
06/04/2014	Power of Attorney	Power of Attorney	1	Petitioner	Yes
06/04/2014	Petition for Inter Partes Review of U.S. Patent No. 8,457,228	Petition	2	Petitioner	Yes
06/04/2014	Patent 8,457,228	Exhibit	1101	Petitioner	Yes
06/04/2014	Complaint	Exhibit	1102	Petitioner	Yes
06/04/2014	Amended Complaint	Exhibit	1103	Petitioner	Yes
06/04/2014	Draft 802.11 Std	Exhibit	1104	Petitioner	Yes
06/04/2014	802.11 Std	Exhibit	1105	Petitioner	Yes
06/04/2014	Boer US5706428	Exhibit	1106	Petitioner	Yes
06/04/2014	Information Disclosure Statement	Exhibit	1107	Petitioner	Yes
06/04/2014	228 Application as Filed	Exhibit	1108	Petitioner	Yes
06/04/2014	228 4.30.2012 Office Action Summary	Exhibit	1109	Petitioner	Yes
06/04/2014	228 4.30.2012 Office Action Response	Exhibit	1110	Petitioner	Yes
06/04/2014	228 First Notice of Allowance and Fees Due	Exhibit	1111	Petitioner	Yes
06/04/2014	228 Request for Continued Examination/Transmittal	Exhibit	1112	Petitioner	Yes
06/04/2014	2nd Notice of Allowance and Fees Due	Exhibit	1113	Petitioner	Yes
06/04/2014	Infringement Contentions	Exhibit	1114	Petitioner	Yes
06/04/2014	Rembrandt Markman Brief	Exhibit	1115	Petitioner	Yes
06/04/2014	580 Application as Filed	Exhibit	1116	Petitioner	Yes
06/04/2014	580 Office Action Summary	Exhibit	1117	Petitioner	Yes
06/04/2014	580 3.1.2011 Reply	Exhibit	1118	Petitioner	Yes
06/04/2014	Rembrandt Tutorial Reference	Exhibit	1119	Petitioner	Yes
06/04/2014	IEEE Dictionary	Exhibit	1120	Petitioner	Yes
06/04/2014	Commuications Dictionary Master Slave	Exhibit	1121	Petitioner	Yes
06/04/2014	O'Hara Declaration	Exhibit	1122	Petitioner	Yes
06/04/2014	Goodman Declaration	Exhibit	1123	Petitioner	Yes
06/18/2014	Notice of Filing Date Accorded to Petition	Notice of Filing Date Accorded to Petition	3	Board	Yes
06/20/2014	Power of Attorney	Power of Attorney	4	Potential Patent Owner	Yes
06/20/2014	Related Matters	Notice	5	Potential Patent Owner	Yes
09/18/2014	PO Preliminary Response	Preliminary Response	6	Patent Owner	Yes
09/18/2014	Exhibit 2501	Exhibit	2501	Patent Owner	Yes

09/18/2014	Exhibit 2502	Exhibit	2502	Patent Owner	Yes
09/18/2014	Exhibit 2503	Exhibit	2503	Patent Owner	Yes
09/18/2014	Exhibit 2504	Exhibit	2504	Patent Owner	Yes
09/18/2014	Exhibit 2505	Exhibit	2505	Patent Owner	Yes
09/18/2014	Exhibit 2506	Exhibit	2506	Patent Owner	Yes
09/18/2014	Exhibit 2507	Exhibit	2507	Patent Owner	Yes
09/18/2014	Exhibit 2508	Exhibit	2508	Patent Owner	Yes
09/18/2014	Exhibit 2509	Exhibit	2509	Patent Owner	Yes
09/18/2014	Exhibit 2510	Exhibit	2510	Patent Owner	Yes
09/18/2014	Exhibit 2511	Exhibit	2511	Patent Owner	Yes
09/18/2014	Exhibit 2512	Exhibit	2512	Patent Owner	Yes
09/18/2014	Exhibit 2513	Exhibit	2513	Patent Owner	Yes
10/31/2014	Supplemental Mandatory Notice	Notice	7	Patent Owner	Yes
12/10/2014	Decision - Denying Institution of Inter Partes Review 37 C.F.R. 42.108	Institution Decision	8	Board	Yes
12/10/2014	Patent Owner's Supplemental Mandatory Notice Information Under 37 C.F.R. 42.8	Notice	9	Patent Owner	Yes
03/10/2015	IPR2014-00890 - Refund request	Refund Request	10	Petitioner	Yes
03/18/2015	Notice of Refund	Notice	11	Board	Yes

Negative Treatment

Negative Direct History

The KeyCited document has been negatively impacted in the following ways by events or decisions in the same litigation or proceedings:

1. SYSTEM AND METHOD OF COMMUNICATION USING AT LEAST TWO MODULATION METHODS

US PAT 8457228 , U.S. PTO Utility , June 04, 2013

Ruled Unpatentable in Part by

2. SAMSUNG ELECTRONICS CO. LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA, LLC, AND SAMSUNG AUSTIN SEMICONDUCTOR, LLC, PETITIONER, v. REMBRANDT WIRELESS TECHNOLOGIES, LP, PATENT OWNER.

2015 WL 5719795 , Patent Tr. & App. Bd. , Sep. 24, 2015

AND Ruled Unpatentable in Part by

3. SAMSUNG ELECTRONICS CO. LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA, LLC, AND SAMSUNG AUSTIN SEMICONDUCTOR, LLC, PETITIONER, v. REMBRANDT WIRELESS TECHNOLOGIES, LP, PATENT OWNER.

2015 WL 5719796 , Patent Tr. & App. Bd. , Sep. 24, 2015

AND Ruled Unpatentable in Part by

4. SAMSUNG ELECTRONICS CO. LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA, LLC, AND SAMSUNG AUSTIN SEMICONDUCTOR, LLC, PETITIONER, v. REMBRANDT WIRELESS TECHNOLOGIES, LP, PATENT OWNER.

2015 WL 5719797 , Patent Tr. & App. Bd. , Sep. 24, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/013,809	09/12/2016	8457228	3277-0114US-RXM2	7821

6449 7590 01/08/2019

ROTHWELL, FIGG, ERNST & MANBECK, P.C.
607 14th Street, N.W.
SUITE 800
WASHINGTON, DC 20005

EXAMINER
WEAVER, SCOTT LOUIS

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
01/08/2019	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

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(THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS)

ROPES & GRAY LLP
IPRM DOCKETING - FLOOR 43
PRUDENTIAL TOWER
800 BOYLSTON STREET
BOSTON, MA 02199-3600

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/013,809* .

PATENT UNDER REEXAMINATION *8457228* .

ART UNIT *3992* .

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Notice of Intent to Issue Ex Parte Reexamination Certificate	**Control No.** 90/013,809	**Patent Under Reexamination** 8457228	
	Examiner SCOTT L WEAVER	**Art Unit** 3992	**AIA Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☑ Prosecution on the merits is (or remains) closed in this *ex parte* reexamination proceeding. This proceeding is subject to reopening at the initiative of the Office or upon petition. *Cf.* 37 CFR 1.313(a). A Certificate will be issued in view of
   (a) ☑ Patent owner's communication(s) filed: 21 December 2018.
   (b) ☐ Patent owner's failure to file an appropriate timely response to the Office action mailed: _____.
   (c) ☐ Patent owner's failure to timely file an Appeal Brief (37 CFR 41.31).
   (d) ☐ The decision on appeal by the ☐ Board of Patent Appeals and Interferences ☐ Court dated _____
   (e) ☐ Other: _____.
2. The Reexamination Certificate will indicate the following:
   (a) Change in the Specification: ☐ Yes ☑ No
   (b) Change in the Drawing(s): ☐ Yes ☑ No
   (c) Status of the Claim(s):
      (1) Patent claim(s) confirmed: 21.
      (2) Patent claim(s) amended (including dependent on amended claim(s)): _____
      (3) Patent claim(s) canceled: _____.
      (4) Newly presented claim(s) patentable: _____.
      (5) Newly presented canceled claims: _____.
      (6) Patent claim(s) ☐ previously ☐ currently disclaimed: _____
      (7) Patent claim(s) not subject to reexamination: 4,6-9,24,30,32-35,42 and 44-46.
3. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
4. ☑ Note the attached statement of reasons for patentability and/or confirmation. Any comments considered necessary by patent owner regarding reasons for patentability and/or confirmation must be submitted promptly to avoid processing delays. Such submission(s) should be labeled: "Comments On Statement of Reasons for Patentability and/or Confirmation."
5. ☐ Note attached NOTICE OF REFERENCES CITED (PTO-892).
6. ☐ Note attached LIST OF REFERENCES CITED (PTO/SB/08 or PTO/SB/08 substitute).
7. ☐ The drawing correction request filed on _____ is: ☐approved ☐disapproved.
8. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐None of the certified copies have
   ☐been received.
   ☐not been received.
   ☐been filed in Application No. _____.
   ☐been filed in reexamination Control No. _____.
   ☐been received by the International Bureau in PCT Application No. _____.

   * Certified copies not received: _____.
9. ☐ Note attached Examiner's Amendment.
10. ☐ Note attached Interview Summary (PTO-474).
11. ☐ Other: _____.

All correspondence relating to this reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this Office action.

/Scott L. Weaver/ Primary Examiner, Art Unit 3992	/Stephen Stein/ /Yuzhen Ge/ MQAS, CRU Primary Examiner, Art Unit 3992

cc: Requester (if third party requester)

REEXAMINATION OF U.S. PATENT 8,457,228

Notice of Intent to Issue a Reexamination Certificate (NIRC)

This NIRC addresses the *ex parte* reexamination of U.S. Patent No. 8,457,228 ("the '228 Patent).

I. PATENTABLE/CONFIRMED SUBJECT MATTER

Claim 21 is confirmed. Below is the reason for the confirmation:

As acknowledged by the Patent Owner, the 8,457,228 Patent expired on December 5, 2018. The patent term of the Patent 8,457,228 is effected by the Terminal Disclaimers filed in application 13/198,568 on October 19, 2012 disclaiming the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent No. 6,614,838 and of prior patent No. 8,023,580.

Therefore, the broadest reasonable interpretation of claim terms reciting "the second modulation method being of a different type than the first modulation method" as relied on in the prior office action is no longer considered the appropriate interpretation for the claim in this reexamination proceeding.

The Federal Circuit, in *Rembrandt Wireless Technologies v. Samsung Electronics Co.*, 853 15 F.3d 1370, 1375-77 (Fed. Cir. 2017), applied a Phillips claim construction and determined that the limitation 'modulation method of a different type' in claim 21 required at least two "different families of modulation techniques, such as the FSK family of modulation methods and the QAM family of modulation methods." Id. at 1377. And likewise in related Patent No. 8,023,580, the claim limitations, including the "at least two types of modulation methods" or "different types of modulation method," is now interpreted under *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316, 75 USPQ2d 1321, 1329 (Fed. Cir. 2005).

Because the prior art on the record does not teach the first and second modulation methods being of 'different types of modulation methods' which are interpreted as different families of modulation techniques such as the FSK family of modulation methods and the QAM family of modulation methods, claims 21 is confirmed.

II. Status of Claims

Claim 21 is subject of the instant 90/013,809 Reexamination Proceeding.

Claim 21 is confirmed patentable.

Claims 1-3, 5, 10-20, 22-23, 25-29, 31, 36-41, 43, and 47-52 are canceled in the certificate issued December 13, 2016 as result of the Decision in IPR2014-00892.

Claims 4, 6-9, 24, 30, 32-35, 42, and 44-46 were not subject to reexamination.

III. CONCLUSION

The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving the instant '228 patent throughout the course of this reexamination proceeding.

Any third party requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286.

Extensions of time under 37 CFR 1.136(a) do not apply in reexamination proceedings. The provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Further, in 35 U.S.C. 305 and in 37 CFR 1.550(a), it is required that reexamination proceedings "will be conducted with special dispatch within the Office."
All correspondence relating to this ex parte reexamination proceeding should be directed:

By Mail to:

Mail Stop Ex Parte Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to:

(571) 273-9900
Central Reexamination Unit

By hand:

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Registered users of EFS-Web may alternatively submit such correspondence via the electronic filing system EFS-Web, at https://efs.uspto.gov/efile/myportal/efs-registered. EFS-Web offers the benefit of quick submission to the particular area of the Office that needs to act on the correspondence. Also, EFS-Web submissions are "soft scanned" (i.e., electronically uploaded) directly into the official file for the reexamination proceeding, which offers parties the

opportunity to review the content of their submissions after the "soft scanning" process is complete.

Any inquiry concerning this communication or earlier communications from the examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

/Scott L. Weaver/
Primary Examiner, Art Unit 3992

Conferees:
/YUZHEN GE/
Primary Examiner, Art Unit 3992

/Stephen Stein/
MQAS
CRU

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/013,809	8457228
	Examiner	Art Unit
	SCOTT L WEAVER	3992

CPC - Searched*		
Symbol	Date	Examiner
H04W84/20	4/20/17	SLW
H04L5/1453	4/20/17	SLW
H04L27/0008	4/20/17	SLW

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Review Applicaiton File Histories 8,457,228 and related Continuation parent cases	4/20/17	SLW

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
H04L	5/1453	01/03/2019	SLW

Reexamination	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/013,809	8457228
	Certificate Date	Certificate Number
		C1

Requester Correspondence Address: ☐ **Patent Owner** ☑ **Third Party**

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BOSTON, MA 02199-3600

LITIGATION REVIEW ☑	SLW (examiner initials)	03 January 2019 (date)
Case Name		Director Initials
IPR2015-00555 Samsung Electronics Co. Vs. Rembrandt Wireless Technologies, LP		SJS for JC
IIPR2014-00889		
IPR2014-00890		
IPR2014-00891		
IPR2014-00892		
IPR2014-00893		
IPR2014-00895		

COPENDING OFFICE PROCEEDINGS	
TYPE OF PROCEEDING	**NUMBER**
Ex Parte Reexamination	90/013808

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/013,809	8457228
	Examiner	**Art Unit**
	SCOTT L WEAVER	3992

CPC						
Symbol					**Type**	**Version**
H04L	/	5	/	1453	F	2013-01-01
H04L	/	25	/	0262	I	2013-01-01
H04L	/	1	/	206	I	2013-01-01
H04L	/	27	/	0008	I	2013-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	1	
/Scott L. Weaver/ Primary Examiner, Art Unit 3992	02 January 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	8

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/013,809	8457228
	Examiner	Art Unit
	SCOTT L WEAVER	3992

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H04L	/	5	/	12

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
375	261

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
455	102					
332	108	119	151			

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	1	
/Scott L. Weaver/ Primary Examiner, Art Unit 3992	02 January 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	8

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/013,809	8457228
	Examiner	**Art Unit**
	SCOTT L WEAVER	3992

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10		19		28		37		46				
	2		11		20		29		38		47				
	3		12	21	21		30		39		48				
	4		13		22		31		40		49				
	5		14		23		32		41		50				
	6		15		24		33		42		51				
	7		16		25		34		43		52				
	8		17		26		35		44						
	9		18		27		36		45						

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	1	
/Scott L. Weaver/ Primary Examiner, Art Unit 3992	02 January 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	8

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/013,809	8457228
	Examiner	Art Unit
	SCOTT L WEAVER	3992

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/02/2017	10/18/2018	01/02/2019						
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	42									

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/013,809	8457228
	Examiner	Art Unit
	SCOTT L WEAVER	3992

CLAIM		DATE								
Final	Original	03/02/2017	10/18/2018	01/02/2019						
	43									
	44									
	45									
	46									
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	48									
	49									
	50									
	51									
	52									

/SLW/
OK to Enter

01/03/2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In *Ex Parte* Reexamination of : Group Art Unit: 3992

Gordon F. BREMER :

Patent No.: 8,457,228 : Control No.: 90/013,809

Issued: June 4, 2013 :

Reexam Request Filed: September 12, 2016

For: SYSTEM AND METHOD OF COMMUNICATION USING AT LEAST TWO MODULATION METHODS

Mail Stop *Ex Parte* Reexam
ATTN: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO FINAL OFFICE ACTION

In this above-referenced reexamination of claim 21 of U.S. Patent No. 8,457,228 ("the '228 Patent"), the Office issued a final Office action on November 5, 2018 ("FOA"). This Response to the FOA is timely-filed, i.e., within the two-month period from the mailing date of the FOA. Thus, this Response includes a request to extend the shortened statutory period for an additional two months, i.e., to March 5, 2019. *See* MPEP § 2265(VII).

Notice of Expiration of U.S. Patent No. 8,457,228

Rembrandt submits this response to notify the Office that the '228 Patent expired on December 5, 2018, a fact that impacts the reexamination in that it requires a claim construction under *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316, 75 USPQ2d 1321, 1329 (Fed. Cir. 2005), and one consistent with the Federal Circuit's previous construction of claim 21 of the '228 Patent and claims 2 and 59 of its parent, U.S. Patent No. 8,023,580 ("the '580 Patent"). The Office's present construction under the broadest reasonable interpretation cannot stand.

In view of the '228 Patent's expiration, Rembrandt requests that the Office (1) construe claim 21, including the "at least two types of modulation methods" limitations, under *Phillips*, (2) confirm the patentability of claim 21 under that construction, and (3) issue a NIRC consistent with this determination, as the Office has now done in the parent case U.S. Patent No. 8,023,580 (also under reexamination).

The proper claim construction of the '228 Patent under *Phillips* is a question of law that was finally and conclusively resolved in Rembrandt's favor by the Federal Circuit in *Rembrandt Wireless Technologies v. Samsung Electronics Co.*, 853 F.3d 1370, 1375-77 (Fed. Cir. 2017) -- an appeal brought by Samsung (the Requestor of this reexamination). The criticisms raised by the Office to Rembrandt's construction of "different types" were raised by the Requestor and were rejected by the Federal Circuit. As a result, the proper construction of the '228 Patent under *Phillips* is now settled law, and the Office is required to apply the Federal Circuit's claim construction going forward in this matter. *See, e.g., In re CSB-System International*, 832 F.3d 1335, 1341 (Fed. Cir. 2016 ("When a patent expires during a reexamination proceeding, the PTO should thereafter apply the *Phillips* standard for claim construction."). The court in *CSB-System* cited *Facebook, Inc. v. Pragmatus AV, LLC*, 582 Fed. Appx. 864, 868-69 (Fed. Cir. 2014) and noted that the court in *Facebook* "appl[ied] the *Phillips* standard when patent expired after the Board's reexamination decision pending appeal to the Federal Circuit." 832 F.3d at 1341; MPEP § 2258(I)(G) ("In a reexamination proceeding involving claims of an expired patent, claim construction pursuant to the principle set forth by the court in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316, 75 USPQ2d 1321, 1329 (Fed. Cir. 2005) … should be applied since the expired claim are not subject to amendment. …").

In the related district court litigation, *Rembrandt Wireless Technologies v. Samsung Electronics Co.*, 853 F.3d 1370, 1375-77 (Fed. Cir. 2017), both the district court and the Federal Circuit applied a *Phillips* claim construction and determined that the limitation "modulation method [] of a different type" in claim 21 required at least two "different families of modulation techniques, such as the FSK family of modulation methods and the QAM family of modulation methods." *Id.* at 1377. The Office in this reexamination and the Board in the related IPRs refused to construe "modulation method [] of a different type" to require at least two "different families of modulation techniques." Instead, it construed the claims under an alleged "broadest reasonable interpretation" and determined that their construction did not require at least two "different families of modulation techniques." Given that the '228 Patent has expired, application of the broadest reasonable interpretation is no longer proper and cannot stand. Thus, Rembrandt respectfully requests that the outstanding rejections be reconsidered in light of the expiration of the '228 Patent and of the proper construction of "at least two different types" to require at least two "different families of modulation techniques," as Rembrandt previously requested prior to the '228 Patent's expiration. *See, e.g.,* Rembrandt's August 14, 2017 Response to the May 3, 2017 non-final Office action ("August 14 Response"), at 50-52, 59-69; Claim Construction Order (Exhibit C to Response) and Akl Declaration, ¶¶ 18-27 (submitted with and cited in the Response).

Additionally, Rembrandt submits the Declaration of Dr. Christopher R. Jones (Ex. 2714 in IPR2014-00892) (attached as Ex. A), in which Dr. Jones explains why the modulation methods disclosed in Boer do not satisfy the limitations of claim 21 that require different modulation types (ones that are not in the same family), when properly construed under *Phillips*.

Jones Decl. ¶¶ 28-41, 44, & 55-62. Dr. Jones' testimony regarding Boer would apply with at least equal force to the disclosure of BPSK and QPSK in Snell and Harris.

The Office's NIRC in the Reexamination of the Parent Patent No. 8,023,580

In a NIRC dated December 21, 2018, the Office confirmed the patentability of all the claims under reexamination in the parent patent, U.S. Patent No. 8,023,580 ("the '580 Patent"), which also expired on December 5, 2018. The NIRC acknowledges that "the broadest reasonable interpretation of claim terms is no longer proper for the claims" in the '580 reexamination. *Id.* at 2. It further acknowledges that the claim limitations "including the 'at least two types of modulation methods' or 'different types of modulation method,' should be interpreted under Phillips v. AWH Corp., 415 F.3d 1303, 1316 … (Fed. Cir. 2005)." *Id.*

The NIRC then explains that the Federal Circuit had "applied a Phillips claim construction and determined that the limitation 'modulation of a different type' in claims 2 and 59 required at least two 'different families of modulation techniques, such as the FSK family of modulation methods and the QAM family of modulation methods.'" *Id.* The same holds true for claim 21 of the '228 Patent, as the Federal Circuit determined. *See Rembrandt Wireless Technologies v. Samsung Electronics Co.*, 853 F.3d 1370, *passim* (Fed. Cir. 2017) (construing the term in both the '580 and '228 Patents). Based on that construction, the Office concluded: "Because the prior art on the record does not teach different types of modulation methods as different families of modulation techniques such as the FSK family of modulation methods and the QAM family of modulation methods, claims 2 and 59 [of the '580 Patent] are confirmed." *Id.* For the same reason, the Office should confirm the patentability of claim 21 of the '228 Patent, as the prior art of record in the '228 reexamination does not teach the different types of

modulation methods required when construed as it must be construed under *Phillips* and Federal Circuit law.

Conclusion

Given the expiration of the '228 Patent, the Federal Circuit's claim construction under *Phillips* of different types of modulation methods, and the Office's determination in the '580 reexamination, Rembrandt respectfully requests that the Office withdraw its rejections of claim 21 in the '228 reexamination and issue a NIRC, consistent with its action it the '580 reexamination.

Any fee required for this submission may be charged to Counsel's Deposit Account Number 02-2135.

Respectfully submitted,

Date: December 21, 2018 By: /Michael V. Battaglia/

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Attorney for Petitioner
Rembrandt Wireless Technologies, LP

cc: Nancy J. Linck, Ph.D.
Counsel for Rembrandt Wireless Technologies, LP

Bibliographic Data

Application No: 90/013,809

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /Scott L. Weaver/ Examiner's Signature | Initials

Title: SYSTEM AND METHOD OF COMMUNICATION USING AT LEAST TWO MODULATION METHODS

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/12/2016	375	3992	3277-0114US-RXM2
RULE			

APPLICANTS

INVENTORS

8457228

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SAMSUNG ELECTRONICS AMERICA, INC. (3RD PTY REQ.) RIDGEFIELD PARK, NJ, UNITED STATES

CONTINUING DATA

This application is a REX of 13198568 08/04/2011 PAT 8457228

13198568 is a CON of 12543910 08/19/2009 PAT 8023580

12543910 is a CON of 11774803 07/09/2007 PAT 7675965

11774803 is a CON of 10412878 04/14/2003 PAT 7248626

10412878 is a CIP of 09205205 12/04/1998 PAT 6614838

09205205 has PRO of 60067562 12/05/1997

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

STATE OR COUNTRY

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WASHINGTON, DC 20005

UNITED STATES

FILING FEE RECEIVED

$12,000

US008457228C1

(12) EX PARTE REEXAMINATION CERTIFICATE (11450th)
United States Patent
Bremer

(10) Number: US 8,457,228 C1
(45) Certificate Issued: *Jan. 28, 2019

(54) **SYSTEM AND METHOD OF COMMUNICATION USING AT LEAST TWO MODULATION METHODS**

(75) Inventor: **Gordon F. Bremer**, Clearwater, FL (US)

(73) Assignee: **REMBRANDT WIRELESS TECHNOLOGIES, LP**, Arlington, VA (US)

Reexamination Request:
No. 90/013,809, Sep. 12, 2016

Reexamination Certificate for:
Patent No.: **8,457,228**
Issued: **Jun. 4, 2013**
Appl. No.: **13/198,568**
Filed: **Aug. 4, 2011**

(*) Notice: This patent is subject to a terminal disclaimer.

Related U.S. Application Data

(63) Continuation of application No. 12/543,910, filed on Aug. 19, 2009, now Pat. No. 8,023,580, which is a continuation of application No. 11/774,803, filed on Jul. 9, 2007, now Pat. No. 7,675,965, which is a continuation of application No. 10/412,878, filed on Apr. 14, 2003, now Pat. No. 7,248,626, which is a continuation-in-part of application No. 09/205,205, filed on Dec. 4, 1998, now Pat. No. 6,614,838.

(60) Provisional application No. 60/067,562, filed on Dec. 5, 1997.

(51) **Int. Cl.**

H04L 5/12	(2006.01)
H04L 5/14	(2006.01)
H04L 25/02	(2006.01)
H04L 1/20	(2006.01)
H04L 27/00	(2006.01)

(52) **U.S. Cl.**
CPC ***H04L 5/1453*** (2013.01); ***H04L 1/206*** (2013.01); ***H04L 25/0262*** (2013.01); ***H04L 27/0008*** (2013.01)

(58) **Field of Classification Search**
CPC ... H04W 84/20; H04L 5/1453; H04L 27/0008
See application file for complete search history.

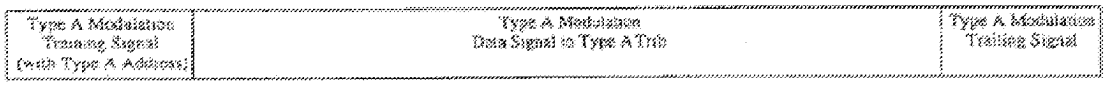
(56) **References Cited**

To view the complete listing of prior art documents cited during the proceeding for Reexamination Control Number 90/013,809, please refer to the USPTO's public Patent Application Information Retrieval (PAIR) system under the Display References tab.

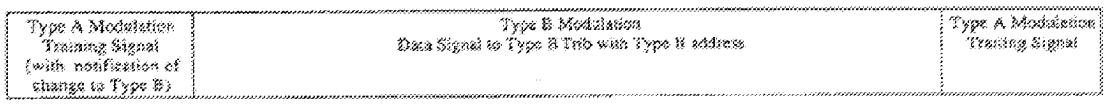
Primary Examiner — Scott L. Weaver

(57) **ABSTRACT**

A device may be capable of communicating using at least two type types of modulation methods. Methods and systems are provided for communication of data according to a communications method in which a master transceiver communicates with one or more slave transceivers according to a master/slave relationship. A first data message may include first information and second information that are modulated according to a first modulation method. The second information may include lower data rate data. A second data message may include third information that may be modulated according to the first modulation method and that may indicate an impending change to a second modulation method. The second modulation method may be used for transmitting fourth information, and the fourth information may be included in the second message. The fourth information may include higher data rate data, for example Internet access data.



170



172

EX PARTE REEXAMINATION CERTIFICATE

NO AMENDMENTS HAVE BEEN MADE TO THE PATENT

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claim **21** is confirmed.

Claims **1-3**, **5**, **10-20**, **22-23**, **25-29**, **31**, **36-41**, **43** and **47-52** were previously cancelled.

Claims **4**, **6-9**, **24**, **30**, **32-35**, **42** and **44-46** were not reexamined.

* * * * *