Beschreibung

Die vorliegende Erfindung betrifft ein Richtfunksystem für Punkt-zu-Mehrpunkt-Verbindungen, bei dem die für die Kommunikation zwischen einer Zentralstation und mehreren Teilnehmern zur Verfügung stehenden Frequenzkanäle bedarfsweise zuteilbar sind.

Ein solches Richtfunksystem ist im Mikrokwellen-Magazin, Vol. 10, No. 6, 1984, S. 629, 630 erwähnt. Bei Punkt-zu-Mehrpunkt-Richtfunkverbindungen läßt sich demnach die Frequenzbandausnutzung durch eine nur bedarfsweise Belegung des erforderlichen Freqenzbandes verbessern. Die Kommunikation zwischen der Zentralstation und den einzelnen Teilnehmern erfolgt entweder durch Vielfachzugriff im Frequenzmultiplex (FDMA) oder durch Vielfachzugriff im Zeitmultiplex (TDMA), wobei die Frequenzkanäle oder Zeitschlitze je nach Bedarf der Teilnehmer zugeteilt werden.

Aus EP 0 169 713 A3 ist ein Duplex-Übertragungssystem bekannt. Dabei erfolgt lediglich zwischen zwei Sende/Empfangs-Stationen eine Sprachübertragung entweder nur in eine Richtung (Simplex-Übertragung) oder in beide Richtungen (Duplex-Übertragung) gleichzeitig. Für eine Simplex-Übertragung wird ein Übertragungskanal zur Verfügung gestellt, der eine größere Bandbreite aufweist als jeder der zwei für eine Duplex-Übertragung bereitgestellten Übertragungskanäle. Dazu werden die Datenraten der übertragenen Signale an die Bandbreite der ihnen jeweils zugeordneten Übertragungskanäle angepaßt.

Bei einem aus der WO-A-93/00751 bekannten Datenübertragungssystem werden die Sendesignalpegel so geregelt, daß sich eine optimale Übertragungsqualität einstellt.

Der Erfindung liegt die Aufgabe zugrunde, ein Richtfunksystem der eingangs genannten Art anzugeben, dessen Übertragungskapazität möglichst flexibel an den Bedarf der Teilnehmer angepaßt werden kann.

Erfindungsgemäß wird diese Aufgabe durch die Merkmale des Anspruchs 1 gelöst. Vorteilhafte Weiterbildungen der Erfindung gehen aus den Unteransprüchen hervor.

Punkt-zu-Mehrpunkt Richtfunksysteme stellen eine kostengünstige und mit geringem Aufwand realisierbare Alternative zu leitergebundenen Übertragungssystemen dar. Dies gilt in besonderem Maße für neue Netzbetreiber im Rahmen des Aufbaus eigener Telekommunikationsinfrastruktur.

Ein nach der Erfindung ausgeführtes Punkt-zu-Mehrpunkt Richtfunksystem kann seine Übertragungsbandbreitenkapazität an verschiedene von den einzelnen Teilnehmern geforderte Datenübertragungsraten anpassen. Damit stellt ein solches System ein frequenzökonomisches, am Bedarf der einzelnen Teilnehmer orientiertes Übertragungsmedium dar.

Anhand eines in der Zeichnung dargestellten Ausführungsbeispiels wird nun die Erfindung näher erläutert.

Die Figur zeigt ein Frequenzkanalraster.

Ein Punkt-zu-Mehrpunkt Richtfunksystem besteht aus einer Zentralstation mit einer in Azimutrichtung rundstrahlenden oder sektorisiert strahlenden Antenne und mehreren Teilnehmern, welche mit Richtantennen ausgestattet sind. Prinzipiell weisen die Zentralstation und die einzelnen Teilnehmer in bekannter Weise Hochfrequenz-Sende/Empfangs-Baugruppen, Umsetzer von der Hochfrequenz- in die Zwischenfrequenzebene und im Zwischenfrequenzbereich arbeitende Modulatoren und Demodulatoren auf.

Die Modulatoren und Demodulatoren in der Zentralstation sind so ausgelegt, daß ein Zwischenfrequenzträger mit einer variablen Datenrate, z.B. im Bereich von 64 KBit/s bis maximal 8 MBit/s, modulierbar bzw. demodulierbar ist. D.h. die Zentralstation kann - z.B. softwaregesteuert - jedem Teilnehmer einen Frequenzkanal zur Verfügung stellen, dessen Bandbreite an die vom jeweiligen Teilnehmer geforderte Datenübertragungsrate angepaßt ist. Das in der Zeichnung dargestellte Frequenzkanalraster enthält beispielhaft zwei Frequenzkanäle 1 und 5 für eine Datenrate von 2 MBit/s, zwei weitere Frequenzkanäle 2 und 4 für eine Datenrate von 64 KBit/s und einen Frequenzkanal 3 für eine Datenrate von 1 MBit/s. Die Lage der einzelnen Kanäle relativ zu der Mittenfrequenz f_m des Übertragungsbandes wird zweckmäßigerweise so organisiert, daß die Kanäle symmetrisch um die Mittenfrequenz f_m herum verteilt sind (vgl. Figur). Die maximal mögliche Anzahl der den Teilnehmern zugeordneten Kanäle ist durch die Kanalrasterung, den zulässigen spektralen Abstand und die kanalindividuelle Datenrate bestimmt.

In der Zentralstation können die von den Teilnehmern geforderten Kanalbandbreiten registriert werden, damit für jeden Teilnehmer eine von der Übertragungsbandbreite abhängige Tarifierung möglich ist.

Modulatoren und Demodulatoren können auch für verschiedene Modulationsarten (z.B. n - PSK, n - QPSK mit n = 1 ... 8 oder M - QAM mit M = 4 ... 256) ausgelegt werden, so daß Datenübertragungen mit teilnehmerindividuell unterschiedlichen Modulationen möglich sind.

Um entfernungsabhängige Empfangspegelunterschiede ausgleichen zu können, ist in der Zentralstation eine entsprechende Verstärkungsregelung für die Sendesignale vorgesehen.

Patentansprüche

1. Richtfunksystem für Punkt-zu-Mehrpunkt Verbindungen, bei dem die für die Kommunikation zwischen einer Zentralstation und mehreren Teilnehmern zur Verfügung stehenden Frequenzkanäle bedarfsweise zuteilbar sind, dadurch gekennzeichnet, daß die Bandbreite der einzelnen Frequenzkanäle (1 ... 5) auf die von den einzelnen Teilnehmern jeweils geforderte Datenübertragungsrate einstellbar ist.

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2. Richtfunksystem nach Anspruch 1, dadurch gekennzeichnet, daß die Verstärkung der Sendesignale regelbar ist, so daß entfernungsabhängige Unterschiede der Empfangssignalpegel ausgeglichen werden können.

3. Richtfunksystem nach Anspruch 1, dadurch gekennzeichnet, daß Modulatoren und Demodulatoren auf verschiedene Modulationsarten einstellbar sind.

4. Richtfunksystem nach Anspruch 1, dadurch gekennzeichnet, daß die Zentralstation für die einzelnen Teilnehmer eine von der Übertragungsbandbreite abhängige Tarifierung vornimmt.

Claims

1. Microwave system for point-to-multipoint links, in which the frequency channels which are available for communication between a central station and a plurality of subscribers can be assigned according to requirements, characterized in that the bandwidth of the individual frequency channels (1 ... 5) can be adjusted to the data transmission rate respectively required by the individual subscribers.

2. Microwave system according to Claim 1, characterized in that the amplification of the transmission signals can be regulated, so that distance-dependent differences in the reception signal levels can be compensated.

3. Microwave system according to Claim 1, characterized in that modulators and demodulators can be adjusted to different types of modulation.

4. Microwave system according to Claim 1, characterized in that the central station performs tariff metering for the individual subscribers as a function of the transmission bandwidth.

Revendications

1. Système de radiodiffusion par faisceau dirigé entre un point et plusieurs points, selon lequel les canaux de fréquence disponibles pour la communication entre une station centrale et plusieurs abonnés peuvent être attribués à la demande,
caractérisé en ce que
la largeur de bande des différents canaux de fréquence (1 ... 5) se règle sur le débit de données de transmission demandé par chacun des abonnés.

2. Système de radiodiffusion par faisceau dirigé selon la revendication 1,
caractérisé en ce que
l'amplification des signaux d'émission est réglable pour permettre de compenser des différences de niveau de signal de réception dépendant de l'éloignement.

3. Système de radiodiffusion par faisceau dirigé selon la revendication 1,
caractérisé en ce que
les modulateurs et démodulateurs peuvent être réglés sur différents types de modulation.

4. Système de radiodiffusion par faisceau dirigé selon la revendication 1,
caractérisé en ce que
la station centrale réalise une tarification dépendant de la largeur de la bande de transmission de chaque abonné.

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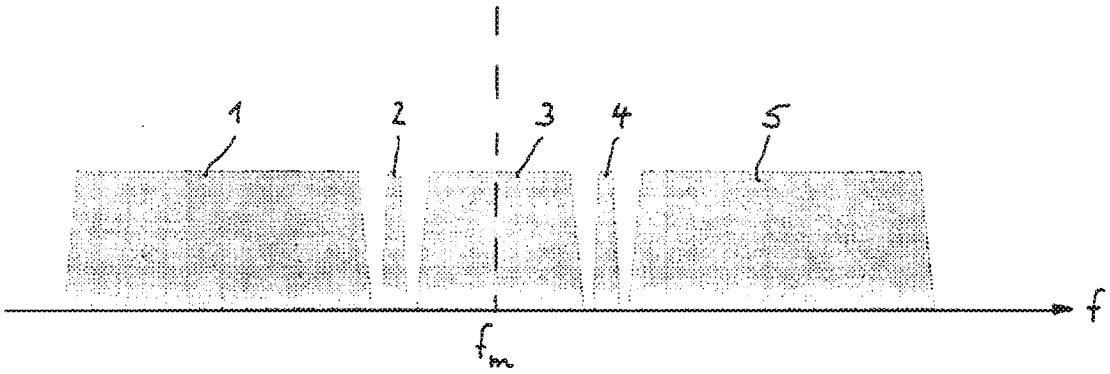

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(54) Digital signal detecting method and detector

Verfahren zum Erfassen eines digitalen Signals und Detektor

Procédé de détection d'un signal numérique et détecteur

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- **DATABASE WPI Section El, Week 9349 Derwent Publications Ltd., London, GB; Class U22, AN 93-390790 XP002069781 & JP 05 291 859 A (HITACHI LTD)**

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Description

[0001] The present invention relates to a digital signal detecting method which permits the reception of signals modulated by different modulation schemes and send signals of various symbol transmission rates and a detector therefor.

[0002] To realize future multimedia communications, there is a demand for techniques of transmitting data, speech and images over the same digital radio channel. One possible means for effectively transmitting data, speech and images by digital radio communication is to use symbol transmission rates and modulation/demodulation schemes optimum for the objects to be transmitted. In the field of mobile communication, for instance, it is to be wished that the base station offer a service of providing still pictures of television, data bank or the like, whereas the mobile station be capable of receiving such still pictures from the base station by simple operation with simple equipment as well as conducting usual voice communications. In this instance, a QPSK modulation scheme is usually employed for the voice communication but a QAM or similar multilevel modulation scheme is needed for the transmission of still pictures because of the necessity for transmitting a larger amount of information than that required for the voice communication. This requirement could be met by providing independent transmitters and receivers each corresponding to a particular modulation/demodulation scheme as shown in Fig. 1A, in which the transmitting station is provided with a transmitter group 10 consisting of, for example, QAM, PSK and FSK modulating transmitters 11, 12 and 13 and the receiving station is provided with a receiver group 20 consisting of QAM, PSK and FSK receivers. Another method is common to the above in the provision of the independent transmitters 11, 12 and 13 at the transmitting side but differs therefrom in that the receiving station is equipped with a single receiver 21 with QAM, PSK and FSK detectors 22, 23 and 24 built therein as shown in Fig. 1B. One possible method for providing a plurality of detectors in the same radio as shown in Fig. 1B is to build therein independent detectors each designed specifically for one modulation/demodulation scheme.

[0003] At present, mobile communication services are allocated 800 and 1500 MHz bands but cannot be switched back and forth between them. If the bands can be switched by a simple operation with a simple structure, however, cochannel interference can be reduced by using the 800 MHz band outdoors and the 1500 MHz band indoors and in closed spaces through utilization of a property that the linearity of electric waves in the 1500 MHz band is higher than in the 800 MHz band.

[0004] The device configuration depicted in Fig. 1B has a plurality of independent detectors built-in, and hence it is inevitably bulky and complex. Furthermore, in the digital radio communication for transmitting data, speech and images, it is hard to instantaneously switch the independent detectors by dynamically changing the demodulating scheme and the carrier frequency. The receiver 21 quadrature-demodulates the received signal, for which it is necessary to generate a local oscillation signal synchronized with the carrier of the input received signal. In this instance, if the carrier frequency of the received signal varies from f_1 to f_2, f_3, and f_4 with the lapse of time as shown in Fig. 2A, the frequency of the local oscillation signal also needs to vary correspondingly. To meet this requirement, it is general practice in the prior art to employ such a method as shown in Fig. 2B, in which the oscillation frequency of a PLL local oscillator 25 is switched by switching means 17 to f_1, f_2, f_3 and f_4 one after another as indicated by local oscillators 25_1, 25_2, 25_3 and 25_4, then the output from the switched local oscillator and the input modulated signal are multiplied by an multiplier 18 and the multiplied output is applied to a filter 19 to obtain a base band signal. The frequency switching speed in the PLL local oscillator 25 is several milliseconds at the highest even by the use of a digital loop preset type frequency synthesizer. With such a low response speed, it is impossible to fully respond to the frequency switching during communication.

[0005] For example, when the symbol transmission rate of the received signal varies from B_1 to B_2, B_3, and B_4 with the lapse of time as shown in Fig. 2C, it is conventional that filters 261, 262, 263 and 264 for filtering the output from a quadrature demodulator are switched one after another by switching means 27 and 28 in response to the variation in the transmission rate of the received signal as depicted in Fig. 2D. Since the filters are formed by hardware, the filter switching speed cannot be increased because of transient characteristics of the filters.

[0006] US-A-5,259,000 discloses a modulator-demodulator constructed of digital circuits that is intended to provide a simple, economical modulator-demodulator apparatus, wherein two MODEMs are provided for G3 facsimile and G2/G1 facsimile which are selectively used by controlling a switch in accordance with the received signal. The functions of the respective facsimile modes are implemented by a digital signal processor, but it is assumed that different algorithms are used for different facsimile modes and the characteristics of each function that implements a corresponding facsimile mode are not changed. The document also shows the use of interpolation; however, the interpolation is performed to increase Signal-to-Noise Power Ratio to thereby avoid degradation in detection when the eye-pattern is closed by change in transmission rate or increase the in number of values of multi-value modulation (M-ary modulation scheme).

[0007] The document *Fines P et al: "Fully Digital M-ary PSK and M-ary QAM demodulators for land mobile satellite communications" Electronics and Communication Engineering Journal, Vol.3, No. 6, 1 December* 1991, *pages* 291-298, *XP000277949* discloses the use of an adaptive filter, and sets of coefficients of the adaptive filter are predetermined and stored in a memory. The document also teaches the use of interpolation, but the purpose is the same as that in

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US-A-5,259,000.

[0008] US-A-3,497,625 relates to digital modulation and demodulation, wherein a desired one of plural types of modulation scheme (and demodulation scheme) is selectively operated.

[0009] The document D4 *SAMUELI H ET AL: "VLSI architectures* for a *high-speed tunable digital modulator/demodulator/bandpass filter chip set", 1992 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS (CAT. No. 92CH3139-3), SAN DIEGO, CA, USA, 10-13 MAY 1992, ISBN 0-7803-0593-0, 1992, NEW YORK, NY, USA, pages 1065-1068 vol.3, XP002069780* relates to an all-digital multirate modulator/demodulator of a 3-chip set, wherein in the first chip a double-sideband IF signal is subjected to a Hilbert transform to obtain a complex single-sideband signal, in the second chip the single-sideband signal is quadrature-demodulated to produce a baseband signal and in the third chip the baseband signal is decimated to effect lowpass-filtering of a selected bandwidth. The document D4 does not teach the use of interpolation and decimation for enhancing time-resolution of quadrature-demodulation.

[0010] It is therefore an object of the present invention to provide a digital signal detecting method and a detector therefor which enable digital communication equipment having a plurality of detecting means built-in to be used in common to pluralities of modulation/demodulation schemes, local oscillation frequencies and symbol transmission rates.

[0011] Another object of the present invention is to provide a digital signal detecting method and a detector therefor which are capable of responding fast to the switching of the modulation schemes and a change in the symbol transmission rate.

SUMMARY OF THE INVENTION

[0012] These objects are achieved by a method as claimed in claim 1 and a detector as claimed in claim 20. Preferred embodiments of the invention are subject-matter of the dpendent claims.

[0013] A feature of the present invention is to obtain a base band signal by subjecting an AD converted received signal to digital signal processing implemented by software.

[0014] The digital signal detecting method according to the present invention comprises: a quadrature-demodulating step of performing a quadrature-demodulating operation of an AD converted received modulated signal; a filtering step of performing a filtering operation of the quadrature-demodulated signal to obtain a base band signal; and a control step of changing at least one process variable in at least one of the quadrature-demodulating step and the filtering step in response to a request for changing the process variable.

[0015] The quadrature-demodulating step comprises: an interpolating step of performing an n-point interpolation of the input modulated digital signal to interpolate therein samples at n points (n being a real number equal to or greater than 1); a multiplying step of complex-multiplying the interpolation result by a local oscillation signal; and a decimating step of performing an n-point decimation of the multiplication result to decimate therefrom samples at n points. The process variables that can be changed in the quadrature demodulation step are the frequency, amplitude and phase of the local oscillation signal and the value of the above-mentioned n.

[0016] The filtering step comprises a smoothing step of smoothing the result of the quadrature-demodulating operation to reduce the number of samples; and a digital filtering step of performing a band-limiting operation of the result of the smoothing operation. The process variables in the band-limiting step are the number of smoothing points and the characteristic of the digital filter used.

[0017] Further, the input modulated signal is gain controlled by an automatic gain controller for input into an AD converter as a signal of a predetermined level range.

[0018] The above-mentioned various processes are performed by a microprocessor which decodes and executes programs.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019]

Fig. 1A is a block diagram schematically showing an example of a digital mobile radio communication system employing a plurality of different modulation/demodulation schemes;

Fig. 1B is a block diagram schematically showing an example of a digital mobile radio communication system employing a receiver which contains a plurality of detectors each corresponding to one of the modulation/demodulation schemes in Fig. 1A;

Fig. 2A is a graph showing variations in the carrier frequency of a received signal with the lapse of time;

Fig. 2B is a diagram showing a conventional method for changing the local oscillation frequency of a detector in response to the variations in the carrier frequency shown in Fig. 2A;

Fig. 2C is a graph showing variations in the symbol transmission rate of the received signal with the lapse of time;

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Fig. 2D is a diagram showing a conventional method for switching band-limiting filters of a detector in response to the variations in the symbol transmission rate shown in Fig. 2C;
Fig. 3 is a block diagram illustrating the functional configuration of the detector according to the present invention;
Fig. 4A is a block diagram illustrating a concrete example of the functional construction of quadrature demodulating means 33 in Fig. 3;
Fig. 4B is a flowchart showing an example of a procedure for automatic synchronization of the local oscillation signal with the input received signal;
Fig. 5A is a diagram explanatory of n-point interpolation processing by an FFT technique;
Fig. 5B is a diagram explanatory of a method for performing the n-point interpolation processing by an interpolation algorithm using an m-order function;
Fig. 5C is a diagram explanatory of a method for performing the n-point interpolation processing by a method of estimating samples to be interpolated by an interpolation algorithm;
Fig. 6A is a diagram explanatory of n-point decimation processing by a simple decimation method;
Fig. 6B is a diagram explanatory of n-point decimation processing by a weighted substitution method;
Fig. 7 is a block diagram illustrating a concrete example of the functional configuration of filter means 43 in Fig. 3;
Fig. 8A is a diagram explanatory of smoothing processing by a simple extraction method;
Fig. 8B is a block diagram showing an example of the functional configuration for another smoothing scheme;
Fig. 8C is a diagram for explaining the operation of the Fig. 8B configuration;
Fig. 9A through 9H are diagrams showing the states of signals occurring at respective parts of the digital detector according to the present invention;
Fig. 10A is a block diagram illustrating an example of the functional configuration for switching the oscillation frequency in the quadrature demodulating means 33 in Fig. 3;
Fig. 10B is a block diagram showing an example of the functional configuration for switching the local oscillation frequency in the filter means 34 in Fig. 3;
Fig. 11 is a block diagram illustrating an example of the functional configuration for carrying out this invention method;
Fig. 12 is a flowchart showing an example of the procedure of the detecting method according to the present invention;
Fig. 13 is a flowchart showing an example of the digital detecting procedure;
Fig. 14 is a diagram showing an example of the frame structure of the received signal;
Fig. 15 is a block diagram illustrating an example of the functional configuration in which a microprocessor for use in the present invention is utilized for other processing;
Fig. 16 is a block diagram illustrating the functional configuration of a transceiver embodying the present invention;
Fig. 17A is a table showing, by way of example, stored contents of a process variable storage part;
Fig. 17B is a table showing, by way of example, some of other stored contents of the process variable storage part; and
Fig. 17C is a table showing, by way of example, stored contents in other areas of the storage part of Fig. 17B.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0020] Referring now to Fig. 3, an embodiment of the present invention will be described below. An analog signal received at an input terminal 30 is provided via a band pass filter (not shown) to an automatic gain controller 31, which controls, with its amplification gain, the received signal so that its amplitude varies within a fixed range. The output analog signal from the automatic gain controller 31 is converted by an AD converter 32 to a digital signal. The received signal thus converted into digital form is subjected to demodulating operation by quadrature demodulating means 33 and is spectrum shaped by filtering operation by digital filter means 34, from which a demodulated digital base band signal is provided at an output terminal 40. The base band signal is provided to decision means 39, wherein its in-phase component and quadrature component are each decided in terms of the symbol period, and based on these decision results, it is determined which signal point on the IQ-diagram the base band signal corresponds to. For example, in the case of a QPSK signal, it is decided whether its in-phase component and quadrature component are +1 or -1, and based on the decision results, it is determined which of four signal points on the IQ-diagram the baseband signal corresponds to.

[0021] In Fig. 3, the arithmetic processing for the digital signal by the quadrature demodulating means 33 and the digital filter means 34 is implemented by software which uses the sampling frequency, the symbol transmission rate, the modulation scheme and the local oscillation frequency as arguments (variables). Control means 35 has software for controlling the automatic gain controller 31, the quadrature demodulating means 33 and the digital filter means 34. The control means 35 controls the automatic gain controller 31 to vary its amplification gain to limit the amplitude variation of the base band signal to a fixed range. The control means 35 controls arguments set in the quadrature

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demodulating means 33 and the digital filter means 34 in response to changes in the sampling frequency, the symbol transmission rate and the modulation scheme of the digitized modulated signal and the local oscillation frequency. A keyboard or similar set/input means 36 is connected to the control means 35. The set/input means 36 has pluralities of keys indicating several sampling frequencies, several symbol transmission rates and several local oscillation frequencies, respectively, and a desired parameter is input by pressing the corresponding one of the keys indicating several parameters of each category. Alternatively, the input means 36 is provided with keys each indicating the sampling frequency, the symbol transmission rate and the local oscillation frequency and has a construction in which a desired parameter can be input by pressing the corresponding key and its numerical value can be set and input by manipulating ten keys. Further, the set/input means 36 has a plurality of keys respectively indicating modulation schemes so that the modulation scheme of the received signal can be input.

[0022] As described above, the digital signal processing by the quadrature demodulating means 33 and the digital filter means 34, which uses the sampling frequency, the symbol transmission rate, the modulation scheme and the local oscillation frequency as variables, can be implemented by software. By controlling the gain of the automatic gain controller 31 and the variables with the software of the control means 35, it is possible to construct a digital signal detector which performs an operation corresponding to a parameter specified in one of the groups of modulation schemes, local oscillation frequencies and symbol transmission rates.

[0023] Fig. 4A shows a preferred configuration of the quadrature demodulating means 33 in Fig. 3. The output digital signal from the AD converter 32 is subjected to an n-point interpolation by n-point interpolation means 41_I and 41_Q, whereby samples are interpolated in the digital signal at n points on the time base. The interpolated signals are fed to multiplying means 42_I and 42_Q, wherein they are multiplied by 90°-out-of-phase signals $f_{LI}(k)$ and $f_{LQ}(k)$from local oscillation means 45. The outputs from the multiplying means 42_I and 42_Q are subjected to an n-point decimation by n-point decimation means 43_I and 43_Q, whereby samples are decimated from the multiplied outputs at n points on the time base. By this decimation processing, the samples interpolated by the n-point interpolation means 41_I and 41_Q are decimated from the multiplied outputs, whereby the in-phase and quadrature components of the demodulated signal from the quadrature demodulation means 33 can be obtained. The time resolution for the multiplication processing can be scaled up by the n-point interpolation means 41_I and 41_Q. The scaled-up time resolution permits the establishment of synchronization between the digitized modulated signals and the local oscillation signals with high accuracy, and the time resolution of the multiplied outputs is scaled down by the n-point decimation means 43_I and 43_Q, lessening the load of subsequent digital signal processing. The multiplying means 42_I and 42_Q constitute a complex multiplying means 42.

[0024] A description will be given of the arithmetic operation by the quadrature demodulating means 33. The input analog signal (an IF signal) y(t) to the AD converter 32 can be expressed by the following equation.

$$y(t) = A(t)\cos\{\omega t+\varphi(t)\} \tag{1}$$

where t is time, ω is $2\pi f$ (where f is the carrier frequency), A(t) is the envelope and $\varphi(t)$ is the phase. The analog signal y(t) is sampled by the AD converter 32 every sampling time T_s and each sample value is converted to a digital signal. Letting m denote an integer, the time t and the sampling time T_s bear the following relationship.

$$t= mT_s \tag{2}$$

The digital signal $y_s(mT_s)$ converted from the analog signal y(t) can be expressed as follows:

$$y_s(mT_s) = A_s(mT_s)\cos\{\omega mT_s+\varphi_s(mT_s)\} \tag{3}$$

where $A_s(mT_s)$ is a sampled value of the envelope at time mT_s and $\varphi_s(mT_s)$ is a sampled phase value of the phase φ (t) at time mT_s.

[0025] Normalizing the time in Eq. (3) with the sampling time T_s gives

$$y_s(m) = A_s(m)\cos\{\omega m+\varphi_s(m)\} \tag{4}$$

[0026] Next, the time sequence of digital signals given by Eq. (4) is subjected to an n-point interpolation operation to insert therein samples at n points, thereby interpolating the digitized received signals. The n-point interpolation result

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y_u is given as follows:

$$y_u(k) = y_s(k/n) \tag{5}$$

$$= A_s(k/n)\cos\{\omega(k/n)+\varphi_s(k/n)\} \tag{6}$$

This interpolation value is calculated by the interpolation algorithm described later on. As the result of this, the amount of data of the interpolation result $y_u(k)$ on the time base becomes n times larger than the amount of data of the digital-signal time sequence $y_s(m)$.

[0027] The local oscillation means 45 outputs the local oscillation signal $f_L(k)$ synchronized with an angular velocity ω.

$$f_L(k) = B_L \exp\{j\omega(k/n)\} \tag{7}$$

where B_L is the amplitude of the local oscillation signal $f_L(k)$ and exp(•) is an exponential function, $f_L(k)$ being a complex number. The digital multiplying means 42 multiplies the n-point interpolation result $y_u(k)$ by the local oscillation signal $f_L(k)$.

$$z_u(k) = y_u(k) \cdot f_L(k) \tag{8}$$

[0028] The multiplication result $z_u(k)$ is the output from the multiplying means 42, which is a complex number. The multiplication result $z_u(k)$ is subjected to an n-point decimation operation by n-point decimation means 43 to decimate samples in the time sequence every n points. The decimation result z_d is as follows:

$$z_d(p) = z_u(pn) \tag{9}$$

$$= y_u(pn) \cdot f_L(pn) \tag{10}$$

$$= y_s(pn/n) \cdot f_L(pn) \tag{11}$$

$$= y_s(p) \cdot f_L(pn) \tag{12}$$

The number of samples of the interpolation result z_u on the time base becomes n/1 the number of samples of the multiplication result $z_u(k)$. As long as the n-point interpolation means 41 and the n-point decimation means 43 are used, the $z_d(p)$ sampling interval in the AD converter 32 always equals the sampling time T_s.

[0029] At the start of demodulation processing, the local oscillation signal $f_L(m'T_s)$ from the local oscillation means 45 is synchronized with the received signal, i.e. the input signal $y_s(mT_s)$ to the quadrature demodulation means 33 for accurate synchronous detection processing in order that the operation result by the quadrature demodulation means 33 may be processed as a demodulation result by the filter means 34,. This synchronization processing is carried out following the procedure shown in Fig. 4B, for instance. In the first place, the output which is obtained from each of the n-point interpolation means 41_I and 41_Q when n is set to zero, that is, the uninterpolated digital signal $y_s(mT_s)$, is multiplied by the local oscillation signal $f_L(m'T_s)$ (S1).

$$z_s(m) = y_s(mT_s) f_L(m'T_s) \tag{13}$$

$$z_s(m) = A_s(m)\cos(2\pi f m T_s+\theta) B_L \cos(2\pi f' m' T_s) \tag{14}$$

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$$z_s(m) = (1/2)A_s(m)B_L[\cos(2\pi(fm-f'm')T_s+\theta)$$

$$+\cos(2\pi(fm+f'm')T_s+q\theta)] \quad (15)$$

This zs(m) is subjected to low-pass filtering to extract a difference frequency component $\hat{z}_s(m)$ which is given by the following equation.

$$\hat{z}_s(m) = (1/2)A_s(m)B_L\cos[2\pi(fm-f'm')T_s+\theta] \quad (16)$$

Normalizing the amplitude and the initial phase in Eq. (16) gives

$$z'_s(m) = \cos(fm-f'm') \quad (17)$$

$2\pi f=\omega$ and $2\pi f'=\omega'$. The $z_s'(m)$ by Eq. (17) is called an evaluation function, and the local oscillation frequency f' is so controlled as to maximize the evaluation function $z_s'(m)$. That is, a check is made to see if the evaluation function has become maximum (S3), and if not, the frequency f' of the local oscillation signal $f_L(m'Ts)$ is adjusted so that the evaluation function $z_s'(m)$ becomes maximum, followed by a return to step S1 (S4). When the evaluation function $z_s'(m)$ becomes maximum, the input signals $y_s(mT_s)$ and the local oscillation signal $f_L(m'T_s)$ are subjected to n-point interpolation processing (S5), and the resulting interpolated signals $y_u(k\Delta)$ and $f_L(k'\Delta)$ (where $n\Delta=Ts$) are multiplied (S6). The multiplication result is subjected to low-pass filter processing to obtain the difference frequency component (S7). A check is made to see if an evaluation function $z_s'(k)=\cos(fk-fk')$ similar to that in step S3 is maximum (S8), and if not, it is determined whether the interpolation number n needs to be changed (S9); if not, the k' in the local oscillation signal $f_L(k'\Delta)$ is so adjusted as to maximize the evaluation function $z_s'(k)$, followed by a return to step S6 (S10). A check is made to see whether the interpolation number n needs to be changed, that is, whether the evaluation function $z_s'(k)$ is larger than a threshold value. If the evaluation function $z_s'(k)$ is larger than the threshold value and will hardly change even if the interpolation number n is increased, the interpolation number n is increased by 1 or so, followed by a return to step S5 (S11). When the evaluation value $z_s'(k)$ is maximum, it is decided that the received signal and the local oscillation signal are synchronized with each other, and synchronization control comes to an end.

[0030] When the evaluation function $z_s'(k)$ hardly increases even if the interpolation number n is increased, the interpolation number n of the smaller value is used in the subsequent processing, that is, the evaluation function $z_s'(k)$ is made maximum and the interpolation number n minimum for synchronization with high accuracy and for minimum computational complexity. In the above, since the adjustable minimum value of the local oscillation signal $z_s(k'\Delta)$ in step S10 is k'=1, i.e. the sample interval Δ after interpolation, the accuracy of synchronization of the local oscillation signal $f_L(m'T_s)$ with the input signal $y_s(mT_s)$ increases with an increase in the interpolation number n. Incidentally, low-pass filter means 101 in Fig. 4A is means for carrying out the processing of steps S2 and S7 in Fig. 4B.

[0031] Next, a description will be given of a concrete interpolation processing method for the interpolation means 41_I and 41_Q. As shown in Fig. 5A, the time sequence signal $y_s(m)$ of the sampling period T_s is transformed by fast-Fourier-transform (FFT) processing into a frequency domain signal y(f) for each period Ta, and a zero point is inserted into the signal y(f) on the frequency axis to obtain a signal y'(f), which is transformed by inverse fast-Fourier-transform (IFFT) processing into a time sequence signal $y_u(k)$ which has an increased number of samples per time Ta. This interpolation method by FFT ensures high reliability of signals interpolated when the number of interpolated samples is large. This method is described in, for example, Toshinori Yoshikawa et al., "Numerical Calculation in Engineering," pp. 183, Nihon Rikoh Kai, 1984.

[0032] Another method is shown in Fig. 5B, in which sample values which are determined by a linear function at+b or quadratic function at^2+bt+c are interpolated between adjacent actual sample values of the time sequence signal $y_s(m)$ for each period Ta as indicated by the broken line to obtain the time sequence signal $y_u(k)$ which has an increased number of samples per time Ta. Such a method of interpolating samples estimated by a linear m-order function is simple and easy. With this method, the computational complexity is low and reliability is relatively high when the number of interpolated samples is small.

[0033] It is also possible to use such a method as shown in Fig. 5C, in which Q previous samples of the time sequence signal $y_u(k)$ derived by interpolation from the time sequence signal $y_s(m)$ are used to estimate, by an adaptive algorithm, the samples to be interpolated next and the estimated samples are interpolated into the next time sequence signal $y_s(m)$ to obtain the time sequence signal $y_u(k)$. The adaptive algorithm for the estimation of samples needs only to have been optimized for or with respect to Gaussian noise; a Kalman Filter algorithm, least means squares algorithm, re-

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cursive least square algorithm, Newton method, or steepest descent method can be used. With this method, it is possible to interpolate samples into the time sequence signal while compensating for the degradation of the signal by the transmission line to some extent.

[0034] Next, a concrete example of the decimation processing method by the decimation means 43_I and 43_Q in Fig. 4A will be described. For example, as shown in Fig. 6A, samples of the same number as those interpolated by each of the interpolating means 41_I and 41_Q are simply decimated from the time sequence signal $z_u(k)$ for each period Ta to obtain a time sequence signal $z_d(p)$ which has a decreased number of samples per time Ta. The processing by this method is very simple and easy.

[0035] Alternatively, as shown in Fig. 6B, an evaluation function is used to perform operation processing of a plurality Q (three in Fig. 6B) of samples in the time sequence signal $z_u(k)$ to obtain one sample, thus decimating samples in the time sequence signal $z_u(k)$ to obtain the time sequence signal $z_d(p)$. The evaluation function may be a function for calculating a mean value or centroids of a plurality of samples. With this method, information about the samples to be decimated can be reflected by the evaluation function on the samples left undecimated.

[0036] The digital filter means 34 in Fig. 3 performs a filtering operation and a smoothing operation. As shown in Fig. 7, the in-phase and quadrature component outputs from the quadrature demodulating means 33, that is, the outputs from the n-point decimation means 43_I and 43_Q in Fig. 4A, are smoothed by smoothing means 51_I and 51_Q, respectively, by which the number of samples on the time base is reduced within the range that meets the Nyquist sampling theorem. In other words, a plurality of samples is reduced by the averaging down to one. This enables decimation processing on the time base. Based on the processing results by the smoothing means 51_I and 51_Q, the orders of filter coefficients can be lowered by digital filter means 52_I and 52_Q, respectively. The smoothing of samples is expressed by the following equation.

$$z_{ds}(p_s) = g(...,z_d((k-1)p), z_d(kp),...) \tag{18}$$

where $g(\cdot)$ is a function indicating the smoothing processing, p_s a normalization variable of the output by the smoothing processing and z_{ds} a complex signal which is the output from the smoothing means 51. The smoothing processing averages signals at m points, for example, to reduce the number of samples down to 1/m. The signal $z_{ds}(p_s)$ is band-limited by the filter means 52. This is expressed by the following equation.

$$\hat{z}(p_s) = h(z_{ds}(p_s)) \tag{19}$$

where $h(\cdot)$ is a signal processing function of the filter means 52, $\hat{z}$ the filter processing output signal and $\hat{z}(\cdot)$ a complex number. The quadrature demodulating operation, the smoothing operation and the filtering operation may be carried out as a complex operation for each of the in-phase and the quadrature component as shown in Figs. 4 and 7; alternatively, such a complex operation as indicated by the above equations may directly be conducted.

[0037] A concrete method for the processing by the smoothing means 51 in Fig. 7 will be described. Fig. 8A shows the simplest method according to which N samples are decimated from the time sequence signal $z_d(p)$ from the quadrature demodulating means 33 every N+1 samples to obtain the smoothed time sequence signal $z_{ds}(p_s)$. Smoothing processing by a linearly weighting scheme is shown in Fig. 8B, in which the time sequence signal $z_{ds}(p)$ is fed directly to multiplying means M_0 (Fig. 8C) and, at the same time, it is applied to delay means D_1, ..., D_L, from which signals delayed by sampling periods T_s, $2T_s$, ..., Lt_s of the time sequence signal $z_d(p)$, respectively, are provided to multiplying means M_1, ..., M_L. The inputs into the multiplying means M_0, M_1, ..., M_L are multiplied by weights f_0, f_1, ..., f_L, respectively, then the multiplication results are added together by adder means S_u, and the addition result is output therefrom as the time sequence signal $z_{ds}(p_s)$ smoothed every L+1 samples. That is, the signal $z_{ds}(p)$ is assigned the weights f_0, ..., f_L every L samples, then added together to form one sample of the smoothed signal $z_{ds}(p_s)$.

$$z_{ds}(p_s) = f_0 \cdot z_d(p) + f_1 \cdot z_d(p-1) + ... + f_L \cdot Zd(p-L)$$

When L=3, four samples $z_d(p-s)$ to $z_d(p)$ are linearly weighted and output as one sample $z_{ds}(p_s)$ as shown in Fig. 8C.

[0038] To perform the smoothing processing by the adaptive filtering scheme, the weighting coefficients f_0, ..., f_L are changed by adaptive algorithm processing means 50 through the use of an adaptive algorithm so as to optimize the decision result from the received data decision means as indicated by the broken lines in Fig. 8C. The weighting coefficients are determined first, for example, in a pilot signal (training signal) period in which received data is already known. The adaptive algorithm for use in this case may be a Kalman Filter algorithm or those derived therefrom.

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[0039] Next, a description will be given, with reference to Fig. 9, of a specific operative example of a method for detecting signals of different modulation schemes according to the present invention. A received analog signal shown in Fig. 9A, whose amplitude component is limited to a certain range by the automatic gain controller 31 (Fig. 3), is converted by the AD converter 32 to a digital signal shown in Fig. 9B. The local oscillation means 45, placed under software control, generates local oscillation signals of in-phase and quadrature components depicted in Figs. 9C and D. The digital signal of Fig. 9B and the local oscillation signals of Figs. 9C and D are multiplied by the multiplying means 42I and 42_Q, respectively. As a result, the in-phase and the quadrature component of the output from the quadrature demodulation means 33 become such as depicted in Figs. 9E and 9F. The thus multiplied in-phase and quadrature components are spectrum shaped by the independent digital filter means 34 placed under software control. In consequence, the spectrum-shaped baseband signal has such in-phase and quadrature components as shown in Figs. 9G and 9H. In this way, even if the modulation scheme or mode of the send signal changes from QPSK to 16QAM and BPSK one after another at time intervals as short as 4 milliseconds during transmission, the signal can accurately be reproduced by the digital signal detector of the present invention. This modulated signal is transmitted and received at rates of 2 bits by QPSK, 4 bits by 16QAM and 1 bit by BPSK per symbol. Thus, the digital signal detector of the present invention implements the detection of signals in the variable-bit transmission. In this example, it is preknown that the QPSK, 16QAM and BPSK modulated signals are sequentially received every 4 milliseconds, and the control means 35 switches variables for respective means in synchronization with the received signals.

[0040] To switch the local oscillation frequency in response to the change in the modulation scheme, the control means 35 sends a frequency switching command to the local oscillation means 45 as shown in Fig. 10A. The local oscillation means 45 is implemented basically by software, and for the designated frequency f, an operation $f_{L1}B_L\exp(j2\pi fmT_s)$ is performed. In the case of switching the frequency as shown in Fig. 2A, the control means 35 instructs the local oscillation means 45 to switch the oscillation frequency in order f_1-f_2-f_3-f_4. This instruction is executed in an instruction execution cycle of a microprocessor which executes software in principle. Hence, the local oscillation frequency can be switched fast in as short a time as several nanoseconds. As will be seen from the above, according to the present invention, the frequency of the local oscillation means 45 can be switched faster than in the past and the frequency switching during communication can be fully dealt with, besides the invention is also applicable to fast frequency hopping for dynamic switching of the carrier frequency.

[0041] In response to a change in the symbol transmission rate, too, the present invention similarly changes the characteristic of the filter means 34 through a program of software; the instruction to change the transmission rate is provided by the control means 35. That is, the filter means 34 and the control means 35 implement digital signal processing by software. For example, when the transmission rate varies as shown in Fig. 2C, the symbol transmission rates B1, B2, B3 and B4 are sequentially indicated from the control means 35 to the filter means 34 as depicted in Fig. 10B. Accordingly, the transmission rate is varied in an instruction execution cycle of a microprocessor which executes software in principle. Thus, according to the present invention, the characteristic of the filter means 34 can be changed by the control means 35 at high speed. The characteristic control of the filter means 34 is effected according to the modulation mode of the received signal as well. For example, when the modulation mode changes as shown in Fig. 9G, the roll-off of the filter characteristic is changed to 0.5 for QPSK, 0.3 for 16QAM and 0.5 for BPSK.

[0042] As described above, various processes involved in the present invention are performed by software operations. That is, as shown in Fig. 11, a microprocessor 37 in the control means 35 decodes and executes a program 38 in the control means 35 to control the automatic gain controller 31, the quadrature demodulation means 33 and the digital filter means 34. The automatic gain controller 31 is controlled as follows. The output level of the automatic gain controller 31 is detected by a level detector (not shown), the detected level is converted to a digital value, which is compared with a reference value in the microprocessor 37, and the amplification gain is controlled step by step to bring the output of the automatic gain controller 31 into a predetermined range of amplitude variations. The control of the quadrature demodulation means 33 is effected by controlling the local oscillation means 45, the n-point interpolation means 41 and the n-point decimation means 43. As regards the local oscillation means 45, the frequency f, phase φ and amplitude B_L of the local oscillation signal are designated by the microprocessor 37. For the n-point interpolation means 41 and the n-point decimation means, the sampling frequency $1/T_s$ and the numbers n of interpolation and decimation points are designated. The digital filter means 34 is controlled through the smoothing means 51 and the digital filter means 52. For the smoothing means 51, the sampling frequency $1/T_s$, the number of smoothing points and the smoothing method are designated. For the digital filter means 52, the sampling frequency $1/T_s$, the filter coefficient and the number of symbols necessary for filtering are designated. That is, once the carrier frequency of the input modulated signal of the AD converter 32 is set and input, the minimum value of its sampling frequency $1/T_s$ is automatically determined in accordance with the input carrier frequency. For example, when the carrier frequency of the input modulated signal is 130 MHz, the minimum value of the sampling frequency of the AD converter 32 is set at 260 MHz. For accurate synchronization with the carrier of the input modulated signal, the local oscillation signal needs to be a digital signal of a sampling frequency at least four times higher than the carrier frequency of the input modulated signal; therefore, the numbers n of interpolation points and decimation points are automatically determined. Where the

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conversion rate of the AD converter 32 is high, it is also possible to sample the input modulated signal above the minimum sampling frequency to reduce the number n of samples to be interpolated and decimated correspondingly.

[0043] When the frequency of the demodulated baseband signal is, for example, 20 KHz, the sampling frequency necessary for this signal processing may be 40 RHz; since the quadrature demodulation means 33 outputs an unnecessarily large number of signals, these signals are effectively used to perform processing by the smoothing means 51 to produce a base band signal as faithful to them as possible and decrease its sampling frequency. The number of smoothing points in this case is automatically determined by the set carrier frequency of the input modulated signal and the set symbol transmission rate. As described previously with reference to Figs. 2D and 10B, an appropriate filter characteristic is needed in accordance with the symbol transmission rate, and hence the filter coefficient and the number of symbols necessary for filtering are automatically determined by the set symbol transmission rate. Further, the filter coefficient is automatically determined, depending on the set modulation mode as mentioned previously. Thus, programs are prepared so that various parameters (variables) for the filter means 34, the local oscillation means 45, the interpolation means 41 and the decimation means 43 are automatically designated in accordance with the carrier frequency, the symbol transmission rate and the modulation mode which are set on the basis of the above-mentioned relations.

[0044] In the present invention, it is possible to employ what is called distributed processing system in which microprocessor are provided for the quadrature demodulation means 33 and the digital filter means 34, these microprocessors supplied with the above-mentioned various parameters (variables) designated by the microprocessor 37 and use them as arguments to execute programs for interpolation, quadrature demodulation and decimation and programs for smoothing and filter processing, respectively. Of course, such distributed processing system may be substituted with a centralized processing system in which the microprocessor 37 itself designates first the parameters for the respective means and executes the interpolation, quadrature demodulation, decimation, smoothing and filtering programs on a time-sharing basis, thereby performing virtually parallel processing.

[0045] Fig. 12 is a flowchart showing the procedure of the digital detector. The procedure begins with making a check to see if a request is made for a variable change (S1). Such a variable change request is made when a change in the carrier frequency or symbol transmission rate is newly set and input via set/input means 36, or when the time of changing the modulation mode arrives which is preknown as described previously with reference to Fig. 9, or when switching between the 800 Mhz and 1500 MHz or between audio and still picture information is input via the set/input means as referred to previously in the section "BACKGROUND OF THE INVENTION." Fig. 14 is explanatory of the case where the received signal is a 3-channel time division multiplex signal. The frame for each channel is composed of a preamble 71 and data 72 as shown in Fig. 14B. The preamble 71 is composed of a synchronization word 73 and a base station number 74 together with modulation system information 75 such as the modulation scheme of the data used in the data frame 72 and the symbol transmission rate as shown in Fig. 14C. For example, in the case where the modulation scheme of the data in the data frame 72 is newly designated, the variable change request is considered to be made when the data indicating the modulation scheme is demodulated.

[0046] When such a variable change request is made, the variables to be changed and their values are determined to comply with the request (52). For example, when the request is made for changing the variables for quadrature demodulation, the newly determined variables such as the number n of interpolation points, the local carrier frequency and its amplitude and phase are set as arguments in the processor which executes the quadrature demodulation program (S3). This is followed by the execution of the digital detection program (S4).

[0047] Fig. 13 shows the procedure for digital detection. In the first place, the received signal is subjected to automatic gain control by the automatic gain controller 31 in Fig. 11 so that the level of the received signal falls within a predetermined range (S1). The thus gain-controlled received signal is converted by the AD converter 32 to a digital signal (S2), which is subjected to an n-point interpolation (S3), and the thus interpolated digital signal is subjected to the quadrature demodulation operation (S4). The demodulation result is subjected to n-point decimation processing (S5) and then smoothing processing (S6), and the smoothing result is subjected to low-pass filter processing (S7). This is followed by a signal point decision to decide which signal point on the IQ plane corresponds to the result of the low-pass filter processing (S8).

[0048] As depicted in Fig. 15, the digital detector 53 of the present invention built in a radio, a radio channel controller 54 and an audio encoding/decoding processor 55 may be placed under the time sharing control of the microprocessor 37. Control programs 38, 56 and 57 are prepared which are exclusive to the digital detector 53, the radio channel controller 54 and the audio encoding/decoding processor 55, respectively. The microprocessor 37 switches each of the digital detector 53, the radio channel controller 54, the audio encoding/decoding processor 55 and its control program at proper time intervals on a time sharing basis. Accordingly, a plurality of objects of control can be processed by the single microprocessor 37. Incidentally, this radio is a mobile station of a mobile communication system, for instance, and the radio channel controller 54 performs switching between control and communication channels.

[0049] Fig. 16 illustrates a digital radio communication transceiver which has the digital detector of the present invention built-in, the parts corresponding to those in Fig. 3 being identified by the same reference numerals. The received

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modulated signal from an antenna 60 is amplified by a low-noise amplifier 61, then converted by frequency converting means 62 to an intermediate-frequency (IF) signal, which is band limited by a filter 63, thereafter being fed to the automatic gain controller 31. That is, the received signal is applied to the digital detector of the present invention, shown in Fig. 3, and the detected output, i.e. the output from the filter means 34 is applied to the radio channel controller 54, from which it is fed to an exchange of a network (not shown), for instance. A signal from the exchange is fed via the radio channel controller 54 to filter means 64, wherein it is band limited. The band-limited signal is applied to quadrature modulating means 65, wherein its IF carrier is quadrature-modulated. The modulated output, i.e. the modulated signal is converted by a DA converter 66 to an analog signal, which is further converted by a frequency converter 67 to a high-frequency signal. The high-frequency modulated signal is power amplified by a transmitting power amplifier 68 for transmission from an antenna 69.

[0050] Next, concrete examples of the present invention will be described.

(i) Mobile Multimedia:

[0051] Here, the control operation of the present invention will be described with respect to the cases where the mode setting is (1) manually changed by the user of a mobile station, (2) automatically changed by a command from a base station, and (3) automatically changed according to an autonomous decision by the mobile station. Now, let it be assumed that the audio service is of a conventional PDC (Personal Digital Cellular) system whereas multimedia service (service of receiving broadcast still pictures, for instance) is of a multilevel modulation system (160QAM, for instance). The transmission bandwidth is supposed not to change with the services. Further, assume that the service is switched from a speech to a still picture mode and that the media service is being broadcast in a predetermined frequency band.

[0052] (1) When switching the reception of the audio service to the media service such as still picture, the user of the mobile station changes the service mode of the mobile station. This change is made by a dial key or mode switch provided in the set/input means 36 (Fig. 11). When supplied with a request signal for mode switching from the audio to the media service mode, for instance, the control means 35 of the mobile station changes the process variables of a synthesizer (not shown) for channel selection, the gain controller 31, the quadrature demodulation means 33 and the filter means 34. In the synthesizer, its frequency is set in a predetermined frequency band. In the gain controller 31, the setting of the maximum amplitude of its input signal is changed. That is, since the modulation mode is switched from QPSK to QAM, the maximum set value of the input signal is made larger than in that for QPSK. For the quadrature demodulation means 33 the setting of the numbers n of interpolation points and decimation points is changed. The value n is made larger than that for QPSK. The process variable of the filter means 34 that are changed are the smoothing method, the filter coefficient and the filter order. In this instance, a plurality of smoothing methods optimum for the modulation schemes used are prepared and algorithms of these optimum smoothing methods are prestored in a ROM. Based on the service mode switching signal applied thereto, the control means 35 reads out of the ROM the smoothing method optimum for the specified mode and performs smoothing processing accordingly. The roll-off rate of the filter means 52 (Fig. 7) is made lower than in the case of QPSK and, at the same time, its coefficient and order are also changed.

[0053] With a view to changing various process variables according to the mode being set, control means 35 includes process variable storage part 102 and a smoothing method storage part 103 as shown in Fig. 11. In the process variable storage part 102, for example, as shown in Fig. 17A, there are stored for each of the audio and the picture mode, the maximum amplitude value of the automatic gain controller, the number n of interpolation points, the number of the ROM having stored therein an algorithm for smoothing processing, the roll-off rate and filter coefficient of the filter means. In accordance with the mode set and input, the control means 35 reads out these variables and uses them for respective particular purposes. In the smoothing method storage part 103 there are stored the numbers of the ROMS which have stored therein algorithms or procedures necessary for the execution of various smoothing processes. In order to receive services other than the audio and picture or visual services, process variables for such service modes may be stored in the process variable storage part 102.

[0054] (2) The user of the mobile station changes the service mode setting of the mobile station by the set/input means 36 as in the case (1). Upon receipt of the service mode change request, the control means 35 of the mobile station transmits it, together with a flag indicating the mode change, over a transmission channel for communication with the base station. To set a flag is to make a predetermined bit 0 or 1 on the transmission frame a 1 or 0. When receiving the service change request flag from the mobile station (a request for media service in this example), the base station sends transmission information on the media service via a down-link channel to the mobile station. The mobile station detects the transmission information from the base station by the radio channel controller 54 (Fig. 16). In the thus detected transmission information there are contained the modulation scheme and the transmission rate to be used in the data frame of the radio channel, the time slot in the TDMA frame to be used, and so forth. The mobile station and the base station exchanges signals over the radio channel several times concerning the new service mode,

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as required. The detected transmission information is input as a variable change request signal into the control means 35. The control means 35 changes the variables for the synthesizer, the gain controller, the quadrature demodulation means and the filter means. The contents to be changes are the same as those in the case (1).

[0055] In this instance, the process variable storage part 102 is designed so that the maximum amplitude value, the interpolation point number n and the ROM number of the smoothing method are read out in accordance with the modulation mode specified by the base station as shown in Fig. 17B and the roll-off rate and the filter coefficient are read out in accordance with the symbol transmission rate specified by the base station as shown in Fig. 17C.

[0056] (3) The user of the mobile station changes the setting of the service mode of the mobile station as in the case (1). In this case, several combinations of modulation schemes and symbol transmission rates are predetermined for each of the audio and media services and are assigned different mode numbers, and the respective process variables are stored in the process number storage part 102 in correspondence with the mode numbers as shown in Fig. 17A. The relationships of the mode numbers to the modulation schemes and the symbol transmission rates are also held in the base station. When a service mode change is set and input, the control means 35 transmits a code indicating the number of the set mode to the base station over the transmission channel for communication therewith. Further, the control means 35 reads out of the storage part 102 the process variables corresponding to the set and input mode and uses the read-out process variables to perform detection processing.

[0057] The base station receives and responds to the mode number indicating the newly set service mode to change the setting of the modulation scheme, the transmission rate and the time slot of the TDMA frame which are used in the radio channel for the transmission of information to the mobile station. As required, the mobile station and the base station exchange signals over the radio channel several times concerning the service mode to be newly changed.

(ii) Compatible Mobile Station

[0058] Here, the control operation of the present invention will be described with respect to the cases where the mode setting is (1) manually changed by the user of a mobile station, (2) automatically changed by a command from a base station, and (3) automatically changed according to an autonomous decision by the mobile station. Assume that the mobile station has gone indoors (a closed space like an underground shopping center). Suppose that the mobile station receives the PDC audio service outdoors and 16QAM media service indoors and that the transmission band remains unchanged.

(1) The user changes the communication mode setting of the mobile station when he goes indoors. This is done using a dial key or dedicated mode change switch of the set/input means 36. Upon receipt of a communication mode change request, the control means 35 changes the setting of the oscillation frequency of the synthesizer. For example, when the 800 MHz band is used outdoors and 1500 MHz band indoors, the local oscillation frequency to be supplied to the frequency converter for conversion to an IF signal is changed for use in the 1500 MHz band. Since the modulation scheme is switched from QPSK to 16QAM as is the case with the mobile multimedia (i), the control means 35 makes the maximum amplitude value of the gain controller large, sets the number n of interpolation and decimation points in the quadrature demodulation to a value larger than in the case of QPSK, uses a ROM having stored the optimum smoothing method, makes the roll-off rates of the filter means 64 at the sending side (Fig. 16) and the filter means 34 at the receiving side (Fig. 16) small, and changes their filter coefficients.

(2) The user of the mobile station changes the communication mode setting of the mobile station by the set/input means 36 when he goes indoors. The mobile station flags a communication mode change signal on the transmission frame of the radio channel to the base station. The base station receives the service change request flag from the mobile station and supplies it with transmission information about the communication mode over the downlink channel. The mobile station detects the transmission information from the base station by the radio channel controller 54. In the detected transmission information there are contained the carrier frequency, the modulation scheme, the transmission rate and the time slot of the TDMA frame which are used in the radio channel. Based on the transmission information, the mobile station changes the process variables which are used in the synthesizer, the quadrature modulation means, the gain controller, quadrature demodulation means and the filter means. The contents of the changes are the same as in the case (1).

(3) As in the cases (1) and (2), the user of the mobile station changes the setting of the communication mode of the mobile station when he goes indoors. In this instance, there are predetermined a plurality of modes corresponding to several combinations of modulation schemes and symbol transmission rates, and the mobile station informs the base station of changing the communication mode setting through the radio channel. The base station responds to the signal from the mobile station to set a predetermined communication mode. At this time, the settings are the carrier frequency, modulation scheme, transmission rate and the time slot of the TDMA frame which are used in the radio channel. The base station and the mobile station exchange signals several times over the radio channel and then communicate with each other in the newly set communication mode. Based on the

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newly set communication mode, the mobile station reads the process variable storage part 102 and changes the variables which are used in the synthesizer, the quadrature demodulation means, the gain controller,the quadrature demodulation means and the filter means. The contents of these changes are the same as in the cases (1) and (2).

[0059] In the above, the variables to be used in the gain controller 31, the quadrature demodulation means 33 and the digital filter means 34 are all changed according to every mode switching. This is a preferred example. For example, when the modulation scheme is changed to QAM, at least the maximum amplitude value of the gain controller 31 is changed to ensure accurate detection of the amplitude value of the received signal and the other variables need not be changed. In the case of switching to the QPSK modulation scheme, the change of the maximum value of the gain controller 31 need not be given priority because the amplitude information is not used. The change of the roll-off rate in the filter means 34 and the corresponding changes of the filter coefficient and filter order are relatively important. Next in the order of importance comes the number of interpolation points, followed by the choice of the smoothing method. The necessity of changing the variables decreases in descending order of their importance.

[0060] While in the above the present invention has been described as being applied to the reception of radio signals, the invention is also applicable to the reception of signals in a wired communication system in which the modulation scheme and the symbol transmission rate are switched to those optimum for each information. In such an instance, the automatic gain controller 31 can be dispensed with.

[0061] As will be appreciated from the above, the present invention is advantageous over the prior art as listed below.

(i) A plurality of modulation schemes can be dealt with;
(ii) A plurality of local oscillation frequencies can be dealt with:
(iii) A plurality of symbol transmission rates can be dealt with;
(iv) Variable bit transmission and variable symbol rate transmission can be implemented with one receiver;
(v) A completely quadrature demodulated wave can be generated; and
(vi) The invention is applicable to fast frequency hopping.

Claims

1. A method of digitally detecting a signal, comprising:

an AD conversion step of converting a received modulated analog signal to a digital signal;
a quadrature demodulation step of performing a digital quadrature-demodulating operation on said digital signal using a local oscillation frequency of a local oscillation signal as a process variable;
a filtering step of performing a digital low-pass filtering operation on said quadrature-demodulated digital signal using filter characteristics as process variables; and
a control step of changing, in response to a process variable change request, at least one process variable in at least one of said quadrature demodulation step, for changing the local oscillation frequency in accordance with a carrier frequency, and said filtering step, for changing the filter characteristics according to the modulation scheme and transmission rate of the modulated signal;

characterized by

an interpolation step of performing n-point interpolation processing on said digital signal resulting from said AD conversion step to interpolate therein samples at n points to produce an n-point interpolated digital signal to be quadrature-demodulated in said quadrature demodulation step, said n being a real number equal to or greater than 1;
a multiplication step of complex-multiplying the n-point interpolated digital signal by said local oscillation signal; and
a decimation step of performing n-point decimation processing on a digital signal resulting from the complex-multiplication to decimate therefrom samples at n points.

2. The method of claim 1, wherein said filtering step comprises:

a smoothing step of performing smoothing processing on the result of said quadrature demodulation to reduce the number of samples on the time base; and
a digital filter step of performing band-limiting operation on the result of said smoothing processing using said filter characteristics.

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3. The method of claim 1, wherein said interpolation step is a step of performing discrete Fourier transform processing on said digital signal and performing inverse discrete Fourier transform on the result of said Fourier transform processing after adding thereto a zero coefficient to obtain said result of said interpolation processing.

4. The method of claim 1, wherein said interpolation step is a step of performing a linear interpolation which approximates an m-th order function to said digital signal and interpolates therein samples which fit said m-th order function.

5. The method of claim 1, wherein said interpolation step is a step of interpolating samples estimated by an adaptive algorithm used for those preceding them in said digital signal every predetermined number of samples.

6. The method of claim 1, wherein said decimation step is a step of decimating from said multiplication result said samples interpolated at said n points in said interpolation step.

7. The method of claim 1, wherein said decimation step is a step of calculating a mean value or centroid of a plurality of samples in a sequence of samples of said multiplication result to obtain one sample.

8. The method of claim 1, further comprising a step of synchronizing said local oscillation signal with said digital signal.

9. The method of claim 8, wherein said synchronizing step comprises the steps of:

synchronizing the local oscillation frequency of said local oscillation signal with said digital signal; and
time-synchronizing said frequency-synchronized local oscillation signal with said n-point interpolated digital signal.

10. The method of claim 1, wherein said at least one process variable in said quadrature demodulation step is the number n of interpolation points.

11. The method of claim 1, wherein said at least one process variable in said quadrature demodulation step is the local oscillation frequency of said local oscillation signal.

12. The method of claim 21, wherein said at least one process variable in said filter step is the number of smoothing points used to reduce said number of samples.

13. The method of claim 2, wherein said at least one process variable in said filter step is a filter characteristic in said digital filter step.

14. The method of any one of claims 2 and 8 to 13, further comprising a gain control step of controlling the maximum amplitude of said received modulated signal to be a set value which is said at least one process variable.

15. The method of claim 14, further comprising:

a process variable change request detecting step of detecting a process variable change request;
a process variable determining step of responding to said process variable change request to determine which process variable is to be changed and its value; and
a step of changing said process variable to said determined variable.

16. The method of claim 15, wherein each of said steps is executed by decoding and executing a program.

17. The method of claim 16, wherein said process variable determining step is a step of reading out a prestored process variable in response to said variable change request.

18. The method of claim 17, wherein said variable change request is input by manipulating set/input means.

19. The method of claim 17, wherein said process variable change request detecting step is a step of detecting said process variable change request from a received signal.

20. A digital signal detector comprising:

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an AD converter (32) for converting a received modulated analog signal to a digital signal;
quadrature demodulation means (33) for performing a digital quadrature demodulating operation on said digital signal using a digital local oscillation signal of a local oscillation frequency as a process variable;
filter means (34) for performing a digital low-pass filter operation on the quadrature demodulated digital signal using filter characteristics as process variables;
input means (36) for inputting a process variable change request for changing a process variable; and
control means (35) responsive to said process variable change request to change at least one process variable in at least one of said quadrature demodulation means, for changing the local oscillation frequency in accordance with a carrier frequency, and said filter means (34) for changing the filter characteristics according to the modulation scheme and transmission rate;

characterized by

interpolating means (41I, 41Q) for performing n-point interpolation processing on said digital signal from said AD converter (32) to interpolate therein samples at n points to produce an n-point interpolated digital signal to be quadrature-demodulated by said quadrature demodulation means (33), said n being a real number equal to or greater than 1;
local oscillation means (45) for generating said digital local oscillation signal through digital operation;
multiplying means (42) for complex-multiplying the n-point interpolated digital signal by said digital local oscillation signal; and
decimating means (43I, 43Q) for performing n-point decimation processing on a digital signal resulting from said complex-multiplication to decimate therefrom samples at said n points.

21. The detector of claim 20, wherein said filter means (34) comprises:

smoothing means (51) for smoothing the output from said quadrature demodulation means (33) and for performing an operation for reducing the number of samples of said output; and
digital filter means (52) for performing a band-limiting operation on the result of said operation by said smoothing means (51) using said filter characteristics.

22. The detector of claim 21, further comprising an automatic gain controller (31) provided at a stage preceding said AD converter (32), for controlling the gain of said received modulated signal so that its maximum amplitude becomes a set value which is one of said process variables that can be changed by said control means (35).

23. The detector of claim 22, further comprising a storage part (102) having prestored therein a comparative table of variable change requests and process variables, and wherein said control means (35) is means responsive to said process variable change request to read out said storage part and to change the process variable corresponding to said read-out one.

24. The detector of claim 23, wherein said input means (36) is set/input means for inputting said process variable change request by a manual operation.

25. The detector of claim 23, wherein said input means is means (36) for detecting said process variable change request from a received signal.

26. The detector of any one of claims 20 to 25, wherein said control means (35) comprises a program and a microprocessor for decoding and executing said program.

27. The detector of claim 26, wherein said control means (35) serves also as control means of a digital radio transceiver.

Patentansprüche

1. Verfahren zum digitalen Erfassen eines Signals, das Folgendes umfasst:

einen AD-Wandlungsschritt des Wandelns eines empfangenen modulierten Analogsignals in ein Digitalsignal;
einen Quadratur-Demodulationsschritt des Ausführens einer digitalen Quadratur-Demodulationsoperation an dem Digitalsignal unter Verwendung eines lokalen Oszillationssignals einer lokalen Oszillationsfrequenz als

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einer Prozessvariablen;
einen Filterschritt des Ausführens einer digitalen Tiefpass-Filteroperation an dem quadratur-demodulierten Digitalsignal unter Verwendung von Filtercharakteristika als Prozessvariablen; und
einen Steuerschritt des Änderns, als Antwort auf eine Prozessvariablenänderungsanfrage, wenigstens einer Prozessvariablen in dem Quadratur-Demodulationsschritt, um die lokale Oszillationsfrequenz in Übereinstimmung mit einer Trägerfrequenz zu ändern, und/oder dem Filterschritt, um die Filtercharakteristika in Übereinstimmung mit dem Modulationsschema und der Übertragungsrate des modulierten Signals zu ändern;

gekennzeichnet durch

einen Interpolationsschritt des Ausführens einer n-Punkt Interpolationsverarbeitung an dem Digitalsignal, das aus dem AD-Wandlungsschritt resultiert, um darin Abtastwerte an n Punkten zu interpolieren, um ein n-Punkt-interpoliertes Digitalsignal zu erzeugen, das in dem Quadratur-Demodulationsschritt quadraturdemoduliert wird, wobei n eine reelle Zahl ist, die gleich oder größer ist als 1;
einen Multiplikationsschritt des komplexen Multiplizierens des n-Punkt-interpolierten Digitalsignals mit dem lokalen Oszillationssignal; und
einen Dezimierungsschritt des Ausführens einer n-Punkt Dezimierungsverarbeitung an einem Digitalsignal, das aus der komplexen Multiplikation resultiert, um daraus Abtastwerte an n Punkten zu dezimieren.

2. Verfahren nach Anspruch 1, bei dem der Filterschritt folgendes umfasst:

einen Glättungsschritt des Ausführens einer Glättungsverarbeitung an dem Ergebnis der Quadraturdemodulation, um die Anzahl der Abtastwerte auf der Zeitachse zu reduzieren; und
einen digitalen Filterschritt des Ausführens einer bandbegrenzenden Operation an dem Ergebnis der Glättungsverarbeitung unter Verwendung der Filtercharakteristika.

3. Verfahren nach Anspruch 1, bei dem der Interpolationsschritt ein Schritt des Ausführens einer diskreten Fouriertransformationsverarbeitung an dem Digitalsignal und einer inversen diskreten Fouriertransformation an dem Ergebnis der Fouriertransformationsverarbeitung nach Hinzuaddieren eines Nullkoeffizienten ist, um das Ergebnis der Interpolationsverarbeitung zu erhalten.

4. Verfahren nach Anspruch 1, bei dem der Interpolationsschritt ein Schritt des Ausführens einer linearen Interpolation ist, welche eine Funktion m-ter Ordnung an das Digitalsignal annähert und darin Abtastwerte interpoliert, welche zu der Funktion m-ter Ordnung passen.

5. Verfahren nach Anspruch 1, bei dem der Interpolationsschritt ein Schritt des Interpolierens von Abtastwerten, die von einem adaptiven Algorithmus geschätzt werden, der auf die ihnen in dem Digitalsignal vorangegangenen angewendet wird, nach jeder vorbestimmten Zahl von Abtastwerten ist.

6. Verfahren nach Anspruch 1, bei dem der Dezimierungsschritt ein Schritt des Dezimierens der in dem Interpolationsschritt an den n Punkten interpolierten Abtastwerte von dem Multiplikationsergebnis ist.

7. Verfahren nach Anspruch 1, bei dem der Dezimierungsschritt ein Schritt des Berechnens eines Mittelwertes oder Schwerpunktes einer Mehrzahl von Abtastwerten in einer Folge von Abtastwerten des Multiplikationsergebnisses zum Erhalten eines Abtastwerts ist.

8. Verfahren nach Anspruch 1, das weiter einen Schritt des Synchronisierens des lokalen Oszillationssignals mit dem Digitalsignal enthält.

9. Verfahren nach Anspruch 8, bei dem der Synchronisationsschritt die folgenden Schritte umfasst:

Synchronisieren der lokalen Oszillationsfrequenz des lokalen Oszillationssignals mit dem Digitalsignal; und
Zeitsynchronisieren des frequenzsynchronisierten lokalen Oszillationssignals mit dem n-Punkt-interpolierten Digitalsignal.

10. Verfahren nach Anspruch 1, bei dem wenigstens eine Prozessvariable in dem Quadratur-Demodulationsschritt die Anzahl n der Interpolationspunkte ist.

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11. Verfahren nach Anspruch 1, bei dem wenigstens eine Prozessvariable in dem Quadratur-Demodulationsschritt die lokale Oszillationsfrequenz des lokalen Oszillationssignals ist.

12. Verfahren nach Anspruch 21, bei dem wenigstens eine Prozessvariable in dem Filterschritt die Anzahl der Glättungspunkte ist, an denen die Anzahl der Abtastwerte reduziert werden soll.

13. Verfahren nach Anspruch 2, bei dem wenigstens eine Prozessvariable in dem Filterschritt eine Filtercharakteristik in dem digitalen Filterschritt ist.

14. Verfahren nach einem der Ansprüche 2 und 8 bis 13, das weiter einen Verstärkungssteuerungsschritt des Steuerns der maximalen Amplitude des empfangenen modulierten Signals auf einen Sollwert umfasst, der die wenigstens eine Prozessvariable ist.

15. Verfahren nach Anspruch 14, das weiter umfasst:

einen Prozessvariablenänderungsanfrage-Erfassungsschritt des Erfassens einer Prozessvariablenänderungsanfrage;
einen Prozessvariablenbestimmungsschritt des Antwortens auf die Prozessvariablenänderungsanfrage, um die zu ändernde Prozessvariable und deren Wert zu bestimmen; und
einen Schritt des Änderns der Prozessvariablen zu der bestimmten Variable.

16. Verfahren nach Anspruch 15, bei dem jeder der Schritte durch Dekodieren und Ausführen eines Programms ausgeführt wird.

17. Verfahren nach Anspruch 16, bei dem der Prozessvariablenbestimmungsschritt ein Schritt des Auslesens einer vorab gespeicherten Prozessvariablen als Antwort auf die Variablenänderungsanfrage ist.

18. Verfahren nach Anspruch 17, bei dem die Variablenänderungsanfrage durch Handhaben eines Setz-/Eingabemittels eingegeben wird.

19. Verfahren nach Anspruch 17, bei dem der Prozessvariablenänderungsanfrage-Erfassungsschritt ein Schritt zum Erfassen der Prozessvariablenänderungsanfrage von einem empfangenen Signal ist.

20. Digitaler Signaldetektor, der Folgendes umfasst:

einen AD-Wandler (32) zum Wandeln eines empfangenen modulierten Analogsignals in ein Digitalsignal;
ein Quadratur-Demodulationsmittel (33) zum Ausführen einer digitalen Quadratur-Demodulationsoperation an dem Digitalsignal unter Verwendung eines digitalen lokalen Oszillationssignals mit einer lokalen Oszillationsfrequenz als einer Prozessvariablen;
ein Filtermittel (34) zum Ausführen einer digitalen Tiefpass-Fitteroperation an dem quadratur-demodulierten Digitalsignal unter Verwendung von Filtercharakteristika als Prozessvariablen;
ein Eingabemittel (36) zum Eingeben einer Prozessvariablenänderungsanfrage zum Ändern einer Prozessvariablen; und
Steuermittel (35), die auf die Prozessvariablenänderungsanfrage zum Ändern wenigstens einer Prozessvariablen in dem Quadratur-Demodulationsmittel, um die lokale Oszillationsfrequenz in Übereinstimmung mit einer Trägerfrequenz zu ändern, und/oder dem Filtermittel (34), um die Filtercharakteristika in Übereinstimmung mit dem Modulationsschema und der Übertragungsrate zu ändern, ansprechen;

gekennzeichnet durch

ein Interpolationsmittel (411, 41Q) zum Ausführen einer n-Punkt-Interpolationsverarbeitung an dem Digitalsignal von dem AD-Wandler (32), um darin Abtastwerte an n Punkten zu interpolieren, um ein n-Punkt-interpoliertes Digitalsignal für die Quadratur-Demodulation **durch** das Quadratur-Demodulationsmittel (33) zu erzeugen, wobei n eine reelle Zahl ist, die gleich oder größer ist als 1;
ein lokales Oszillationsmittel (45) zum Erzeugen des digitalen lokalen Oszillationssignals **durch** digitale Operation;
ein Multiplikationsmittel (42) zur komplexen Multiplikation des n-Punkt-interpolierten Digitalsignals mit dem digitalen lokalen Oszillationssignal; und

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ein Dezimierungsmittel (431, 43Q) zum Ausführen einer n-Punkt-Dezimierungsverarbeitung an dem Digitalsignal, das aus der komplexen Multiplikation resultiert, um daraus Abtastwerte an den n Punkten zu dezimieren.

21. Detektor nach Anspruch 20, wobei das Filtermittel (34) folgendes umfasst:

ein Glättungsmittel (51) zum Glätten der Ausgabe von dem Quadratur-Demodulationsmittel (33) und zum Ausführen einer Operation zum Reduzieren der Anzahl der Abtastwerte der Ausgabe; und
ein digitales Filtermittel (52) zum Ausführen einer bandbegrenzenden Operation an dem Ergebnis der Operation des Glättungsmittels (51) unter Verwendung der Filtercharakteristika.

22. Detektor nach Anspruch 21, der ferner einen automatischen Verstärkungsregler (31) umfasst, der in einer dem AD-Wandler (32) vorangehenden Stufe vorgesehen ist, zum Regeln der Verstärkung des empfangenen modulierten Signals, so dass dessen maximale Amplitude zu einem Sollwert wird, der eine der Prozessvariablen ist, die durch das Steuermittel (35) geändert werden kann.

23. Detektor nach Anspruch 22, der ferner ein Speicherteil (102) umfasst, in dem eine Vergleichstabelle von Variablenänderungsanfragen und Prozessvariablen vorab gespeichert ist, und bei dem das Steuermittel (35) ein Mittel ist, das auf die Prozessvariablenänderungsanfrage anspricht, um aus dem Speicherteil auszulesen, und um die Prozessvariable entsprechend der ausgelesenen zu ändern.

24. Detektor nach Anspruch 23, bei dem das Eingabemittel (36) ein Setz-/Eingabemittel zum Eingeben der Prozessvariablenänderungsanfrage durch eine manuelle Operation ist.

25. Detektor nach Anspruch 23, bei dem das Eingabemittel ein Mittel (36) zum Erfassen der Prozessvariablenänderungsanfrage von einem empfangenen Signal ist.

26. Detektor nach einem der Ansprüche 20 bis 25, bei dem das Steuermittel (35) ein Programm und einen Mikroprozessor zum Entschlüsseln und Ausführen dieses Programms umfasst.

27. Detektor nach Anspruch 26, bei dem das Steuermittel (35) auch als Steuermittel eines digitalen Funk-Sender-Empfängers dient.

Revendications

1. Procédé pour détecter un signal de façon numérique, comprenant :

une étape de conversion A/N consistant à convertir en un signal numérique un signal analogique modulé reçu;
une étape de démodulation en quadrature consistant à effectuer une opération de démodulation en quadrature numérique sur le signal numérique en utilisant une fréquence d'oscillation locale d'un signal d'oscillation locale en tant que variable de processus;
une étape de filtrage consistant à effectuer une opération de filtrage passe-bas numérique sur le signal numérique démodulé en quadrature, en utilisant des caractéristiques de filtre en tant que variables de processus; et
une étape de commande consistant à changer, en réponse à une demande de changement de variable de processus, au moins une variable de processus dans l'une au moins de l'étape de démodulation en quadrature, pour changer la fréquence d'oscillation locale conformément à une fréquence porteuse, et de l'étape de filtrage, pour changer les caractéristiques de filtre conformément à la technique de modulation et au débit de transmission du signal modulé;

caractérisé par

une étape d'interpolation consistant à effectuer un traitement d'interpolation à n points sur le signal numérique résultant de l'étape de conversion A-N, pour interpoler dans celui-ci des échantillons à n points, pour produire un signal numérique interpolé à n points devant être démodulé en quadrature dans l'étape de démodulation en quadrature, n étant un nombre réel égal ou supérieur à 1;
une étape de multiplication consistant à effectuer une multiplication complexe du signal numérique interpolé

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à n points par le signal d'oscillation locale; et
une étape de décimation consistant à effectuer un traitement de décimation à n points sur un signal numérique résultant de la multiplication complexe, pour décimer à partir de celui-ci des échantillons à n points.

2. Procédé selon la revendication 1, dans lequel l'étape de filtrage comprend :

une étape de lissage consistant à effectuer un traitement de lissage sur le résultat de la démodulation en quadrature pour réduire le nombre d'échantillons sur la base de temps; et
une étape de filtrage numérique consistant à effectuer une opération de limitation de bande sur le résultat du traitement de lissage, en utilisant les caractéristiques de filtre.

3. Procédé selon la revendication 1, dans lequel l'étape d'interpolation est une étape consistant à effectuer un traitement de transformation de Fourier discrète sur le signal numérique et à effectuer une transformation de Fourier discrète inverse sur le résultat du traitement de transformation de Fourier, après lui avoir ajouté un coefficient zéro pour obtenir le résultat du traitement d'interpolation.

4. Procédé selon la revendication 1, dans lequel l'étape d'interpolation est une étape consistant à effectuer une interpolation linéaire qui forme une approximation du signal numérique avec une fonction du m-ième ordre, et interpole dans celui-ci des échantillons qui sont ajustés à la fonction du m-ième ordre.

5. Procédé selon la revendication 1, dans lequel l'étape d'interpolation est une étape consistant à interpoler des échantillons estimés par un algorithme adaptatif utilisé pour ceux qui les précèdent dans le signal numérique, à chaque nombre prédéterminé d'échantillons.

6. Procédé selon la revendication 1, dans lequel l'étape de décimation est une étape consistant à décimer à partir du résultat de multiplication les échantillons interpolés auxdits n points dans l'étape d'interpolation.

7. Procédé selon la revendication 1, dans lequel l'étape de décimation est une étape consistant à calculer une valeur moyenne ou un centroïde d'une multiplicité d'échantillons dans une séquence d'échantillons du résultat de multiplication, pour obtenir un échantillon.

8. Procédé selon la revendication 1, comprenant en outre une étape consistant à synchroniser le signal d'oscillation locale avec le signal numérique.

9. Procédé selon la revendication 8, dans lequel l'étape de synchronisation comprend les étapes suivantes :

on synchronise la fréquence d'oscillation du signal d'oscillation locale avec le signal numérique; et
on effectue une synchronisation temporelle du signal d'oscillation locale synchronisé en fréquence avec le signal numérique interpolé à n points.

10. Procédé selon la revendication 1, dans lequel l'au moins une variable de processus dans l'étape de démodulation en quadrature est le nombre n de points d'interpolation.

11. Procédé selon la revendication 1, dans lequel l'au moins une variable de processus dans l'étape de démodulation en quadrature est la fréquence d'oscillation locale du signal d'oscillation locale.

12. Procédé selon la revendication 21, dans lequel l'au moins une variable de processus dans l'étape de filtrage est le nombre de points de lissage utilisés pour réduire le nombre d'échantillons.

13. Procédé selon la revendication 2, dans lequel l'au moins une variable de processus dans l'étape de filtrage est une caractéristique de filtre dans l'étape de filtrage numérique.

14. Procédé selon l'une quelconque des revendications 2 et 8 à 13, comprenant en outre une étape de commande de gain consistant à commander l'amplitude maximale du signal modulé reçu de façon qu'elle soit une valeur fixée qui est l'au moins une variable de processus.

15. Procédé selon la revendication 14, comprenant en outre :

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une étape de détection de demande de changement de variable de processus consistant à détecter une demande de changement de variable de processus;
une étape de détermination de variable de processus consistant à réagir à la demande de changement de variable de processus en déterminant quelle variable de processus doit être changée, et sa valeur; et
une étape de changement de la variable de processus pour qu'elle devienne la variable déterminée.

16. Procédé selon la revendication 15, dans lequel chacune des étapes est exécutée en décodant et en exécutant un programme.

17. Procédé selon la revendication 16, dans lequel l'étape de détermination de variable de processus est une étape consistant à lire une variable de processus préenregistrée, en réponse à la demande de changement de variable.

18. Procédé selon la revendication 18, dans lequel la demande de changement de variable est introduite en manipulant un moyen de fixation / d'entrée.

19. Procédé selon la revendication 17, dans lequel l'étape de détection de demande de changement de variable de processus est une étape consistant à détecter la demande de changement de variable de processus à partir d'un signal reçu.

20. Détecteur de signal numérique, comprenant :

un convertisseur A/N (32) pour convertir en un signal numérique un signal analogique modulé reçu;
un moyen de démodulation en quadrature (33) pour effectuer une opération de démodulation en quadrature numérique sur le signal numérique en utilisant un signal d'oscillation locale numérique d'une fréquence d'oscillation locale, en tant que variable de processus;
un moyen de filtrage (34) pour effectuer une opération de filtrage passe-bas numérique sur le signal numérique démodulé en quadrature, en utilisant des caractéristiques de filtre en tant que variables de processus;
un moyen d'entrée (36) pour introduire une demande de changement de variable de processus pour changer une variable de processus; et
un moyen de commande (35) réagissant à la demande de changement de variable de processus en changeant au moins une variable de processus dans l'un au moins du moyen de démodulation en quadrature, pour changer la fréquence d'oscillation locale conformément à une fréquence porteuse, et du moyen de filtrage (34) pour changer les caractéristiques de filtre conformément à la technique de modulation et au débit de transmission;

caractérisé par

un moyen d'interpolation (41I, 41Q) pour effectuer un traitement d'interpolation à n points sur le signal numérique provenant du convertisseur A/N (32), pour interpoler à l'intérieur des échantillons à n points, pour produire un signal numérique interpolé à n points devant être démodulé en quadrature par le moyen de démodulation en quadrature (33), le nombre n étant un nombre réel égal ou supérieur à 1;
un moyen d'oscillation locale (45) pour générer le signal d'oscillation locale numérique par l'intermédiaire d'une opération numérique;
un moyen de multiplication (42) pour effectuer une multiplication complexe du signal numérique interpolé à n points, par le signal d'oscillation locale numérique; et
un moyen de décimation (43I, 43Q) pour effectuer un traitement de décimation à n points sur un signal numérique résultant de la multiplication complexe, pour décimer à partir de celui-ci des échantillons auxdits n points.

21. Détecteur selon la revendication 20, dans lequel le moyen de filtrage (34) comprend :

un moyen de lissage (51) pour lisser le signal de sortie du moyen de démodulation en quadrature (33) et pour effectuer une opération pour réduire le nombre d'échantillons du signal de sortie; et
un moyen de filtrage numérique (52) pour effectuer une opération de limitation de bande sur le résultat de l'opération effectuée par le moyen de lissage (51), en utilisant lesdites caractéristiques de filtre.

22. Détecteur selon la revendication 21, comprenant en outre une unité de commande automatique de gain (31) placée à un étage qui précède le convertisseur A/N (32), pour commander le gain du signal modulé reçu, de façon que

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son amplitude maximale devienne une valeur fixée qui est l'une des variables de processus qui peuvent être changées par le moyen de commande (35).

23. Détecteur selon la revendication 22, comprenant en outre un élément de stockage (102) dans lequel est préenregistrée une table comparative de demandes de changement de variable et de variables de processus, et dans lequel le moyen de commande (35) est un moyen qui réagit à la demande de changement de variable de processus en lisant l'élément de stockage et en changeant la variable de processus correspondant à celle qui est lue.

24. Détecteur selon la revendication 23, dans lequel le moyen d'entrée (36) est un moyen de fixation / d'entrée pour introduire la demande de changement de variable de processus, par une opération manuelle.

25. Détecteur selon la revendication 23, dans lequel le moyen d'entrée est un moyen (36) pour détecter la demande de changement de variable de processus à partir d'un signal reçu.

26. Détecteur selon l'une quelconque des revendications 20 à 25, dans lequel le moyen de commande (35) comprend un programme et un microprocesseur pour décoder et exécuter le programme.

27. Détecteur selon la revendication 26, dans lequel le moyen de commande (35) remplit également la fonction d'un moyen de commande d'un émetteur-récepteur de radio numérique.

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FIG. 1A PRIOR ART

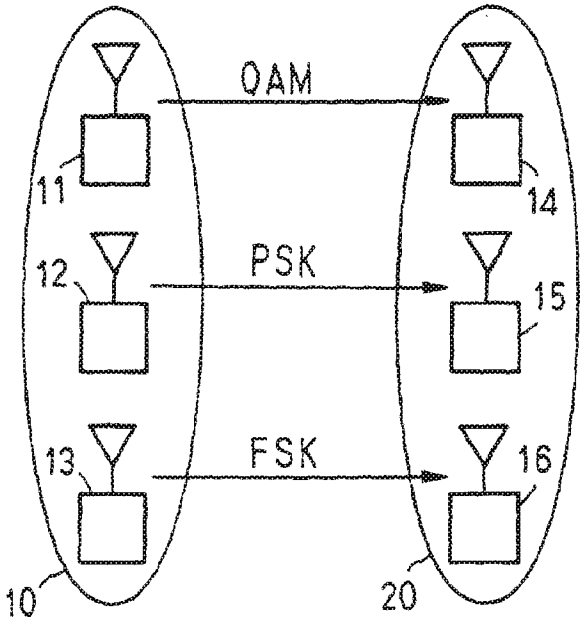

FIG. 1B PRIOR ART

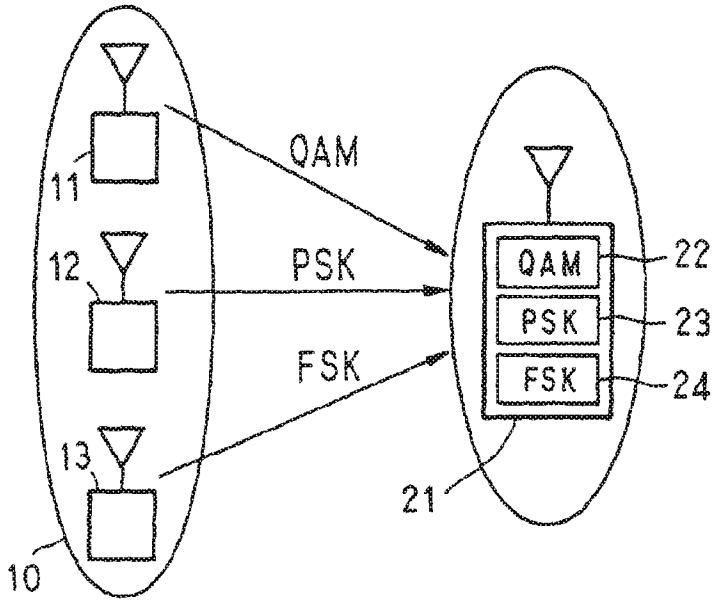

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FIG. 2A PRIOR ART

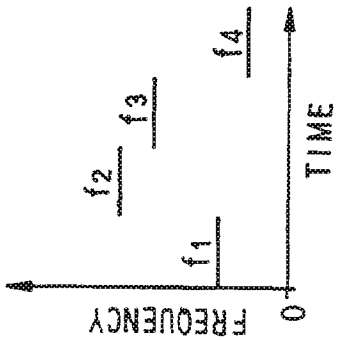


FIG. 2B PRIOR ART

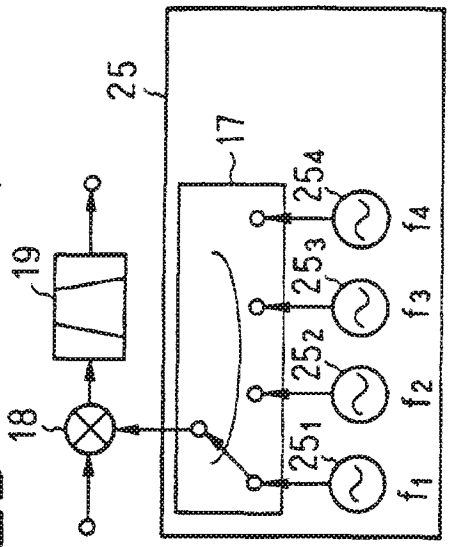


FIG. 2C PRIOR ART

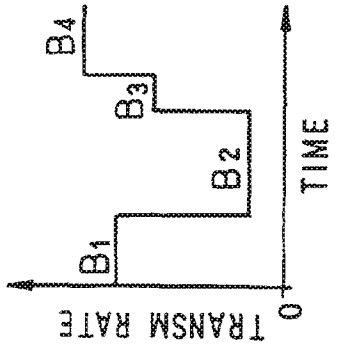
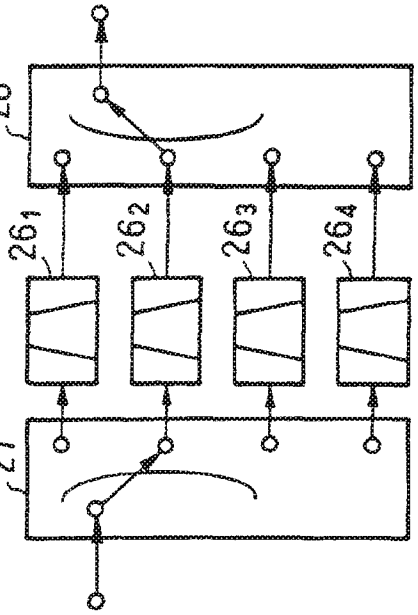


FIG. 2D PRIOR ART



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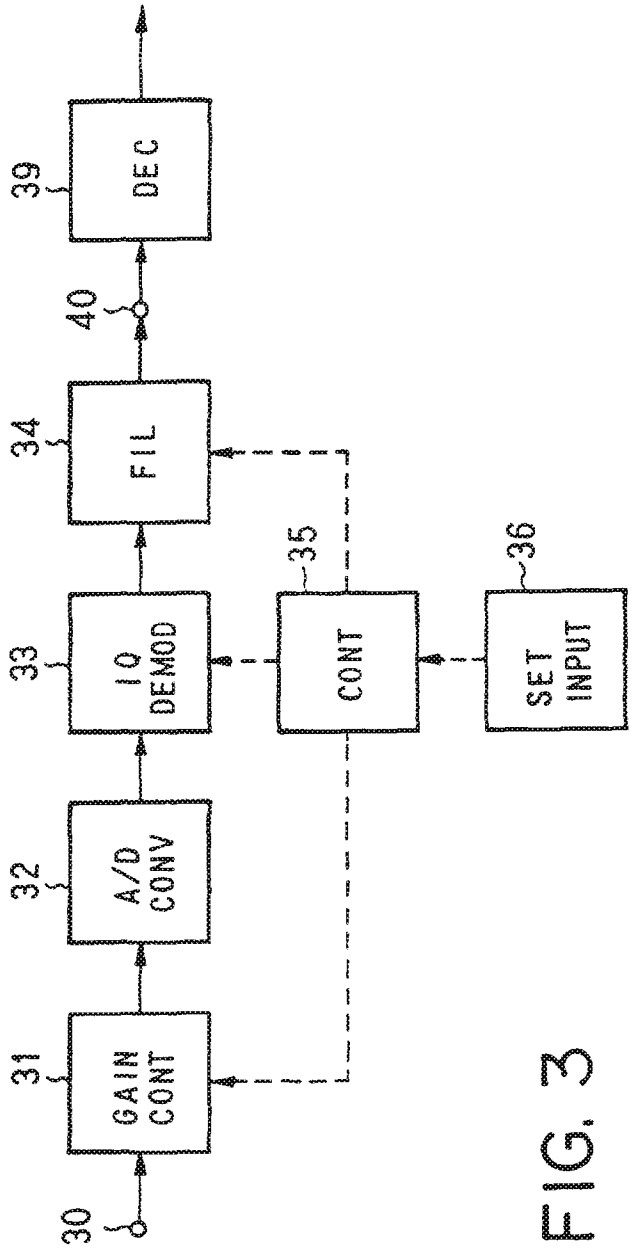

FIG. 3

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FIG.4A

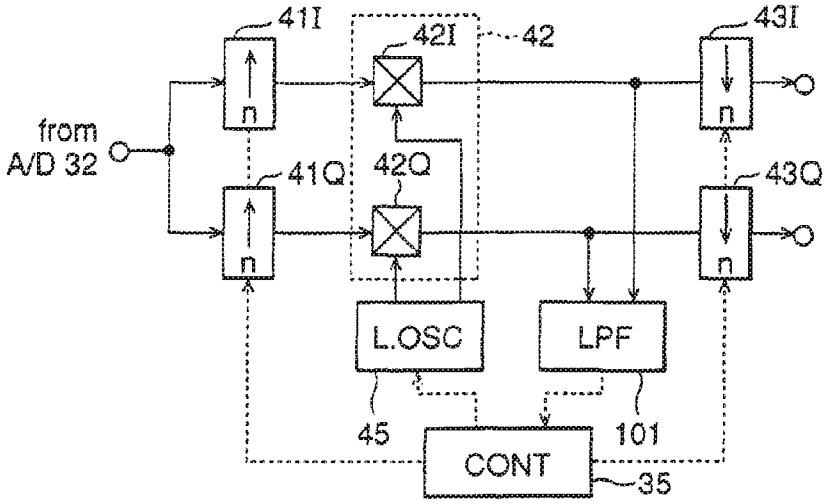
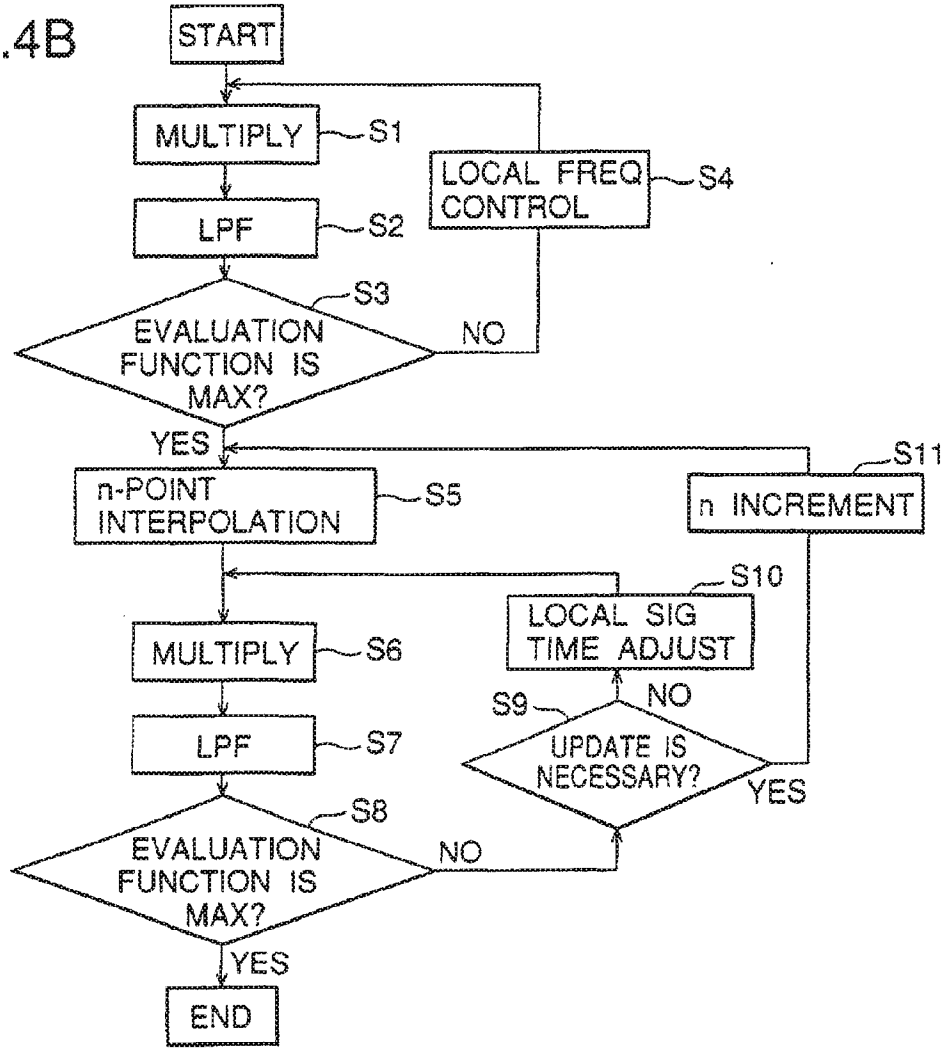


FIG.4B



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DEF0000299

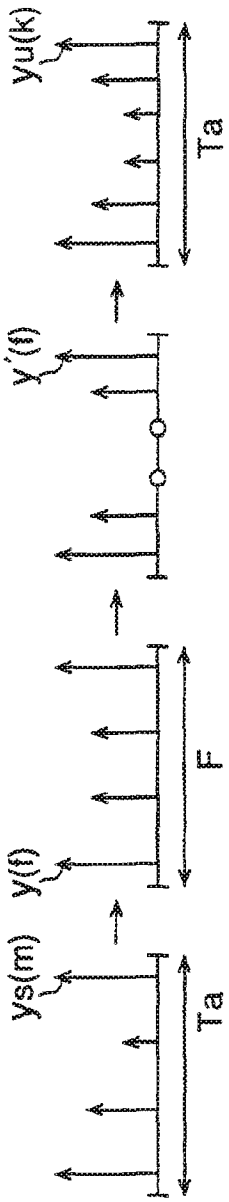

FIG.5A

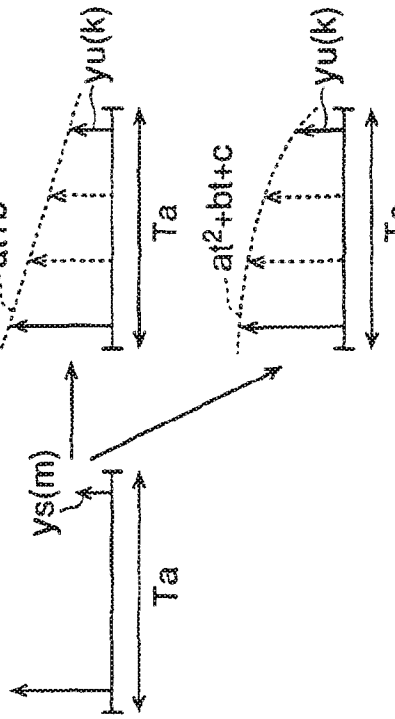

FIG.5B

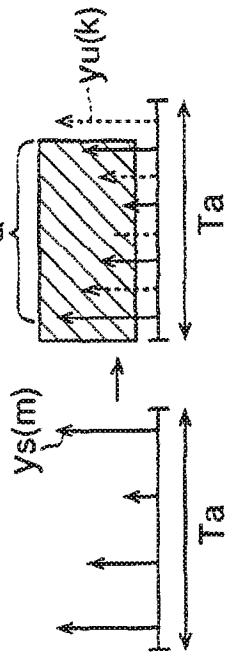

FIG.5C

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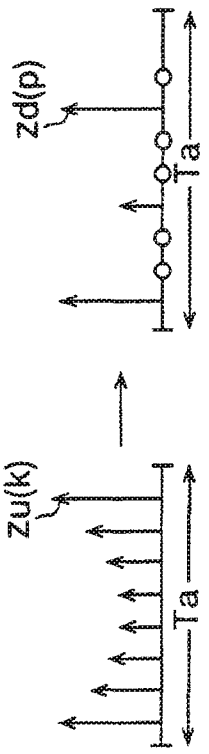

FIG.6A

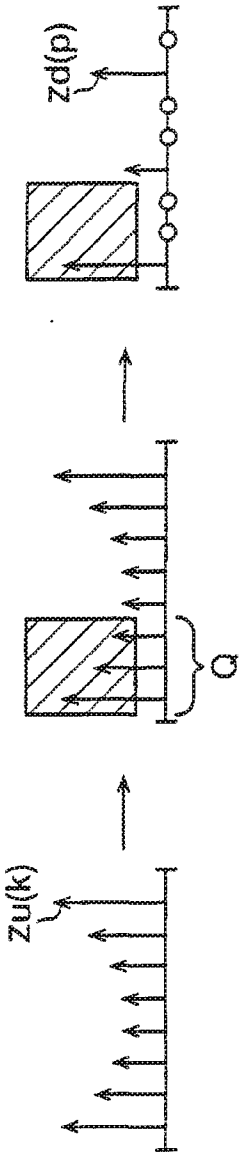

FIG.6B

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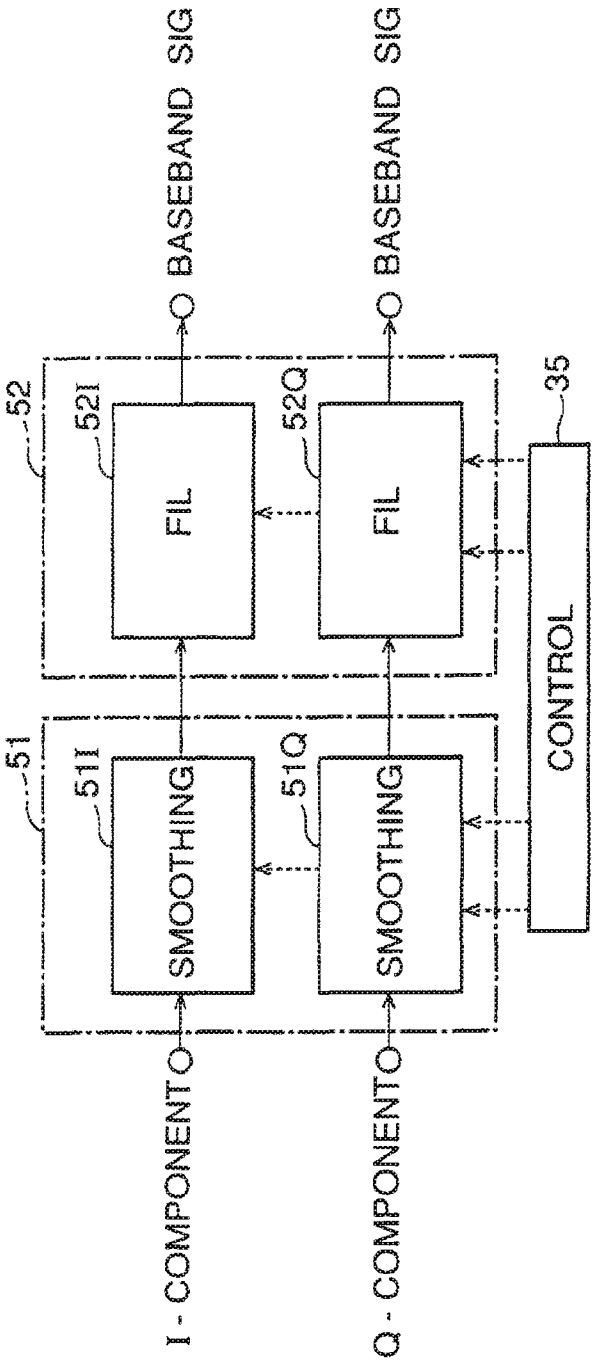
FIG.7



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DEF0000302

FIG.8A

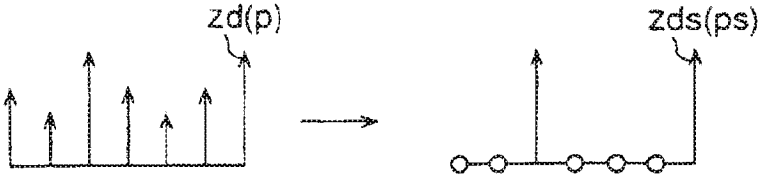


FIG.8B

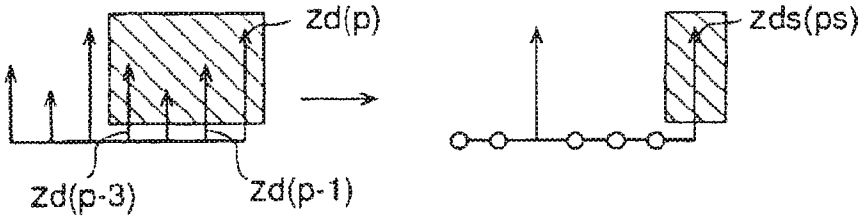
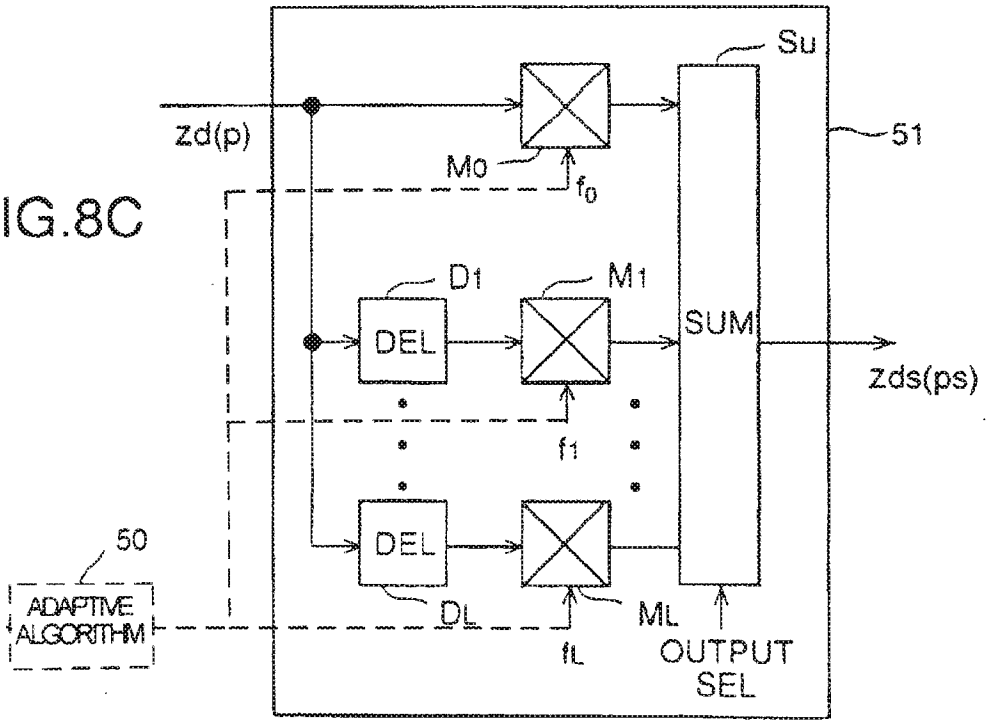


FIG.8C



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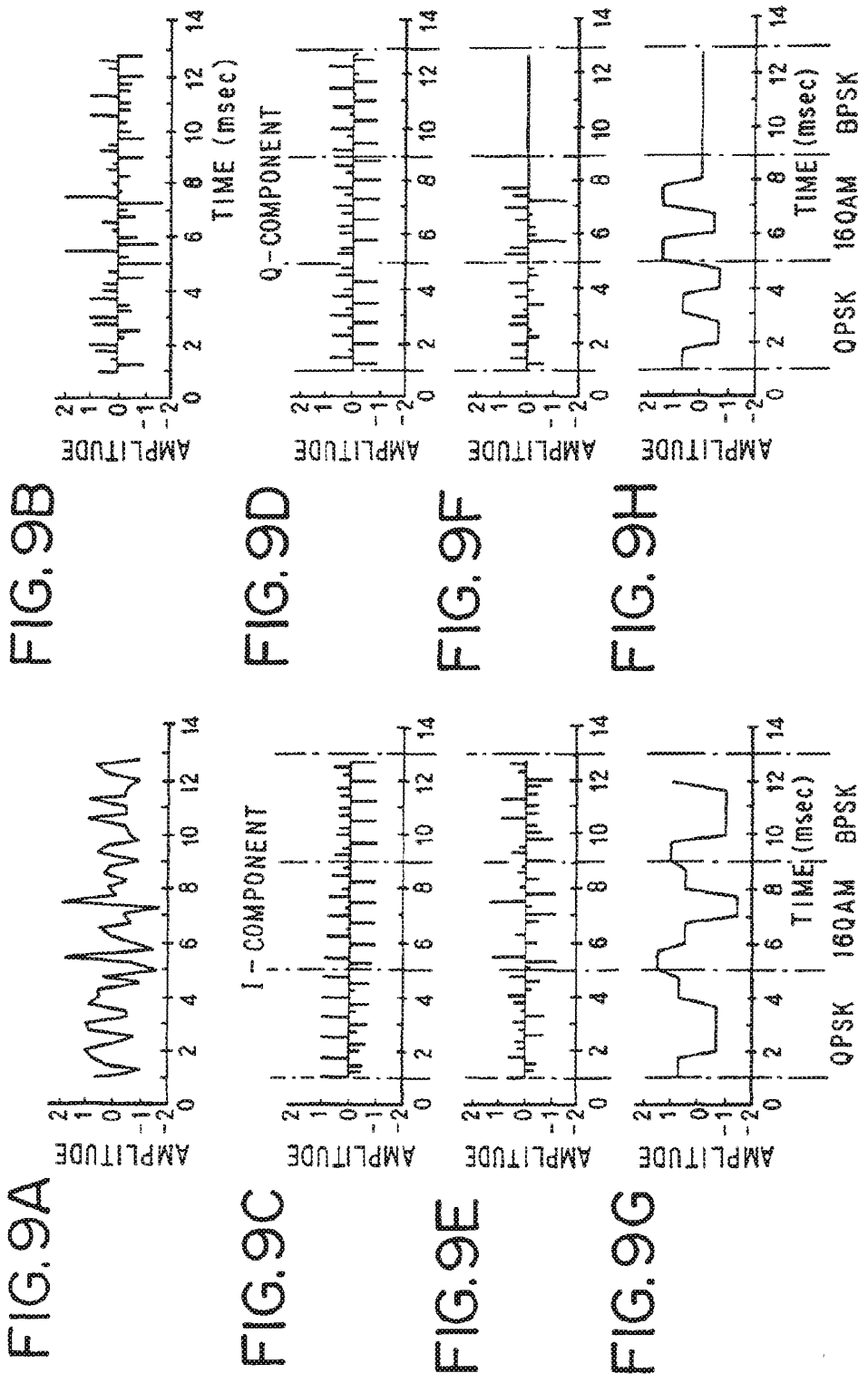
DEF0000303



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DEF0000304

FIG. 10A

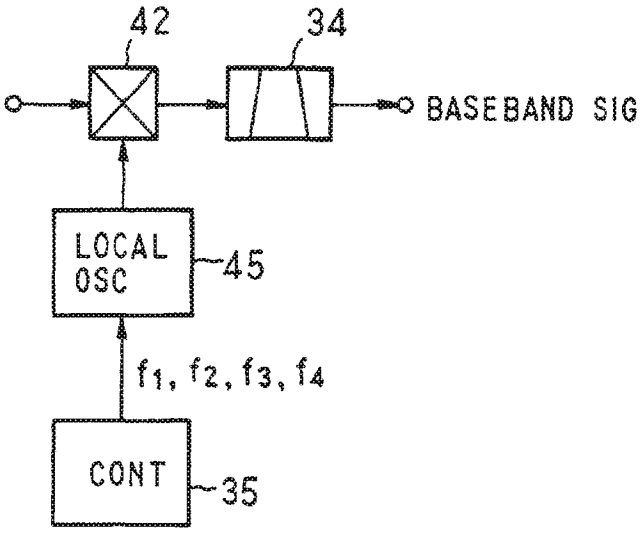
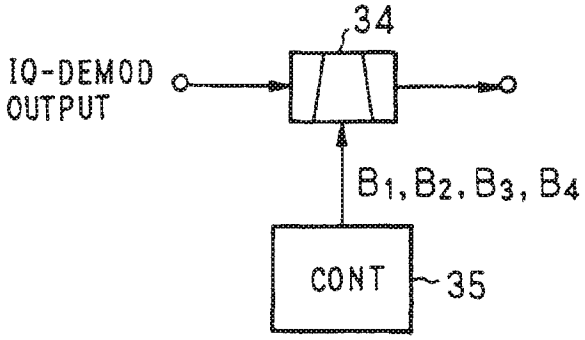


FIG. 10B



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DEF0000305

FIG.11

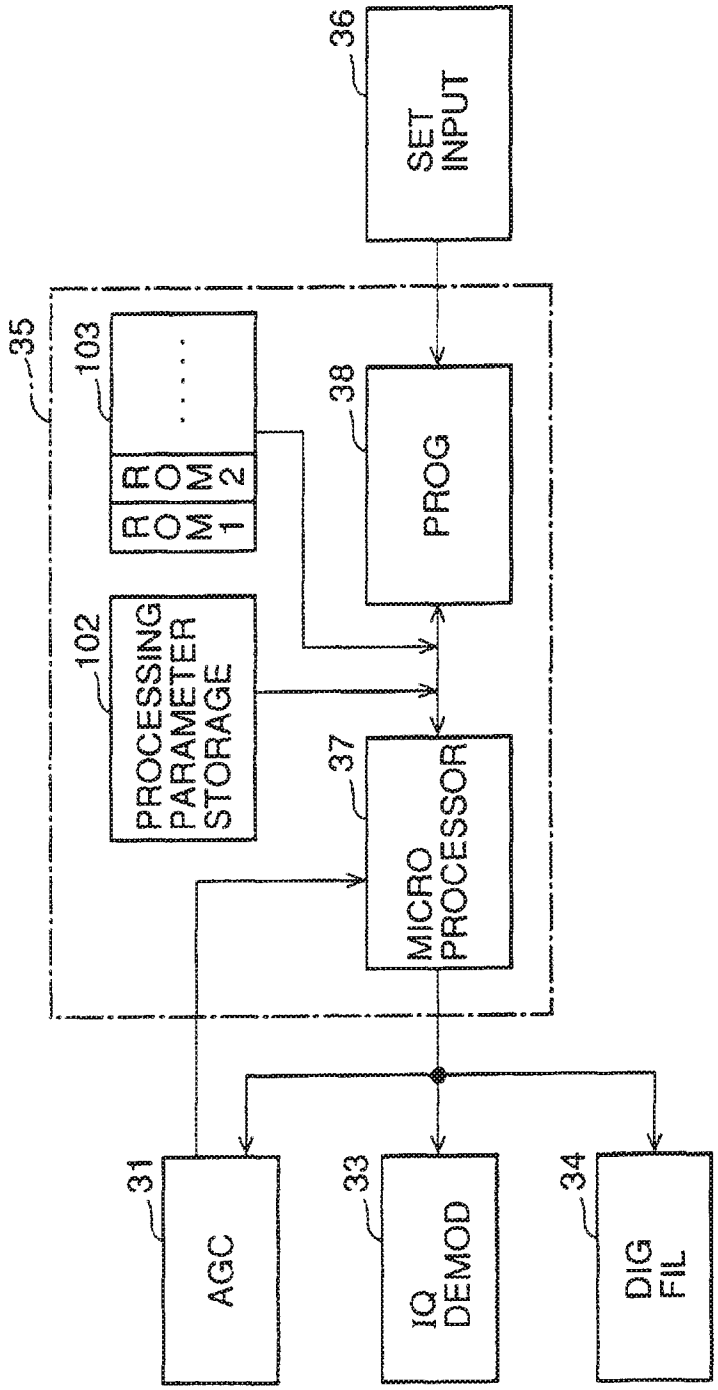

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FIG.12

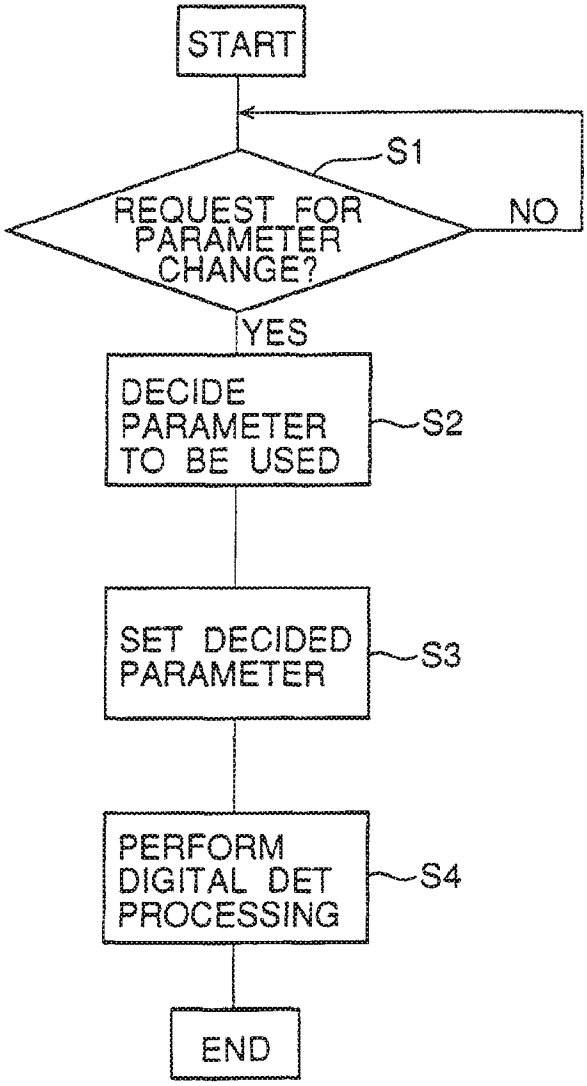

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FIG.13

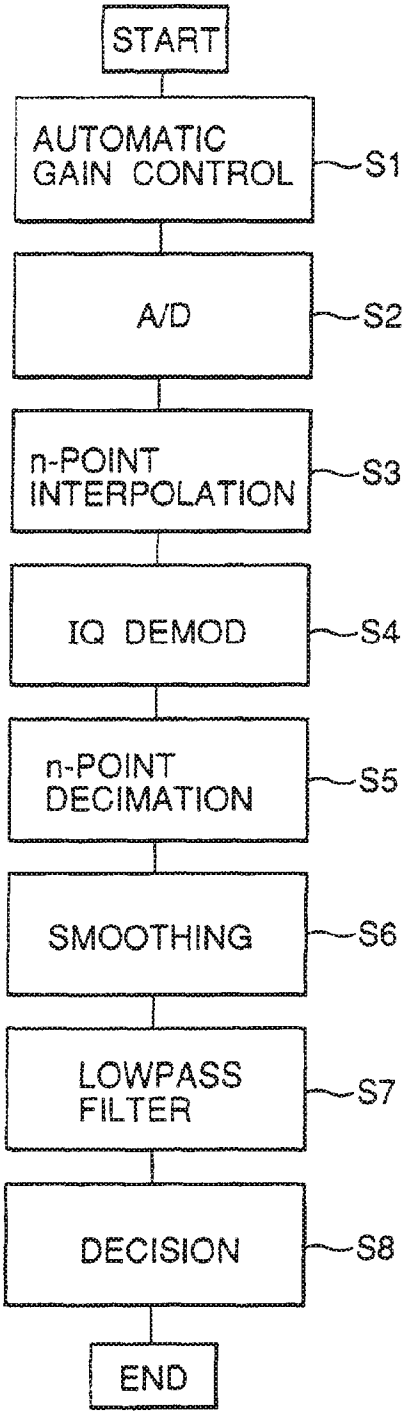

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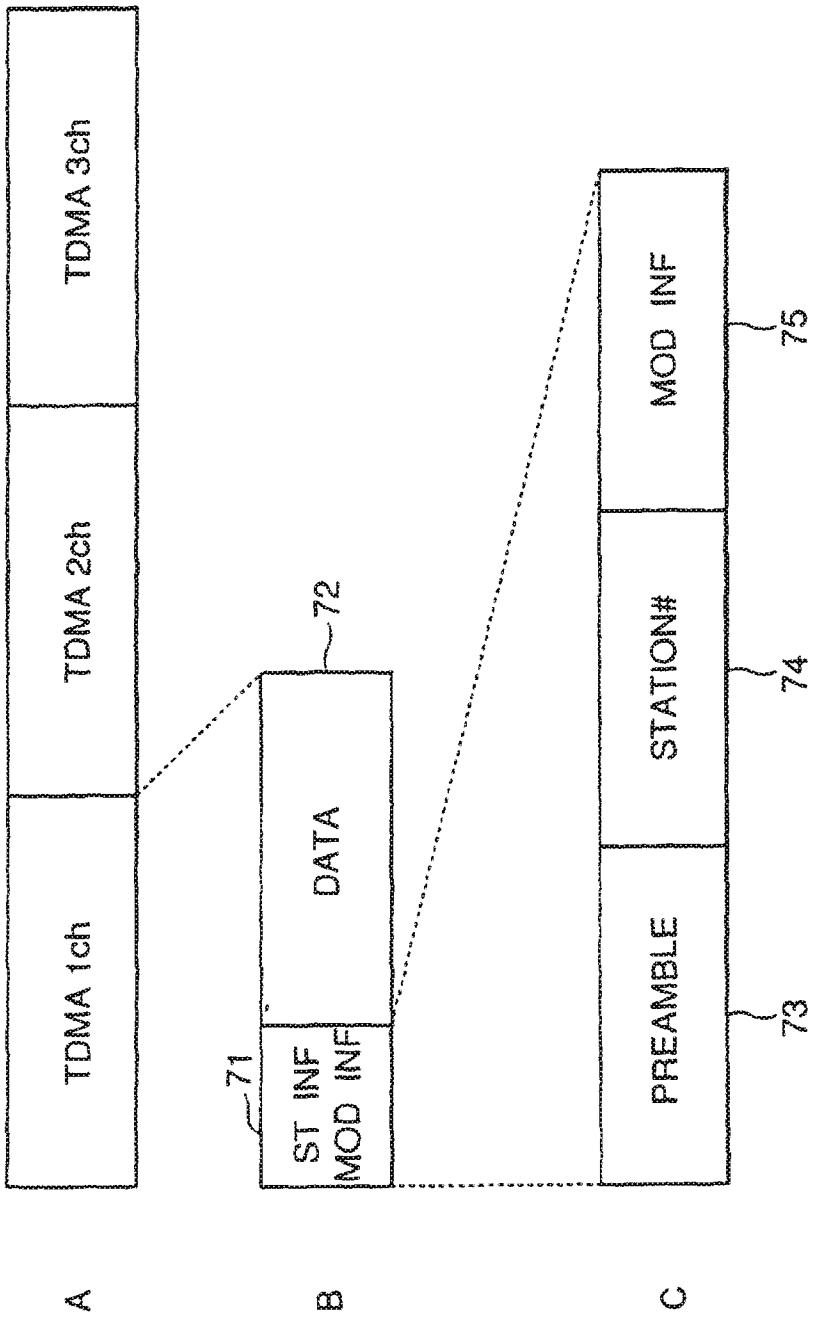
FIG.14



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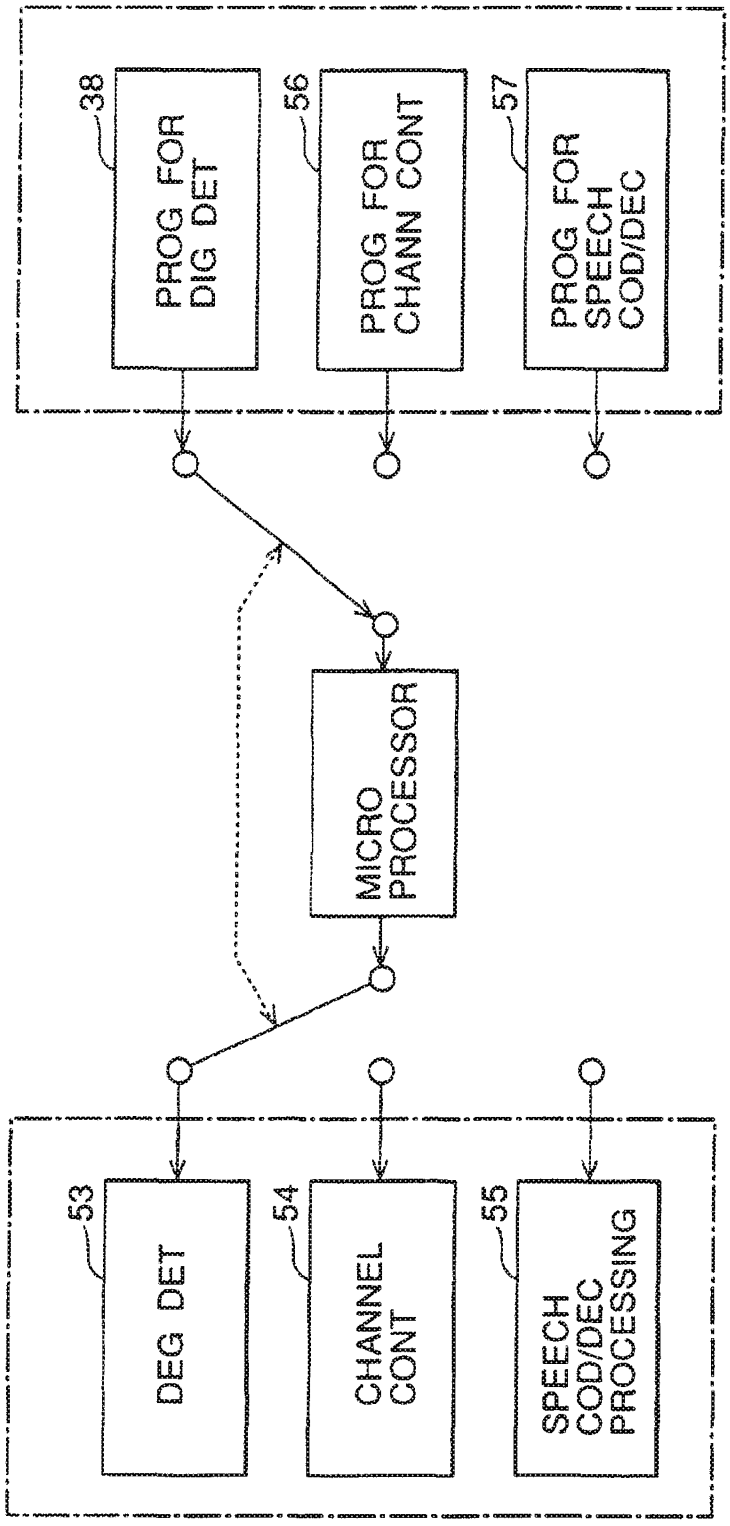
DEF0000309

FIG.15



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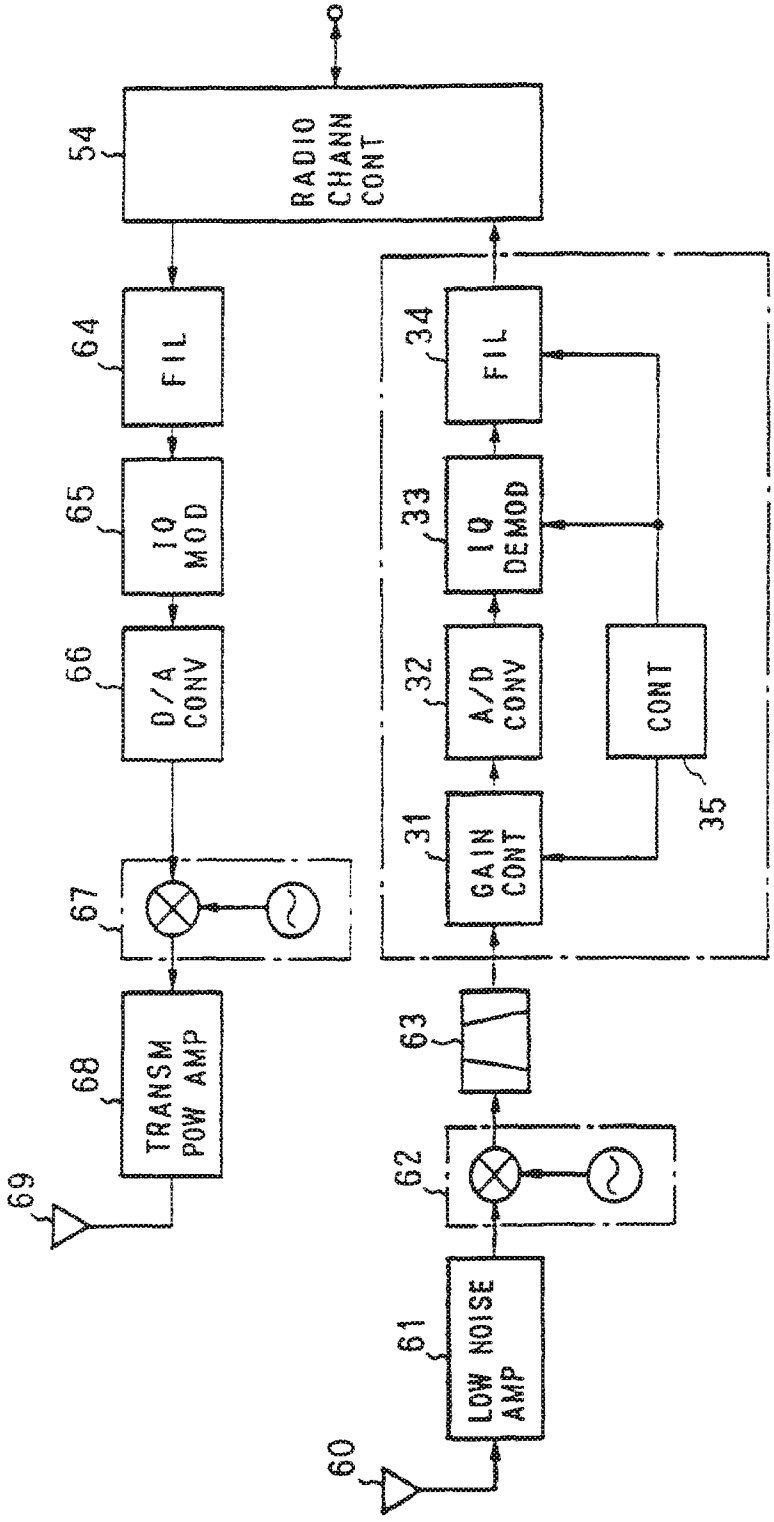
DEF0000310

FIG. 16



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DEF0000311

FIG.17A

	MAX AMPLITUDE	n	SMOOTHING	ROLL-OFF RATIO	FIL COEFF
AUDIO	AM1	n1	ROM1	RO1	$h_1, h_2, \cdots, h_n$
IMAGE	AM2	n2	ROM2	RO2	$h_1, h_2, \cdots, h_m$

FIG.17B

MOD TYPE	MAX AMPLITUDE	n	SMOOTHING
QPSK	AM1	n1	ROM1
16QAM	AM2	n2	ROM2

FIG.17C

CODE RATE	ROLL-OFF RATIO	FIL COEFF
B1	RO1	$h_1, h_2, \cdots, h_n$
B2	RO2	$h_1, h_2, \cdots, h_m$

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DEF0000312

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(11) EP 0 845 916 B1

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(21) Application number: **97850165.8**

(22) Date of filing: **02.12.1997**

(54) Point to multipoint radio access system

Punkt zu multipunkt Funksystem

Système radio point à multipoint

(84) Designated Contracting States:
DE FR GB SE

(30) Priority: **02.12.1996 US 31536 P**
13.08.1997 US 910147

(43) Date of publication of application:
03.06.1998 Bulletin 1998/23

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Ericsson AB,
Patent Unit Radio Networks
164 80 Stockholm (SE)

(56) References cited:
WO-A-95/25409

- **SAMPEI S ET AL: "ADAPTIVE MODULATION/TDMA SCHEME FOR PERSONAL MULTI-MEDIA COMMUNICATION SYSTEMS" PROCEEDINGS OF THE GLOBAL TELECOMMUNICATIONS CONFERENCE (GLOBECOM), SAN FRANCISCO, NOV. 28 - DEC. 2, 1994, vol. VOL. 2, 28 November 1994, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 989-993, XP000488685**
- **VADGAMA S K: "ADAPTIVE BIT RATE TRANSMISSION FOR PERSONAL COMMUNICATIONS" PROCEEDINGS OF THE NORDIC SEMINAR ON DIGITAL LAND MOBILE RADIO COMMUNICATIONS (DMR), OSLO, JUNE 26 - 28, 1990, no. SEMINAR 4, 26 June 1990, GENERAL DIRECTORATE OF POSTS AND TELECOMMUNICATIONS;FINLAND, pages 1-9, XP000515571**

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EP 0 845 916 B1

Description

BACKGROUND

1. Field of Invention

[0001] This invention pertains to a point to multipoint radio access system. The invention particularly pertains to the configuration of such system which utilizes a number of different modulation methods, the modulation methods being distinguishable with regard to the bandwidth efficiency but also with regard to the coverage range and the interference immunity.

2. Related Art and Other Considerations

[0002] Radio access methods have become frequently used to enable the rapid and economic implementation of the access network in modern telecommunication networks. Most known solutions up to date are based on conventional mobile cellular techniques, where the subscribers are fixed instead of mobile. One disadvantage of using cellular techniques for the access network is that the radio spectrum is limited and the implication of this is that these systems normally have a too limited capacity, especially in cities.

[0003] Recently a new point to multi point system has been suggested that uses microwave links between a central base station and subscriber terminals. The central base station uses normally 45 or 90 degree sector antennas and the terminals directive antennas pointing towards the base station.

[0004] In the suggested system, frequency reuse can be very effective by the use of alternating vertical and horizontal polarizations for the links in adjacent sectors.

[0005] Also, the line of sight radio links lends themselves to high quality connections, the capacity of which can be adapted individually to different capacities (bitrates).

[0006] To further improve on the frequency economy of this system, it has been suggested to use a number of different modulation types for the links. The highest order of modulation requires minimum bandwidth for a given bitrate but has also the minimum range and is most sensitive for interferences from other links. The lowest order of modulation is the most robust. It has the longest coverage range and is also the least sensitive to interferences from other links.

[0007] The problem in this kind of system is then to select for each link the most suitable modulation, considering bandwidth economy, coverage range and the foreseen interference situation.

[0008] A system of this kind is described in a paper entitled Link Capacity and Cellular Planning Aspects of a Point to Point Fixed Radio Access System, by A Bollmann, D. Chicon, and M Glauner, European conference on Radio Relay Systems 1996, Bologna, Italy. However heretofore there has not been a clear cut procedure for arriving to a suitable strategy to allocate suitable modulation types and bandwidth to each terminal in the system.

[0009] In an article by Sunil K. Vadgama titled "Adaptive Bit Rate Transmission for Personal Communications", Proc. of the Nordic seminar on digital land mobile radio communications (DMR), Oslo, June 26 - 28, 1990, the idea of trading off transmission bit rate for either lower transmission power or extra communication range is discussed. It is noted that in multilevel modulation the bit rate is varied by changing the order of modulation, i.e. the number of bits per modulation symbol, whereby the nominal bandwidth remains constant, making frequency planning simpler. Three system implementations are suggested for a personal communication system: a) using a fixed modulation in a given type of cell, b) creating a number of concentric zones using respective modulation orders, and c) varying the modulation order dynamically across each cell. However, it is noted that the latter implementation would require rather complex signaling, call setup protocols and frame formats. This document forms the preamble of claim 1.

[0010] What is needed, therefore, is a system, which enables a proper choice of a modulation type considering bandwidth efficiency, coverage range and the interference situation.

SUMMARY

[0011] A method is provided for allocating radio link characteristics in a point to multipoint radio access system. The point to multipoint radio access system comprising a number of base stations including a selected base station connected by a plurality of radio links to a corresponding plurality of subscriber terminals located within respective coverage areas of the selected base station. At least some of the plurality of radio links are within a same frequency band.

[0012] In accordance with the method, a base station power density is selected for the selected base station. The base station power density, for each of a plurality of modulation types, is constant for all bitrates. Similarly, for each of the plurality of subscriber terminals located within the coverage area of the selected base station, a terminal power density is selected. The terminal power density, for each of the plurality of modulation types, is constant for all bitrates. A maximum range is then determined for each of the plurality of modulation types. Then, for each of the plurality of

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subscriber terminals, a modulation type is allocated to the corresponding radio link dependent upon range from the selected base station. A determination is then made, for each of the plurality of subscriber terminals, whether at the subscriber terminal there is an acceptable signal quality. If not, a next lower modulation type is allocated to the radio link corresponding to the subscriber terminal which does not have the acceptable signal quality.

[0013] After the foregoing has occurred with respect to the subscriber terminals, a determination is made at the selected base station whether there is an acceptable signal quality with respect to each of the plurality of subscriber terminals. If not, the radio link corresponding to the subscriber terminal having unacceptable signal quality is allocated a next lower modulation type. Thereafter, frequencies and bandwidth are allocated to each of the plurality of radio links.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The foregoing and other objects, features, and advantages of the invention will be apparent from the following more particular description of preferred embodiments as illustrated in the accompanying drawings in which reference characters refer to the same parts throughout the various views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

Fig. 1 is schematic view of a microwave coverage network according to an embodiment of the invention.

Fig. 1A is an enlarged schematic view of a portion of a coverage area served by a base station site of the network of Fig. 1.

Fig. 2 is a schematic view of a base station according to an embodiment of the invention.

Fig. 3 is a schematic view of a base station network according to an embodiment of the invention.

Fig. 4 is a schematic view depicting the relationship of Fig. 4A and Fig. 4B.

Fig. 4A and Fig. 4B are flowcharts showing steps executed by a network planning processor according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[0015] In the following description, for purposes of explanation and not limitation, specific details are set forth such as particular architectures, interfaces, techniques, etc. in order to provide a thorough understanding of the present invention. However, it will be apparent to those skilled in the art that the present invention may be practiced in other embodiments that depart from these specific details. In other instances, detailed descriptions of well known devices, circuits, and methods are omitted so as not to obscure the description of the present invention with unnecessary detail.

[0016] Fig. 1 shows a microwave coverage network 20. Network 20 includes a regular pattern of base station sites and the corresponding cell or coverage area for each base station site. In Fig. 1, the cell or coverage area for each base station site is shown as a square, with a base station site being located at the center of the square (i.e., the center of the cell). For example, base station site B1 is centrally located in its cell C1 and base station site B2 is centrally located in its cell C2.

[0017] In the illustrated embodiment, each cell C comprises four triangular sectors. For example, cell C1 comprises sectors $S1_{C1}$, $S2_{C1}$, $S3_{c1}$, and $S4_{C1}$ and cell C2 comprises sectors $S1_{C2}$, $S2_{C2}$, $S3_{C2}$, and $S4_{C2}$.

[0018] Fig. 1A shows an enlargement of the center of cell C1 served by base station site B1. As seen in Fig. 1A, each base station site, such as base station site B1, includes four base stations (base stations B1-1, B1-2, B1-3, and B1-4 being shown as included in base station site B1 in Fig. 1A).

[0019] As shown both in Fig. 1 and Fig. 1A, alternating sectors S of a cell C have differing polarizations. That is, directly adjacent sectors receive transmissions in orthogonal polarizations to obtain decoupling in the overlap regions of the antenna patterns. For example, in cell C1 sectors $S1_{C1}$ and $S3_{C1}$ have horizontal polarization (as indicated by the letter "H") while sectors $S2_{C1}$ and $S4_{C1}$ have vertical polarization (as indicated by the letter "V").

[0020] In Fig. 1, two terminals T1 and T2 are shown. Terminal T1 is located in sector $S4_{C1}$ which is served by base station B1-4; T2 is located in sector $S4_{C2}$ which is served by base station B2-4. Terminals T1 and T2 are thus served by base stations which use the same polarizations.

[0021] In the particular configuration shown in Fig. 1, base stations B1, B2 have approximately 90 degree wide antennas. Terminals T1 and T2, on the other hand, have much smaller antenna beamwidths, typically 4-8 degrees. Although only two terminals T1 and T2 are illustrated in Fig. 1, it should be understood that many terminals typically reside in each sector S. Terminals are located at premises of customers, with each terminal being connected by lines

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(e.g., POTS or ISDN lines) to many telephone subscribers. Each terminal is dedicated and adjusted to one base station (e.g., terminal T1 is dedicated to base station B1-4).

[0022] Although there are several terminals within each sector, for a given sector each terminal T is allocated its individual frequency from a range of frequencies available in that sector. It can occur that the same frequency is being utilized both in sector $S4_{C1}$ and $S4_{C2}$. Thus, if terminals T1 and T2 were assigned the same frequency, a potential interference problem would arise. In this regard, a signal transmitted on a frequency f1 to terminal T1 from base station B1-4 at site B1 would, due to the wide antenna angle of base station B1-4, also hit the terminal T2 as indicated by line 30. If terminal T2 is also using frequency f1, interference would result. Thus, base station B1-4 could cause interference at terminal T2.

[0023] Likewise, terminal T2 could cause interference in base station B1-4. In this regard, terminal T2 has a narrow antenna beam which is directed towards its own base station B2-4. Normally the signal directed from terminal T2 to base station B2-4 would not hit the base station B1. However, if terminal T2 is more or less in line with both base station B2-4 as well as with base station B1-4 in the manner shown in Fig. 1, interference may arise. In this situation, the antenna of terminal T2 cannot discriminate between base station B2-4 and base station B1-4, and interference results.

[0024] It should be understood the use of four sectors S per cell as illustrated in Fig. 1 is merely to serve as an example. Whereas Fig. 1 illustrates each cell C sector at ninety degrees in view of the particular antennae employed, the cells can be sectored at other angles (e.g., forty five degree or fifteen degree angles) in accordance with the angles of the antennae chosen for the base stations.

[0025] The person skilled in the art will appreciate that the wide angle sectored base station antennae have a lower gain than the highly directive terminal antennae (which have a smaller beam). For example, an antenna at a terminal T may have an eight degree main beam with high antenna gain (e.g., 22 dB at 10 Ghz).

[0026] Fig. 2 shows a block diagram of a base station 40 (base station 40 being representative, for example, of base stations B1-4 and B2-4 discussed above). Base station 40 includes in its transmitter part a plurality of transmission channels 41, one such channel 41A being fully shown in Fig. 2. Each channel 41 has a modulator 42 and an upconverter 44 to convert the signals to RF-frequency. All transmission channels 41 are connected to power amplifier 46 as indicated by lines 47. Base station 40 also has a receiver part or receiver side having receiver channels 51, only channel 51A being fully illustrated in Fig. 2. All receiver channels 51 share a common RF-amplifier 52. Amplifier 52 is connected by lines 53 to each receiver channel 51. Each receiver channel 51 includes a down converter 54 and a demodulator 56. Duplexer 60 of base station 40 combines the transmitter and the receiver to a common antenna 62. The modulator 42 and demodulator 56 of each channel (commonly known as a modem) are controlled by a control unit 70. Control unit 70 connects to all transmission and receive channels. Control unit 70 sets the basic link parameters for the modem, i. e. modulation type, transmit power density, and bitrate. In a DBA (Dynamic Bandwidth Allocation) mode, control unit 70 also makes bandwidth allocations to the individual terminals on a momentary basis.

[0027] Fig. 3 shows an overview of a base station network 100. A number of base stations 40_0, 40_1, 40_2, etc. are connected to a Network Management System (NMS) 102. In particular, control units 70 of the plurality of base stations 40 are connected to Network Management System (NMS) 102.

[0028] Network Management System (NMS) 102 is, in turn, connected to a network planning processor (NPP) 110. Network planning processor (NPP) 110 can take various forms, such as a stand alone personal computer (PC). Operations and calculations performed by NPP 110 are described in more detail below. Results and outputs from Network planning processor 110 are transmitted to Network management system 102. The output operations from Network planning processor 110 to Network management system 102 can take the form of a simple file transfer. Inputs to Network management system 102 include the allowed modulation types for each terminal T. Thus, when control unit 70 of a base station 40 allocates a channel to a particular terminal T, control unit 70 knows beforehand which modulation types are allowed due to the interference situation.

[0029] The inputs to Network planning processor 110 include the locations of the base stations B and the terminals T; the particular antenna patterns employed; basic link parameters such as power densities available; and modulation sensitivities such as C/N and C/I requirements. In addition, in an FBA (Fixed Bandwidth Allocation) mode, the inputs include the capacities (bitrates) needed per terminal.

[0030] As the notion of modes has been broached above, it should be mentioned that the invention can operate in either of two modes of operation. In the FBA (Fixed Bandwidth Allocation) mode, each specific terminal is allocated a specific capacity (bitrate), modulation type, bandwidth and frequency once and for all. In the Dynamic Bandwidth Allocation (DBA) mode, each terminal is allocated a capacity, modulation type and bandwidth by controller 70 according to the actual need at every moment. In the DBA mode any terminal can change allocated frequency with time as the system tries to move the users to make optimum usage of the total bandwidth.

[0031] Mention is also often made herein to "modulation types". Five different examples of modulation types and corresponding characteristics are shown in Table I.

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TABLE I

Example Modulation Types and Corresponding Characteristics				
Modulation Type	C/N	C/I	Efficiency	Relative range
QPSK ½	6.5	9.5	0.85	1
QPSK 3/4	9	12	1.30	0.75
QPSK 7/8	11	14	1.50	0.60
8 TCM 2/3	11.5	14.5	1.70	0.55
16 TCM 3/4	18	21	2.50	0.26

In Table I, the C/I ratio are the values for 3 dB degradation of the noise threshold. This difference is necessary in C/N and C/I is 11.5 dB for the two extremes. The bandwidth requirements are differing by a factor of 3 and the range by a factor of almost 4 between the most robust and the most bandwidth efficient modulation.

[0032] Fig. 4A and Fig. 4B show selected general operations or steps performed by Network planning processor 110 in accordance with the present invention. Prior to performance of the steps shown in Fig. 4A and Fig. 4B, it is assumed four preliminary steps have occurred.

[0033] As a first preliminary, the sites and the needed capacities in number of 64 kb/s lines per site are defined. As a second preliminary, the base station sites B are found by overall considerations of capacity and coverage. For selection of appropriate sites, use is made of line of sight (LOS) coverage diagrams in Network planning processor 110. The base station sites are sectorized and the different sectors are allocated different polarizations. As a third preliminary, terminal sites are allocated to the different base stations. As a fourth preliminary, rain zone and the requirements on unavailable time (UAT) and link quality are defined. Typical other link quality requirements are defined in ITU-T:s Rec G 821. For radio link calculations different rain zones are used, as also defined by ITU.

[0034] Assuming that the foregoing preliminaries have been performed, Network planning processor 110 executes the general steps shown in Fig. 4A and Fig. 4B. Execution begins with selection of a power strategy, as depicted by steps 400 and 402.

[0035] At step 400 a base station's transmit power density (i.e. power transmitted per Hz bandwidth) is selected to be constant for all bitrates and modulation types. This implies that all bitrates transmitted with one specific modulation type have the same range. However a more bandwidth effective modulation type will have a shorter range since it will be less robust [require a higher signal to noise ratio C/N or signal to noise and interference ratio C/(N+I)].

[0036] At step 402 the transmit power density of a terminal is selected to be constant for all bitrates and for all modulation types measured at the range limit of the respective moculation type. With decreasing distance from the terminal to its base station, the power density is decreased so that the power density received at the base is constant for all distances. The power density transmitted from the terminals and also received at the base will differ for the various modulation types with the difference in the C/(N+I) required for the respective modulation types.

[0037] In considering the power selection steps 400 and 402, a typical power density for a base station could be e. g., -60 dBm/Hz bandwidth for all modulation types. For a terminal, power density will vary depending on its distance to the base station, e.g., for a QPSK ½ modulated link the power density could be -70 dBm/Hz at the range limit and would then decrease with distance to result in a constant received power density at the base (the power density would typically decrease with 6 dB for half the distance). For a 16 TCM 3/4 link, the power density would be 11.5 dB higher corresponding to the difference in C/I requirements for a 16 TCM terminal at the same range as a terminal using QPSK $^1/_2$ This implies that the power density received at the base station would be 11.5 dB higher for the 16 TCM terminal.

[0038] At step 404, a maximum range is calculated for each of the various modulation types. At this calculation a 3 dB degradation of the noise threshold is allowed for interference from other links (this means in the C/(N+1) ratio that I=N). The coverage calculations of step 404 are straight forward calculations in microwave link technology which are understood by the person skilled in the art, and accordingly are not described here in further detail. Typical coverage ranges vary with frequency band. In 10.5 GHz, which is a typical band allocated by ITU for point to multipoint services, distances are around 10 km for modulation type QPSK ½ and shorter for the more sensitive modulation types, e.g., 2-3 km for 16 TCM 3/4. In higher frequency bands, e.g. 18 and 26 GHz, ranges are shorter due to the attenuation effect of rain (which is higher with higher frequency). A special case could be that the cell radius is selected so small that all modulation types have enough range.

[0039] At step 406 the minimum bandwidth modulation type is allocated to each terminal in dependence on its range from the base station. Thus, depending on the range of the terminal sites, the different links are allocated a modulation scheme which complies with the maximum range for that modulation and which uses minimum bandwidth.

[0040] At step 408, for each terminal a calculation is performed of the C/I ratio, where C represents the desired signal

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from the own base station sector and I the interference from each other base station sector. The interference from all other (sector) base stations is calculated taking the polarizations, antenna patterns (these have diagrams for both copolar and cross polarizations) and assigned power density into account. These interferences are added together to obtain the "I" of the C/I ratio.

[0041] At step 410, for each terminal the calculated C/I is checked to determine if it is greater than the minimum required C/I. Here the C/I values that represent a 3 dB degradation of the noise threshold should be used to comply with the coverage calculation of step 404. If the required C/I is not satisfied when checked at step 410, for any terminal failing the check the next lower (more robust modulation type) is selected for that terminal (step 412). If a further check (step 414) whether the C/I ratio is greater than the minimum, it is determined that no modulation type will satisfy the condition and the terminal is designated at step 416 as a problem terminal to be handled separated (e.g., such a problem terminal could be denied service or allocated a separate frequency from the total available bandwidth).

[0042] As an example of the foregoing, suppose that at step 410 the C/I is calculated to be 13. Such C/I ratio is permissible if the selected modulation type is QPSK ½, which requires 9.5 dB. On the other hand, if the selected modulation type were 16 TCM 3/4, which requires 21 dB, the nearest most robust modulation type compatible with C/I – 13 dB would be QPSK 3/4. Thus QPSK 3/4 would be selected instead of 16 TCM 3/4. In connection with step 412, it should be noted that a change from one modulation type to another will not affect the C/I calculations just performed as all modulation types are transmitted with the same power density.

[0043] At step 418 (see Fig. 4B) the C/I ratios at the base stations are calculated (i.e., C/I calculations are made from each terminal to its base). For each terminal, the desired signal C is compared to the received interference signals I from other terminals. Note here that within each sector only one terminal will work on a specific frequency. Thus one link at the base station will only be interfered by a maximum of one terminal in each sector. With normal cell plans it is not likely that more than two terminals will contribute significantly to the interference. Thus it will be sufficient as a worst case to add a 3 dB margin to the interference level from the worst terminal.

[0044] At step 420 a check is made at the base station whether the received interference power density is below this maximum for each terminal. If not, at step 422 the terminal is allocated the next more robust modulation type, which will mean that the terminal will decrease its transmit power density. After a further check for such terminal at step 424, any terminal that can not be made to satisfy the condition on maximum interference power is marked as a problem terminal (step 426) and is treated separately as described above.

[0045] The present invention does not lead to a large number of calculations. By observing that (1) the received desired signal C from each terminal is constant for a specific modulation type (see step 402), and (2) that the difference in received signal level for the various modulation types corresponds to the difference in required ratio C/I, it can be derived that the maximum allowed interference level is constant for all modulation types.

[0046] In connection with even numbered steps 418 through 426, it is to be noted that the wanted signal at a base station is always received with the same level for each specific modulation type. For a 16 TCM 3/4 modulated link, however, the received level is 11.5 dB higher than for a QPSK ½ modulated link. As the allowed carrier to interference ratio C/I for the 16 TCM 3/4 link is 11.5 dB higher than for the QPSK link, it can be concluded that the maximum allowed interference level is the same for all modulation types. Thus, in order to check the C/I for the uplink from the terminals to the base stations, it is sufficient to calculate the received interference signal at the base station. For example, if the nominal wanted signal C at the base is -140 dBm/Hz for a QPSK ½ link, the maximum interference signal level would be -140-9.5 = - 149.5 dBm/Hz for all modulation types. Thus, if the calculated interference signal level from terminal T2 were -145 dBm/Hz, it would have to be reduced. If the modulation type for terminal T2 were e.g., 16 TCM 3/4, the interference level could be reduced by selecting a more robust modulation type, which would have a lower power density at the same range. To be not higher that the maximum -149.5 dBm/Hz the interference signal level must be reduced by 4.5 dB. This could be done by selecting the modulation 8 TCM 2/3, which would reduce the interference level by 6.5 dB (decoupling by modulation type). If it would not be possible to find a more robust modulation that reduces the interference level enough, the terminal would be marked as a problem terminal (step 426) and could, e.g., be allocated a special frequency band, not used in the interfering sector (decoupling by frequency).

[0047] A special problem for the uplink (terminal to base) is that terminals from different sectors may add interference signals and it is difficult to know which terminals contribute (work on the same frequencies). This is typical for the DBA mode. However, it is not likely that more than two terminals will contribute simultaneously. Thus by using a 3 dB margin in the maximum allowed interference level the problem will be taken into account. Moreover, instead of using the figure -149.5 dBm/Hz as the maximum allowed interference signal level, the figure -152.5 dBm/Hz should be used.

[0048] Upon completion of either steps 420 or 424, the bitrate and modulation type for each terminal is be clear. Then, at step 428, when in the FBA mode, a specific frequency and bandwidth is allocated to each link, allowing for appropriate guardbands between the links. The links should basically be packed from narrow to broader channels. It should be understood that step 428 is executed only for the FBA mode. For the DBA mode the allocation of bitrate, modulation type and bandwidth is done momentarily by the control unit 70 in the sector.

[0049] At step 430 it is determined whether a new terminal is to be added to the system. When adding a new terminal

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to the system, steps 432, 434, and 436 are executed. These steps are similar to operations discussed above, in that for the new terminal: (1) a modulation type is determined with regard to range [step 432], (2) the C/I is checked from all base station sectors and the modulation type adjusted if necessary [step 434], and, (3) the interference level is checked in each base station sector from the new terminal and the modulation type is adjusted if necessary to comply with the maximum allowed interference density at the base [step 436]. Network planning processor 210 can continue to operate in a loop awaiting additions of other terminals as shown in Fig. 4B.

[0050] The above-described operations and calculations of Fig. 4A and Fig. 4B are performed by Network planning processor 110 and the results thereof passed to control units 70 of the various base stations. In the DBA mode, for each terminal the highest possible modulation type is specified. It is then up to the control units 70 to decide the actual modulation, bandwidth and frequency to use. The suggested highest possible modulation types are preferably inputted to control units 70 via the network management system 102.

[0051] Thus, the invention concerns a point to multipoint radio access system, comprising a number of sectorized base station sites and a number of subscriber terminals located within the coverage area of the base station sites. The radio links between subscriber terminals and base stations all work within the same frequency band. From sector to sector the base station antennas alternate between vertical and horizontal polarization in a systematic way to minimize the potential interference areas. In accordance with the invention, the links connecting a base station site to the subscriber terminals can be allocated differing capacities and differing modulation schemes selected from a number of choices. Of the modulation schemes, the most robust scheme corresponds to the widest bandwidth needed for a specific bitrate and also to the largest range possible. The least robust modulation scheme corresponds to the most narrow bandwidth needed for a specific bitrate and also the minimum possible range.

[0052] Characteristics of the system and method thus include the following:

(1) the base stations transmit with constant power density for all specific modulation types.

(2) the terminals transmit with constant power density for all bitrates and for all modulation types measured at the range limit of the respective modulation type and decrease the power density with decreasing range to the base station so that the power density received at the base station is constant for all distances for a specific modulation type;

(3) at a given range the transmitted power density from a terminal will differ for different modulation types corresponding to the differences in C/(N+I); and

(4) the individual links to the terminals are designated a modulation type that is consistent with its range to the base station, the C/(N+I) from the various base stations and a maximum allowed interference level received at the base stations which is consistent with the required C/(N+I) and which occupies the least bandwidth.

[0053] Thus, the present invention advantageously provides a simple method to allocate modulation type, power strategy and bandwidth to each radio link in a point to multipoint system including the feature of allowing for various modulation types, considering the required coverage range, the minimum bandwidth requirement and the foreseen interference situation. The operation and allocation of the present invention is without undue consideration of other links, which could easily lead into countless iterations back and force before a satisfactory solution is achieved. The present invention also facilitates a system with dynamic channel allocation.

[0054] While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood, for example, that the polarization scheme for the antennas need not necessarily systematically alternate by sector between vertical and horizontal polarization. Moreover, the radio links can operate in more than one frequency band, e.g., two frequency bands.

Claims

1. A method of allocating radio link characteristics in a point to multipoint radio access system, the point to multipoint radio access system comprising a number of base stations including a selected base station connected by a plurality of radio links to a corresponding plurality of subscriber terminals located within respective coverage areas of the selected base station, at least some of the plurality of radio links being within a same frequency band, **characterized in that** the method comprising:

   for the selected base station (40, B1, B2), selecting a base station transmit power density which, for each of a plurality of modulation types, is constant for all bitrates (400);

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for each of the plurality of subscriber terminals (T1, T2) located within the coverage area of the selected base station, selecting a terminal transmit power density which, for each of the plurality of modulation types, is constant for all bitrates (402);

determining a maximum range for each of the plurality of modulation types (404);

for each of the plurality of subscriber terminals, allocating a modulation type to the corresponding radio link dependent upon range from the selected base station (406);

determining, for each of the plurality of subscriber terminals (T1, T2), whether at the subscriber terminal there is an acceptable signal quality and, if not, allocating a next lower order modulation type to the radio link corresponding to the subscriber terminal which does not have the acceptable signal quality (408, 410, 412); and

determining at the selected base station (40, B1, B2) whether there is an acceptable signal quality with respect to each of the plurality of subscriber terminals and, if not, allocating a next lower order modulation type to the radio link corresponding to the subscriber terminal with respect to which there is not the acceptable signal quality (418, 420, 422).

2. The method of claim 1, further comprising allocating frequencies within the same frequency band and bandwidth to each of the plurality of radio links.

3. The method of claim 1, wherein the acceptable signal quality is indicated by a signal to noise and interference ratio [C/(N+I)].

4. The method of claim 1, wherein for all modulation types there is constant power density for all bitrates measured at range limits of the respective modulation types, wherein the power density decreases with decreasing range to the selected base station (40, B1, B2) whereby the power density received at the selected base station is constant for all distances for a specific modulation type, at a given range the transmitted power density from the selected subscriber terminal (T1, T2) differing for different modulation types in accordance with corresponding differences in the signal quality.

5. The method of claim 1, wherein a most robust modulation type corresponds to a widest bandwidth needed for a specific bitrate and also to a largest range possible, and a least robust modulation type corresponds to a most narrow bandwidth needed for a specific bitrate and also a minimum possible range.

6. The method of claim 1, wherein the base stations are provided with antennas, which systematically alternate by sector between vertical (V) and horizontal (H) polarization to minimize potential interference.

Patentansprüche

1. Verfahren zur Zuweisung von Funkverbindungseigenschaften in einem Punkt-zu-Mehrpunkt-Funkzugangssystem, wobei das Punkt-zu-Mehrpunkt-Funkzugangssystem eine Anzahl von Basisstationen, einschließlich einer gewählten Basisstation, umfaßt, die durch eine Vielzahl von Funkverbindungen mit einer entsprechenden Vielzahl von Teilnehmerendgeräten verbunden sind, die sich in jeweiligen Versorgungsbereichen der gewählten Basisstation befinden, wobei zumindest einige aus der Vielzahl von Funkverbindungen in einem gleichen Frequenzband sind, **dadurch gekennzeichnet, daß** das Verfahren umfaßt:

für die gewählte Basisstation (40, B1, B2), Wählen einer Basisstations-Sendeleistungsdichte, die für jeden aus einer Vielzahl von Modulationstypen bei allen Bitraten (400) konstant ist;
für jedes aus der Vielzahl von Teilnehmerendgeräten (T1, T2), die sich im Versorgungsbereich der gewählten Basisstation befinden, Wählen einer Endgerät-Sendeleistungsdichte, die für jeden aus der Vielzahl von Modulationstypen bei allen Bitraten (402) konstant ist;
Bestimmen einer maximalen Reichweite für jeden aus der Vielzahl von Modulationstypen (404);
für jedes aus der Vielzahl von Teilnehmerendgeräten, Zuweisen eines Modulationstyps der entsprechenden Funkverbindung in Abhängigkeit von der Reichweite der gewählten Basisstation (406);
Bestimmen für jedes aus der Vielzahl von Teilnehmerendgeräten (T1, T2), ob am Teilnehmerendgerät eine annehmbare Signalqualität vorhanden ist, und wenn nicht, Zuweisen eines Modulationstyps der nächstnied-

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rigeren Ordnung an die Funkverbindung entsprechend dem Teilnehmerendgerät, das keine annehmbare Signalqualität hat (408, 410, 412); und
Bestimmen an der gewählten Basisstation (40, B1, B2), ob eine annehmbare Signalqualität vorhanden ist in bezug auf jedes aus der Vielzahl von Teilnehmerendgeräten, und wenn nicht, Zuweisen eines Modulationstyps der nächstniedrigeren Ordnung an die Funkverbindung entsprechend dem Teilnehmerendgerät, bei dem die annehmbare Signalqualität nicht vorhanden ist (418, 420, 422).

2. Verfahren nach Anspruch 1, ferner mit dem folgenden Schritt: Zuweisen von Frequenzen im gleichen Frequenzband und in der gleichen Frequenzbandbreite an jede aus der Vielzahl von Funkverbindungen.

3. Verfahren nach Anspruch 1, wobei die annehmbare Signalqualität durch ein Signal-Rausch und Stör-Verhältnis [C/(N + I)] angegeben wird.

4. Verfahren nach Anspruch 1, wobei für alle Modulationstypen eine konstante Leistungsdichte bei allen Bitraten vorhanden ist, die in den Reichweitegrenzen der jeweiligen Modulationstypen gemessen werden, wobei die Leistungsdichte mit abnehmender Reichweite bis zur gewählten Basisstation (40, B1, B2) abnimmt, wobei die Leistungsdichte, die an der gewählten Basisstation empfangen wird, für alle Entfernungen für einen spezifischen Modulationstyp konstant ist, wobei bei einer gegebenen Reichweite die Sendeleistungsdichte vom gewählten Teilnehmerendgerät (T1, T2) für verschiedene Modulationstypen gemäß entsprechenden Unterschieden der Signalqualität unterschiedlich ist.

5. Verfahren nach Anspruch 1, wobei ein robustester Modulationstyp einer für eine spezifische Bitrate benötigten breitesten Bandbreite und auch einer möglichst größten Reichweite entspricht, und ein am wenigsten robuster Modulationstyp einer für eine spezifische Bitrate benötigten schmalsten Bandbreite und auch einer möglichst geringen Reichweite entspricht.

6. Verfahren nach Anspruch 1, wobei die Basisstationen mit Antennen versehen sind, die systematisch um einen Sektor zwischen einer vertikalen (V) und einer horizontalen (H) Polarisation alternieren, um die potentielle Interferenz zu minimieren.

Revendications

1. Procédé d'allocation de caractéristiques de liaison radio dans un système d'accès radio point à multipoint, le système d'accès radio point à multipoint comprenant un certain nombre de stations de base incluant une station de base sélectionnée qui est connectée au moyen d'une pluralité de liaisons radio à une pluralité correspondante de terminaux d'abonnés qui sont localisés à l'intérieur de zones de couverture respectives de la station de base sélectionnée, au moins certaines de la pluralité de liaisons radio étant à l'intérieur d'une même bande de fréquences, **caractérisé en ce que** le procédé comprend:

pour la station de base sélectionnée (40, B1, B2), la sélection d'une densité de puissance d'émission de station de base qui, pour chacun d'une pluralité de types de modulation, est constante pour tous les débits de bits (400);
pour chacun de la pluralité de terminaux d'abonnés (T1, T2) qui sont localisés à l'intérieur de la zone de couverture de la station de base sélectionnée, la sélection d'une densité de puissance d'émission de terminal qui, pour chacun de la pluralité de types de modulation, est constante pour tous les débits de bits (402);
la détermination d'une plage maximum pour chacun de la pluralité de types de modulation (404);
pour chacun de la pluralité de terminaux d'abonnés, l'allocation d'un type de modulation à la liaison radio correspondante en fonction d'une plage par rapport à la station de base sélectionnée (406);
la détermination, pour chacun de la pluralité de terminaux d'abonnés (T1, T2), de si oui ou non, au niveau du terminal d'abonné, il y a une qualité de signal acceptable et si ce n'est pas le cas, l'allocation d'un type de modulation d'ordre plus faible suivant à la liaison radio correspondant au terminal d'abonné qui ne dispose pas de la qualité de signal acceptable (406, 410, 412); et
la détermination, au niveau de la station de base sélectionnée (40, B1; B2), de si oui ou non il y a une qualité de signal acceptable par rapport à chacun de la pluralité de terminaux d'abonnés et si ce n'est pas le cas, l'allocation d'un type de modulation d'ordre plus faible suivant à la liaison radio correspondant au terminal d'abonné en relation avec lequel il n'y a pas la qualité de signal acceptable (418, 420, 422).

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2. Procédé selon la revendication 1, comprenant en outre l'allocation de fréquences, à l'intérieur de la même bande de fréquences et de la même largeur de bande, à chacune de la pluralité de liaisons radio.

3. Procédé selon la revendication 1, dans lequel la qualité de signal acceptable est indiquée au moyen d'un rapport signal sur bruit et interférence [C/(N + I)].

4. Procédé selon la revendication 1, dans lequel, pour tous les types de modulation, il y a une densité de puissance constante pour tous les débits de bits mesurés pour des limites de plage des types de modulation respectifs, dans lequel la densité de puissance diminue avec une plage décroissante sur la station de base sélectionnée (40, B1, B2) et ainsi, la densité de puissance qui est reçue au niveau de la station de base sélectionnée est constante pour toutes les distances pour un type de modulation spécifique, et pour une plage donnée, la densité de puissance émise depuis le terminal d'abonné sélectionné (T1, T2) différant pour différents types de modulation conformément à des différences correspondantes au niveau de la qualité de signal.

5. Procédé selon la revendication 1, dans lequel un type de modulation le plus robuste correspond à une largeur de bande la plus large nécessaire pour un débit de bits spécifique et également à une plage possible la plus grande et un type de modulation le moins robuste correspond à une largeur de bande la plus étroite nécessaire pour un débit de bits spécifique et également une plage possible minimum.

6. Procédé selon la revendication 1, dans lequel les stations de base sont munies d'antennes qui sont en alternance de façon systématique, au moyen d'un secteur entre les polarisations verticale (V) et horizontale (H) afin de minimiser une interférence potentielle.

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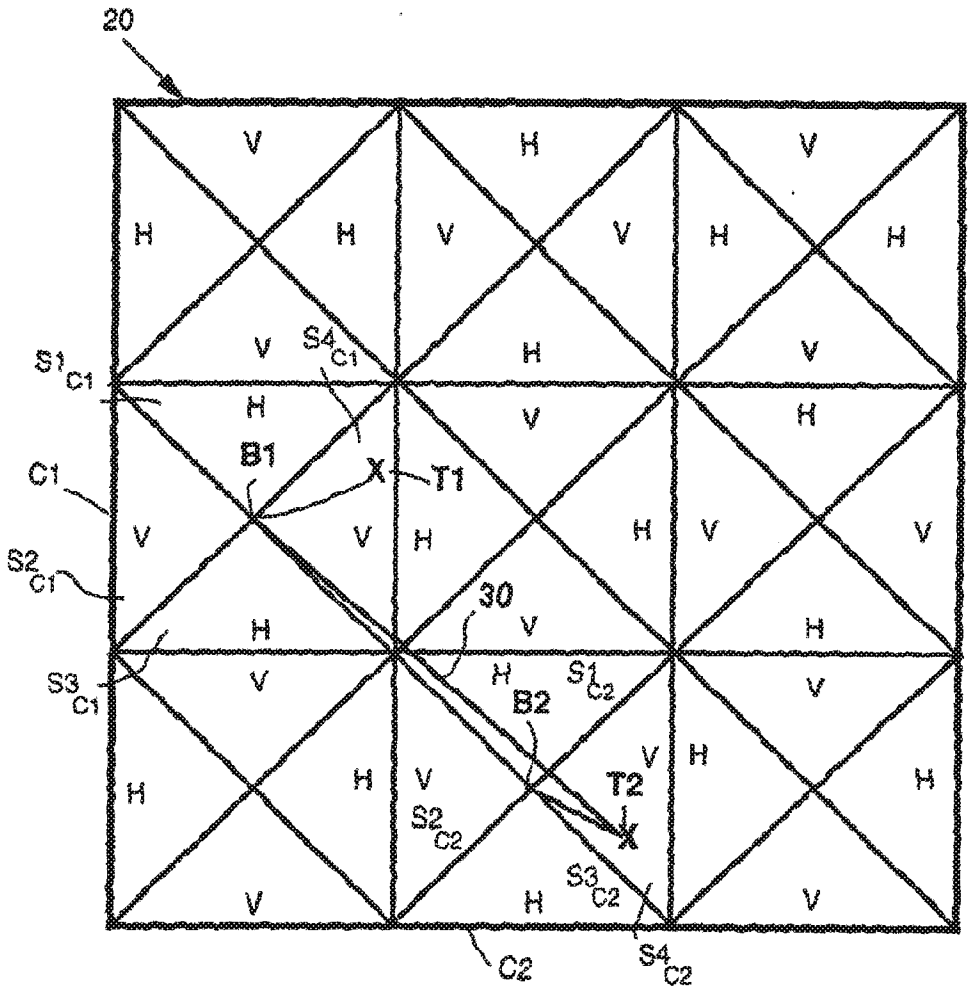
Fig. 1 Microwave coverage network



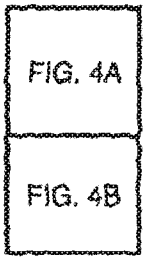


Fig. 4

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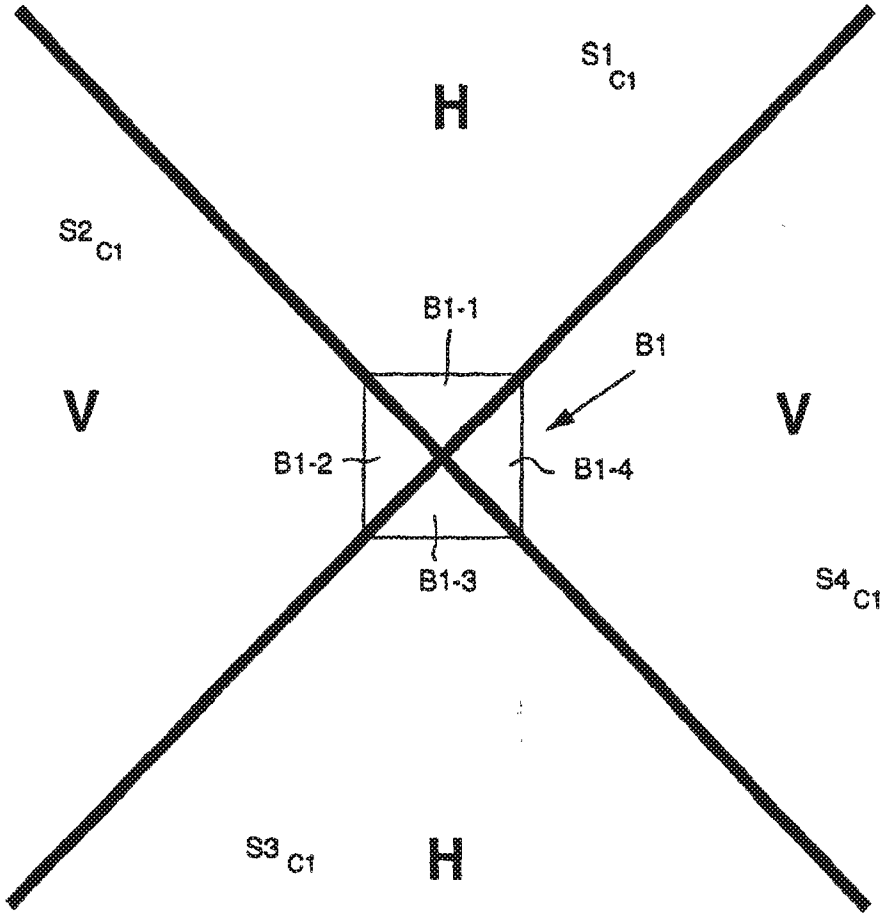
Fig. 1A



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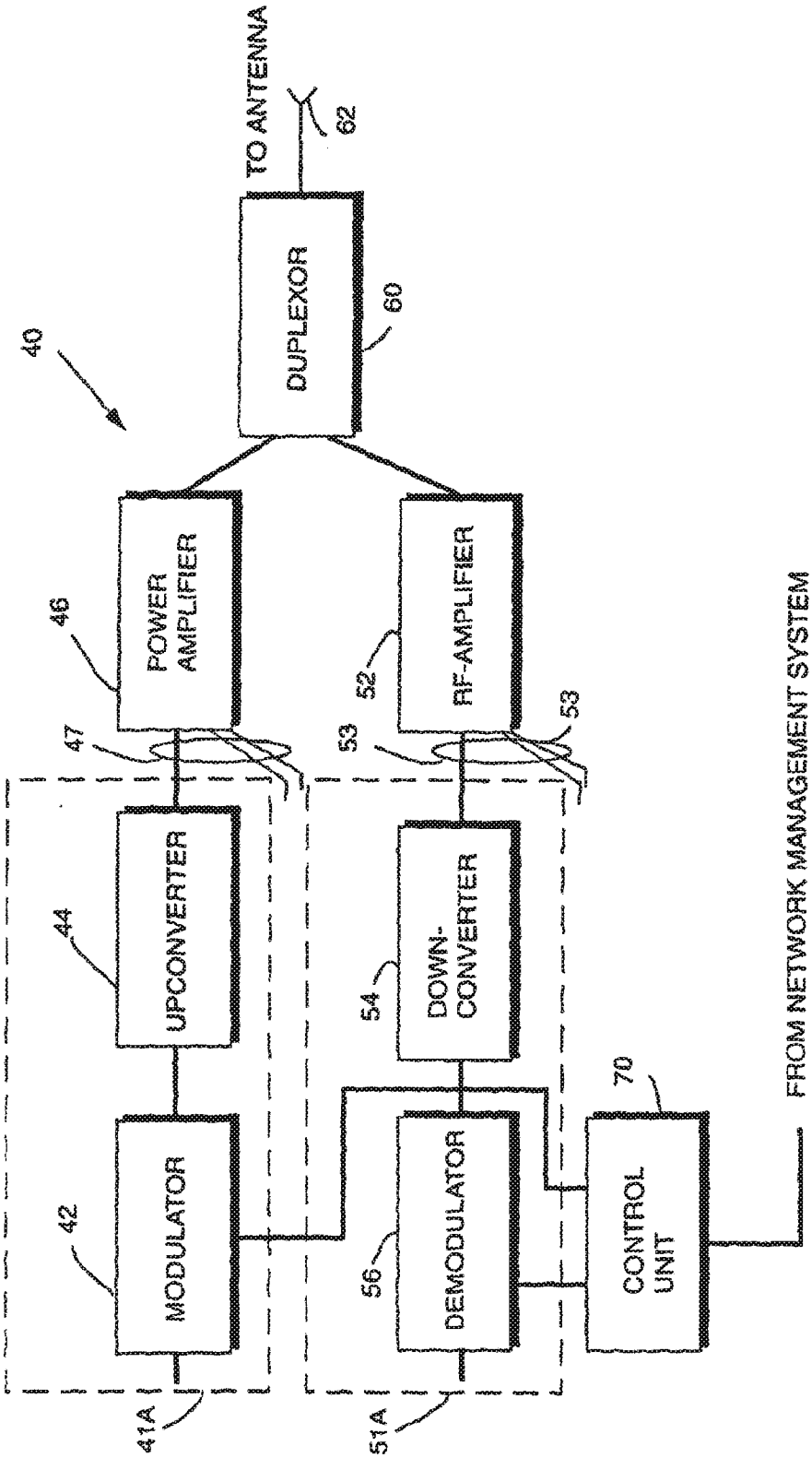

Fig. 2 Basic base station block diagram

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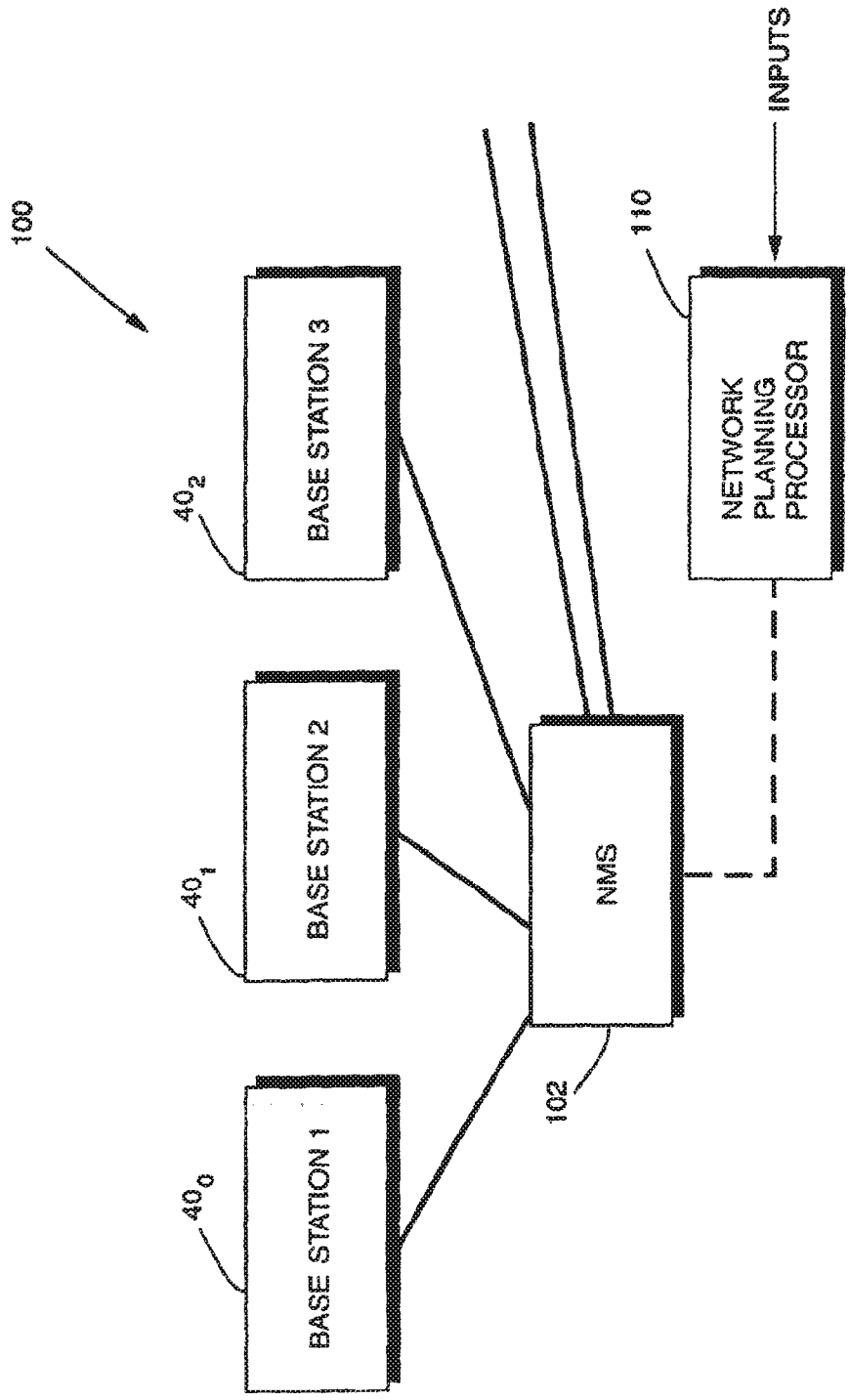

Fig. 3 Basic base station network

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Fig. 4A

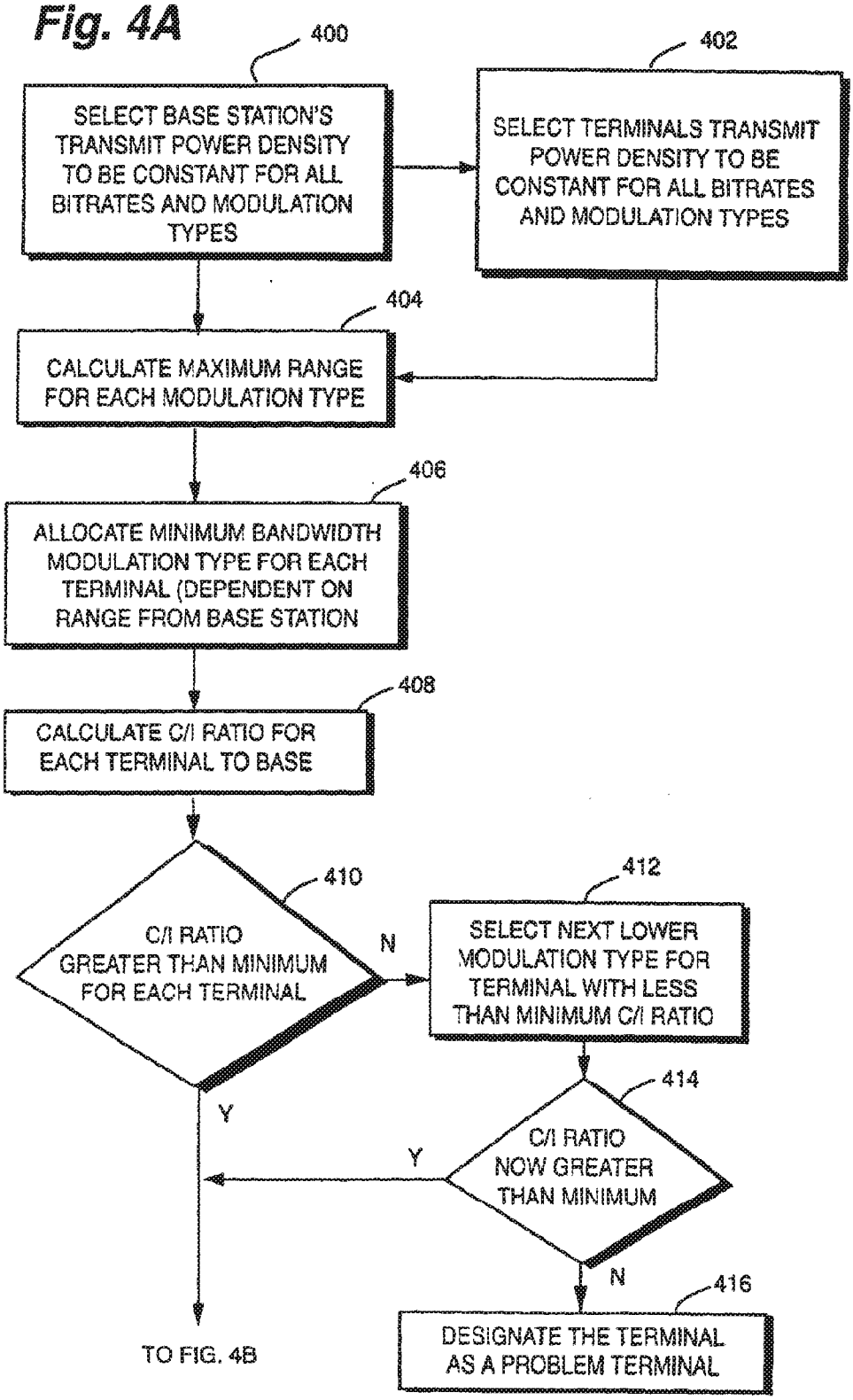

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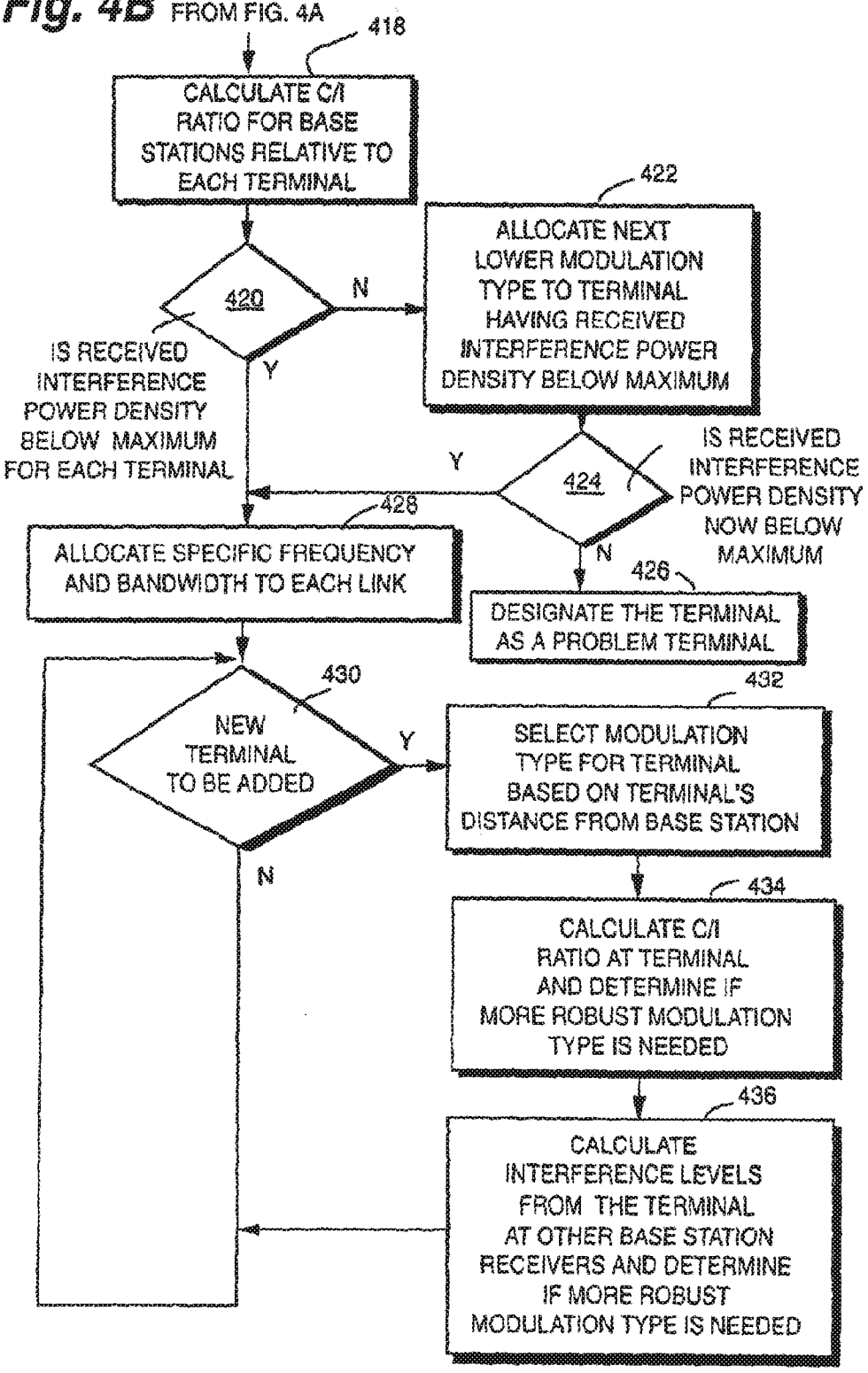
Fig. 4B FROM FIG. 4A



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Modulation à multirésolution

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Beschreibung

Stand der Technik

[0001] Die Erfindung geht aus von einem Verfahren zur Vergrößerung der mit einem Multiträger-Übertragungsverfahren über Rundfunk übertragenen Datenrate, sowie einem Sender und einem Empfänger, insbesondere stationäre Geräte, nach der Gattung der unabhängigen Ansprüche.

Aus dem Stand der Technik ist die Übertragung von digitalen Daten nach dem ETS 300 401 bekannt, der entwickelt wurde um den mobilen Multimediaempfang über terrestrische, digitale Rundfunksysteme zu standardisieren. Dieser zunächst für den Hörfunk konzipierte Standard DAB (Digital Audio Broadcasting) eignet sich auch für die mobile Fernsehübertragung. Beim DAB-Verfahren bietet sich die Möglichkeit, die gesamte Bandbreite von 1,5 MHz für die Datenübertragung von Videodaten zur Verfügung zu stellen. So können Daten mit einer maximalen Datenrate von ungefähr 1,8 Mbit/s zum mobilen Empfänger übertragen werden. Diese Datenrate erlaubt unter Einsatz bisheriger Kompressionsverfahren (MPEG) eine gute Qualität auf Bildschirmen, wie sie bei mobilen Geräten eingesetzt werden. Da ein über DAB ausgestrahltes Fernsehprogramm auch stationär empfangen werden kann, können bei den wesentlich größeren Bildschirmdiagonalen, Kodierungseffekte, Unschärfe oder Blockbildung sichtbar werden. Für eine Darstellung auf größeren Bildschirmen ist eine größere Datenübertragungsrate notwendig. Aus "X-DAB - Eine abwärtskompatible Erweiterung des DAB-Standards für Multimediaanwendungen", Kleinheubacher Berichte, 1996, G. Zimmermann u. H. Schulze, ist eine Erweiterung des DAB-Verfahrens bekannt, wobei ein kodiertes 8-PSK-(Phase Shift Keying) Verfahren als Modulationsverfahren angewendet wird. Diese Erweiterung das sogenannte X-DAB bietet die Möglichkeit, die mobil zu empfangenden Datenraten um 20 % zu erhöhen. Das Modulationsverfahren macht es allerdings für bisher konventionelle DAB-Empfänger unmöglich, die Signale zu empfangen.

[0002] Aus EP 616 454 A1 ist ein digitales Übertragungsverfahren bekannt, das eine sogenannte Multi-Resolution-Modulation ermöglicht. Dabei können Daten mit unterschiedlichen Modulationsverfahren moduliert werden. Aus K. Ramchandran et al.: Multiresolution Broadcast for Digital HDTV Using Joint Source/Channel Coding, IEEE Journal on Selected Areas in Communications, New York, US, Vol. 11 Nr. 1, Seiten 6 bis 22 ist ebenfalls die Verwendung der Multi-Resolution-Modulation für die Übertragung von digitalen HDTV-Signalen bekannt. Auch R. Kays: Kanalcodierung und Modulation für die digitale Fernsehübertragung, Fernseh- und Kinotechnik, VDE Verlag, Berlin, Vol. 48, Nr. 3, Seiten 109 bis 114 zeigt die Verwendung einer hierarchischen Übertragung eines HDTV-Programms in einem 8 MHz-Kanal. Dabei wird eine Multi-Resolution-QAM verwendet. Aus K. Pazel et al.: A Concept of Digital Tewestrial Television Broadcasting, Wireless Personal Communications Kluwer, Vol. 2, Nr. 1 bis 2, Seiten 9 bis 27 ist es bekannt, HDTV-Signale in drei Stufen mit unterschiedlichen Codierungen bereitzustellen, um eine "graceful degradation" empfängerseitig zu ermöglichen. Damit liegt das gleiche Signal verschieden aufgelöst vor. Es können dabei Modulationsverfahren wie QPSK und QAM verwendet werden. Dies ermöglicht insbesondere Empfang durch stationäre und mobile Empfänger mit angepassten Empfangsqualitäten.

Vorteile der Erfindung

[0003] Das erfindungsgemäße Verfahren mit den kennzeichnenden Merkmalen des Hauptanspruchs 1 hat demgegenüber den Vorteil, die übertragene Datenrate zu erhöhen, indem zwei Datenströme getrennt voneinander moduliert und anschließend vor der Übertragung kombiniert werden. Mit der zusätzlichen Modulation lassen sich die Datenraten stark steigern. Durch das erfindungsgemäße Verfahren ist es möglich, daß ein Empfänger, der nur Daten, die mit einem ersten Modulationsverfahren moduliert werden, empfangen kann, die Daten problemlos empfängt, während ein weiterer, z. B. stationärer Empfänger die Daten, die mit dem zweiten Modulationsverfahren moduliert werden, zusätzlich verarbeiten kann. Dadurch wird das Übertragungsverfahren an die im Augenblick gegebenen Modulationsverfahren angepaßt, während es gleichzeitig zusätzliche Informationen für verbesserten Empfang liefert.

[0004] Durch die in den Unteransprüchen aufgeführten Maßnahmen ist eine vorteilhafte Weiterbildung und Verbesserung des im unabhängigen Anspruch angegebenen Verfahrens möglich. Besonders vorteilhaft ist es, wenn die Daten des zweiten Teildatenstroms mit einer Amplituden-Modulation oder anderen alternativen Modulationsverfahren moduliert werden.

[0005] Vorteilhaft ist es weiterhin, daß die Daten des ersten Teildatenstroms einer DQPSK-Modulation (Differential Quadrature Phase Shift Keying) unterzogen werden. Dadurch ist es für konventionelle Empfänger des DAB-Verfahrens möglich die Daten des ersten Teildatenstroms zu empfangen.

[0006] Vorteilhafter Weise enthalten die Daten des ersten Teildatenstroms alle notwendigen Informationen, um z. B. ein Fernsehbild in einem mobilen Empfänger darzustellen. Der zweite Teildatenstrom enthält zusätzliche Informationen, die zu einer besseren Bildqualität in einem stationären Empfänger verarbeitet werden können.

[0007] Der erfindungsgemäße Sender zur Vergrößerung der übertragenen Datenrate mit den kennzeichnenden Merkmalen des unabhängigen Anspruchs 6 hat den Vorteil, daß er zusätzlich zu den Bauteilen, die ein Sender für das DAB-Verfahren aufweisen muß, einen weiteren Modulator für den zweiten Teildatenstrom enthält. Zusätzlich ist ein Kombinierer für die mit den un-

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terschiedlichen Modulationsverfahren modulierten Teildatenströme vorhanden.

[0008] Vorteilhafter Weise ist der zweite Modulator ein Amplitudenmodulator oder ein äquivalenter Modulator.

[0009] Der erfindungsgemäße Empfänger zum Empfang von digitalen Daten mit den kennzeichnenden Merkmalen des unabhängigen Anspruchs 8 hat den Vorteil, daß er einen Abzweig für einen zweiten Teildatenstrom aufweist, in dem ein zweiter Demodulator vorhanden ist. Vorteilhafter Weise enthält der Empfänger einen Decoder, der die Teildatenströme zusammenführen kann.

Zeichnung

[0010] Ein Ausführungsbeispiel der Erfindung ist in der Zeichnung dargestellt und in der nachfolgenden Beschreibung näher erläutert. Es zeigt Figur 1 einen erfindungsgemäßen Sender, Figur 2 einen erfindungsgemäßen Empfänger und Figur 3 eine Darstellung des erfindungsgemäßen Modulationsverfahrens.

Beschreibung des Ausführungsbeispiels

[0011] Figur 1 zeigt das Schaltungsschema für einen erfindungsgemäßen Sender. Auf der linken Seite erkennt man die verschiedenen Datenquellen bestehend aus den Videodaten 1, den Audiodaten 2, allgemeinen Daten 3 und Paketdaten 4. Video-, Audio- und sonstige Daten werden in einen MPEG-Enkoder 5 eingespeist, der die Daten in zwei Teilströme kodiert. Der erste Teilstrom 7 durchläuft einen DVB-Enkoder 8 und einen DAB-Enkoder 9. Der zweite Datenstrom 6 wird ebenfalls über den DVB-Enkoder 8 und den DAB-Enkoder geführt. Weitere Audiodaten 2 werden über einen Audioenkoder 10, den DAB-Enkoder 9 zu einem DAB-Multiplexer 12 geführt. Die Paketdaten 4 durchlaufen einen Paketmultiplexer 11, den DAB-Enkoder 9 und den DAB-Multiplexer 12. Alle Daten des ersten Teildatenstroms 40 durchlaufen eine DQPSK-Modulation 13. Der zweite Datenstrom 41 durchläuft einen Amplitudenmodulator 14 und wird in einem Kombinierer 15 mit dem Datenstrom 40 zusammengeführt. Die resultierenden Daten 42 durchlaufen einen OFDM-Generator 16 und werden über eine Antenne 17 abgestrahlt.

[0012] Das analoge Fernsehsignal liegt zunächst als Kombination aus Videodaten 1, Audiodaten 2, sowie anderen Daten 3 vor. Dieses Signal wird im MPEG-Enkoder 5 komprimiert. Das komprimierte Videosignal besteht dabei aus zwei Teildatenströmen: Dem Low-Definition-Teildatenstrom 7 für eine Basis-Bildqualität, sowie den Standarddefinition-Teildatenstrom 6, der zusammen mit dem Low-Definition-Datenstrom 7 eine verbesserte Bildqualität für einen stationären Empfänger ermöglicht. Die Datenrate der Teildatenströme richtet sich nach der möglichen Übertragungskapazität der Teilkanäle. Der Teildatenstrom 40, der für den mobilen Empfang gedacht ist, hat eine maximale Nutzdatenrate von etwa 1,8 MBit/s. Der zweite Teildatenstrom 6 für den stationären Empfänger, der zusammen mit dem für mobile Teilnehmer gesendeten Teildatenstrom 7 eine verbesserte Bildqualität auf einem großen Bildschirm ermöglicht, beträgt je nach verwendeter Kanalcodierung ebenfalls ca. 1,8 MBit/s. Beide Übertragungskanäle haben eine maximale Kapazität von ca. 2,3 MBit/s. Der für den mobilen Empfänger bestimmten Teildatenstrom 7, sowie der zusätzliche Teildatenstrom 6 werden wie bisher im DAB-Sender mit einem äußeren Fehlerschutz versehen. Dazu durchlaufen die Daten den DVB-Enkoder 8, der in mehreren Schritten den Fehlerschutz beaufschlagt, durch DVB-Energy-Dispersal, äußeren Reed-Solomon-Code und äußeren Faltungsinterleaver. Es folgen für beide Teildatenströme die im DAB-Verfahren vorgesehenen Schritte für die Übertragung im Stream-Mode. Die Daten durchlaufen den DAB-Enkoder 9 der die Schritte DAB-Energy-Dispersal, DAB-Faltungscoding und DAB-Faltungsinterleaver enthält. Im folgenden DAB-Multiplexer 12 werden die Daten des Teildatenstroms 7 mit evtl. vorhandenen zusätzlichen Audiodaten 2 oder Paketdaten 4 gemischt, und aus der Gesamtheit der Daten der DAB-Übertragungsrahmen gebildet. Der erste Datenstrom 40 durchläuft einen DQPSK (Differential Quadrature Phase Shift Keying) -Modulator mit vorgeschaltetem Frequenzinterleaving. Der für den stationären Empfänger bestimmte Datenstrom 6 durchläuft den gleichen äußeren Fehlerschutz wie der erste Datenstrom 7 sowie die DAB-Kodierung. Im folgenden Amplitudenmodulator 14 werden die eingehenden Bits mit einem bestimmten Modulationsverfahren kodiert. Der darauffolgende Kombinierer 15 kombiniert die Datenströme 41 und 40 mit den unterschiedlichen Modulationsverfahren zu einem resultierenden Datenstrom 42, der nach der OFDM-Modulation über die Antenne 17 gesendet wird.

Figur 3 zeigt die Darstellung des Modulationsverfahrens an drei Beispielen. Aufgetragen ist in Figur 3a bis 3c der komplexe Phasenraum. Im komplexen Phasenraum sind die DQPSK-Symbole 34 dargestellt. Im Beispiel Figur 3a wird dem zweiten Datenstrom 41 durch eine Amplitudenmodulation eines von vier möglichen Symbolen, die als Punkte ausgeführt sind, zugeordnet. Die Zuordnung entspricht in diesem Beispiel einer Gray-Kodierung, d. h. um Doppelfehler bei falscher Detektion zu vermeiden wird so durchnumeriert, daß wenn man bei der Detektion um ein Symbol danebenliegt, in jedem Fall ein Bit korrekt empfangen wird. Im Kombinierer 15 werden die DQPSK-Symbole 34 mit den entsprechend zugewiesenen Amplituden des Modulators 14 beaufschlagt. Die daraus resultierenden Signalpunkte sind in Figur 3a dargestellt. Der relative Abstand der Signalpunkte zueinander, der durch die Amplitude des Signals bestimmt ist, beeinflußt die Empfangseigenschaften sowohl vom mobilen als auch stationären Empfänger. So bedeutet eine enge Lage der vier amplitudenmodulierten Signalpunkte zueinander keine oder eine sehr ge-

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ringe Verschlechterung der mobilen Empfangseigenschaften auf Kosten der stationären Empfangseigenschaften, da ein größerer Signal-Störungsabstand benötigt wird. Dagegen lassen sich bei zunehmendem Abstand der Signalpunkte zueinander, d. h. bei größeren Amplituden, die Empfangseigenschaften vom mobilen und stationären Empfänger gegeneinander abwägen. Dies ermöglicht eine große Flexibilität des Übertragungsverfahrens in Bezug auf gewünschte oder vorgegebene Empfangseigenschaften. Alternativ zu der Amplitudenmodulation aus Figur 3a ist in Figur 3b eine Quadratureamplitudenmodulation in Verbindung mit der DQPSK-Modulation dargestellt. In Figur 3 c wird die Möglichkeit einer Phasenshiftmodulation in Kombination mit der DQPSK-Modulation gezeigt. Alle Modulationskombinationen haben die Eigenschaft, daß die Signalpunkte innerhalb der DQPSK-Symbole liegen. Das bedeutet, daß ein Standard DAB-Empfänger die Signale, innerhalb der von den Symbolen vorgegebenen Rahmen empfangen kann. Das bedeutet auch daß ein normaler DAB-Empänger von der zusätzlichen Modulation nicht beeinflußt wird.

[0013] Figur 2 stellt das Schaltschema eines erfindungsgemäßen Empfängers dar. Eingangsseitig ist die Antenne 17 mit dem A/D-Wandler 18 und der Synchronisierung 19 verbunden. Anschließend ist ein schneller Fouriertransformator 20, und ein DQPSK-Demodulator 21 einem DAB-Multiplexer 22 vorgeschaltet. Der DAB-Demultiplexer 22 ist über einen DAB-Decoder 24 sowie einem Audio-Decoder 27 mit der Audiosenke 30 und über einen Paketdemultiplexer 28 mit der Paketdatensenke 29 verbunden. Videodaten werden in einem DVB-Decoder 25 in einem MPEG-Decoder 26 eingespeist, von wo aus sie mit den Audiosenken 30, mobilen Videosenken 32, stationären Videosenken 33, sowie weiteren Datensenken 31 verbunden sind. Nach dem DQPSK-Demodulator 21 zweigt ein Signalzweig zu einem Amplituden-Demodulator 23 ab. Dieser ist über einen DAB-Decoder 24 mit einem DVB-Decoder 25 und dem MPEG-Decoder 26 verbunden.

[0014] Über die Antenne 17 wird das OFDM-Symbol empfangen und im A/D-Wandler 18 einer Analog-Digitalwandlung unterzogen. Anschließend erfolgt die Zeit-, Frequenz- und Phasensynchronisation im Synchronisierer 19. Das Datensignal wird von der schnellen Fourier-Transformation 20 zerlegt und im DQPSK-Demodulator 21 demoduliert. Nach dem Demodulator 21 folgen für den mobilen Empfänger die Verarbeitungsschritte wie bei einer konventionellen Videoübertragung. Der stationäre Empfänger verwendet für den Demodulator 23 eine Amplitudenschätzung aus dem Phasenreferenzsymbol nach der Synchronisierung 19, um die Amplitudendemodulation durchzuführen. Hier werden aus der Amplitude des komplexen DQPSK-Symbols die zwei fehlenden Codebits gewonnen. Es folgt die DAB-konforme Kanalkodierung im Decoder 24 und die DVB-konforme äußere Kanaldecodierung. Der Quelldecoder der MPEG-Decoder 26 stellt dem mobilen Empfänger den Low-Definition Teilstrom 7 für das Videosignal zur Verfügung. Zudem erhält er die zugehörigen Audioinformationen und evtl. gesendete Daten. Ein stationärer Empfänger kann mit Hilfe des zusätzlichen Datenstroms 6, Zusatzanteil für Standarddefinition, und eines hierarchischen MPEG-Decoders ein verbessertes Fernsehbild darstellen.

[0015] Bei dem erfindungsgemäßen Verfahren wird die volle Kompatibilität mit der bisherigen mobilen Fernsehübertragung über das DAB-Verfahren möglich. Das heißt DAB-Geräte für den mobilen Fernsehempfang können sowohl eine einstufige Standarddefinition als auch die erste Stufe eines hierarchischen Low-Definition/Standarddefinition-Fernsehsignals empfangen und wiedergeben. Es ist wesentlich einfacher mobile Endgeräte zur Videoübertragung für die Bandbreite von 1,5 MHz zu realisieren, als Systeme, die eine größere Bandbreite erforderlich machen. Durch die große Flexibilität der Wahl der Lage der amplitudenmodulierten Signalpunkte im Hinblick auf gewünschte bzw. geforderte Empfangseigenschaften der mobilen und der stationären Empfänger sind bessere Realisierungen möglich.

Patentansprüche

1. Verfahren zur Vergrößerung der mit einem Multiträgerübertragungsverfahren über Rundfunk übertragenen Datenrate, insbesondere für stationären Empfang, wobei digitale Daten in zwei Datenströme geteilt werden und ein erster Teildatenstrom (40) mit einem ersten Modulationsverfahren (13) moduliert wird, wobei ein zweiter Teildatenstrom (41) mit einem zweiten Modulationsverfahren (14) moduliert wird und wobei beide Teildatenströme vor der Übertragung kombiniert werden, **dadurch gekennzeichnet, dass** beide Teildatenströme (6, 7) zuerst einen DVB-Encoder (8) und dann einen DAB-Encoder (9) zur Bildung eines DAB-Übertragungsrahmens durchlaufen.

2. Verfahren zur Vergrößerung der übertragenen Datenrate über Rundfunk nach Anspruch 1, **dadurch gekennzeichnet, dass** die Daten des zweiten Teildatenstroms (41) einer Amplitudenmodulation oder einer Quadraturamplitudenmodulation oder einer Phase Shift Keying-Modulation unterzogen werden.

3. Verfahren zur Vergrößerung der übertragenen Datenrate über Rundfunk nach Anspruch 1 oder 2, **dadurch gekennzeichnet, dass** die Daten des ersten Teildatenstroms (40) einer DQPSK-Modulation unterzogen werden.

4. Verfahren zur Vergrößerung der übertragenen Datenrate über Rundfunk nach Anspruch 1 bis 3, **dadurch gekennzeichnet, dass** der zweite Teildaten-

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strom (41) zusätzliche Informationen zum ersten Teildatenstrom (40) enthält.

5. Verfahren zur Vergrößerung der übertragenen Datenrate über Rundfunk nach Anspruch 1 bis 4, **dadurch gekennzeichnet, dass** die digitalen Daten Fernsehbilder enthalten und im ersten Teildatenstrom (40) Daten für das Basisbild und im zweiten Teildatenstrom (41) Daten für ein Standardbild übertragen werden.

6. Sender zur Vergrößerung der übertragenen Datenrate über Rundfunk, wobei der Sender zur Verarbeitung der Audio- (2), Video- (1) und sonstigen Daten (3, 4), Encoder (5, 8, 9, 10), einen Multiplexer (12) sowie einen ersten Modulator (13) aufweist, wobei ein erster Encoder (5) einen ersten und zweiten Teildatenstrom erzeugt und ein zweiter Modulator (14) für den zweiten Teildatenstrom (41) und ein Kombinierer (15) für den ersten und zweiten Teildatenstrom vorhanden ist, **dadurch gekennzeichnet, dass** für beide Teildatenströme (6, 7) für die Codierung zuerst ein DVB-Encoder (8) und dann ein DAB-Encoder (9) vorhanden sind, wobei der Sender derart konfiguriert ist, dass er einen DAB-Übertragungsrahmen bildet.

7. Sender zur Vergrößerung der übertragenen Datenrate über Rundfunk nach Anspruch 6, **dadurch gekennzeichnet, dass** der zweite Modulator ein Amplitudenmodulator oder ein Quadraturamplitudenmodulator oder ein Phase Shift Keying-Modulator ist.

8. Empfänger zum Empfang von digitalen Daten über Rundfunk, wobei der Empfänger einen A/D-Wandler (18), ein Synchronisationsbauteil (19), eine FFT (20), einen ersten Demodulator (21), sowie Demultiplexer (22), Decoder (25, 24, 26, 27, 28) mit Anschlüssen zu den jeweiligen Datensenken (29, 30, 31, 32, 33) aufweist, wobei nach dem ersten Demodulator (21) ein Abzweig für einen zweiten Teildatenstrom (41) in einen zweiten Demodulator (23) vorhanden ist und wobei ein Decoder (26) die Teildatenströme zusammenführt, **dadurch gekennzeichnet, dass** für beide Teildatenströme ein DAB- und ein DVB-Decoder (24, 25) vorgesehen sind, wobei die Teildatenströme zuerst den DAB- und dann den DVB-Decoder (24, 25) durchlaufen.

9. Empfänger von digitalen Daten über Rundfunk nach Anspruch 8, **dadurch gekennzeichnet, dass** der zweite Demodulator (23) ein Amplitudendemodulator oder ein Quadraturamplitudendemodulator oder ein Phase Shift Keying-Demodulator ist.

Claims

1. Method for increasing the data rate transmitted by broadcast radio using a multicarrier transmission method, particularly for stationary reception, where digital data are divided into two datastreams, and a first subsidiary datastream (40) is modulated using a first modulation method (13), with a second subsidiary datastream (41) being modulated with a second modulating method (14), and where the two subsidiary datastreams are combined before transmission, **characterized in that** the two subsidiary datastreams (6, 7) first pass through a DVB encoder (8) and then through a DAB encoder (9) in order to form a DAB transmission frame.

2. Method for increasing the transmitted data rate by broadcast radio according to Claim 1, **characterized in that** the data in the second subsidiary datastream (41) are subjected to amplitude modulation or to quadrature amplitude modulation or to phase shift keying modulation.

3. Method for increasing the transmitted data rate by broadcast radio according to Claim 1 or 2, **characterized in that** the data in the first subsidiary datastream (40) are subjected to DQPSK modulation.

4. Method for increasing the transmitted data rate by broadcast radio according to Claim 1 to 3, **characterized in that** the second subsidiary datastream (41) contains additional information relating to the first subsidiary datastream (40).

5. Method for increasing the transmitted data rate by broadcast radio according to Claim 1 to 4, **characterized in that** the digital data contain television pictures, and the first subsidiary datastream (40) is used to transmit data for the base picture, and the second subsidiary datastream (41) is used to transmit data for a standard picture.

6. Transmitter for increasing the transmitted data rate by broadcast radio, where the transmitter has encoders (5, 8, 9, 10), a multiplexer (12) and a first modulator (13) in order to process the audio (2), video (1) and other data (3, 4), where a first encoder (5) produces a first and a second subsidiary datastream, and a second modulator (14) for the second subsidiary datastream (41) and a combiner (15) for the first and the second subsidiary datastream are provided, **characterized in that** first a DVB encoder (8) and then a DAB encoder (9) are provided for the coding for the two datastreams (6, 7), with the transmitter being configured such that it forms a DAB transmission frame.

7. Transmitter for increasing the transmitted data rate

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by broadcast radio according to Claim 6, **characterized in that** the second modulator is an amplitude modulator or a quadrature amplitude modulator or a phase shift keying modulator.

8. Receiver for receiving digital data by broadcast radio, where the receiver has an A/D converter (18), a synchronization component (19), an FFT (20), a first demodulator (21), and also a demultiplexer (22), decoders (25, 24, 26, 27, 28) with connections to the respective data sinks (29, 30, 31, 32, 33), where a branch for a second subsidiary datastream (41) into a second demodulator (23) is provided downstream of the first demodulator (21), and where a decoder (26) combines the subsidiary datastreams, **characterized in that** a DAB decoder and a DVB decoder (24, 25) are provided for the two subsidiary datastreams, with the subsidiary datastreams first passing through the DAB decoder and then through the DVB decoder (24, 25).

9. Receiver for digital data by broadcast radio according to Claim 8, **characterized in that** the second demodulator (23) is an amplitude demodulator or a quadrature amplitude demodulator or a phase shift keying demodulator.

Revendications

1. Procédé pour augmenter le débit de données transmises par radiodiffusion avec un procédé de transmission multiporteuse, en particulier pour la réception fixe, selon lequel des données numériques sont divisées en deux flux de données, un premier flux de données (40) est modulé avec un premier procédé de modulation (13), un deuxième flux de données (41) est modulé avec un deuxième procédé de modulation (14), les deux flux de données étant combinés avant la transmission,
caractérisé en ce que
les deux flux de données (6, 7) traversent tout d'abord un encodeur DVB (8) puis un encodeur DAB (9) pour former un cadre de transmission DAB.

2. Procédé pour augmenter le débit de données transmises par radiodiffusion selon la revendication 1,
caractérisé en ce que
les données du deuxième flux partiel de données (41) sont soumises à une modulation d'amplitude ou une modulation d'amplitude en quadrature ou à une modulation Phase Shift Keying.

3. Procédé pour augmenter le débit de données transmises par radiodiffusion selon la revendication 1 ou 2,
caractérisé en ce que
les données du premier flux partiel de données (40) sont soumises à une modulation DQPSK.

4. Procédé pour augmenter le débit de données transmises par radiodiffusion selon la revendication 1 à 3,
caractérisé en ce que
le deuxième flux partiel de données (41) contient des informations en supplément du premier flux partiel de données (40).

5. Procédé pour augmenter le débit de données transmises par radiodiffusion selon la revendication 1 à 4,
caractérisé en ce que
les données numériques contiennent des images de télévision et des données pour l'image de base sont transmises dans le premier flux partiel de données (40) et des données pour une image standard sont transmises dans le deuxième flux partiel de données (41).

6. Emetteur destiné à augmenter le débit de données transmises par radiodiffusion, dans lequel l'émetteur présente, pour le traitement des données audio (2), vidéo (1) et autres (3, 4), des encodeurs (5, 8, 9, 10), un multiplexeur (12) ainsi qu'un premier modulateur (13), avec un premier encodeur (5) produisant un premier et un deuxième flux partiels de données, un deuxième modulateur (14) pour le deuxième flux partiel de données (41) et un combinateur (15) pour le premier et le deuxième flux partiel de données,
caractérisé en ce que
pour les deux flux partiels de données (6, 7), tout d'abord un encodeur DVB (8) et ensuite un encodeur DAB (9) sont présents pour le codage, l'émetteur étant configuré de manière qu'il forme un cadre de transmission DAB.

7. Emetteur destiné à augmenter le débit de données transmises par radiodiffusion selon la revendication 6,
caractérisé en ce que
le deuxième modulateur est un modulateur d'amplitude ou un modulateur d'amplitude en quadrature ou un Phase Shift Keying Modulator.

8. Récepteur destiné à recevoir des données numériques par radiodiffusion, dans lequel le récepteur présente un convertisseur A/N (18), un composant de synchronisation (19), un FFT (20), un premier démodulateur (21), ainsi que des multiplexeurs (22), des décodeurs (25, 24, 26, 27, 28) munis de connexions qui aboutissent aux drains de données correspondants (29, 30, 31, 32, 33), dans lequel, en aval du premier démodulateur (21) une branche dérivée pour un deuxième flux partiel de données (41) est présente dans un deuxième démodulateur (23),

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et dans lequel un décodeur (26) réunit les flux partiels de données,
caractérisé en ce que
pour les deux flux partiels de données, sont prévus un décodeur DAB et un décodeur DVB (24, 25), les flux partiels de données traversant tout d'abord le décodeur DAB puis le décodeur DVB (24, 25).

9. Récepteur de données numériques par radiodiffusion selon la revendication 8,
caractérisé en ce que
le deuxième démodulateur (23) est un démodulateur d'amplitude ou un démodulateur d'amplitude en quadrature ou un Phase Shift Keying Demodulator.

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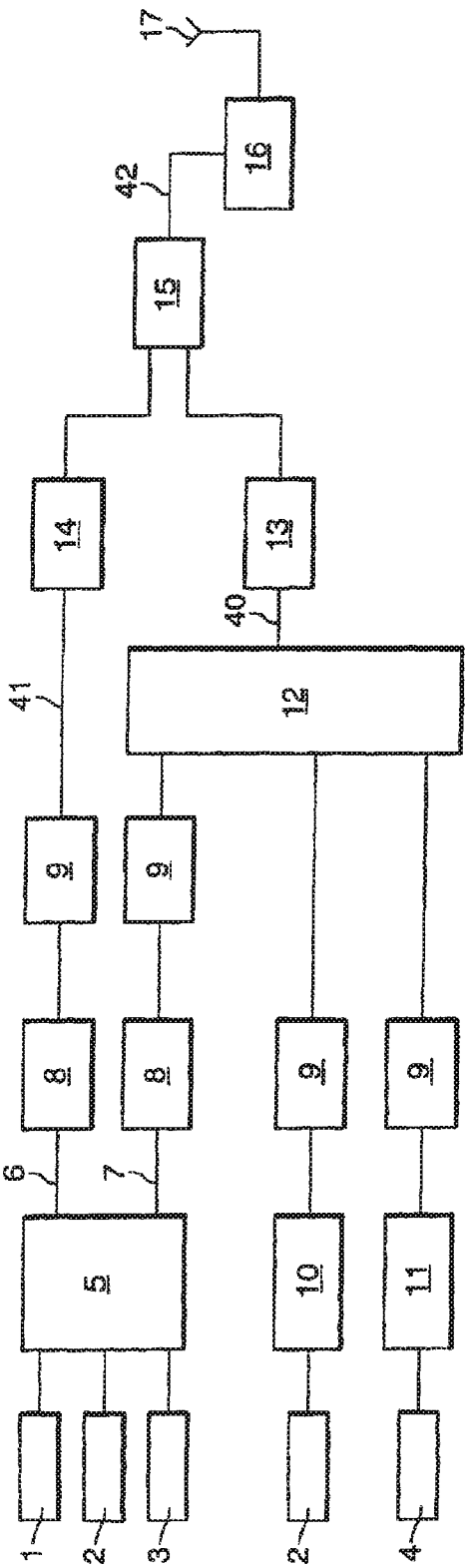

Fig. 1

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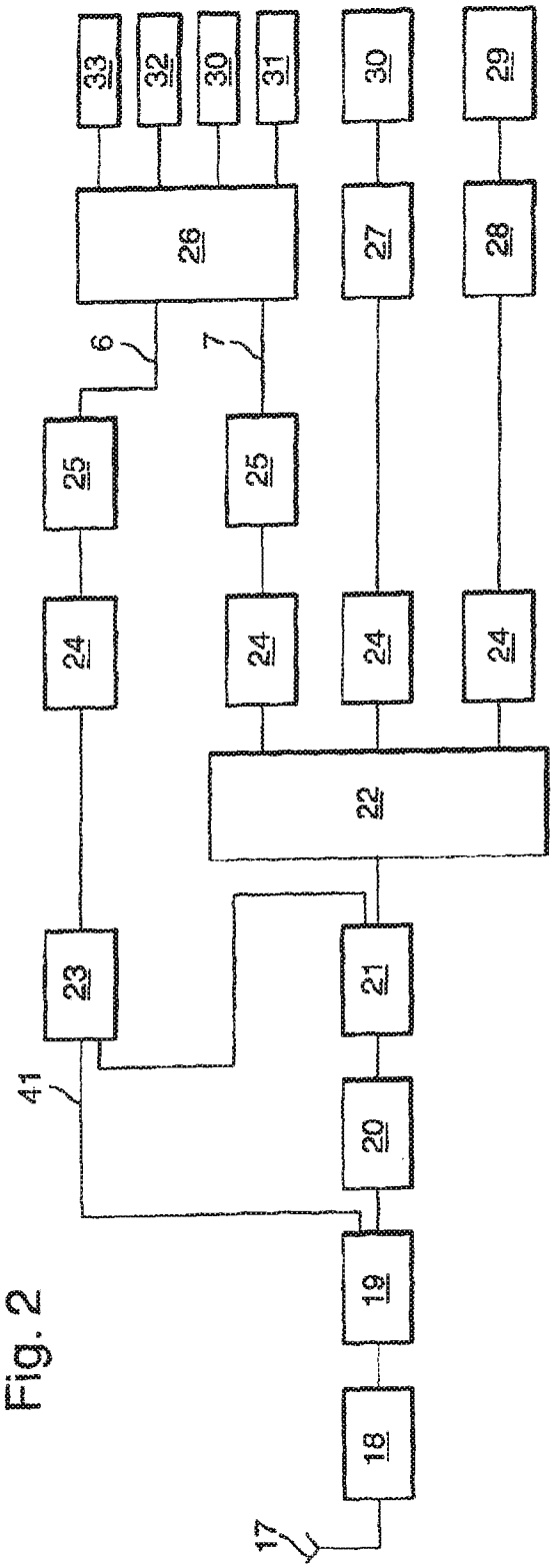

Fig. 2

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Fig. 3a

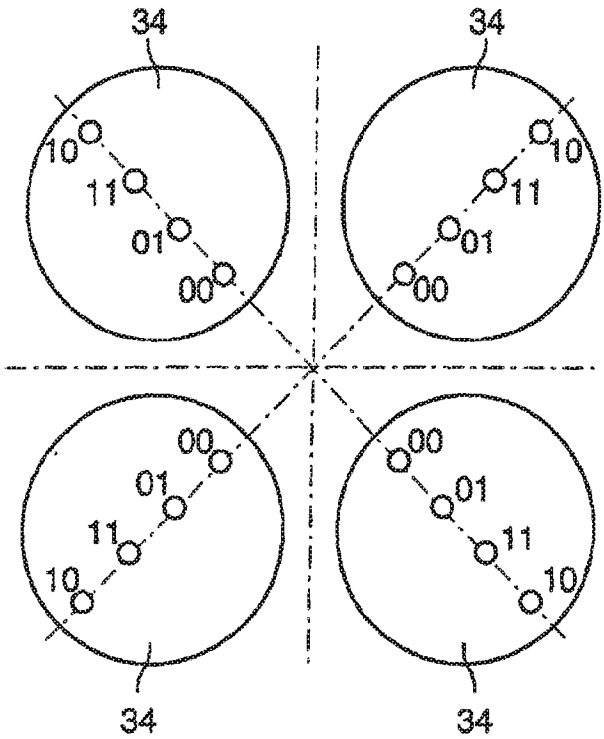


Fig. 3b

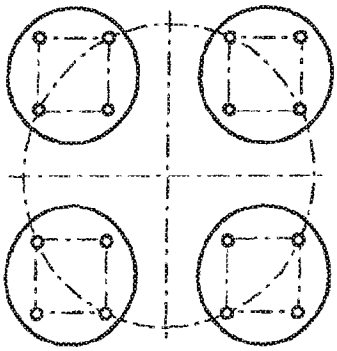
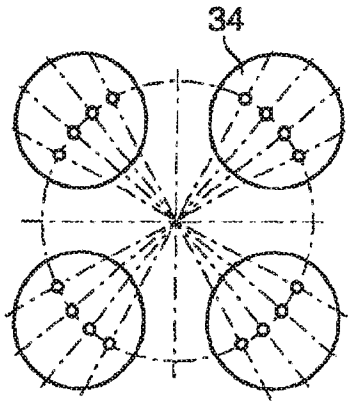


Fig. 3c



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審査請求　未請求

（全 5 頁）

⑭デイジタルデータ記録方法

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明　　細　　書

1、発明の名称

ディジタルデータ記録方法

2、特許請求の範囲

第一のディジタルデータを第一の変調方法により記録した後、第一のディジタルデータを復調し、該ディジタルデータを基準に第二のディジタルデータを第一のディジタルデータに続いて、第二の変調方法により記録し、第一の変調方法による変調信号のレベル反転間隔を第二の変調方法による変調信号に現われるレベル反転間隔の中に存在するものとすることを特徴とするディジタルデータ記録方法。

3、発明の詳細な説明

産業上の利用分野

本発明はディジタルデータを記録媒体に記録再生するに際してのディジタルデータの記録方法に関するものである。

従来例の構成とその問題点

近年、磁気ディスク装置によるディジタルデータの記録が計算機との整合性が良く広く使用されている。特に大容量のディジタルデータ記録再生が可能なものとして光メモリディスクがある。

この光ディスク装置において、ディジタルデータの読み出しに際して、光ディスク上に書かれたアドレスを検出し、このアドレスに続くディジタルデータを読み出すという検索を行なっている。また、ディジタルデータの書込みに際しては、既に書込まれているアドレスを検出し、このアドレスに続く空白部にディジタルデータを書込むことが行なわれている。アドレスデータ及びディジタルデータは記録に際して変調、例えばＦＭ，MFM，４－５変換，３ＰＭ変調等の変調を受けて記録される。第１図(ｱ)，(ｲ)にディジタルデータの記録される前の状態Ａと、記録された後Ｂの状態を示す。さらに第２図に再生側の構成を示す。従来、アドレス部１の記録の変調方式としては変復調アルゴリズムが簡易なもの、及び可変速再生の簡易なもの、例えばＦＭ変調が用いられ、データ部２の記録の変調方式としては高密度記録可能なもの、例

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えば4－5変換、3PM変調等が用いられている。アドレス部1とデータ部2の変調方法が異なるので、復調回路6，7はそれぞれに対応したものが必要となる。また復調に際してのクロック再生が必要であるが、アドレス部1のクロック周波数とデータ部2の周波数が異なっているために、クロック再生回路4，5もまたそれぞれ異なるものが必要となる。また、クロック再生回路4，5に位相制御発振回路（以下PLL回路と呼ぶ）を用いた場合、アドレス部1ではデータ部2のクロック再生回路のクロックが、データ部2ではアドレス部1のクロック再生回路のクロックが所定の周波数よりずれるので、アドレス部1でのアドレス部クロック再生回路4のPLL回路の引き込み、データ部2でのデータ部クロック再生回路5のPLL回路の引き込みに時間がかかり、アドレス，データの前部に引き込みに必要にアンプル部を長くとる必要があるという問題点を有していた。

発明の目的

本発明は上記従来の問題点を解消するもので、アドレス部とデータ部のクロック周波数が同一になるようにし、アドレス部，データ部のクロック再生回路を一つにし、クロック再生回路にPLL回路を用いた場合に引き込み時間を短くし、アンプル部の期間を短くするディジタルデータの記録再生方法を提供することを目的とする。

発明の構成

本発明はアドレス部にアドレスを記録するに用いる第一の変調方法による変調信号のレベル反転間隔をデータ部にデータを記録するに用いる第二の変調方法による変調信号に現われるレベル反転間隔より選択したものとすることにより、アドレス部とデータ部のクロック周波数を同一にし、クロック再生回路を一つとし、クロック再生時の引き込み時間を短くすることを目的とする。

実施例の説明

本発明の一実施例として、アドレス部の変調方法としてFM変調，データ部の変調方法として4－5変換変調を用いた場合を示す。FM変調は、データが"1"のときデータのビットセルの中央でレベル反転，データが"0"のときはレベル反転なし、データのビットセルの境界は常にレベル反転する変調方法であり、第3図にその例を示す。4－5変換変調は、データを4ビット単位に分割し，該4ビットのデータ語に対して第4図に示す変換テーブルに従って5ビットの符号語に変換し該符号語のビット"1"のビットセルの中央でレベル反転させる変調方法であり、第5図にその例を示す。FM変調のレベル反転間隔はT_1とT_2の2種類のみであり、4－5変換変調ではT_3，T_4，T_5の3種類である。T_1とT_2の関係は

$$T_2 = 2T_1 \quad \cdots\cdots\cdots\cdots(1)$$

であり、T_3，T_4，T_5の関係は

$$\left.\begin{aligned} T_5 &= 3T_3 \\ T_4 &= 2T_1 \end{aligned}\right\} \quad \cdots\cdots\cdots\cdots(2)$$

である。以上の関係から、T_1をT_3と等しくし、T_4をT_2と等しくすることにより、FM変調のレベル反転間隔は、4－5変換変調のレベル反転間隔に存在するものとなる。その結果、各変調信号に対する再生クロック信号を第6図に示すように同一とすることができる。

次に第7図により再生クロック信号を用いたFM変調信号の復調について説明する。得られた再生クロック信号Dより検出窓Fを作る。この検出窓Fのハイレベル内にあるFM信号Cのエッヂパルスを抜き取りパルスGを得る。パルスGをDフリップフロップのクロック入力に入力し、データ入力に検出窓Fを入力し、エッヂパルスEの検出窓Fのローレベル内にあるパルスをリセット入力に入力することにより、データが"1"を示す信号Hを得る。この信号Hを検出窓Fの立下り時にDフリップフロップに読み込むようにすることにより再生データIが得られることになる。

再生クロック信号を用いた4－5変換変調信号の復調を以下に示す。得られた再生クロックDを用いて4－5変換変調信号を1クロック分遅延させた信号Kを作り、JとKとを排他的論理和をとることにより再生符号語データ系列Lを得る。この再生符号語データ系列を再生クロックDにより5ビットシフトレジスタに入力し、この5ビット

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ごとに変換テーブルに従って4ビットのデータ語に変換すれば、もとのデータが得られる。

以上のように4－5変換変調のレベル反転間隔の内2種類を用いたFM変調とすることにより、アドレス部の再生クロックとデータ部の再生クロックとが同一となるので、クロック再生回路を一つにすることができ、アドレス部でクロックが引き込まれておればアドレス部とデータ部の境界で若干のクロックの乱れがあるが、クロック周波数は大きくはずれないので次のデータ部のクロック引き込みが容易となる。それゆえデータ部の前のクロック引き込みのアンプル期間を短くすることができるので、データ部の有効データ量を多く確保することができる。

以上は、第一の変調をFM変調とし、第二の変調を4－5変換変調としたものであるが、その他の変調方法でも同様に考えることができる。例えば第一の変調をMFM変調で、第二の変調が3PM変調の場合を次に説明する。3PM変調の場合、レベル反転間隔は、データのビット周期をTとすれば、1.5T，2T，2.5T，3T，3.5T，4T，4.5T，5T，5.5T，6Tの10種類がある。MFM変調では最短のレベル反転間隔をT_Mとすれば、T_M，$1.5T_M$，$2T_M$の3種類である。T_Mを2Tとすることにより、$1.5T_M$は3T，$2T_M$は4Tとなり、3PM変調のレベル反転間隔を用いて変調信号を構成することができる。それゆえ、第一の実施例で述べたように再生クロックが同一となり、同様の効果が得られる。

発明の効果

本発明のディジタルデータ記録再生方法は、第一の変調方法による変調信号のレベル反転間隔を第二の変調方法による変調信号に現われるレベル反転間隔の中より選択したものとすることにより、第一の変調方法による記録及び第二の変調方法による記録が共に存在する記録再生装置において、クロック再生回路を第一の変調の復調回路、第二の変調の復調回路とで共用することができ、第一の変調から第二の変調へ変化する部分において、再生クロックの乱れを最小限にすることができ、第二の変調の記録部分の前部に存在するアンプル部分を短くすることができ、第二の変調の記録部の有効データ量を多く確保することができる。

4．図面の簡単な説明

第1図は従来の光ディスクディジタル記録再生装置の記録信号構成を示す図、第2図は前記装置の再生側のブロック図、第3図は本発明の第一の実施例で用いるFM変調を説明する波形図、第4図は第一の実施例で用いる4－5変換変調の対応関係を説明する図、第5図は4－5変換の波形図、第6図は本発明を実施した場合の波形図、第7図はFM変調の復調を説明するための波形図、第8図は4－5変換変調の復調を説明するための波形図である。

D……再生クロック信号、F……検出窓、E……パルス、H……"1"を示す信号、I……再生データ。

代理人の氏名　弁理士　中　尾　敏　男　ほか1名

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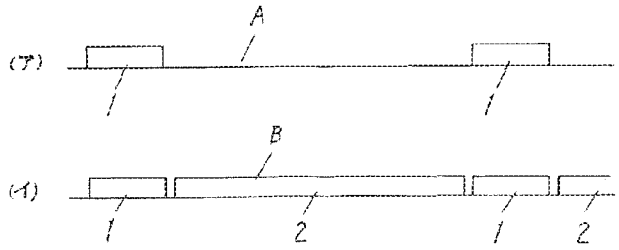
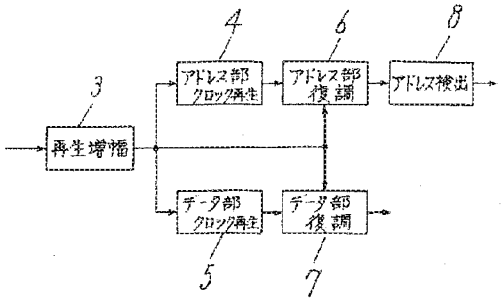
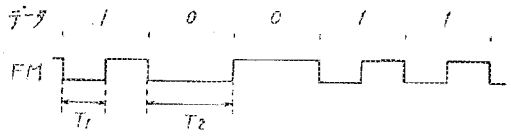
第 1 図



第 2 図



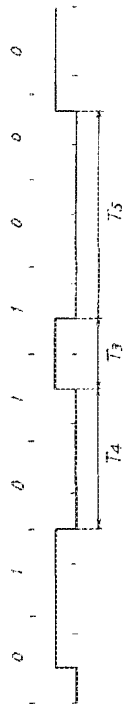
第 3 図



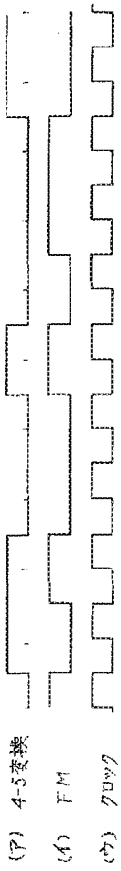
第 4 図

データ語	符号語
0 0 0 0	1 1 0 0 1
0 0 0 1	1 1 0 1 1
0 0 1 0	1 0 0 1 0
0 0 1 1	1 0 0 1 1
0 1 0 0	1 1 1 0 1
0 1 0 1	1 0 1 0 1
0 1 1 0	1 0 1 1 0
0 1 1 1	1 0 1 1 1
1 0 0 0	1 0 0 1 0
1 0 0 1	0 1 0 0 1
1 0 1 0	0 1 0 1 0
1 0 1 1	0 1 0 1 1
1 1 0 0	1 1 1 1 0
1 1 0 1	0 1 1 0 1
1 1 1 0	0 1 1 1 0
1 1 1 1	0 1 1 1 1

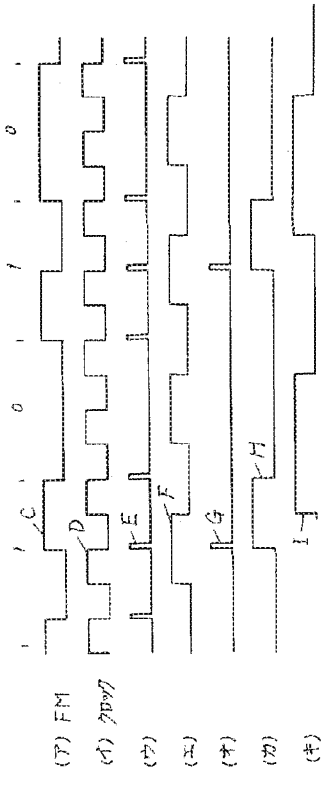
第 5 図



第 6 図



第 7 図



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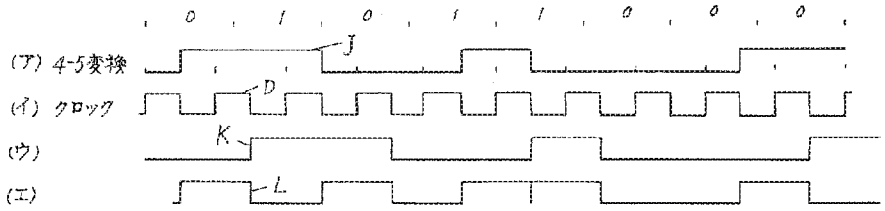
第 8 図



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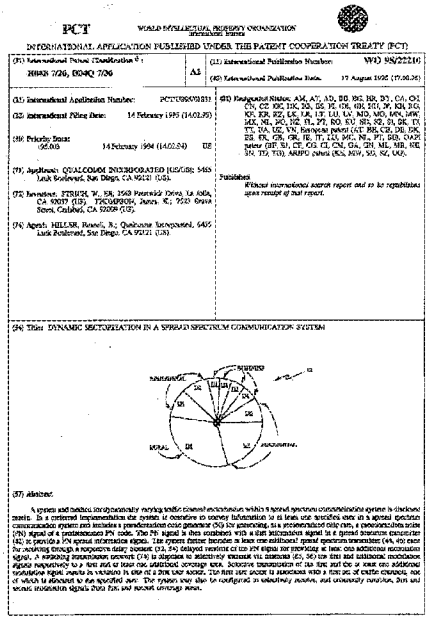
(54) Title: DYNAMIC SECTORIZATION IN A SPREAD SPECTRUM COMMUNICATION SYSTEM.

Un sistema para transportar informaci¢n a por lo menos un usuario en un sistema de comunicaci¢n de espectro disperso, que comprende: un medio para generar, a una velocidad de chip predeterminada, una primera se¤al de ruido pseudoaleatorio (PN) de un primer c¢digo PN predeterminado; un primer medio para combinar la primera se¤al Pn y una primera se¤al de informaci¢n y para proporcionar una primera se¤al de modulaci¢n resultante; un medio para proporcionar una segunda se¤al de modulaci¢n haciendo retardar la primera se¤al de modulaci¢n en un primer retardo predeterminado que se relaciona inversamente a la velocidad de chip; un medio para transmitir selectivamente la primer y la segunda se¤ales de modulaci¢n respectivamente a la primera y la segunda reas de cobertura; mediante lo cual la transmisi¢n selectiva de la primera y la segunda se¤ales de modulaci¢n da por resultado la variaci¢n en tama¤o de un primer sector de usuario en donde se incluye el por lo menos un usuario.



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(54) Title: DYNAMIC SECTORIZATION IN A SPREAD SPECTRUM COMMUNICATION SYSTEM

(57) Abstract

A system and method for dynamically varying traffic channel sectorization within a spread spectrum communication system is disclosed herein. In a preferred implementation the system is operative to convey information to at least one specified user in a spread spectrum communication system and includes a pseudorandom code generator (50) for generating, at a predetermined chip rate, a pseudorandom noise (PN) signal of a predetermined PN code. The PN signal is then combined with a first information signal in a spread spectrum transmitter (42) to provide a PN spread information signal. The system further includes at least one additional spread spectrum transmitter (44, 46) each for receiving through a respective delay element (52, 54) delayed versions of the PN signal for providing at least one additional modulation signal. A switching transmission network (74) is disposed to selectively transmit via antennas (85, 86) the first and additional modulation signals respectively to a first and at least one additional coverage area. Selective transmission of the first and the at least one additional modulation signal results in variation in size of a first user sector. The first user sector is associated with a first set of traffic channels, one of which is allocated to the specified user. The system may also be configured to selectively receive, and coherently combine, first and second modulation signals from first and second coverage areas.

SECTORIZACIÓN DINAMICA EN UN SISTEMA DE COMUNICACIÓN DE ESPECTRO DE DISPERSIÓN

ANTECEDENTES DE LA INVENCIÓN

I. Campo de la Invención

La presente invención se relaciona con sistemas de comunicación que utilizan señales de espectro disperso, y en forma más particular se relaciona con un método y un aparato novedosos para la sectorización dinámica de canal dentro de un sistema de comunicación de espectro disperso.

II. Descripción de la Técnica Relacionada

Se han desarrollado sistemas de comunicación que permiten la transmisión de señales de información a partir de una ubicación fuente hacia un destino de usuario físicamente distinto. Los dos métodos, analógico y digital, se han utilizado para transmitir estas señales de información sobre canales de comunicación que se eslabonan con la fuente y las ubicaciones de usuario. Los métodos digitales tienden a proporcionar varias ventajas con relación a las técnicas analógicas, entre ellas se incluyen, por ejemplo, la inmunidad mejorada al ruido e interferencia de canal, la capacidad aumentada, y la mejor seguridad de las comunicaciones a través del uso del cifrado.

Al transmitir una señal de información desde una ubicación fuente sobre un canal de comunicación, la señal de información se convierte primero en una forma adecuada para la eficiente transmisión sobre el canal. La conversión, o modulación, de la señal de información involucra variar un parámetro de una onda portadora con base en la señal de información, de tal forma que el espectro de la portadora modulada resultante queda confinado dentro de la anchura de banda del canal. En la ubicación del usuario la señal de mensaje original se replica de una versión de la portadora modulada recibida subsecuentemente para la propagación sobre el canal. Esta replicación en general se logra utilizando un inverso del proceso de modulación empleado por el transmisor fuente.

La modulación facilita también el multiplexado, es decir, la transmisión simultánea de varias señales sobre un canal común. Los sistemas de comunicación multiplexados en general incluirán una pluralidad de unidades de suscriptor remotas que requieren del servicio intermitente de una duración relativamente corta en lugar del acceso continuo hacia el canal de comunicación. Los sistemas diseñados para permitir la comunicación en breves periodos de tiempo con un juego de unidades de suscriptor, se han denominado: sistemas de comunicación de acceso múltiple.

Un tipo particular de sistemas de comunicación de

acceso múltiple es el conocido como sistema de espectro disperso. En los sistemas de espectro disperso la técnica de modulación utilizada da por resultado una dispersión de la señal transmitida sobre una banda de frecuencia amplia dentro del canal de comunicación. Un tipo de sistema de espectro disperso de acceso múltiple es un sistema de modulación de acceso múltiple por división de código (CDMA). Otras técnicas de sistema de comunicación de acceso múltiple como por ejemplo los esquemas de acceso múltiple por división de tiempo (TDMA), acceso múltiple por división de frecuencia (FDMA) y modulación AM, tales como los esquemas de banda lateral simple de amplitud compuesta, ya se conocen en la técnica. Sin embargo, la técnica de modulación de espectro disperso de CDMA tiene ventajas considerables sobre estas técnicas de modulación para los sistemas de comunicación de acceso múltiple. El uso de las técnicas CDMA en un sistema de comunicación de acceso múltiple se revela en la Patente de los Estados Unidos No. 4,901,307, otorgada el 13 de febrero de 1990 y titulada *"Spread Spectrum Multiple Access Communication System Using Satellite or Terrestrial Repeaters"*, cedida a la cesionaria de esta invención.

En la Patente de los Estados Unidos No. 4,901,307 antes mencionada, se revela una técnica de acceso múltiple en donde un gran número de usuarios del sistema móvil,

tienen cada uno un transceptor que se comunica a través de repetidores vía satélite o de estaciones base terrestres utilizando señales de comunicación de espectro disperso CDMA. Al utilizar comunicaciones CDMA, el espectro de frecuencia puede reutilizarse varias veces permitiendo así un aumento en la capacidad de usuario del sistema. El uso del CDMA da por resultado una eficiencia espectral mucho mayor que aquella lograda utilizando otras técnicas de acceso múltiple.

En particular, la comunicación de los sistemas CDMA entre una estación base y las unidades de suscriptor dentro de la región celular circundante se logra mediante la dispersión de cada señal transmitida sobre la anchura de banda de canal disponible utilizando un código de dispersión usuario único. En estos sistemas CDMA, las secuencias de código utilizados para dispersar el espectro se construyen a partir de dos tipos diferentes de secuencias, cada una con diferentes propiedades para proporcionar diferentes funciones. Existe un código externo que se comparte por todas las señales en una célula o sector que se utiliza para discriminar entre señales de trayectoria múltiple. Además, el ajustar la fase del código externo permite que éste se utilice para discriminar entre juegos de usuarios agrupados en "sectores" dentro de una célula dada. Por ejemplo, los usuarios dentro de una

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célula dada pueden dividirse en tres sectores disponiendo tres fases del código externo. También existe un código interno que se utiliza para discriminar entre señales de usuario transmitidas sobre una pluralidad de "canales de tráfico" asociados con cada sector usuario. Las señales transmitidas específicas se extraen de los canales de comunicación mediante la desdispersión de la energía de señal compuesta en el canal de comunicación con el código interno asociado con la señal transmitida que va a extraerse.

Haciendo referencia a la Figura 1A, se muestra una primera célula 10 ejemplaria en la que están dispuestas una pluralidad de unidades de suscriptor 12 y una estación base 14. Como se indica en la Figura 1A, la célula 10 está dividida en seis áreas de cobertura C1-C6. La estación base 14 puede incluir un juego de seis antenas de haz fijo (no mostradas) dedicadas a facilitar la comunicación con las unidades de suscriptor en las áreas de cobertura C1-C6, respectivamente. Las unidades de suscriptor 12 se agrupan en una pluralidad de sectores de usuario, cada uno de los cuales soporta un número equivalente de canales de tráfico. Como se indica por la Figura 1A, un primer sector de usuario residencial abarca las áreas de cobertura C1 y C6, mientras que un segundo sector de usuario residencial expande el área de cobertura C4. En forma similar, el

sector de usuario que incluye las áreas principalmente rurales está asociado con las áreas de cobertura C2 y C3, mientras que los usuarios comerciales se concentran dentro del área de cobertura C5.

Como se indica en la Figura 1A, es necesario que ciertos sectores de usuarios sean relativamente angostos con objeto de ajustarse a las demandas durante los períodos pico de la utilización del sistema. Por ejemplo, la región neutral relativamente angosta del sector de usuarios comerciales es necesaria debido a la alta concentración de usuarios comerciales dentro del área de cobertura C5 que desean comunicarse durante horas de trabajo, es decir entre las 8 a.m. y las 5 p.m. Esto es, si el alcance del sector de los usuarios comerciales se expandiera para incluir otras regiones diferentes al área de cobertura C5, sería posible que un número insuficiente de los canales de tráficos estuvieran disponibles durante las horas comerciales para ajustarse a todos aquellos que desean hacer llamadas. En contraste, la concentración difusa de las unidades de suscriptor 12 entre las áreas rurales permite que los canales de tráfico asociados con el sector del usuario rural sean asignados entre usuarios distribuidos en dos áreas de cobertura C2-C3.

Desafortunadamente, durante las horas inhábiles, un número de canales de tráfico dedicados al sector de los

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usuarios comerciales muy probablemente quedaría sin utilizarse, ya que en esos momentos existen considerablemente menos interesados comerciales en hacer llamadas y un número correspondientemente mayor de personas que desean hacer llamadas residenciales. Consecuentemente, sería deseable poder proporcionar una alta concentración de canales de tráfico a los usuarios comerciales dentro del área de cobertura CS durante las horas hábiles y proporcionar una concentración relativamente menor de canal de tráfico durante las horas inhábiles.

Aunque existen arreglos de antena capaces de conformar de manera adaptable un haz proyectado en respuesta al cambio de la demanda del usuario, la implementación de este tipo de arreglos de antena dentro del sistema de la Figura 1A requeriría de una modificación correspondiente en la arquitectura del haz fijo de la estación base 14. Además, la circuitería relativamente sofisticada de RF/microondas que se emplea típicamente en las redes formadoras de haz adaptable dan por resultado un costo y complejidad mayores en el sistema. En consecuencia, es el objeto de la presente invención el proporcionar una técnica redituable para variar la concentración de los canales de tráfico en respuesta a los cambios en la distribución de usuarios dentro de un sistema de comunicación celular de espectro disperso.

En el ejemplo específico de un sistema de comunicación CDMA, cada sector de usuario es capaz de soportar un nivel dado de demanda de tráfico. En consecuencia, es un objeto adicional de la invención el diseñar el tamaño de los sectores de usuarios específicos dentro de una comunicación CDMA a la demanda de los canales de tráfico dentro del sector. Esta asignación de canal de tráfico eficiente permitiría la utilización óptima de las fuentes de sistemas de comunicación, disminuyendo así el costo por usuario.

Además de dirigirse a la necesidad de la asignación de canales de tráfico flexibles como consecuencia de los cambios a corto término en la demanda de usuario que se describe antes, también es un objeto de la invención el ajustarse a cambios a largo término en la demanda de los usuarios. Estas variaciones a largo término en la demanda podrían surgir, por ejemplo, de desplazamientos en la distribución de la población y de los patrones de construcción dentro de un área geográfica dada.

Una ventaja adicional de los sistemas de haz fijo convencionales, como por ejemplo el sistema de la figura 1A, es que los estimados relativamente precisos de las demandas de los usuarios deberán típicamente estar disponibles antes de la instalación del sistema. Es decir, los diseñadores del sistema generalmente deben contar con

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la información detallada que se relaciona con los patrones de demanda esperados con objeto de configurar la estación base de haz fijo para proporcionar la capacidad de canal de tráfico requerida para cada sector de usuarios. Los cambios en los patrones de uso que ocurren en forma próxima al período de instalación tienden por lo tanto a evitar la utilización óptima de los canales de tráfico disponibles. Por lo tanto es todavía otro objeto de la presente invención el proporcionar un sistema de comunicación capaz de ser diseñado, durante la instalación, de acuerdo con los patrones existentes de la demanda de canales de tráfico.

SUMARIO DE LA INVENCIÓN

La invención proporciona un sistema y un método para variar en forma dinámica la sectorización de los canales de tráfico dentro de un sistema de comunicación de espectro de dispersión.

En una modalidad preferida, el sistema de la invención funciona para transportar información hacia por lo menos un usuario específico en un sistema de comunicación de espectro disperso. El sistema incluye una primer red para generar, a una velocidad de chip predeterminada, una primera señal de ruido pseudoaleatorio (PN) de un primer código PN predeterminado. La primera señal PN se combina entonces con una primera señal de

información con objeto de proporcionar una primera señal de modulación resultante. El sistema incluye además una segunda red para proporcionar una segunda señal de modulación retardando la primera señal de modulación en un retardo predeterminado, inversamente relacionado con la velocidad de chip PN. Una red de transmisión de conmutación está colocada para transmitir selectivamente la primera y segunda señales de modulación respectivamente la primera y segunda áreas de cobertura. En esta forma puede utilizarse la transmisión selectiva de la primera y segunda señales de modulación para variar el tamaño del primer sector de usuario durante diferentes períodos de operación del sistema. El primer sector de usuario se asocia con un primer juego de canales de tráfico, uno de los cuales se asigna al usuario específico.

BREVE DESCRIPCIÓN DE LOS DIBUJOS

Los objetos y particularidades adicionales de la invención se podrán comprender con mayor facilidad a partir de la siguiente descripción detallada y de las reivindicaciones anexas, cuando se tomen con relación a los dibujos que se acompañan en donde:

La Figura 1A muestra una célula ejemplo, incluida dentro de un sistema de comunicación celular, en donde se colocan una pluralidad de unidades de suscriptor y una

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estación base.

La Figura 1B muestra una segunda célula ejemplo en la forma sectorizada de acuerdo a la invención durante horas hábiles típicas.

La Figura 1C ilustra la segunda célula ejemplo tal como se sectoriza durante horas nocturnas de acuerdo a la invención.

La Figura 1D muestra un diagrama de bloques que representa un transceptor de comunicaciones de estación base ejemplario, en donde el sistema de sectorización dinámica de la invención está incorporado.

La Figura 2 proporciona una representación en diagrama de bloques de una red del transmisor de estación base configurada para proporcionar la sectorización dinámica de usuarios de acuerdo a la invención.

La Figura 3 ilustra una matriz de conmutador, colocada dentro del transmisor de estación base, para proporcionar una conexión conmutable entre la señal de información asociada con cada sector de usuario y un juego de seis manipuladores de antena.

La Figura 4 ilustra un diagrama de bloques de una red del transmisor de estación base capaz de proporcionar la sectorización dinámica de usuarios incrementada, utilizando tanto haces de antena polarizados horizontal y verticalmente.

Las Figuras 5A y 5B proporcionan respectivamente vista superior y lateral de la antena provisional resonante de modo dual incorporada dentro de una implementación requerida de las antenas de estación base.

La Figura 6 muestra una representación en diagrama de bloques de una red receptora de estación base configurada para configurar la sectorización dinámica de usuarios de acuerdo con la invención.

La Figura 7 proporciona una representación en diagrama de bloques de un transmisor de espectro disperso ejemplario.

La Figura 8 ilustra una red de generación piloto para proporcionar las secuencias piloto de canal I y Q.

La Figura 9 muestra una implementación ejemplo de un transmisor de estación base RF.

La Figura 10 es un diagrama de bloques de un receptor de diversidad ejemplo colocado dentro de una unidad de suscriptor.

La Figura 11A representa en forma ilustrativa el patrón de azimuth de un haz fijo de 40 grados, que se asume va a proyectarse por una primera antena de estación base asociada con una de las áreas de cobertura C1-C6 (Figura 1A).

La Figura 11B representa en forma ilustrativa el patrón de azimuth producido cuando par adyacente de antenas

de estación base de haz fijo son manipulados en fase.

La Figura 12 muestra una representación en diagrama de bloques de una red de transmisor de estación base configurada para proporcionar la sectorización dinámica de los usuarios al proyectar un juego de haces en faz a cada sector de usuario.

La Figura 13 ilustra una configuración de estación base alterna para proporcionar la sectorización dinámica de los usuarios al proyectar un juego de haces en fase.

La Figura 14 muestra un arreglo triangular de los paneles de antena del arreglo de primera, segunda y tercera fase, que operan colectivamente para proporcionar un juego de nueve haces de antena.

La Figura 15 ilustra una implementación preferida de los paneles de antena de la Figura 14, cada uno de los cuales incluye un arreglo 4x4 de elementos provisionales.

La Figura 16 es un diagrama de bloques de una red formadora de haz que se utiliza para manipular un panel de antena de arreglo en fase.

DESCRIPCIÓN DE LA MODALIDAD PREFERIDA

I. Introducción

Volviendo ahora a la Figura 1B, se muestra una segunda célula 18 ejemplo, sectorizada de acuerdo con la

invención, durante horas hábiles normales. Como se indica en la Figura 1B, la segunda célula 18 está sectorizada en un juego de nueve sectores de usuario U1-U9. La segunda célula 18 está dividida durante las horas hábiles de manera que un juego de cuatro sectores U1-U4, cada uno expandiéndose en un ángulo de, por ejemplo, 20 grados, se asignan a un centro de alta densidad de población. Durante las horas hábiles las áreas rurales y residenciales menos pobladas de la celda reciben servicio mediante un juego de sectores de usuario relativamente amplio U5 y U6-U9, respectivamente. En una modalidad ejemplo la anchura angular del sector de usuario rural U5 es un juego de 100 grados, los sectores usuario residenciales U6, U8 y U9 son cada uno de 40 grados, y el sector usuario residencial U7 es de 60 grados. El respiro angosto de los sectores de usuario U1-U4 se necesitan por la alta concentración de usuarios dentro del centro comercial que desean comunicarse durante horas hábiles. En esta forma el alcance confinado de los sectores de usuario U1-U4 asegura que un número suficiente de los canales de tráfico estén disponibles durante horas hábiles para ajustarse a un número deseado de usuarios que están en el centro comercial.

La Figura 1C ilustra la segunda célula 18 ejemplo sectorizada durante la noche (es decir las horas no hábiles) en una pluralidad de nueve sectores de usuario

U1'-U9' de acuerdo con la invención. Como se indica en la Figura 1C, durante las horas inhábiles un solo sector de usuario U1' de 80 grados, en lugar de cuatro sectores U1-U4 de 20 grados se requieren durante las horas hábiles, y se emplean para dar servicio a las demandas dentro del centro comercial. En forma similar, el desplazamiento de población hacia las áreas residenciales durante las horas de la tarde y noche requieren la sectorización aumentada proporcionada por siete sectores de usuario U2'-U6', y U7'-U9', en relación a los cuatro sectores U6-U9 que se requieren durante el día. En la modalidad ejemplo, la anchura angular de los sectores de usuario residencial U2'-U4' y U8'-U9', se ajusta a 20 grados, y la anchura de los sectores de usuario residencial U6' y U7' se ajusta a 40 grados. Los sectores de usuario rural U5' permanecen en 100 grados durante tanto las horas del día como de la noche como consecuencia de la variación temporal mínima típica en la demanda de los usuarios en las regiones rurales. El cambio en la sectorización ilustrado por las Figuras 1B-1C puede lograrse utilizando el sistema de sectorización dinámica de la invención, la operación del cual se describe a continuación con relación al diagrama de bloques de la Figura 1D.

La Figura 1D muestra una representación en diagrama de bloques de un transceptor de comunicaciones 25

de estación base ejemplo, en donde el sistema de sectorización dinámico de la invención está incorporado. Como se discute abajo, el transceptor 25 funciona para proporcionar servicio mejorado a los usuarios colocados dentro de una primera célula de un sistema de comunicación celular al variar dinámicamente la asignación de los canales de tráfico entre varios sectores de usuario dentro de la célula. El transceptor 25 se observa que incluye un controlador 27, un sistema de antena 29 y bancos de canal de transmisión/recepción 31. El controlador 27 se programa típicamente para proporcionar bancos 31 de ajuste de canal/asignación de transmisión/canal de recepción. Los bancos de canal de transmisión/recepción 31 se acoplan electromagnéticamente al sistema de antena 29 mediante una línea 32 de transmisión de onda guía 32 o semejante. Cada banco de canal individual puede comprender, por ejemplo, una pluralidad de unidades de canal capaces de facilitar la comunicación con un usuario particular. En la modalidad de la Figura 1D, los bancos de canal de transmisión/recepción 31 suministran señales formadoras de haz al sistema de antena 29 a fin de sectorizar la primer célula en una pluralidad de sectores de usuario, cada uno de los cuales tiene asociado con el mismo una pluralidad de canales de tráfico de usuario. Las señales de información se relevan entre los bancos de canal 31 y una red de comunicaciones

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externa, por ejemplo una red de teléfono público conmutada (PSTN) sobre un bus de datos 33.

Una primera modalidad preferida de la invención, un número fijo de los canales de tráfico está asociado con cada uno de los sectores de usuario. Bajo esta restricción, la presente invención contempla la variación de ajuste en la demanda de usuarios dentro de las diversas regiones de la célula, ajustando el tamaño relativo de cada sector de usuario. Por ejemplo, podrían emplearse un número de sectores de usuario relativamente angostos para dar servicio a los usuarios que están dentro de un área particular de la célula durante períodos de alta demanda del usuario. Esto aumenta al máximo la probabilidad de que un canal de tráfico esté disponible a todos aquellos que deseen establecer comunicación durante esos períodos de demanda superior. Inversamente, durante los períodos de mínima demanda podría utilizarse un número relativamente menor de sectores de usuario de anchura más amplia para proporcionar la capacidad requerida en el canal de tráfico. Esta ampliación de los sectores de usuario asociado con un área celular particular durante períodos de demanda reducida permite el uso eficiente de un número fijo de canales de tráfico asignados a cada sector de usuario. Es decir, al aumentar la extensión geográfica de los sectores de usuario durante el período de demanda mínima el número

de usuarios probables del sistema incluidos dentro de cada sector de usuario, pueda mantenerse relativamente constante. Esto evita que una capacidad en exceso del canal de tráfico se desarrolle en los sectores de usuario dirigidos a un área geográfica dada en caso de que disminuya la concentración de usuarios es decir la demanda dentro del área dada.

Debe entenderse sin embargo, que en modalidades alternativas de la presente invención el número de canales de tráfico asignados a un sector de usuario particular puede variar en respuesta al cambio de las condiciones de demanda. Además, la presente invención puede permitir todavía una mejora en la utilización del canal de tráfico permitiendo que se tengan alteraciones tanto en el tamaño geográfico como en el número de canales de tráfico asociados con un sector de usuario dado

En una modalidad actualmente preferida de la invención se supervisan las estadísticas que se relacionan con el uso del canal dentro de cada sector de usuarios mediante los bancos asociados de los bancos de canal 31 y se transfieren al controlador 27 mediante un primer bus de control 34. La información de control proveniente del controlador 27, recibida respectivamente por los bancos de canal 31 y el sistema de antena 29 sobre el primer bus de control 34, y el segundo bus de control 35, permite que los

canales de tráfico sean asignados a los sectores de usuario con base en las estadísticas de uso suministradas por los bancos de canal 31. Es decir, el patrón de haz proyectado por el sistema de antena 29 se ajusta con objeto de que un juego seleccionado de los canales de tráfico se proporcionen a cada sector de usuario. En la modalidad actualmente preferida, el uso de canal monitoreado es desplegado a un operador (no mostrado) mediante el controlador 27, permitiendo así la especificación de la sectorización celular deseada. En un modo automático, el control 27 se programa para asignar canales y/o tamaños de sector con base en las estadísticas de uso de canal.

En otras modalidades de la invención el controlador 27 puede configurarse para monitorear el uso del canal en virtud de la información recibida de los bancos de canal 31 sobre el primer bus control 34. La información de uso de canal pertinente podría de nuevo desplegarse a un operador con objeto de permitirle hacer los ajustes adecuados en el tamaño de cada sector de usuario. Alternativamente el controlador 27 podría programarse para proporcionar automáticamente los mandos de ajuste/asignación de canal a los bancos de canal 31 con base en el uso de canal monitoreado, una vez más evitando la necesidad de controlar la información que va a suministrarse a un operador.

Aunque en las modalidades actualmente preferidas de la invención el tamaño de cada sector de usuario se ajusta a través de la alteración del patrón de haz proyectado por el sistema de antena 29, en otras implementaciones podría lograrse una modificación equivalente del tamaño del sector a través del procesamiento de las señales formadoras de haz suministradas por los bancos de canal 31. En estas implementaciones las señales formadoras de haz procesadas por los bancos de canal 31 podrían ponderarse y combinarse antes de proporcionarse al sistema de antena 29 o recibirse desde el mismo. En esta forma podría lograrse la sectorización dinámica proporcionando información de control a los elementos electrónicos procesadores de señal (que no se muestran) acoplados a los bancos de canal 31, en lugar de suministrar esta información al sistema de antena 29.

Haciendo otra vez referencia a la Figura 1D, aparentemente una forma de acomodar la variación en la demanda del usuario sería configurar el sistema de antena 29 de la estación base para proporcionar una pluralidad de haces de antena fijos utilizando un juego asociado de elementos de antena de haz fijo. En este arreglo, cada antena de estación base proyectaría un haz de anchura fija sobre una de un juego de áreas de cobertura adyacentes. Se

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asignarían entonces a cada sector de usuario diferentes números de áreas de cobertura con base en los requerimientos de uso esperados. En esta forma los cambios en la concentración de usuarios podrían compensarse al variar dinámicamente el número de haces de antena fijos utilizados para llevar los canales de tráfico asociados con un sector dado

Una dificultad que se presenta con este enfoque es que podría esperarse una distorsión considerable del patrón de haz en forma próxima a los límites entre las áreas de cobertura incluidas dentro de un sector de usuario dado. Como ya se discutió en la parte de antecedentes de la invención, en algunos sistemas de comunicación celular, se utiliza un código PN largo de fase determinada para modular las señales de información llevadas por los canales de tráfico de un sector de usuario dado. Si estas señales de información moduladas con el código PN largo del sector de usuario dado fueran a proyectarse por un par de antenas de haz fijo en áreas de cobertura adyacentes, existiría una diferencia de fase arbitraria entre las señales moduladas PN idénticas llevadas por cada haz. Esta diferencia de fase podría engendrarse, por ejemplo, por la variación en las longitudes de las trayectorias de señal provenientes de la red formadora de haz de la estación base de cada antena de haz fijo. Como estas señales moduladas PN no están

alineadas en fase, en el límite del área de cobertura de haz la interferencia coherente resultante tendería a distorsionar el patrón de haz al producir anulaciones de señal u otras irregularidades. El desvanecimiento de la señal resultante que acompaña esta distorsión del patrón degradaría entonces la proporción señal a ruido de la señal modulada PN recibida por cualquiera de los receptores de unidad de suscriptor ubicados en forma próxima.

II. Sectorización Dinámica Utilizando Arreglo de Antena de Transmisión.

Como se describe a continuación, en una modalidad preferida de la presente invención se contempla el uso de un arreglo de antenas de haz fijo para variar dinámicamente el área abarcada por cada sector de usuario. En la forma empleada aquí, el término "sectorización dinámica de usuarios" está destinado a describir el proceso de variación de tamaño de un juego de sectores de usuario entre períodos de operación de sistema sucesivos. De acuerdo con la invención, se introduce un retardo entre cada par de señales moduladas PN idénticas proyectadas a las áreas de cobertura adyacentes dentro de un sector de usuario dado, descorrelacionando de esta manera cada uno de estos pares de señales. En la modalidad preferida se utiliza un retardo que tiene una duración ligeramente menor

que el periodo de un chip de código largo PN para descorrelacionar las señales proyectadas hacia áreas de cobertura adyacentes dentro de cada sector de usuario. Una unidad de suscriptor colocada en un límite de área de cobertura puede de esta manera discriminarse entre, y por lo tanto recibirse separadamente, las señales moduladas PN descorrelacionadas proporcionadas hacia las áreas de cobertura adyacentes. Las señales recibidas en forma separada se alinean entonces en tiempo dentro del receptor utilizando técnicas convencionales de recepción de diversidad, y se desdispersan utilizando una replica generada localmente del código PN largo.

Al aplicar la técnica de la invención al sistema de la Figura 1A podrían introducirse retardos por lo menos entre las señales proyectadas para las áreas de cobertura C1 y C6 del primer sector de usuario residencial, y entre los pares de señal proporcionados a las áreas de cobertura C2/C3 del sector de usuario rural. Aunque en una modalidad preferida los retardos también se introducen entre los pares de señal proyectados a áreas de cobertura adyacentes dentro de diferentes sectores de usuario (por ejemplo entre el par de señal proporcionados a las áreas de coberturas C3/C4) estos pares de señal se suponen como independientemente descorrelacionados como consecuencia de la diferenciación de la fase de código largo PN asociada

con cada sector de usuario.

Haciendo referencia a la Figura 2, se muestra una representación diagramática en bloques de una red de transmisión 40 de estación base configurada para proporcionar la sectorización dinámica de usuarios de acuerdo con la invención. La red 40 se observa que incluye primero, segundo y tercer transmisores de espectro disperso 42, 44 y 46 para procesar señales de información de banda base que van a transmitirse sobre canales de tráfico asociados con el primer (#1), segundo (#2) y tercero (#3) sectores de usuario. Un generador 50 de código largo PN proporciona el código PN largo utilizado por los transmisores 42, 44 y 46 al modular las señales de información transmitidas a cada sector de usuario. Las fases relativas de los códigos largos PN suministradas a los transmisores 42, 44 y 46 se desvían por márgenes predeterminados mediante elementos de retardo de fase 52 y 54. En la modalidad preferida los elementos de retardo de fase 52 y 54 proporcionan retardos aproximadamente equivalentes en duración a chips de 768 PN. Dentro de los transmisores 42, 44 y 46 las señales de información moduladas PN se utilizan para la modulación bifase de un par de cuadratura de sinusoides. Los sinusoides modulados se suman entonces, se filtran en paso de banda, se desplazan hacia una frecuencia portadora RF y se

proporcionan a los amplificadores de transmisión 58, 60 y 62. Las señales amplificadas producidas por los amplificadores 58, 60 y 62 comprenden las señales de información moduladas PN que van a proporcionarse mediante una portadora RF a los sectores de usuarios #1, #2 y #3, respectivamente. Las salidas de cada uno de los amplificadores 58, 60 y 62 se conectan respectivamente a redes divisoras de seis vías 66, 68 y 70. Como se indica en la Figura 2, las redes divisoras 66, 68 y 70 se acoplan a una matriz de conmutación 74.

Como se describe con mayor detalle en relación a la Figura 3, la matriz de conmutación 74 comprende una conexión conmutable entre la señal de información asociada con cada sector de usuario y un juego de seis manipuladores de antena 75-80. Es decir, la matriz de conmutación 74 permite que las señales de información provenientes de cada sector de usuario se enruten hacia usuarios que están dentro de cualquiera de las áreas de cobertura C1-C6. Los manipuladores de antena 75-80 están asociados con un juego de seis antenas de estación base 85-90, cada una de las antenas 85-90 funcionan para proyectar un haz sobre una de las áreas de cobertura C1-C6 (Figura 1A). Cada manipulador de antena 75-80 se observa además que incluye un nodo de suma de entrada 92. Los nodos de suma de entrada 92 están cada uno acoplados a la matriz de conmutación 74 a través

de un juego de tres líneas de señal de entrada, cada línea de señal lleva las señales de información moduladas PN que corresponden a cualquiera de los sectores de usuario #1, #2 ó #3.

Como se observó antes, en una modalidad preferida se introducen retardos entre las señales proyectadas hacia un par de áreas de cobertura adyacentes. En consecuencia, los manipuladores de antena 75-80 se observa que incluyen elementos de retardo 95a-95f capaces de proporcionar retardos ligeramente mayores que el período de chip del código PN proporcionado por el generador de código largo PN 50. En una modalidad preferida se designa que elementos de retardo alternos a los elementos de retardo 25a-25f (por ejemplo los elementos 95b, 95d y 95f) proporcionan un retardo ligeramente mayor a un solo período de chip PN, mientras que los elementos de retardo restantes (por ejemplo los elementos 95a, 95c y 95e) se omiten (retardo de cero). Los elementos de retardo 95a-95f podrían conceptualizarse usando uno o más filtros de onda acústica de superficie (SAW). Alternativamente, una fibra óptica en espiral de longitud predeterminada podría utilizarse para crear el retardo deseado. Cada manipulador de antena 75-80 podría también incluir un amplificador de energía 96 para proporcionar una señal de salida a una de las antenas 85-90.

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Haciendo referencia a la Figura 3, se muestra una representación ilustrativa de esa porción de la matriz de conmutación 74 que funciona para conectar de manera conmutable al divisor de seis vías 68 con cada uno de los manipuladores de antena 75-80. En particular, los atenuadores 97a-97f controlados digitalmente se interponen entre las salidas de los divisores 66 y los manipuladores de antena 75-80. Si, por ejemplo, se deseara que el primer sector de usuario abarcara áreas de cobertura C2-C4, entonces los atenuadores 97a, 97e y 97f podrían ajustarse a la atenuación máxima, mientras que los atenuadores 97b-97d podrían apagarse (es decir ajustarse para proporcionar una atenuación de cero). En una modalidad preferida la matriz de conmutación 74 incluye otros dos juegos de seis atenuadores digitales (no mostrados), prácticamente idénticos a los atenuadores 97a-97f, para conectar de manera conmutable los divisores 68 y 70 a los manipuladores de antena 75-80.

Los atenuadores 97a-97f de preferencia tendrían un intervalo dinámico de aproximadamente 30 dB, y serían capaces de ajustarse en incrementos de 1 dB. En esta forma, el haz proyectado a un área de cobertura particular podría extinguirse gradualmente, y después establecerse gradualmente una vez más, durante una transición entre las configuraciones de sector. Por ejemplo, si se deseara

modificar el alcance del primer sector de usuario de manera que se incluyeran solamente áreas de cobertura C3-C4 en lugar de las C2-C4, el atenuador 97b se ajustaría de manera incrementante de una atenuación cero a una atenuación máxima. Suponiendo que se deseara aumentar simultáneamente el alcance del segundo sector de usuario, el ajuste de un atenuador (no mostrado) conectado entre el segundo manipulador de antena 76 y el divisor 68 el sector cambiaría contemporáneamente de la atenuación máxima a la atenuación cero. Los atenuadores digitales 97a-97f son del tipo disponible de, por ejemplo, Anzac Corp., Parte NO. AT-210.

Aunque en la implementación de la Figura 3 la matriz de conmutación 74 se configura para permitir que cualquier sector de usuario abarque cualquier combinación de áreas de cobertura C1-C6, se entiende que en las modalidades alternas la matriz 74 podría suministrarse limitando el alcance potencial de tres a cuatro áreas de cobertura.

Haciendo referencia a las Figuras 1 y 2, cada una de las antenas 85 a 90 se diseña para proyectar una de 60 grados a una de las seis áreas de cobertura C1-C6. Se entiende, sin embargo, que la sectorización incrementada podría lograrse utilizando nueve antenas, cada una de las cuales se diseñaría para proyectar un haz de 40 grados.

Además, las antenas de modo dual capaces de proporcionar haces polarizados tanto horizontal como verticalmente podrían emplearse para ajustar hasta dos veces más usuarios dentro de cada área de cobertura. Como se describe abajo en relación a la Figura 4, los manipuladores de antena separados se utilizan para generar las señales proyectadas por cada haz polarizado horizontal y verticalmente.

Haciendo referencia a la Figura 4, se muestra un diagrama de bloques de una red 100 de transmisor de estación base, colocada para proporcionar la sectorización aumentada de usuarios al emplear tanto haces de antena polarizados horizontalmente como verticalmente. La red 100 que incluye primero, segundo y tercer pares de transmisores de espectro disperso 102a-102b, 104a-104b y 106a-106b, para procesar señales de información de banda base que van a transmitirse sobre primero (#1a-b), segundo (#2a-b) y tercero (#3-b) juegos pareados de canales de tráfico asociados con un juego correspondiente de tres sectores de usuario. Como se describe abajo, los juegos de canales de tráfico #1a, #2a y #3a pueden proyectarse selectivamente a cada área de cobertura usando haces polarizados horizontalmente, mientras que los canales de tráfico #1b, #2b y #3b pueden proyectarse de manera similar y selectiva utilizando haces polarizados verticalmente. Un generador de código largo PN (no mostrado) proporciona el código PN

largo utilizado por los transmisores 102a-102b, 104a-104b y 106a-106b al modular las señales de información transmitidas a cada sector de usuario. Una vez más, las fases relativas de los códigos largos PN suministrados a los transmisores 102a-102b, 104a-104b y 106a-106b se desvían por márgenes de fase equivalentes a un número predeterminado de chips PN.

Dentro de los transmisores 102a-102b, 104a-104b y 106a-106b las señales de información modulada PN se utilizan para modular en bifase un par de cuadratura de sinusoides. Los sinusoides modulados son entonces sumados, filtrados en paso de banda, desplazados a una frecuencia portadora RF y amplificados. Las salidas de cada uno de los transmisores 102a-102b, 104a-104b y 106a-106b se conectan respectivamente a redes divisoras de seis vías 112a-112b, 114a-114b y 116a-116b. Como se indica en la Figura 4 las redes divisoras 112a-112b, 114a-114b y 116a-116b se acoplan a una matriz de conmutación 120.

La matriz de conmutación 120 proporciona una conexión conmutable entre las señales de información transmitidas sobre los juegos pareados de canales de tráfico (por ejemplo #1a y #1b) de cada sector de usuario en un juego de seis manipuladores de antena 125a-125b hasta 130a-130b. La aplicación de la salida de cada manipulador de antena 125a-130a a las antenas 135-140 da por resultado

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la proyección de haces polarizados horizontalmente hacia las áreas de cobertura C1-C6, mientras que la aplicación de la salida de cada manipulador de antena 125b-130b a las antenas 135-140 da por resultado la proyección de un haz polarizado verticalmente a cada una de las áreas de cobertura C1-C6. Como se indica por la Figura 4, la matriz de conmutación 120 está configurada de manera que los dos juegos de usuarios asociados con cada sector de usuario quedan tener servicio dentro de cada una de las áreas de cobertura C1-C6.

Haciendo referencia a la Figura 4, se muestra una representación ilustrativa de la porción de la matriz de conmutación 120 que funciona para conectar conmutablemente los divisores de seis vías 112a-b a cada uno de los manipuladores de antena 125a-b hasta 130a-b. En particular, los atenuadores controlados digitalmente 142 y 144 se interponen entre las salidas de los divisores de seis vías 112a-b y cada uno de los manipuladores de antena 125a-b hasta 130a-b. En una modalidad preferida, la matriz de conmutación 120 incluye otros dos juegos de doce atenuadores digitales (no mostrados) para conectar conmutablemente los divisores 114a-114b y 116a-116b hacia los manipuladores de antena 125a-125b hasta 130a-130b.

Cada par de manipuladores de antena (por ejemplo los manipuladores 125a-b) está conectado a una de las seis

antenas de estación base 135-140, cada antena 135-140 funciona para proyectar un haz polarizado horizontalmente y un haz polarizado verticalmente sobre una de las áreas de cobertura C1-C6 (Figura 1A). Como se observó antes, en una modalidad preferida los retardos se introducen entre las señales proyectadas hacia un par de áreas de cobertura adyacentes. Consecuentemente, los pares alternos de manipuladores de antena (por ejemplo manipuladores 105a-b, 107a-b) se colocan para proporcionar retardos ligeramente más largos que un período de chip PN simple. En otros aspectos los manipuladores de antena 105a-105b hasta 110a-110b son substancialmente similares a los manipuladores de antena 75-80.

Las Figuras 5A y 5B proporcionan respectivamente las vistas superior y lateral de una antena provisional resonante de modo dual capaz de conceptualizar las antenas 135-140. El elemento provisional 160 mostrado en la Figura 5A es de la mitad de la longitud de onda portadora en cada dimensión y se suspende por arriba de un plano de tierra 162 (Figura 5B) mediante un poste 163. El elemento provisional 160 se observa separado del plano de tierra 162 en una distancia de separación S. En la modalidad preferida la distancia S se selecciona de manera que se proporcione suficiente anchura de banda para expandir tanto las bandas de frecuencia de transmisión como de recepción.

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El modo polarizado verticalmente se crea mediante la resonancia del elemento provisional 160 de manera que los máximos de voltaje se presentan en forma próxima a los bordes superior e inferior 170 y 172 del elemento provisional 160, y de manera que se presentan un voltaje nulo en la sección media. En forma similar, el modo polarizado horizontalmente se crea haciendo resonar el elemento provisional 160 de manera que los máximos de voltaje surjan en los bordes izquierdo y derecho 176 y 178 del elemento provisional 160. En una modalidad preferida, el modo polarizado verticalmente se excita mediante una sonda de voltaje aplicada al centro de los bordes superior 170 e inferior 172 del elemento provisional 160. En forma semejante el modo horizontal se induce utilizando sondas de voltaje conectadas a los bordes derecho e izquierdo 176 y 178.

III. Sectorización Dinámica Dentro de una Red de Recepción.

Haciendo referencia a la Figura 6, se muestra una representación diagramática en bloques de una red receptora 200 de estación base configurada para proporcionar la sectorización dinámica de usuarios de acuerdo a la invención. La red 200 se observa generalmente como complementaria a la red transmisora 40 (Figura 3) ya que se

introduce un retardo de descorrelación entre las señales recibidas desde las áreas de cobertura adyacentes. La red receptora 200 y la red transmisor 40 pueden acoplarse simultáneamente a las antenas 85-90 a través de un duplexor (no mostrado).

Las señales recibidas de las áreas de cobertura C1-C6 a través de las antenas 85 a 90 se proporcionan respectivamente para recibir amplificadores 210-215. Los amplificadores de recepción 210-215 incluyen cada uno un amplificador de bajo ruido (LNA) 220 que tiene una banda de paso centrada aproximadamente en la frecuencia de la portadora RF recibida. Los amplificadores 210-215 se observan además incluyendo elementos de retardo 225a-225f capaces de proporcionar retardos ligeramente mayores al período de chip del código largo PN utilizado para hacer la discriminación entre los sectores de usuario. En una modalidad preferida, se designan elementos alternantes a los elementos de retardo 225a-225f (por ejemplo los elementos 225b, 225d y 225f) para proporcionar un retardo ligeramente mayor a un solo período de chip PN, mientras que los elementos de retardo restantes se omiten (retardo de cero). Los elementos de retardo 225a-225f podrían conceptualizarse utilizando uno o más filtros de onda acústica superficial (SAW). Alternativamente, una fibra óptica en espiral de longitud predeterminada podría

utilizarse para crear el retardo deseado.

La salida de cada elemento de retardo 225a-225f se proporciona hacia un divisor de 3 vías 230 conectado a una matriz de conmutación 232. La matriz de conmutación 232 es esencialmente idéntica a la matriz de conmutación 74, y por lo tanto proporciona una conexión conmutable entre cada salida de los divisores de 3 vías 230 y una entrada hacia uno de las tres redes sumadoras de 6 vías 240-242. Las redes sumadoras 240-242 se acoplan a un juego correspondiente de tres receptores de diversidad 250-252 a través de los amplificadores 254-256, cada receptor de diversidad es capaz de implementarse en la forma descrita abajo en relación a la Figura 10. Cada receptor de diversidad 250-252 hace la conversión descendente en frecuencia y digitaliza la señal recibida en componentes compuestos I y Q. Los componentes compuestos I y Q se demodulan, combinan, desintercalan y decodifican.

Cada componente I y Q puede estar comprendido de señales de datos provenientes de una unidad de suscriptor dada recibida por dos o más de las antenas 88-90 asociadas con las áreas de cobertura adyacentes C1-C6 de un monitor de usuario dado. Las señales recibidas asociadas con cada área de cobertura, como se selecciona por un receptor buscador en combinación con un controlador, se procesan cada uno por un receptor o modulador diferente a los

múltiples receptores o demoduladores de datos, a los que también se hace referencia como "dedos" (no mostrados). A partir de los componentes compuestos I y Q cada dedo extrae, por desdispersión, a los componentes I y Q, RI y RQ de las señales de datos y las señales piloto asociadas con cada área de cobertura. Un generador de código largo PN 260 proporciona el código PN largo utilizado por los receptores 250-252 para demodular las señales de información recibidas desde cada sector de usuario. Las fases relativas de los códigos largos PN suministrados a los receptores 251-252 se desvían en márgenes predeterminados por elementos de retardo de fase 270 y 272. En la modalidad preferida los elementos de retardo de fase 52 y 54 proporcionan retardos aproximadamente equivalentes en duración a los chips PN 768.

IV. Sectorización Dinámica Dentro de un Sistema CDMA

Haciendo referencia a la Figura 7, se muestra una representación diagramática en bloques de un transmisor de espectro disperso adecuado para conceptualizar los transmisores de espectro disperso 42, 44 y 46 (Figura 2). El transmisor de espectro disperso de la Figura 7 es del tipo descrito en la Patente de los Estados Unidos NO. 5,103,459 emitido en 1992 y titulada *"System and Method for Generating Signal Waveforms In a CDMA Cellular Telephone*

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System", cedida a la titular de la presente invención, y que se incorpora aquí por referencia. En el transmisor de la Figura 7, los bits de datos 300 consisten, por ejemplo, de voz convertida en datos por un vocodificador, y que se suministran a un codificador 302 en donde los bits se codifican convolucionalmente con la repetición de símbolo código de acuerdo con la velocidad de datos de entrada. Cuando la velocidad de bit de datos es menor a la velocidad de procesamiento de bit del codificador 302, la repetición del símbolo código dicta que el codificador 302 repita los bits de datos de entrada 300 con objeto de crear una corriente de datos repetitiva a una velocidad de bits que coincide con la velocidad operativa del codificador 302. Los datos del codificador se proporcionan entonces al intercalador 304 en donde se intercala en forma convolucional. Los datos de símbolo intercalados salen del intercalador 304 a una velocidad ejemplo de 19.2 ksps a una entrada O-exclusiva 306.

En el sistema de la Figura 7 los símbolos de datos intercalados se mezclan para proporcionar una mayor seguridad en las transmisiones sobre el canal. El mezclado de las señales de canal de voz puede lograrse por codificación de pseudoruido (PN) de los datos intercalados con un código PN específico hacia una unidad de suscriptor recipiente pretendida. Estos códigos de mezclado

comprenden los códigos PN "internos" a los cuales se hace referencia en la sección de antecedentes de la invención. Estos mezclados PN pueden proporcionarse por el generador PN 308 utilizando un esquema de cifrado o secuencia PN. El generador PN 308 incluirá típicamente un generador PN largo para producir un código PN único a una velocidad fija de 1.2288 MHz. Este código PN se hace pasar entonces a través de un decimador (no mostrado) con la secuencia de mezclado resultante de 9.2 MHz suministrándose a otra entrada del O exclusivo 306 de acuerdo con la información de identificación de la unidad del suscriptor proporcionada al mismo. La salida O-exclusiva 306 se proporciona a una entrada O-exclusiva 310.

Otra vez haciendo referencia a la Figura 7, la otra entrada de la compuerta O-exclusiva 310 se conecta a un generador de código Walsh 312. El generador Walsh 312 generá una señal que corresponde a la secuencia Walsh asignada al canal de datos sobre el cual se está transmitiendo la información. El código Walsh proporcionado por el generador 312 se selecciona a partir de un juego de 64 códigos Walsh de longitud 64. Los 64 códigos ortogonales corresponden a los códigos Walsh de una matriz Hadamard de 64 por 64, en donde un código Walsh es una sola hilera o columna de la matriz. Los datos de símbolo mezclados y el código Walsh se hacen pasar por la

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compuerta O-exclusiva 310 siendo el resultado una entrada hacia las dos compuertas O-exclusivas 314 y 316.

La compuerta O-exclusiva 314 recibe también una señal PN_I, mientras que la otra entrada de la compuerta O-exclusiva 316 recibe una señal PN_Q. En aplicaciones CDMA, el generador de código largo PN 50 (Figura 2) opera para proporcionar las dos secuencias PN_I y PN_Q a los transmisores de espectro disperso 42, 44 y 46. Las señales PN_I y PN_Q son señales pseudoaleatorias (PN) que corresponden a un sector de usuario particular cubierto por el sistema CDMA y que se relaciona respectivamente con los canales de comunicación de en fase (I) y en cuadratura (Q). Las señales PN_I y PN_Q respectivamente se hacen pasar por una compuerta O-exclusiva con la salida de la compuerta O-exclusiva 310 a fin de dispersar adicionalmente los datos de usuario antes de la transmisión. La secuencia de dispersión 322 de código de canal I resultante y la secuencia de dispersión 326 de código de canal Q se utilizan para modular en bi-fase un par en cuadratura de sinusoides. Cada par en cuadratura de sinusoides se suma dentro de los transmisores 42, 44 y 46, se desplaza a una frecuencia RF y se proporciona a uno de los amplificadores 58, 60 y 62.

En la modalidad preferida, un canal piloto que no contiene modulación de datos se transmite junto con las

secuencias de dispersión S_I y S_Q de los canales I y Q. El canal piloto puede caracterizarse como una señal de espectro disperso no modulada que se utiliza para fines de rastreo y adquisición de señale. En sistemas que incorporan una pluralidad de transmisores de estación base en células adyacentes, el juego de canales de comunicación proporcionado por cada uno se identificará por una señal piloto única. Sin embargo, en lugar de utilizar un juego separado de generadores PN para las señales piloto, se entiende que un enfoque más eficiente para generar un juego de señales pilotos es utilizar desplazamientos en la misma secuencia base. La utilización de esta técnica hace que una unidad receptora destinada busque secuencialmente la totalidad de la secuencia piloto y se sintonice a la desviación o desplazamiento que produce la correlación más fuerte.

En consecuencia, la secuencia piloto de preferencia será lo suficientemente larga para que muchas secuencias diferentes puedan generarse por desplazamientos en la secuencia básica para soportar un gran número de señales piloto en el sistema. Además, la separación o desplazamiento debe ser suficientemente grande para asegurar que no haya interferencia en las señales piloto. Por lo tanto, en una modalidad ejemplaria la longitud de la secuencia piloto se selecciona para sea de 2^{15}, lo que

permite 512 señales piloto distintas que se derivan de una secuencia básica de 64 chips.

Haciendo referencia a la Figura 8, una red de generación piloto 330 incluye un generador Walsh 340 para proporcionar la secuencia Walsh W_0 "cero" que consiste de todos los ceros hacia los combinadores O-exclusivos 344 y 346. La secuencia Walsh W_0 se multiplica por las secuencias PN_I y PN_Q utilizando los combinadores O-exclusivos 344 y 346 respectivamente. Como la secuencia W_0 incluye solamente ceros, el contenido de información de las secuencias resultantes depende solamente de las secuencias PN_I y PN_Q. Las secuencias producidas por los combinadores O-exclusivos 344 y 346 se proporcionan como entradas a los Filtros de Respuesta de Impulso Finito (FIR) 350 y 352. La salida de las secuencias filtradas proveniente de los filtros FIR 350 y 352, corresponde respectivamente a las secuencias piloto P_I y P_Q de los canales I y Q, y se suministra a los transmisores RF 382.

Haciendo referencia a la Figura 9, se muestra una implementación ejemplo del transmisor RF 382. Los transmisores 382 incluyen un sumador de canal I 370 para sumar las señales de datos dispersos PM_I, S_{Ii}, i=1 hasta N, con el piloto P_I de canal I. En forma similar un sumador de canal Q 372 sirve para combinar las señales de datos dispersos PM_Q, S_{Qi}, i=1 a N, con el piloto P_I de canal Q.

Los convertidores digital a analógico (D/A) 374 y 376 se proporcionan para convertir la información digital de los sumadores de canal I y canal Q 370 y 372, respectivamente a la forma analógica. Las formas de onda analógica producidas por los convertidores D/A 374 y 376 se proporcionan junto con las señales de frecuencia portadora de oscilador local (LO), Cos(2πft) y Sen(πft), respectivamente, a los mezcladores 388 y 390 en donde se mezclan y proporcionan al sumador 392. Las señales portadoras de fase en cuadratura Sen(πft) y Cos(2πft) se proporcionan a partir de fuentes de frecuencia adecuadas (no mostradas). Estas señales IF se suman en el sumador 392 y se proporcionan al mezclador 394.

El mezclador 394 mezcla la señal sumada con una señal de frecuencia RF a partir del sintetizador de frecuencia 396 a fin de proporcionar la conversión ascendente en frecuencia a la banda de frecuencia RF. La señal RF incluye componentes en fase (I) y en cuadratura (Q), y se filtra en paso de banda por el filtro de paso de banda 398 y sale a uno de los amplificadores RF 58, 60, 62 (Figura 2). Debe entenderse que el transmisor RF 382 puede emplear diferentes implementaciones con una variedad de técnicas de sumado, mezclado, filtrado y amplificación de señal que no se describen aquí, pero que son bien conocidas en este campo.

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La Figura 10 es un diagrama de bloques de un receptor de diversidad ejemplo asociado con una de las unidades de suscriptor 12 (Figura 1A), y por lo tanto se coloca para recibir las señales RF transmitidas por uno o más de las antenas 85-90 de la estación base 40 (Figura 2). En la Figura 10 la señal RF transmitida por la estación base 40 es recibida por la antena 410 y proporcionada a un receptor RAKE de diversidad que está comprendido del receptor analógico 412 y el receptor digital 414. La señal como es recibida por la antena 410 y proporcionada al receptor analógico 412 puede estar comprendida de propagaciones de trayectoria múltiple de las mismas señales piloto y de datos destinadas para los receptores de suscriptor individuales o múltiples. Los receptores analógicos 412, que se configuran en la modalidad ejemplo como un modem QPSK, se convierte en forma descendente en frecuencia y digitaliza la señal recibida a los componentes compuestos I y Q. Los componentes compuestos I y Q se proporcionan al receptor digital 414 para la demodulación. Los datos demodulados son proporcionados entonces a la circuiteria digital 416 para la combinación, desintercalación y decodificación.

Cada salida de los componentes I y Q provenientes del receptor analógico 412 puede estar comprendida de señales de datos correspondientes transmitidas por dos o

más de las antenas 85-90 asociadas con las áreas de cobertura adyacentes C1-C6 de un sector de usuario dado. Como se discutió antes, una desviación de fase se introduce entre las señales de datos proporcionadas a las áreas de cobertura adyacentes en un sector de usuario particular. En el receptor digital 414 las señales recibidas asociadas con cada área de cobertura, según se selecciona por un receptor buscador 415 en combinación con un controlador 418, se procesan cada uno por un receptor o demodulador de los varios receptores o demoduladores de datos 420a-420c, a los que también se hace referencia como "dedos". Aunque solo tres de los dedos demoduladores de datos (demoduladores 420a-420c) se ilustran en la figura 10, debe entenderse que pueden utilizarse más o menos dedos. A partir de los componentes compuestos I y Q, cada dedo extrae, por desdispersión, los componentes I y Q PI y PQ de las señales piloto y de datos, asociados con cada área de cobertura.

En una implementación ejemplo, cada unidad de suscriptor 12 es asignada a uno de un juego de 64 códigos Walsh ortogonales W_i de longitud 64. Esto permite que un juego de canales que incluyen a un canal piloto, 63 canales I y 63 canales Q se transmiten utilizando un par dado de secuencias de dispersión PN_I y PN_Q. La señal piloto extraído se utiliza para alinearse en tiempo dentro de un

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combinador de símbolo (no mostrado) dentro del receptor de la unidad de suscriptor. Cuando la unidad de suscriptor se coloca en forma próxima al límite de las áreas de cobertura adyacentes asignadas al mismo sector de usuario, los cálculos de los datos admitidos a cada área de cobertura se alinean en tiempo y se adicionan conjuntamente, mejorando así la proporción señal a ruido.

V. Sectorización Dinámica Utilizando Patrón de Haz en Fase.

Como se discutirá antes, en la modalidad preferida se introduce un retardo entre los haces proyectados a áreas de cobertura de antena adyacentes a fin de descorrelacionar las señales transmitidas a cada área. Este enfoque se diseña para eliminar prácticamente toda interferencia destructiva entre los haces proporcionados a áreas de cobertura adyacentes, evitando así la formación de señales nulas y otras distorsiones del patrón de haz. Un receptor de diversidad asociado con una unidad suscriptora colocado cerca del límite del área de cobertura puede por lo tanto recibir de manera separada las señales descorrelacionadas, y subsecuentemente combinar las señales recibidas en forma separada.

En una modalidad alterna de la invención la estación base celular se diseña para efectuar la

sectorización dinámica de usuarios proporcionando un juego de haces fijos proyectados en alineamiento preciso de fase. Haciendo referencia a la Figura 11A, se muestra el patrón de azimuth de un haz fijo de 40 grados que se supone se proyecta mediante una primera antena de estación base asociada con una de las áreas de cobertura C1-C6 (Figura 1A). Si una segunda antena de estación base, dispuesta para proporcionar un segundo haz fijo de 40 grados a un área de cobertura adyacente es manipulada en fase con la primera antena de estación base, el patrón mostrado en la Figura 11B se produce. Por lo tanto es evidente que la anchura de un sector de usuario puede aumentarse en proporción al número de haces excitados. Como los haces se generan en fase, los haces interfieren constructivamente cerca de los límites del área de cobertura y por lo tanto se combinan efectiva y coherentemente dentro del sector base en lugar de dentro del receptor de la unidad de suscriptor.

Haciendo referencia a la Figura 12, se muestra una representación diagramática de bloque de una red de transmisor 440 de estación base configurada para proporcionar la sectorización dinámica de usuarios proyectando un juego de haces en fase a cada sector de usuario. La red 440 se observa prácticamente similar a la red de la Figura 2, en donde se utilizan números iguales

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para identificar componentes similares del sistema. En lugar de incluir elementos de retardo de fase 95a-95f, los manipuladores de antena 75-80 incluyen ecualizadores de fase 444a-444f ajustados de manera que las antenas 85-90 sean manipuladas en fase. El ajuste de los ecualizadores 444a-444f puede efectuarse, por ejemplo, durante la instalación de la estación base aplicando una señal de prueba idéntica a cada manipulador 75-80.

Más específicamente, durante un proceso de calibración se proporciona un juego de señales de prueba de amplitud y fase idénticas hacia los manipuladores de antena 75-80. La salida de los pares adyacentes de cables de antena 445a-445f, respectivamente, asociada con las antenas 85-90, se conectan entonces a los portillos de entrada dual de un combinador de energía. El ecualizador de fase dentro de los impulsores de antena acoplados a uno de los cables de antena se ajusta entonces hasta que la salida del combinador de energía se aumente al máximo. Este procedimiento se repite para cada par adyacente de manipuladores de antena, es decir para manipuladores 75 y 76, los manipuladores 76 y 77, y así sucesivamente.

Un procedimiento análogo se utiliza para calibrar la red de recepción 200 (Figura 6). En particular, un juego de señales de prueba de amplitud y fase idénticas que inyectan en los portillos de los cables de antena 224a-224f

acoplados nominalmente a las antenas 85-90. Un combinador de energía que tiene seis portillos de entrada y un solo portillo de salida se conecta entonces a los divisores 230 de un par adyacente de amplificadores de recepción 210-215. Un ecualizador de fase (no mostrado) dentro de uno de los amplificadores de recepción conectado al combinador de energía, se ajusta entonces hasta que la energía de salida del combinador aumenta al máximo. Este proceso se repite para cada par adyacente de amplificadores de recepción 210-215.

La Figura 13 ilustra una configuración 450 de estación de base alternativa para proporcionar sectorización dinámica de usuarios al proyectar un juego de haces en fase. Como se indica en la Figura 13, el alineamiento de fase se mantiene entre haces adyacentes colocando la matriz de conmutación y los manipuladores de antena en forma próxima a las antenas 85-90. Es decir, en la configuración de la Figura 13, la matriz de conmutación 74 y los manipuladores de antena 85-90, le seguirán a los cables de transmisión 452-454, en lugar de precederlos, dentro de la torre de antena 458 de estación base. El acoplamiento directo de los manipuladores 75-80 a las antenas 85-90 evita ventajosamente que las diferencias de fase que se deben a la variación y a la longitud del cable y semejantes, se introduzcan entre los haces transmitidos a

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las áreas de cobertura adyacentes.

VI. Subsistema de Antena

En las dos modalidades tanto de la fase descorrelacionada como de la fase controlada de la invención (ver por ejemplo las Figuras 2 y 12), el tamaño de un sector de usuario dado varía utilizando una combinación de uno o más haces para proporcionar la señal de información para el sector. Cada uno de estos haces puede crearse utilizando cualquiera de un número de técnicas convencionales. Por ejemplo un juego de antenas de haz fijo distintas podrían utilizarse para proyectar un juego de haces de ángulo predeterminado. En este enfoque, las antenas se montan y alinean de manera que cada haz abarca un área de cobertura predeterminada. En una modalidad ejemplo un juego de seis antenas se utilizan para proporcionar un haz de 60 grados a cada una de las seis áreas de cobertura (ver por ejemplo Figura 1A).

Alternativamente, una antena de arreglo en fase puede utilizarse para formar simultáneamente más de un solo haz. Por ejemplo, la Figura 14 muestra un arreglo triangular de paneles de antena de arreglo en fase, primero, segundo y tercero, 480, 482 y 484, que colectivamente operan para proporcionar un juego de nueve haces de antena a las áreas de cobertura C1-C9. En

particular, el panel de antena 480 proyecta tres haces fijos de 40 grados para las áreas de cobertura C1-C3, mientras que los paneles de antena 482 y 484 proyectan haces fijos de 40 grados para las áreas de cobertura C4-C6 y C7-C9, respectivamente.

Como se indica en la Figura 15, una implementación preferida de la cara de cada panel de antena incluye un arreglo de 4x4 de elementos provisionales, los elementos dentro de cada columna se identifican respectivamente con los números de referencia 486 a 489. Suponiendo una frecuencia portadora RF de 850 MHz, cada elemento provisional puede fabricarse a partir de una sección cuadrada de un material provisional cargado dialéctricamente con un área de 4 pulgadas^2. Esto da por resultado en cada panel de antena cuadrada 482-484 un área de aproximadamente 4 pies cuadrados.

Haciendo referencia a la Figura 16, se muestra una antena de arreglo en fase y una red formadora de haz 490, colocada para proporcionar tres haces de una sola cara de antena. Una matriz de conmutación (no mostrada) proporciona las señales de información que corresponden a los sectores de usuario #1, #2 y #3 mediante las líneas de señal de entrada 494a-494c. La red formadora de haz 490 incluye divisores de 4 vías 495a-c, respectivamente conectados a las líneas de señal 494a-c. Las cuatro

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salidas de cada divisor 455a-c están conectadas mediante elementos de retardo de fase 496 a uno de cuatro nodos de suma 498-501. Las señales compuestas provenientes de los nodos de suma 498-501 se proporcionan respectivamente a amplificadores de potencia 504-507. Como se indica en la Figura 16, cada columna de elementos de arreglo 486-489 es manipulada por uno de los amplificadores 504-507. En implementaciones alternas se utiliza un amplificador de energía separado para manipular cada elemento de arreglo 486-489.

En una modalidad ejemplo los elementos de retardo 496 se ajustan de manera que cada uno de los tres haces se proyectan a un ángulo de 40 grados a una de las tres áreas de cobertura adyacentes. Los tres haces proyectados por un solo panel de antena expandirían entonces en un arco de 120 grados. Tres de estos paneles podrían montarse para proporcionar un juego de nueve haces que abarquen un arco de 360 grados.

La descripción anterior de las modalidades preferidas se proporciona para permitir a cualquier persona con pericia normal en este campo elaborar o utilizar la presente invención. Las diversas modificaciones a estas modalidades se harán evidentes para los expertos en este campo y los principios genéricos definidos aquí pueden aplicarse a otras modalidades sin el uso de la facultad

inventiva. De esta manera, la presente invención no pretende limitarse a las modalidades aquí mostradas sino que tiene el alcance más amplio consistente con los principios y particularidades novedosas que se revelan aquí. Por ejemplo, además de dirigirse a la necesidad de la asignación de canales de tráfico flexibles como consecuencia de los cambios a corto término en la demanda de los usuarios, el método y el aparato de la invención pueden emplearse para ajustarse a cambios a largo término en la demanda de los usuarios. Estas variaciones a largo término en la demanda podrían estar acompañadas, por ejemplo, de desplazamiento en la distribución de la población y en los patrones de construcción dentro de un área geográfica dada.

NOVEDAD DE LA INVENCIÓN

Habiendo descrito el presente invento, se considera como una novedad y, por lo tanto, se reclama como propiedad lo contenido en las siguientes

REIVINDICACIONES:

1. Un sistema para transportar información a por lo menos un usuario en un sistema de comunicación de espectro disperso, que comprende:

un medio para generar, a una velocidad de chip predeterminada, una primera señal de ruido pseudoaleatorio (PN) de un primer código PN predeterminado;

un primer medio para combinar la primera señal PN y una primera señal de información y para proporcionar una primera señal de modulación resultante;

un medio para proporcionar una segunda señal de modulación haciendo retardar la primera señal de modulación en un primer retardo predeterminado que se relaciona inversamente a la velocidad de chip;

un medio para transmitir selectivamente la primera y la segunda señales de modulación respectivamente a la primera y la segunda áreas de cobertura;

mediante lo cual la transmisión selectiva de la primera y la segunda señales de modulación da por resultado la variación en tamaño de un primer sector de usuario en donde se incluye el por lo menos un usuario.

2. El sistema según la reivindicación 1, en donde el medio para transmitir selectivamente incluye medios para transmitir la primera y la segunda señales de modulación de manera que la segunda área de cobertura traslape por lo menos parcialmente a la primera área de cobertura.

3. El sistema según la reivindicación 2, que incluye además:

un medio para proporcionar una tercera señal de modulación y para proporcionar una cuarta señal de modulación que corresponde a una versión retardada de la tercera señal de modulación;

un medio para transmitir selectivamente la tercera y la cuarta señales de modulación respectivamente a la segunda área de cobertura y a la tercera área de cobertura;

mediante lo cual la transmisión selectiva de la tercera y la cuarta señales de modulación da por resultado la variación en tamaño de un segundo sector de usuario.

4. El sistema según la reivindicación 2, en donde el sistema incluye además:

un medio para generar, a una velocidad de chip predeterminada, una segunda señal de ruido pseudoaleatorio del código PN predeterminado, la primera y la segunda señales PN se desvían en fase,

un segundo medio para combinar la segunda señal PN en una segunda señal de información y para proporcionar una tercera señal de modulación resultante, y

un medio para proporcionar una cuarta señal de modulación al retardar la tercer señal de modulación en un retardo predeterminado que está inversamente relacionado con la velocidad de chip predeterminada.

5. El sistema según la reivindicación 4, en donde el medio para transmitir selectivamente incluye un medio para transmitir selectivamente la primera y la segunda señales de modulación respectivamente a la primera y la segunda áreas de cobertura, exclusivamente durante un primer período de operación del sistema, y para transmitir selectivamente la tercera y la cuarta señales de modulación respectivamente a la primera y la segunda áreas de cobertura, exclusivamente durante un segundo período de operación del sistema.

6. El sistema según la reivindicación 1, que incluye además un receptor para recibir la primera y la segunda señales de modulación y para proporcionar la primera señal de información al por lo menos un usuario con base en la misma.

7. El sistema según la reivindicación 6, en donde el receptor incluye medios para generar una replica del código PN, y medios para demodular la primera y la

segunda señales moduladas, dando una primera y una segunda señales demoduladas que utilizan la replica del primer código PN.

8. El sistema según la reivindicación 7, en donde el receptor incluye medios para combinar coherentemente la primera y la segunda señales demoduladas.

9. En un sistema de comunicación de suscriptor celular en donde los usuarios que están dentro de por lo menos una célula se comunican señales de información entre sí mediante por lo menos un sitio celular que utiliza señales de comunicación de espectro disperso, en donde ese sitio celular incluye un transmisor de sitio celular, el transmisor comprende:

un primer medio para proporcionar primero y segundo juegos de señales de información de espectro disperso para transmitirse a los usuarios dentro de un primer sector de usuario de la primer célula, el medio para proporcionar incluye un medio para generar el segundo juego de señales de información de espectro disperso retardando cada una de las señales de información incluidas dentro del primer juego; y

un primer medio para transmitir selectivamente, durante un primer periodo de funcionamiento del sistema, al primero y al segundo juegos de señales de información de espectro disperso respectivamente hacia la primera y la

segunda áreas de cobertura dentro de la por lo menos una célula, en donde el tamaño del primer sector de usuario varía a través de la transmisión selectiva del primero y segundo juegos de señales de información de espectro disperso.

10. El sistema según la reivindicación 9, en donde el primer medio para transmitir selectivamente incluye primera y segunda antenas para proyectar primero y segundo haces sobre la primera y segunda áreas de cobertura, respectivamente, el primer haz lleva el primer juego de señales de información de espectro disperso y el segundo haz lleva el segundo juego de señales de información de espectro disperso.

11. El sistema según la reivindicación 10, en donde el primer medio para proporcionar incluye medios para dividir cada una de las señales de información incluidas dentro del primer juego en un par de subseñales idénticas y para retardar una de las subseñales de cada par.

12. El transmisor según la reivindicación 11, caracterizado porque el medio para transmitir selectivamente incluye:

un medio para atenuar selectivamente cada una de las subseñales, y

un medio para acoplar una de las subseñales dentro de cada par de la primera antena y para acoplar la

otra de las subseñales dentro de cada par de la segunda antena.

13. El transmisor según la reivindicación 9, que incluye además:

un segundo medio para proporcionar tercero y cuarto juegos de señales de información de espectro disperso para su recepción por los usuarios dentro de un segundo sector de usuario de la primera célula, el segundo medio para proporcionar incluye medios para generar el cuarto juego de señales de información de espectro disperso retardando cada una de las señales de información incluidas dentro del tercer juego;

un segundo medio para transmitir selectivamente, durante un segundo periodo de operación del sistema, al tercero y cuarto juegos de señales de información de espectro disperso respectivamente hacia la primera y la segunda área de cobertura dentro de la por lo menos una célula, permitiendo así que el tamaño de un segundo sector de usuario incluido dentro de la por lo menos una célula varíe de acuerdo con la concentración de usuario en el segundo sector.

14. El sistema según la reivindicación 9, que incluye además un receptor, el receptor comprende:

medios para recibir una de las señales de información incluidas dentro del primer juego y para

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recibir una versión retardada de la señal de información incluida dentro del segundo juego;

un medio para combinar coherentemente las señales de información recibidas y para proporcionar la señal resultante a un usuario del sistema.

15. Un sistema para transportar información a por lo menos un usuario en un sistema de comunicación de espectro disperso, que comprende:

medios para generar una primera señal de ruido pseudoaleatorio (PN) de un primer código PN predeterminado;

un primer medio para combinar la primera señal PN y una primera señal de información y para proporcionar una primera señal de modulación resultante;

un medio para proporciona una segunda señal de modulación replicando la primera señal de modulación;

un medio para alinear la primera y la segundas señales de modulación en fase, y para transmitir selectivamente la primera y la segunda señales de modulación alineadas en fase resultantes, respectivamente a la primera y a la segunda área de cobertura;

mediante lo cual la transmisión selectiva de la primera y la segunda señales de modulación da por resultado una variación en tamaño de un primer sector de usuario en el que está incluido por lo menos un usuario.

16. El sistema según la reivindicación 15, en

donde el medio para transmitir selectivamente incluye medios para permitir selectivamente la primera y la segunda señales de modulación, respectivamente hacia primera y segunda áreas de coberturas exclusivamente durante un primer periodo de operación del sistema, y para transmitir selectivamente tercera y cuarta señales de modulación respectivamente a la primera y segunda áreas de cobertura, exclusivamente durante un segundo periodo de operación del sistema, la tercer señal de modulación es esencialmente idéntica a la cuarta señal de modulación y está alineada en fase con la misma.

17. Un sistema de comunicación de suscriptor celular en donde los usuarios dentro de por lo menos una de las señales de información de comunicación celular entre ellos mediante por lo menos un sitio celular que utiliza señales de comunicación de espectro de dispersión en donde ese sitio celular incluye un transmisor de sitio celular, el transmisor comprende:

primeros medios para proporcionar el primero y el segundo juegos de señales de información de espectro de dispersión para ser recibidas por los usuarios dentro de un primer sector de usuario de la primera célula, el medio para proporcionar incluye medios del segundo juego de señales de información de espectro disperso replicando cada una de las señales de información dentro del primer juego;

un medio para alinear en fase cada una de las señales de información dentro del primer juego con las correspondientes réplicas de las mismas dentro del segundo juego a fin de formar primero y segundo juegos de las señales de información alineadas en fase;

un primer medio para transmitir selectivamente, durante un primer periodo de operación del sistema, el primero y el segundo juegos de señales de información alineadas en fase, respectivamente a la primera y a la segunda áreas de cobertura dentro de la por lo menos una célula, en donde el tamaño del primer sector de usuario varía a través de la transmisión selectiva del primero y segundo juegos de señales de información alineadas en fase.

18. Un método para transportar información a por lo menos un usuario en un sistema de comunicación de espectro disperso, que comprende de:

generar a una velocidad de chip predeterminada, una primera señal de ruido pseudoaleatorio (PN) de un primer código PN predeterminado;

combinar la primera señal PN y una primera señal de información, y para proporcionar una primera señal de modulación resultante;

proporcionar una segunda señal de modulación al retardar la primera señal de modulación en un retardo predeterminado que se relaciona inversamente a la velocidad

de chip;

transmitir selectivamente la primera y la segunda señales de modulación respectivamente a la primera y a la segunda áreas de cobertura; mediante lo cual la transmisión selectiva de la primera y la segunda señales de modulación da por resultado una variación en tamaño de un primer sector de usuario en el que está incluido por lo menos un usuario.

19. El método según la reivindicación 18, en donde el paso de transmitir selectivamente incluye el paso de transmitir la primera y la segunda señales de modulación de manera que la segunda área de cobertura traslape por lo menos parcialmente la primer área de cobertura.

20. El método según la reivindicación 19, que incluye además el paso de;

proporcionar una tercera señal de modulación, y proporcionar una cuarta señal de modulación que corresponde a una versión retardada de la tercera señal de modulación;

transmitir selectivamente la tercera y cuarta señales de modulación respectivamente a la segunda área de cobertura y a una tercera área de cobertura;

mediante lo cual la transmisión selectiva de la primera y la segunda señales de modulación da por resultado la variación del tamaño del segundo sector de usuario.

21. El método según la reivindicación 19, que

incluye además el paso de:

generar, a una velocidad de chip predeterminada, una segunda señal de ruido pseudoaleatorio (PN) del código PN predeterminado, la primera y la segunda señales PN están desviadas en fase;

combinar la segunda señal PN y una segunda señal de información, y proporcionar una tercera señal de modulación resultante; y

proporcionar una cuarta señal de modulación al retardar la tercera señal de modulación en un retardo predeterminado que se relaciona inversamente a la velocidad de chip predeterminada.

22. El método según la reivindicación 21, en donde el paso de transmitir selectivamente incluye el paso de transmitir selectivamente la primera y la segunda señales de modulación respectivamente hacia la primera y la segunda áreas de cobertura, exclusivamente durante un primer periodo de operación del sistema, y el paso de transmitir selectivamente la tercera y cuarta señales de modulación respectivamente a la primera y a la segunda áreas de cobertura exclusivamente durante un segundo periodo de operación del sistema.

23. El método según la reivindicación 18, que incluye además el paso de recibir la primera y la segunda señales de modulación y proporcionar la primera señal de

información al por lo menos un usuario con base a la misma.

24. El método según la reivindicación 23, que incluye además el paso de generar una réplica del código PN, y demodular la primera y la segunda señales moduladas hacia la primera y segunda señales demoduladas que utilizan las réplicas del primer código PN.

25. El método según la reivindicación 24, que incluye además el paso de combinar coherentemente la primera y la segunda señales demoduladas.

26. En un sistema de comunicación de subscriptor celular en donde los usuarios que están dentro de por lo menos una célula se comunican entre sí señales de información mediante por lo menos un sitio celular utilizando señales de comunicación de espectro disperso, en donde el sitio celular incluye un transmisor de sitio celular, un método de transmisión de señal proveniente del sitio celular que comprende los pasos de:

proporcionar primero y segundo juegos de señales de información de espectro disperso para transportarse a los usuarios dentro de un primer sector de usuario de la primera célula, el paso de proporcionar incluye el paso de generar el segundo juego de señales de información de espectro disperso retardando cada una de las señales de información incluidas dentro del primer juego; y

transmitir selectivamente, dentro de un primer

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periodo de operación del sistema, el primero y segundos juegos de señales de información de espectro disperso respectivamente a la primera y segunda áreas de cobertura dentro de la por lo menos una célula, en donde el tamaño del primer sector de usuario varía a través de la transmisión selectiva del primero y segundo juegos de señales de información de espectro disperso.

27. Un método para transportar información a por lo menos un usuario en un sistema de comunicación de espectro disperso, que comprende los pasos de:

generar, a una velocidad de chip predeterminada, una primera señal de ruido pseudoaleatorio (PN) de un primer código PN predeterminado;

combinar la primera señal PN y un primera señal de información y proporcionar una primera señal de modulación resultante;

proporcionar una segunda señal de modulación replicando la primera señal de modulación;

alinear la primera y la segunda señales de modulación en fase, y transmitir selectivamente la primera y la segunda señales de modulación resultantes alineadas en fase a la primera y a la segunda áreas de cobertura.

28. Un sistema para recibir información transmitida por lo menos a un usuario en un sistema de comunicación de espectro disperso, que comprende:

un medio para recibir selectivamente una primera señal proveniente de una primera área de cobertura y para recibir selectivamente una segunda señal proveniente de una segunda área de cobertura, la primera y la segunda señales son recibidas respectivamente a través de primera y segunda antenas asociadas con la primera y la segunda áreas de cobertura, la primera y la segunda señales están moduladas por una primera señal de ruido pseudoaleatorio de un primer código PN predeterminado;

un medio para retardar la primera señal recibida a través de la segunda antena mediante un primer retardo a fin de producir una señal retardada, el retardo se selecciona inversamente a una velocidad de chip de la señal PN; y

un medio para combinar coherentemente la segunda señal recibida a través de la segunda antena con la señal retardada, y para proporcionar una primera señal de modulación resultante;

mediante lo cual la recepción selectiva de la primera y la segunda señales dan por resultado la variación en tamaño en un primer sector de usuario en el cual está incluido el por lo menos un usuario.

29. El sistema según la reivindicación 28, que incluye además:

un medio para recibir selectivamente una tercera

señal proveniente de la segunda área de cobertura y para recibir selectivamente una cuarta señal proveniente de una tercera área de cobertura, la tercera y la cuarta señales se reciben respectivamente a través de la segunda hasta la tercera antenas;

un medio para retardar la tercer señal recibida a través de la segunda antena en por lo menos un primer retardo a fin de producir una segunda señal retardada; y

un medio para combinar coherentemente la cuarta señal recibida a través de la tercer antena con la segunda señal retardada;

mediante lo cual la recepción selectiva de la tercera y la cuarta señales da por resultado la variación de tamaño de un segundo sector de usuario.

30. El sistema según la reivindicación 1, y en donde el medio para transmitir selectivamente la primera y la segunda señales de modulación incluye el paso de transmitir selectivamente el primero y el segundo componentes de polarización de la primera señal de modulación y el primero y el segundo componentes de polarización de la segunda señal de modulación.

31. Un transceptor de comunicaciones colocado dentro de una primera célula de un sistema de comunicación celular, el transceptor comprende:

un sistema de antena para proyectar un patrón de

haz de antenas sobre la primera célula;

un medio de banco de canal, acoplado electromagnéticamente al sistema de antena, para suministrar señales forzadoras de haz hacia el sistema de antena, de manera que el patrón de haz de antena se proyecte a fin de sectorizar la primer célula en una pluralidad de sectores de usuario;

cada uno de los sectores de usuario tiene una pluralidad de canales de tráfico asociados con el mismo; y

un medio controlador para supervisar el uso de la pluralidad de canales de tráfico asociados con cada sector de usuario, y para suministrar información de control al sistema de antena con objeto de que el tamaño de los sectores de usuario se ajuste de acuerdo al uso de canal de tráfico monitoreado.

32. En sistema de comunicación celular que incluye por lo menos una célula sectorizada en una pluralidad de sectores de usuario, un método para variar dinámicamente la sectorización de usuarios de la por lo menos una célula, que comprende los pasos de:

monitorear el uso de una pluralidad de canales de tráfico asignados a la pluralidad de sectores de usuario, cada uno de los canales de tráfico de usuario es asignado a un usuario dentro de la por lo menos una célula; y

ajustar el tamaño geográfico de los sectores de

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usuario con base en el uso monitoreado de la pluralidad de canales de tráfico.

33. El método según la reivindicación 32, que incluye además el paso de:

proyectar un patrón de haz de antena sobre la por lo menos una célula, el patrón de haz de antena lleva señales de información asociadas con la pluralidad de canales de tráfico de usuario,

y variar la proyección del patrón de haz de antena de acuerdo con el uso monitoreado de la pluralidad de canales de tráfico.

RESUMEN DE LA INVENCIÓN

Se revelan un sistema y un método para variar dinámicamente la sectorización de canal de tráfico dentro de un sistema de comunicación de espectro disperso. En una implementación preferida el sistema funciona para transportar información a por lo menos un usuario especificado en un sistema de comunicación de espectro disperso e incluye un generador de códigos pseudoaleatorios (50) para generar, a una velocidad de chip predeterminada, una señal de ruido pseudoaleatorio (PN) de un código PN predeterminado. La señal PN se combina entonces con una primera señal de información en un transmisor de espectro disperso (42) para proporcionar una señal de información dispersa PN. El sistema incluye además por lo menos un transmisor de espectro disperso adicional (44, 46), cada uno para recibir a través del elemento de retardo respecto (52, 54) versiones retardadas de la señal PN para proporcionar por lo menos una señal de modulación adicional. Una red de transmisión de conmutación (74) se coloca para transmitir selectivamente mediante las antenas (85, 86) la primera señal de modulación y las señales de modulación adicionales respectivamente hacia la primera y la por lo menos una área de cobertura adicional. La transmisión selectiva de la primera y la por lo menos una señal de modulación adicional da por resultado la variación

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en tamaño del primer sector de usuario. El primer sector de usuario está asociado con un primer juego de canales de tráfico, uno de los cuales es designado al usuario específico. El sistema también puede configurarse para recibir selectivamente y para combinar coherentemente, la primera y la segunda señales de modulación a partir de la primera y la segunda áreas de cobertura.

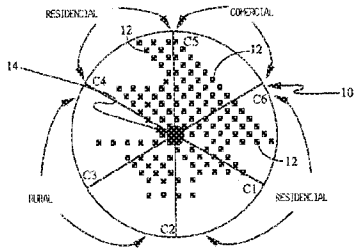
RESIDENCIAL
COMERCIAL
12
C5
12
14
C4
C6
10
12
C3
C1
RURAL
RESIDENCIAL
C2

FIG. 1A

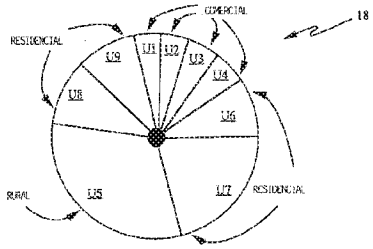
COMERCIAL
18
RESIDENCIAL
U1
U2
U3
U4
U9
U8
U6
U5
U7
RURAL
RESIDENCIAL

FIG. 1B

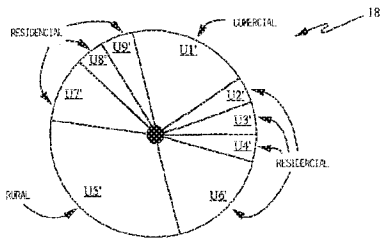
18
RESIDENCIAL
COMERCIAL
U9'
U11'
U8'
U7'
U2'
U3'
U4'
RESIDENCIAL
RURAL
U5'
U6'

FIG. 1C

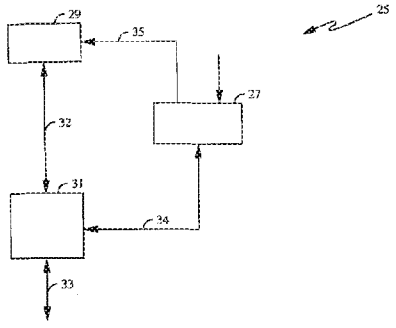
25
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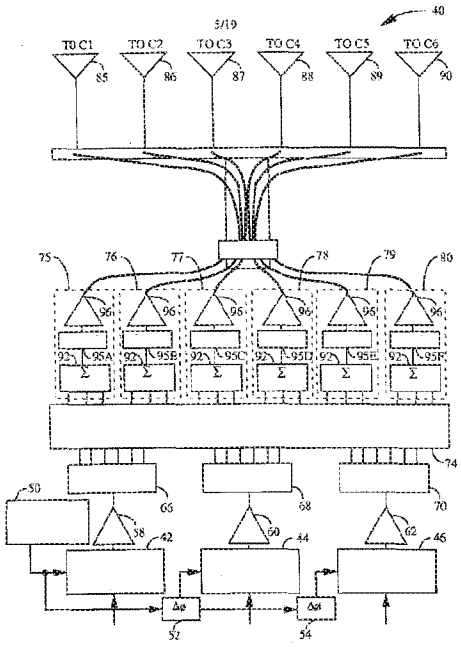
FIG. 1D


40
TO C1
TO C2
TO C3
TO C4
TO C5
TO C6
85
86
87
88
89
90
75
76
77
78
79
80
96
92
95A
95B
95C
95D
95E
95F
Σ
74
50
65
68
70
38
42
60
44
62
46
Δφ
52
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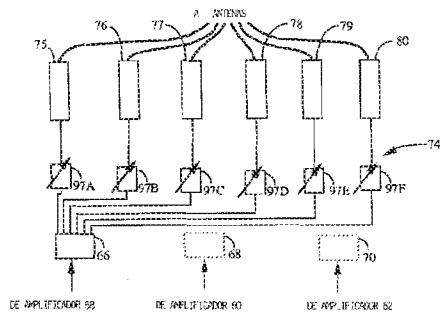
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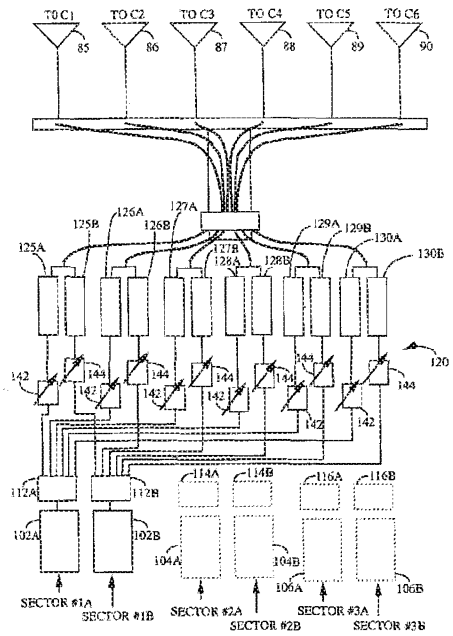
DE AMPLIFICADOR 58
DE AMPLIFICADOR 60
DE AMPLIFICADOR 62

FIG. 3


TO C1
TO C2
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85
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125A
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126A
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142
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116A
116B
102A
102B
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SECTOR #1A
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SECTOR #2A
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SECTOR #3A
SECTOR #3B

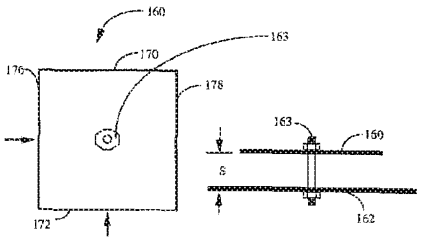
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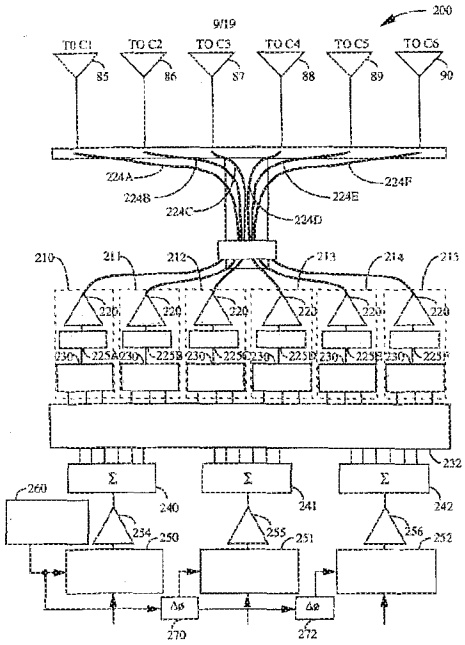
FIG. 5A

FIG. 5B


200
TO C1
TO C2
TO C3
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85
86
87
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224A
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224C
224D
224E
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211
212
213
214
215
220
225A
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225E
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230
232
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256
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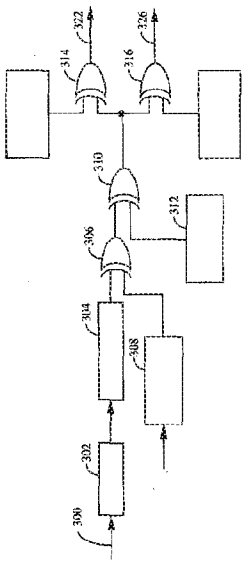
322
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316
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FIG. 7

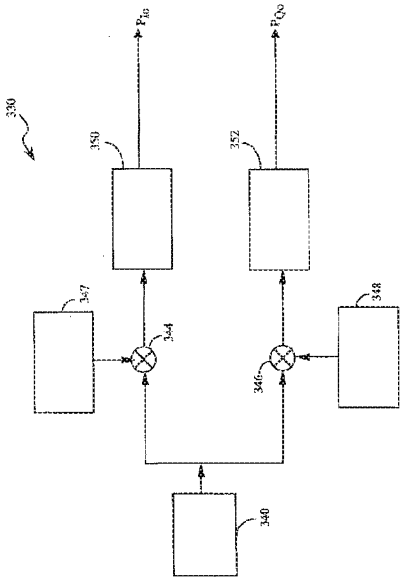
330
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FIG. 8

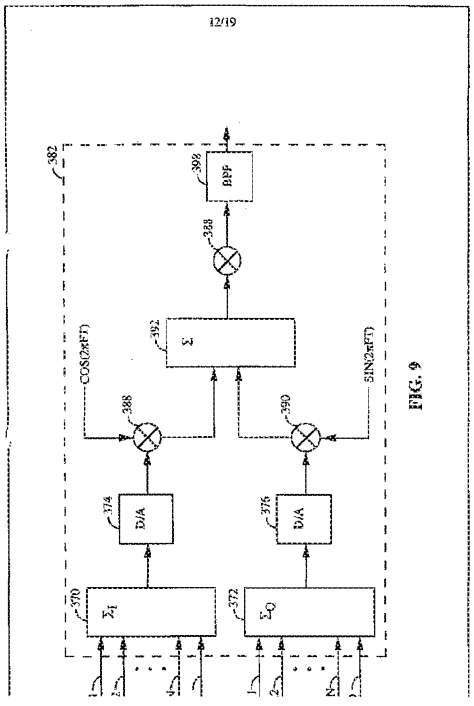

382
398
BPF
388
392
Σ
COS(2πFT)
SIN(2πFT)
388
390
374
D/A
376
D/A
370
372

FIG. 9

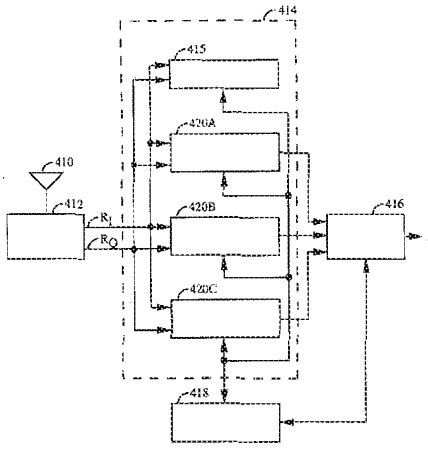


FIG. 10

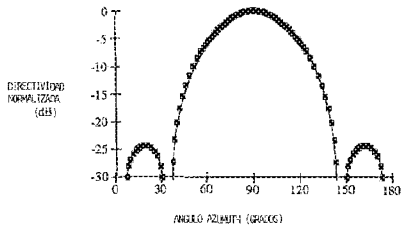


FIG. 11A

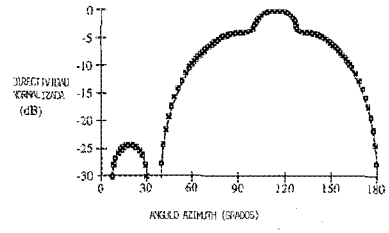
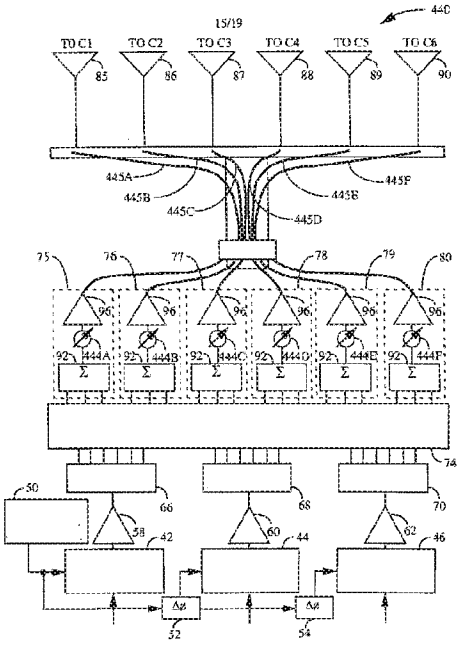


FIG. 11B


440
TO C1
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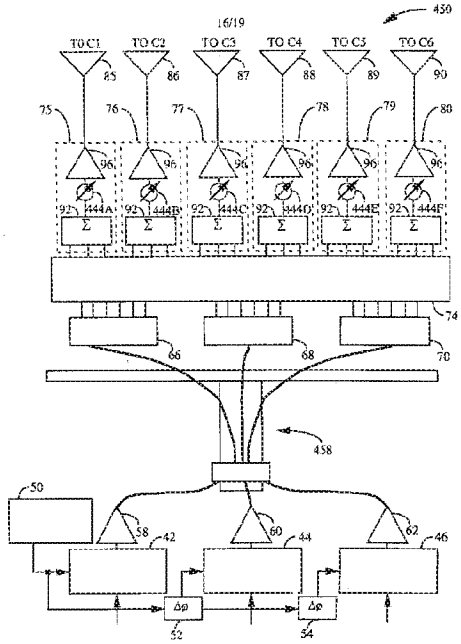
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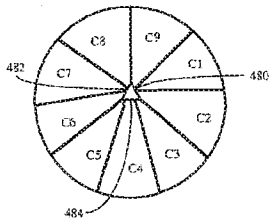

FIG. 14

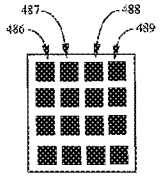

FIG. 15

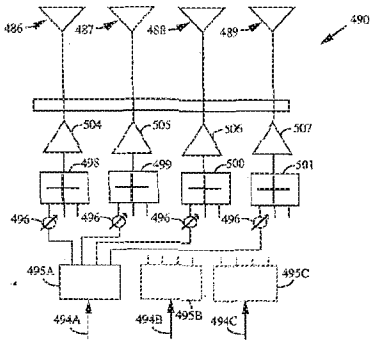
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FIG. 16

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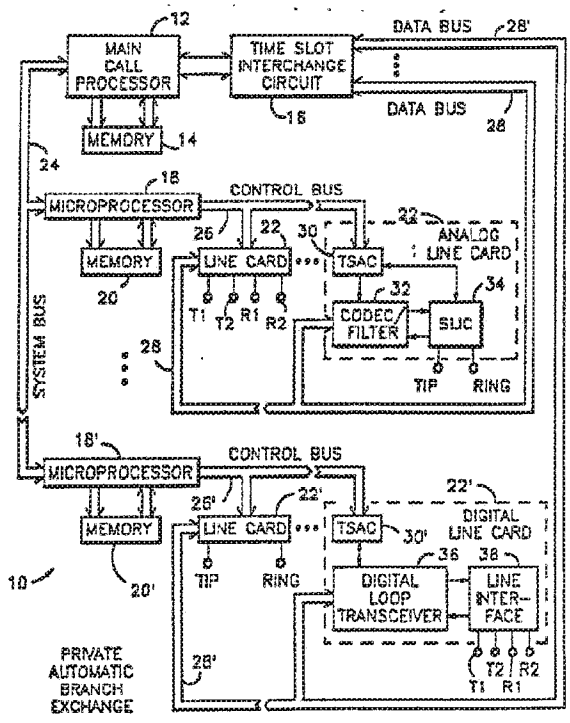
(57) Abstract

In a digital telephone system, a digital private automatic branch exchange (PABX) (10) has a plurality of digital line cards (22-22') for coupling the PABX (10) two respective digital subscriber sets (44) via subscriber lines. In each digital line card (22), a digital loop transceiver (36) operates in a master mode to couple the digital data bus (28') of the PABX (10) to the subscriber line via a subscriber line interface circuit (38) in response to control signals provided by the PABX (10) on the control bus (26') thereof. In each digital subscriber set (44), a digital loop transceiver (36') operates in a slave mode to couple the subscriber set (44) to the subscriber line via a subscriber line interface circuit (38) and to provide the several control signals required by the other components thereof. The digital loop transceivers (36') provide communication on each of two communication channels, with the digital data words of the first channel being treated the same as the digital data words of the second channel.



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DIGITAL LOOP TRANSCEIVER FOR INTERFACING A DIGITAL PABX TO A DIGITAL SUBSCRIBER SET VIA A SUBSCRIBER LINE

Technical Field

This invention relates generally to digital telephone systems and, more particularly, to a digital loop transceiver for use in a digital telephone system comprising a digital PABX and a plurality of digital subscriber sets.

Background Art

When a voice call is made using a conventional analog subscriber set, only a small portion of the frequency spectrum available on the typical subscriber line is utilized. During the development of distributed data processing systems, an effort was made to utilize the existing subscriber line network to facilitate communication of the digital data used by such systems. Various types of modulator/demodulator (modem) devices have been developed to take advantage of the latent capability of the subscriber line network to support digital data communication at data rates significantly greater than that required for analog voice communication. For example, synchronous modems are commercially available which utilize the differential phase shift keyed (DPSK) modulation/demodulation technique to provide data communication at rates up to 9600 baud. However, even in the digital private automatic branch exchanges (PABXs) which support intra-exchange communication of voice information in the form of digital PCM voice data words, the response characteristics of the several analog components of the typical analog line card used therein generally prevent reliable communication at higher rates.

Several techniques have been proposed for providing

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higher speed digital data communication between subscribers through such PABXs. However, such proposals typically require the installation of additional pairs of subscriber lines to subscribers requiring the service and/or redesign/modification of the particular PABX to provide the capability to process the pure digital data words in a manner different from the digital PCM voice data words.

Summary of the Invention

Accordingly, it is an object of the present invention to enable digital data words to be communicated at significantly higher speeds over the existing, installed base of subscriber lines, without any redesign or modification whatsoever of the conventional digital PABX.

In accordance with the present invention, the analog to digital conversion function required to support voice communication in the digital PABX is transferred from the PABX to the subscriber set itself, by moving the conventional codec/filter from the analog line card to the subscriber set, and by interfaceing the codec/filter and the PABX to the subscriber line via a pair of digital loop transceivers (DLT) constructed in accordance with the present invention. The existing subscriber line is then converted from the typical, relatively low speed analog link into a high speed data link by providing, at both the subscriber and exchange ends, a subscriber line interface network which is responsive to the much higher frequencies, e.g. up to about 256 kHz, otherwise unavailable on the typical subscriber line.

Once the subscriber set has been converted into a digital form and the existing subscriber line upgraded to a high speed data link in accordance with the present invention, the digital PCM voice data words and associated signalling information for a single voice call will require only about half of the bandwidth available on the

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subscriber line. Accordingly, the preferred form of the DLT of the present invention simultaneously supports a second communication channel, with the digital data words and associated signalling information of the second channel being time multiplexed with the digital data words and signalling information of the first channel. However, as far as the DLT is concerned, neither, either or both of these channels may carry PCM voice data words, depending upon the requirements of a given subscriber.

Brief Description of the Drawings

Figure 1 is a block representation of a private automatic branch exchange (PABX) adapted in accordance with the present invention.

Figure 2 is a schematic diagram of an analog line card for use in the PABX of Figure 1.

Figure 3 is a digital line card constructed in accordance with the present invention for use in the PABX of Figure 1.

Figure 4 is a digital subscriber set constructed in accordance with the present invention to communicate over a subscriber line with the digital line card of Figure 3.

Figure 5 is a digital loop transceiver (DLT) constructed in accordance with the present invention for use in the digital line card of Figure 3 and the digital subscriber set of Figure 4.

Figure 6 is a schematic representation of a 4-wire communication system between the DLT in the digital line card of Figure 3 and the DLT in the digital subscriber set of Figure 4.

Figure 7 is a timing diagram illustrating a typical exchange between the DLT in the digital line card of Figure 3 and the PABX of Figure 1.

Figure 8 is a timing diagram illustrating a typical exchange between the DLT in the subscriber set of Figure 4

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and the codec/filter therein.

Figure 9 is a schematic representation of a 2-wire communication system between the DLT in the digital line card of Figure 3 and the DLT in the digital subscriber set of Figure 4.

Description of the Preferred Embodiment

Shown in Figure 1 is a conventional private automatic branch exchange (PABX) 10 comprised generally of a main call processor 12 having associated memory 14, a time slot interchange circuit 16, a set of call processing microprocessors 18-18', each having an associated memory 20-20', and a plurality of conventional analog line cards 22. In the illustrated form, the PABX 10 also includes at least two digital line cards 22' constructed in accordance with the present invention.

In a typical digital telephone switching system such as the PABX 10, the main call processor 12 coordinates, via a system bus 24, the call processing activities of each of the several call processing microprocessors 18-18'. In turn, each of the call processing microprocessors 18-18' controls, via respective control buses 26-26', the communication of digital PCM voice data words via respective data buses 28-28' between the several line cards 22 assigned to such microprocessor 18-18'.

In general, each of the analog line cards 22 comprises a time slot assignment and control circuit (TSAC) 30 for selectively enabling a codec/filter 32 to digitally encode an analog voice input signal received via a subscriber line interface circuit (SLIC) 34 from a conventional single channel subscriber set (not shown) coupled to tip and ring conductors for output as a digital pulse code modulation (PCM) voice data word on the respective data bus 28-28', and to decode a digital PCM voice data word received on the data bus 28-28' for output as an analog

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voice output signal to the subscriber set (not shown) via the SLIC 34. Shown in Figure 2 is a circuit schematic for such a conventional analog line card 22, using components commercially available from Motorola. The various control and data signals which are provided to or by the line card 22 are generally referred to as the "backplane" of the PABX 10.

In a typical telephone call initiated by a subscriber served by a "source" line card 22 controlled by, say, the call processing microprocessor 18 to a subscriber served by a "destination" line card 22 controlled by, for example, the call processing microprocessor 18', the TSAC 30 on the source line card 22 initially detects via the associated SLIC 34 that the source subscriber set is off hook, and routes the call routing information to the call processing microprocessor 18 for transfer to the main call processor 12. If the destination line card 22 is not indicated in the memory 14 as being busy, the main call processor 12 then requests the call processing microprocessor 18' to notify the destination line card 22 of the call. If, upon providing the system-generated ring signal to the destination subscriber set via the respective SLIC 34, the associated TSAC 30 advises the call processor 18' that the destination subscriber set has been taken off hook, the call processing microprocessor 18' advises the main call processor 12 that the requested connection has been established. During a particular transmit time slot assigned by the main call processor 12, the TSAC 30 on the source line card 22 enables the associated codec/filter 32 to encode the analog voice signal then being received from the source subscriber set via the SLIC 34 for output as a digital PCM voice data word onto the data bus 28. Meanwhile, the main call processor 12 has enabled the time slot interchange circuit 16 to couple the data bus 28 to the data bus 28' to

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facilitate the requested intra-exchange communication of the digital PCM voice data word. Simultaneously, the TSAC 30 on the destination line card 22 enables the associated codec/filter 32 to decode the digital PCM voice data word on the data bus 28' for output as an analog voice signal to the destination subscriber set via the SLIC 34. In a similar manner, but during a different receive time slot assigned by the main call processor 12, the destination line card 22 is allowed to encode the analog voice signal received from the destination subscriber set for transmission as a digital PCM voice data word via data bus 28', interchange circuit 16 and data bus 28' to the source line card 22 for decoding and output to the source subscriber set. If this exchange of digital PCM voice data words occurs at a sufficiently high frame rate, say of the order of 8kHz, then it will appear to each of the subscribers that there is a direct analog link between their respective subscriber sets.

In the general form shown in Figure 1, each of the digital line cards 22' comprises a time slot assignment and control circuit (TSAC) 30' for selectively enabling a digital loop tranceiver (DLT) 36 (see Figure 5) to receive digital data words via a subscriber line interface network 38 from a dual channel, digital subscriber set, such as that shown in Figure 4, which is coupled to respective receive and transmit pairs of tip and ring conductors, for direct output on the respective data bus 28-28' in the same manner as the digital PCM voice data words are output by the codec/filter 32 in the analog line cards 22; and to receive digital data words on the data bus 28-28' for direct output to the subscriber set via the subscriber line interface network 38. Shown in Figure 3 is a circuit schematic for the digital line card 22', wherein: the TSAC 30' comprises a pair of the Motorola time slot assignment circuits (TSACs), one for each of the two digital

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communication channels the digital line card 22' is capable of simultaneously supporting; the DLT 36 comprises an integrated circuit constructed in accordance with Figure 5; and the subscriber line interface network 38 comprises a transmit isolation transformer 40 coupled to the tip and ring conductors which comprise the receive pair of the subscriber line and a receive isolation transformer 42 coupled to the tip and ring conductors which comprise the transmit pair of the subscriber line. As illustrated in Figure 3, the digital line card 22' responds to and provides the same control and data signals which are provided to or by the analog line card 22 via the backplane of the PABX 10.

Shown in Figure 4 is a dual channel, digital subscriber set 44 constructed in accordance with the present invention. In general, the subscriber set 44 comprises a digital loop transceiver (DLT) 36' (see Figure 5) for receiving digital data words from the digital line card 22' (see Figure 3) via a subscriber line interface network 38' coupled to respective receive and transmit pairs of tip and ring conductors, for output, if digital PCM voice data words, to a conventional codec/filter 32' for subsequent decoding and output as an analog voice output via a voice I/O network 46, or, if digital data words, to a subscriber data processor (not shown) via a data port 48; and for transmitting digital data words provided either by the codec/filter 32' in the form of digital PCM voice data words or by the subscriber data processor in the form of digital data words, to the digital line card 22' via the subscriber line interface network 38'. In the preferred form, the voice I/O network 46 includes a voice input portion 50, and a voice output portion 52; the DLT 36' comprises an integrated circuit constructed in accordance with Figure 5; and the subscriber line interface network 38' comprises a transmit isolation

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transformer 40' coupled to the tip and ring conductors which comprise the transmit pair of the subscriber line and a receive isolation transformer 42' coupled to the tip and ring conductors which comprise the receive pair of the subscriber line. In the illustrated form, a conventional tone generator 54, such as the Mostek MK5087, interacts with a dial keypad 56 and the voice I/O network 46 to provide the call routing information required to establish each of the two communication channels, while a conventional hook switch 58 provides call initiation signalling information to the DLT 36'. An audible indication of an incoming call is provided via a ringing transducer 60. A subscriber set power supply 62 derives operating power for the several components of the subscriber set 44 from the subscriber line in a conventional manner.

Shown in Figure 5 is a block diagram of the digital loop transceiver (DLT) 36, constructed in accordance with the present invention. In general, the DLT 36 comprises a digital interface portion 64 for interfacing with the PABX 10 in a master operating mode and with the codec/filter 32 and subscriber data processor in a slave operating mode, a modulator/demodulator portion 66 for transmitting and receiving digital data words via the subscriber line, and a sequencer and control portion 68 for controlling the sequence of operations performed by the digital interface and modulator/demodulator portions 64 and 66, respectively.

In the digital interface portion 64, a receive (RX) control circuit 70 responds to either of two channel receive enable signals, RE1 and RE2, by enabling a receive (RX) register 72 of the shift register type to serially receive digital data bits via a receive (RX) terminal in synchronization with a receive data clock (RDC) on a CLK/RDC terminal. When a predetermined "frame" of data

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(see discussion below) has been received, the sequencer and control portion 68 enables the RX register 72 to transfer the "transmit" frame of data in parallel into a transmitter (XMIT) register 74 in the modulator/demodulator portion 66. Simultaneously, the then-current states of the two channel signalling bits on respective S1I and S2I terminals are latched and inserted into the frame of data in the XMIT register 74. Substantially independently, the sequencer and control portion 68 enables a transmit (TX) register 76 to receive a "receive" frame of data in parallel from a receiver (RCV) register 78 in the modulator/demodulator portion 66. Simultaneously, the two channel signalling bits in the receive frame of data are latched and outputted on respective S1O and S2O terminals. In response to either of two channel transmit enable signals, TE1 and TE2, a transmit (TX) control circuit 80 enables the TX register 76 to serially transmit the receive frame of data via a TX terminal in synchronization with a transmit data clock (TDC) on an X1/TDC terminal.

In the modulator/demodulator portion 66, a digital to analog converter (DAC) control circuit 82 periodically enables a digital to analog converter (DAC) 84 to transmit the transmit frame of data in the XMIT register 74 to the transmit transformer 40 in the subscriber line interface network 38 using a differential pair of output drivers 86 and 88 coupled to respective line output terminals LO1 and LO2. In the preferred embodiment, the DAC 84 utilizes a burst differential phase shift keyed (DPSK) modulation technique at a carrier frequency of 256 kHz. Substantially independently, an input buffer 90 of the differential to single ended output type in the modulation/demodulation portion 66 couples the signal received from the receive transformer 42 in the subscriber line interface network 38 via line input terminals LI1 and

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LI2 to a sync detector 92 via a window detector 94 and to a correlator 96 via a comparator 98. As phase shifts of the proper form are decoded by the correlator 96, the "decoded" bits are shifted into a shift register portion thereof which maintains the most recently received set of data bits which might constitute a frame. When the energy of a DPSK signal of the proper frame length is detected, the sync detector 92 provides a valid sync signal to enable the correlator 96 to transfer the receive frame of data bits being maintained therein, in parallel to the RCV register 78. A demodulator having a sync detector and correlator of suitable form is shown and described in copending U.S. Patent Application Serial No. 332,408. A switched capacitor bandgap reference 100 similar to that shown and described in copending US Patent Application Serial No. 231,073 provides a precision reference voltage to the DAC 84, the window detector 94, and the comparator 98. Periodically, the offsets of the input buffer 90, the window detector 94, the comparator 98, and the bandgap reference 100 are zeroed by an auto-zero circuit 102 in a manner similar to that shown and described in copending U.S. Patent Application Serial No. 231,079.

In operation, the DLT 36 provides duplex communication of digital data words on a pair of independent channels and a signalling bit associated with each of the channels, between the duplex subscriber line and a digital data port. In a typical line transmission operation, the RX register 72 successively receives a digital data word for each of the channels in synchronization with the receive data clock, with the digital data word for the first of the channels being received from the digital I/O port via the RX terminal in response to the first of the channel receive enable signals, RE1, and the digital data word for the second of the channels being received from the digital

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I/O port via the RX terminal in response to the second of the channel receive enable signals, RE2. After the last data bit of the frame has been clocked into the RX register 72, both data words are transferred to the XMIT register 74, and the then-current states of the respective channel signalling bits on the S1I and S2I terminals added to complete the frame. As soon as the frame has been assembled, the DAC control circuit 82 actuates the DAC 84 to serially modulate the first and second digital data words and the respective channel signalling bits in the frame, for transmission via the transmit transformer 40 to one of the pairs of wires in the subscriber line.

In a typical line reception operation, the sync detector 92 monitors the signal received via the receive transformer 42 on the other pair of wires in the subscriber line, and provides a valid sync signal in response to detecting the energy of a DPSK modulated signal of the proper frame length. Meanwhile, the correlator 96 has been serially demodulating the sequentially received bits which might constitute a frame containing a digital data word for each of the channels and the respective channel signalling bits. In response to the valid sync signal, indicating that a valid frame has indeed been received, the correlator 96 transfers the frame to the RCVR register 78. At an appropriate time depending upon the mode of operation, the frame is then transferred from the RCVR register 78 to the TX register 76 and the respective channel signalling bits latched for output on the S1O and S2O terminals. The TX register 76 then sequentially transmits the digital data words in synchronization with the transmit data clock, with the digital data word for the first channel being transmitted to the digital I/O port via the TX terminal in response to the first of the channel transmit enable signals, TE1, and the digital data word for the second channel being

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transmitted to the digital I/O port via the TX terminal in response to the second of the channel transmit enable signals, TE2.

Shown in Figure 6 is a schematic representation of a 4-wire or duplex subscriber line which has been coupled at the exchange end thereof to the DLT 36 in the digital line card 22' via the transmit and receive transformers 40 and 42, respectively, and at the subscriber end thereof to the DLT 36' in the digital subscriber set 44 via the transmit and receive transformers 40' and 42', respectively. In the dual-channel form of the duplex system, a frame of data comprises an 8-bit digital data word for the first channel, an 8-bit digital data word for the second channel, and the signalling bits for the first and second channels. Preferably, the frame also includes a parity bit, either even or odd, as desired. A suitable frame format is illustrated in Figure 6.

In the digital line card 22' shown in Figure 3, the DLT 36 is placed in the master mode of operation by a logic high signal on a master/slave (M/S) terminal. In the master mode, the DLT 36 emulates the codec/filter 32 with respect to the backplane by receiving/transmitting the digital data words just like the codec/filter 32, and by responding to the various control signals just like the codec/filter 32. In particular, the RX register 72 successively receives a digital data word for each of the channels in synchronization with the data clock provided by the PABX 10 via the backplane, with the data word for the first channel being received from the backplane via the RX terminal in response to the RE1 signal provided by a respective one of the TSACs 30 during the receive time slot assigned to the first channel, and the data word for the second channel being received from the backplane via the RX terminal in response to the RE2 signal provided by the other TSAC 30 during the receive time slot assigned to

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the second channel. In response to the next master sync input (MSI) received via an X2/MSI terminal after the last data bit of the frame has been clocked into the RX register 72, both digital data words are transferred to the XMIT register 74, and the then-current states of the respective channel signalling bits provided via the S1I and S2I terminals by the TSACs 30, respectively, added to complete the frame. As soon as the frame has been assembled, the DAC control circuit 82 actuates the DAC 84 to serially modulate the first and second digital data words and the respective channel signalling bits in the frame, for transmission via the transmit transformer 40 to the receive pair of wires in the subscriber line.

Simultaneously, the sync detector 92 monitors the signal received via the receive transformer 42 on the transmit pair of wires in the subscriber line, and provides the valid sync signal in response to detecting the energy of a DPSK modulated signal of the proper frame length. Meanwhile, the correlator 96 has been serially demodulating the sequentially received bits which might constitute a frame containing a digital data word for each of the channels and the respective channel signalling bits. In response to the valid sync signal, indicating that a valid frame has indeed been received, the correlator 96 transfers the frame to the RCVR register 78. In response to the next MSI, the frame is then transferred from the RCVR register 78 to the TX register 76 and the respective channel signalling bits latched for output on the S1O and S2O terminals. The TX register 76 then sequentially transmits the digital data words in synchronization with the transmit data clock provided by the PABX 10 via the backplane, with the digital data word for the first channel being transmitted to the backplane via the TX terminal in response to the TE1 signal provided by the first one of the TSACs 30 during the transmit time

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slot assigned to the first channel, and the digital data word for the second data channel being transmitted to the backplane via the TX terminal in response to the TE2 signal provided by the other TSAC 30 during the transmit time slot assigned to the second channel. A typical sequential interaction of the DLT 36 with the TSACs 30, and with the PABX 10 is illustrated by way of example in the timing diagram of Figure 7.

In the subscriber set 44 shown in Figure 4, the DLT 36' is placed in the slave mode of operation by a logic low on the master/slave (M/S) terminal. In the slave mode, the DLT 36' emulates the functions of the TSAC 30 and the backplane with respect to the codec/filter 32' by providing the digital PCM voice data words and control signals necessary for the codec/filter 32' to operate, and by receiving the digital PCM voice data words provided by the codec/filter 32' just like the backplane. In this mode, the sync detector 92 monitors the signal received via the receive transformer 42' on the receive pair of wires in the subscriber line, and provides the valid sync signal in response to detecting the energy of a DPSK modulated signal of the proper frame length. Meanwhile, the correlator 96 has been serially demodulating the sequentially received bits which might constitute a frame containing a digital data word for each of the channels and the respective channel signalling bits. In response to the valid sync signal, indicating that a valid frame has indeed been received, the correlator 96 transfers the frame to the RCVR register 78. The frame is then promptly transferred from the RCVR register 78 to the TX register 76 and the respective channel signalling bits latched for output on the S10 and S20 terminals. The TX register 76 then sequentially transmits the digital data words in synchronization with a transmit data clock generated by a prescaler and oscillator 104 using a crystal coupled

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between the X1/TDC and X2/MSI terminals, with the digital data word for the first channel being transmitted to the codec/filter 32' via the TX terminal in synchronization with a TE1 signal generated by the TX control 80 relative to the last valid sync signal, and the digital data word for the second data channel being transmitted to the data port 48 via the TX terminal in synchronization with a TE2 signal generated by the TX control 80 relative to the last valid sync signal.

In response to each of the valid sync signals provided by the sync detector 92, the RX register 72 successively receives a digital data word for each of the channels in synchronization with a receive data clock generated by the sequencer and control 68, with the digital PCM voice data word for the first channel being received from the codec/filter 32' via the RX terminal in synchronization with an RE1 signal generated by the RX control 70 relative to the last valid sync signal, and the digital data word for the second channel being received from the data port 48 via the RX terminal in response to an RE2 signal generated by the RX control 70 relative to the last valid sync signal. In response to the next valid sync signal provided by the sync detector 92, both digital data words are transferred to the XMIT register 74 and the then-current states of the respective channel signalling bits provided via the S1I and S2I terminals by the hook switch 58 and, if appropriate, the subscriber data processor, respectively, are added to complete the frame. As soon as the frame has been assembled, the DAC control circuit 82 actuates the DAC 84 to serially modulate the first and second digital data words and the respective channel signalling bits in the frame, for transmission via the transmit transformer 40' to the transmit pair of wires in the subscriber line. A typical sequential interaction of the DLT 36' with the codec/filter 32' and the

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subscriber data processor is illustrated by way of example in the timing diagram of Figure 8.

Although the DLT 36 is designed to operate primarily in the dual-channel mode over a duplex subscriber line, the DLT 36 may be operated in an exchange which has only one pair of wires in each subscriber line by applying a logic high to a format (FOR) terminal thereof. In the illustrated form of such a 2-wire system shown in Figure 9, the half duplex subscriber line is coupled at the exchange end thereof to the DLT 36 in the digital line card 22' via a transmit/receive isolation transformer 106, and at the subscriber end thereof to the DLT 36' in the digital subscriber set 44 via a transmit/receive isolation transformer 106'. In the dual-channel form of the half duplex system, a frame of data comprises an 8-bit digital data word for the first channel, the signalling bit for the first channel, and a second signalling bit for use by the subscriber data processor as a digital data bit. Preferably, the frame also includes a parity bit, either even or odd, as desired. A suitable frame format is illustrated in Figure 9. Since only a single digital data bit may be transferred in each frame, the effective data bit transmission rate is only 8kHz rather than the 64kHz of the duplex system. However, this reduced data rate may be acceptable in situations where the cost to install the second pair of wires in the subscriber line outweighs the benefits of higher transmission rate.

These and other changes and modifications may be made in the arrangement or construction of the various parts or elements of the preferred embodiments as disclosed herein without departing from the spirit and scope of the present invention as defined in the appended claims.

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CLAIMS

1. A digital loop transceiver circuit for providing duplex communication of digital data words on first and second channels and a signalling bit associated with each of said first and second channels, between a duplex subscriber line and a digital I/O port, the transceiver circuit characterized by:

receiver means for successively receiving said first and second of said digital data words and the respective signalling bits in synchronization with a receive data clock, said first digital data word and the respective signalling bit being received from said digital I/O port in response to a first channel receive enable signal, and said second digital data word and the respective signalling bit being received from said digital I/O port in response to a second channel receive enable signal;

modulation means for serially modulating said first and second digital data words and the respective signalling bits for transmission via a first portion of said subscriber line;

sync detection means for detecting a modulated signal on a second portion of said subscriber line, and providing a valid sync signal in response to said detection;

demodulation means for serially demodulating, in response to said valid sync signal, third and fourth of said digital data words and the respective signalling bits received via said second portion of said subscriber line; and

transmitter means for transmitting said third and fourth digital data words and the respective signalling bits in synchronization with a transmit data clock, said third digital data word being transmitted to said digital I/O port in response to a first channel transmit control signal, and said

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fourth digital data word being transmitted to said digital data port in response to a second channel transmit control signal.

2. A digital subscriber set having substantially independent voice and data channels, said digital subscriber set characterized by:

voice channel means for periodically providing a digital PCM voice data word representing a digitized voice input signal, and for receiving a digital PCM voice data word for output as a voice output signal;

data channel means for receiving a digital data word provided to said digital subscriber set, and for transmitting from said digital subscriber set a received digital data word;

signalling means for selectively generating call control signals, including a transmit channel signalling bit, for each of said voice and data channels, and for providing an output signal in response to receiving a predetermined receive channel signalling bit for each of said voice and data channels;

subscriber line interface means for coupling said digital subscriber set to transmit and receive portions of a duplex subscriber line; and

the digital loop transceiver means of claim 1 coupled between said subscriber line interface means and said voice channel means, said data channel means and said signalling means.

3. A telecommunication subscriber line interface circuit for coupling a digital switching system having a digital data bus and a control bus via a duplex subscriber line to a digital subscriber set having time multiplexed first and second digital data channels, the interface circuit characterized by:

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time slot assignment and control means coupled to said control bus and responsive to control signals received therefrom and to first and second transmit channel signalling bits coupled thereto, for selectively providing first and second receive enable signals during respective first and second receive channel time slots, first and second transmit enable signals during respective first and second transmit channel time slots, and first and second receive channel signalling bits;

subscriber line interface means for coupling said interface circuit to a transmit and a receive portion of said duplex subscriber line; and

the digital loop transceiver means of claim 1 coupled between said subscriber line interface means and said data bus, and to said time slot assignment and control means.

4. A telecommunication subscriber line interface network characterized by a plurality of the digital subscriber sets of claim 2 coupled via respective subscriber lines and respective subscriber line interface circuits of claim 3 to a digital switching system having a digital data bus and a control bus.

5. A digital subscriber set having substantially independent voice and data channels, said digital subscriber set comprising:

voice channel means for periodically providing a digital PCM voice data word representing a digitized voice input signal, and for receiving a digital PCM voice data word for output as a voice output signal;

data channel means for receiving a digital data word provided to said digital subscriber set, and for transmitting from said digital subscriber set a received digital data word;

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signalling means for selectively generating call control signals, including a transmit channel signalling bit, for each of said voice and data channels, and for providing an output signal in response to receiving a predetermined receive channel signalling bit for each of said voice and data channels;

subscriber line interface means for coupling said digital subscriber set to transmit and receive portions of a duplex subscriber line; and

digital loop transceiver means coupled between said subscriber line interface means and said voice channel means, said data channel means and said signalling means, characterized by:

sync detection means for detecting a modulated signal on said transmit portion of said subscriber line via said subscriber line interface means, providing a valid sync signal in response to the detection thereof, and providing first and second receive enable signals and first and second transmit enable signals in predetermined relationship to said detection;

demodulation means for serially demodulating, in response to said valid sync signal, a digital PCM voice data word and a digital data word and a receive channel signalling bit associated with each, received from said transmit portion of said subscriber line via said subscriber line interface means;

transmitter means for transmitting said digital PCM voice data word and said digital data word and the respective receive channel signalling bits in synchronization with a data clock developed by said transmitter means, said digital PCM voice data word being transmitted to said voice channel

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means in response to said first transmit enable signal, said digital data word being transmitted to said data channel means in response to said second transmit enable signal, and said signalling bits being transmitted to said signalling means;

receiver means for successively receiving a digital PCM voice data word and a digital data word and a transmit channel signalling bit associated with each, in synchronization with said data clock, said digital PCM voice data word being received from said voice channel means in response to said first receive enable signal, said digital data word being received from said data channel means in response to said second receive enable signal, and said transmit channel signalling bits being received from said signalling means; and

modulation means for serially modulating said digital PCM voice data word and said digital data word and the respective transmit channel signalling bits for transmission in response to said valid sync signal to said receive portion of said subscriber line via said subscriber line interface means.

6. A telecommunication subscriber line interface circuit for coupling a digital switching system having a digital data bus and a control bus via a duplex subscriber line to a digital subscriber set having time multiplexed first and second digital data channels, the interface circuit comprising:

time slot assignment and control means coupled to said control bus and responsive to control signals received therefrom and to first and second transmit channel signalling bits coupled thereto, for selectively providing first and second receive

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enable signals during respective first and second receive channel time slots, first and second transmit enable signals during respective first and second transmit channel time slots, and first and second receive channel signalling bits;

subscriber line interface means for coupling said interface circuit to a transmit and a receive portion of said duplex subscriber line; and

digital loop transceiver means coupled between said subscriber line interface means and said data bus, and to said time slot assignment and control means, said transceiver characterized by:

receiver means for successively receiving first and second digital data words and the receive channel signalling bit associated with each in synchronization with a receive data clock provided by said switching system, said first digital data word being received from said data bus in response to said first receive enable signal, said second digital data word being received from said data bus in response to said second receive enable signal, and said receive channel signalling bits being received from said time slot assignment and control means;

modulation means for serially modulating said first and second digital data words and the respective receive channel signalling bits for transmission, in response to a sync signal provided by said switching system, to said transmit portion of said subscriber line via said subscriber line interface means;

sync detection means for detecting a modulated signal on said receive portion of said subscriber line via said subscriber line interface means, and for providing a valid sync signal in response

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to the detection thereof;

demodulation means for serially demodulating, in response to said valid sync signal, third and fourth digital data words and a transmit channel signalling bit associated with each, received on said receive portion of said subscriber line via said subscriber line interface means; and

transmitter means for transmitting said third and fourth digital data words and the respective transmit channel signalling bits in synchronization with a transmit data clock provided by said switching system, said third digital data word being transmitted to said data bus in response to said first transmit enable signal, said second digital data word being transmitted to said data bus in response to said second transmit enable signal, and said transmit channel signalling bits being transmitted to said time slot assignment and control means.

7. A telecommunication subscriber line interface network comprising:

a digital subscriber set having substantially independent voice and data channels, said digital subscriber set comprising:

voice channel means for periodically providing a digital PCM voice data word representing a digitized voice input signal, and for receiving a digital PCM voice data word for output as a voice output signal;

data channel means for receiving a digital data word provided to said digital subscriber set, and for transmitting from said digital subscriber set a received digital data word;

signalling means for selectively generating call control signals, including a transmit channel

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signalling bit, for each of said voice and data channels, and for providing an output signal in response to receiving a predetermined receive channel signalling bit for each of said voice and data channels;

subscriber line interface means for coupling said digital subscriber set to transmit and receive portions of a duplex subscriber line; and

digital loop transceiver means coupled between said subscriber line interface means and said voice channel means, said data channel means and said signalling means, characterized by:

sync detection means for detecting a modulated signal on said transmit portion of said subscriber line via said subscriber line interface means, providing a valid sync signal in response to the detection thereof, and providing first and second receive enable signals and first and second transmit enable signals in predetermined relationship to said detection;

demodulation means for serially demodulating, in response to said valid sync signal, a digital PCM voice data word and a digital data word and a receive channel signalling bit associated with each, received from said transmit portion of said subscriber line via said subscriber line interface means;

transmitter means for transmitting said digital PCM voice data word and said digital data word and the respective receive channel signalling bits in synchronization with a data clock developed by said transmitter means, said digital PCM voice data word being transmitted to said voice channel means in response to said first transmit enable signal, said digital data word being transmitted

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to said data channel means in response to said second transmit enable signal, and said signalling bits being transmitted to said signalling means;

receiver means for successively receiving a digital PCM voice data word and a digital data word and a transmit channel signalling bit associated with each, in synchronization with said data clock, said digital PCM voice data word being received from said voice channel means in response to said first receive enable signal, said digital data word being received from said data channel means in response to said second receive enable signal, and said transmit channel signalling bits being received from said signalling means; and

modulation means for serially modulating said digital PCM voice data word and said digital data word and the respective transmit channel signalling bits for transmission in response to said valid sync signal to said receive portion of said subscriber line via said subscriber line interface means; and

a telecommunication subscriber line interface circuit for coupling a digital switching system having a digital data bus and a control bus via said duplex subscriber line to said digital subscriber set, said interface circuit comprising:

time slot assignment and control means coupled to said control bus and responsive to control signals received therefrom and to first and second transmit channel signalling bits coupled thereto, for selectively providing first and second receive enable signals during respective first and second receive channel time slots, first and second transmit enable signals during respective first and

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second transmit channel time slots, and first and second receive channel signalling bits;

subscriber line interface means for coupling said interface circuit to a transmit and a receive portion of said duplex subscriber line; and

digital loop transceiver means coupled between said subscriber line interface means and said data bus, and to said time slot assignment and control means, said transceiver comprising:

receiver means for successively receiving first and second digital data words and the receive channel signalling bit associated with each in synchronization with a receive data clock provided by said switching system, said first digital data word being received from said data bus in response to said first receive enable signal, said second digital data word being received from said data bus in response to said second receive enable signal, and said receive channel signalling bits being received from said time slot assignment and control means;

modulation means for serially modulating said first and second digital data words and the respective receive channel signalling bits for transmission, in response to a sync signal provided by said switching system, to said transmit portion of said subscriber line via said subscriber line interface means;

sync detection means for detecting a modulated signal on said receive portion of said subscriber line via said subscriber line interface means, and for providing a valid sync signal in response to the detection thereof;

demodulation means for serially demodulating, in response to said valid sync signal, third and

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fourth digital data words and a transmit channel signalling bit associated with each, received on said receive portion of said subscriber line via said subscriber line interface means; and

transmitter means for transmitting said third and fourth digital data words and the respective transmit channel signalling bits in synchronization with a transmit data clock provided by said switching system, said third digital data word being transmitted to said data bus in response to said first transmit enable signal, said second digital data word being transmitted to said data bus in response to said second transmit enable signal, and said transmit channel signalling bits being transmitted to said time slot assignment and control means.

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AMENDED CLAIMS
(received by the International Bureau on 21 March 1983 (21.03.83))

1. (Amended) A digital loop transceiver circuit for providing duplex communication of digital data words on first and second channels and a signalling bit associated with each of said first and second channels, between a duplex subscriber line and a digital I/O port, the transceiver circuit characterized by:

receiver means for successively receiving a first and a second of said digital data words and of said signalling bits in synchronization with a receive data clock, said first digital data word and the respective signalling bit being received from said digital I/O port in response to a first channel receive enable signal, and said second digital data word and the respective signalling bit being received from said digital I/O port in response to a second channel receive enable signal;

modulation means for serially modulating said first and second digital data words and the respective signalling bits for transmission via a first portion of said subscriber line;

sync detection means for detecting a modulated signal on a second portion of said subscriber line, and providing a valid sync signal in response to said detection;

demodulation means for serially demodulating, in response to said valid sync signal, a third and a fourth of said digital data words and of said signalling bits received via said second portion of said subscriber line; and

transmitter means for transmitting said third and fourth digital data words and the respective signalling bits in synchronization with a transmit data clock, said third digital data word being transmitted to said digital I/O port in response to

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a first channel transmit enable signal, and said fourth digital data word being transmitted to said digital data port in response to a second channel transmit enable signal.

2. (Amended) A digital subscriber set having substantially independent voice and data channels, said digital subscriber set characterized by:

voice channel means for periodically providing a digital PCM voice input data word representing a digitized voice input signal, and for receiving a digital PCM voice output data word for output as a voice output signal;

data channel means for receiving a digital information input data word provided to said digital subscriber set, and for transmitting from said digital subscriber set a received digital information input data word;

signalling means for selectively generating call control signals, including a transmit channel signalling bit, for each of said voice and data channels, and for providing an output signal in response to receiving a predetermined receive channel signalling bit for each of said voice and data channels;

subscriber line interface means for coupling said digital subscriber set to transmit and receive portions of a duplex subscriber line; and

the digital loop transceiver means of claim 1 coupled between said subscriber line interface means and said voice channel means, said data channel means and said signalling means wherein said digital PCM voice input data word, said digital information input data word, said digital PCM voice output data word, and said digital information output data word

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comprise said first, second, third and fourth digital data words, respectively, wherein said transmit channel signalling bits comprise said first and second signalling bits, and wherein said receive channel signalling bits comprise said third and fourth signalling bits.

3. (Amended) A telecommunication subscriber line interface circuit for coupling a digital switching system having a digital data bus and a control bus via a duplex subscriber line to a digital subscriber set having time multiplexed first and second digital data channels, the interface circuit characterized by:

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time slot assignment and control means coupled to said control bus and responsive to control signals received therefrom and to first and second transmit channel signalling bits coupled thereto, for selectively providing first and second receive enable signals during respective first and second receive channel time slots, first and second transmit enable signals during respective first and second transmit channel time slots, and first and second receive channel signalling bits;

subscriber line interface means for coupling said interface circuit to a transmit and a receive portion of said duplex subscriber line; and

the digital loop transceiver means of claim 1 coupled between said subscriber line interface means and said data bus, and to said time slot assignment and control means, wherein said first and second transmit channel signalling bits comprise said first and second signalling bits and wherein said first and second receive channel signalling bits comprise said third and fourth signalling bits.

4. Cancelled.

5. (Amended) A digital subscriber set having substantially independent voice and data channels, said digital subscriber set characterized by:

voice channel means for periodically providing a digital PCM voice input data word representing a digitized voice input signal, and for receiving a digital PCM voice output data word for output as a voice output signal;

data channel means for receiving a digital information input data word provided to said digital subscriber

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set, and for transmitting from said digital subscriber set a received digital information input data word;

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signalling means for selectively generating call control signals, including a transmit channel signalling bit, for each of said voice and data channels, and for providing an output signal in response to receiving a predetermined receive channel signalling bit for each of said voice and data channels;

subscriber line interface means for coupling said digital subscriber set to transmit and receive portions of a duplex subscriber line; and

digital loop transceiver means coupled between said subscriber line interface means and said voice channel means, said data channel means and said signalling means, comprising:

sync detection means for detecting a modulated signal on said transmit portion of said subscriber line via said subscriber line interface means, providing a valid sync signal in response to the detection thereof, and providing first and second receive enable signals and first and second transmit enable signals in predetermined relationship to said detection;

demodulation means for serially demodulating, in response to said valid sync signal, a digital PCM voice input data word and a digital output data word and a receive channel signalling bit associated with each, received from said transmit portion of said subscriber line via said subscriber line interface means;

transmitter means for transmitting said digital PCM voice output data word and said digital information input data word and the respective receive channel signalling bits in synchronization with a data clock developed by said transmitter means, said digital PCM voice output data word being transmitted to said voice channel means in response to said first

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transmit enable signal, said digital information input data word being transmitted to said data channel means in response to said second transmit enable signal, and said signalling bits being transmitted to said signalling means;

receiver means for successsively receiving a digital PCM voice input data word and a digital information input data word and a transmit channel signalling bit associated with each, in synchronization with said data clock, said digital PCM voice input data word being received from said voice channel means in response to said first receive enable signal, said digital information input data word being received from said data channel means in response to said second receive enable signal, and said transmit channel signalling bits being received from said signalling means; and

modulation means for serially modulating said digital PCM voice input data word and said digital information input data word and the respective transmit channel signalling bits for transmission in response to said valid sync signal to said receive portion of said subscriber line via said subscriber line interface means.

6. (Amended) A telecommunication subscriber line interface circuit for coupling a digital switching system having a digital data bus and a control bus via a duplex subscriber line to a digital subscriber set having time multiplexed first and second digital data channels, the interface circuit characterised by:

time slot assignment and control means coupled to said control bus and responsive to control signals received therefrom and to first and second transmit channel signalling bits coupled thereto, for selectively providing first and second receive

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to the detection thereof;

demodulation means for serially demodulating, in response to said valid sync signal, third and fourth digital data words and a transmit channel signalling bit associated with each, received on said receive portion of said subscriber line via said subscriber line interface means; and

transmitter means for transmitting said third and fourth digital data words and the respective transmit channel signalling bits in synchronization with a transmit data clock provided by said switching system, said third digital data word being transmitted to said data bus in response to said first transmit enable signal, said second digital data word being transmitted to said data bus in response to said second transmit enable signal, and said transmit channel signalling bits being transmitted to said time slot assignment and control means.

7. Cancelled.

8. (New Claim) A digital loop transceiver circuit for providing duplex communication of digital data words on first and second channels and a signalling bit associated with said first channel, between a duplex subscriber line and a digital I/O port, the transceiver circuit comprising:

receiver means for successively receiving a first and a second of said digital data words and a first of said signalling bits in synchronization with a receive data clock, said first and second digital data words and said first signalling bit being received from said digital I/O port in response to a channel receive enable signal;

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modulation means for serially modulating said first and second digital data words and said signalling bit for transmission via a first portion of said subscriber line;

sync detection means for detecting a modulated signal on a second portion of said subscriber line, and providing a valid sync signal in response to said detection;

demodulation means for serially demodulating, in response to said valid sync signal, a third and a fourth of said digital data words and a second of said signalling bits received via said second portion of said subscriber line; and

transmitter means for transmitting said third and fourth digital data words and said second signalling bit in synchronization with a transmit data clock, said third and fourth digital data words being transmitted to said digital I/O port in response to first channel transmit enable signal.

9. (New Claim) A digital subscriber set having substantially independent voice and data channels, said digital subscriber set comprising:

voice channel means for periodically providing a digital PCM voice input data word representing a digitized voice input signal, and for receiving a digital PCM voice output data word for output as a voice output signal;

data channel means for receiving a digital information input data word provided to said digital subscriber set, and for transmitting from said digital subscriber set a received digital information output data word;

signalling means for selectively generating a call control signal, including a transmit channel

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signalling bit, for said voice channel, and for providing an output signal in response to receiving a predetermined receive channel signalling bit for said voice channel;

subscriber line interface means for coupling said digital subscriber set to transmit and receive portions of a duplex subscriber line; and

the digital loop transceiver means of claim 10 coupled between said subscriber line interface means and said voice channel means, said data channel means and said signalling means, wherein said digital PCM voice input data word, said digital information input data word, said digital PCM voice output data word, and said digital information output data word comprise said first, second, third and fourth digital data words, respectively, wherein said transmit channel signalling bit comprises said first signalling bit, and wherein said receive channel signalling bit comprises said second signalling bit.

10. (New Claim) A digital loop transceiver circuit for providing duplex communication of digital data words on a channel and a signalling bit associated with said channel, between a duplex subscriber line and a digital I/O port, the transceiver circuit comprising:

receiver means for successively receiving a first of said digital data words and a first of said signalling bits in synchronization with a receive data clock, said first digital data word and said first signalling bit being received from said digital I/O port in response to a channel receive enable signal;

modulation means for serially modulating said first digital data word and said first signalling bit for transmission via a first portion of said subscriber

BUREAU OMPI WIPO INTERNATIONAL

line;
sync detection means for detecting a modulated signal on a second portion of said subscriber line, and providing a valid sync signal in response to said detection;
demodulation means for serially demodulating, in response to said valid sync signal, a second of said digital data words and a second of said signalling bits received via said second portion of said subscriber line; and
transmitter means for transmitting said second digital data word and said second signalling bit in synchronization with a transmit data clock, said second digital data word being transmitted to said digital I/O port in response to a channel transmit enable signal.

11. (New Claim) A digital subscriber set comprising:
voice channel means for periodically providing a digital PCM voice input data word representing a digitized voice input signal, and for receiving a digital PCM voice output data word for output as a voice output signal;
signalling means for selectively generating a call control signal, including a transmit channel signalling bit, for said voice channel and for providing an output signal in response to receiving predetermined receive channel signalling bit for said voice channel;
subscriber line interface means for coupling said digital subscriber set to transmit and receive portions of a duplex subscriber line; and
the digital loop transceiver means of claim 10 coupled between said subscriber line interface means and said voice channel means, wherein said digital PCM

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voice input data word and said digital PCM voice output data word comprise said first and second digital data words, respectively, wherein said transmit channel signalling bit comprises said first signalling bit, and wherein said receive channel signalling bit comprises said second signalling bit.

12. (New Claim) A telecommunication subscriber line interface circuit for coupling a digital switching system having a digital data bus and a control bus via a duplex subscriber line to a digital subscriber set, the interface circuit comprising:

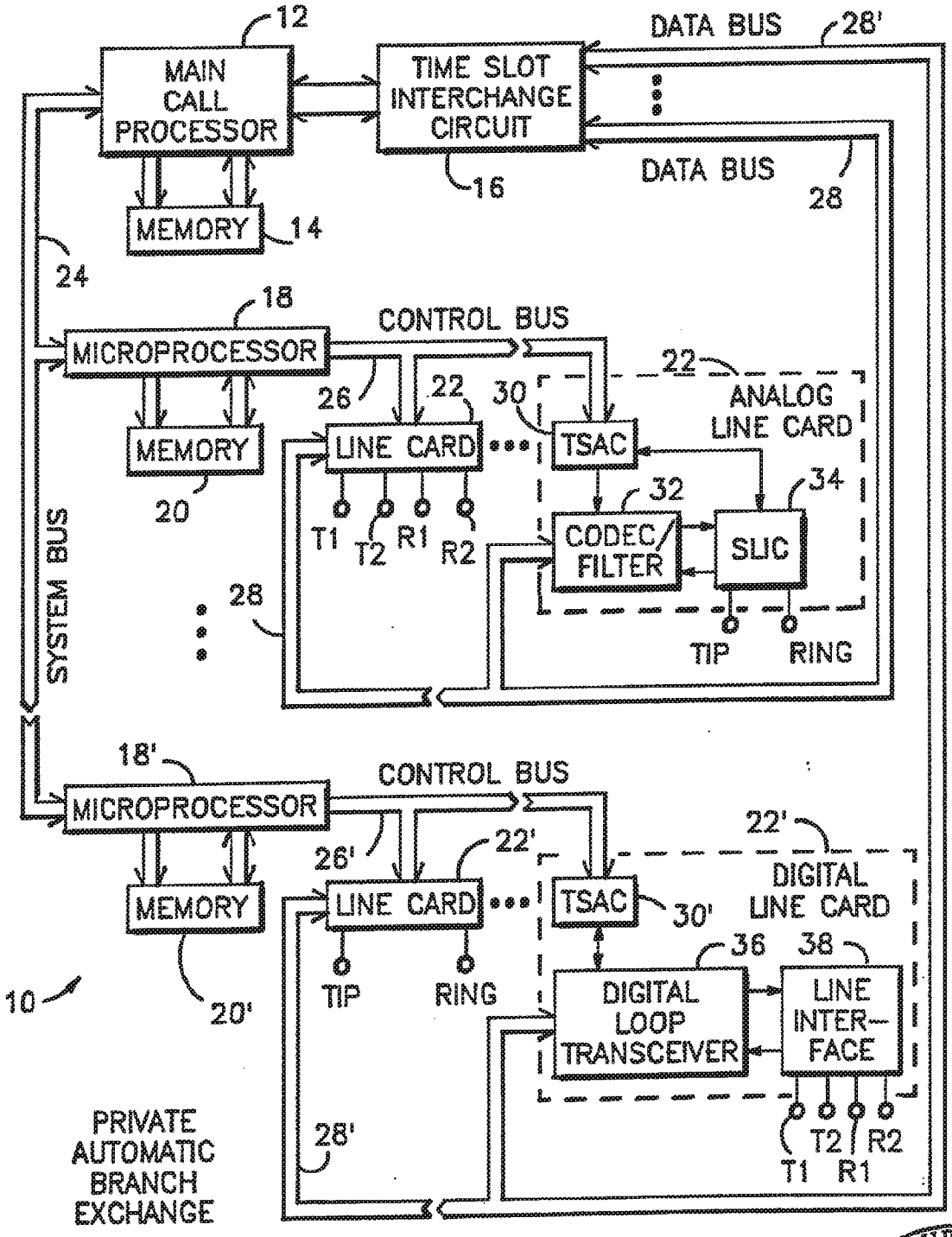
time slot assignment and control means coupled to said control bus and responsive to control signals received therefrom and to a transmit channel signalling bit coupled thereto, for selectively providing a receive enable signal during a receive channel time slot, a transmit enable signal during a transmit channel time slot, and a receive channel signalling bit;

subscriber line interface means for coupling said interface circuit to a transmit and a receive portion of said duplex subscriber line; and

the digital loop transceiver means of claim 10 coupled between said subscriber line interface means and said data bus, and to said time slot assignment and control means, wherein said transmit channel signalling bit comprises said first signalling bit, and wherein said receive channel signalling bit comprises said second signalling bit.

BUREAU OMPI WIPO INTERNATIONAL
IPR2020-00034 Page 01811
DEF0002928

Fig. 1



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IPR2020-00034 Page 01812
DEF0002929

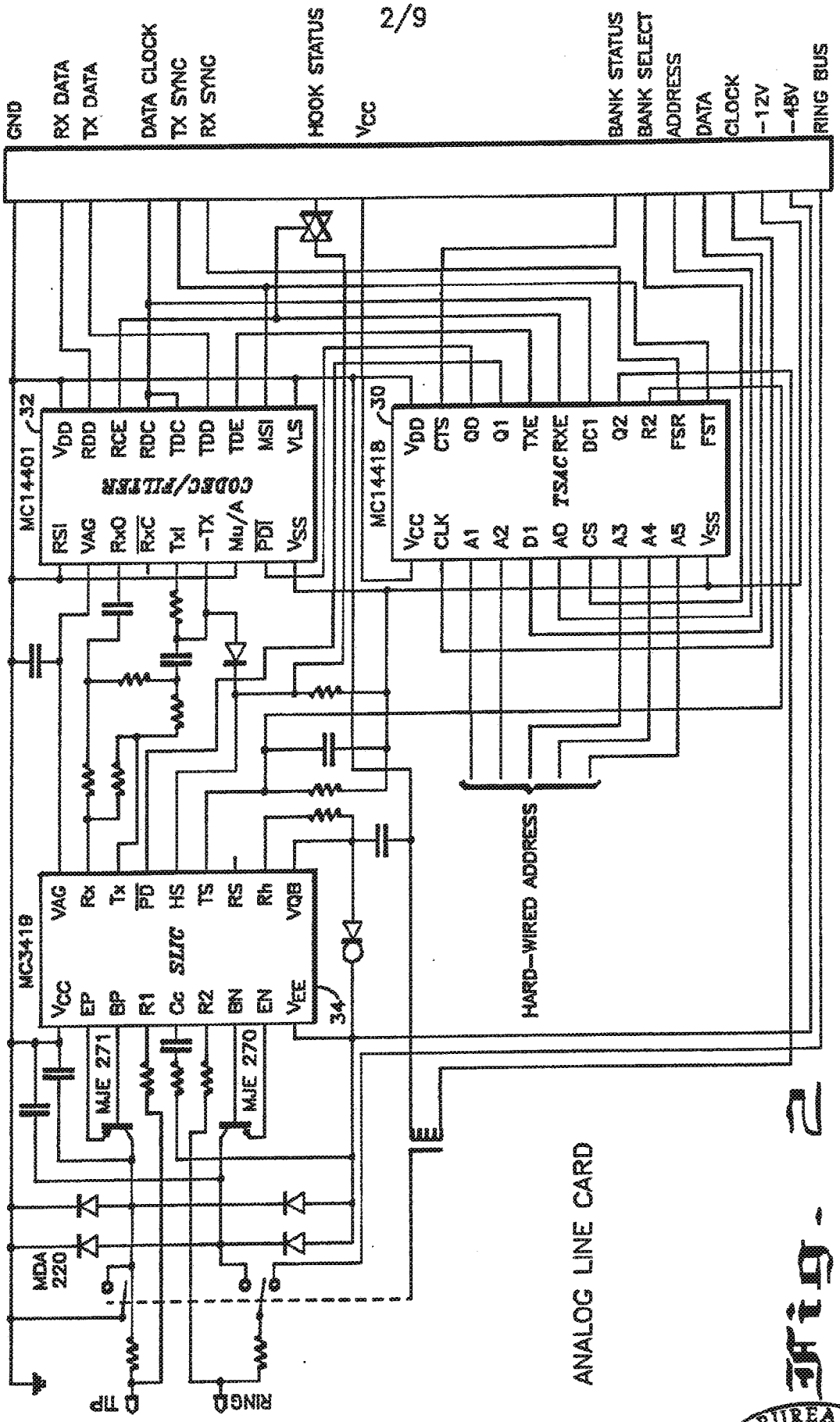

Fig. 2

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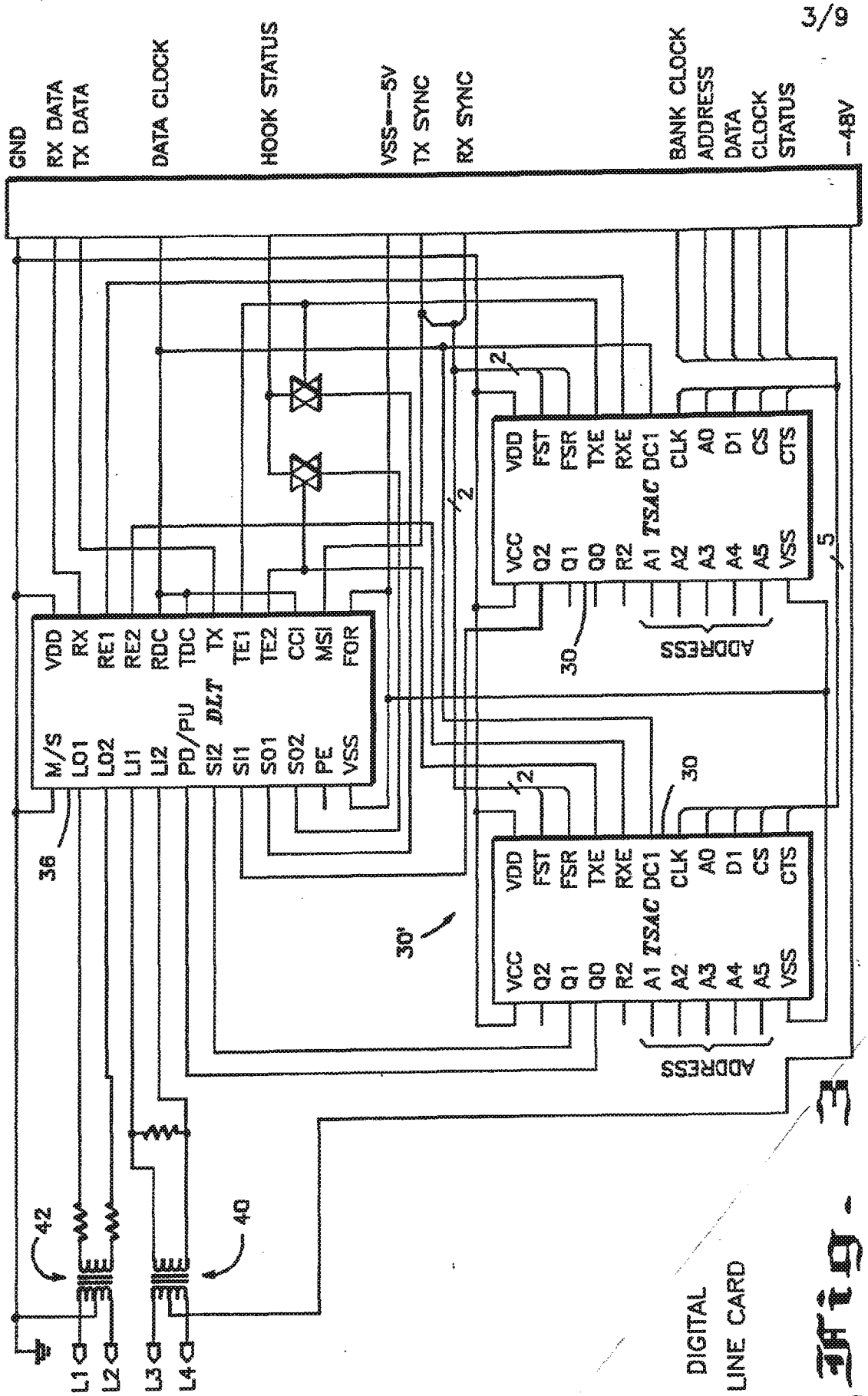

Fig. 3

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IPR2020-00034 Page 01814
DEF0002931

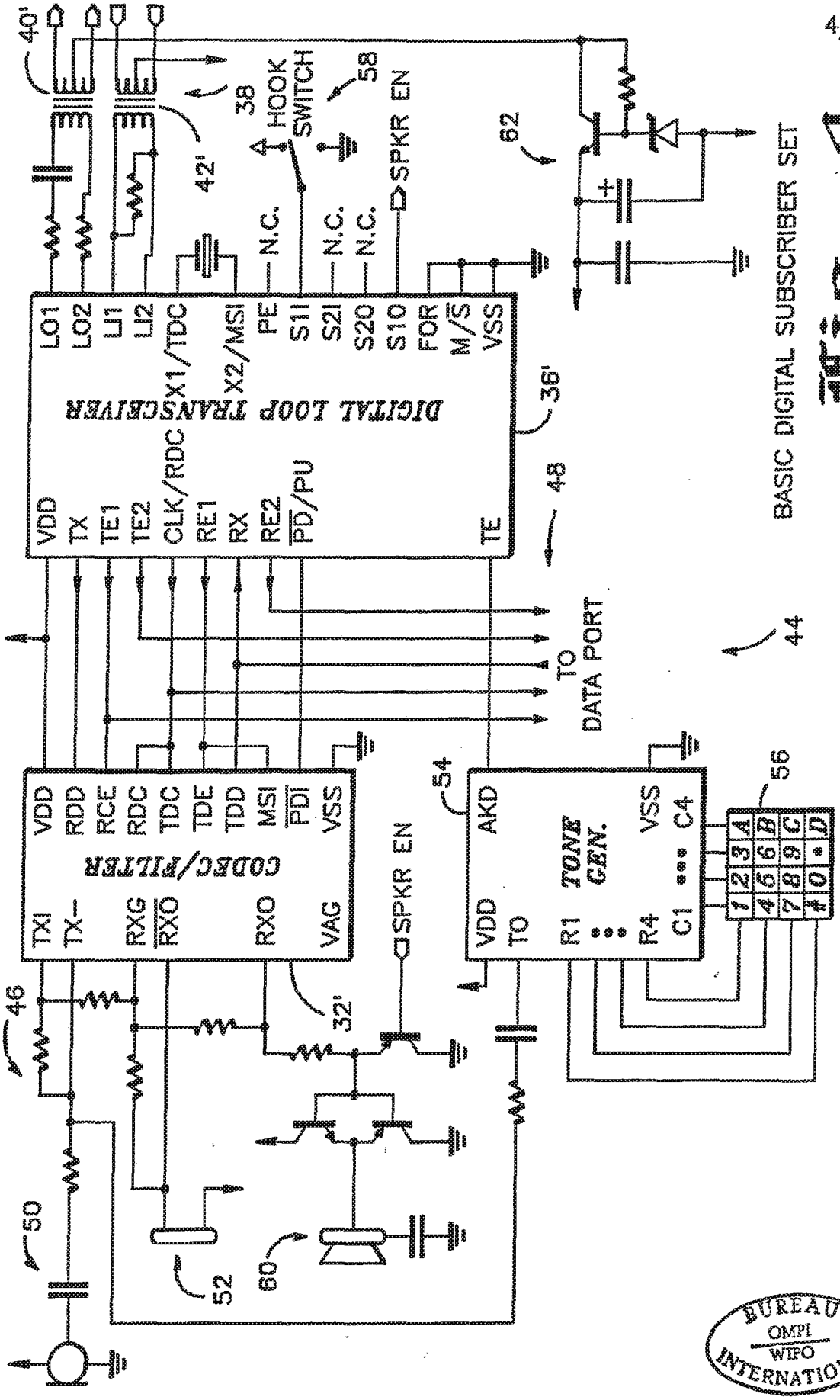

Fig. 4

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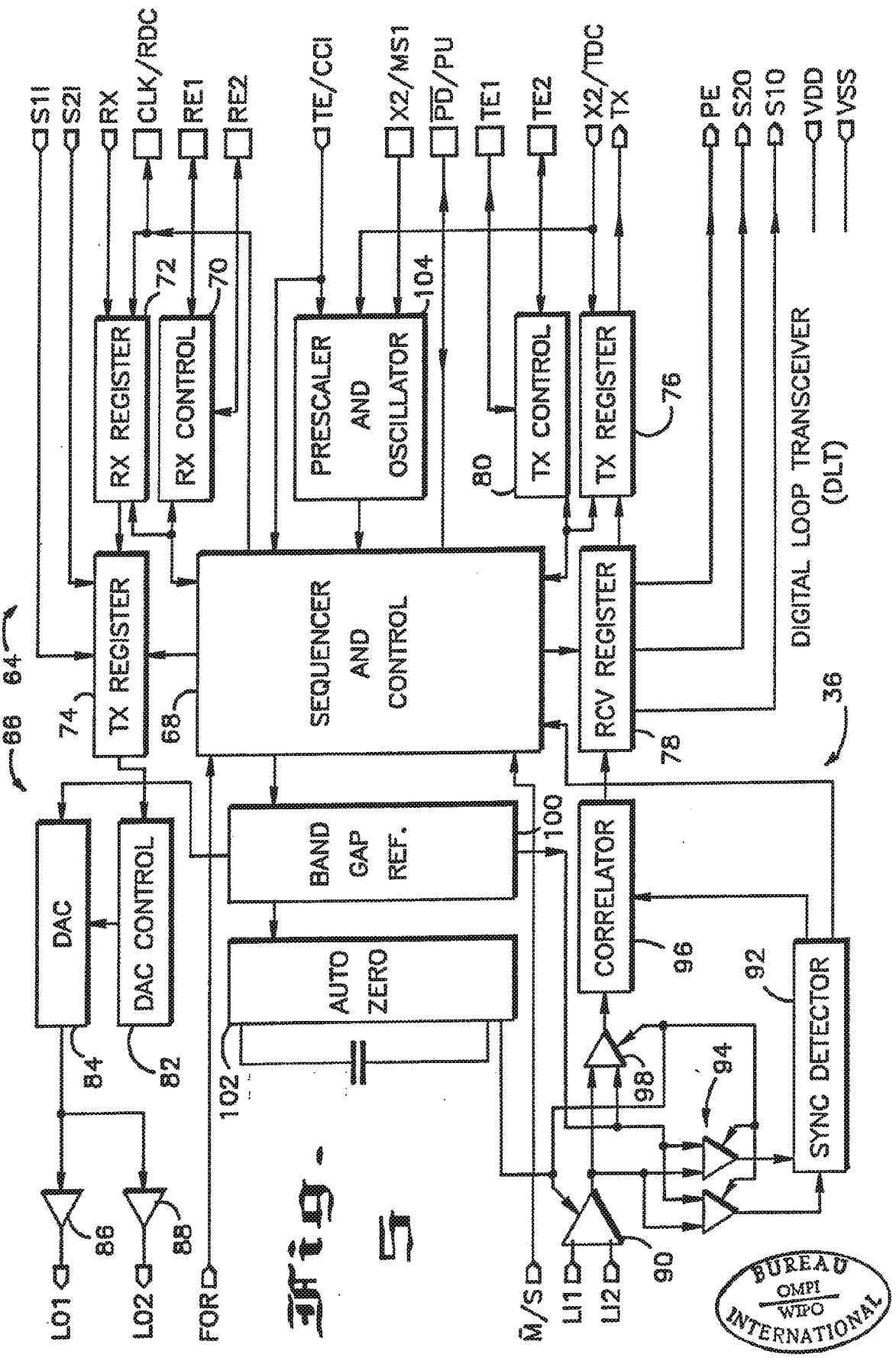

Fig. 5

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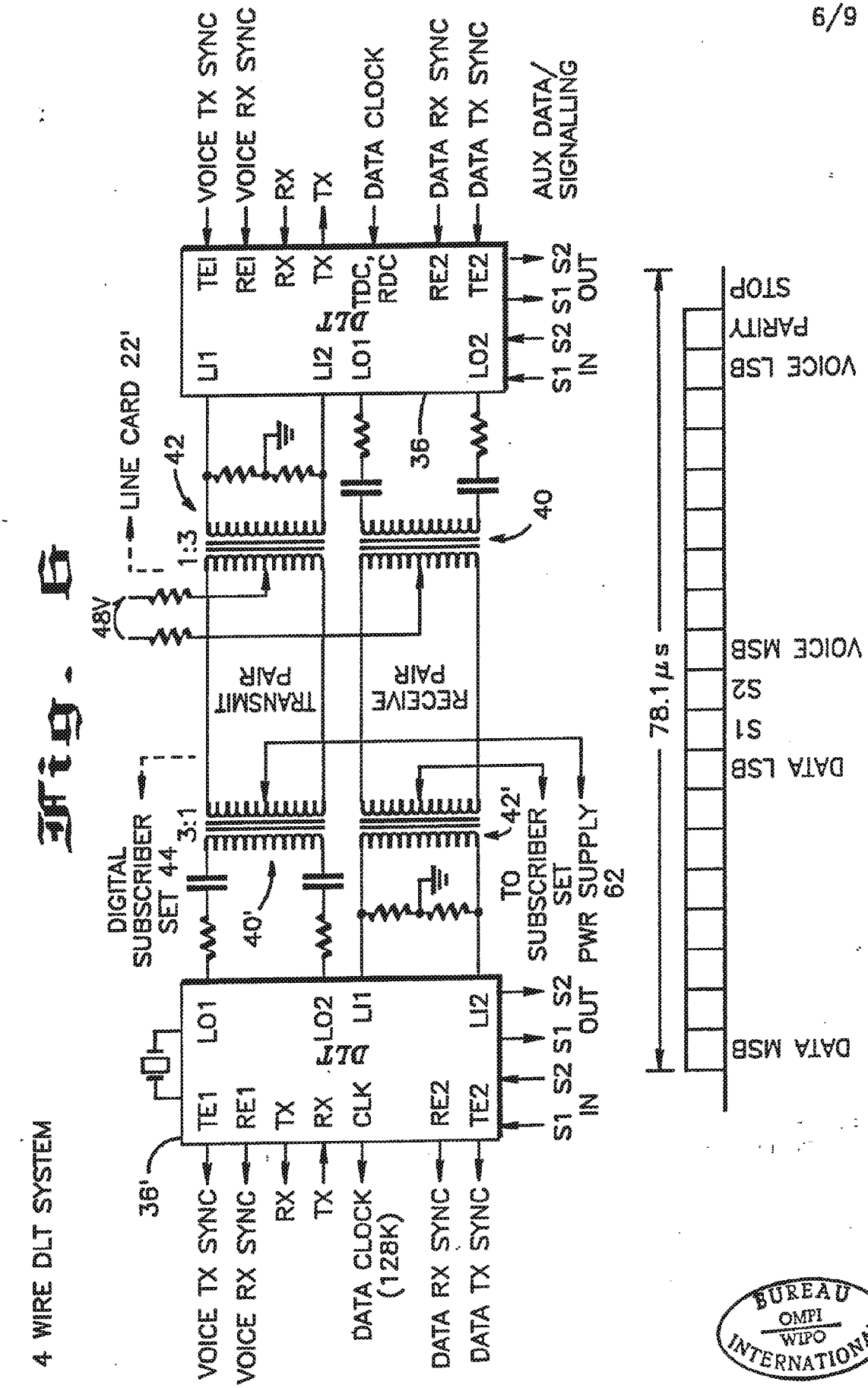
Fig. 6



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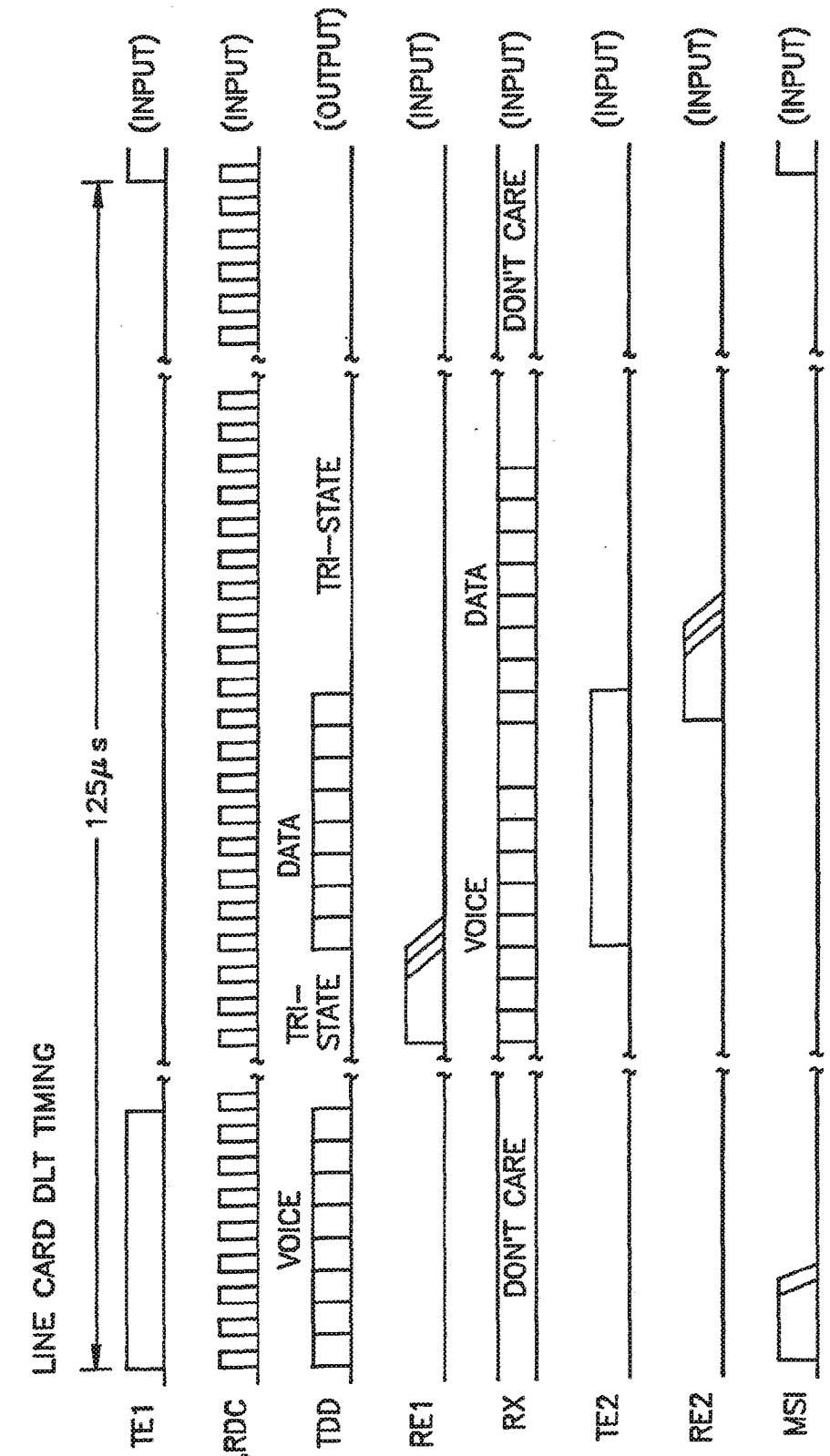

Fig. 7

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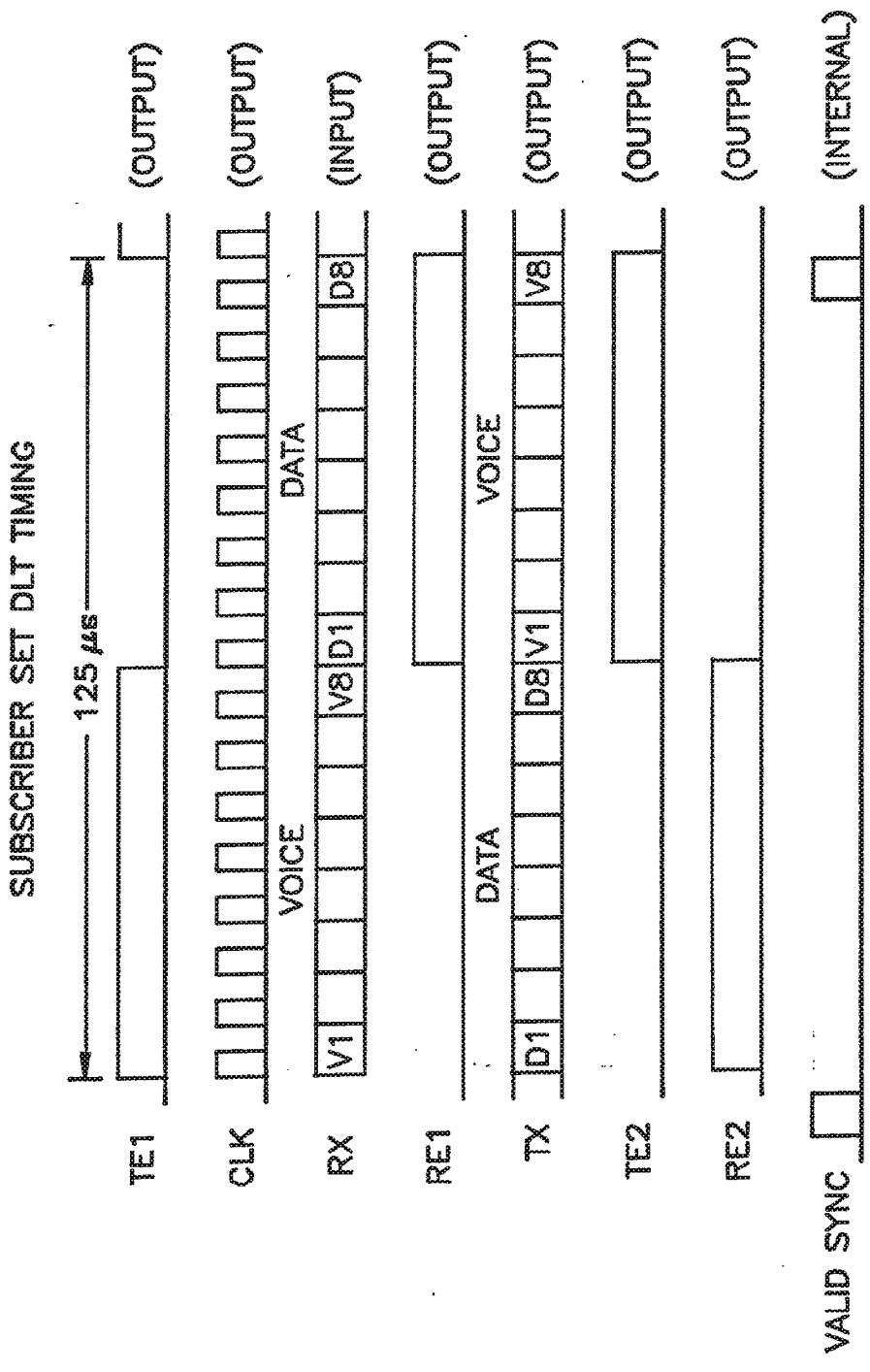

Fig. 8

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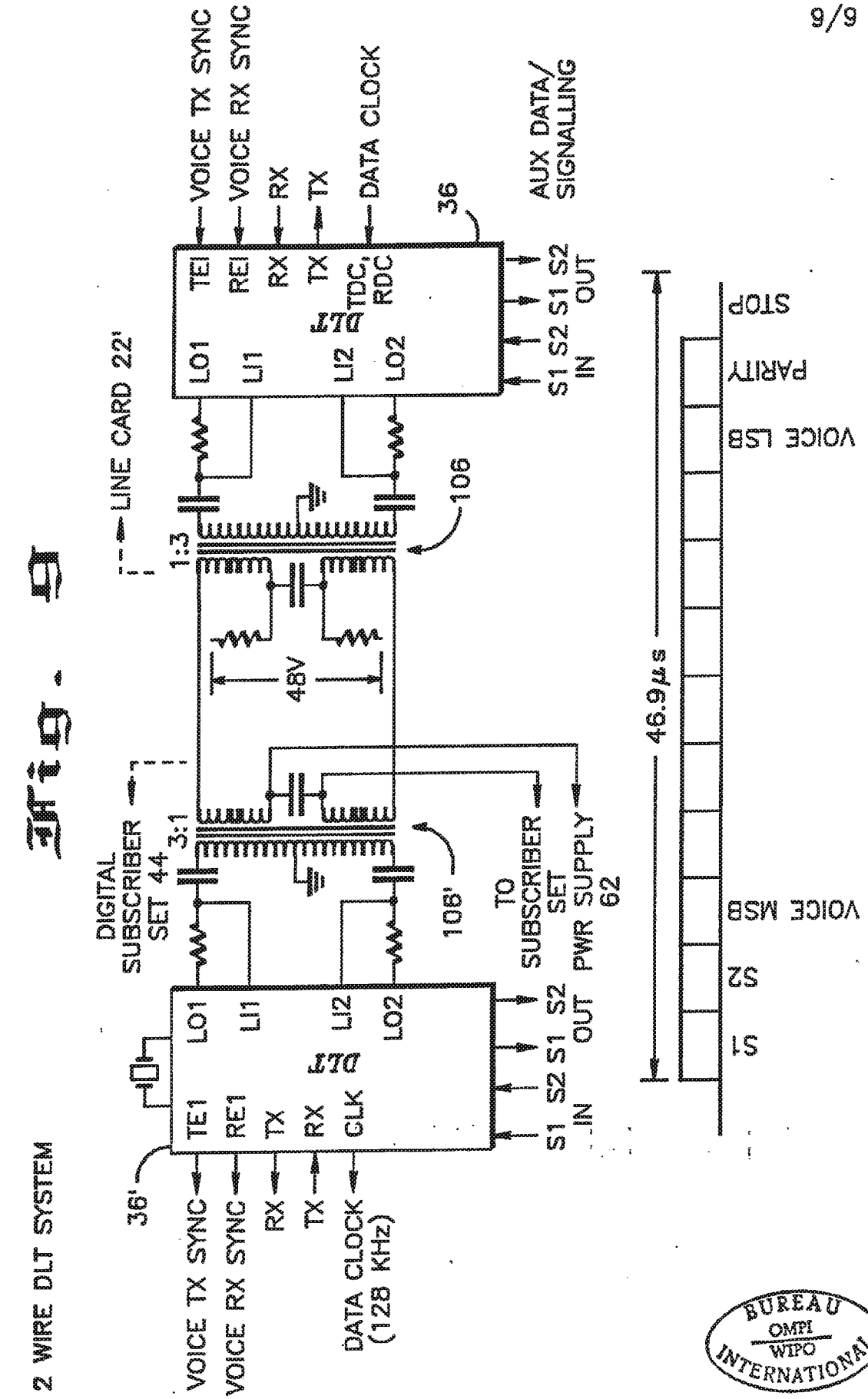

Fig. 9

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INTERNATIONAL SEARCH REPORT

International Application No PCT/US82/01435

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.3 H 04 Q 5/20, H 04 M 9/00
U.S. CL. 370/29, 179/18 AD

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	370/24,29,110.1,77 179/18AD,99M

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	International Conference on Communications, IEEE, June 1980, P.K. Desikan and M.K. Warner, "A Data Switching Technique For A Digital PBX"	1-7
A.	US,.A, 3,924,077, Published 02 December, 1975 Blakeslee	1-7
A.	US, A, 3,978,290, Published 31 August, 1976 Sarma	1-7
A	US, A, 4,145,574, Published 20 March, 1979 Wintzer	1-7
A	US, A, 4,281,410, Published 28 July, 1981 Agricola et al	1-7

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IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
1-11/83	21 JAN 1983
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	Gerald J Boyer

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(51) International Patent Classification 5 : H04L 25/06, 25/10

A1

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(30) Priority data:
414,504 29 September 1989 (29.09.89) US

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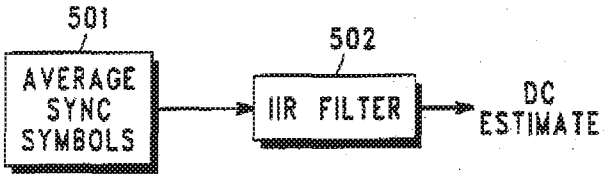
(74) Agents: PARMELEE, Steven, G. et al.; Motorola, Inc., Intellectual Property Dept., 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(81) Designated States: AT (European patent), BE (European patent), CA, CH (European patent), DE (European patent)*, DK (European patent), ES (European patent), FR (European patent), GB (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent).

Published
With international search report.

(54) Title: METHOD OF DC OFFSET COMPENSATION USING A TRANSMITTED DC COMPENSATION SIGNAL



(57) Abstract

A DC offset compensation method that makes use of a received DC compensation signal (107) having a known average value, such as zero. Differences between the known average value and the actually received average value are utilized to calculate a DC compensation value suitable for use in compensating subsequently received data information.

* See back of page

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METHOD OF DC OFFSET COMPENSATION USING A TRANSMITTED DC COMPENSATION SIGNAL

Technical Field

This invention relates generally to DC offset compensation of received data signals.

Background of the Invention

Transmission of data signals through various mediums is known in the art (as used herein, "data" refers to binary or multilevel signalling, as versus analog signal waveforms). When receiving such a signal, it is not uncommon for a varying DC component to become combined therewith and possibly distort data recovery.

To compensate for this, various DC offset compensation methodologies have been proposed. Although at least some of these prior art approaches can be implemented in a digital signal processor (DSP), such implementations require a relatively significant portion of the processing capacity of the DSP. This, in turn, increases current drain requirements for the DSP and/or limits availability of the DSP for support of other desired functions.

Accordingly, a need exists for a method of DC offset compensation that will substantially reliably compensate for DC offset in a received data signal, and that may be implemented, if desired, in a DSP without over burdening the processing capacity of the DSP.

Brief Description of the Drawings

Fig. 1 comprises a timing diagram of a communication resource format implemented in accordance with the invention;

Fig. 2 comprises a depiction of a sync word waveform in accordance with the invention;

Fig. 3 comprises a block diagram of a receiver constructed in accordance with the invention;

Fig. 4 comprises a depiction of a received sync word; and

Fig. 5 comprises a block diagram depiction of a part of the DSP operation when programmed in accordance with the invention.

Best Mode For Carrying Out The Invention

For purposes of this description, an embodiment of the invention will be described in conjunction with a time division multiplexed (TDM) communication resource. In this particular example, the frequency is subdivided into time frames, wherein each time frame is further subdivided into four time slots (101) (Fig. 1). In a given time frame, two of the time slots (102) are used for the transmission of binary signalling information relevant to the allocation of the voice time slots (103) and other system control information.

Each control slot (102) in turn includes space for four commands (104), a slot designation (106), and a sync word (107).

In this embodiment, the sync word (107) is comprised of the hex word zero nine D seven (09D7) (see Fig. 2). In binary form, as represented in Fig. 2, this equates with the sequential transmission of: 0000100111010111. Since this particular sync word, when represented in binary form, includes eight zeroes and eight ones, the average value of the sync word equals zero.

In this embodiment, it will be presumed that the constituent elements of the sync word will be transmitted in a predetermined order, as set forth above, with each broadcast. In a particular application, however, such a requirement may not be necessary. Also, in this particular embodiment, the average value of the sync word elements equals zero, and the importance of this will be made more clear below. (Other elements could perhaps be used in an appropriate application, wherein the average value would not equal zero. What would be important in such an application, however, is that both the average value of the constituent elements of the sync word be predetermined and known to the receiver, and that the system gain also be known to the receiver, since this gain would scale the non-zero average value.)

A receiver (300) (Fig. 3) suitable for practicing the method of the invention will now be described. This receiver (300) includes an antenna (301) for receiving the signalling information (302) transmitted to it, including the data sync words (107). These signals (302)

are processed in an appropriate RF unit (303) and reduced to baseband. An analog to digital convertor (304) then digitizes this representation, and provides the digitized representation to a DSP (306) (such as a 56000 family device as manufactured and sold by Motorola, Inc.) where the signal can be demodulated and processed as desired. Voice transmissions received and processed in this way can then be reconverted to analog form by a digital to analog convertor (307), and the resulting audio signal (308) can be further processed and amplified as appropriate to the particular application.

The receiver (300) further includes a processing unit (309) to control the operation of the RF unit (303) and of the DSP (306). In addition, the processing unit (309) can receive and process recovered signalling information from the DSP (306). Also, an appropriate clock (311) provides necessary clock signals to the DSP (306) and processing unit (309), as may be appropriate to the particular application.

So configured, signals (302) received by the receiver can be processed in various programmable ways in the DSP (306). Such configurations, of course, are known in the art. In this particular embodiment, however, the DSP (306) processes samples (401) of the received sync word (107) (see Fig. 4) at various times. The anticipated time of arrival of the sync word (107), and the constituent elements and order thereof, are of course known to the receiver (300). Therefore, by comparing an average of the sampled values with the value that the receiver (300) would expect to find, the DSP (306) can calculate the difference. These differences can then be used to calculate a DC

compensation value suitable for use with subsequently received data.

In particular, the offset values calculated for this sync word, and also for previously received sync words, can effectively be averaged over time (501 and 502) (see Fig. 5) in the DSP to provide an estimated DC compensation value. As indicated earlier, this DC compensation value can then be used by the DSP to compensate for DC offset in subsequently received data information.

So configured, the DSP (306) is spared the necessity of constantly monitoring the received signal in support of an ongoing DC offset compensation calculation. Instead, by providing for reception of a sync word that effectively also operates as a DC compensation signal, having a substantially known average value, the DSP need only occasionally calculate a substantially reliable DC compensation value that can be used for DC compensation purposes.

What is claimed is:

Claims

1. A method of DC compensating a received signal, characterized by the steps of:

A) receiving a DC compensation signal having a substantially known average value;

B) calculating a DC compensation value using the DC compensation signal.

2. The method of claim 1 wherein the known average value is approximately zero.

3. The method of claim 1 wherein the DC compensation signal comprises a data packet.

4. The method of claim 3 wherein the data packet includes a binary representation of 0, 9, D, and 7.

5. The method of claim 4 wherein the binary representations of 0, 9, D, and 7 are organized in a predetermined manner.

6. The method of claim 3 wherein the known average value of the data packet is zero.

7. The method of claim 1 and further characterized by the steps of:

A) receiving subsequent non-DC compensation signals;

B) using the DC compensation value to DC compensate the non-DC compensation signals.

8. The method of claim 7 wherein the known average value is approximately zero.

9. The method of claim 7 wherein the DC compensation signal comprises a data packet.

10. The method of claim 9 wherein the data packet includes a binary representation of 0, 9, D, and 7.

11. The method of claim 10 wherein the binary representations of 0, 9, D, and 7 are organized in a predetermined manner.

12. The method of claim 9 wherein the known average value of the data packet is zero.

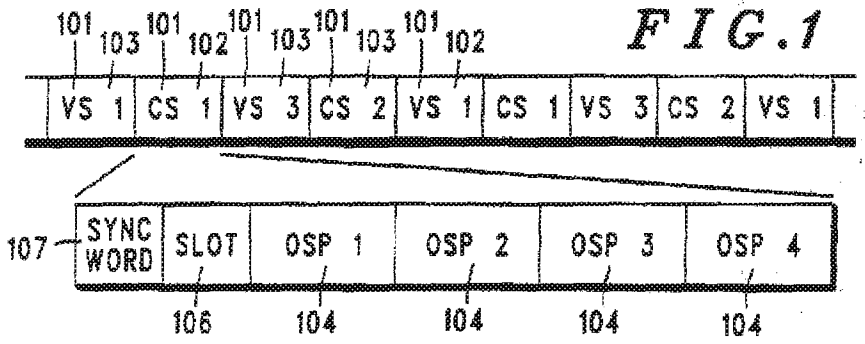


FIG. 1

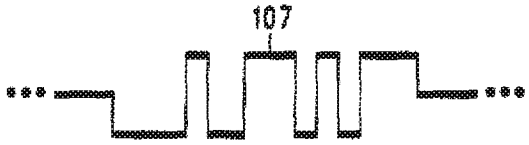


FIG. 2

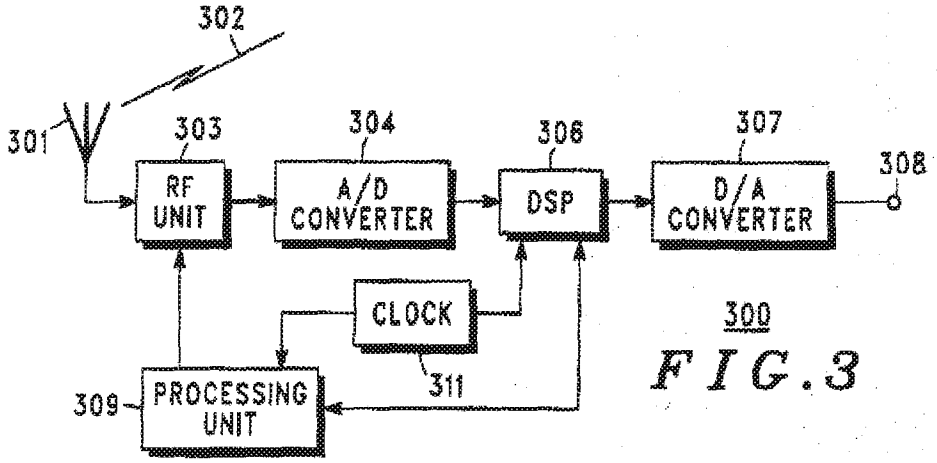
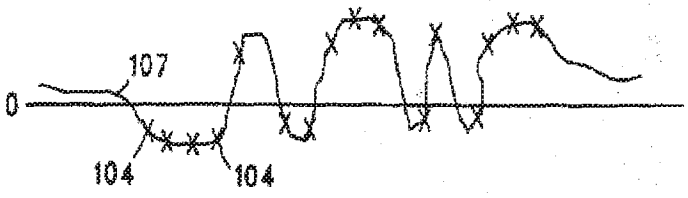


FIG. 3

FIG. 4



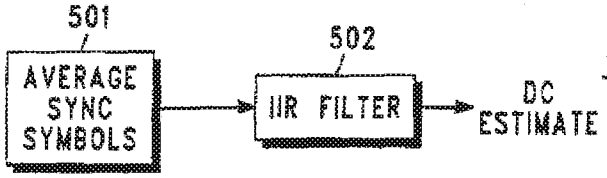


FIG. 5

INTERNATIONAL SEARCH REPORT

International Application No PCT/US90/05358

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (5) : H04L 25/06,25/10
U.S. Cl : 375/36

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	375/19; 358/171; 307/491; 328/168,173; 330/11

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X / Y P	US,A 4,873,702 (CHIU) 10 October 1989 See the Abstract and Figure 2.	1 & 7 / 2-6 & 8-12
Y	US,A 4,387,364 (SHIROTA) 07 June 1983 See Figures 4-7.	2-6 & 8-12

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IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
06 DECEMBER 1990	31 JAN 1991

International Searching Authority [1]	Signature of Authorized Officer [20]
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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : H04L 27/10, 27/18

A1

(11) International Publication Number: WO 94/00943

(43) International Publication Date: 6 January 1994 (06.01.94)

(21) International Application Number: PCT/US92/05317

(22) International Filing Date: 23 June 1992 (23.06.92)

(71) Applicant: MOTOROLA, INC. [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

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(74) Agents: PARMELEE, Steven, G. et al.; Motorola, Inc., Intellectual Property Dept., 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(81) Designated States: AU, BR, CA, JP, UA, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LU, MC, NL, SE).

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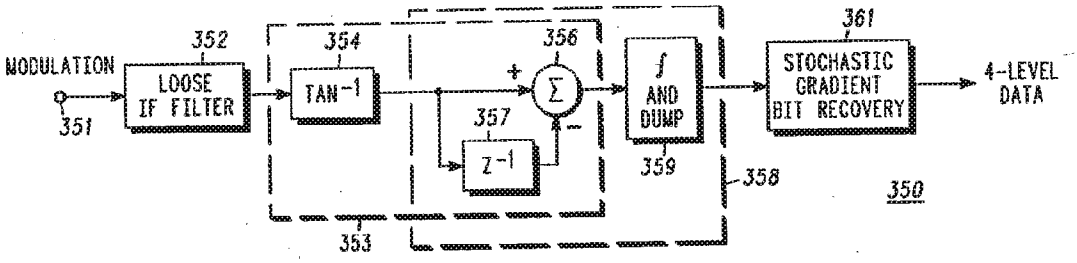
(54) Title: MULTI-MODULATION SCHEME COMPATIBLE RADIO



(57) Abstract

A receiver (350) compatible with both wide channel constant envelope 4 level FSK FM modulation and narrow channel π/4 differential QPSK linear modulation allows compatible interaction between modified constant envelope and non-constant envelope transmitters (300). All Nyquist filtering occurs in the transmitters (300), and none in the receiver (350).

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MULTI-MODULATION SCHEME COMPATIBLE RADIO

Technical Field

This invention relates generally to modulation techniques, including but not limited to constant envelope modulation techniques and non-constant envelope modulation techniques, and transmitters and receivers suitable for use therewith.

Background of the Invention

Various modulation techniques are known to support radio communications. For example, constant envelope modulation techniques, such as frequency modulation (FM), are well known and understood. Non-constant envelope modulation techniques, such as $\pi/4$ differential QPSK, are also known.

Digital signalling techniques suitable for use with various modulation schemes are also known, such as $\pi/4$ differential QPSK (noted above) and 4 level FSK as used with FM. Although both techniques are well understood, present technology readily supports rapid introduction of 4 level FSK FM based radios, whereas $\pi/4$ differential QPSK based non-constant envelope radios pose a greater challenge. Although the various barriers to fielding a

technologically and economically viable platform to support such signalling and modulation will no doubt exist in the near term future, users who require digital signalling will typically find 4 level FSK FM a more likely candidate for relatively immediate implementation.

Radio system users greatly desire immediate availability of digital signalling, in part for reasons of spectral efficiency, and in part to support various desired operating features. These same users, however, do not wish to invest in currently available technology at the expense of being either foreclosed from next generation advances, or at the expense of eliminating a currently acquired digital signalling system in favor of a next generation platform. In short, system users do not wish to acquire a 4 level FSK FM system to serve immediate needs, with the likely availability of $\pi/4$ differential QPSK radios in the future. At the same time, however, these same users want to realize the benefits of digital signalling now.

Accordingly, a need exists for some communications approach that will satisfy the current need for digital signalling, such as 4 level FSK FM, and yet viably accommodate likely future technologies, such as $\pi/4$ differential QPSK, in a cost effective manner.

Summary of the Invention

This need and others are substantially met through provision of a radio transceiver, which transceiver includes a transmitter having a Nyquist filter, and a corresponding receiver that does not include a Nyquist filter.

In one embodiment, the transmitter may be configured to transmit either a constant envelope signal, or a non-constant envelope signal, depending upon the intent of the designer. The receiver, however, functions to receive and properly demodulate either a constant envelope signal or a non-constant envelope signal. So provided, a system can accommodate a plurality of users, wherein some of the users transmit constant envelope signals and other users transmit non-constant envelope signals. Regardless of the transmission type, however, all radios are capable of receiving and demodulating all signals.

So provided, constant envelope transmitters can be coupled with the above receiver to allow provision of 4 level FSK radios to meet near term needs. Later, as economic issues are resolved, radios having $\pi/4$ differential QPSK transmitters can be introduced into the system. A system operator is therefore provided with radios that meet immediate needs, while yet retaining a compatible migration path that readily accommodates a next generation platform.

In one embodiment, the constant envelope signal and the non-constant envelope signal can occupy differing spectral bandwidths. Notwithstanding this difference, the receiver can yet receive and properly demodulate both signals.

Brief Description of the Drawings

FIGS. 1a-b comprise block diagram depictions of prior art 4 level FSK FM transmitter and receiver structures;

FIGS. 2a-b comprise block diagram depictions of prior art π/4 differential QPSK transmitter and receiver structures;

FIGS. 3a-c comprise block diagram depictions of a 4 level FSK transmitter and a π/4 differential QPSK transmitter, respectively, and a receiver suitable for use with both transmitters.

FIG. 4 depicts IF filter design constraints;

FIG. 5a represents the impulse response of an integrate and dump filter;

FIG. 5b represents the frequency response of the integrate and dump filter; and

FIG. 5c represents the band limited frequency response of the integrate and dump filter.

Detailed Description Of A Preferred Embodiment

Prior to describing an embodiment of the invention, it will be helpful to first briefly describe currently proposed 4 level FSK and π/4 differential QPSK transceiver structures.

FIG. 1a depicts pertinent components of a 4 level FSK transmitter (100). The transmitter includes a Nyquist filter (102) designed to have a roll-off factor of 0.2. The Nyquist filter (102) processes the 4 level data as a function of the square root of the raised cosine.

Subsequent to Nyquist filtering, a frequency modulator (103) having a deviation index of 0.27 effectively integrates the previously filtered data, and then frequency modulates the data with respect to a predetermined carrier, as represented by $e^{j(\phi+\omega t)}$. For purposes of simplicity, the above functions are readily

implementable in a DSP, such as a DSP56000 family device as manufactured and sold by Motorola, Inc. The blocks described, and other blocks not described but typically included in a transmitter (such as a power amplifier), are well understood by those skilled in the art, and hence further description would serve no pertinent purpose here.

FIG. 1b depicts relevant components for a proposed 4 level FSK receiver (125). An IF filter (127) filters a received modulation signal (126), which filtered signal is then frequency demodulated. In this embodiment, the frequency demodulator includes an inverse tangent block (128) that feeds its signal to a differential summer (129), the inverting input of which couples to a unit sample delay (131). (Though described as a differential summer, this element really appears as an approximate differentiator. The approximation is based on the first difference in a discrete time system to approximate the true differentiator of a continuous time system.) The output of the differential summer (129) couples to a Nyquist filter (132) (again having a roll-off factor of 0.2), and the resultant data residing within the Nyquist filtered and demodulated signal is recovered by a stochastic gradient bit recovery block (133).

As with the transmitter (100) described above, the above generally referred to functions can be readily implemented in a DSP, and are otherwise sufficiently well known and understood by those skilled in the art such that further elaboration need not be presented here.

FIG. 2a depicts a proposed $\pi/4$ differential QPSK transmitter (200). Again presuming a 4 level data source (201), a summer (202) sums this data with a feed back

signal processed through a unit sample delay (203), the latter components cooperating to realize a differential encoder. A phase modulator (204) then processes the encoded signal as a function of $e^{j\phi}$ to thereby yield complex in phase and quadrature components at, in this embodiment, one sample per symbol. The in phase and quadrature components are then Nyquist filtered (206) (where the roll-off factor = 0.2) and mixed (207) with an appropriate carrier frequency (208) to yield the desired modulation.

FIG. 2b depicts a proposed $\pi/4$ differential QPSK receiver suitable for receiving and demodulating a signal sourced by the above described transmitter (200). The receiver (225) receives the modulation (266) and Nyquist filters (227) the captured signal. The Nyquist filter (227) has a roll-off factor of 0.2. A phase demodulator (228) processes the Nyquist filtered signal as a function of an inverse tangent, and then provides the phase demodulated signal to a differential decoder (229). The differential decoder (229) includes a differential summer (231) that receives the phase demodulated signal and also the phase demodulated signal as processed through a unit sample delay (232). The resultant signal is then processed in an integrate and dump filter (233). A stochastic gradient bit recovery mechanism (234) then processes the decoded information to yield a 4 level data output, as generally referred to above with respect to FIG. 1b.

The blocks generally referred to above with respect to both the transmitter (200) and the receiver (225) for the $\pi/4$ differential QPSK modulation are relatively well understood by those skilled in the art, as well as other

components that would be appropriate to complete a transmitter and receiver, such as power amplifiers, transmission elements, and the like. Therefore, no additional description need be provided here.

The above described constant envelope and non-constant envelope receivers and transmitters are essentially incompatible with one another. For example, the 4 level FSK FM modulation provided by the first described transmitter (100) cannot be properly recovered and decoded using the second described receiver (225). Therefore, a selection of either one or the other transmitter/receiver (100/125 or 200/225) for use in a particular system will preclude an ability to compatibly select later the previously undesignated transmitter/receiver.

Referring now to FIGS. 3a-c, a solution to this dilemma will be presented.

First, in FIG. 3a, a constant envelope transmitter suitable for transmitting 4 level FSK FM modulation in a 12.5 kHz channel appears as generally depicted by reference numeral 300. This constant envelope transmitter (300) processes incoming 4 level data (301) through a raised cosine Nyquist filter (302) having a roll-off factor of 0.2. Those skilled in the art will note that, whereas the previously described proposed transmitters include Nyquist filters wherein the raised cosine function appears in both the transmitter and receiver as a square root function, here the raised cosine function is not so circumscribed. Instead of distributing the Nyquist filtering between the transmitter and receiver, all Nyquist filtering, in this embodiment, occurs at the transmission end.

Subsequent to Nyquist filtering, a differential encoder (303) processes the Nyquist filtered signal in a band limited filter (304) as a function of $\frac{\pi f T}{\sin(\pi f T)}$. A particular design problem, in this embodiment, involves computing the impulse response of this filter (304). Let

$H(\omega)$ = frequency response of ideal Nyquist raised cosine filter
The normalized corner frequency is 1 rad./sec.
The normalized symbol time (denoted by T) is π seconds.

$$H(\omega) = 1 \qquad \text{where } |\omega| \le 1-\alpha$$

$$H(\omega) = \frac{1}{2} + \frac{1}{2}\cos\left(\frac{\pi(|\omega|-1+\alpha)}{2\alpha}\right) \qquad \text{where } 1-\alpha < |\omega| \le 1+\alpha$$

$$H(\omega) = 0 \qquad \text{where } 1+\alpha < |\omega|$$

the impulse response of the filter may then be found using the inverse Fourier transform:

$$h(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} H(\omega)e^{j\omega t}d\omega$$

$$= \frac{1}{\pi}\int_{0}^{\infty} H(\omega)\cos(\omega t)d\omega \qquad \text{since } H(\omega) \text{ is an even function}$$

$$= \frac{1}{\pi}\int_{0}^{1-\alpha}\cos(\omega t)d\omega + \frac{1}{2\pi}\int_{1-\alpha}^{1+\alpha}\cos(\omega t)d\omega + \frac{1}{2\pi}\int_{1-\alpha}^{1+\alpha}\cos\left(\frac{\pi(\omega-1+\alpha)}{2\alpha}\right)\cos(\omega t)d\omega$$

The product rule, cosine (x) cosine (y) equals 0.5 cosine (x + y) + 0.5 cosine (x - y) is then used, and the integration then performed.

$$h(t) = \frac{\sin((1-\alpha)t)}{\pi t} + \frac{\sin((1+\alpha)t)-\sin((1-\alpha)t)}{2\pi t} + \frac{\sin(\pi+(1+\alpha)t)-\sin((1-\alpha)t)}{4\pi\left(\frac{\pi}{2\alpha}+t\right)}$$

$$+ \frac{\sin(\pi-(1+\alpha)t)+\sin((1-\alpha)t)}{4\pi\left(\frac{\pi}{2\alpha}-t\right)}$$

Next, use $\sin(\pi + x) = -\sin(x)$, and algebraically regroup the terms to yield the following result.

$$h(t) = \frac{\pi}{8\alpha^2 t} \frac{\sin((1+\alpha)t) + \sin((1-\alpha)t)}{\left(\frac{\pi}{2\alpha}\right)^2 - t^2}$$

Finally, using sine (x + y) + sine (x - y) equals 2 sine (x) cosine (y), one obtains

$$h(t) = \frac{\pi\sin(t)\cos(\alpha t)}{t(\pi^2-4\alpha^2t^2)}$$

The filter function h(t) can now be sampled at discrete time intervals to realize a Nyquist raised cosine finite impulse response (FIR) filter in a DSP embodiment.

Now, consider the shaping filter f(t). If we let F(ω) equal the frequency response of the shaping filter (304), and T equals symbol time equal 208.333 microseconds for 9600 bps equal π seconds for the normalized system used in H above, then

$$F(\omega) = \frac{\frac{\omega T}{2}}{\sin\left(\frac{\omega T}{2}\right)}$$

for all frequencies. With a roll-off factor of 0.2 for the Nyquist filter $H(\omega)$, $-1.2\pi < \omega T < 1.2\pi$ becomes the

frequency range of interest for F(ω). Such a filter function cannot be directly integrated with elementary calculus. Numerical methods could be used to compute the inverse Fourier integral, but that presents significant difficulties. A discrete Fourier transform method could be used or the FFT version of this transform could be used, to speed up the calculation. Such methods would be suitable presuming availability of sufficient processing abilities. In this embodiment, however, another method is preferred. Here, the function F will be approximated with a Fourier series of cosine terms that are then transformed to the time domain. To begin, select a suitable time interval that approximates F. This must equal or exceed plus or minus 1.2π and be less than plus or minus 2π since a singularity in F exists at WT equals to π. Plus or minus 1.3333π constitutes a useful interval, since this allows the samples to be spaced six samples apart when over sampling H by a factor of 8.

With the above in mind,

$$F(x) = \frac{\pi x}{\sin(\pi x)} \quad \text{where } x = \text{normalized frequency} = fT = \frac{\omega T}{2\pi}$$

$$= fo + \sum_{k=1}^{\infty} f_k \cos\left(\frac{2\pi k x}{1.33333}\right)$$

which is the Fourier series expansion

$$fo = 0.75 \int_{-2/3}^{2/3} F(x)dx$$

$$f_k = 1.5 \int_{-2/3}^{2/3} F(x)\cos\left(\frac{2\pi k x}{1.33333}\right)dx \quad \text{for } k > 0$$

These integrals are easily evaluated numerically. The first 12 terms are tabulated below.

TABLE 1

k	f_k
0	1.35697
1	-0.4839
2	0.189043
3	-0.0982102
4	0.0594481
5	-0.0396059
6	0.0281791
7	-0.0210304
8	0.0162746
9	-0.0129571
10	0.0105541
11	-0.00875928

Upon plotting the function F(x) and its Fourier series approximation, one ascertains a sufficiently close relationship. The series is within 1% of the desired value at most places in the passband of the Nyquist filter, though the error does approximate 2% near the band edge just before the Nyquist filter cuts off.

The inverse Fourier transform can then be performed on the series as follows:

$$f(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} F(\omega)e^{j\omega t}d\omega$$

$$= \frac{1}{2\pi}\int_{-\infty}^{\infty}\left(fo + \sum_{k=1}^{\infty} f_k \cos\left(\frac{k\omega T}{1.33333}\right)\right)e^{j\omega t}d\omega$$

$$= \frac{1}{2\pi}\left(f_0\,\delta(t) + \sum_{k=1}^{\infty} \frac{f_k}{2}\,\delta(t+0.75kT) + \sum_{k=1}^{\infty} \frac{f_k}{2}\,\delta(t-0.75kT) \right)$$

where the Dirac delta function is represented as $\delta(t)$.

Upon sampling at eight samples per symbol, non-zero samples are obtained at 0.75 X 8 = 6 sample intervals. The middle or zeroth sample has amplitude f0 and the remaining samples have amplitudes f_k /2 for k equals plus or minus 1, plus or minus 2, plus or minus 3, and so forth. This can then be cascaded with the h(t) function computed above to yield the filters necessary for this filter.

Subsequent to filtering, an integration function (306) completes the differential encoding process. Then, the signal can be frequency modulated as a function of $e^{j(\phi+\omega t)}$,while maintaining a deviation index of 0.25. The resultant modulation can then be appropriately amplified and transmitted in accordance with a particular application.

FIG. 3b depicts a non-constant envelope transmitter (325) suitable for use in transmission of a $\pi/4$ differential QPSK signal having a bandwidth of 6.25 kHz. A summer (327) receives a 4 level data input (326) and sums that with a feedback signal (328). This provides a differential encoder process as generally referred to above with respect to FIG. 2a. Also as presented in FIG. 2a, a phase modulator (329) processes the signal and provides complex in-phase and quadrature components at one sample per symbol. These components are then filtered in a raised cosine Nyquist filter (331). As with the constant envelope transmitter (300) described above,

this raised cosine Nyquist filter (331) has a roll-off factor of 0.2, and does not process the signal as a function of a square root of the raised cosine. Instead, all Nyquist processing from source to destination occurs in the transmitter (325). Subsequent to Nyquist filtering, a mixer (332) mixes the information signal with an appropriate carrier frequency (333) and the desired $\pi/4$ differential QPSK modulation results.

FIG. 3c depicts a receiver suitable for use in receiving and decoding modulation from either of the above described transmitters (300 and 325). Received modulation (351) couples to a loose IF filter (352). Design of this IF filter crucially affects the ability of the receiver (350) to properly receive either a wide frequency modulation signal (as presented in a 12.5 kHz channel) or a narrow linear modulation signal (as presented in a 6.25 kHz channel). In particular, the IF design must accommodate a pass bandwidth wide enough and flat enough to avoid intersymbol interference while having a stop bandwidth that is narrow enough to allow 6.25 kHz channel spacing. The constraints on the filter design are presented in FIG. 4 for a system with 9600 bits/second of throughput in a 6.25 kHz channel. As noted above, a Nyquist raised cosine filter having a roll-off factor of 0.2 appears in the transmitter. The stop bandwidth limit is 6.25 kHz while the pass bandwidth limit is designed to exceed

$$(1+\alpha)\frac{9600}{2} = 5.76 \text{ kHz.}$$

Due to the very demanding transition ratio,

$$r = \frac{\text{stop bandwidth}}{\text{pass bandwidth}} < \frac{6.25}{5.76} = 1.085$$

the number of necessary filter coefficients is about 350 when implementing such a filter in a single finite impulse response configuration. Since computation complexity is directly proportional to the number of filter coefficients, this constitutes an obvious drawback. In this embodiment, the loose IF filter (352) uses two FIR filters in a DSP embodiment. In particular, a decimating filter first narrows the bandwidth enough to reduce the sample rate for introduction to the subsequent filter, the latter providing a rapid filter roll-off. Both FIR filters in this embodiment are equi-ripple designs. The first FIR filter attains 80 db of stop band rejection with a stop frequency of 4.68 kHz and a pass frequency of 3 kHz. The second FIR filter has a stop frequency of 3.00 kHz and a pass frequency of 2.88 kHz. Parameters for both FIR filters appear in Table 2, below.

TABLE 2

Parameter	FIR 1	FIR 2
f_s= sample frequency	38.4 kHz	7.68 kHz
f_1= passband corner frequency	3.00 kHz	2.88 kHz
f_2= stopband corner frequency	4.68 kHz	3.00 kHz
r = transition ratio = f_1/f_2	1.56	1.04165
stopband rejection	100 dB	57.5 dB
passband ripple	0.0012 dB	0.4 dB
number of filter coefficients	128	128

Even though the second FIR filter attains a tighter transition ratio than the specified requirement for a 6.25 kHz channel, it does so with fewer filter coefficients than the previously referred to approach.

Subsequent to IF filtering, a frequency demodulator (353) demodulates constant envelope information. To this extent, the frequency demodulator includes an inverse tangent block (354), a differential summer (356) and a unit sample delay path (357) as essentially described above with respect to the proposed 4 level FSK receiver (125).

The receiver (350) also includes a differential decoder (358) substantially as described above for the $\pi/4$ differential QPSK receiver (255), inclusive of the unit sample delay path (357) and the differential summer (356), in conjunction with an integrate and dump filter (359). The integrate and dump filter essentially comprises a linear filter that integrates over a predetermined sample period and then dumps historical data in preparation for a new integration window. The impulse response for the integrate and dump filter appears in FIG. 5a, where the vertical scale represents normalized amplitude and the horizontal scale represents normalized time in seconds for T = 1 second. A corresponding frequency response (reflective of the familiar $\frac{\sin(\pi f T)}{\pi f T}$ filter response) appears in FIG. 5b, where the vertical scale again represents normalized amplitude and the horizontal scale represents normalized frequency in Hertz for T = 1 second. In this integrate and dump filter (359), some portion of the side lobes are filtered out of the frequency response, therefore yielding a band limited filter. To achieve perfect symbol recovery, a frequency response in the range of $\frac{-(1+\alpha)}{2T}$ Hz to $\frac{1+\alpha}{2T}$ Hz

must be retained. Taking advantage of the spectral null at 1/T Hz, the response is restricted to a low pass filter cutoff at 1/T Hz. The resulting frequency response appears in FIG. 5c, where the vertical and horizontal scales are as described earlier for FIG. 5b.

The impulse response for this filter (359) can be directly calculated with an inverse Fourier transform. A closed form solution can be expressed in terms of the sine integral function Si (X) as shown below.

Let $H(x)$ = frequency response of bandlimited filter

$$= \frac{\sin(\pi x)}{\pi x} \qquad \text{for } |x| < 1$$

$$= 0 \qquad \text{for } |x| \geq 1$$

$h(t)$ = inverse Fourier transform of $H(x)$ Let $\omega = 2\pi x$

$$= \frac{1}{\pi}\int_0^{2\pi} \frac{2}{\omega} \sin\left(\frac{\omega}{2}\right)\cos(\omega t)d\omega \quad \text{since } H(\omega) \text{ is an even function}$$

$$= \frac{1}{\pi}\int_0^{2\pi} \frac{1}{\omega} \left(\sin((t+\frac{1}{2})\omega)-\sin((t-\frac{1}{2})\omega)\right)d\omega \quad \text{using a trig identity}$$

$$\frac{1}{\pi}\left(\int_0^{2\pi(t+1/2)} \sin(y)\frac{dy}{y} - \int_0^{2\pi(t-1/2)} \sin(y)\frac{dy}{y}\right) \quad \text{substituting variables}$$

$$= \frac{1}{\pi}\left(\sin(2\pi(t+\frac{1}{2}))-\sin(2\pi(t-\frac{1}{2}))\right) \text{ where } Si(x) = \int_0^x \frac{\sin(t)}{t}\,dt$$

Following this, a stochastic gradient bit recovery mechanism (361) is again provided and the resultant 4 level data recovered.

So configured, a number of salient points should now be evident to those skilled in the art. First, the receiver provides no Nyquist filtering. All Nyquist filtering occurs in the transmitters. (The rolloff ratio constitutes the important variable to be controlled in a Nyquist filter. In prior art transceivers using Nyquist filters, this ratio must be identical for both the transmitter filter and the receiver filter. Here, the receiver is independent of this variable, and can receive signals from different transmitters that use different values for the rolloff ratio.) Second, the receiver can effectively demodulate and recover either constant envelope signals or non-constant envelope signals, such as 4 level FSK FM or $\pi/4$ differential QPSK linear modulation. Third, this receiver can accommodate these alternative modulation types, notwithstanding differing channel widths, in this case 12.5 kHz and 6.25 kHz, respectively.

With the architectures described above, a system operator can select to realize the advantages of digital signalling by fielding 4 level FSK FM transmitters coupled with the described compatible receiver. At such time as linear transmission technologies make viable economic fielding of $\pi/4$ differential QPSK transmitters, the operator can introduce such transmitters into a system in conjunction with the same compatible receiver as used for the constant envelope transceivers. Notwithstanding differing modulation types and differing bandwidth requirements, the same receiver platform allows compatible communication between these differing units.

What is claimed is:

Claims

1. A radio transceiver, comprising:

A) a transmitter, which transmitter includes a Nyquist filter; and

B) a receiver, which receiver does not include a Nyquist filter.

2. A radio transceiver, comprising:

A) a transmitter, comprising at least a Nyquist filter and transmitting at least one of:

i) a constant envelope signal; and

ii) a non-constant envelope signal; and

B) a receiver, which receiver does not have a Nyquist filter, for receiving and properly demodulating both:

i) a constant envelope signal; and

ii) a non-constant envelope signal.

3. A radio transceiver, comprising:

A) a transmitter, comprising at least a Nyquist filter and transmitting at least one of:

i) a constant envelope signal occupying a first spectral bandwidth; and

ii) a non-constant envelope signal occupying a second spectral bandwidth, which second spectral bandwidth is different from the first spectral bandwidth; and

B) a receiver, which receiver does not have a Nyquist filter, for receiving and properly demodulating both:

i) a constant envelope signal occupying the first spectral bandwidth; and

ii) a non-constant envelope signal occupying the second spectral bandwidth.

4. A radio transceiver, comprising:

A) a transmitter, comprising:

i) a Nyquist filter;

ii) differential encoder means coupled to the Nyquist filter for filtering an input information signal to cause selective rotation of a phase value of a modulated signal by a predetermined amount; and

iii) frequency modulator means operably coupled to the differential encoder means for outputting the modulated signal; and

B) a receiver, which receiver does not have a Nyquist filter, for receiving and properly demodulating both:

i) a constant envelope signal occupying a first spectral bandwidth; and

ii) a non-constant envelope signal occupying a second spectral bandwidth, wherein the first spectral bandwidth is different from the second spectral bandwidth.

5. A radio communication system, comprising:

A) a first plurality of transceivers, each transceiver comprising:

i) a transmitter, comprising at least a Nyquist filter and transmitting a constant envelope signal occupying a first spectral bandwidth;

ii) receiver means, which receiver means does not have a Nyquist filter, for receiving and properly demodulating both:

a) a constant envelope signal occupying the first spectral bandwidth; and

b) a non-constant envelope signal occupying a second spectral bandwidth, which second spectral bandwidth is different than the first spectral bandwidth;

B) a second plurality of transceivers, each comprising:

i) a transmitter, comprising at least a Nyquist filter and transmitting a non-constant envelope signal occupying the second spectral bandwidth; and

ii) receiver means, which receiver means does not have a Nyquist filter, for receiving and properly demodulating both:

a) a constant envelope signal occupying the first spectral bandwidth; and

b) a non-constant envelope signal occupying the second spectral bandwidth;

such that transceivers from the first plurality of transceivers can compatibly communicate with transceivers from the second plurality of transceivers.

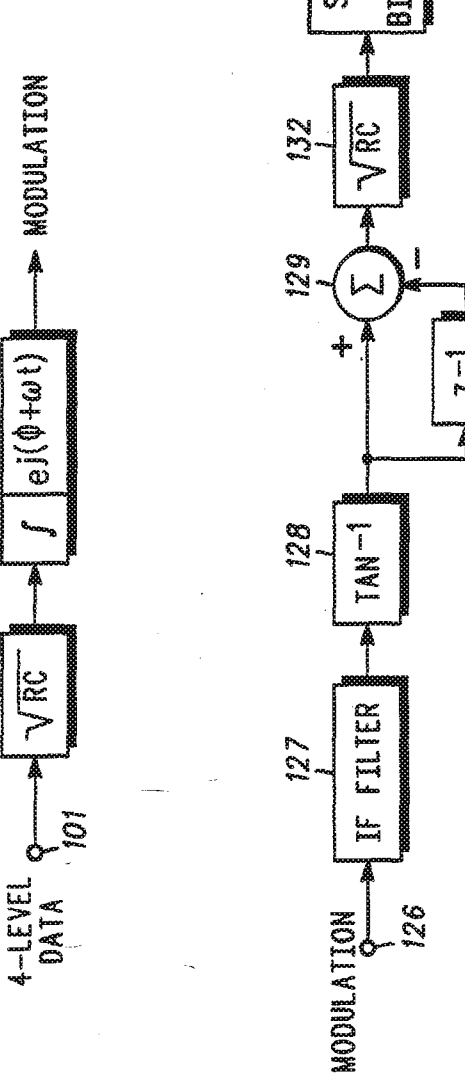

FIG. 1A
— PRIOR ART —

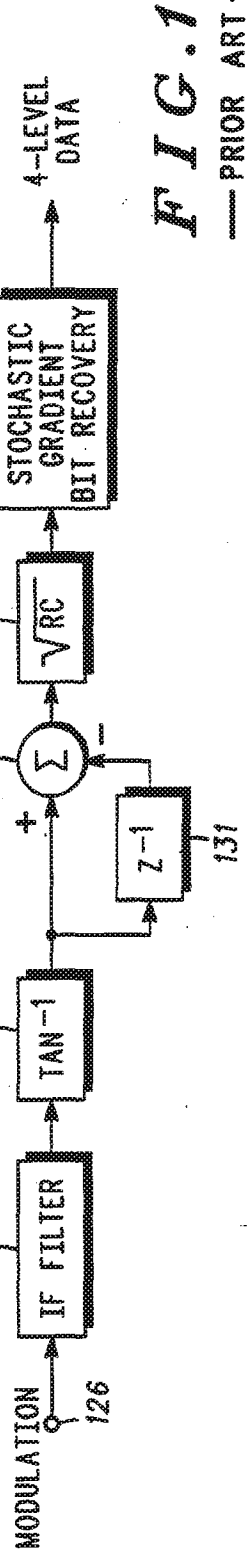

FIG. 1B
— PRIOR ART —

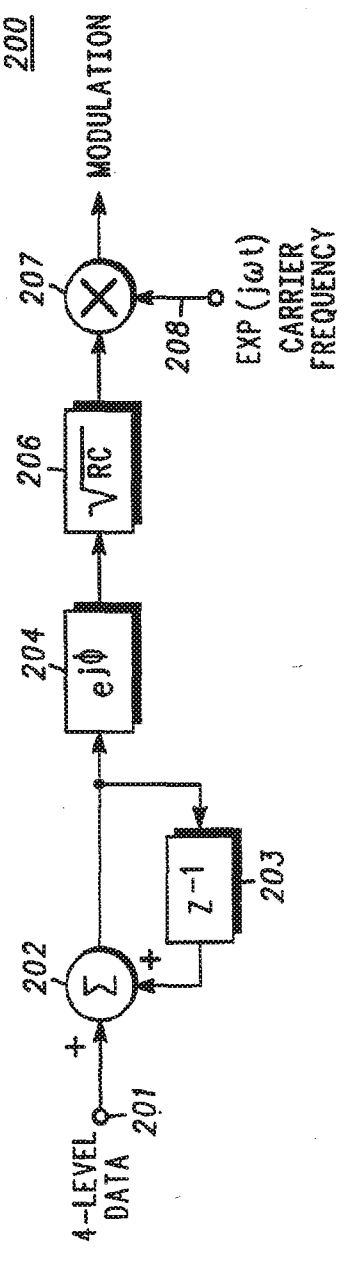

FIG. 2A
— PRIOR ART —

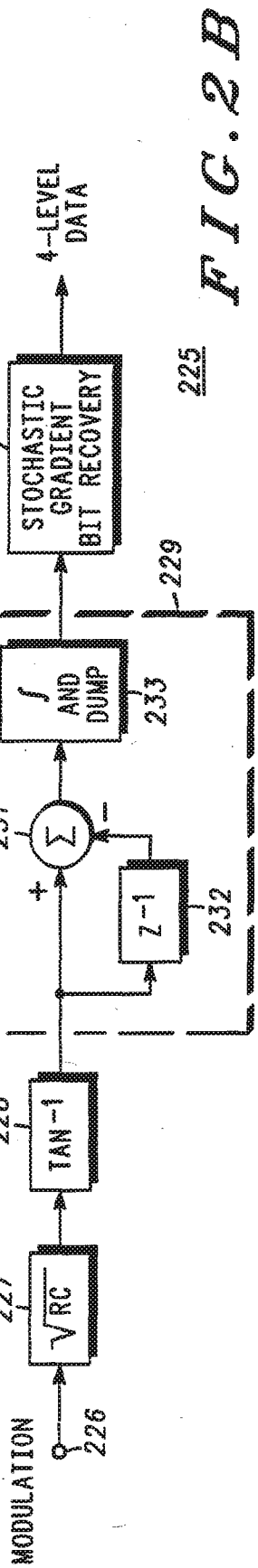

FIG. 2B
— PRIOR ART —

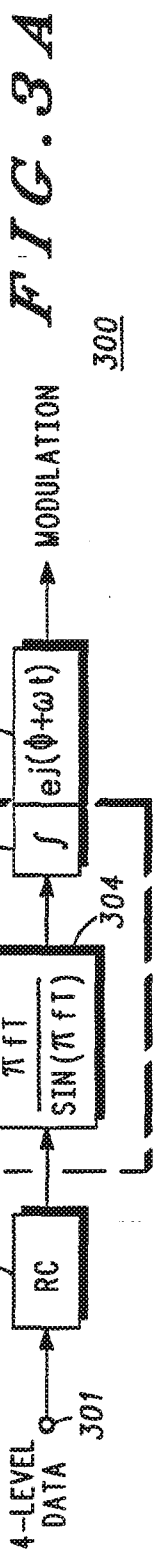

FIG. 3A

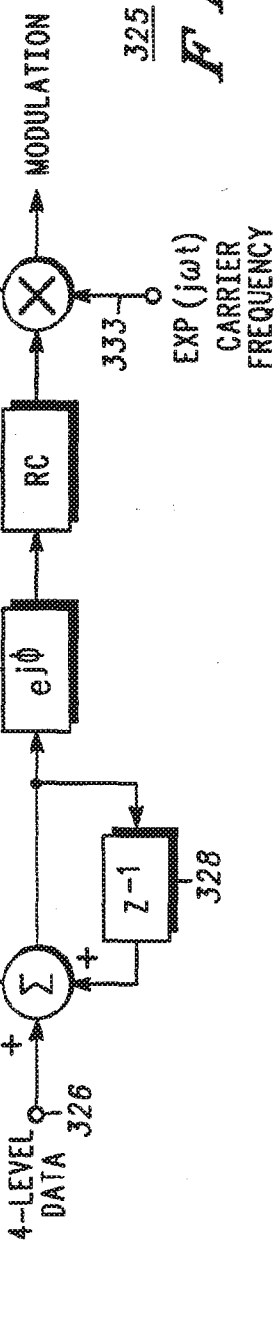

FIG. 3B

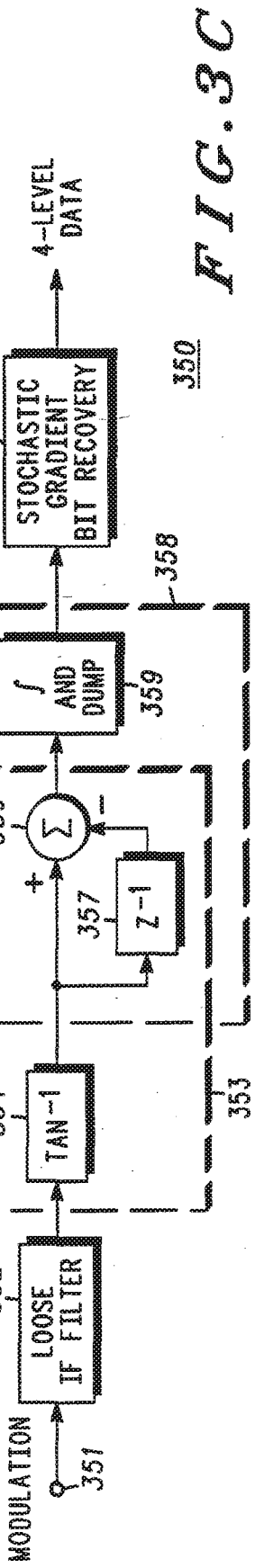
MODULATION
351
LOOSE IF FILTER
352
TAN⁻¹
354
353
Σ
356
357
Z⁻¹
I AND DUMP
359
358
STOCHASTIC GRADIENT BIT RECOVERY
361
4-LEVEL DATA
350

FIG. 3C

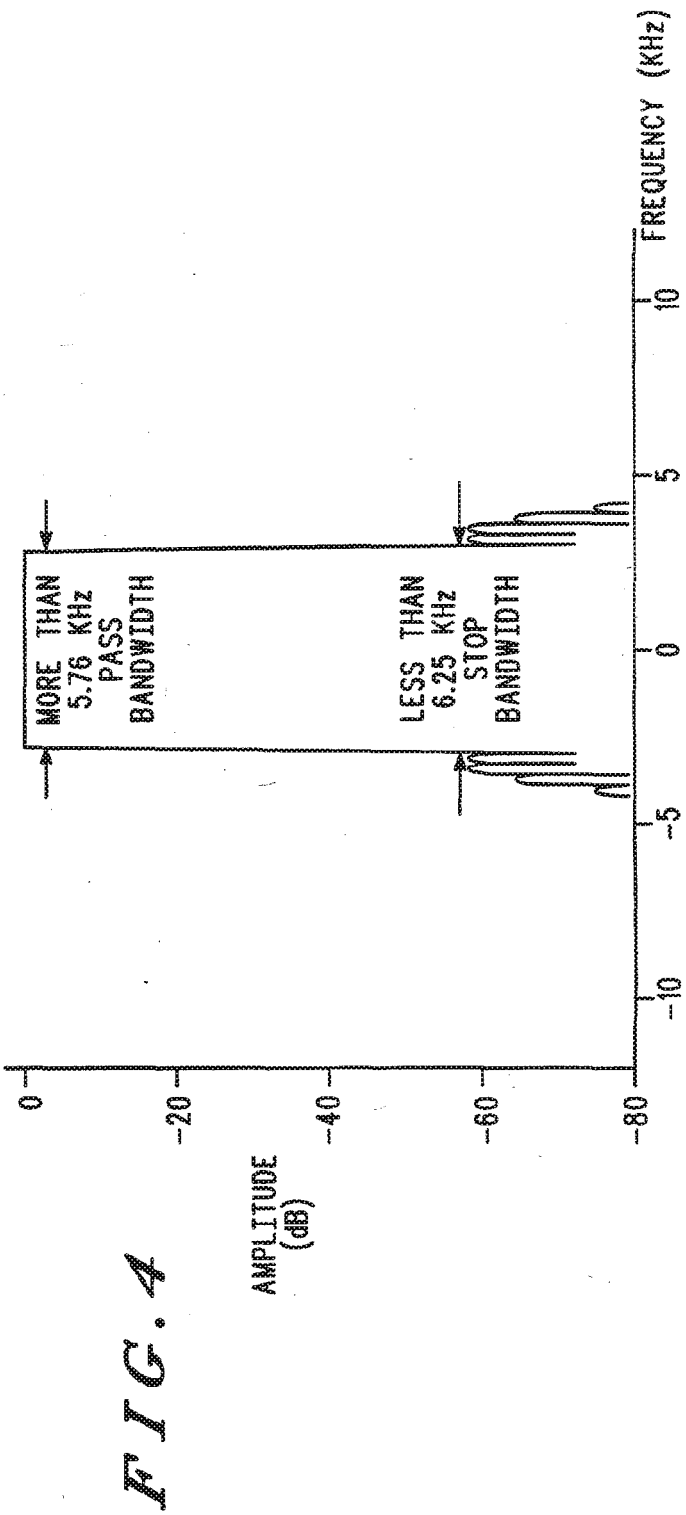
MORE THAN 5.76 KHz PASS BANDWIDTH
LESS THAN 6.25 KHz STOP BANDWIDTH
AMPLITUDE (dB)
0
-20
-40
-60
-80
FREQUENCY (KHz)
10
5
0
-5
-10

FIG. 4

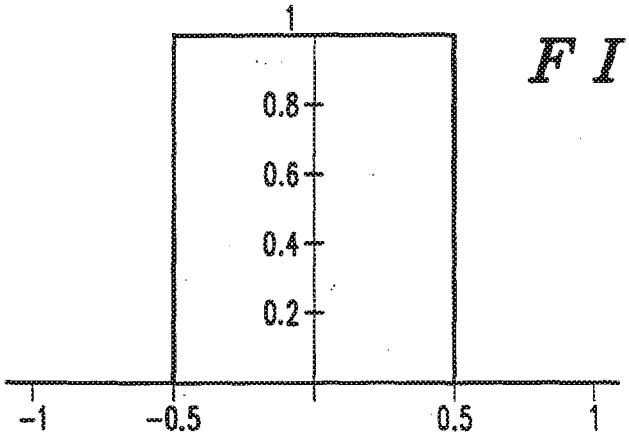

FIG.5A

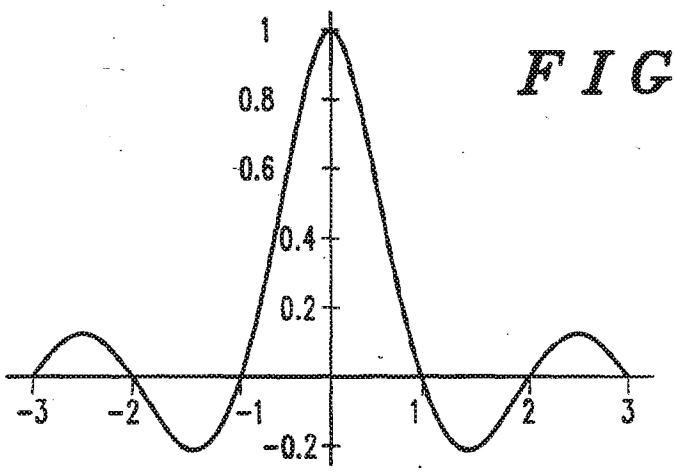

FIG.5B

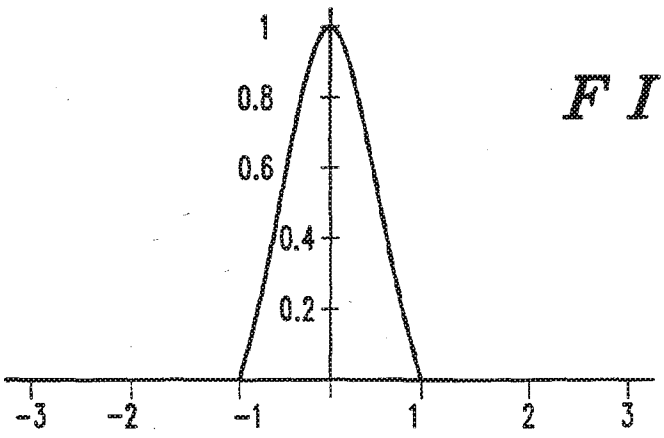

FIG.5C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/05317

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) : H04L 27/10; H04L 27/18
US CL : 375/9
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : U.S. CL 375/8, 44, 45, 51,52, 58, 60,99; 455/49,50, 73, 74, 93, 142; 329/300, 304; 370/123

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A, 4,720,B39 (FEHER) 19 JANUARY 1988 (SEE FIGURE 1B, COL 2 LINES 29-42)	1-3
A	US,A, 4,601,04B (RYAN) 15 JULY 1986	1-5
A	US,A, 4,731,796 (MASTERTON) 15 MARCH 1988	1-5
A	US,A, 4,843,615 (DAVIS) 27 JUNE 1989	1-5

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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Date of the actual completion of the international search 10 SEPTEMBER 1992	Date of mailing of the international search report 21 OCT 1992
Name and mailing address of the ISA/ Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer SAFOUREK, BENEDICT V Telephone No. (703) 305-4364

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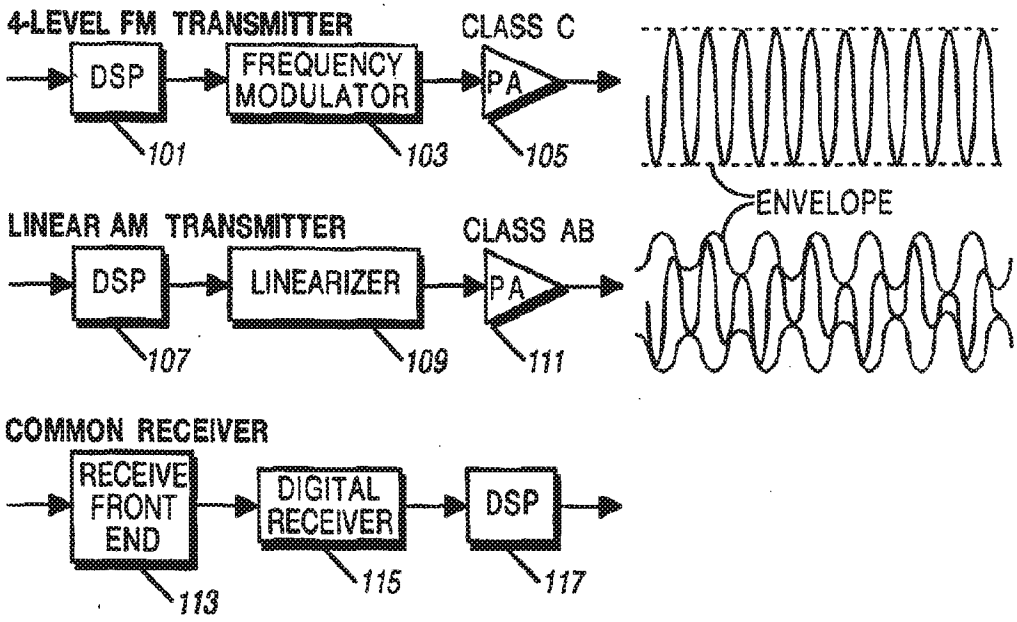
(54) Title: MULTIPLE-MODULATION COMMUNICATION SYSTEM



(57) Abstract

A multiple-modulation communication system includes a transmitter (201, 203, 205, 207, 209, 211, 213, 215, 217, 219) that modulates and transmits communication signals modulated by a first modulation technique (201, 203, 205, 207) and communication signals modulated by a second modulation technique (211, 213, 215, 217). The first modulation technique and the second modulation technique are different. The communication system also includes a receiver (221, 223, 225, 227, 229, 231) capable or receiving the communication signals modulated by the first modulation technique and the communication signals modulated by the second modulation technique and demodulating the communication signals.

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MULTIPLE-MODULATION COMMUNICATION SYSTEM

Field of the Invention

This invention relates to radio frequency signals, including but not limited to transmission and reception of amplitude modulated (AM) and frequency modulated (FM) signals.

Background of the Invention

A radio communication system permits transmission of information between a transmitter and a receiver. A radio frequency (RF) channel permits transmission of information between the transmitter and the receiver. By combining the information with an RF electromagnetic wave of a particular frequency, i.e., modulating the information signal onto a carrier frequency, the resultant modulated information signal may be transmitted through free space to a receiver. Various modulation techniques (e.g., amplitude (AM), frequency (FM), phase, and composite modulation) are known to combine the information signal with an electromagnetic wave. Communication units, such as portable radios, mobile radios, and base stations, contain transmitters and/or receivers.

A linear AM transmitter does not have as much coverage area, i.e., the signal does not travel as far, as an FM transmitter at the same peak transmit power level because the average envelope size of an AM transmission varies below the maximum output level, whereas the average envelope size of an FM transmission is constant at the maximum output level. An FM transmitter,

however, uses more energy to transmit at the same power level as an AM transmitter, and hence the FM transmitter will more quickly drain the battery of a portable transmitter.

Accordingly, there is a need for a transmitter which has the low power characteristic of an AM transmitter while retaining the advantage of coverage area of an FM transmitter.

Brief Description of the Drawings

FIG. 1 shows an FM transmitter, an AM transmitter, and a common receiver in accordance with the invention.

FIG. 2 shows a detailed FM transmitter, a detailed AM transmitter, and a detailed common receiver in accordance with the invention.

Description of a Preferred Embodiment

The following describes an apparatus for and method of transmitting communication signals with a single transmitter and receiving the same signals with a single receiver. Additional communication range is obtained when transmitting FM signals. More efficient battery performance is achieved when transmitting linear AM signals. A single transmitter transmits both AM and FM signals. A single receiver capable of differentiating phase differences demodulates either AM or FM signals. Only one receiver is necessary, and there is no need to inform the receiver of what type of modulation was performed on the transmitted signal.

In the preferred embodiment, FM modulators have 12.5 kHz channels and linear AM modulators have 6.25 kHz channels. The receiver can be the same in either case. The form of modulation used in the present invention is called QPSK-c. This modulation technique is discussed in detail in U.S. Application No. 07/629,931 titled "Multi-Modulation Scheme Compatible Radio" filed on behalf

of Alan L. Wilson et al. on December 19, 1990, which information is enclosed herein by reference. QPSK stands for Quaternary Phase Shift Keying. QPSK-c, where the c stands for compatible, is a linear differential form of QPSK that is AM and FM compatible. It is possible to transmit with a higher average power using FM, and hence increased coverage area is obtained for the signal than when AM is used. An AM transmitter, however, consumes less power and hence is a more efficient user of a portable radio's battery charge or power than an FM transmitter. When using QPSK-c modulation, 4-level FSK (Frequency Shift Keying) is used in FM transmissions and D-QPSK (Differential QPSK) is used in AM transmissions. Switching from AM to FM yields higher average power, and hence increased coverage area for the signal, at the cost of battery charge. Thus range is enhanced and greater coverage is obtained for the same radio, or communication unit, when such coverage is desired. Conversely, switching from FM to AM when extended range is not necessary conserves battery charge. In the present invention, the communication unit changes its type of modulation and thus is more quickly responsive to such a change. This is accomplished by, inter alia, an $x/(\sin x)$ filter, where $x = \pi fT$ in the preferred embodiment, and a phase angle integrator for the exponential function.

One part of FIG. 1 shows a conventional four-level FM transmitter. Information to be transmitted enters a digital signal processor (DSP) 101. The DSP 101 processes the information and sends it to frequency modulator 103 which passes the information to power amplifier (PA) 105 which is rated class C. As shown in FIG. 1, a class C four-level FM transmitter transmits a constant envelope.

A conventional linear AM transmitter is also shown in FIG. 1. Information to be transmitted is processed in DSP 107 and output to a conventional linearizer 109, the output of which is input to a class AB power amplifier 111. As seen in the diagram, an AM signal has a non-constant envelope. The average signal power of

an AM signal is less than the average signal power of an FM signal having the same peak envelope size.

Also shown in FIG. 1 is a common receiver which may receive information from both four-level FM transmitter and linear AM transmitters. The common receiver has a front-end receiver 113, a digital receiver 115, and a digital signal processor 117 that processes the information into data or audible speech. A linear AM transmitter has a time-varying amplitude that is reduced for high frequency deviation. Note that DSP 101, DSP 107, and DSP 117 also perform functions other than those shown. Throughout the specification and drawings, the DSP as shown may be a DSP 56001 available from Motorola, Inc.

FIG. 2 shows a detailed implementation of the transmitters and receiver of FIG. 1. An FM transmitter, yielding 4-level FSK data, is shown by blocks 201, 203, 205 and 207. 4-level data is input to a raised-cosine filter 201 which is a splatter filter of the Nyquist raised-cosine finite impulse response type with splatter filter transition ratio alpha = 0.2, as is known in the art. The FM transmitter includes a differential encoder comprised of blocks 203 and 205. A π fT/sin(π fT) filter 203 and an integrator 205 comprise the differential encoder. In the preferred embodiment, the integrator 205 is a simple integrator that uses the modulo 2π property of the phase to avoid overflowing, as is known in the art. The output of integrator 205 is the phase ϕ of the 4-level input signal. A detailed description of one implementation of the raised-cosine filter 201 and π fT/sin(π fT) filter 203 follows in the next paragraph. Phase modulator 207 takes the phase ϕ and modulates it, creating a complex-valued result that is designated $e^{j\phi}$. The output, $e^{j\phi}$, of phase modulator is input to switch 209.

The cascaded filter implementation of the Nyquist raised-cosine filter 201 and the π fT/sin(π fT) filter 203 may be implemented as follows. Let $H(\omega)$ equal the frequency response of an ideal Nyquist raised cosine filter. The normalized corner frequency is 1 radian/second, and the normalized symbol time (denoted by T) is π seconds, and

$$H(\omega) = 1 \quad \text{for } 1 - \alpha \geq |\omega|$$
$$H(\omega) = \frac{1}{2} + \frac{1}{2}\cos\left(\frac{\pi(|\omega| - 1 + \alpha)}{2\alpha}\right) \quad \text{for } 1 - \alpha < |\omega| \leq 1 + \alpha$$
$$H(\omega) = 0 \quad \text{for } 1 + \alpha < |\omega| .$$

The impulse response, h(t), of the filter is found with the inverse Fourier transform, and noting that H(ω) is an even function:

$$h(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} H(\omega)e^{j\omega t}d\omega = \frac{1}{\pi}\int_{0}^{\infty} H(\omega)\cos(\omega t)\,d\omega$$

$$= \frac{1}{\pi}\int_{0}^{1-\alpha} \cos(\omega t)\,d\omega + \frac{1}{2\pi}\int_{1-\alpha}^{1+\alpha} \cos(\omega t)\,d\omega + \frac{1}{2\pi}\int_{1-\alpha}^{1+\alpha} \cos\left(\frac{\pi(\omega-1+\alpha)}{2\alpha}\right)\cos(\omega t)\,d\omega$$

Using the identity $\cos(x)\cos(y) = 0.5\cos(x+y) + 0.5\cos(x-y)$ and performing the integration:

$$h(t) = \frac{\sin[(1-\alpha)t]}{\pi t} + \frac{\sin[(1+\alpha)t] - \sin[(1-\alpha)t]}{2\pi t}$$
$$+ \frac{\sin[\pi+(1+\alpha)t] - \sin[(1-\alpha)t]}{4\pi\left(\frac{\pi}{2\alpha} + t\right)} + \frac{\sin[\pi-(1+\alpha)t] + \sin[(1-\alpha)t]}{4\pi\left(\frac{\pi}{2\alpha} - t\right)}.$$

Using the identity $\sin(\pi+x) = -\sin(x)$, regrouping terms, and then using the identity $\sin(x+y) + \sin(x-y) = 2\sin(x)\cos(y)$:

$$h(t) = \frac{\pi}{8\alpha^2 t}\,\frac{\sin[(1+\alpha)t] + \sin[(1-\alpha)t]}{\left(\frac{\pi}{2\alpha}\right)^2} = \frac{\pi\sin(t)\cos(\alpha t)}{\alpha^2} .$$

The filter function h(t) can be sampled at discrete time intervals to realize the Nyquist raised-cosine finite impulse response filter 201.

The shaping filter, f(t), is derived as follows, where F(ω) is the frequency response of the shaping filter, T is the symbol time which equals 208.333 μsec for 9600 bits per second which equals π seconds for the normalized system used in H above, and

$$F(\omega) = \frac{\omega T/2}{\sin(\omega T/2)} \quad \text{for all frequencies.}$$

The frequency range of interest for $F(\omega)$ is $-1.2\pi < \omega T < 1.2\pi$, which is the frequency range covered by the Nyquist filter $H(\omega)$ when the roll-off factor $\alpha = 0.2$. In order to find a suitable impulse response, the function F will be approximated with a Fourier series of cosine terms, and the result will be transformed to the time domain.

A time interval to approximate F is first selected to be $\pm 1.33333\pi$, because it must exceed $\pm 1.2\pi$ and be less than $\pm 2\pi$ because there is a singularity in F at $\omega T = 2\pi$. The Fourier series expansion follows, where x is the normalized frequency:

$$F(x) = \frac{\pi x}{\sin(\pi x)} = f_0 + \sum_{k=1}^{\infty} f_k \cos\left(\frac{2\pi k x}{1.33333}\right) \text{ where } x = fT = \frac{\omega T}{2\pi},$$

$$f_0 = 0.75 \int_{-2/3}^{2/3} F(x)\, dx, \text{ and}$$

$$f_k = 1.5 \int_{-2/3}^{2/3} F(x) \cos\left(\frac{2\pi k x}{1.33333}\right) dx \quad \text{for } k > 0.$$

These integrals are easily evaluated numerically. The first twelve terms appear in the following table.

k	f_k	k	f_k
0	1.35697	6	0.0281791
1	-0.4839	7	-0.0210304
2	0.189043	8	0.0162746
3	-0.0982102	9	-0.0129571
4	0.0594481	10	0.0105541
5	-0.0396059	11	-0.00875928

Performing the inverse Fourier transform on the series as follows:

$$f(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} F(\omega)e^{j\omega t}d\omega = \frac{1}{2\pi}\int_{-\infty}^{\infty}\left(f_0 + \sum_{k=1}^{\infty} f_k \cos\left(\frac{2\pi kx}{1.33333}\right)\right)e^{j\omega t}\,d\omega$$

$$= \frac{1}{2\pi}\left(f_0\delta(t) + \sum_{k=1}^{\infty}\frac{f_k}{2}\delta(0.75\ kT) + \sum_{k=1}^{\infty}\frac{f_k}{2}\delta(-0.75\ kT)\right)$$

where $\delta(t)$ represents the Dirac delta function. Sampling at 8 samples per symbol yields non-zero samples and 0.75 x 8 = 6 sample intervals. The middle or 0th sample has amplitude f_0, and the remaining samples have amplitudes $f_k/2$ for k=±1, ±2, ±3,... Cascading the previously computed h(t) with f(t) yields the filters necessary for an FM $\pi/4$ DQPSK-c transmitter, as used in the preferred embodiment of the present invention. Although the above implementation is shown in band-limited form, band-limiting is optional and is not required for the present invention.

The AM transmitter, yielding D-QPSK data, is comprised of blocks 211, 213, 215, and 217. Four level data having levels of $\pm\pi/4$ and $\pm 3\pi/4$ enters a differential encoder comprised of a summer 211 and a delay 213. The output of this differential encoder enters a phase modulator 215, where the output of the phase modulator 215 has complex components I and Q at one sample per symbol. I represents the in-phase component, and Q represents the quadrature component. The output of modulator 215 is input to raised cosine filter 217 with alpha = 0.2 where raised cosine filter 217 is similar to raised cosine filter 201. The output of raised cosine filter 217 is input to switch 209. Whichever form of transmission is selected, either FM or AM, the output of that part of the transmitter is input to modulator 219, which modulates the signal to the carrier frequency ω.

Blocks 211, 213, and 215 each operate at the rate of one sample/symbol or 4800 symbols/second. Blocks 201 and 217 interpolate from 1 sample/symbol to N samples/symbol at the

output, where N is usually 10 or more, but at least greater than one. Blocks 203, 205, and 207 each operate at N samples/symbol.

For efficiency and to eliminate redundant parts in the preferred embodiment, only one class AB PA is used in the transmitter, thus the linear AM transmitter configuration of FIG. 1 is used to embody the entire transmitter of FIG. 2, blocks 201 through 219 inclusive. Because the preferred embodiment of the present invention uses a DSP, transmitter blocks 201, 203, 205, 207, 209, 211, 213, 215, 217, and 219 are easily implemented in the DSP 107 of the linear AM transmitter. Because blocks 201 through 219 are included in the DSP 107, it is unnecessary to duplicate DSP 101, frequency modulator 103, and PA 105. The modulator 219 is also implemented in the DSP 107, and the output of the modulator 219 is input to the linearizer 109 prior to transmission.

A detailed common receiver is also shown in FIG. 2. In the preferred embodiment, the receiver blocks 221, 223, 225, 227, 229, and 231 are all implemented in the DSP 117. When the receiver and transmitter are in the same communication unit or radio, one or more DSPs may be used to support the functions of DSP 107 and DSP 117. A loose IF (intermediate frequency) filter 221, first receives a modulated signal. The output of the loose IF filter 221 is input to inverse tangent function 223, which is part of a frequency demodulator including blocks 223, 225 and 227. Blocks 225 and 227 are also part of a differential encoder also including integrate and dump filter 229, the function of which is described in detail in the following paragraph. The output of block 223 is input to summer 227 and the positive form of the delayed component is subtracted from block 227 as output from block 225. The output of integrate and dump filter 229 is input to stochastic gradient bit recovery block 231 the output of which is four level data as transmitted initially. Stochastic gradient bit recovery is well known in the art. Because the receiver is sensitive only to phase, the envelope does not matter and both FM and AM transmission may be received and properly decoded by this common receiver. Thus, because a more powerful AM PA is required than for an FM PA for the same

range, a switch of the two modulations temporarily although draining more power gains extra (greater) coverage area.

The impulse response for the integrate and dump filter 229 is derived below, in a closed-form solution that is expressed in terms of the sine integral function Si(x), which is well known in the art. A band-limited integrate and dump filter is achieved when a portion of the side lobes are filtered out of the frequency response. The portion of the frequency response that is necessary for good fidelity in the symbol recovery is in the range $-(1+\alpha)/(2T)$ Hz to $(1+\alpha)/(2T)$ Hz. Because of a spectral null at 1/T Hz, the response is restricted to 1/T Hz cutoff. Where H(x) is the frequency response of a band-limited integrate and dump filter:

$$H(x) = \frac{\sin(\pi x)}{\pi x} \quad \text{for } |x| < 1$$

$$H(x) = 0 \quad \text{for } |x| \geq 1.$$

Where h(t) is the impulse response of the filter H(x), $\omega = 2\pi x$, and $H(\omega)$ is an even function:

$$h(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} H(\omega)e^{j\omega t}d\omega = \frac{1}{2\pi}\int_{-2\pi}^{2\pi} \frac{\sin(\omega/2)}{\omega/2} e^{j\omega t}d\omega$$

$$= \frac{1}{\pi}\int_{0}^{2\pi} \frac{2}{\omega}\sin(\omega/2)\cos(\omega t)\,d\omega$$

$$= \frac{1}{\pi}\int_{0}^{2\pi} \frac{1}{\omega}\left(\sin[(t+1/2)\,\omega] - \sin[(t-1/2)\,\omega]\right)d\omega$$

$$= \frac{1}{\pi}\left(\int_{0}^{2\pi(t+1/2)} \sin(y)\frac{dy}{y} - \int_{0}^{2\pi(t-1/2)} \sin(y)\frac{dy}{y}\right)$$

$$= \frac{1}{\pi}\{Si[2\pi(t+1/2)] - Si[2\pi(t-1/2)]\} \quad \text{where } Si(x) = \int_{0}^{x} \sin(t)\frac{dt}{t}.$$

Although the above implementation is shown in band-limited form, band-limiting is optional and is not required for the present invention.

Hence in the present invention, when it is desired for any reason by command or as determined by the radio, the radio will automatically switch from AM to FM to gain extra range for a particular signal. The radio or communication unit may also receive a signal, such as from a base station or other controlling unit including another radio, instructing it to transmit with a particular modulation. Similarly, the radio will automatically switch from FM to AM to gain better battery efficiency. This switching takes place in switch 209, which is controlled by a DSP in the preferred embodiment.

Although the preferred embodiment uses QPSK-c modulation, a common receiver can still be used for any modulation that distinguishes data by phase, i.e., where all the constellation points fall on a circle, such as QPSK, D-QPSK, and CORPSK (Correlated PSK).

Although a DSP is used to perform many of the functions of the present invention, discrete elements or other programmable logic may also be used and will achieve the same effect.

What is claimed is:

Claims

1. A communication system characterized by:

a transmitter that modulates and transmits communication signals modulated by a first modulation technique and communication signals modulated by a second modulation technique, wherein said first modulation technique and said second modulation technique are different; and

a receiver capable of receiving said communication signals modulated by said first modulation technique and said communication signals modulated by said second modulation technique and demodulating said communication signals.

2. The communication system of claim 1, further characterized in that said first modulation technique is amplitude modulation and said second modulation technique is frequency modulation.

3. The communication system of claim 1, further characterized in that said first modulation technique is differential quaternary phase shift keying and said second modulation technique is 4-level frequency shift keying.

4. The communication system of claim 1, further characterized in that said communication signals modulated by said first modulation technique are transmitted when low power consumption by said transmitter is desired.

5. The communication system of claim 1, further characterized in that said communication signals modulated by said second modulation technique are transmitted when greater signal coverage by said transmitter is desired.

6. A communication unit characterized by:

means for modulating communication signals by a first modulation technique, producing a first modulated signal;

means for modulating communication signals by a second modulation technique, producing a second modulated signal, wherein said first modulation technique and said second modulation technique are different;

means for selecting between said first modulated signal and said second modulated signal, producing a selected signal; and

a transmitter for transmitting said selected signal.

7. The communication unit of claim 6, further characterized in that said first modulation technique is amplitude modulation and said second modulation technique is frequency modulation.

8. The communication unit of claim 6, further characterized in that said first modulation technique is differential quaternary phase shift keying and said second modulation technique is 4-level frequency shift keying.

9. The communication unit of claim 6, further characterized in that said first modulated signal is selected when low power consumption by said transmitter is desired.

10. The communication unit of claim 6, further characterized in that said second modulated signal is selected when greater signal coverage by said transmitter is desired.

1/1

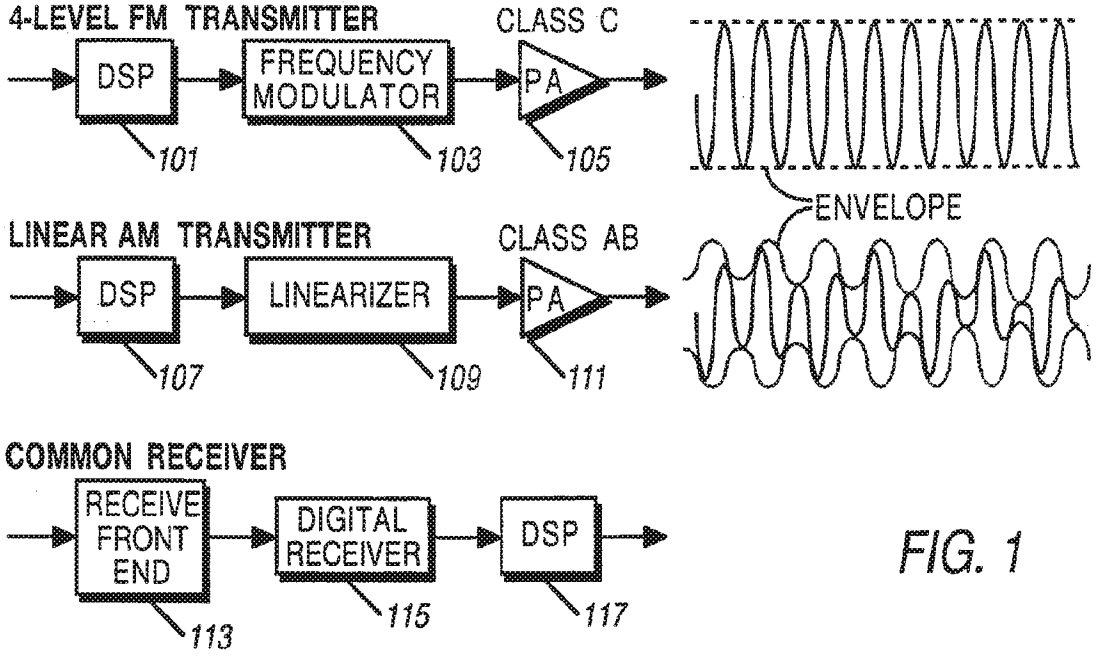
4-LEVEL FM TRANSMITTER
DSP
FREQUENCY MODULATOR
CLASS C
PA
101
103
105
ENVELOPE
LINEAR AM TRANSMITTER
DSP
LINEARIZER
CLASS AB
PA
107
109
111
COMMON RECEIVER
RECEIVE FRONT END
DIGITAL RECEIVER
DSP
113
115
117

FIG. 1

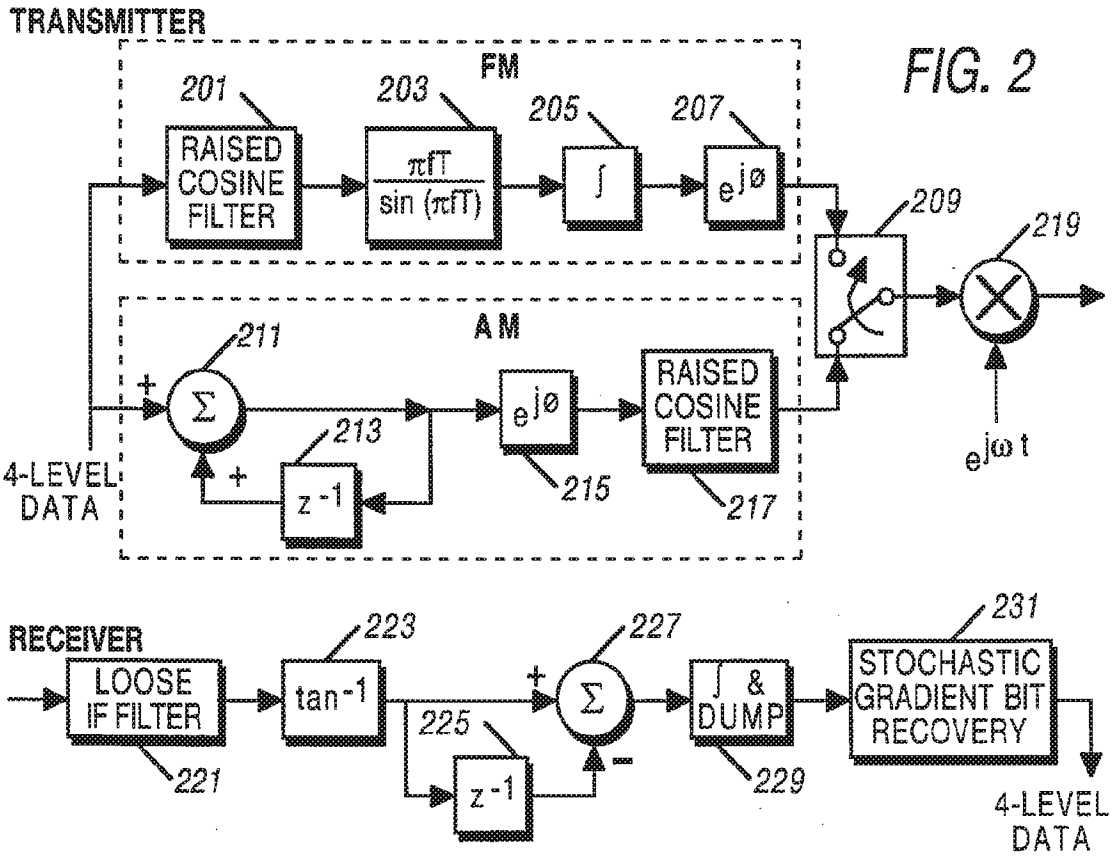
TRANSMITTER
FM
201
RAISED COSINE FILTER
203
πfT / sin (πfT)
205
∫
207
e^jø
209
219
AM
211
Σ
213
z -1
e^jø
215
RAISED COSINE FILTER
217
4-LEVEL DATA
e^jω t
RECEIVER
LOOSE IF FILTER
221
tan -1
223
225
z -1
227
Σ
∫ & DUMP
229
231
STOCHASTIC GRADIENT BIT RECOVERY
4-LEVEL DATA

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/00580

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H04L 27/10, 14, 16, 22; H04B 1/00, 02, 66, 16; 7/00
US CL :332/120, 151; 375/46, 59, 80; 455/61, 93, 102, 142, 343
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 332/108, 119, 120, 150, 151; 375/45, 46, 54, 59, 79, 80; 455/59, 61, 93, 101, 102, 108, 142, 205, 343

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US, A, 5,155,455 (COWLEY ET AL) 13 October 1992, Figure 2.	6-8, 10 --- 1-5, 9
X	US, A, 5,109,542 (ECKLUND) 28 April 1992, Abstract and Figure 1.	1-5
Y	Digital Analog Communication System, 1979 by John Wiley and Sons Inc., K. S. Shanmugam, "Power Requirements", pages 414, 416.	4, 9
A	US, A, 5,163,159 (RICH ET AL) 10 November 1992.	1-10
A	US, A, 4,660,192 (POMATTO SR.) 21 April 1987	1-10
A	US, A, 3,378,773 (JEFFERS) 16 April 1968.	1-10

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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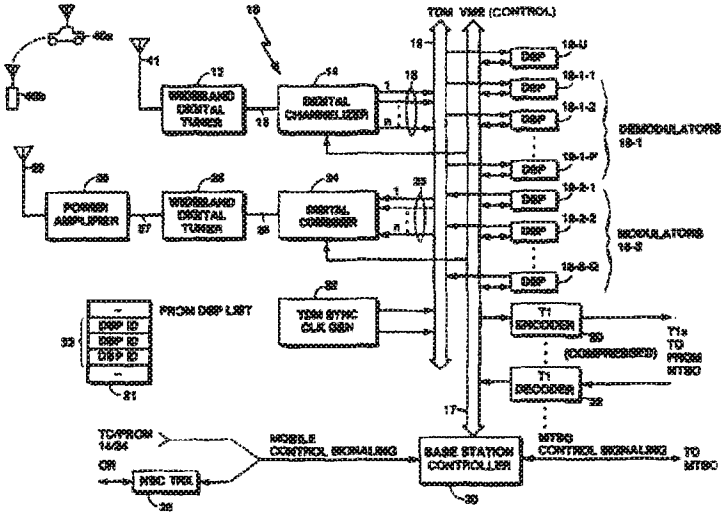

(57) Abstract

A wireless communication system basestation making use of a wideband, multichannel digital transceiver having incorporated therein a time division multiple-access (TDM) bus for providing digital samples of a plurality of wireless communication channels, wherein the time slot duration and frame rate of the TDM bus may be reconfigured. The invention allows various air interface standards, even those having different channel bandwidths, to be serviced by the same basestation, without having to install additional or different equipment, and by automatically redistributing signal processing resources, eliminating the need to reconfigure the basestation when different types of wireless signalling must be accomodated.

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WIDEBAND WIRELESS BASESTATION MAKING USE OF TIME DIVISION MULTIPLE-ACCESS BUS HAVING SELECTABLE NUMBER OF TIME SLOTS AND FRAME SYNCHRONIZATION TO SUPPORT DIFFERENT MODULATION STANDARDS

FIELD OF THE INVENTION

This invention relates generally to communication networks, and in particular to a wireless communication system basestation making use of a wideband, multichannel digital transceiver having incorporated therein a time division multiple-access (TDM) bus for providing digital samples of a plurality of wireless communication channels, wherein the TDM bus has a selectable number of time slots per frame, and a selectable frame synchronization rate, to permit dynamic allocation of modulator and demodulator signal processing resources, and to support wireless modulation standards of different bandwidths.

BACKGROUND

The basestations used by the providers of current day multiple channel wireless communication services, such as cellular mobile telephone (CMT) and personal communication systems (PCS), typically designate signal processing equipment for each single receiver channel. This is probably a result of the fact that each basestation is configured to provide communication capability for only a limited predetermined number of channels in the overall frequency spectrum that is available to the service provider.

A typical basestation may thus contain several racks of equipment which house multiple sets of receiver and transmitter signal processing components that service a prescribed subset of the available channels. For example, in an Advanced Mobile Phone Service (AMPS) cellular system, a typical basestation may service a pre-selected number of channels, such as 48, of the total number, such as 416, of the channels available to the service provider.

Certain types of wireless service providers would prefer, however, to employ equipment that would be more flexible, both in terms of where it can be located, as well as in the extent of the available bandwidth coverage provided by a particular transceiver site. This is particularly true in rural areas where cellular coverage may be concentrated along a highway, and for which the limited capacity of a conventional 48 channel

transceiver may be inadequate. This may also be true in other instances, where relatively large, secure, and protective structures for multiple racks of equipment are not necessarily available or cost effective, such as for PCS applications.

One way to resolve this difficulty is to implement a basestation transceiver using a high speed analog-to-digital (A/D) converter and equipment which makes use of efficient digital filtering algorithms such as the Fast Fourier Transform (FFT), to separate the incoming signal energy into multiple ones of the desired channels. On the transmit side, this basestation implementation includes an inverse FFT processing combiner which outputs a combined signal representative of the contents of the communication channel signals processed thereby. In this manner, relatively compact, lightweight, inexpensive, and reliable digital integrated circuits may be used to cover the entire channel capacity offered by the service provider, rather than only the subset of the available channels.

Thus unlike prior art basestations, the wideband digital basestation is capable of receiving any channel. While this provides a certain number of advantages as described above, it also poses a number of unique problems to the service provider.

Perhaps most importantly, there exists a need to efficiently support a varying number of active channels and the required connections into the public switched telephone network.

These connections should be made in such a way as to simplify call control. Indeed, it would be desirable for as many of the call set up control functions required by such a basestation were handled to the maximum extent possible by the basestation itself.

By so simplifying the network interface, the Mobile Telephone Switching Office (MTSO) and/or Mobile Switching Center (MSC) through which the basestation is connected to the Public Switched Telephone Network (PSTN) may be freed, as much as possible, from the details of maintaining a proper connection from the PSTN to the remote subscriber unit.

Secondly, the basestation should make efficient use of the available resources to process each call. In particular, while the wideband channelizer separates the signals into channels, certain other signal processing resources such as demodulators and modulators are also required.

Using the wideband front end, any channel in the bandwidth available to the service provider is available at any time. However, it is desirable for such a basestation

to only activate as many of the other, per-channel resources as is required to support the present call density.

By making the basestation's implementation of call processing resources as modular as possible, the basestation could initially be configured to support a limited number of channels. Then, as the demand for services grows, additional channels could be supported by the addition of the necessary resources.

In other instances, the basestation should be reconfigurable in the event of an change or expansion in one type of service. For example, given the emergence of several air interface standards such as code division multiple access (CDMA) as well as time division multiple access (TDMA) standards for cellular, it is desirable for a given wideband basestation to be able to support each such standard, thereby reducing the number of such basestations that need to be deployed. However, it would be desirable if the resources allocated to one particular air interface, when no longer needed, could then be made available to process signals formatted using the other air interface. That is, as the demands of one type of service or the other come and go, the basestation should be automatically reconfigured, without requiring an investment in new or different basestation resources.

Thus, several difficulties exist with a wideband digital basestation that can process at any time, any one of many channels in the RF bandwidth available to a service provider.

SUMMARY OF THE INVENTION

Briefly, the invention is a wideband transceiver basestation for a wireless communication system. The receiver portion of the basestation includes a digital channelizer which provides digital samples of multiple wireless channel signals, and a time division multiplexed (TDM) data bus, to provide switching functionality between the various channel outputs and other basestation receiver resources such as digital demodulators.

On the transmitter side, basestation signal processing resources such as digital modulators are also connected to a multichannel digital combiner over the TDM bus. Thus, the same flexibility in switching functionality is provided between transmitter signal processing resources and the transmitter channel inputs.

A synchronization and clock generation circuit has the capability of selecting the number of time slots, as well as the bus frame rate, to be used on the TDM bus. The number of time slots and the bus frame rate depend upon, respectively, the number of the channel signals and the bandwidth of each of the channel signals provided by the channelizer.

More particularly, the wideband basestation transceiver includes a receive antenna and one or more digital tuners that provide wideband digital signal energy to a digital channelizer. The digital channelizer, in turn, produces a plurality of channel signals, with each channel signal representing the signal energy in one of the radio frequency channels. The channel signals each consist of a series of digital samples.

The digital samples of each channel signal are, in turn, connected to a time division multiplex (TDM) bus. A basestation controller grants access to the TDM bus by each channel signal in a predetermined timeslot, in a predetermined order.

The samples of the digital channel signals are then forwarded to an available one of the associated receiver resources, such as a demodulator. The demodulators, typically implemented in a digital signal processor (DSP), are then connected to an outgoing landline such as a T1 line to a telephone switching office (MTSO) or mobile switching center (MSC) for further connection into the PSTN.

Accordingly, when the basestation is to support a particular number of channel signals simultaneously, each channel signal having a bandwidth as dictated by a particular modulation or air interface standard to be supported, the TDM bus reconfigured accordingly, to provide the required number of bus time slots, as well as the frame repeat rate required to support the desired per-channel sampling rate.

When it is desired that the basestation support a protocol which has a larger number of narrower bandwidth channels, the bus timing circuits are reconfigured to provide a correpondingly larger number of time slots at a slower frame rate, and, likewise, when the basestation is to support a protocol which has a smaller number of wider bandwidth channels, the bus timing circuits are again reconfigured to provide a smaller numnber of time slots at a higher frame rate.

As a result of the switching functionality provided by the TDM bus, the basestation is thus capable of supporting different signalling protocols, or air interface standards, which have different channel bandwidths.

The invention provides other advantages as well.

For example, the basestation may efficiently service both code division multiple access (CDMA) and time division multiple access (TDMA) signals at the same time. In such an arrangement, there are at least two digital channelizers, with one allocated to separating the incoming RF energy into the channel bandwidths required by TDMA, and another channelizer dedicated to separating the energy into the bandwidth required by CDMA. As the channels are activated, they are then serviced by the pool of demodulator resources, by allocating the correct number of additional time slots to accommodate each standard.

If, for example, a wideband CDMA mobile unit goes off line, the timeslots as modulators and demodulators freed thereby can be allocated to processing TDMA signals. This results in automatic on-demand redistribution of basestation resources to one signaling standard or another, without intervention by an MTSO, MSC, or the service provider in any way.

Such a system architecture also exhibits scalability, in the sense that additional DSP processors may be added to support additional channels as traffic increases, without having to change the RF front configuration. This is unlike the prior art, where each basestation had a fixed channel allocation, and, to add capacity, one must add additional narrowband receivers and transmitters.

As a result, a basestation according to the invention permits a wireless service provider much greater flexibility in planning implementations, as different and even future protocols can be supported.

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the advantages provided by the invention, reference should be had to the following detailed description together with the accompanying drawings, in which:

Fig. 1 is a block diagram of wideband digital basestation making use of a time division multiplex (TDM) bus according to the invention;

Fig. 2 is a more detailed block diagram showing addressable bus drivers and receivers which permits access to the TDM bus;

Fig. 3 is a detailed diagram of an addressable bus driver using a dual-port random access memory (DP-RAM);

Figs. 4A and 4B are timing diagrams showing the frame length and number of time slots on the TDM bus for two different channel bandwidths;

Fig. 5 is a detailed diagram of an addressable bus driver using a first-in, first-out (FIFO) memory;

Fig. 6 is a detailed diagram of an addressable bus receiver using a FIFO;

Fig. 7 is a detailed diagram of an addressable bus transmitter using a FIFO;

Fig. 8 is a sequence of operations performed by a basestation control processor in setting up a connection; and

Fig. 9 is an alternate embodiment of the invention making use of multiple tuners and channelizers to support multiple air interface standards while making maximum use of basestation resources.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Fig. 1 is a block diagram of a wideband wireless digital basestation 10 according to the invention. Briefly, the basestation 10 consists of a receive antenna 11, one or more wideband digital tuners 12, one or more digital channelizers 14, a time division multiplex (TDM) bus 16, a control bus 17, a plurality of digital signal processors (DSPs), a first subset of which are programmed to operate as demodulators 18-1-1, 18-1-2,...,18-1-P (collectively, demodulators 18-1); a second subset of which are programmed to operate as modulators 18-2-1, 18-2-2, ..., 18-2-Q; and a third subset 18-u of which are presently idle, transport signal (T-1) encoder 20, a T-1 decoder 22, one or more digital combiners 24, one or more wideband digital exciters 26, a power amplifier 28, a transmit antenna 29, a basestation control processor (controller) 30, and a TDM synchronization clock generator 32.

More particularly, the basestation exchanges radio frequency (RF) signals with a number of mobile subscriber terminals (mobiles) 40a, 40b. The RF carrier signals are modulated with voice and/or data (channel) signals which are to be coupled to the public switched telephone network (PSTN) by the basestation 10. The particular modulation in

used may be any one of a number of different wireless (air interface) standards such as the well known Advanced Mobile Phone Service (AMPS), time division multiple access (TDMA) such as IS-54B, code division multiple access (CDMA) such as IS-95, frequency hopping standards such as the European Groupe Speciale Mobile (GSM), personal communication network (PCN) standards, and the like. Indeed, in a manner that will be described below, the basestation 10 may even be configured to simultaneously process RF signals formatted according to more than one such air interface at the same time.

On the receive side (that is, with respect to the basestation 10), RF modulated signals are first received at the receive antenna 11, and forwarded to the wideband digital tuner 12. The digital tuner 12 downconverts the RF signal received at the antenna to a intermediate frequency (IF) and then performs an analog to digital (A/D) conversion to produce a digital composite signal 13.

Digital tuner 12 is wideband in the sense that it covers a substantial portion of the bandwidth available to the wireless service provider who is operating the basestation 10. For example, if the air interface implemented by the basestation 10 is IS-54B, the wideband digital tuner may downconvert as much as a 12.5 MegaHertz (MHz) bandwidth in the 800-900 MHz range which contains as many as 416 receive and transmit channel signals, each having an approximately 30 kiloHertz (kHz) bandwidth.

The digital channelizer 14 implements a channel bank to separate the downconverted composite digital signal 13 to a plurality, N, of digital channel signals 15.

This digital sampled signal is then further filtered to separate it into the individual 30 kHz channel signals. The digital channelizer 14 can thus be considered as a bank of digital filters with each filter having a 30 kHz bandwidth. The digital channelizer 14 may implement the filter bank using any of several different filter structures, and no particular digital filter structure is critical to the operation of the invention. However, in one preferred embodiment, the digital channelizer 14 consists of a set of convolutional digital filters and a Fast Fourier Transform (FFT) processor. The convolutional digital filters make use of multirate digital filter techniques, such as overlap and add, or polyphase, to efficiently implement a digital filter bank by grouping samples of the downconverted signal together, multiplying the sample groups by a convolutional function, and then forwarding the samples to the FFT for conversion into the n individual channel signals. Such filter banks may

implemented using any of the techniques as are described in the textbook by Crochiere, R.E., and Rabiner, L.R., entitled "Multirate Digital Signal Processing" (Englewood Cliffs, New Jersey: Prentice-Hall, 1983), pages 289-399.

In any event, the channelizer 14 provides N individual digital channel signals 15, wherein each of the N outputs represent information in one of the radio frequency channels originated by the mobile 40. Usually, one-half of the channels are used for transmitting signals and one-half for receiving signals. Thus, in the IS-54B example being described, N is 208, and thus there are 208 receive and 208 transmit channels implemented by the basestation 10.

These N digital channel signals are then provided over the time division multiplex (TDM) bus 16 to a plurality of digital signal processors (DSPs) 18-1-1, 18-1-2, ..., 18-1-P (collectively, demodulator-DSP 18-1). In a manner that will be understood in greater detail shortly, the TDM bus 16 operates as a time division multiplexed cross-bar switch. That is, any one of the N digital channel signals 15 may be connected to any one of the demodulator DSPs 18-1 via the TDM bus 16.

The exact nature of the timing of the TDM bus 16, that is, the number of time slots available for eaech frame of data samples output by the digital channelizer 14, and thus the manner in which the N digital channel signals are transferred over the TDM bus 16, changes depending upon the number of channel signals, N. The manner in which the basestation 10 accomodates these changes in the timing of the TDM bus 16 will be decribed in greater detail below.

The DSPs 18-1 are each programmed to remove the modulation on each channel signal 15 as specified by the air interface standard supported by the basestation 10. There typically is not a one-to-one correspondence between the number of DSPs 18-1 and the number of channel signals, N, provided by the channelizer 14. For example, the DSPs may each process a number, such as 24, of digital channel signals 15 at the same time.

The basestation controller 30, using the VME bus and TDM synchronization clock generator 32, manages access by individual digital channel signals 15 to the TDM bus 16, in a manner that will be described shortly.

The outputs of the digital signal processors 18-1, representing demodulated audio or data signals, are then forwarded over the VME bus 17 to the encoder 20. The VME

bus 17 is a well known industry standard relatively high frequency bus for interconnecting digital processors and components.

The encoder 20, in turn, reformats the demodulated signals as necessary for transmission to a local Mobile Telephone Switching Office (MTSO). The demodulated signals may be reformatted according to any one of a number of well-known time multiplex telephone signal transport protocols, such as the so-called T1 span (or E1). The T1 signals are then processed by the MTSO in an known fashion, to ultimately complete a telephone call from the subscriber unit 40 to a desired destination, such as another telephone subscriber who is connected to the Public Switched Telephone Network (PSTN).

Since each T1 span has a limited capacity, there may be more than one T1 signal necessary to accommodate all of the channels serviced by the basestation 10. In the example being discussed, each T1 signal may be formatted to carry up to 96 IS-54B bandwidth-compressed signals to the MTSO, assuming that the demodulated signals remain as compressed audio. Thus, as few as five T1 lines can be used to carry all of the 416 transmit and receive channels. When not all of the channels are busy, however, on as many of the T1 line resources as are necessary are connected to the MTSO, in a manner that will be understood shortly.

In other words, the demodulated signals output by the DSPs 18-1 may each be sub-rate (e.g., sub-DS0 frequency signals) which still contain additional encoding other than the air interface standard, such as impressed by a bandwidth compression scheme, which is not removed by the basestation 10. Rather, to minimize the required number of time slots used by the T1 signals, such compression may be removed at the MTSO.

The signal flow on the transmit side of the basestation 10 is analogous. Signals are received from the MTSO and provided to the T1 decoder 22, which removes the T1 formatting.

The unformatted T1 signals are then coupled to the DSPs 18 over the bus 17. A subset of the DSPs 18-2-1, 18-2-2, ..., 18-2-Q (collectively, modulators 18-2) then modulate these signals and presents them to the TDM bus 16. Ultimately, these are then each coupled to one of the N digital channel signals 23 input to the combiner 24. As was true in the receive direction, being a cross-bar swtich, the TDM bus 16 permits any one of the modulator DSPs 18-2 to be connected to any one of the channel signal inputs 23.

Although each modulator DSP 18-2 typically processes multiple channel signals, each such channel signal generated by the modulator DSP 18-2 is typically assigned one or more unique time slots on the TDM bus 16, with no two channel signals thus occupying the same time slot. Similarly, no two channel signals on the receive side ever occupy the same timeslot on the TDM bus 16.

As for the demodulators DSPs 18-1, the number of time slots assigned per frame on the TDM bus 16 varies, depending upon the channel bandwidth of the moduation standard implemented.

Other DSPs 18-u may be unused at a particular point in time. However, these unused DSPs remain as an available resource to the basestation 10, should a new mobile 40 request access. The manner in which DSPs are allocated at the time of setting up a call will be described in detail below.

The digital combiner 24 combines the TDM bus outputs to produce a composite IF digital signal 25 representing the N channels to be transmitted. The digital combiner 24 then feeds this combined signal to a digital exciter 26, which generates an RF signal 27. This RF signal 27 is then amplified by the power amplifier 28 and fed to the transmit antenna 29.

In order to set up each call, the basestation control processor 32 must exchange certain control information with the MTSO. For example, when a mobile unit 40 wishes to place a call, the mobile unit 40 indicates this by transmitting on one or more control signal channels. These control signals may be exchanged in one of several ways. As shown, the control signals may be in-band or out of band signals present in one or more of the channel signals output by the channelizer 14 or input to the combiner 24. Alternatively, a separate control signal transceiver 35 may be used to receive and transmit such control signaling.

In either event, the basestation 10 forwards the request for access by the mobile 40 to the MTSO, to set up the end to end connection. Upon receiving an indication from the MTSO that the connection can be made at the remote end, the basestation 10 then performs a number of steps, to insure that the appropriate data path through the TDM bus is then enabled to support communication with between the newly enabled mobile 40 and the MTSO.

For example, the MTSO typically returns a pair of T1 span line and T1 time slot identifiers. These inform the basestation controller 30 on which outgoing T1 line and time slot to place the received signal, and on which incoming T1 line and time slot it can expect to obtain the transmit signal for the mobile 40.

However, before proceeding with a detailed explanation of this call set-up process, a bit more detail of the operation of the TDM bus 16 will be provided. As shown in Fig. 2, the digital channelizer 14 consists of a convolutional digital filter 140, a fast Fourier transform (FFT) 142, as well as a TDM dual port (DP) driver 144.

The operation of the convolutional filter 140 and FFT 142 is not critical to the present invention, and is explained in the co-pending application. It is sufficient here to say that the convolutional filter 140 and FFT 142 make use of multirate digital signal processing techniques, such as overlap and add or polyphase, to efficiently implement a digital filter bank by (1) grouping samples of the downconverted signal 13 together and multiplying them by a weighting function, and then (2) forwarding them to the FFT 142 for conversion into the N individual channel signals.

An exemplary DSP demodulator 18-1-1 and modulator 18-2-1 are also shown in Fig. 2. The demodulator DSP 18-1-1 includes a TDM first-in first-out (FIFO) driver 180-1, a TDM FIFO receiver 182-1, a DSP central processing unit 184-1 and program memory 186-1. Similarly, the modulator DSP 18-2-1 includes a TDM FIFO driver 180-2, a TDM FIFO receiver 182-2, a DSP central processing unit 184-2 and program memory 186-2.

Indeed, the modulator and demodulator DSPs may share the same hardware architecture, with the only difference being the in the program which is enable in the program memory 186, which in turn may control whether the TDM receiver or TDM driver hardware is enabled.

Thus, in the DSP demodulator 18-1-1, only the TDM receiver 182-is enabled (as indicated by the dashed lines around the driver 180-1), since the demodulator 18-1-1 only receives data from the TDM bus 16. Likewise, only the TDM driver 180-2 is enabled in the DSP modulator 18-2-1, since it only transmits data on the TDM bus 16.

On the transmit side, the digital combiner 24 consists of a TDM dual port (DP) receiver 244, an inverse FFT 242, and deconvolutional digital filter 240. In a manner that is described below, the TDM DP receiver 244 reads each of the data samples off the

TDM bus 16 in their assigned time slot, and provides them to the inverse FFT 242 in the required order.

The samples are then operated on by the inverse FFT 242 and deconvolutional filter 240, to provide the composite digital signal 25 (Fig. 1).

Returning attention now to the channelizer 14, a detailed diagram of the TDM DP driver 144 is shown in Fig. 3. Briefly, it operates to assert the output samples from the FFT 142 in the proper time slots on the TDM bus 16. In order to simply the implementation of the TDM bus 16, these time slots are fixedly assigned to particular channels (such as in ascending order by frequency and time slot number). Thus, a sample of a given one, k, of the N channel signals, will always appear in a particular time slot, k, when it is active.

The DP driver 144 consists of a TDM slot counter 200, a first Dual Port Random Access Memory (DP-RAM) referred to as the enable DP-RAM 202, a second DP-RAM referred to as the data DP-RAM 204, and a driver 208 having an enable input EN.

As is conventional, each of the DP-RAMs have two separate address and data ports for reading and writing data, namely, input address and data ports AI and DI, and output address and data ports AO and DO.

In operation, the TDM slot counter 200 receives a pair of signals generated by the TDM synchronization circuit 32 (Fig. 1). The first signal, TDM CLK, is a digital clock signal identifying the clock periods, or time slots, on the TDM bus 16. The second signal is a TDM FRAME SYNC signal, indicating when a new frame starts on the TDM bus 16.

The TDM slot counter 200, which is a standard digital counter, receives the TDM FRAME SYNC signal at a reset input R, and the TDM CLK signal at a clock input (denoted by a chevron in the Figures). Thus, the TDM slot counter 200 continuously keeps track of which consecutively numbered slot on the TDM bus 16 is presently active.

According to the invention, the manner in which the signals are multiplexed onto the TDM bus 16 is changed, depending upon the bandwidth of channels in the modulation scheme being supported. In particular, the number of time slots per frame on the TDM bus 16 is adjusted, depending upon the bandwidth of the modulation of the air interface which is implemented.

Thus, for different air interface standards, the TDM slot counter 200 will receive different TDM CLK and different TDM FRAME SYNC signals. Turning attention

briefly to Figs. 4A and 4B, this concept will be better understood. As shown in Fig. 4A, for the IS-54B TDMA standard, the channelizer 14 provides 208 channels, each having a 30kHz bandwidth. The desired complex-valued (e.g., in-phase and quadrature) sampling rate of each TDMA channel is approximately 40kHz, so that the frame rate, that is, the rate at which each group of 208 samples is asserted on the TDM bus 16, is also set to 40kHz.

Accordingly, in order to support IS-54B channels, the TDM FRAME SYNC signal is controlled by the TDM synchronization clock generator 32 to reset the TDM slot counter 200 every 1/40 kHz, or every 25μs, and the TDM CLK signal is set to clock the complex-valued samples, one from each of the 208 channels, every 25 μs / 208; in other words, to provide approximately one TDM time slot every 121 ns.

As shown in Fig. 4B, for the IS-95 CDMA standard, the channelizer provides 10 channels, each having a 1.25 Mhz bandwidth. The desired complex-valued sampling rate of each channel is approximately 1.67 MHz, so that the frame rate is 600 ns.

Accordingly, in order to support IS-95 channels, the TDM FRAME SYNC signal is controlled to reset the TDM slot counter 200 every 600 ns, and the TDM CLK signal is set to clock the complex-valued samples, one from each of the 10 channels, every 600 ns / 10, or to provide approximately one TDM time slot every 60 ns.

As shown in Fig. 1, the TDM synchronization clock generator receives appropriate signals from the basestation controller 30 via the VMS bus 17 indicating the desired TDM CLK and desired TDM FRAME SYNC rate.

The manner in which data may be asserted on the TDM bus 16 in any of the time slots will now be described in detail. In particular, the enable RAM 202 generates an enable signal 203 indicating when the TDM DP driver 144 may assert data on the TDM bus 16. The AI and DI inputs to the enable DP-RAM 202 are typically written into by the basestation controller 30 during the process of setting up a new call. In particular, as shown in the table depicting the contents of the enable DP-RAM 202, a location in the RAM is associated with each time slot on the TDM bus 16 (e.g., if the TDM bus contained 512 time slots, then the RAM 202 has 512 locations).

A logical "0" in the associated enable DP-RAM 202 location indicates that the TDM driver is inactive in the time slot, that is, no data is to be asserted at that time. A

logical "1" in the associated location indicates that the time slot has been assigned to this particular TDM driver 144.

Thus, to enable a connection through the TDM bus 16, one step for the basestation controller 30, via the VME bus 17, is to write a logical "1" into the DP-RAM 202 location "x" associated with the newly enabled digital channel signal "x". In the example, shown, a "1" has been written at locations "27" and "30", indicating that this particular TDM driver 144 is now active in timeslot numbers 27 and 30.

The data DP-RAM 204 acts as a buffer, writing the digital channel signal samples output by the FFT at the DI input of the data DP-RAM 204. The DP-RAM 204 then stores the data samples until addressed by the TDM slot counter at the output side.

A data dual port (DP) RAM 204 is as a buffer in the case of processing the FFT output. This is because although the samples do come in bursts, or frames, the samples are not necessarily provided by the FFT 142 in the same order as they must be output onto the TDM bus 16. This is a particular phenomenon of at least one of the channelizer algorithms used. Thus, an address associated with each output sample from the FFT is used to determine at which location each sample is written in the data DP-RAM 204.

However, the input data is already in the correct order for the TDM FIFO driver 180-2 used by the DSP modulator. Such a TDM driver 180-2 can thus use a first-in first out memory (FIFO) 210 in the place of a data DP-RAM. As shown in Fig. 5, the configuration and operation of such as TDM FIFO driver 180-2 is somewhat similar to the DP driver 144.

In particular, the TDM slot counter 200, enable DP-RAM 202 and driver 208 operate in the same way as for the embodiment of Fig.3. The only difference is in the connection of the clock signals to the FIFO 210. On the input side, a clock signal is provided by the data source (e.g., the DSP processor 184-2) to cause data to be stored in the FIFO. The signal from the enable DP-RAM 202 is used to clock the FIFO output, DO.

A detailed diagram of the TDM FIFO receiver 182-1 is shown in Fig. 6. It includes a TDM slot counter 200, enable DP-RAM 202, bus receiver 212, and FIFO 214. The TDM slot counter 200 and enable DP-RAM 202 operate as for the TDM FIFO driver 180-1 shown in Fig. 5, to identify when the receiver 212 is to be active. The FIFO 214 is connected to the output of the receiver 212, having its input port connected to the enable

DP-RAM 202 output. The output side of the FIFO is clocked as needed by the destination for the data (such as the DSP processor 184-1 in Fig. 2).

The TDM DP receiver 244 is shown in detail in Fig. 7. As for each of the other driver/receivers, it includes a TDM slot counter 200, enable DP-RAM 202. It includes a data DP-RAM 220 operating similarly to the data DP-RAM in the TDM DP driver 144 (Fig. 3) and bus receiver 218.

With this background in mind, the details of how the basestation control processor 30 effects the switching operation of the TDM bus 16 can now be better understood.

Fig. 8 is a flowchart of these operations. This sequence of steps is initiated (step 300) when the basestation controller 30 receives control signals from the mobile 40 (Fig. 1) indicating that the mobile wishes to have access to the PSTN. The controller 30 then determines whether a free transmit and receive frequency (step 302) are available among the N channels.

An available modulator DSP and demodulator DSP resource are then identified (step 303) by examining a list 33 of free DSP resources maintained in a memory portion 31 of the basestation controller 30 (Fig. 1). The list 33 is updated by removing the two DSPs once allocated.

Access to an MTSO T1 channel (e.g., access to one or more T1 time slots as needed on a particular T1 span line) is then requested from the MTSO by issuing the appropriate MTSO control signaling (step 304). The MTSO then returns T1 span and time slot identifiers to be used for the transmit and receive channels for this connection.

In the next step (306), the appropriate destination and source information is written into the various TDM bus drivers and receivers.

In particular, given a receive channel identification, a receive channel signal time slot on the TDM bus is thus identified. The corresponding location of the enable DP-RAM 202 in the TDM DP driver 144 associated with this time slot is then set to a logical "1" in the manner already described.

Next, a logical "1" is also written into the enable DP-RAM in the TDM receiver 182-1 associated with the DSP demodulator 18-1 which was identified as being an available resource. If the per-channel bandwidth is greater than that which can be supported by a single timeslot, then a sufficient number of logical "1"s are written into the appropriate locations.

Also, now given a transmit channel identification, the free DSP modulator 18-2 is enabled (step 306) to use the TDM bus 16, by writing a logical "1" into the enable DP-RAM of the TDM driver 180-2 connected to the available one of the DSP modulators 18-2. To complete the connection, a logical "1" is also written into the location of the TDM DP receiver 244 associated with the identified transmit channel.

Finally (step 308), the basestation controller 30 issues control signals to the mobile 40 and MTSO to indicate that the connection has been set up.

The invention can also be used to advantage in implementing a basestation 10 which simultaneously services mobiles 40 which use different air interface standards. That is, the basestation 10 may at the same time process signals from a first mobile 40a which uses TDMA (IS-54B) signaling, as well as a second mobile 40b which uses CDMA signaling (IS-95).

As shown in Fig. 9, to support this implementation, the basestation 10 includes a pair of wideband digital tuners 12-1, 12-2. The first digital tuner 12-1 downconverts a bandwidth, such as 5 MHz, from an RF bandwidth which is occupied by TDMA signals. A second digital tuner section 12-2 downconverters a bandwidth, such as 7.5 MHz, which is occupied by CDMA signals.

Next, the tuners 12-1, 12-2 forward the downconverted signals to respective channelizers 14-1, 14-2. The TDMA channelizer 14-1 is configured to separate the received signal into the 30 kHz bandwidth channels specified by IS-54B. Likewise, the CDMA IS-95 channelizer 14-2 is configured to provide 1.25 MHz channels as specified by that standard.

The TDM synchronization clock generator 32 is appropriately set to provide a sufficient number of time slots on the TDM bus 16 to permit transmission of both the required number of samples from the TDMA channelizer 14-1 as well as the required number of samples from the CDMA channelizer 14-2.

The modulators and demodulators are then grouped according to the air interface modulation they must deal with. For example, at any given instant in time, a certain number of DSPs 18-1-T will have been allocated to operate as demodulators for the TDMA channels provided by the TDMA channelizer 14-1. A different set of DSP processors 18-1-C will be serving as demodulators for the CDMA channels provided by the CDMA channelizer 14-2. The active modulator DSPs will likewise be so allocated.

Thus, assuming that each of the DSPs 18 can be configured to execute either a TDMA modulation/demodulation program or a CDMA modulation/demodulation program by simply accessing the correct program memory, the available DSP resources and TDM bus time slots are only allocated as needed.

In other words, the DSPs (and associated T1 connections, for that matter) are allocated according to user demand automatically, and without intervention by the service provider. Thus, for example, as more customers migrate to using CDMA, additional CDMA channels are automatically made available and processed by the DSPs, at the expense of the unused TDMA channels.

A number of advantages can now be see for a basestation 10 configured according to the invention.

When the basestation is to receive and transmit channel signals having a bandwidth as dictated by a particular modulation or air interface standard to, the TDM bus is reconfigured accordingly, to provide the required number of bus time slots, as well as to provide a frame repeat rate approraite to support the required per-channel sampling rate.

When, at a different time, the basestation is to support a protocol having a larger number of narrower bandwidth channels, the bus timing circuits are reconfigured to provide a correpondingly larger number of time slots at a slower frame rate. Likewise, when the basestation is to support a protocol which has a smaller number of wider bandwidth channels, the bus timing circuits are again reconfigured to provide a smaller numnber of time slots at the higher required frame rate.

By disposing the TDM bus 16 between the output of the wideband digital channelizer 14 and the demodulator DSPs 18-1, the demodulator DSPs 18-1 may be allocated only as needed. Similarly, the modulator DSPs 18-2 are allocable as needed, since the TDM bus 16 is disposed between them and the digital combiner 24 as well.

Thus, if the basestation 10 is expected to service only a small number of channels, a correspondingly small number of modulator and demodulator DSPs can be installed in the basestation 10. As the basestation's demands increases, these additional RF channels can be serviced by simply adding more DSPs, and without having to reconfigure the RF front end.

Another advantage is provided in that this switching functionality is distributed at the basestation level as much as possible. In particular, unlike certain prior cellular signal switching techniques, the MTSO need not be concerned with the details of how the mobile units 40 are connected through the basestation. Indeed, the MTSO need not even know or care about which transmit and receive frequencies have been assigned to a particular mobile. All the MTSO need provide is identification of a T1 transport line and time slot on which it expects to receive and provide signals from and to the mobile.

Furthermore, because the basestation may efficiently allocate its demodulator/modulator resources, a number of different air interface standards may be supported by the basestation at the same time, without the need to determine in advance an exact plan for allocating receiver/transmitter resources for each air interface type. Upon detecting a request by a new mobile for access, the basestation simply determines the type of air interface used by the mobile, and then signals the appropriately programmed DSPs, or even initiates the DSPs to run a different modulator/demodulator program, as required to support the additional mobile.

While we have shown and described several embodiments in accordance with the present invention, it is to be understood that the invention is not limited thereto, but is susceptible to numerous changes and modifications as known to a person skilled in the art, and we therefore do not wish to be limited to the details shown and described herein but intend to cover all such changes and modifications as are obvious to one of ordinary skill in the art.

What is claimed is:

CLAIMS

1. A basestation for processing signals in a multiple mobile subscriber unit wireless communication system comprising:

an antenna for receiving signals from a plurality of the mobile units as a composite radio frequency, RF, signal;

wideband digital tuner means, connected to the antenna, for downconverting a selected bandwidth of the RF signal to an intermediate frequency, IF, signal and for performing an analog to digital conversion on the IF signal, to provide a wideband digital tuner output signal;

digital channelization means, being connected to receive the wideband tuner output signal, and providing multiple digital channel signal outputs, each digital channel signal output having a predetermined channel bandwidth, and each digital channel signal corresponding to one of the signals received from one of the mobile units;

a plurality of digital signal processing means, for providing digitally processed channel signal outputs; and

time division multiplex switching means, disposed between the multiple digital channel signal outputs and the plurality of digital signal processing means, the switching means for interconnecting any one of the multiple digital channel signal outputs to any one of the plurality of digital signal processing means; and

time division multipex synchronization timing means, connected to control the time division multiplex means, to provide, at a frame rate which depends upon the predetermined bandwidth of the channel signals, a plurality of time slots, the numer of time slots depending upon the number of digital channel signals.

2. The basestation of claim 1 wherein the signals received from the mobile units contain modulation, and the digital signal processors include demodulators to remove the modulation.

3. The basestation of claim 1 additionally comprising:

signal-transport encoding means, connected to the output of the digital signal processing means, for encoding the digitally processed channel outputs for further transmission to a mobile telephone switching office, MTSO.

4. The basestation of claim 3 wherein the signal-transport encoding means is a T1 encoder.

5. The basestation of claim 1 additionally comprising:

second digital channelization means, being connected to receive the wideband tuner output signal, and providing a second set of multiple digital channel signal outputs, each one of the second set of the digital channel signal outputs having a predetermined channel bandwidth which is different from the predetermined channel bandwidth of said above mentioned first digital channel signals, and each one of the second set of digital channel signals corresponding to one of the signals received from one of the mobile units.

6. The basestation of claim 1 additionally comprising:

second wideband tuner means, connected to the antenna, for downconverting a second selected bandwidth of the RF signal to a second intermediate frequency, IF, signal, and for performing an analog to digital conversion on the second IF signal, to provide a second wideband digital tuner output signal; and

second digital channelization means, being connected to receive the second wideband tuner output signal, and providing a second set of multiple digital channel signal outputs, each one of the second set of the digital channel signal outputs having a predetermined channel bandwidth which is different from the predetermined channel bandwidth of said above mentioned first digital channel signals, and each one of the second set of digital channel signals corresponding to one of the signals received from one of the mobile units.

7. A basestation as in claim 6 wherein the first and second set of digital channel signals are modulated in accordance with first and second standards, respectively.

8. A basestation as in claim 7 wherein the digital signal processors include a first set of digital signal processor means for demodulating said first set of digital channel signals, and a second set of digital signal processors for demodulating said second set of digital channel signals.

9. A basestation as in claim 7 wherein said first and second standards are each different one of a time division multiplex, TDMA, code division multiplex, CDMA, Advanced Mobile Phone System, AMPS, Personal Communications System , PCS, or Groupe Especiale Mobile, GSM.

10. A basestation as in claim 1 additionally comprising:

basestation controller means, connected to the time division multiplex switching means and the digital signal processing means, for maintaining a list of unused digital signal processing means that are not presently interconnected through the time division multiplex switching means to one of the digital channel outputs, and for dynamically allocating digital signal processing means from the list of unused digital signal processing means to be interconnected to one of the digital channel outputs only when the digital channel output contains an active signal being transmitted by the mobile unit which has not yet been assigned to one of the digital signal processing means.

11. A basestation as in claim 1 wherein the time division multiplex switching means further comprises:

a time division multiplex, TDM, data bus including data lines;

basestation controller means, connected to the TDM bus, and to generate TDM bus synchronization signals and driver address signals, the TDM bus synchronization signals used to identify access timeslots on the TDM bus; and

TDM bus driver means, connected to the TDM bus, the basestation controller means, and at least one of the digital channel signals, for receiving the TDM bus synchronization signals and the driver address signals, for storing the driver address signals, and for asserting the digital channel signal on the TDM bus when the value of driver address signals corresponds to the value of the bus synchronization signals, thereby indicating that a timeslot associated with the digital channel signal is currently active.

12. A basestation as in claim 11 wherein the basestation controller means, connected to the TDM bus, additionally generates receiver address signals, and the time division multiplex switching means additionally includes:

TDM bus receiver means, connected to the TDM bus, the basestation controller means, and at least one of the digital signal processor means, for receiving the TDM bus synchronization signals and the receiver address signals, for storing the receiver address signals, and for reading a signal asserted on the TDM bus and providing such asserted signal to the digital signal processor means when the value of receiver address signals corresponds to the value of the bus synchronization signals, indicating that a timeslot associated with the digital signal processor is currently active.

13. A wideband basestation as in claim 6 wherein the first and second channelizers each comprise:

a convolutional digital filter, connected to receive the respective one of the digitized wideband signals; and

a fast Fourier transform, FFT, processor, connected to receive the output of the convolutional digital filter, and to provide the digital channel signals.

14. A basestation as in claim 1 additionally comprising:

a second plurality of digital signal processing means, connected to receive digital input signals from a communication signal source;

a wideband digital combiner, being connected to receive a second plurality of digital channel signals, and to provide a composite digital signal for transmission;

wherein the time division multiplex switching means is also disposed between the second plurality of digital signal processors and the wideband digital combiner, the switching means connecting any one of the second set of digital signal processors to any one of the digital channel signals input to the combiner;

a wideband digital exciter, connected to receive the composite digital signal and to provide a combined RF signal; and

a transmit antenna, connected to receive the combined RF signal and the radiate the combined RF signal.

15. A basestation as in claim 14 additionally comprising:

basestation controller means, connected to the time division multiplex switching means and the first and second plurality of digital signal processing means, for

maintaining a list of all unused digital signal processing means that are not presently interconnected through the time division multiplex switching means to one of the digital channel outputs, and for dynamically allocating digital signal processing means from the list of unused digital signal processing means to function as one of the first or second digital signal processing means only when the digital channel output contains an active signal being transmitted by the mobile unit which has not yet been assigned to one of the digital signal processing means, or when the digital inputs from the communications source are active.

16. A wideband basestation transceiver including:

a wideband digital tuner that provides a wideband digital signal at an output;

a digital channelizer, connected to the wideband tuner, to produce a plurality of sampled channel signals, with each channel signal representing signal energy in one of a plurality of radio frequency channels serviced by the basestation;

a time division multiple-access, TDM, data bus;

means for selectively connecting the digital samples of each channel signal, in turn, to the TDM bus;

basestation controller means, for controlling the means for selectively connecting the digital samples of each channel signal to the TDM bus, by so connecting each channel signal in a predetermined timeslot, in a predetermined order;

means, coupled to the TDM bus, for selecting the digital samples in a particular timeslot, and for generating a reconstructed channel signal thereby;

means for allocating a demodulator to be coupled to the reconstructed channel signal when the associated radio frequency channel is active, the demodulator providing a demodulated channel signal;

means for allocating a T1 line encoder to the demodulated channel signal, to format the demodulated channel signal for transmission over a T1 span line;

means for coupling the T1 line to a mobile telephone switching office, MTSO, or mobile switching center, MSC, for further connection into the public switched telephone network, PSTN; and

A synchronization and clock generation circuit has the capability of selecting the number of time slots, as well as the bus frame rate, to be used on the TDM bus. The number of time slots and the bus frame rate depend upon, respectively, the number of the channel signals and the bandwidth of each of the channel signals provided by the channelizer.

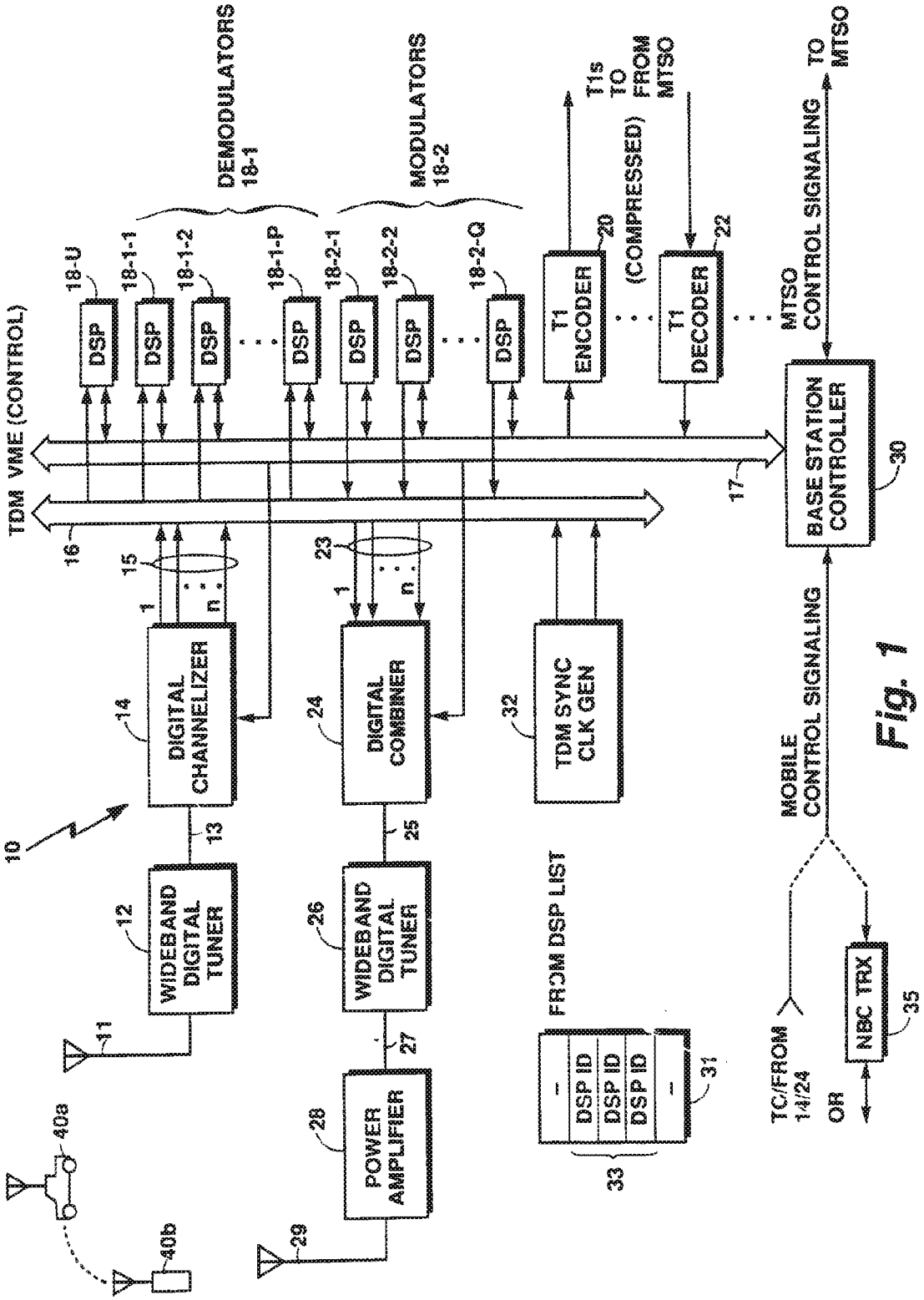

DEMODULATORS 18-1
MODULATORS 18-2
18-U
18-1-1
18-1-2
18-1-P
18-2-1
18-2-2
18-2-Q
DSP
T1 ENCODER
T1 DECODER
20
22
T1s TO FROM MTSO
(COMPRESSED)
TO MTSO
MTSO CONTROL SIGNALING
TDM VME (CONTROL)
16
17
BASE STATION CONTROLLER
30
15
23
1
n
DIGITAL CHANNELIZER
14
DIGITAL COMBINER
24
TDM SYNC CLK GEN
32
MOBILE CONTROL SIGNALING
10
13
25
WIDEBAND DIGITAL TUNER
12
26
11
27
FROM DSP LIST
DSP ID
31
33
TC/FROM 14/24
OR
NBC TRX
35
40a
40b
28
POWER AMPLIFIER
29

Fig. 1

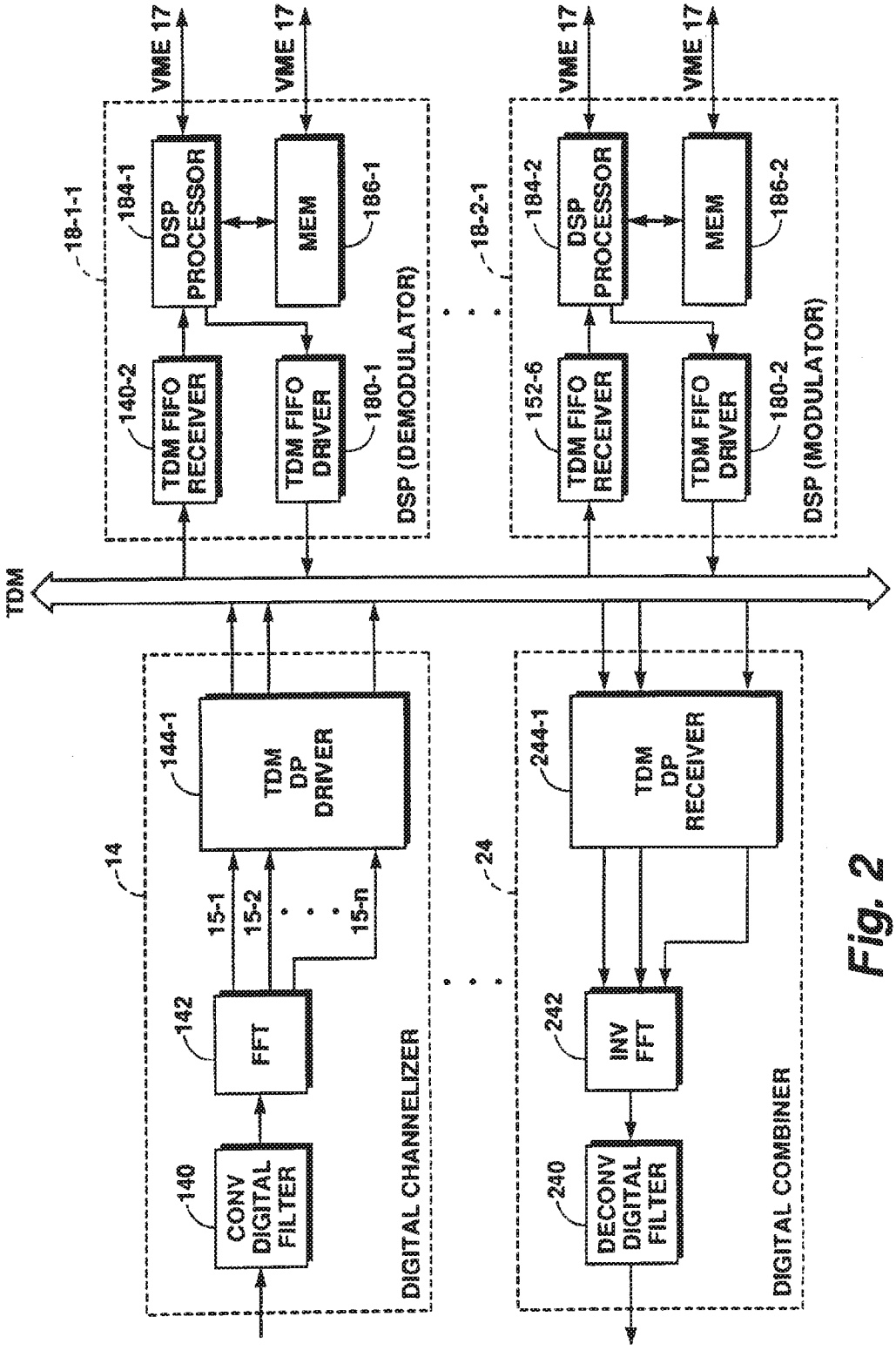
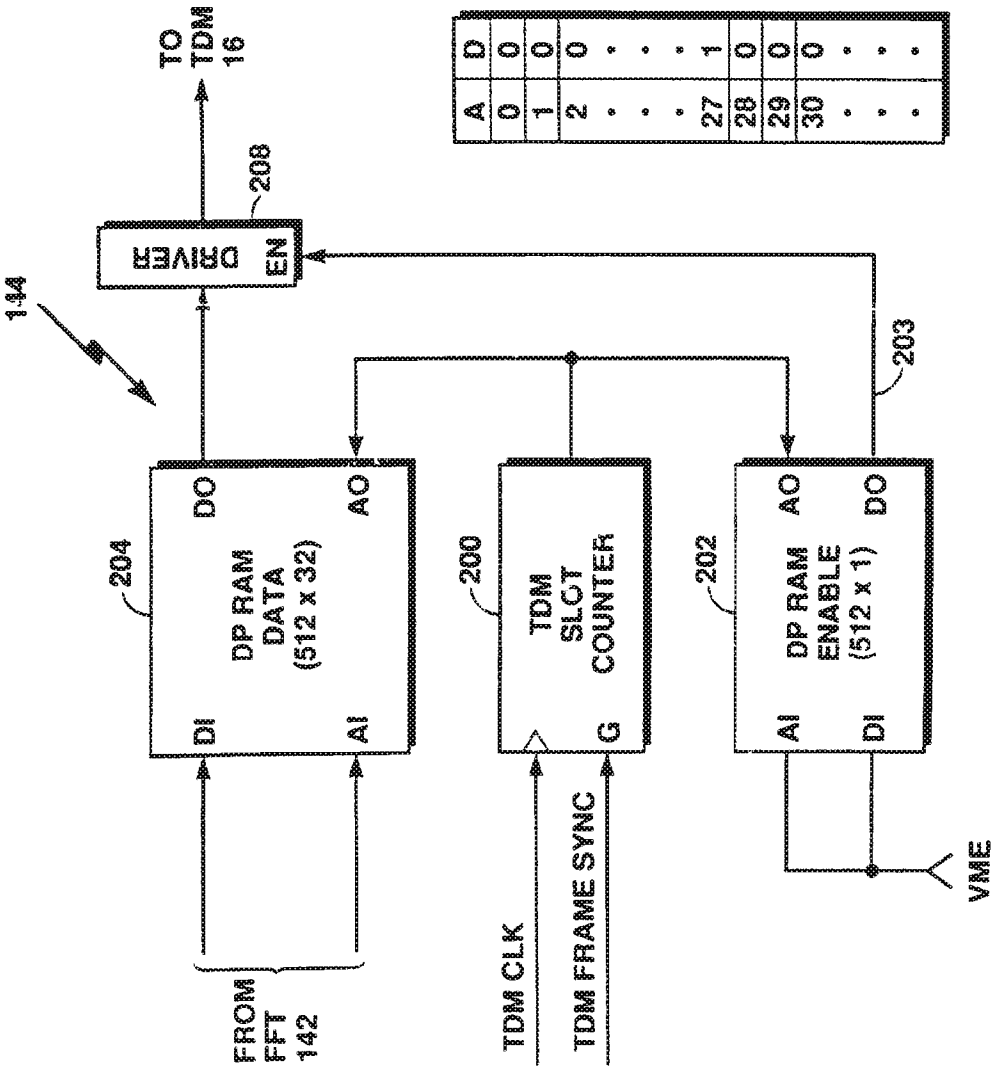

VME 17
VME 17
18-1-1
184-1
DSP PROCESSOR
MEM
186-1
140-2
TDM FIFO RECEIVER
TDM FIFO DRIVER
180-1
DSP (DEMODULATOR)
18-2-1
184-2
DSP PROCESSOR
MEM
186-2
152-6
TDM FIFO RECEIVER
TDM FIFO DRIVER
180-2
DSP (MODULATOR)
TDM
14
144-1
TDM DP DRIVER
15-1
15-2
15-n
142
FFT
140
CONV DIGITAL FILTER
DIGITAL CHANNELIZER
24
244-1
TDM DP RECEIVER
242
INV FFT
240
DECONV DIGITAL FILTER
DIGITAL COMBINER

Fig. 2

Fig. 3



RECTIFIED SHEET (RULE 91)
ISA/EP

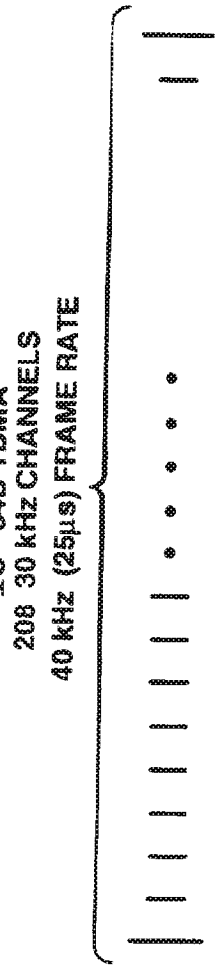

IS - 54B TDMA
208 30 kHz CHANNELS
40 kHz (25μs) FRAME RATE

Fig. 4A

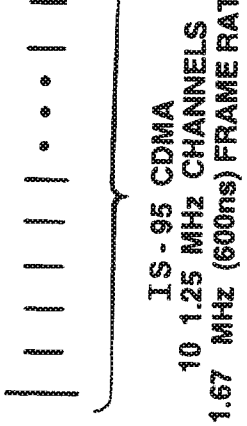

IS - 95 CDMA
10 1.25 MHz CHANNELS
1.67 MHz (600ns) FRAME RATE

Fig. 4B

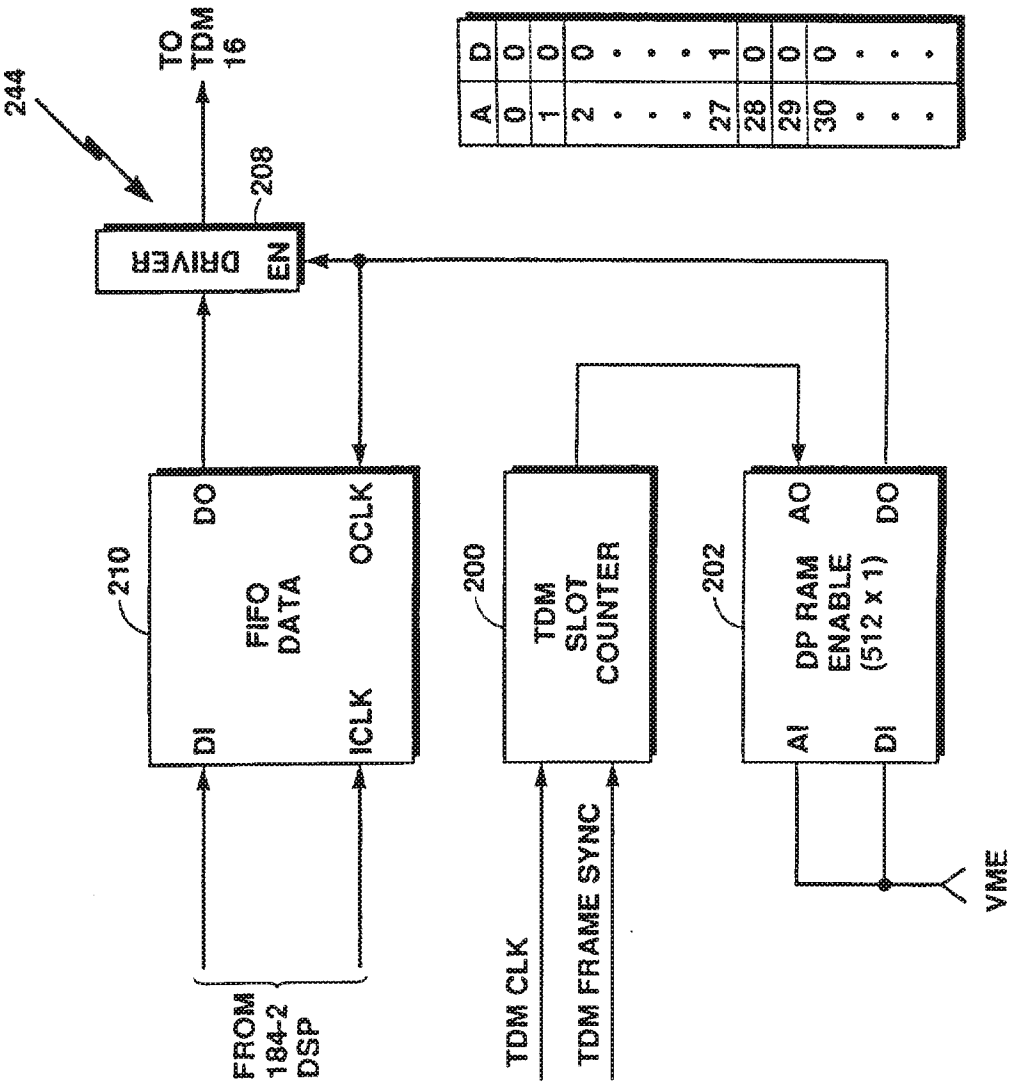
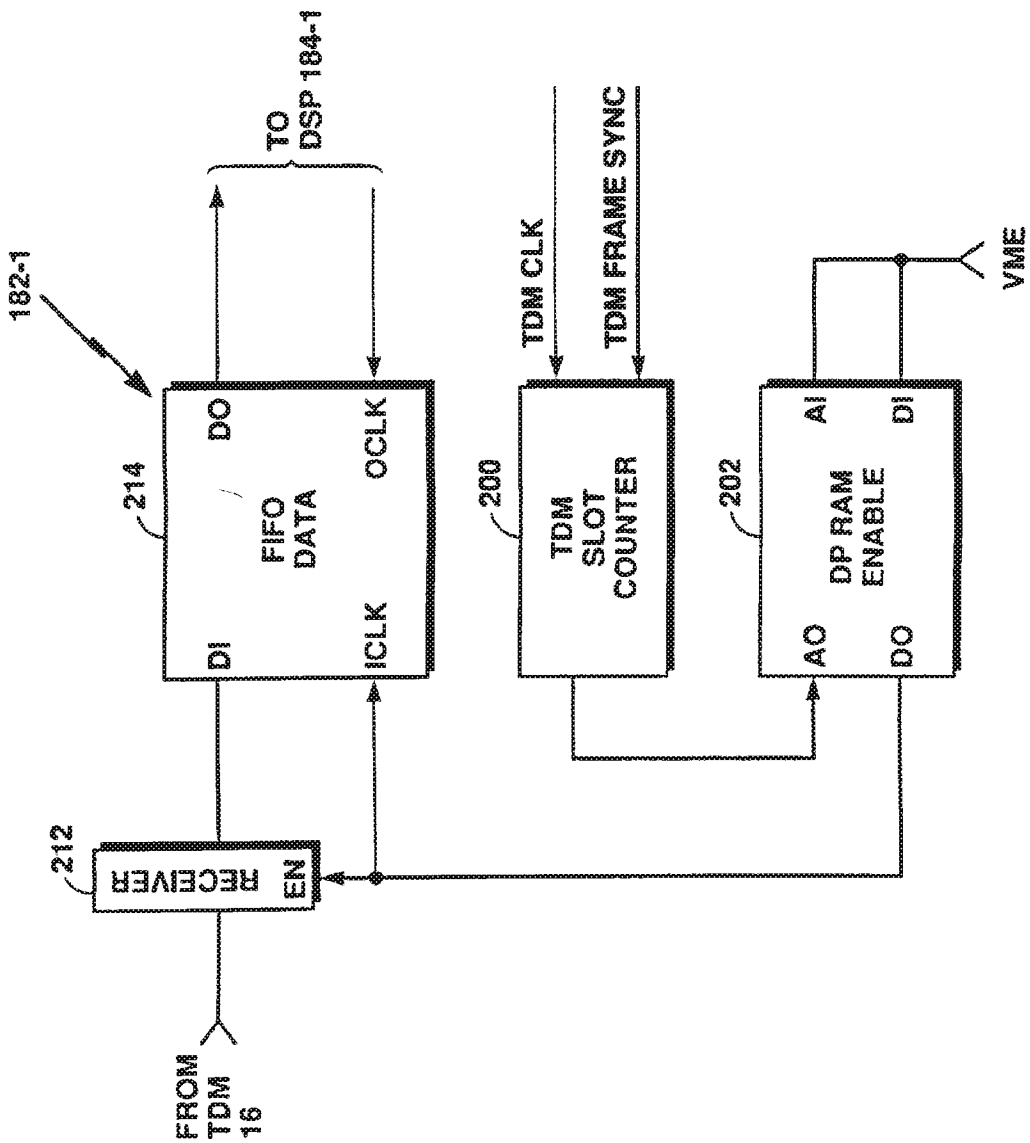

244
TO TDM 16
208
DRIVER
EN
210
FIFO DATA
DO
OCLK
DI
ICLK
200
TDM SLOT COUNTER
202
DP RAM ENABLE (512 x 1)
AO
DO
AI
DI
FROM 184-2 DSP
TDM CLK
TDM FRAME SYNC
VME
A D
0 0
1 0
2 0
27 1
28 0
29 0
30 0

Fig. 5

Fig. 6



SUBSTITUTE SHEET (RULE 26)

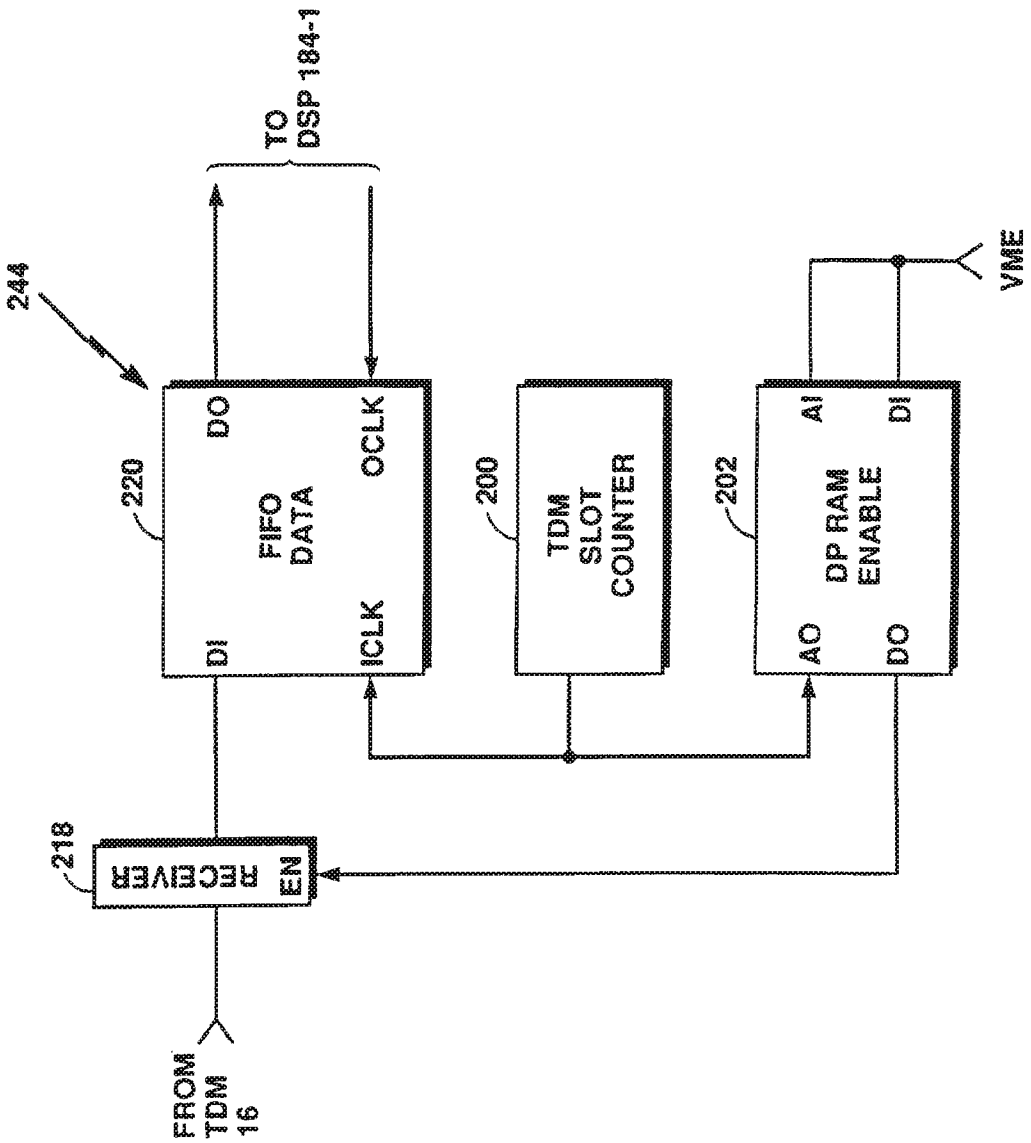


Fig. 7

IPR2020-00034 Page 01911
DEF0002105

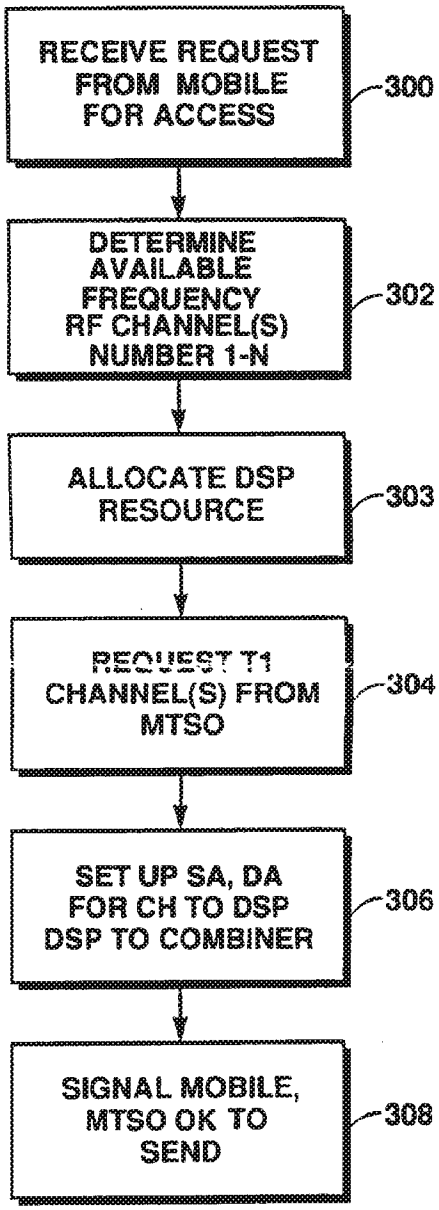


Fig. 8

RECTIFIED SHEET (RULE 91)
ISA/EP

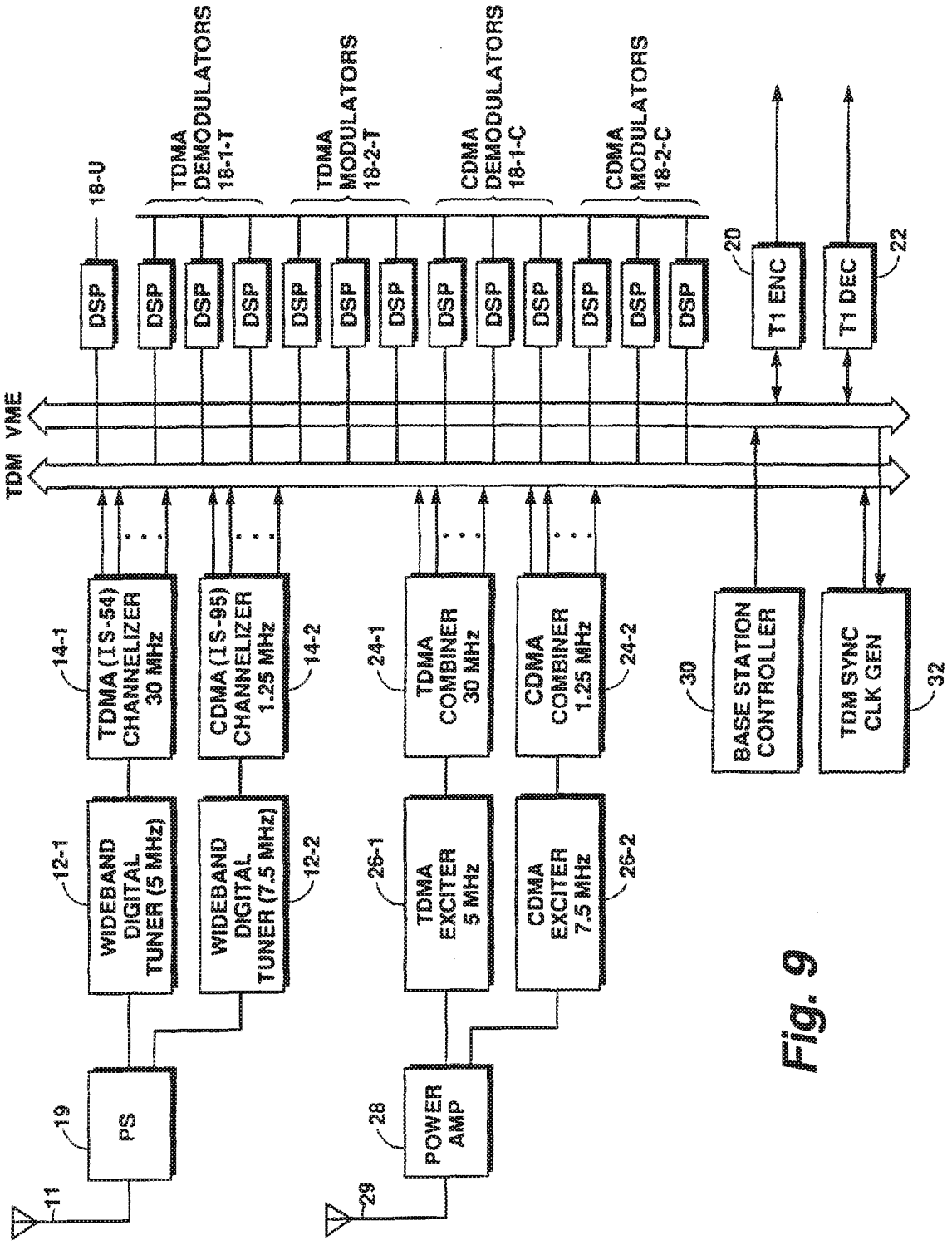

TDM VME
18-U
DSP
TDMA DEMODULATORS 18-1-T
TDMA MODULATORS 18-2-T
CDMA DEMODULATORS 18-1-C
CDMA MODULATORS 18-2-C
T1 ENC
20
T1 DEC
22
TDMA (IS-54) CHANNELIZER 30 MHz
14-1
CDMA (IS-95) CHANNELIZER 1.25 MHz
14-2
TDMA COMBINER 30 MHz
24-1
CDMA COMBINER 1.25 MHz
24-2
BASE STATION CONTROLLER
30
TDM SYNC CLK GEN
32
WIDEBAND DIGITAL TUNER (5 MHz)
12-1
WIDEBAND DIGITAL TUNER (7.5 MHz)
12-2
TDMA EXCITER 5 MHz
26-1
CDMA EXCITER 7.5 MHz
26-2
PS
19
POWER AMP
28
11
29

Fig. 9

INTERNATIONAL SEARCH REPORT

Interna...nal Application No
PCT/US 96/02200

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04Q7/30 H04B7/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04Q H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP,A,0 590 412 (SIEMENS) 6 April 1994 see claims 1-25; figures 1-4	1-16
X	EP,A,0 439 926 (ATT) 7 August 1991 see page 2, column 1, line 39 - column 2, line 43; figure 3	1-16
X	DE,A,44 23 582 (MOTOROLA) 12 January 1995 see claims 1-8; figures 1-4	1-16
X	EP,A,0 560 388 (NEC CORPORATION) 15 September 1993 see claims 1-5; figures 1-9	1-16
X	EP,A,0 605 182 (NIKI YOSHIRO) 6 July 1994 see claims 1-12	1,6-9,16

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

2

Date of the actual completion of the international search	Date of mailing of the international search report
24 May 1996	04.07.96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Bischof, J-L

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IPR2020-00034 Page 01914
DEF0002108

INTERNATIONAL SEARCH REPORT

Intern. ..al Application No
PCT/US 96/02200

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP,A,0 507 384 (PHILIPS ELECTRONICS UK LIMITED) 7 October 1992 see page 3, line 1 - page 5, line 25; figures 1-7	1-8, 10-12, 14-16
X	EP,A,0 471 246 (MOTOROLA) 19 February 1992 see page 3, column 3, line 8 - column 4, line 26; claims 1-10; figure 1	1-8, 10-12, 14-16

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

IPR2020-00034 Page 01915
DEF0002109

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 96/02200

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A-590412	06-04-94	DE-A-	4232480	31-03-94
		DE-A-	4238410	19-05-94
		FI-A-	934235	29-03-94
		NO-A-	933457	29-03-94
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		AU-B-	621011	27-02-92
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		DE-T-	69023114	18-04-96
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		JP-A-	5091079	09-04-93
		US-A-	5369637	29-11-94
EP-A-471246	19-02-92	US-A-	5111454	05-05-92

INTERNATIONAL SEARCH REPORT

information on patent family members

Inter .onal Application No
PCT/US 96/02200

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-471246		AU-B- 641521	23-09-93
		AU-B- 8034991	20-02-92

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IPR2020-00034 Page 01917

DEF0002111

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International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04L 1/12, 1/24, 5/14 — A3

(11) International Publication Number: WO 97/15131

(43) International Publication Date: 24 April 1997 (24.04.97)

(21) International Application Number: PCT/US96/16675

(22) International Filing Date: 18 October 1996 (18.10.96)

(30) Priority Data:
08/544,491 18 October 1995 (18.10.95) US

(71) Applicants: TELEFONAKTIEBOLAGET LM ERICSSON [SE/SE]; S-126 25 Stockholm (SE). ERICSSON INC. [US/US]; 7001 Development Drive, P.O. Box 13969, Research Triangle Park, NC 27709 (US).

(72) Inventor: RAITH, Alex, Krister; 805-A5 Park Ridge Road, Durham, NC 27713 (US).

(74) Agents: GRUDZIECKI, Ronald, L. et al.; Burns, Doane, Swecker & Mathis, L.L.P., P.O. Box 1404, Alexandria, VA 22313-1404 (US).

(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

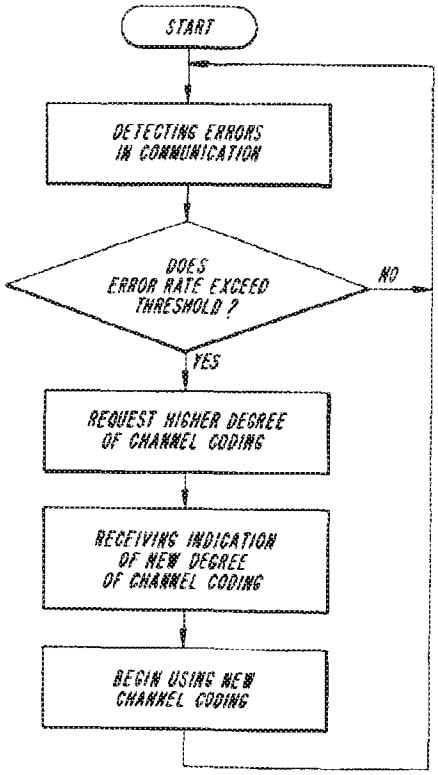
Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(88) Date of publication of the international search report:
5 June 1997 (05.06.97)

(54) Title: METHOD FOR IMPROVING THE EFFICIENCY OF TRANSMISSION IN MOBILE NETWORKS

(57) Abstract

A method for indicating a change in coding rate is disclosed so as to maintain synchronization between a communication system and a mobile station. A mobile station can request either to increase or decrease the degree of channel coding. The system can grant the request and send an indication to the mobile station indicating the new degree of coding. The indication is provided outside the field in which the coding rate is going to be changed. A modulation symbol alphabet can also be changed.



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FR	France	MN	Mongolia	UZ	Uzbekistan
GA	Gabon	MR	Mauritania	VN	Viet Nam

INTERNATIONAL SEARCH REPORT

Intern nal Application No
PCT/US 96/16675

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04L1/12 H04L1/24 H04L5/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 627 827 A (CSELT; PHILIPS) 7 December 1994 see abstract see page 2, line 4 - line 6 see page 2, line 48 - line 58 see page 3, line 47 - line 51 see page 3, line 56 - line 58 see page 4, line 4 - line 7 see page 4, line 24 - line 30	1-5
A	--- -/--	6-12

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

2

Date of the actual completion of the international search	Date of mailing of the international search report
15 April 1997	24.04.97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Scriven, P

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IPR2020-00034 Page 01920
DEF0002957

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 188 271 A (OKI ELECTRIC INDUSTRY) 23 July 1986 see abstract see page 1, line 16 - line 19 see page 2, line 21 - line 27 see page 3, line 1 - line 6 see page 3, line 12 - line 24 see page 9, line 7 - line 13 see page 13, line 24 - page 14, line 15 see page 19, line 21 - page 20, line 6	1-5
A	---	6-12
X	EP 0 423 485 A (BOSCH) 24 April 1991 see column 1, line 3 - line 11 see column 1, line 52 - line 53 see column 2, line 1 - line 5 see column 2, line 18 - line 42	1-5
A	---	6-12
X	EP 0 197 545 A (OKI ELECTRIC INDUSTRY) 15 October 1986 see abstract see column 1, line 1 - line 5 see column 1, line 49 - column 2, line 11 see column 2, line 18 - line 34	1-5
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X	GB 2 160 392 A (RACAL RESEARCH) 18 December 1985 see abstract see page 1, line 58 - line 72 see page 1, line 98 - line 106 see page 1, line 120 - line 125 see page 2, line 117 - line 124 see page 3, line 47 - line 56	1-5
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A	---	1-5
X	WO 90 06637 A (CODEX) 14 June 1990 see abstract see page 3, line 20 - line 26 see page 4, line 9 - line 21 see page 5, line 33 - page 6, line 1 see page 15, line 27 - line 33	6-12
A	---	1-5
	-/--	

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IPR2020-00034 Page 01921
DEF0002958

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 93 00751 A (MICROCOM SYSTEMS) 7 January 1993 see page 5, line 3 - line 7 see page 7, line 3 - line 7 see page 9, line 33 - page 10, line 1 see page 10, line 29 - page 11, line 2 see page 13, line 2 - line 6 see page 15, line 18 - line 36	6-12
A	---	1-5
X	IEICE TRANSACTIONS ON COMMUNICATIONS, vol. E77-B, no. 9, September 1994, TOKYO JP, pages 1096-1103, XP000474107 SAMPEI ET AL.: "Adaptive modulation/TDMA scheme for large capacity personal multi-media communication system" see abstract see figures 2,3 see page 1097, left-hand column, paragraph 3 see page 1097, right-hand column, paragraph 5	6-12
A	---	1-5
X	PROCEEDINGS OF THE VEHICULAR TECHNOLOGY CONFERENCE, 25 - 28 July 1995, NEW YORK, US, pages 306-310, XP000550184 UE ET AL.: "Symbol rate and modulation level controlled adaptive modulation/TDMA/TDD for personal communications systems" see abstract see page 306, left-hand column, paragraph 4 see page 306, right-hand column, paragraph 2	6-12
A	see page 309, left-hand column, paragraph 1 - paragraph 3	1-5

	-/--	

IPR2020-00034 Page 01922

DEF0002959

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PROCEEDINGS OF THE VEHICULAR TECHNOLOGY CONFERENCE, 25 - 28 July 1995, NEW YORK, US, pages 221-225, XP000550167 KAMIO ET AL.: "Performance of modulation-level-controlled adaptive-modulation under limited transmission delay time for land mobile communications" see abstract see page 221, right-hand column, paragraph 4 - page 222, left-hand column, paragraph 1 see figure 2	6-12
A	-----	1-5

2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 96/16675

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. Claims 1-5: Adjustment of the degree of channel coding.
2. Claims 6-12: Adjustment of the modulation symbol alphabet.

1. ☒ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searches without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

IPR2020-00034 Page 01924

DEF0002961

INTERNATIONAL SEARCH REPORT

ormation on patent family members

Interr nal Application No
PCT/US 96/16675

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		JP 7143572 A	02-06-95
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		EP 0587620 A	23-03-94
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INTERNATIONAL SEARCH REPORT

ormation on patent family members

Interr nal Application No
PCT/US 96/16675

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9300751 A		AU 2295292 A	25-01-93

Form PCT/ISA/210 (patent family annex) (July 1992)

IPR2020-00034 Page 01926
DEF0002963

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04L 1/12, H04Q 7/18 — A1

(11) International Publication Number: WO 97/24828

(43) International Publication Date: 10 July 1997 (10.07.97)

(21) International Application Number: PCT/JP96/03755

(22) International Filing Date: 24 December 1996 (24.12.96)

(30) Priority Data:
7/354309 29 December 1995 (29.12.95) JP

(71) Applicant: CASIO COMPUTER CO., LTD. [JP/JP]; 6-1, Nishi-Shinjuku 2-chome, Shinjuku-ku, Tokyo 160 (JP).

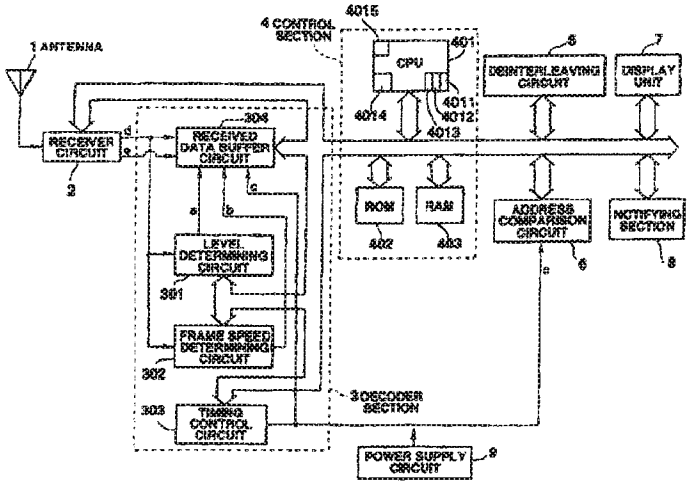
(72) Inventors: TACHIBANA, Toshiyuki; 278-102, Shimmachi, Ome-shi, Tokyo 198 (JP). SATO, Satoshi; 2-24-12, Nakamuraminami, Nerima-ku, Tokyo 176 (JP).

(74) Agents: SUZUYE, Takehiko et al.; Suzuye & Suzuye, 7-2, Kasumigaseki 3-chome, Chiyoda-ku, Tokyo 100 (JP).

(81) Designated States: AU, CA, CN, KR, MX, NO, PL, SG, Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (CH, DE, ES, FI, FR, GB, IT, NL, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: MULTI-RATE AND MULTIPLE-MODULATION FORMAT DATA RECEIVING APPARATUS AND METHOD OF DEINTERLEAVING DATA



(57) Abstract

When a frame information (F1)C2 defining the frame type in a transmission protocol format is received in a pager, data of a following interleaving portion is received. A receiving buffer circuit converts the received data from serial data into parallel data in accordance with the frame type, and a deinterleaving circuit reproduces (deinterleaves) the converted parallel data. The conversion means converts data received by one of a plurality of receiving means into parallel data corresponding to format data denoting data modulation mode and/or data transmission rate.

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D E S C R I P T I O N

MULTI-RATE AND MULTIPLE-MODULATION FORMAT DATA RECEIVING APPARATUS AND METHOD OF DEINTERLEAVING DATA

Technical Field

The present invention relates to a data receiving apparatus and a method of deinterleaving data for reproducing data transmitted by a modulation mode at a frame speed (or transmission rate) and by an interleaving mode arbitrarily selected from predetermined modulation modes, frame speeds and interleaving modes.

Background Art

Hitherto, NTT system and POCSAG system have been known as paging (wireless paging) systems.

The POCSAG system employs, for example, binary FSK (Frequency Shift Keying) method as a modulation mode and sets a frame speed to 512 bps (Bit/Second). When paging is performed, a paging service company transmits digital data, which has been FSK-modulated, to the called pager, at the rated frame speed. Thus, a service for communicating messages has been performed.

Meanwhile, the progress of the mobile communication technique made recently has resulted in the communication service charge being reduced. Thus, the mobile communication has been widely used in business, personal, and in particular, among the young, thus resulting in subscribers being increased. As a result,

addresses for the subscribers are in short and the traffic has been always congested. Thus, the conventional POCSAG system has encountered difficulty in providing service satisfactory for the subscribers.

Since the paging service has been in a great demand and the serviceable menus have been increased recently, there arise a necessity of improving the paging system. As a result, employment "RCR STD-43" in future has been decided as the next standard system.

The foregoing paging system (hereinafter called "STD-43") will briefly be described. The structure of data, which is employed in STD-43, is shown in FIG. 32. Referring to FIG. 32, symbol "A" shows the structure of data which is transmitted at a period of one hour and "B" shows one cycle of the data structure "A". Symbol "C" shows the structure of data in one frame of the cycle structure "B". Symbol "D" shows the block structure of one frame. The data structure "A" is composed of 15 cycles respectively given numbers "No. 0" to "No. 14".

The cycle structure "B" is composed of 128 frames respectively given numbers "No. 0" to "No. 127", which are transmitted at a period of four minutes. One frame has a data length of 1.875 seconds. Data in one frame of the frame structure cycle is sectioned into 8 section corresponding to the contents of data.

The eight section of the data contents is, as

indicated in the data structure "C" and the block structure "D", composed of sync structure D1 composed of, when viewed from the leading end, synchronization 1 (S1)C1, frame information (F1) C2 and synchronization 2 (S2)C3 and arranged to be transmitted at 115 ms (milliseconds); and interleaved block structure D2 composed of block information (B1) C4, address field (AF)C5, vector field (VF)C6, message field (MF)C7 and idle blocks (IB)C8 and arranged to be transmitted at a frame speed of 160 ms for each block so that 11 blocks are transmitted.

In the synchronizing signal section D, the synchronization 1 (S1)C1 is composed of 112-bit 2-level FM data (binary-FSK-modulated data, in detail) at 1600 bps, the synchronization 1 (S1)C1 containing frame pattern data including information of frame receiving timing, timing for receiving 1600 bps symbol data and the transmitted type selected from the following four frame types/rates with which the interleaving block portion D1 is interleaved/transmitted:

1. 2-Level FM 1600bps (Binary FSK Modulation/1600 bps)

2. 2-Level FM 3200bps (Binary FSK Modulation/3200 bps)

3. 4-Level FM 3200bps (Quadruple FSK Modulation/3200 bps)

4. 4-Level FM 6400bps (Quadruple FSK

Modulation/6400 bps)

The frame information (F1) C2 is composed of 32-bit 2-level FM data at 1600 bps and includes data (four bits) of cycle number of the cycle of the data structure "A" to which this frame belongs, data (7 bits) of the frame number of the cycle to which this frame belongs, and information of indication of plural transmitted operations and the number of the transmitted operations.

The interleaved block structure D2 formed of the synchronization 2 (S2)C3 and the block information (B1) C4 to the idle blocks (IB)C8 is data which is transmitted by means of the frame type specified by the synchronization 1 (S1)C1. The synchronization 2 (S2)C3 is a block for supplying timing information to the interleaved block structure D2 transmitted by the modulation method and the frame speed specified by the synchronization 1 (S1)C1 to enable the called pager to fetch the interleaved block structure D2.

The block information (BI)C4 is data disposed in block #0 of the interleaved block structure D2 and composed of one word. The block information (BI)C4 includes block information 1 for storing information of the word number (2 bits) which is used as the start point of address field (AF)C5 and the end point of the present field, to be described later, the word (6 bits) which is used as the start point of vector field (VF)C6 and the like, and block information items 2, 3 and 4 so

that ID of the simulcast system and, if the frame number is zero, information of the actual time, time zone and system message are stored.

The address field (AF)C5 is a field for storing address data of the called pager, the data to be stored being short address (32 bits) or long address (64 bits).

The vector filed (VF)C6 and the address field (AF)C5 form a pair and the vector field (VF)C6 is a field for storing the word at which the own message data is started in a message field (MF)C7 to be described later, the word length of own message data (hereinafter simply referred to message length) and information of the data format of the own message data.

The message field (MF)C7 is a field for storing message data corresponding to information specified by the vector field (VF)C6. The idle blocks (IB)C8 is an unused block to which a pattern composed of "1" or "0" is set.

The signal format shown in FIG. 32 is, in parallel, interleaved/transmitted in a time sequential manner in independent four phases "a", "b", "c" and "d". That is, if STD-43 is employed, the paging service company uses any one of the above-mentioned four phases or two to four phases to enable data in one frame having different contents to be multiplexed so as to be transmitted simultaneously.

In STD-43, the relationship between the phases of

the frame speeds is regulated as follows:

1600 bps: any one of phases "a", "b", "c" and "d" is used (multiplex degree: 1)

3200 bps: a pair of phases "a" and "c" or a pair of "b" and "d" is used (multiplex degree: 2)

6400 bps: all of the phases "a", "b", "c" and "d" are used (multiplex degree: 4)

The block structure of the interleaved block structure D2 will now be described. Referring to FIG. 32, one block is structured such that the frame speed is 160 ms. One block stores, in parallel, 8 rows (one row is called one word) for one phase, each row being composed of the following 32 bits:

Information (Information Bit): 21 bits

Parity(Check Bit): 10 bits

CK(Even-Number Parity Bit): 1 bit

The number of bits of data in one block is different depending upon the frame speed. The relationship between the frame speeds and the number of bits of data in one block is as follows:

1600 bps: 1 phase × 8 words × 32 bits = 256 bits

3200 bps: 2 phases × 8 words × 32 bits = 512 bits

6400 bps: 4 phases × 8 words × 32 bits = 1024 bits

The structure of bit data in one block at each frame speed will now be described with reference to FIG. 33 to 35. FIG. 33 shows the structure of bit data in one block at the frame speed of 1600 bps, FIG. 34

shows the structure of bit data in one block at the frame speed of 3200 bps and FIG. 35 shows the structure of bit data in one block at the frame speed of 6400 bps.

In the case where the interleaved block structure D2 is transmitted at 1600 bps, the structure of bit data in one block shown in FIG. 33 is employed. The transmitted order of bit data is, in a direction indicated by an arrow β shown in FIG. 33, as W(word)0a1, W1a1, W2a1, ..., W5a32, W6a32 and W7a32.

In the case where transmitted at 3200 bps is performed, the structure of bit data in one block as shown in FIG. 34 is employed. The transmitted order of bit data is, in a direction indicated by an arrow β shown in FIG. 34, as W0a1, W0c1, W1a1, ..., W6c32, W7a32 and W7c32 (in the case of 2-level FM), as W0a1 and W0c1, W1a1 and W1c1, W2a1 and W2c1, ...,W6a32 and W6c32, W7a32 and W7c32 (in the case of 4-level FM). In the case where transmitted at 6400 bps is performed, the structure of bit data in one block as shown in FIG. 35 is employed. The transmitted order of bit data is, in a direction indicated by an arrow β shown in FIG. 35, as W0a1 and W0b1, W0c1 and W0d1, W1a1 and W1b1, W1c1 and W1d1, ..., W6a32 and W6b32, W6c32 and W6d32, W7a32 and W7b32, W7c32 and W7d32 (in the case of 4-level FM).

As described above, STD-43 involves the number of bits of data in one block which is received at each frame speed and the interleaving mode being different.

Also in the case of the frame speed of 3200 bps, the structure of bit data becomes different depending upon whether the modulation mode is 2-level FM or 4-level FM.

When a paging service company employs paging system STD-43, one frame type is selected from four types of the frame types/rates in the synchronization 1 (S1)C1 of the sync structure D1. Thus, the number of bits of data in one frame which is transmitted to the called pager can arbitrarily be changed.

Therefore, if the called pager uniformly receives, amplifies and digitizes data, which has been transmitted in the wireless manner, to simply convert 2-level FM serial data into parallel data as has been performed by the conventional POCSAG system, meaningless serial data is unintentionally transmitted. Thus, a data reproducing method adaptable to STD-43 and capable of rearranging bit data to correspond to the received frame type must be provided for the pager.

The following methods of reproducing received data to be provided for the pager have been suggested:

(1) A method in which plural types of hardware units (decoders) adaptable to the respective frame speeds and the multiplex degree are mounted on the pager; any one of the mounted hardware unit is selected so that data transmitted at any one of the frame speeds is received; and bit data of the interleaved block structure D2 of above data is reproduced in accordance

with the multiplex degree and by the selected deinterleaving circuit.

(2) One type of hardware is mounted on a pager; and software for performing control to rearrange bit data in the interleaved block structure D2 in accordance with the frame type of the received data is installed so that received data is reproducing.

In the case where method (1) is employed, the pager is provided with a plurality of S/P conversion circuits for converting the serial data to the parallel data in accordance with the frame type of received data; and a rearranging circuit for rearranging the parallel data in order to separate data into each phase.

In the case where method (2) is employed, one S/P conversion circuit and the rearranging circuit are provided which are controlled by software. However, in the above-mentioned case (1), the number of hardware units which receive and reproduce data and which must be provided for the pager increases. What is even worse, since the structure of each of the circuits has a complicated structure, the size of the reception processing circuit after it has been mounted cannot be reduced. In the case of (2), the software must perform a heavier task and therefore the structure of the system becomes too complicated.

Disclosure of the Invention

Accordingly, the present invention is achieved to

solve expected problems to arise for a pager for receiving and reproducing data when STD-43 standard is employed and, thus, it is an object of the present invention to provide a data receiving apparatus and a method of reproducing received data which can keep the balance between hardware and software for use to receive and reproduce data and reduce the size of the hardware and the load which must be borne by the software.

Another object of the present invention is to provide a data receiving apparatus and a method of reproducing received data capable of adapting the above-mentioned data transmission method, keeping the balance of load distributed to hardware and software, and reducing the size of the circuit and load, which must be borne by a CPU.

In order to achieve the above-mentioned objects, according to the present invention, there is provided a data receiving apparatus comprising:

receiving means for receiving data;

plural reproducing means capable of reproducing received data having a format which can be recognized by said data receiving apparatus;

format data receiving means for receiving format data; and

selection means for selecting one of said plural reproducing means in accordance with the format data received by said format data receiving means.

Therefore, the load distributed to the hardware and the software can be balanced so that the size of the circuit and the load of the CPU are reduced.

The format data denotes a frame speed and the reproducing means is selected in accordance with the received frame speed. The reproducing process rate of the reproducing means is controlled in accordance with the frame speed received by the format data receiving means.

The format data denotes a modulation mode and the reproducing means is selected in accordance with the received modulation method. The received data is converted to parallel data in accordance with the modulation method.

The format data denotes a frame speed and a modulation mode and the reproducing means is selected in accordance with the received frame speed and the modulation method. The reproducing process rate of the reproducing means is controlled in accordance with the frame speed received by the format data receiving means. The received data is converted to parallel data in accordance with the modulation method.

The data reproducing process rate of the reproducing means is controlled in accordance with a data interleaving mode. Received data is converted into parallel data in accordance with the data interleaving mode.

Since the received data is converted into parallel data in accordance with the data interleaving mode, the load distributed to hardware and software can be balanced, and thus the size of the circuit and load, which must be borne by a CPU, can be reduced.

Plural registers used for converting the received data into parallel data are provided.

When parallel data is divided into predetermined units so as to be sequentially stored, stored parallel data are read sequentially in the storing order so as to be supplied to the selected reproducing means, and reproduced parallel data is stored in the storage position from which the same has been read, the operation required to transfer data in the data transmission process is performed by, for example, a DMA circuit in place of the CPU. Thus, the load of the CPU can furthermore be reduced.

When data which is reproduced in one operation by the reproducing means selected by the selection means is stored in data storage means, when reproducing timing of the reproducing means selected by the selection means is detected, parallel data is sequentially transmitted from the data storage means to the reproducing means and simultaneously parallel data transmitted from the conversion means is sequentially stored by the data storage means, the operation required to transmit and receive data in the data transmitted process is

performed by, for example, a DMA circuit in place of the CPU. Thus, the load of the CPU can furthermore be reduced.

The format data received by the format data receiving means is stored until the format data is received next.

An ID code of paging of the data receiving apparatus is stored, if the ID code is detected in reproduced data while continuing the reproducing operation of the reproducing means, the detected ID code and the stored ID code are compared with each other. If the ID codes do not coincide with each other, the reproducing operation of the reproducing means is interrupted.

By providing an interface, the data receiving operation of the data receiving apparatus is controlled in accordance with control data supplied from a connected external device through the interface. Therefore, even if data which cannot be processed by only the data receiving apparatus, it can be processed under control of the connected external device.

According to another aspect of the present invention, there is provided a method of deinterleaving data in which data received by plural rearranging circuits are reproduced into data comprising the following steps of:

receiving format data; and

selecting one of said plural rearranging circuits in accordance with received format data.

According to the above method, a rearranging circuit is selected from the plural rearranging circuits in accordance with information of the data format if information (synchronization 1(S1)C1) of the data format is received. Thus, received data is reproduced by the selected rearranging circuit.

Therefore, the load of the process distributed to the hardware and the software can be balanced. Thus, the size of the circuit and the load of the CPU can be reduced.

Brief Description of the Drawings

FIG. 1 is a block diagram showing a circuit of a pager which is a first embodiment of a data receiving apparatus according to the present invention;

FIG. 2 is a circuit diagram showing an example of the internal structure of the received data buffer circuit 304 shown in FIG. 1;

FIG. 3 shows the correspondence between input to registers 3042 (Ra to Rh) and output from latches 3043 (La to Lh) with respect to 64-bit data supplied to the received data buffer circuit 304 shown in FIG. 2;

FIG. 4 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data (phase "a") in a range α for one block, the frame type

of which is 1600 bps (2-level FM) and which is transmitted at a frame speed of 1600 bps as shown in FIG. 32 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 5 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data (a pair of phases "a" and "c") in a range "α 1", which is transmitted at the first time, in the range α for one block, the frame type of which is 3200 bps (2-level FM) and which is transmitted at a frame speed of 3200 bps as shown in FIG. 34 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 6 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data (a pair of phases "a" and "c") in a range "α 2" which is transmitted at the second time, in the range α for one block, the frame type of which is 3200 bps (2-level FM) and which is transmitted at a frame speed of 3200 bps as shown in FIG. 34 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 7 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data (a pair of phases "a" and "c") in a range "α 1", which is transmitted at the first time, in the range α for one

block, the frame type of which is 3200 bps (4-level FM) and which is transmitted at a frame speed of 3200 bps as shown in FIG. 34 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 8 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data (a pair of phases "a" and "c") in a range "α 2", which is transmitted at the second time, in the range α for one block, the frame type of which is 3200 bps (4-level FM) and which is transmitted at a frame speed of 3200 bps as shown in FIG. 34 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 9 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data in a range "α 1", which is transmitted at the first time, in the range α for one block, the frame type of which is 6400 bps (4-level FM) and which is transmitted at a frame speed of 6400 bps as shown in FIG. 35 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 10 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data in a range "α 2", which is transmitted at the second time, in the range α for one block, the frame type of which is 6400 bps (4-level FM) and which is transmitted at

a frame speed of 6400 bps as shown in FIG. 35 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 11 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data in a range "α 3", which is transmitted at the third time, in the range α for one block, the frame type of which is 6400 bps (4-level FM) and which is transmitted at a frame speed of 6400 bps as shown in FIG. 35 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 12 shows the correspondence between input to the registers 3042 (Ra to Rh) and output from the latches 3043 (La to Lh) with respect to the bit data in a range "α 4", which is transmitted at the fourth time, in the range α for one block, the frame type of which is 6400 bps (4-level FM) and which is transmitted at a frame speed of 6400 bps as shown in FIG. 35 and received by the received data buffer circuit 304 shown in FIG. 2;

FIG. 13 is a diagram showing an example of the structure of memory areas of the RAM 403 shown in FIG. 1;

FIG. 14 is a block diagram showing an example of the structure of the deinterleaving circuit 5 shown in FIG. 1;

FIG. 15 is a diagram showing a rearranging operation which is performed by a rearranging

circuit 502;

FIG. 16 is a diagram showing the rearranging operation which is performed by a rearranging circuit 503;

FIG. 17 a diagram showing the rearranging operation which is performed by a rearranging circuit 504;

FIG. 18 is a circuit diagram showing an example of the internal structure of the address comparison circuit 6 shown in FIG. 1;

FIGS. 19A and 19B are a flow chart showing a data receiving operation which is performed by the pager according to the first embodiment of the present invention;

FIG. 20 is a flow chart showing the data receiving operation which is performed by the pager according to the first embodiment of the present invention;

FIGS. 21A and 21B are a flow chart showing the data receiving operation which is performed by the pager according to the first embodiment of the present invention;

FIG. 22 is a flow chart showing the data receiving operation which is performed by the pager according to the first embodiment of the present invention;

FIG. 23 is a flow chart showing a reproducing operation which is performed by the deinterleaving circuit 5 of the pager according to the first embodiment of the present invention;

FIG. 24 is a block diagram showing a circuit of a pager according to a second embodiment of the data receiving apparatus according to the present invention;

FIG. 25 is a diagram showing an example of the structure of memory areas in the RAM 404 shown in FIG. 24;

FIGS. 26A and 26B are a flow chart showing a data receiving operation which is performed by the pager according to the second embodiment of the present invention;

FIG. 27 is a flow chart showing the data receiving operation which is performed by the pager according to the second embodiment of the present invention;

FIG. 28 is a flow chart showing the data receiving operation which is performed by the pager according to the second embodiment of the present invention;

FIG. 29 is a flow chart showing the data receiving operation which is performed by the pager according to the second embodiment of the present invention;

FIG. 30 is a timing chart showing a data transmitting and receiving operations which is performed by a DMA circuit 11 when the data receiving operation is performed;

FIG. 31 is a block diagram showing the structure of a circuit of a modification of the second embodiment of the present invention;

FIG. 32 is a diagram showing an example of the

structure of transmitted data which is employed by pager system "RCR STD-43";

FIG. 33 is a diagram showing the structure of one block of an interleaved block structure D2 when the frame speed is 1600 bps (phase "a");

FIG. 34 is a diagram showing the structure of one block of an interleaved block structure D2 when the frame speed is 3200 bps (a pair of phases "a" and "c"); and

FIG. 35 is a diagram showing the structure of one block of the interleaved block structure D2 when the frame speed is 6400 bps.

Best Mode of Carrying Out the Invention

A preferred embodiment of a data receiving apparatus and a method of reproducing received data according to the present invention will now be described with reference to the accompanying drawings. Note that the embodiments employ the data structure C and block structure D shown in FIG. 32.

(First Embodiment)

FIG. 1 is a block diagram showing the structures of circuits in a pager which is a first embodiment of a data receiving apparatus according to the present invention. The pager comprises an antenna 1, a receiver circuit 2, a decoder section 3, a control section 4, a deinterleaving circuit 5, an address comparison circuit 6, a display unit 7, a notifying section 8 and a power

supply circuit 9.

The antenna 1 receives data transmitted from a transmitting station of, for example, a pager service company in the format shown in FIG. 32 to supply the received data to the receiver circuit 2.

The receiver circuit 2 is connected to the decoder section 3 and arranged to be operated in response to a control signal supplied from the decoder section 3 so as to demodulate and wave-detect the received data. The receiver circuit 2 fetches the synchronization 1 (S1)C1 to select and output serial bit data in accordance with the 2-level FM or 4-level FM modulation method. That is, when the 2-level FM modulation is performed, only "d" is output. When 4-level FM modulation is performed, MSB signal of 4-level FM bit data is output to "d" and LSB signal is output to "e".

Data included in the frame pattern data obtained by fetching the synchronization 1 (S1)C1 and relating to the modulation method, is supplied to a level determining circuit 301 through the output "d", while data relating to the frame speed is supplied to a frame speed determining circuit 302. The decoder section 3 determines the frame pattern of the interleaved block structure D2 following the synchronization 2 (S2)C3 in response to a line selection signal "a" output from the level determining circuit 301, a shift clock signal "b" output from the frame speed determining circuit 302 and

a data trigger "c" output from the timing control circuit 303. Moreover, the decoder section 3 converts the detected digital data into 8-bit parallel data in accordance with the modulation method so as to supply the obtained 8-bit parallel data to a bus line "B".

The decoder section 3 includes the level determining circuit 301, the frame speed determining circuit 302, a timing control circuit 303 and a received data buffer circuit 304. Each of the level determining circuit 301 and frame speed determining circuit 302 has a buffer memory (not shown). The buffer memories store control data output from a CPU 401 of the control section 4 when initialization is performed, data included in the received frame type data which relates to the modulation method and data relating to the frame speed. Moreover, the buffer memories store control data output from the CPU 401 of the control section 4.

The level determining circuit 301 receives serial bit data "d" (data of the synchronization 1 (S1)C1) output from the receiver circuit 2 to determine the modulation method of the received data so as to generate the line selection signal "a".

The frame speed determining circuit 302 receives the serial data "d" (data of the synchronization 1 (S1)C1) output from the receiver circuit 2 so as to determine the frame type of the received data. Specifically, the frame speed determining circuit 302

determines the frame type among the following four types:

1. 1600bps 2-Level FM (Binary FSK Modulation/1600 bps)

2. 3200bps 2-Level FM (Binary FSK modulation/3200 bps)

3. 3200bps 4-Level FM (Quadruple FSK modulation/3200 bps)

4. 6400bps 4-Level FM (Quadruple FSK modulation/6400 bps)

After the frame speed determining circuit 302 has determined the frame type, it generates the shift clock signal "b".

The timing control circuit 303 has a buffer for temporarily storing timing control information obtained from the CPU 401 when the synchronizing signal portion D1 has been received. Thus, the timing control circuit 303 controls bit-synchronization and the frame-synchronization of the decoder section 3. Moreover, the timing control circuit 303 generates the data trigger "c" for controlling an output timing of 8-bit parallel data from the received data buffer circuit 304.

The received data buffer circuit 304 converts serial bit data (outputs "d" and "e") output from the receiver circuit 2 into 8-bit parallel data so as to output the 8-bit parallel data to the bus line "B". The received data buffer circuit 304 converts the above bit

data in unit of 64 bits in accordance with the line selection signal "a" output from the level determining circuit 301, the shift clock signal "b" output from the frame speed determining circuit 302 and the data trigger "c" output from the timing control circuit 303 so as to sequentially output 8-bit parallel data.

The control section 4 includes a CPU 401, a ROM 402 and a RAM 403 and controls the overall operation of the pager in accordance with a control program stored in the ROM 402.

The CPU 401 has a buffer memory 4011 for temporarily storing the frame pattern data read from, for example, the synchronization 1 (S1)C1, a buffer memory 4012 for temporarily storing data (cycle number, frame number and number of plural output operations) read from the frame information (F1)C2, a buffer memory 4013 for storing block information (BI)C4 and data (the start word of the address field (AF)C4, vector field (VF)C5,and own message data in the message field (MF)C6, and the message length of own message data in the message field (MF)C6) read from the vector field (VF) C5, a buffer memory 4014 for storing reproduced data in unit of one block so as to correct errors and a clock generator 4015 for generating clocks for use to adjust the timing of the receiving process and the like.

The CPU 401 controls circuit sections connected with each data by data and clocks contained in the above

one frame.

The ROM 402 stores various programs for operating the CPU 401 and ID information for storing information of the frequency bands which must be received by the own pager, frame data and address data, which are ID codes of the own pager, and phase data indicating the phase in which the ID codes are stored.

As shown in FIG. 13, the RAM 403 has a work area WA for use in an operation of the CPU 401, a data reading memory area RDA for use in reproducing the received data and a memory area MMA for use in a process for storing the received message data.

The memory area RDA is a memory area for temporarily storing 8-bit parallel data output from the decoder section 3 before it has been output to a deinterleaving circuit 5 to be described later. When the output timing to the deinterleaving circuit 5 has been detected under control of the CPU 401, the number of bits of data (16 bits if the frame speed is 3200 bps and 32 bits if the frame speed is 6400 bps) which can be reproduced is sequentially output to the deinterleaving circuit 5.

The deinterleaving circuit 5, for each phase, reproduces 16-bit data of 3200 bps (2-level FM), 16-bit data of 3200 bps (4-level FM) and 32-bit data of 6400 bps (4-level FM) in accordance with the corresponding frame pattern so as to output reproduced

data to the bus line "B".

The address comparison circuit 6 operates in accordance with the data trigger "c" output from the timing control circuit 303 and which compares and collates whether address data, which is included in the reproduced address field (AF)C5, coincides with address data of the own pager.

The display unit 7 is a circuit section formed by, for example, a liquid crystal panel, a display buffer or a driver so as to display information, such as a message, on a liquid crystal panel.

The notifying section 8 is composed of notifying means including, for example, an LED (Light Emission Diode) which is turned on or allowed to flicker to notify the receipt of message, a speaker which produces sound for notifying the same, a vibrator which is vibrated to notify the same.

The power supply circuit 9 supplies electric power to the overall circuits of the pager when a power switch (not shown) is switched on.

The decoder section 3 will now be described in detail. FIG. 2 is a circuit diagram showing the internal structure of the received data buffer circuit 304 in the decoder section 3. The received data buffer circuit 304 shown in FIG. 2 has eight registers 3042 consisting of registers Ra to Rh for, in unit of 8-bit from B0 to B7, sequentially storing serial bit data

output from the receiver circuit 2 through the outputs "d" and "e"; eight latches 3043 consisting of La to Lh respectively corresponding to the foregoing registers 3042; and a line selection circuit 3044.

A principle of the operation of the decoder section 3 to convert serial bit data to 64-bit data in 8-bit parallel will now be described. FIG. 3 shows correspondence between the inputs to the registers 3042 (Ra to Rh) and the outputs from the latches 3043 (La to Lh) with respect to the 64-bit data input to the received data buffer circuit 304 in one input operation.

As can be understood from table shown in FIG. 3, serial bit data supplied to B7 of the register Rh of the registers 3042 shown in FIG. 2 is, as 8-bit parallel data, output to D7 of the latch Lh of the latches 3043. Serial bit data supplied to B4 of the register Rd of the registers 3042 is, as 8-bit parallel data, output to D3 of the latch Le of the latches 3043.

FIGS. 4 to 12 show correspondence between the inputs to the registers 3042 (Ra to Rh) and the outputs from the latches 3043 (La to Lh) with respect to bit data in a range α among bit data in one block shown in FIGS. 32 to 35 in cases of frame types/rates 1600 bps (2-level FM: when phase "a" has been received), 3200 bps (2-level FM : when the pair of phases "a" and "c" has been received), 3200 bps (4-level FM : when the pair of phases "a" and "c" has been received) and 6400 bps

(4-level).

In the received data buffer circuit 304, the shift clock signal "b" output from the frame speed determining circuit 302 is supplied to each of the registers 3042, while the line selection signal "a" output from the level determining circuit 301 is supplied to the received data buffer circuit 304. The data trigger "c" output from the timing control circuit 303 is supplied to each of the latches 3043.

When 2-level FM bit data has been output from the receiver circuit 2, the registers 3042 (Ra to Rh), which are input registers, fetch 64-bit data through the output "d". When 4-level FM bit data has been output from the receiver circuit 2, the registers 3042 fetch MSB (upper bits) of 64-bit data through the output "d" and LSB (lower bits) through the output "e".

Thus-fetched bit data is controlled by the line selection signal "a" output from the level determining circuit 301, the shift clock signal "b" output from the frame speed determining circuit 302 and the data trigger "c" output from the timing control circuit 303 as follows so that bit data is output as 8-bit parallel data corresponding to the respective frame types/rates.

1. In a case where the frame type is 1600 bps (2-level FM: when phase "a" has been received"):

When bit data, the frame type of which is 1600 bps (2-level FM), has been fetched, the bit data

sequentially output from the receiver circuit 2 through the output "d" as W(word)0a1, W1a1, W2a1, W3a1, ..., in a direction indicated by an arrow β shown in FIG. 33 is, as shown in FIG. 4, fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rh) in the vertical directional order as W(word)0a1, W1a1, W2a1, W3a1, ..., W5a8, W6a8 and W7a8. When the data trigger "c" has been supplied, 64 bits are, in unit of 8-bit, output to the bus line B through D0 to D7 of the latches 3043 (La to Lh).

Since 8-bit parallel data of this frame type has been received in a single phase, the process for reproducing data is completed at this time. Thus, data is, as it is, output to the buffer memory 4014 through the bus line "B". Then, the CPU 401 performs an error correction process.

Moreover, since 8 bits $\times$ 8 columns, that is, 8-byte data, output from the received data buffer circuit 304 in one output operation uses only one phase, bit data in one block is converted into 8-bit parallel data for one block by performing the foregoing operation four times for each 64 bits in the case shown in FIG. 32.

2. In a case where the frame type is 3200 bps (2-level FM: when the pair of phases "a" and "c" has been received):

In the case where the frame type is 3200 bps (2-level FM), bit data in the phases "a" and "c" is

multiplexed and fetched. Therefore, paralleled data is allowed to pass through the RDA of the RAM 403, and then subjected to the so-called data reproducing process in the deinterleaving circuit 5 so that the received data is separated for each phase. Then, reproduced data is, through the bus line "B", stored in the buffer memory 4014, and then subjected to the error correction process in the CPU 401.

As for a portion in the range α which is indicated by α 1, bit data sequentially output from the receiver circuit 2 through the output "d" as W0a1, W0c1, W1a1, ..., in a direction indicated by an arrow β shown in FIG. 34 is, as shown in FIG. 5, fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rh) in the vertical directional order as W0a1, W0c1, W1a1, ..., W6c4, W7a4 and W7c4. When the data trigger "c" has been supplied, 64 bits are, in unit of 8-bit, output to the bus line "B" through D0 to D7 of the latches 3043 (La to Lh).

As for a portion in the range α which is indicated by α 2, bit data sequentially output from the receiver circuit 2 through the output "d" as W0a5, W0c5, W1a5, ..., in a direction indicated by an arrow β shown in FIG. 34 is, as shown in FIG. 6, fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rh) in the vertical directional order as W0a5, W0c5, W1a5, ..., W6c8, W7a8 and W7c8. When the data trigger "c" has been

supplied, 64 bits are, in unit of 8-bit, output to the bus line "B" through D0 to D7 of the latches 3043 (La to Lh).

3. In a case where the frame type is 3200 bps (4-level FM: when the pair of phases "a" and "c" has been received):

In the case where the frame type is 3200 bps (4-level FM), bit data in the phases "a" and "c" is multiplexed and fetched. Therefore, paralleled data is allowed to pass through the RDA of the RAM 403, and then subjected to the so-called data reproducing process in the deinterleaving circuit 5 so that received data is separated for each phase. Then, reproduced data is, through the bus line "B", stored in the buffer memory 4014, and then subjected to the error correction process in the CPU 401.

In this case, each one bit included in the phase "a" and the phase "c" is taken so that 2 bits (one symbol) are obtained. Therefore, serial bit data is supplied in such a manner that one bit data in the phase "a" and that in the phase "c", respectively are, as MSB and LSB, supplied in parallel to the received data buffer circuit 304 through the outputs d and e of the receiver circuit 2.

Therefore, data in the LSB of one symbol data is stored in the front portion from Ra to Rd of the registers 3042, while data in the MSB of the same is

stored in the rear portion from Re to Rh.

As for a portion in the range α which is indicated by α 1, bit data in the MSB sequentially output from the receiver circuit 2 through the output "d" as W0a1, W1a1, W2a1, ..., in a direction indicated by an arrow β shown in FIG.34 is, as shown in FIG. 7, fetched by B0 of the register 3042 (Re) to B7 of the register 3042 (Rh) in the vertical directional order as W0a1, W1a1, W2a1, ..., W5a4, W6a4 and W7a4. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D4 to D7 of the latches 3043 (La to Lh).

Simultaneously, bit data in the LSB sequentially output from the receiver circuit 2 through the output "e" as W0c1, W1c1, W2c1, ..., in a direction indicated by an arrow β shown in FIG. 34 is, as shown in FIG. 7, fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rd) in the vertical directional order as W0c1, W1c1, W2c1, ..., W5c4, W6c4 and W7c4. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D0 to D3 of the latches 3043 (La to Lh).

As for a portion in the range α which is indicated by α 2, bit data in the MSB sequentially output from the receiver circuit 2 through the output "d" as W0a5, W0c5, W1a5, ,..., in a direction indicated by an arrow β shown in FIG.34 is, as shown in FIG. 8, fetched by B0 of

the register 3042 (Re) to B7 of the register 3042 (Rh) in the vertical directional order as W0a5, W1a5, W2a5, ..., W5a8, W6a8 and W7a8. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D4 to D7 of the latches 3043 (La to Lh).

Simultaneously, bit data in the LSB sequentially output from the receiver circuit 2 through the output "e" as W0c5, W1c5, W2c5, ..., in a direction indicated by an arrow β shown in FIG. 34 is , as shown in FIG. 8, fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rd) in the vertical directional order as W0c5, W1c5, W2c5, ..., W5c8, W6c8 and W7c8. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D0 to D3 of the latches 3043 (La to Lh).

Since data of 8 bits × 8 columns, that is, 8-byte data, which is output from the received data buffer circuit 304 in one output operation uses the phases "a" and "c", bit data for one block is converted into 8-bit parallel data for one block by performing the foregoing operations by eight times for each 64-bit data as shown in FIG. 34.

4. In a case where the frame type is 6400 bps (4-level FM):

In the case where the frame type is 6400 bps (4-level FM), all of the phase "a", phase "b", phase "c"

and phase "d" are multiplexed and fetched. Therefore, paralleled data is allowed to pass through the RDA of the RAM 403, and then subjected to the so-called data reproducing process in the deinterleaving circuit 5 so that received data is separated for each phase. Then, reproduced data is, through the bus line "B", stored in the buffer memory 4014, and then subjected to the error correction process in the CPU 401.

In the case of 6400 bps (4-level FM), each one bit included in the phase "a" and the phase "b" is taken so that 2 bits (one symbol) are obtained. Moreover, each one bit included in the phase "c" and the phase "d" is taken so that 2 bits (one symbol) are obtained. Therefore, serial bit data is supplied in such a manner that one bit data in the phase "a" and that in the phase "c", are, MSB, and that in the phase "b" and that in the phase "d" are, as LSB, supplied through the outputs "d" and "e" of the receiver circuit 2.

Therefore, data in the LSB of one symbol data is stored in the front portion from Ra to Rd of the registers 3042, while data in the MSB of the same is stored in the rear portion from Re to Rh.

As for a portion in the range α which is indicated by α 1, bit data in the MSB sequentially output from the receiver circuit 2 through the output "d" as W0a1, W0c1, W1a1, ..., in a direction indicated by an arrow β shown in FIG. 35, is, as shown in FIG. 9, fetched by B0 of

the register 3042 (Re) to B7 of the register 3042 (Rh) in the vertical directional order as W0a1, W0c1, W1a1, ..., W6c2, W7a2 and W7c2. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D4 to D7 of the latches 3043 (La to Lh).

Simultaneously, bit data in the LSB sequentially output from the receiver circuit 2 through the output "e" as W0b1, W0d1, W1b1, ..., in a direction indicated by an arrow β shown in FIG. 35 is fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rd) in the vertical directional order as W0b1, W0d1, W1b1, ..., W6d2, W7b2 and W7d2. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D0 to D3 of the latches 3043 (La to Lh).

As for a portion in the range α which is indicated by α 2, bit data in the MSB sequentially output from the receiver circuit 2 through the output "d" as W0a3, W0c3, W1a3, ..., in a direction indicated by an arrow β shown in FIG. . 35, is, as shown in FIG. 10, fetched by B0 of the register 3042 (Re) to B7 of the register 3042 (Rh) in the vertical directional order as W0a3, W0c3, W1a3, ..., W6c4, W7a4 and W7c4. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D4 to D7 of the latches 3043 (La to Lh).

Simultaneously, bit data in the LSB sequentially output from the receiver circuit 2 through the output "e" as W0b3, W0d3, W1b3, ..., in a direction indicated by an arrow β shown in FIG. 35 is fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rd) in the vertical directional order as W0b3, W0d3, W1b3, ..., W6d4, W7b4 and W7d4. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D0 to D3 of the latches 3043 (La to Lh).

As for a portion in the range α which is indicated by α 3, bit data in the MSB sequentially output from the receiver circuit 2 through the output "d" as W0a5, W0c5, W1a5, ..., in a direction indicated by an arrow β shown in FIG. 35, is, as shown in FIG. 11, fetched by B0 of the register 3042 (Re) to B7 of the register 3042 (Rh) in the vertical directional order as W0a5, W0c5, W1a5, ..., W6c6, W7a6 and W7ct. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D4 to D7 of the latches 3043 (La to Lh).

Simultaneously, bit data in the LSB sequentially output from the receiver circuit 2 through the output "e" as W0b5, W0d5, W1b5, ..., in a direction indicated by an arrow β shown in FIG. 35 is fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rd) in the vertical directional order as W0b5, W0d5, W1b5, ...,

W6d6, W7b6 and W7d6. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D0 to D3 of the latches 3043 (La to Lh).

As for a portion in the range α which is indicated by α 4, bit data in the MSB sequentially output from the receiver circuit 2 through the output "d" as W0a7, W0c7, W1a7, ..., in a direction indicated by an arrow β shown in FIG. 35, is, as shown in FIG. 12, fetched by B0 of the register 3042 (Re) to B7 of the register 3042 (Rh) in the vertical directional order as W0a5, W0c5, W1a5, ..., W6c6, W7a6 and W7c6. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D4 to D7 of the latches 3043 (La to Lh).

Simultaneously, bit data in the LSB sequentially output from the receiver circuit 2 through the output "e" as W0b7, W0d7, W1b7, ..., in a direction indicated by an arrow β shown in FIG. 35 is fetched by B0 of the register 3042 (Ra) to B7 of the register 3042 (Rd) in the vertical directional order as W0b7, W0d7, W1b7, ..., W6d8, W7b8 and W7d8. When the data trigger "c" has been supplied, 32 bits are, in unit of 4-bit, output to the bus line "B" through D0 to D3 of the latches 3043 (La to Lh).

Since data of 8 bits × 8 columns, that is, 8-byte data, which is output from the received data buffer

circuit 304 in one output operation uses all of the phases "a", "b", "c" and "d", bit data for one block is converted into 8-bit parallel data for one block by performing the foregoing operation by 16 times for each 64 bits as shown in FIG. 32.

The deinterleaving circuit 5 will now be described. The deinterleaving circuit 5 is separately provided from the decoder section 3 and controlled by the CPU 401 to reproduce the received interleaved block structure D2 in accordance with the received frame type so as to output the reproduced interleaved block structure D2 to the buffer memory 4014.

FIG. 14 is a block diagram showing an example of the structure of the deinterleaving circuit 5. The deinterleaving circuit 5 shown in FIG. 14 comprises shift registers 501A, 501B, 501C and 501D, rearranging circuits 502, 503 and 504 and a selector circuit 505.

Each of the shift registers 501A, 501B, 501C and 501D has a memory, the capacity of which is 8 bits, and receives data from the selector circuit 505 in unit of 8-bit. The shift registers 501A and 501B have output terminals connected to addresses 0 and 1 of the rearranging circuit 502 and to addresses 4 and 5 of the rearranging circuit 504. The shift registers 501C and 501D have output terminals connected to addresses 2 and 3 of the rearranging circuit 503 and to addresses 6 and 7 of the rearranging circuit 504.

The selector circuit 505 has an output terminal connected to the shift registers 501A, 501B, 501C and 501D and arranged to determine a rearranging circuit by selecting the address, to which data is input, the selection being performed under control of the CPU 401. The selector circuit 505 output data supplied from the RDA to each shift register corresponding to the output of the rearranging circuit.

The rearranging circuit 502 treats data, the frame type of which is 3200 bps (2-level FM), such that it fetches 1-byte data from each of the shift registers 501A and 501B to rearrange 2-byte data. Then, the rearranging circuit 502 sequentially output, to the bus line "B", reproduced data in unit of 1-byte, that is, in unit of 8-bit, in the total sum of 2 bytes.

The rearranging circuit 503 treats data, the frame type of which is 3200 bps (4-level FM), such that it fetches 1-byte data from each of the shift registers 501C and 501D to rearrange 2-byte data. Then, the rearranging circuit 503 sequentially output, to the bus line "B", two type data in unit of 1-byte, that is, in unit of 8-bit.

The rearranging circuit 504 treats data, the frame type of which is 6400 bps (4-level FM), such that it fetches 1-byte data from each of the shift registers 501A, 501B, 501C and 501D to rearrange 4-byte data to sequentially output 4-byte reproduced data in unit of

1-byte, that is, in unit of 8-bit, to the bus line "B".

The operation of the deinterleaving circuit 5 will now be described. FIGS. 15 to 17 are diagrams respectively showing the rearranging operations of the rearranging circuits 502, 503 and 504 provided to correspond to the frame types/rates. Referring to FIGS. 15 to 17, a portion of 8-bit data RD, stored in the shift registers 501A to 501D so as to be rearranged and output, which corresponds to four bits including D0 to D3 of the input data WR is referred to LSB, while a portion corresponding to four bits including D4 to D7 is referred to MSB.

1. In the case of 3200 bps (2-level FM):

As shown in FIG. 15, the rearranging circuit 502 is supplied with 8-bit data (D0 to D7) stored in the shift register 501A and 8-bit data (D0 to D7) stored in the shift register 501B by two supplying operations. Then, the rearranging operation is performed such that four odd-order bits (D0, D2, D4 and D6) of 8-bit data supplied to address 1 are rearranged to LSB of address 1 and four even-order bits (D1, D3, D5 and D7) are rearranged to LSB of address 0 so as to be reproduced and output to the bus line "B".

On the other hand, four odd-order bits (D0, D2, D4 and D6) of 8-bit data supplied to address 0 are rearranged to MSB of address 0 and four even-order bits (D1, D3, D5 and D7) are rearranged to MSB of address 1

so as to be reproducing and output to the bus line "B".

As described above, the rearranging circuit 502 is able to reproduce 16-bit (8 bits × 2) data.

2. In the case of 3200 bps (4-level FM):

As shown in FIG. 16, the rearranging circuit 503 is supplied with 8-bit data (D0 to D7) stored in the shift register 501C and 8-bit data (D0 to D7) stored in the shift register 501D by two supplying operations. Then, the rearranging operation is performed such that MSB (D4, D5, D6 and D7) of 8-bit data supplied to address 2 are rearranged to MSB of address 2 and LSB (D0, D1, D2 and D3) are rearranged to MSB of address 3 so as to be reproduced and output to the bus line "B".

On the other hand, MSB (D4, D5, D6 and D7) of 8-bit data supplied to address 3 are rearranged to LSB of address 2 and LSB (D0, D1, D2 and D3) are rearranged to LSB of address 3 so as to be reproduced and output to the bus line "B".

3. In the case of 6400 bps (4-level FM):

Addresses 4, 5, 6 and 7 of the rearranging circuit 504 are, as shown in FIG. 17, supplied with 8-bit data (D0 to D7) respectively stored in the shift registers 501A to 501D in four supplying operations. When the rearranging operation is performed, D5 and D7 in the MSB portion are fetched from input 8-bit data in each of addresses 4, 5, 6 and 7. Then, each of 2-bit data is assigned from LSB portion of address 4 which is output

to the bus line "B" so that 8-bit data at address 4 is formed.

Similarly, D4 and D6 in the MSB portion are fetched from input 8-bit data in each of addresses 4, 5, 6 and 7. Then, each of 2-bit data is assigned from LSB portion of address 5 which is output to the bus line "B" so that 8-bit data at address 5 is formed.

Similarly, D3 and D1 in the LSB portion are fetched from input 8-bit data in each of addresses 4, 5, 6 and 7. Then, each of 2-bit data is assigned from LSB portion of address 6 which is output to the bus line "B" so that 8-bit data at address 6 is formed.

Similarly, D2 and D0 in the LSB portion are fetched from input 8-bit data in each of addresses 4, 5, 6 and 7. Then, each of 2-bit data is assigned from LSB portion of address 7 which is output to the bus line "B" so that 8-bit data at address 7 is formed.

As described above, the rearranging circuit 504 is able to reproduce 6400 bps (4-level FM) 32-bit (8 bits × 4) of 8-bit parallel data.

The address comparison circuit 6 will now be described. FIG. 18 is a circuit diagram showing an example of the internal structure of the address comparison circuit 6. The address comparison circuit 6 has, for example, an address register 601 for previously storing the own address data (21 bits), a comparison circuit 602 for comparing received/reproduced address

data with address data which is stored in the address register 601 and a shift register 603 for outputting, to the bus line "B", an 8-bit coincidence signal "f", which is a result of the comparison performed by the comparison circuit 602.

The operation will now be described. The address field (AF)C5 of data reproduced by the deinterleaving circuit 5 has formatted address data which must be compared and collated with address data previously stored in the own pager.

When the comparison circuit 602 has, in unit of 8-bit, fetched data (data structure in the reproduced address field (AF)C5) supplied from the bus line "B" and which is a subject of comparison, the comparison circuit 602 compares the fetched data and address data supplied from the address register 601 (by using, for example, an EXOR circuit). By totaling the result of the comparison of each bit, a final result of the comparison is obtained (by using, for example, a NOR circuit). The result of the comparison is output to the shift register 603. The shift register 603 sequentially fetches the results of the comparison from the comparison circuit 602 so that the 8-bit coincidence signal "f" denoting the comparison result of the 8-byte address is output.

The overall operation of the circuit for receiving and reproducing data according to the first embodiment will now be described. FIGS. 19 to 22 are flow charts

of the main operation of the pager. FIG. 23 is a flow chart of the operation of the deinterleaving circuit 5.

The main operation of the pager will now be described. FIGS. 19 to 22 are flow charts of the operations of the CPU 401 and the decoder section 3 to be performed from a moment at which the power source of the pager has been turned on to a moment of completion of an operation for receiving data for one frame wherein the operations of the CPU 401 and the decoder section 3 are linked to each other. Note that the operation of the decoder section 3 is described as step R... and that of the CPU 401 is described as step C....

When a predetermined number of bit data has been stored in the RDA of the RAM 403, which can be reproduced by the deinterleaving circuit 5 and CPU 401 has detected the timing at which the deinterleaving circuit 5 can perform a reproducing process, the CPU 401 always output data to the deinterleaving circuit 5 through the bus line "B". The CPU 401 fetches data from the decoder section 3 to write this data to the RDA and performs an operation for correcting an error of data one preceding block stored in the buffer memory 4014 so as to read the contents.

Therefore, if address data included in the received address field (AF)C5 has been determined to be non-coincidence on the basis of the coincidence signal supplied from the address comparison circuit 6, control

is performed such that the operations of the decoder section 3 and the receiver circuit 2 are interrupted.

Referring to FIGS. 19 to 22, data receiving and reproducing processes will now be described. When the CPU 401 has detected at step C1 that the electric power has been supplied by the operation of a power supply switch (not shown), the CPU 401 allows electric power to be supplied to the respective circuit sections connected to the CPU 401 and initializes the sections. At this time, also the operation of the decoder section 3 is started when the initializing operation has been performed so that control data for controlling the received data buffer circuit 304 corresponding to each frame pattern is set to the frame speed determining circuit 302 and the level determining circuit 301. Then, the decoder section 3 is brought into a standby state at the frequency band and the phase set by ID-ROM (steps R1 and R2). In this standby state, the CPU 401 starts an internal timer (not shown) to perform intermittent reception in a period from 1.875 seconds (one frame) to 10 seconds at intervals of 30 seconds for two minutes until synchronization is detected when the synchronization 1 (S1)C1 of the synchronizing signal portion D1 is received (step C3). Then, synchronization detection is performed by receiving the synchronization 1 (S1)C1 until a predetermined time has been elapsed (steps C4 and C6).

If synchronization has been detected, the operation proceeds to step C5 so that the timer is reset, and frame pattern data set by the synchronization 1 (S1)C1 is stored in the buffer memory 4011. If no synchronization is detected in two minutes and the lapse of the predetermined time has been confirmed, the pager is moving or stays in an area outside the service zone. Therefore, the operation proceeds to step C7 in which the fact that the pager exists outside the service zone is displayed on display unit 7. Moreover, an out-of-zone notification interruption signal for interrupting out-of-zone notification, which is output by the notifying portion 8 when the pager exists outside the zone, is output.

When the decoder section 3 has received the synchronization 1 (S1)C1, the decoder section 3 fetches it and causes the level determining circuit 301 to store data included in frame pattern data set by the synchronization 1 (S1)C1 and relating to the modulation method (step R3). Moreover, the decoder section 3 causes the frame speed determining circuit 302 to store data included in the frame pattern data set by the synchronization 1 (S1)C1 and relating to the frame speed (step R4). The received frame pattern data is also output to the CPU 401.

The decoder section 3 continues the intermittent reception at steps R2, R3 and R6 until the out-of-zone

notification interruption signal is received by the CPU 401 at step C7. When the out-of-zone notification interruption signal has been received, the operation proceeds to step R7 in which the operation of the receiver circuit 2 is interrupted.

After step R4 has been performed, the decoder section 3 receives frame information (F1)C2 at step R5, and then output, to the CPU 401, the received cycle number, the received frame number and this timing information for obtaining the own frame from the frame information (F1)C2. The CPU 401, at step C8, recognizes the position of the own frame in accordance with the frame information 42B (FI) and timing information supplied from the decoder section 3 to interrupt operation of the receiver circuit 2 to the timing for the own frame comes. The process at step C8 is continued to the timing for the frame precedes to the own frame by one (step C9). The control of interrupting the operation of the receiver circuit 2 is performed by the decoder section 3 under control of the CPU 401 (step R8). The process at step R8 is repeatedly performed until a re-drive signal is input (step R9).

If the frame timing, which is preceding to the own frame by one, is detected at step C9, the CPU 401 re-drives the decoder section 3 at step C10. When the decoder section 3 is instructed to re-drive from the CPU 401 (step R9), it re-drives the decoder section 3

(step R10) in which the decoder section 3 waits for input of a re-drive control signal for the receiver circuit 2 from the CPU 401 (step R11). When the re-drive control signal for the receiver circuit 2 has been supplied from the CPU 401, the receiver circuit 2 is re-driven at step R12.

The CPU 401 re-drives the decoder section 3 (step C10), and then, at step C11, sets address data read from the ID-ROM of the ROM 402 to the address register of the address comparison circuit 6. At step C12, the CPU 401 determines an output timing of the final block of the frame, which is preceding to the own frame by one. When the timing of the final block has been detected, the CPU 401 outputs an operation control signal to the receiver circuit 2 (step C13).

When the receiver circuit 2 has been re-driven, the decoder section 3 establishes synchronization by the synchronization 1 (S1)C1 of the own frame received at step R13. Moreover, the decoder portion 3 causes the level determining circuit 301 to store data among frame pattern data of the own frame relating to the modulation method and that relating to the frame speed (step R16). Simultaneously, the received frame pattern data is also output to the CPU 401.

Then, the decoder section 3 fetches, decodes and outputs frame information (F1)C2 at step R14. Since the frame type data is, at step R13, also output to the CPU

401, the CPU 401 causes the buffer memory 4011 to re-store the frame type data at step C14. At step C15, whether or not the frames coincide with each other is determined in accordance with the decoded frame information (F1)C2. If non-coincidence is detected, the operation returns to step C8 in which frame timing, which is preceding to the own frame by one, is waited for. If coincidence is detected, the operation proceeds to step C16 in which the own frame is confirmed, continuous reception is controlled and the address of the rearranging circuit is determined by the deinterleaving circuit 5.

The decoder section 3 outputs frame information (F1)C2 to the CPU 401 at step R14, and then, at step R15, waits for input of an interruption signal which is generated when the frame non-coincidence is detected. If the interruption signal has been supplied, the operation returns to step R8 in which the operation of the receiver circuit 2 is interrupted. If the interruption is not supplied, the operation proceeds to step R16. At step R16, the synchronization 2 (S2)C3 is received, and then the timing control circuit 303 confirms synchronization of the reception of the interleaved block structure D2 and performs fine adjustment. At step R17, received data is rearranged by the received data buffer circuit 304 so that the rearranged data is output as 8-bit parallel data.

Then, the operation proceeds to step R18 in which block information (BI)C4, address field (AF)C5 and vector field (VF)C6 set by the synchronizing signal portion D1 are input and the reception is continued.

At step C16, the CPU 401 also performs a process for supplying a selection control signal for selecting any one of the rearranging circuits 502, 503 and 504 which is to be connected to the selector circuit 505 of the deinterleaving circuit 5 in accordance with the frame type of the subject frame by determining the address to be employed (the operation proceeds to step D1 shown in FIG. 23).

After the operation at step C16 has been completed, the CPU 401 determines at step C17 whether or not the received frame type is 1600 bps (2-level FM). If the frame type is 1600 bps (2-level FM), the operation proceeds to step S38 in which the start word of the address field (AF)C5 is read from the block information (BI)C4 so as to be stored in the buffer memory 4013. Then, the operation proceeds to step C39.

If a determination has been performed at step C17 that data is output with a frame type except 1600 bps (2-level FM), the operation proceeds to step C18 in which received data is sequentially stored in the RDA of the RAM 403 until the number of bits of data is stored to permit the reproducing process to be performed and the timing of the reproducing process comes (step C19).

When a determination has been performed that the number of bits of data, which permits the reproducing process can be performed, has been stored and the timing of the reproducing process has come, the operation proceeds to step C20 in which data is read from the RDA to supply data to the deinterleaving circuit 5. Thus, the deinterleaving circuit 5 starts performing the process for reproducing data (refer to step D4 shown in FIG. 23).

The operation of the deinterleaving circuit 5 shown in FIG. 23 will now be described. At step D1, the selector circuit 505 determines the address of the rearranging circuit for storing 8-bit data in accordance with the selection control signal for the rearranging circuit determined at step C16. Then, an operation for waiting for input of 8-bit parallel data starts (step D2). If input of 8-bit parallel data has been confirmed at step D3, the operation proceeds to step D4 in which the input 8-bit parallel data are sequentially stored in the shift register 501 (A to D). Then, 8-bit parallel data are output to the address of the rearranging circuits from the respective shift registers at step D5 as described with reference to FIGS. 15 to 17. Data reproduced by each of the rearranging circuits is, at step D6, again output to the bus line "B". After the reproducing process at step D6 has been completed, operations at steps C21, C25 and C35 are performed.

After the reproducing process at step D6 has been

completed, the CPU 401 stores this data in the buffer memory 4014 to subject the same to the error correction process. At step C21, the start word of the address field (AF)C5 is read in accordance with the block information (BI)C4 to store it in the buffer memory 4013. Then, the operation proceeds to step C22.

At step C22, the CPU 401 stores the received data in the RDA of the RAM 403. At step C23, the CPU 401 determines whether a predetermined number of bits of data, which permits the reproducing process can be performed, has been stored and the timing of the reproducing process has come. If the storage of the predetermined number bits of data and the reproducing timing are confirmed at step C23, the received data are sequentially read from the RDA so as to be output to the deinterleaving circuit 5, at step C24. When data has been supplied to the deinterleaving circuit 5 through the bus line "B", the deinterleaving circuit 5 reproduces data, the frame type of which is that except 1600 bps (2-level FM) and are stored in the shift register 501 (A to D) at step D3.

Then, when the reproduced data is fetched from the deinterleaving circuit 5 through the bus line "B", the CPU 401 stores this data in the buffer memory 4014 to subject the same to the error correction process. Then, the CPU 401 outputs address data included in the address field (AF)C5 to the address comparison circuit 6 (step

C25). At this time, the address comparison circuit 6 compares the received address data fetched through the bus line "B" at the timing of the data trigger "c" with the address data in the address register 601. Then, the coincidence signal "f" denoting the coincidence or non-coincidence is output to the CPU 401.

The CPU 401 instructs the decoder section 3 to fetch data. If the CPU 401 has detected coincidence of addresses because it has received the coincidence signal "f" from the address comparison circuit 6 at step C26, the operation proceeds to step C28. If the coincidence of addresses is not detected, the operation proceeds to step C27 in which the CPU 401 outputs an interruption signal to the decoder section 3. When the interruption signal has been supplied to the decoder section 3 from the CPU 401, the operation returns to step R8 in which the operation of the receiver circuit 2 is interrupted. If the coincidence signal "f" is not supplied, the operation proceeds to step R20. At steps R20 and R21, reception is continued until the interruption signal is received from the CPU 401.

At step C28, data of vector field (VF)C6 is read from the RDA following the address field (AF)C5 so that the start word and the number of words in the message field (MF)C7 are determined. At step C29, a process for interrupting the operation of the receiver circuit 2 until the start word of own message data appears is

performed. When the interruption control starts, only own message data can be fetched in accordance with the determined start word. Since the decoder section 3 receives the interruption signal at step R21, the decoder section 3 interrupts the operation of the receiver circuit 2 at step R22 and the above-mentioned state is maintained until the re-drive signal is received.

When the CPU 401 has confirmed the timing for receiving the start word of own message data at step C30, the CPU 401 outputs the re-drive signal to the decoder section 3 at step C31 in order to re-drive the receiver circuit 2. Thus, the receiver circuit 2 receives data. At step C32, the CPU 401 sequentially stores received data in the RDA through the decoder section 3. When the decoder section 3 has received the above-mentioned re-drive signal output at step C31 (step R23), the receiver circuit 2 is re-driven (step R24).

After data storage in the RDA has been started at step C32, the CPU 401 determines at step C23 whether a predetermined number of bits of data, which permits the reproducing process can be performed, has been stored and the timing of the reproducing process has come. If the storage of the predetermined number bits of data and the reproducing timing are confirmed at step C32, the received data (message data) are sequentially read from the RDA so as to be output to the deinterleaving circuit

5, at step C35. When the deinterleaving circuit 5 performs the data reproducing process, data in the next block is stored in the RDA. Then, the operation proceeds to step C35.

When data reproduced by the deinterleaving circuit 5 has been output to the bus line "B", idle blocks (IB)C8 is detected at step C35. When the idle blocks (IB)C8 is detected, an interruption signal is output to the decoder section 3 in order to interrupt the operation of the receiver circuit 2 to the timing for receiving the own frame. In order to control the reception notification at step C37, the CPU 401 causes the notifying section 8 to notify the reception and reproduces and displays a message in accordance with the received own message data, and then the operation returns to step C9. Thus, the CPU 401, at step C9, waits for the timing of the frame, which precedes to the own frame by one. When the receiver circuit 2 has been re-driven at step R24, the decoder section 3 continues the reception operation until the operation is interrupted by the CPU 401 at step C36 (steps R25 and R26). When the interruption signal has been received at step R26, the operation proceeds to step R27 in which the operation of the receiver circuit 2 is interrupted. Then, the decoder section 3 completes the receiving operation.

Thus, the operations of the CPU 401 and the decoder

section 3 have been described so that they are linked to each other to receive data with the frame pattern except 1600 bps (2-level FM) in accordance with a result of the determination performed at step C17. If the frame type of the received data is determined as 1600 bps (2-level FM) at step C17, the receiving operation, which is performed by the CPU 401, is shifted to step C38 in which an operation, in which the reproducing operation is not performed, is started.

At step C38, the block information (BI)C4 is fetched into the buffer memory 4014 so as to be subjected to the error correction process. Then, the start word of the address field (AF)C5 is stored. The CPU 401, at step C39, outputs address data, which is stored in the address field (AF)C5, to the address comparison circuit 6. Thus, the address comparison circuit 6 compares the received address data fetched through the bus line "B" at the timing of the supplied data trigger "c" with the address data in the address register 601. Then, the address comparison circuit 6 outputs the coincidence signal "f" to the CPU 401.

When the CPU 401 has detected the coincidence signal "f" denoting the coincidence of the addresses supplied from the address comparison circuit 6 at step C40, the CPU 401 shifts the operation to step C41. If the coincidence signal "f" is not detected, the CPU 401 shifts the operation to step C27 in which

an interruption signal is output to the decoder section 3. When the decoder section 3 has received the interruption signal from the CPU 401, the operation returns to step R8 in which the operation of the receiver circuit 2 is interrupted. If the coincidence signal "f" is not detected, the operation proceeds to steps R20 and R21 in which reception is continued until the interruption signal is supplied from the CPU 401.

At step C41, data of the vector field (VF)C6 is, following the address field (AF)C5, supplied from the receiver circuit 2 so that the start word of own message data and the number of words in the message field (MF)C7 are determined. At step C42, control is performed such that the operation of the receiver circuit 2 is interrupted until the start word of own message data is detected. When the interruption control has started, only own message can be fetched in accordance with the determined start word. Since the decoder section 3 receives the interruption signal at step R21, it interrupts the operation of the receiver circuit 2 at step R22 and maintains this state until the re-drive signal is supplied.

When the CPU 401 has confirmed timing for receiving the start word of own message data at step C43, the CPU 401 outputs the re-drive signal to the decoder section 3 in order to re-drive the receiver circuit 2 (step C44). Thus, the receiver circuit 2 receives data, and the CPU

401 sequentially reads own message data in unit of 8-bit (step C45) and detects the idle blocks (IB)C8 (step C46). When the re-drive signal output at step C31 has been supplied at step R23, the decoder section 3 re-drives the receiver circuit 2 (step R24).

If the idle blocks (IB)C8 has been detected at step C45, an interruption signal is output to the decoder section 3 in order to interrupt the operation of the receiver circuit 2 to the timing for receiving a next own frame (step C36). The CPU 401, at step C37, causes the notifying section 8 to perform the notification process and reproduces and displays the message in accordance with the received message data in order to control notification of reception. Then, the CPU 401 returns the operation to step C9. As described above, the CPU 401, at step C9, waits for timing for the frame, which is preceding to the own frame by one. After the receiver circuit 2 has been re-driven at step R24, the decoder section 3 continues the receiving operation until the operation is interrupted by the CPU 401 at step C36 (steps R25 and R26). When the interruption signal has been received at step R26, the operation proceeds to step R27 in which the operation of the receiver circuit 2 is interrupted. Then, the decoder section 3 completes the receiving operation.

As described above, according to the first embodiment, when information (synchronization 1 (S1)C1)

indicating the frame type has been received, the frame type of the data is determined. In accordance with the determined frame type, a suitable rearranging circuit is selected from the plural rearranging circuits. Therefore, load distribution to the hardware and software can be balanced. As a result, the size of the circuit and the load of the CPU can be reduced.

(Second Embodiment)

The first embodiment has the structure such that the data receiving operation is performed by the CPU 401 as follows. When a predetermined number of data bits have been stored in the RDA in the RAM 403, which can be reproduced and the timing for performing the reproducing process comes, a suitable rearranging circuit is selected from the plural rearranging circuits in the deinterleaving circuit 5 in accordance with the frame type of the received data. The addresses of the data reproduced by the selected rearranging circuit are subjected to a comparison processing. If the coincidence is detected, own data of the message field is fetched so that the reproducing process is performed.

However, according to the first embodiment, the CPU 401 controls the data transfer among the RAM 403, the deinterleaving circuit 5 and the address comparison circuit 6, complicated control of data transfer is required in addition to the main operation for reproducing data. Therefore, there sometimes arises

a problem in that the data processing rate is lowered.

Accordingly, a pager according to a second embodiment is provided with a DMA (Direct Memory Access) circuit 11. Thus, when the CPU 401 performs the data receiving operation, as shown in FIG. 30, the DMA circuit 11 controls data transfer among the CPU 401, the RAM 404, the deinterleaving circuit 5 and the BCH decoder 10 for performing the error correction process. Thus, load which must be borne by the CPU 401 for transferring data is intended to be reduced.

Referring to FIGS. 24 to 32, the second embodiment of the present invention will now be described. In the second embodiment, the data structure C and the block structure D shown in FIG. 32 are employed.

FIG. 24 is a block diagram showing the structure of circuits in the pager which is the second embodiment of the data receiving apparatus according to the present invention. The same elements as those of the pager according to the first embodiment and shown in FIG. 1 are indicated by the same reference numerals and the same elements are omitted from description.

The pager according to this embodiment comprises the antenna 1, the receiver circuit 2, the decoder section 3, the control section 4, the deinterleaving circuit 5, the address comparison circuit 6, the display unit 7, the notifying section 8, the power supply circuit 9, the BCH decoder 10, the DMA circuit 11 and

a key input section 12.

The control section 4 controls the overall operation of the pager in accordance with a control program stored in the ROM 402 and comprises the CPU 401, the ROM 402 and a RAM 404. The CPU 401 has the buffer memory 4011 for temporarily storing the frame pattern read from, for example, the synchronization 1 (S1)C1, the buffer memory 4012 for temporarily storing data (cycle number, frame number and number of plural output operations) read from the frame information (F1)C2, the buffer memory 4013 for storing the block information (BI)C4 and data read from the vector field (VF)C5 (the start word of the own message data and the number of words of message data in the address field (AF), the vector field (VF) and the message field (MF)) and the clock generator 4015 for generating clocks for use to adjust the timing of the receiving process and the like. The CPU 401 controls circuit sections connected to the CPU 401 by using the data contained in one frame and the clocks.

The RAM 404, as shown in FIG. 25, has a work area WA for enabling the CPU 401 to be operated, a memory area BDM (Block Data Memory) which is used to reproduce the received data and so that 11-block addresses of the received data for one frame supplied from the decoder section 3 at the time of performing the receiving operation are assigned in unit of block, and a memory

area MMA for storing the received message data.

The BDM stores data for one frame, which is being received and reproduced, by assigning the address.

Data thus-stored is, under control of the DMA circuit 11, to be described later, output to the deinterleaving circuit 5. Data reproduced by the deinterleaving circuit 5 is re-stored in the same storage address, and then output so as to be subjected to an error correction process in the BCH decoder 10.

In a case where the block data includes an address field, data subjected to the error correction process in the address comparison circuit 6 is again output so as to be subjected to a comparison of the address data is then subjected to the address comparison process. If the coincidence is detected, data is re-stored in the same address. If the non-coincidence is detected, data is not stored in the DBM and deleted.

The BCH decoder 10 corrects an error in data by using a 10-bit BCH code and even-number parity bits included in data for one block reproduced by the deinterleaving circuit 5, and then output the error bit number to the CPU 401.

The DMA (Direct Memory Access) circuit 11 controls data transfer among the CPU 401, the RAM 404, the deinterleaving circuit 5, the address comparison circuit 6 and the DMA circuit 11 through the bus line "B".

The key input section 12 is composed of a main

switch, cursor keys and memory keys to output signals denoting the operations of the key operations to the CPU 401.

The overall operation of the second embodiment will now be described.

FIGS. 26 to 29 are flow charts of the main operation of the pager. FIG. 30 is a timing chart of the operations in the DMA circuit 11 for reading and writing data between the BDM and the other circuits.

When the CPU 401 has detected at step C101 that the electric power has been supplied by the operation of a power supply switch (not shown), the CPU 401 allows electric power to be supplied to the respective circuit sections connected to the CPU 401 and initializes the sections. At this time, also the operation of the decoder section 3 is started when the initializing operation has been performed so that control data for controlling the received data buffer circuit 304 corresponding to each frame pattern is set to the frame speed determining circuit 302 and the level determining circuit 301. Then, the decoder section 3 is brought into a standby state at the frequency band and the phase set by ID-ROM (steps R101 and R102). In this standby state, the CPU 401 starts an internal timer (not shown) to perform intermittent reception in a period from 1.875 seconds (one frame) to 10 seconds at intervals of 30 seconds for two minutes until synchronization is

detected when the synchronization 1 (S1)C1 of the synchronizing signal portion D1 is received (step C103). Then, synchronization detection is performed by receiving the synchronization 1 (S1)C1 until a predetermined time has been elapsed (steps C104 and C106).

If synchronization has been detected, the operation proceeds to step C105 in which the timer is reset, and frame pattern data set by the synchronization 1 (S1)C1 is stored in the buffer memory 4011. If no synchronization is detected in two minutes and the lapse of the predetermined time has been confirmed, the pager is moving or stays in an area outside the service zone. Therefore, the operation proceeds to step C107 in which the fact that the pager exists outside the service zone is displayed on display unit 7. Moreover, an out-of-zone notification interruption signal for interrupting out-of-zone notification, which is output by the notifying portion 8 when the pager exists outside the zone, is output.

When the decoder section 3 has received the synchronization 1 (S1)C1, the decoder section 3 fetches it and causes the level determining circuit 301 to store data included in frame pattern data set by the synchronization 1 (S1)C1 and relating to the modulation method (step R103). Moreover, the decoder section 3 causes the frame speed determining circuit 302 to store

data included in the frame pattern data set by the synchronization 1 (S1)C1 and relating to the frame speed (step R104). The received frame pattern data is also output to the CPU 401.

The decoder section 3 continues the intermittent reception at steps R102, R103 and R106 until the out-of-zone notification interruption signal is received by the CPU 401 at step C107. When the out-of-zone notification interruption signal has been received, the operation proceeds to step R107 in which the operation of the receiver circuit 2 is interrupted.

After step R104 has been performed, the decoder section 3 receives frame information (F1)C2 at step R105, and then output, to the CPU 401, the received cycle number, the received frame number and this timing information for obtaining the own frame from the frame information (F1)C2. The CPU 401, at step C108, recognizes the position of the own frame in accordance with the frame information 42B (FI) and timing information supplied from the decoder section 3 to interrupt operation of the receiver circuit 2 until the timing for the own frame comes. The process at step C8 is continued to the timing for the frame which precedes to the own frame by one (step C109). The control of interrupting the operation of the receiver circuit 2 is performed by the decoder section 3 under control of the CPU 401 (step R108). The process at step R108 is

repeatedly performed until a re-drive signal is input (step R109).

If the frame timing, which is preceding to the own frame by one, is detected at step C109, the CPU 401 re-drives the decoder section 3 at step C110. When the decoder section 3 is instructed to re-drive from the CPU 401 (step R109), it re-drives the decoder section 3 (step R110) in which the decoder section 3 waits for input of a re-drive control signal for the receiver circuit 2 from the CPU 401 (step R111). When the re-drive control signal for the receiver circuit 2 has been supplied from the CPU 401, the receiver circuit 2 is re-driven at step R112.

The CPU 401 re-drives the decoder section 3 (step C110), and then, at step C111, sets address data read from the ID-ROM of the ROM 402 to the address register of the address comparison circuit 6. At step C112, the CPU 401 determines an output timing of the final block of the frame, which is preceding to the own frame by one. When the timing of the final block has been detected, the CPU 401 outputs an operation control signal to the receiver circuit 2 (step C113).

When the receiver circuit 2 has been re-driven, the decoder section 3 establishes synchronization by the synchronization 1 (S1)C1 of the own frame received at step R113. Moreover, the decoder portion 3 causes the level determining circuit 301 to store data among frame

pattern data of the own frame relating to the modulation method and that relating to the frame speed (step R116). Simultaneously, the received frame pattern data is also output to the CPU 401.

Then, the decoder section 3 fetches, decodes and outputs frame information (F1)C2 at step R114. Since the frame type data is, at step R113, also output to the CPU 401, the CPU 401 causes the buffer memory 4011 to re-store the frame type data at step C114. At step C115, whether or not the frames coincide with each other is determined in accordance with the decoded frame information (F1)C2. If non-coincidence is detected, the operation returns to step C108 in which frame timing, which is preceding to the own frame by one, is waited for. If coincidence is detected, the operation proceeds to step C116 in which the own frame is confirmed, continuous reception is controlled and the address of the rearranging circuit is determined by the deinterleaving circuit 5.

The decoder section 3 outputs frame information (F1)C2 to the CPU 401 at step R114, and then, at step R115, waits for input of an interruption signal which is generated when the frame non-coincidence is detected. If the interruption signal has been supplied, the operation returns to step R108 in which the operation of the receiver circuit 2 is interrupted. If the interruption is not supplied, the operation proceeds to

step R116. At step R116, the synchronization 2 (S2)C3 is received, and then the timing control circuit 303 confirms synchronization of the reception of the interleaved block structure D2 and performs fine adjustment. At step R117, received data is rearranged by the received data buffer circuit 304 so that the rearranged data is output as 8-bit parallel data. Then, the operation proceeds to step R118 in which block information (BI)C4, address field (AF)C5 and vector field (VF)C6 set by the synchronizing signal portion D1 are input and the reception is continued.

At step C116, the CPU 401 also performs a process for supplying a selection control signal for selecting any one of the rearranging circuits 502, 503 and 504 which is to be connected to the selector circuit 505 of the deinterleaving circuit 5 in accordance with the frame type of the subject frame by determining the address to be employed.

After the operation at step C116 has been completed, the CPU 401 determines at step C117 whether or not the received frame type is 1600 bps (2-level FM). If the frame type is 1600 bps (2-level FM), the operation proceeds to step C127 in which the start word of the address field (AF)C5 is read from the block information (BI)C4 so as to be stored in the buffer memory 4013. Then, the operation proceeds to step C128.

If a determination has been performed at step C117

that data is output with a frame type except 1600 bps (2-level FM), the operation proceeds to step C118 in which the 8-bit parallel data is stored in the BDA of the RAM 404 with the addresses being assigned.

When it is determined that the number of data bits, which permits the reproducing process can be performed, has been stored, the DMA circuit 11 sequentially reads the data from the BDM and supplies the data to the deinterleaving circuit 5. Thus, the deinterleaving circuit 5 performs the data reproducing process and re-stores the reproduced data at the read address. When the data of one block is reproduced, the data of one block are read from the BDM and are supplied to the BCH decoder 10. The error-corrected data of one block are re-stored at the read addresses.

Then, the CPU 401, at step C119, on the basis of the block information (BI)C4, reads the start word of each of the address field (AF)C5 and the vector field (VF)C6 of data subjected to the error correction process. Then, the operation proceeds to step C120.

Then, the CPU 401 instructs to perform a comparison of address data stored in the BDM of the RAM 404. The DMA circuit 11 reads address data included in the reproduced address field (AF)C5 which has been stored in the BDM so as to output the same to the address comparison circuit 6. The address comparison circuit 6, at the timing of the data trigger "c", compares the

address data received through the bus line "B" with the address data in the address register 601. Then, the address comparison circuit 6 outputs, to the CPU 401, a coincidence signal "f" denoting whether address data items coincide with each other.

The CPU 401 instructs the decoder section 3 to fetch data. Moreover, when the CPU 401 has detected the coincidence of addresses because it has received the coincidence signal "f" from the address comparison circuit 6 at step C120, it shifts the operation to step C121. If the address coincidence is not detected, the operation proceeds to step C123 in which an interruption signal is output to the decoder section 3. When the decoder section 3 has been supplied with the interruption signal from the CPU 401, the operation returns to step R108 in which the operation of the receiver circuit 2 is interrupted. If the coincidence signal "f" is not supplied, the operation proceeds to step R120 in which the receiving operation is continued.

At step C121, the start word and the number of words of own message data in the message field (MF)C7 are determined in accordance with vector data in the vector field (VF)C6. At step C122, data for one frame is sequentially fetched, and then storage address is assigned. Then, data is sequentially stored in the BDM of the RAM 404.

Simultaneously with the receiving operation

performed by the CPU 401, data which is sequentially stored in the BDM is repeatedly written to and read from both of the deinterleaving circuit 5 and the BCH decoder 10.

At step C124, the idle blocks (IB)C8 is detected. When the idle blocks (IB)C8 has been detected, an interruption signal is output in order to interrupt the operation of the receiver circuit 2 to the timing for receiving a next own frame. The CPU 401, at step C126, performs control of the reception notification by performing processes for reproducing and displaying message in accordance with the received message data subjected to the notifying process in the notifying section 8. Then, the operation returns to step C109. As described above, the CPU 401 waits for a frame timing which precedes to the own frame by one. Note that the receiving operation of the decoder section 3 is continued (step R121) until interruption of the operation is instructed from the CPU 401 at step C125. If the interruption signal is supplied at step R121, the operation proceeds to step R122 in which the operation of the receiver circuit 2 is interrupted. Then, the decoder section 3 completes the receiving operation.

The operations of the CPU 401 and the decoder section 3 have been described in which they are linked to each other to receive data with the frame pattern except 1600 bps in accordance with a result of the

determination performed at step C117. If the frame type of received data is detected as 1600 bps (2-level FM) at step C117, the receiving operation, which is performed by the CPU 401, is shifted to step C127 in which an operation, in which the reproducing operation is not performed, is started.

At step C127 block information (BI)C4 is output to the BCH decoder 10 so as to be subjected to the error correction process, and then stored in the BDM of the RAM 404. Then, the start words of each of the address field (AF)C5 and the vector field (VF)C6 are stored in the buffer memory 4013.

The CPU 401, at step C128, outputs address data, which is included in the address field (AF)C5, to the address comparison circuit 6. The address comparison circuit 6 compares the address data supplied through the bus line "B" at the timing of the data trigger "c" and the address data in the address register 601. Then, the address comparison circuit 6 outputs the coincidence signal "f" to the CPU 401.

At step C129, the CPU 401 detects the coincidence signal "f" supplied from the address comparison circuit 6. If the addresses coincide with each other, the operation proceeds to step C130. If the coincidence is not detected, the operation proceeds to step C123 in which an interruption signal is output to the decoder section 3. When the decoder section 3 has received the

interruption signal from the CPU 401, the operation returns to step R108 in which the operation of the receiver circuit 2 is interrupted. If the coincidence signal "f" is not detected, the operation proceeds to step R131 in which the receiving operation is continued.

At step C130, the start word and the number of words of own message data in the message field (MF)C7 are determined in accordance with data of the vector field (VF)C6.

The CPU 401 causes the receiver circuit 2 to continue the data receiving process in which data is sequentially stored in the BDM in unit of one block. Moreover, the CPU 401 causes the DMA circuit 11 to continue the data transfer processes (step C131). Then, own message data are sequentially read, and then the idle blocks (IB)C8 is detected (step C132).

If the idle blocks (IB)C8 is detected at step C132, the CPU 401 outputs an interruption signal to the decoder section 3 in order to interrupt the operation of the receiver circuit 2 to the timing for receiving a next own frame (step C125). In order to control the reception notification at step C125, the notification process is performed by the notifying section 8 and the message is reproduced and displayed in accordance with received own message data. Then, the operation returns to step C109. As described above, the CPU 401, at step C109, waits for the frame timing, which is preceding to

the own frame by one. When the interruption signal has been supplied to the decoder section 3 at step R121, the operation proceeds to step R122 in which the operation of the receiver circuit 2 is interrupted. Then, the decoder section 3 completes the receiving operation.

The operation, which is performed by the DMA circuit 11 will now be described with reference to a timing chart shown in FIG. 30. The timing chart shown in FIG. 30 shows the operation of the DMA circuit 11 for transfer data for one block (block #0) when data, the frame type of which is, for example, 6400 bps (4-level FM) has been received. Data, the frame type of which is 6400 bps (4-level FM), and which has been received by the receiver circuit 2 is decoded into parallel data by the decoder section 3 for each 8 bits. When parallel data has been output to the bus line "B", addresses are assigned and sequentially stored in the BDM formed in the RAM 404 under control of the CPU 401.

The DMA circuit 11, is turned on simultaneously with the reproducing process, sequentially makes accesses to data among 8-bit parallel data being stored in the BDM. The data of the block #0 having a predetermined number of bits which can be reproduced are sequentially read and supplied to the deinterleaving circuit 5. After the data reproducing process has been completed by the deinterleaving circuit 5, the reproduced data is again output to the BDM so as to be

written to the same address.

As described above, when data, the frame type of which is 6400 bps (4-level FM), has been received, the DMA circuit 11 repeatedly outputs and receives block data between the BDM and the deinterleaving circuit 5 until reproducing process for one block is performed four times.

In order to cause the BCH decoder 10 to BCH-decode (correct an error) data written back to the BDM by the DMA circuit 11, the CPU 401 causes the DMA circuit 11 to read data again from the BDM so as to output the same to the BCH decoder 10. After the BCH decoder 10 has completed the error correction process, corrected data is again output to the BDM so as to be written to the same address.

During the error correction process which is performed by the BCH decoder 10, the DMA circuit 11 makes an access to data in a next block (block #1) which is being stored in the BDM to follow an instruction from the CPU 401 to output the same to the deinterleaving circuit 5 so as to be reproduced. In the case shown in FIG. 30, a process is being performed with which data is output to the deinterleaving circuit 5 relating to a process for reproducing data (second time and third time) in the next blocks.

In a case where the corrected block is data (block #1 or block #1 and block #2) in the address field (AF)C5,

the CPU 401 reads address data in data which is written back to the BDM by the DMA circuit 11 and outputs the same to the address comparison circuit 6 so as to be compared with the address data of ID information. If the coincidence signal "f" from the address comparison circuit 6 is detected, the address data is written back to the BDM.

Simultaneously with the address comparison process which is performed by the address comparison circuit 6, the following process is repeatedly performed in the DMA circuit 11. The reproduced data (data of the block #3) is repeatedly transfered from the BDM to the BCH decoder 10 and the next data (data of the block #4) which is output from the decoder section 3 and stored in the BDM are accessed to be supplied to the deinterleaving circuit 5.

As described above, according to the second embodiment, the DMA circuit 11 for controlling data transfer among the CPU 401, the BDM of the RAM 404, the deinterleaving circuit 5, the address comparison circuit 6 and the BCH decoder 10 is provided in addition to the structure of the first embodiment so that the load which must be borne by the CPU 401 for transferring data is reduced.

FIG. 31 is a circuit diagram showing a modification of the second embodiment. As shown in FIG. 31, the structure according to this modification comprises

a receiver module 14 formed of a PC card having an interface 15 and a circuit substrate for a personal computer, and a portable data terminal 17 having an interface 16 for a PC card slot or the like.

Referring to FIG. 31, the receiver module 14 has the antenna 1, the receiver circuit 2, the decoder section 3, the buffer memories 4011 to 4014, the clock generator 4015, the ROM 402, the RAM 404, the deinterleaving circuit 5, the address comparison circuit 6, the BCH decoder 10, the DMA circuit 11 and the interface 15 capable of output and receiving data in the bus line "B". The portable data terminal 17 has the CPU 401 for controlling the data receiving and reproducing processes, the display unit 7, the notifying section 8 and a CPU 13 for controlling circuits in the portable data terminal 17.

Although both of the first embodiment and the second embodiment of the present invention have the structure such that the present invention is applied to a sole pager adapted to paging system STD-43, the present invention is not limited to this system. The present invention may be applied to any one of information communication terminal, data communication device connected to a personal computer and the like.

For example, the present invention may be applied to any pager adapted to a data communication method in which information about regulation of the data frame

speed or the modulation method can be output. In this case, even if a paging service company mixedly uses a plurality of paging systems, the pager according to the present invention may be applied.

C L A I M S

1. A data receiving apparatus comprising:

receiving means for receiving data;

plural reproducing means capable of reproducing received data having a format which can be recognized by said data receiving apparatus;

format data receiving means for receiving format data; and

selection means for selecting one of said plural reproducing means in accordance with the format data received by said format data receiving means.

2. A data receiving apparatus according to claim 1, wherein said format data denotes a data transmission rate.

3. A data receiving apparatus according to claim 2, further comprising control means for controlling a reproducing process rate of said selected reproducing means in accordance with the format data denoting the transmission rate received by said format data receiving means.

4. A data receiving apparatus according to claim 1, wherein said format data denotes a data modulation mode.

5. A data receiving apparatus according to claim 4, further comprising conversion means for converting data received by said one of plural receiving means into parallel data corresponding to the format data denoting the data modulation mode.

6. A data receiving apparatus according to any one of claims 5, wherein said conversion means comprises plural registers for used for converting received data into the parallel data and corresponding to data modulation modes.

7. A data receiving apparatus according to any one of claims 5, further comprising:

data storage means for dividing the parallel data output from said conversion means into data items of a predetermined unit and for sequentially storing divided data items;

reading means for reading the divided data items from said data storage means in a storing order and supplying read data items to said one of plural reproducing means selected by said selection means; and

storage control means for storing the parallel data output from said one of plural reproducing means in said data storage means at addresses of the divided data items read by said reading means.

8. A data receiving apparatus according to any one of claims 5, further comprising:

data storage means for storing data which is to be reproduced by one time by said one of plural reproducing means selected by said selection means;

detection means for detecting a data reproduction timing of said one of plural reproducing means selected by said selection means; and

storage control means for sequentially transferring the parallel data from said data storage means to said reproducing means and sequentially storing the parallel data output from said converting means to said data storage means.

9. A data receiving apparatus according to claim 1, wherein said format data includes first format data denoting a data transmission rate and second format data denoting a data modulation mode.

10. A data receiving apparatus according to claim 9, further comprising control means for controlling a reproducing process rate of said selected reproducing means in accordance with the first format data received by said format data receiving means.

11. A data receiving apparatus according to claim 10, further comprising conversion means for converting data received by said receiving means into parallel data corresponding to the second format data received by said format data receiving means.

12. A data receiving apparatus according to claim 11, wherein said conversion means comprises plural registers for used for converting received data into the parallel data and corresponding to data modulation modes.

13. A data receiving apparatus according to claim 11, further comprising:

data storage means for dividing the parallel data output from said conversion means into data items of

a predetermined unit and for sequentially storing divided data items;

reading means for reading the divided data items from said data storage means in a storing order and supplying read data items to said one of plural reproducing means selected by said selection means; and

storage control means for storing the parallel data output from said one of plural reproducing means in said data storage means at addresses of the divided data items read by said reading means.

14. A data receiving apparatus according to claim 11, further comprising:

data storage means for storing data which is to be reproduced by one time by said one of plural reproducing means selected by said selection means;

detection means for detecting a data reproduction timing of said one of plural reproducing means selected by said selection means; and

storage control means for sequentially transferring the parallel data from said data storage means to said reproducing means and sequentially storing the parallel data output from said converting means to said data storage means.

15. A data receiving apparatus according to claim 1, wherein said format data denotes a data interleaving mode.

16. A data receiving apparatus according to

claim 15, further comprising conversion means for converting data received by said receiving means into parallel data corresponding to the format data received by said format data receiving means.

17. A data receiving apparatus according to claim 16, wherein said conversion means comprises plural registers for used for converting received data into the parallel data and corresponding to data modulation modes.

18. A data receiving apparatus according to claim 16, further comprising:

data storage means for dividing the parallel data output from said conversion means into data items of a predetermined unit and for sequentially storing divided data items;

reading means for reading the divided data items from said data storage means in a storing order and supplying read data items to said one of plural reproducing means selected by said selection means; and

storage control means for storing the parallel data output from said one of plural reproducing means in said data storage means at addresses of the divided data items read by said reading means.

19. A data receiving apparatus according to claim 16, further comprising:

data storage means for storing data which is to be reproduced by one time by said one of plural reproducing means selected by said selection means;

detection means for detecting a data reproduction timing of said one of plural reproducing means selected by said selection means; and

storage control means for sequentially transferring the parallel data from said data storage means to said reproducing means and sequentially storing the parallel data output from said converting means to said data storage means.

20. A data receiving apparatus according to claim 1, further comprising format data storage means for storing the format data received by said format data receiving means until format data is received next.

21. A data receiving apparatus according to claim 1, further comprising:

ID code storage means for storing an ID code for specifying paging of said data receiving apparatus;

detection means for detecting the ID code from reproduced data while a reproducing process of said reproducing means continues; and

interrupting means for comparing a detected ID code with the ID code stored in said ID code storage means and for interrupting the reproducing process of said reproducing means when a coincidence is not detected.

22. A data receiving apparatus according to claim 1, which further comprises an interface for establishing a connection with an external device, and in which a receiving process of said data receiving apparatus is

performed in accordance with a control signal supplied from said external device through said interface.

23. A method of deinterleaving data in which data received by plural rearranging circuits are reproduced into data comprising the following steps of:

receiving format data; and

selecting one of said plural rearranging circuits in accordance with received format data.

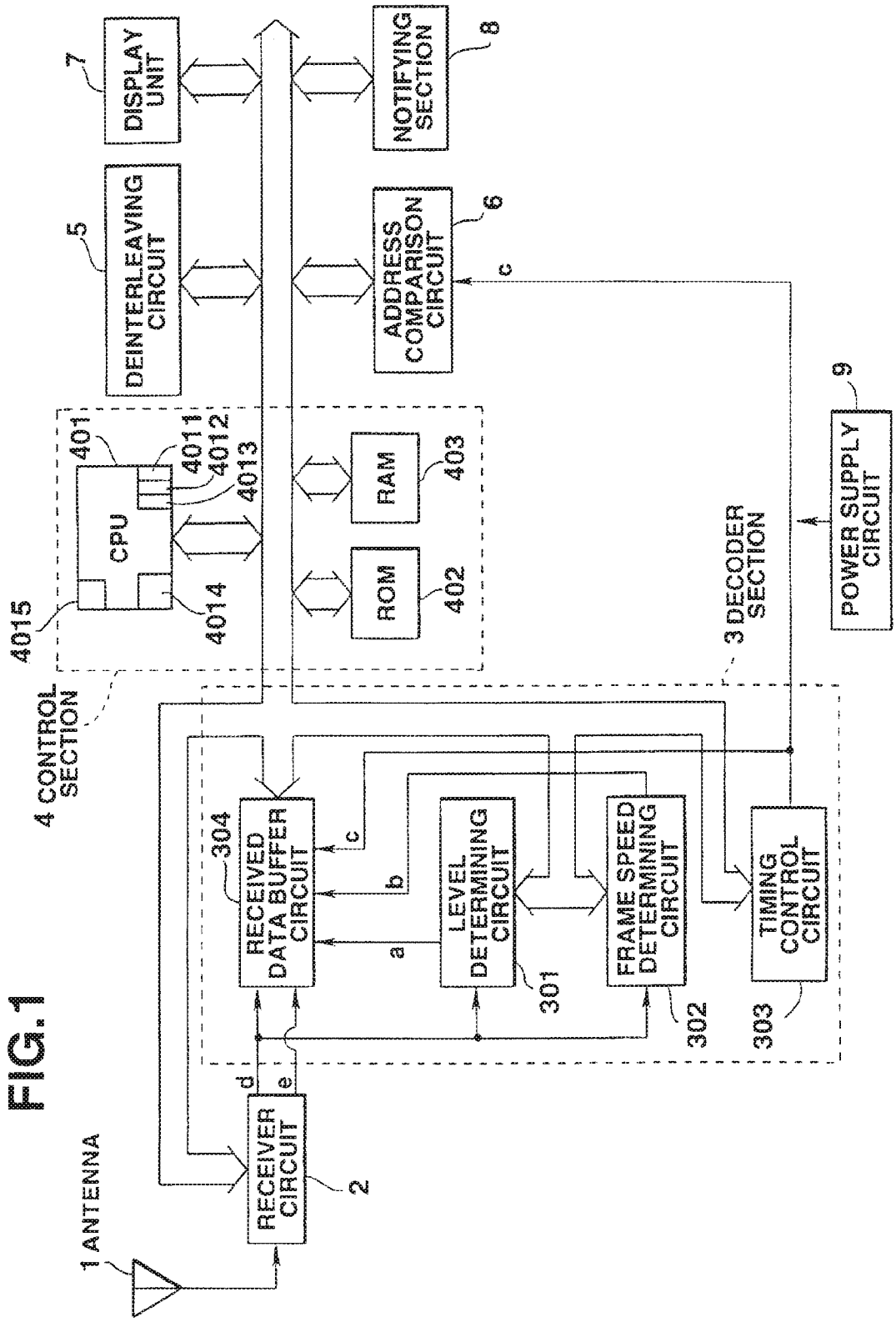

1 ANTENNA
RECEIVER CIRCUIT
2
4 CONTROL SECTION
4015
CPU
401
4011
4012
4013
4014
RAM
403
ROM
402
3 DECODER SECTION
RECEIVED DATA BUFFER CIRCUIT
304
LEVEL DETERMINING CIRCUIT
301
FRAME SPEED DETERMINING CIRCUIT
302
TIMING CONTROL CIRCUIT
303
a
b
c
d
e
DEINTERLEAVING CIRCUIT
5
ADDRESS COMPARISON CIRCUIT
6
DISPLAY UNIT
7
NOTIFYING SECTION
8
POWER SUPPLY CIRCUIT
9

FIG. 1

FIG.2

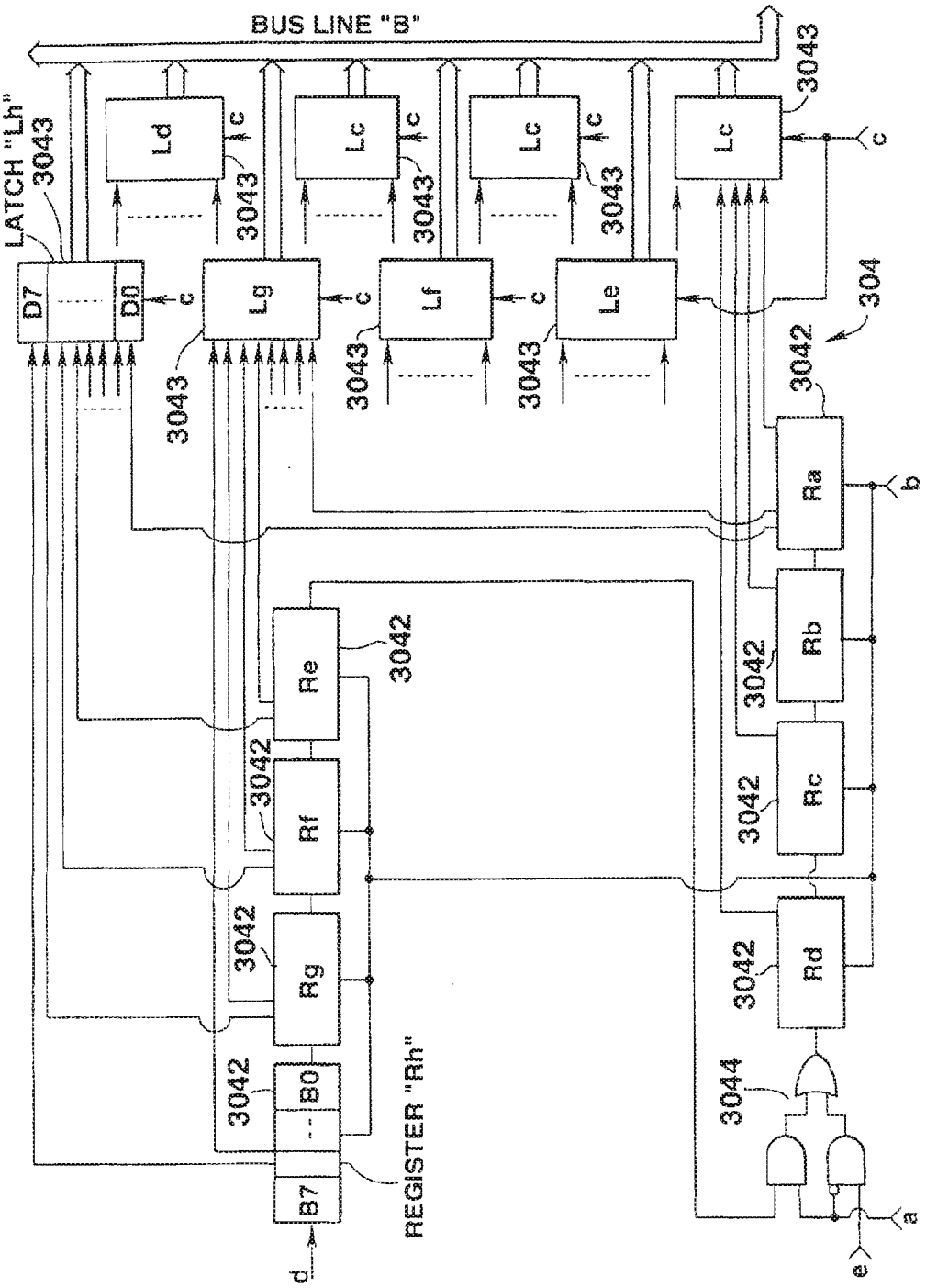

BUS LINE "B"
LATCH "Lh"
3043
D7
D0
Ld
Lc
Lg
Lf
Le
c
304
3042
Ra
Rb
Rc
Rd
Re
Rf
Rg
B0
B7
REGISTER "Rh"
3044
a
b
d
e

FIG.3

REGISTER		Rh	Rg	Rf	Re	Rd	Rc	Rb	Ra
	LATCH								
B7		LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
B6		LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
B5		LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
B4		LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
B3		LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
B2		LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
B1		LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
B0		LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0

FIG.4

REGISTER		Rh	Rg	Rf	Re	Rd	Rc	Rb	Ra
	LATCH								
B7		LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
		W7a8	W7a7	W7a6	W7a5	W7a4	W7a3	W7a2	W7a1
B6		LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
		W6a8	W6a7	W6a6	W6a5	W6a4	W6a3	W6a2	W6a1
B5		LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
		W5a8	W5a7	W5a6	W5a5	W5a4	W5a3	W5a2	W5a1
B4		LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
		W4a8	W4a7	W4a6	W4a5	W4a4	W4a3	W4a2	W4a1
B3		LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
		W3a8	W3a7	W3a6	W3a5	W3a4	W3a3	W3a2	W3a1
B2		LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
		W2a8	W2a7	W2a6	W2a5	W2a4	W2a3	W2a2	W2a1
B1		LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
		W1a8	W1a7	W1a6	W1a5	W1a4	W1a3	W1a2	W1a1
B0		LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0
		W0a8	W0a7	W0a6	W0a5	W0a4	W0a3	W0a2	W0a1

FIG.5

REGISTER		Rh	Rg	Rf	Re	Rd	Rc	Rb	Ra
	LATCH								
B7		LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
		W7c4	W3c4	W7c3	W3c3	W7c2	W3c2	W7c1	W3c1
B6		LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
		W7a4	W3a4	W7a3	W3a3	W7a2	W3a2	W7a1	W3a1
B5		LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
		W6c4	W2c4	W6c3	W2c3	W6c2	W2c2	W6c1	W2c1
B4		LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
		W6a4	W2a4	W6a3	W2a3	W6a2	W2a2	W6a1	W2a1
B3		LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
		W5c4	W1c4	W5c3	W1c3	W5c2	W1c2	W5c1	W1c1
B2		LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
		W5a4	W1a4	W5a3	W1a3	W5a2	W1a2	W5a1	W1a1
B1		LbD7	LbbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
		W4c4	W0c4	W4c3	W0c3	W4c2	W0c2	W4c1	W0c1
B0		LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0
		W4a4	W0a4	W4a3	W0a3	W4a2	W0a2	W4a1	W0a1

FIG.6

REGISTER		Rh	Rg	Rf	Re	Rd	Rc	Rb	Ra
	LATCH								
B7		LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
		W7c8	W3c8	W7c7	W3c7	W7c6	W3c6	W7c5	W3c5
B6		LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
		W7a8	W3a8	W7a7	W3a7	W7a6	W3a6	W7a5	W3a5
B5		LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
		W6c8	W2c8	W6c7	W2c7	W6c6	W2c6	W6c5	W2c5
B4		LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
		W6a8	W2a8	W6a7	W2a7	W6a6	W2a6	W6a5	W2a5
B3		LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
		W5c8	W1c8	W5c7	W1c7	W5c6	W1c6	W5c5	W1c5
B2		LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
		W5a8	W1a8	W5a7	W1a7	W5a6	W1a6	W5a5	W1a5
B1		LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
		W4c8	W0c8	W4c7	W0c7	W4c6	W0c6	W4c5	W0c5
B0		LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0
		W4a8	W0a8	W4a7	W0a7	W4a6	W0a6	W4a5	W0a5

FIG.7

REGISTER		Rh	Rf	Rf	Re	Rd	Rc	Rb	Ra
	LATCH								
B7		LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
		W7a4	W7a3	W7a2	W7a1	W7c4	W7c3	W7c2	W7c1
B6		LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
		W6a4	W6a3	W6a2	W6a1	W6c4	W6c3	W6c2	W6c1
B5		LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
		W5a4	W5a3	W5a2	W5a1	W5c4	W5c3	W5c2	W5c1
B4		LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
		W4a4	W4a3	W4a2	W4a1	W4c4	W4c3	W4c2	W4c1
B3		LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
		W3a4	W3a3	W3a2	W3a1	W3c4	W3c3	W3c2	W3c1
B2		LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
		W2a4	W2a3	W2a2	W2a1	W2c4	W2c3	W2c2	W2c1
B1		LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
		W1a4	W1a3	W1a2	W1a1	W1c4	W1c3	W1c2	W1c1
B0		LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0
		W0a4	W0a3	W0a2	W0a1	W0c4	W0c3	W0c2	W0c1

MSB LSB

FIG.8

REGISTER	Rh	Rg	Rf	Re	Rd	Rc	Rb	Ra
	LATCH							
B7	LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
	W7a8	W7a7	W7a6	W7a5	W7c8	W7c7	W7c6	W7c5
B6	LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
	W6a8	W6a7	W6a6	W6a5	W6c8	W6c7	W6c6	W6c5
B5	LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
	W5a8	W5a7	W5a6	W5a5	W5c8	W5c7	W5c6	W5c5
B4	LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
	W4a8	W4a7	W4a6	W4a5	W4c8	W4c7	W4c6	W4c5
B3	LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
	W3a8	W3a7	W3a6	W3a5	W3c8	W3c7	W3c6	W3c5
B2	LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
	W2a8	W2a7	W2a6	W2a5	W2c8	W2c7	W2c6	W2c5
B1	LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
	W1a8	W1a7	W1a6	W1a5	W1c8	W1c7	W1c6	W1c5
B0	LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0
	W0a8	W0a7	W0a6	W0a5	W0c8	W0c7	W0c6	W0c5

MSB LSB

FIG.9

REGISTER	Rh	Rg	Rf	Re	Rd	Rc	Rb	Ra
	LATCH							
B7	LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
	W7c2	W3c2	W7c1	W3c1	W7d2	W3d2	W7d1	W3d1
B6	LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
	W7a2	W3a2	W7a1	W3a1	W7b2	W3b2	W7b1	W3b1
B5	LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
	W6c2	W2c2	W6c1	W2c1	W6d2	W2d2	W6d1	W2d1
B4	LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
	W6a2	W2a2	W6a1	W2a1	W6b2	W2b2	W6b1	W2b1
B3	LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
	W5c2	W1c2	W5c1	W1c1	W5d2	W1d2	W5d1	W1d1
B2	LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
	W5a2	W1a2	W5a1	W1a1	W5b2	W1b2	W5b1	W1b1
B1	LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
	W4c2	W0c2	W4c1	W0c1	W4d2	W0d2	W4d1	W0d1
B0	LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0
	W4a2	W0a2	W4a1	W0a1	W4b2	W0b2	W4b1	W0b1
	MSB				LSB			

FIG.10

REGISTER	Rh	Rg	Rf	Re	Rd	Rc	Rb	Ra
	LATCH							
B7	LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
	W7c4	W3c4	W7c3	W3c3	W7d4	W3d4	W7d3	W3d3
B6	LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
	W7a4	W3a4	W7a3	W3a3	W7b4	W3b4	W7b3	W3b3
B5	LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
	W6c4	W2c4	W6c3	W2c3	W6d4	W2d4	W6d3	W2d3
B4	LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
	W6a4	W2a4	W6a3	W2a3	W6b4	W2b4	W6b3	W2b3
B3	LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
	W5c4	W1c4	W5c3	W1c3	W5d4	W1d4	W5d3	W1d3
B2	LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
	W5a4	W1a4	W5a3	W1a3	W5b4	W1b4	W5b3	W1b3
B1	LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
	W4c4	W0c4	W4c3	W0C3	W4d4	W0d4	W4d3	W0d3
B0	LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0
	W4a4	W0a4	W4a3	W0a3	W4b4	W0b4	W4b3	W0b3
	MSB				LSB			

FIG.11

REGISTER		Rh	Rg	Rf	Re	Rd	Rc	Rb	Ra
	LATCH								
B7		LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
		W7c6	W3c6	W7c5	W3c5	W7d6	W3d6	W7d5	W3d5
B6		LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
		W7a6	W3a6	W7a5	W3a5	W7b6	W3b6	W7b5	W3b5
B5		LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
		W6c6	W2c6	W6c5	W2c5	W6d6	W2d6	W6d5	W2d5
B4		LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
		W6a6	W2a6	W6a5	W2a5	W6b6	W2b6	W6b5	W2b5
B3		LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
		W5c6	W1c6	W5c5	W1c5	W5d6	W1d6	W5d5	W1d5
B2		LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD1	LcD0
		W5a6	W1a6	W5a5	W1a5	W5b6	W1b6	W5b5	W1b5
B1		LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD1	LbD0
		W4c6	W0c6	W4c5	W0c5	W4d6	W0d6	W4d5	W0d5
B0		LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD1	LaD0
		W4a6	W0a6	W4a5	W0a5	W4b6	W0b6	W4b5	W0b5
		MSB				LSB			

FIG.12

REGISTER		Rh	Rf	Rf	Re	Rd	Rc	Rb	Ra
	LATCH								
B7		LhD7	LhD6	LhD5	LhD4	LhD3	LhD2	LhD1	LhD0
		W7c8	W3c8	W7c7	W3c7	W7d8	W3d8	W7d7	W3d7
B6		LgD7	LgD6	LgD5	LgD4	LgD3	LgD2	LgD1	LgD0
		W7a8	W3a8	W7a7	W3a7	W7b8	W3b8	W7b7	W3b7
B5		LfD7	LfD6	LfD5	LfD4	LfD3	LfD2	LfD1	LfD0
		W6c8	W2c8	W6c7	W2c7	W6d8	W2d8	W6d7	W2d7
B4		LeD7	LeD6	LeD5	LeD4	LeD3	LeD2	LeD1	LeD0
		W6a8	W2a8	W6a7	W2a7	W6b8	W2b8	W6b7	W2b7
B3		LdD7	LdD6	LdD5	LdD4	LdD3	LdD2	LdD1	LdD0
		W5c8	W1c8	W5c7	W1c7	W5d8	W1d8	W5d7	W1d7
B2		LcD7	LcD6	LcD5	LcD4	LcD3	LcD2	LcD6	LcD6
		W5a8	W1a8	W5a7	W1a7	W5b8	W1b8	W5b7	W1b7
B1		LbD7	LbD6	LbD5	LbD4	LbD3	LbD2	LbD6	LbD6
		W4c8	W0c8	W4c7	W0c7	W4d8	W0d8	W4d7	W0d7
B0		LaD7	LaD6	LaD5	LaD4	LaD3	LaD2	LaD6	LaD6
		W4a8	W0a8	W4a7	W0a7	W4b8	W0b8	W4b7	W0b7
		MSB				LSB			

FIG.13

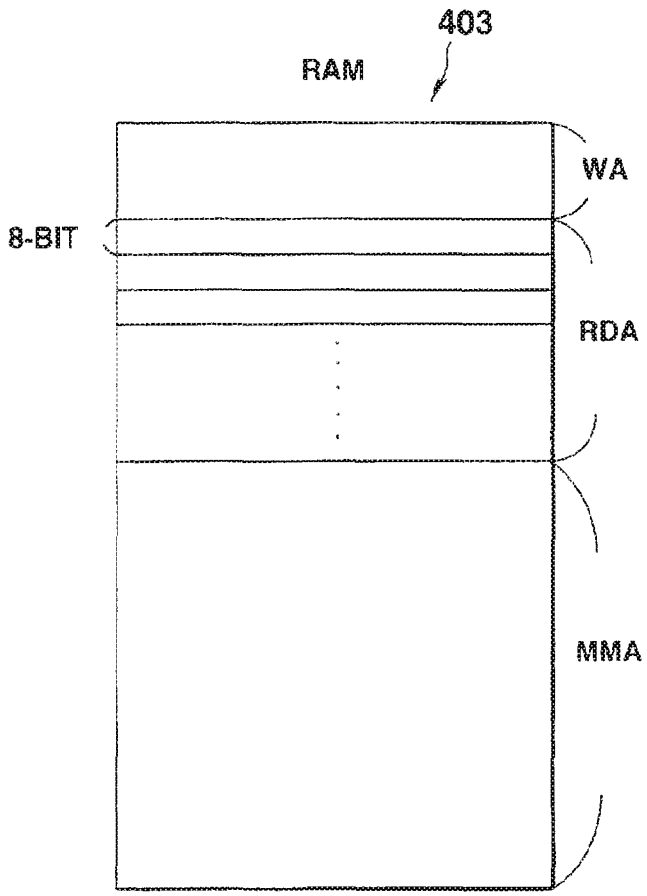


FIG.14

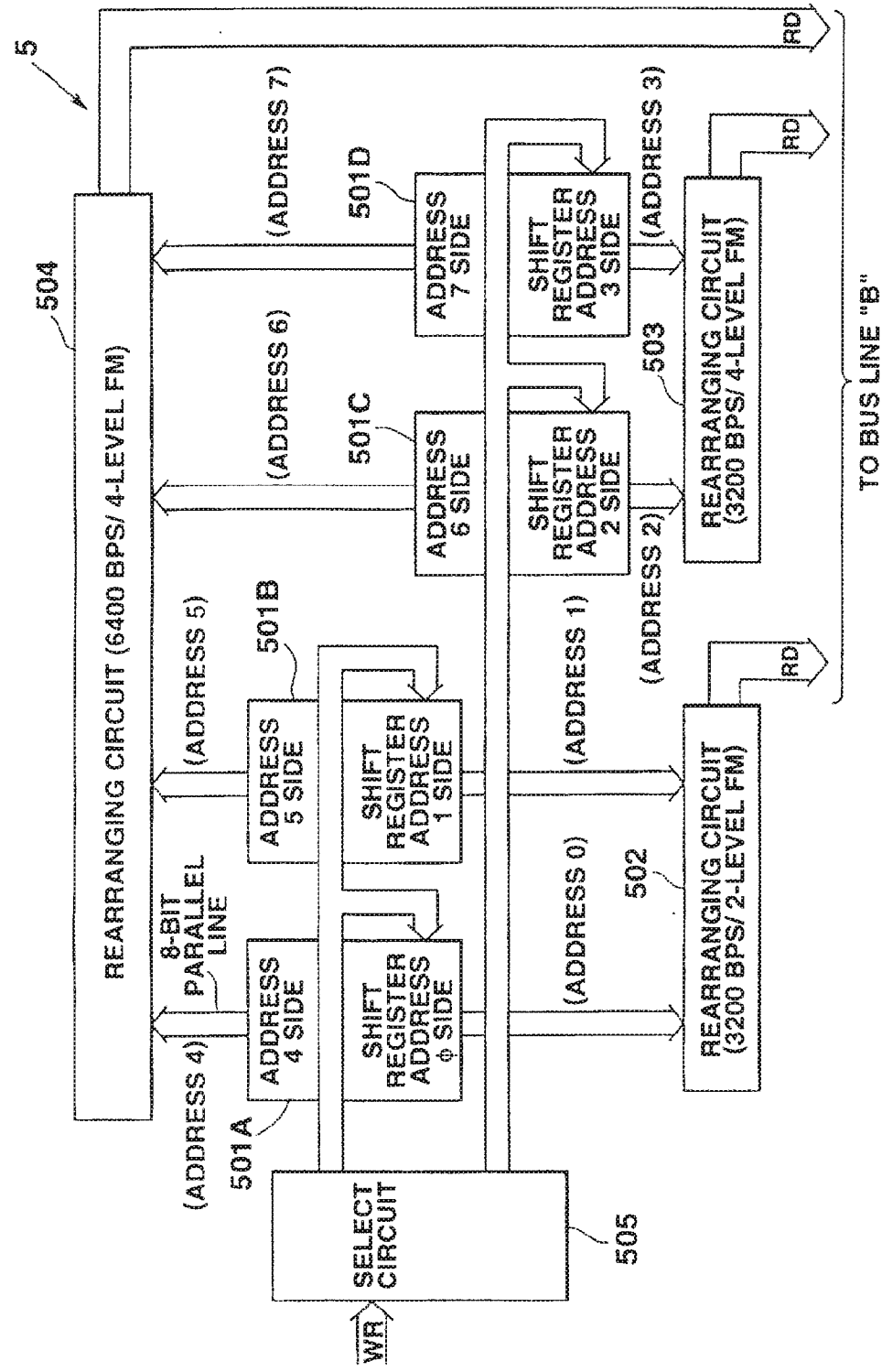

5
504
REARRANGING CIRCUIT (6400 BPS/ 4-LEVEL FM)
8-BIT PARALLEL LINE
(ADDRESS 4)
(ADDRESS 5)
(ADDRESS 6)
(ADDRESS 7)
501A
ADDRESS 4 SIDE
501B
ADDRESS 5 SIDE
501C
ADDRESS 6 SIDE
501D
ADDRESS 7 SIDE
SHIFT REGISTER ADDRESS ϕ SIDE
SHIFT REGISTER ADDRESS 1 SIDE
SHIFT REGISTER ADDRESS 2 SIDE
SHIFT REGISTER ADDRESS 3 SIDE
(ADDRESS 0)
(ADDRESS 1)
(ADDRESS 2)
(ADDRESS 3)
502
503
REARRANGING CIRCUIT (3200 BPS/ 2-LEVEL FM)
REARRANGING CIRCUIT (3200 BPS/ 4-LEVEL FM)
RD
RD
RD
TO BUS LINE "B"
SELECT CIRCUIT
505
WR

FIG.15

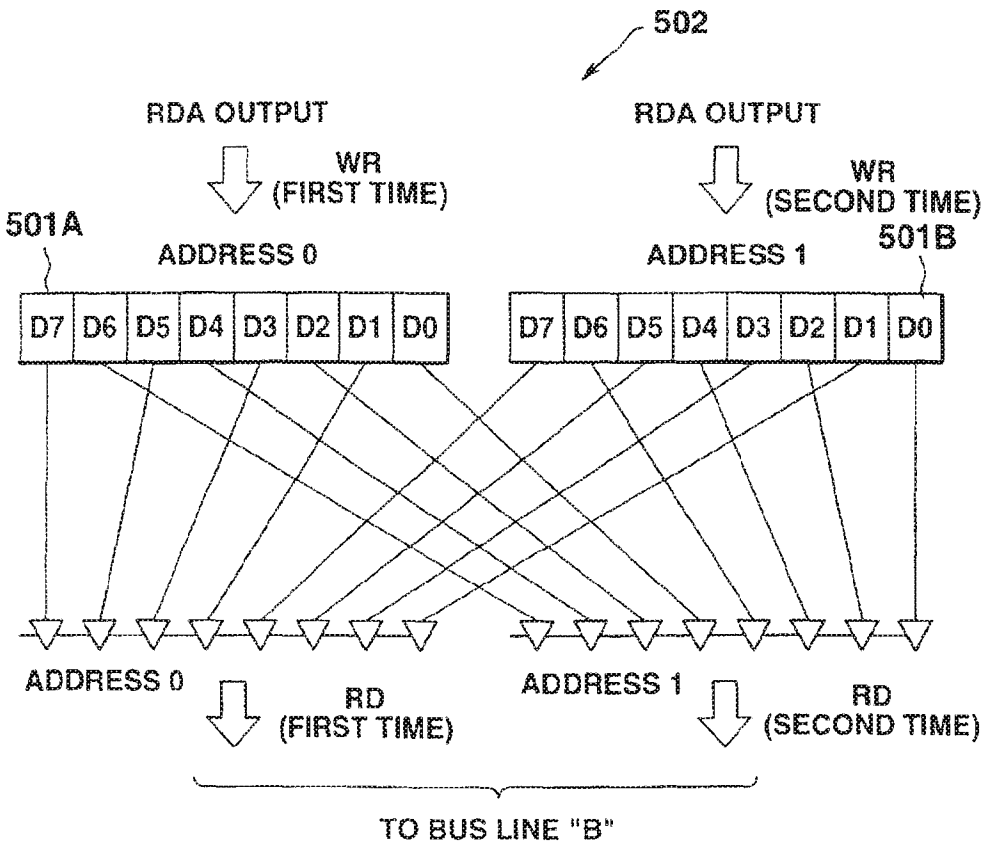

502
RDA OUTPUT
RDA OUTPUT
WR
(FIRST TIME)
WR
(SECOND TIME)
501A
501B
ADDRESS 0
ADDRESS 1
D7 D6 D5 D4 D3 D2 D1 D0
D7 D6 D5 D4 D3 D2 D1 D0
ADDRESS 0
ADDRESS 1
RD
(FIRST TIME)
RD
(SECOND TIME)
TO BUS LINE "B"

FIG.16

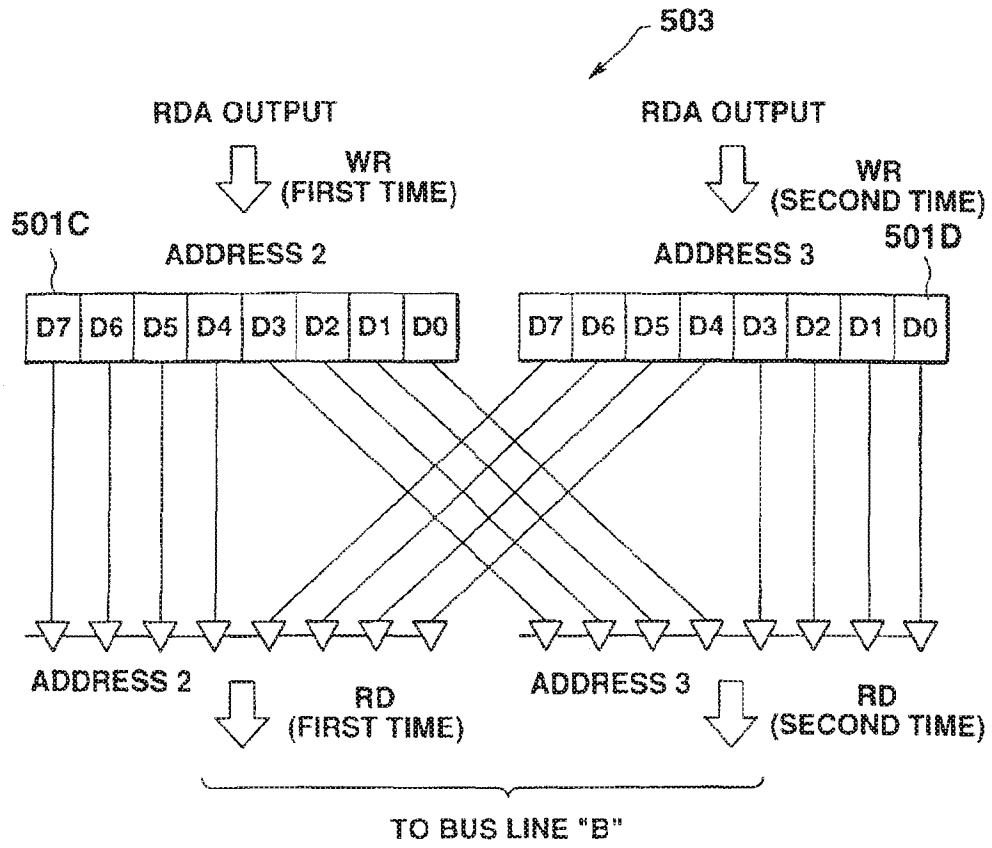

503
RDA OUTPUT
WR
(FIRST TIME)
RDA OUTPUT
WR
(SECOND TIME)
501C
ADDRESS 2
ADDRESS 3
501D
D7 D6 D5 D4 D3 D2 D1 D0
D7 D6 D5 D4 D3 D2 D1 D0
ADDRESS 2
RD
(FIRST TIME)
ADDRESS 3
RD
(SECOND TIME)
TO BUS LINE "B"

FIG.17

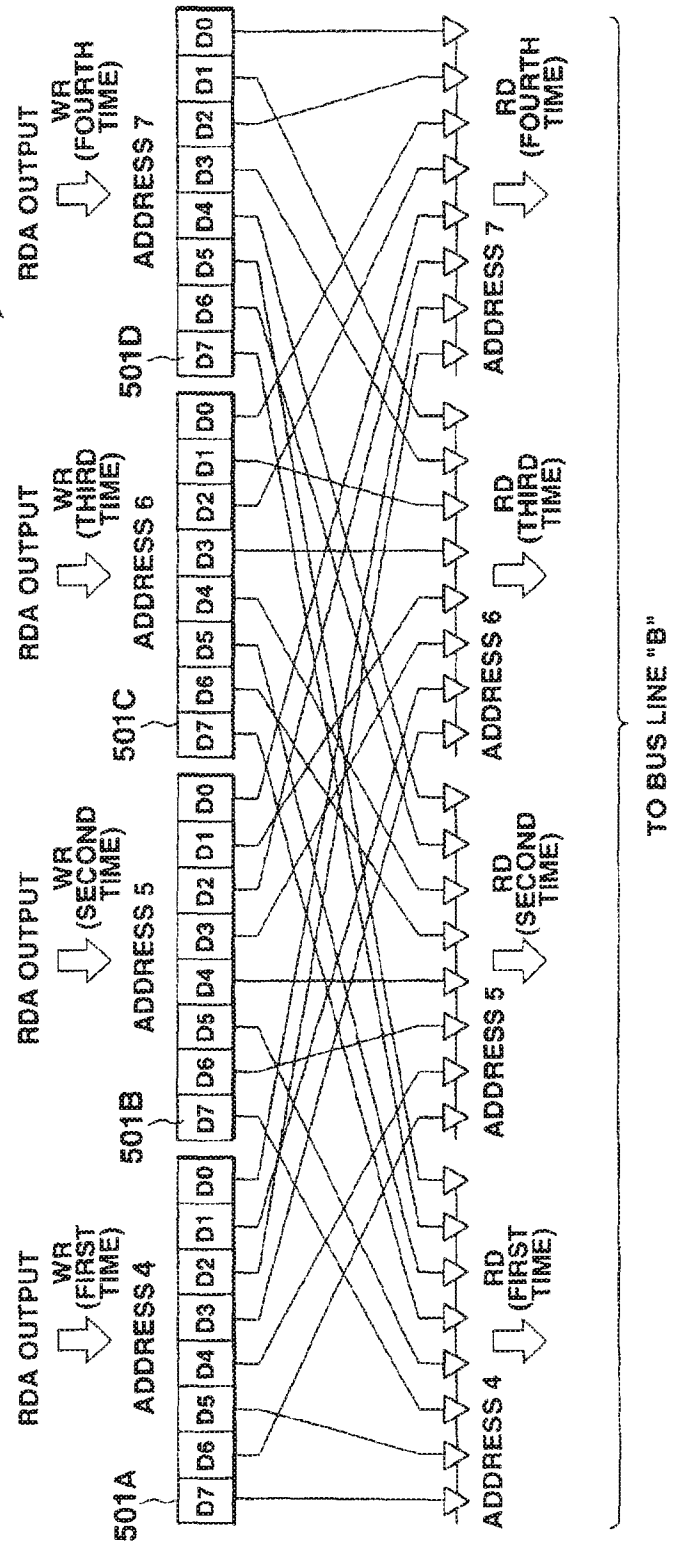

504
RDA OUTPUT
WR (FIRST TIME)
ADDRESS 4
501A
RDA OUTPUT
WR (SECOND TIME)
ADDRESS 5
501B
RDA OUTPUT
WR (THIRD TIME)
ADDRESS 6
501C
RDA OUTPUT
WR (FOURTH TIME)
ADDRESS 7
501D
D7 D6 D5 D4 D3 D2 D1 D0
RD (FIRST TIME)
ADDRESS 4
RD (SECOND TIME)
ADDRESS 5
RD (THIRD TIME)
ADDRESS 6
RD (FOURTH TIME)
ADDRESS 7
TO BUS LINE "B"

FIG.18

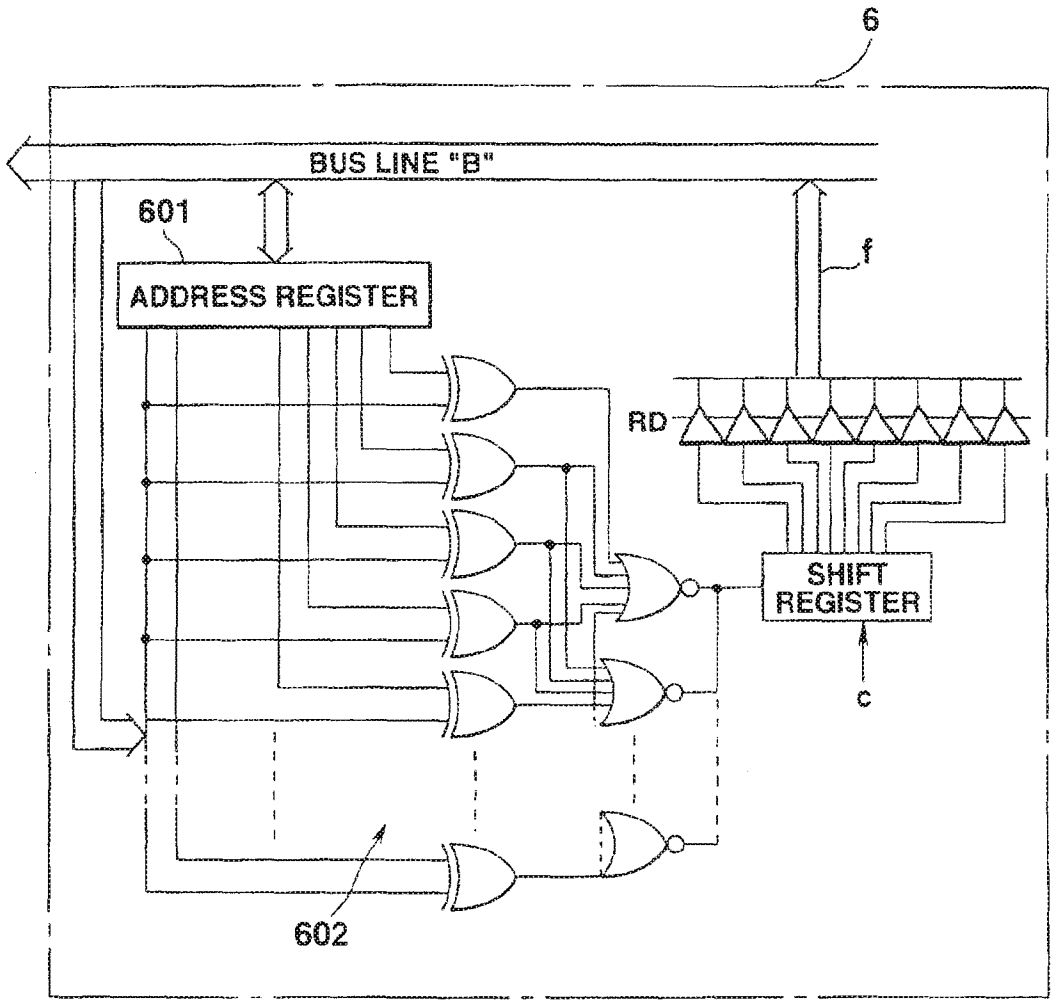


FIG.19A

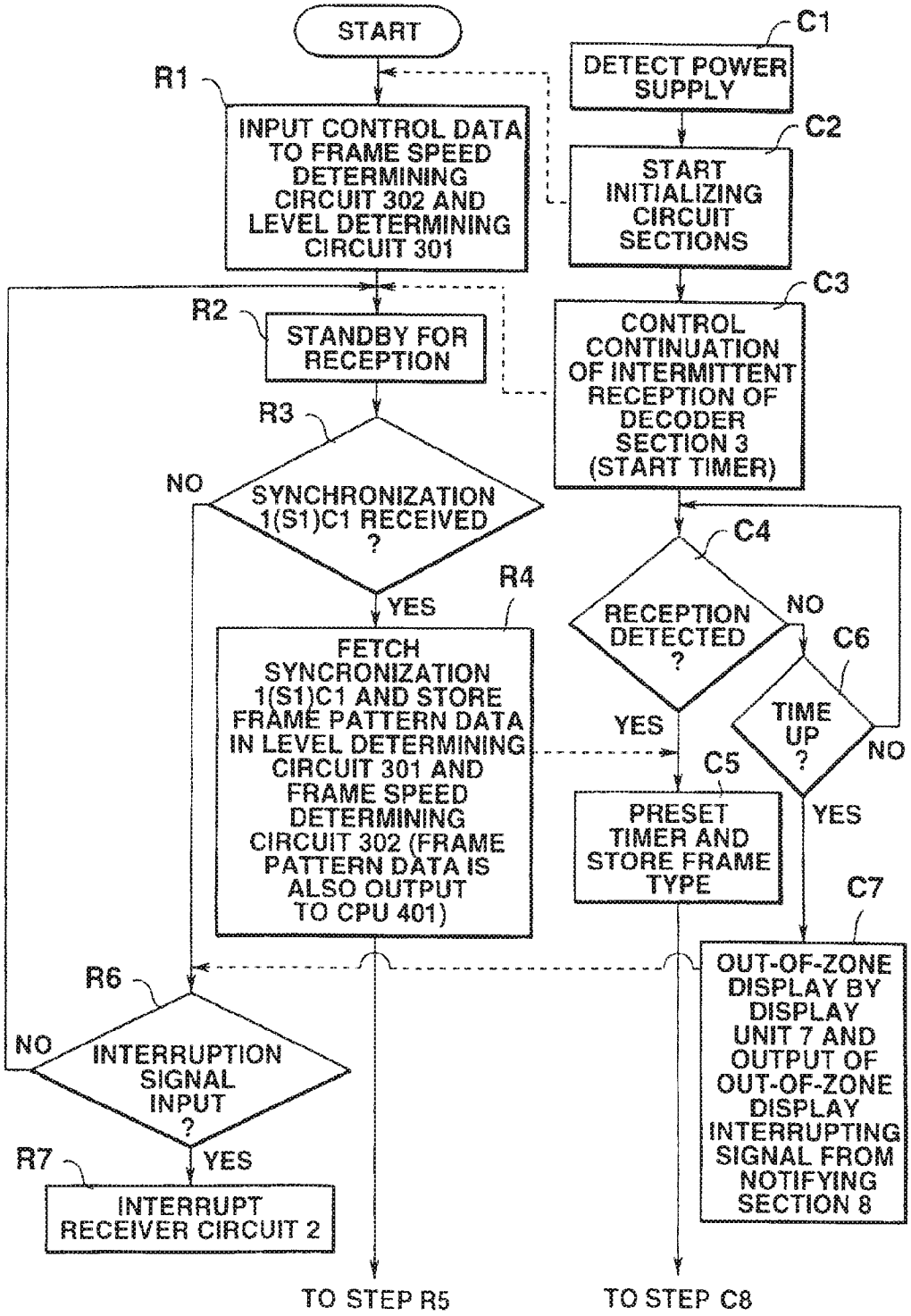

START
C1
DETECT POWER SUPPLY
R1
INPUT CONTROL DATA TO FRAME SPEED DETERMINING CIRCUIT 302 AND LEVEL DETERMINING CIRCUIT 301
C2
START INITIALIZING CIRCUIT SECTIONS
C3
CONTROL CONTINUATION OF INTERMITTENT RECEPTION OF DECODER SECTION 3 (START TIMER)
R2
STANDBY FOR RECEPTION
R3
NO
SYNCHRONIZATION 1(S1)C1 RECEIVED ?
YES
R4
FETCH SYNCRONIZATION 1(S1)C1 AND STORE FRAME PATTERN DATA IN LEVEL DETERMINING CIRCUIT 301 AND FRAME SPEED DETERMINING CIRCUIT 302 (FRAME PATTERN DATA IS ALSO OUTPUT TO CPU 401)
C4
RECEPTION DETECTED ?
NO
C6
TIME UP ?
NO
YES
YES
C5
PRESET TIMER AND STORE FRAME TYPE
C7
OUT-OF-ZONE DISPLAY BY DISPLAY UNIT 7 AND OUTPUT OF OUT-OF-ZONE DISPLAY INTERRUPTING SIGNAL FROM NOTIFYING SECTION 8
R6
NO
INTERRUPTION SIGNAL INPUT ?
YES
R7
INTERRUPT RECEIVER CIRCUIT 2
TO STEP R5
TO STEP C8

FIG.19B

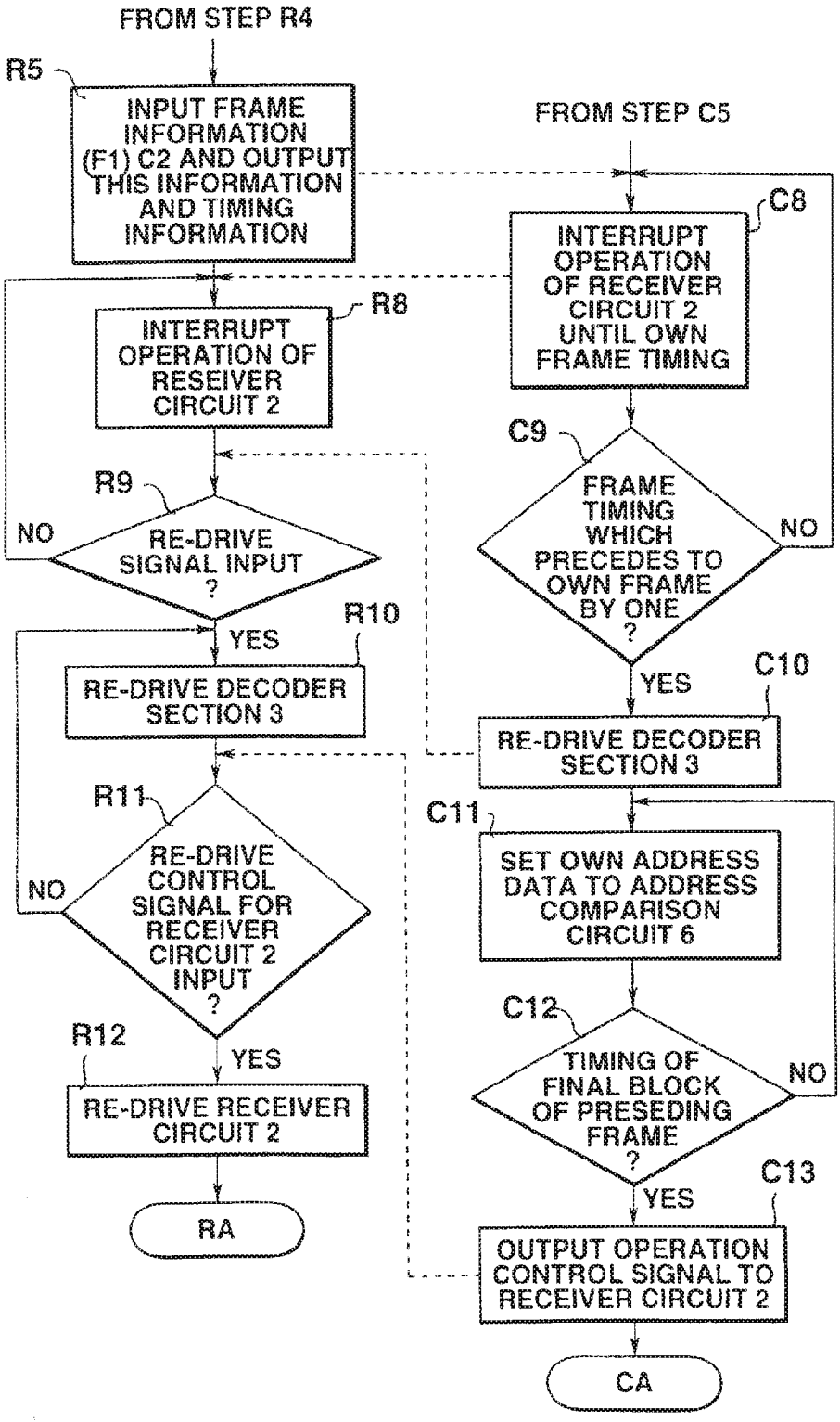

FROM STEP R4
R5
INPUT FRAME INFORMATION (F1) C2 AND OUTPUT THIS INFORMATION AND TIMING INFORMATION
R8
INTERRUPT OPERATION OF RESEIVER CIRCUIT 2
R9
RE-DRIVE SIGNAL INPUT ?
NO
YES
R10
RE-DRIVE DECODER SECTION 3
R11
RE-DRIVE CONTROL SIGNAL FOR RECEIVER CIRCUIT 2 INPUT ?
NO
R12
YES
RE-DRIVE RECEIVER CIRCUIT 2
RA
FROM STEP C5
C8
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2 UNTIL OWN FRAME TIMING
C9
FRAME TIMING WHICH PRECEDES TO OWN FRAME BY ONE ?
NO
YES
C10
RE-DRIVE DECODER SECTION 3
C11
SET OWN ADDRESS DATA TO ADDRESS COMPARISON CIRCUIT 6
C12
TIMING OF FINAL BLOCK OF PRESEDING FRAME ?
NO
YES
C13
OUTPUT OPERATION CONTROL SIGNAL TO RECEIVER CIRCUIT 2
CA

FIG.20

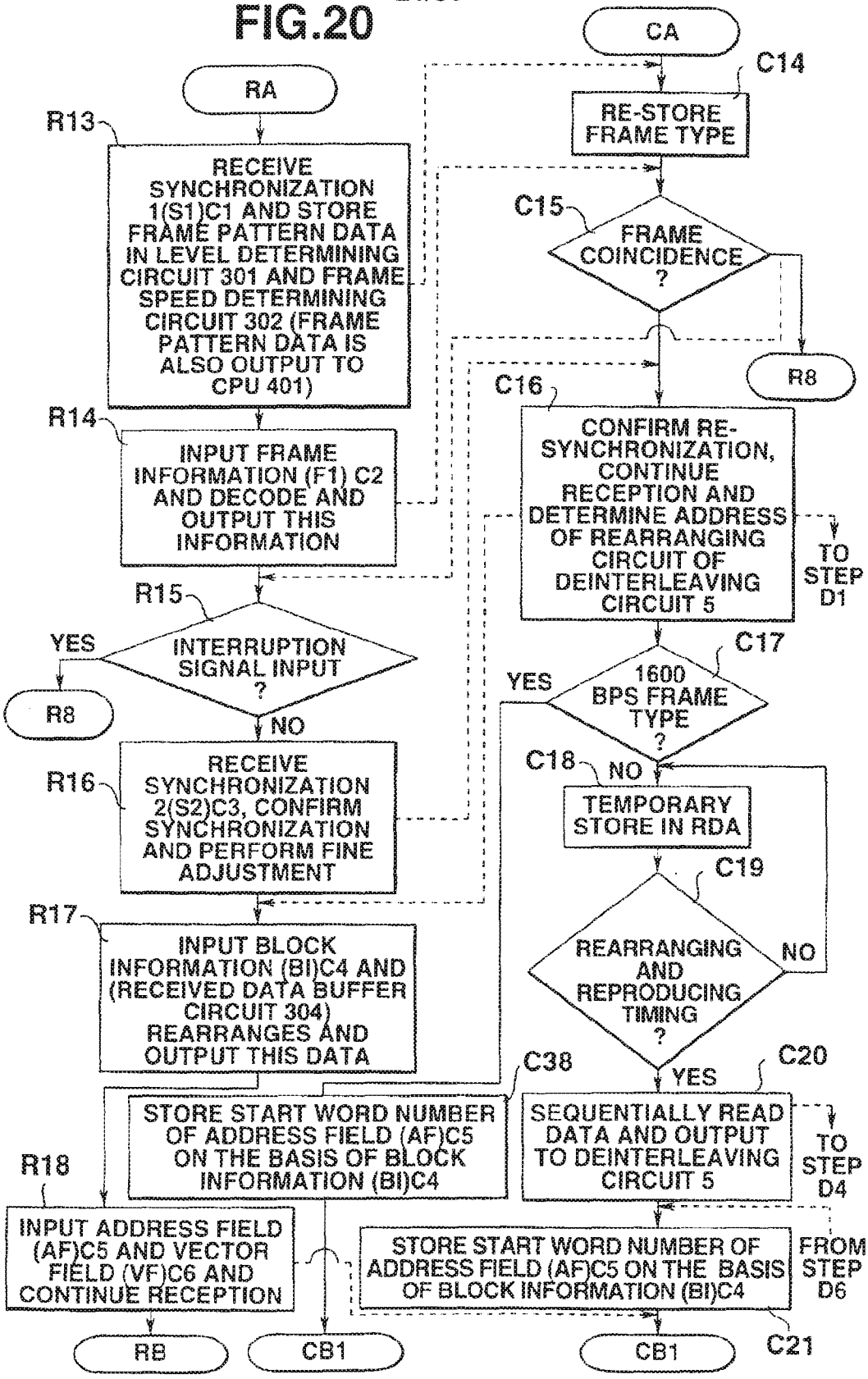

RA
R13
RECEIVE SYNCHRONIZATION 1(S1)C1 AND STORE FRAME PATTERN DATA IN LEVEL DETERMINING CIRCUIT 301 AND FRAME SPEED DETERMINING CIRCUIT 302 (FRAME PATTERN DATA IS ALSO OUTPUT TO CPU 401)
R14
INPUT FRAME INFORMATION (F1) C2 AND DECODE AND OUTPUT THIS INFORMATION
R15
INTERRUPTION SIGNAL INPUT ?
YES
R8
NO
R16
RECEIVE SYNCHRONIZATION 2(S2)C3, CONFIRM SYNCHRONIZATION AND PERFORM FINE ADJUSTMENT
R17
INPUT BLOCK INFORMATION (BI)C4 AND (RECEIVED DATA BUFFER CIRCUIT 304) REARRANGES AND OUTPUT THIS DATA
R18
INPUT ADDRESS FIELD (AF)C5 AND VECTOR FIELD (VF)C6 AND CONTINUE RECEPTION
RB
CB1
CA
C14
RE-STORE FRAME TYPE
C15
FRAME COINCIDENCE ?
R8
C16
CONFIRM RE-SYNCHRONIZATION, CONTINUE RECEPTION AND DETERMINE ADDRESS OF REARRANGING CIRCUIT OF DEINTERLEAVING CIRCUIT 5
TO STEP D1
C17
1600 BPS FRAME TYPE ?
YES
NO
C18
TEMPORARY STORE IN RDA
C19
REARRANGING AND REPRODUCING TIMING ?
NO
YES
C20
SEQUENTIALLY READ DATA AND OUTPUT TO DEINTERLEAVING CIRCUIT 5
TO STEP D4
C38
STORE START WORD NUMBER OF ADDRESS FIELD (AF)C5 ON THE BASIS OF BLOCK INFORMATION (BI)C4
STORE START WORD NUMBER OF ADDRESS FIELD (AF)C5 ON THE BASIS OF BLOCK INFORMATION (BI)C4
FROM STEP D6
CB1
C21

FIG.21A

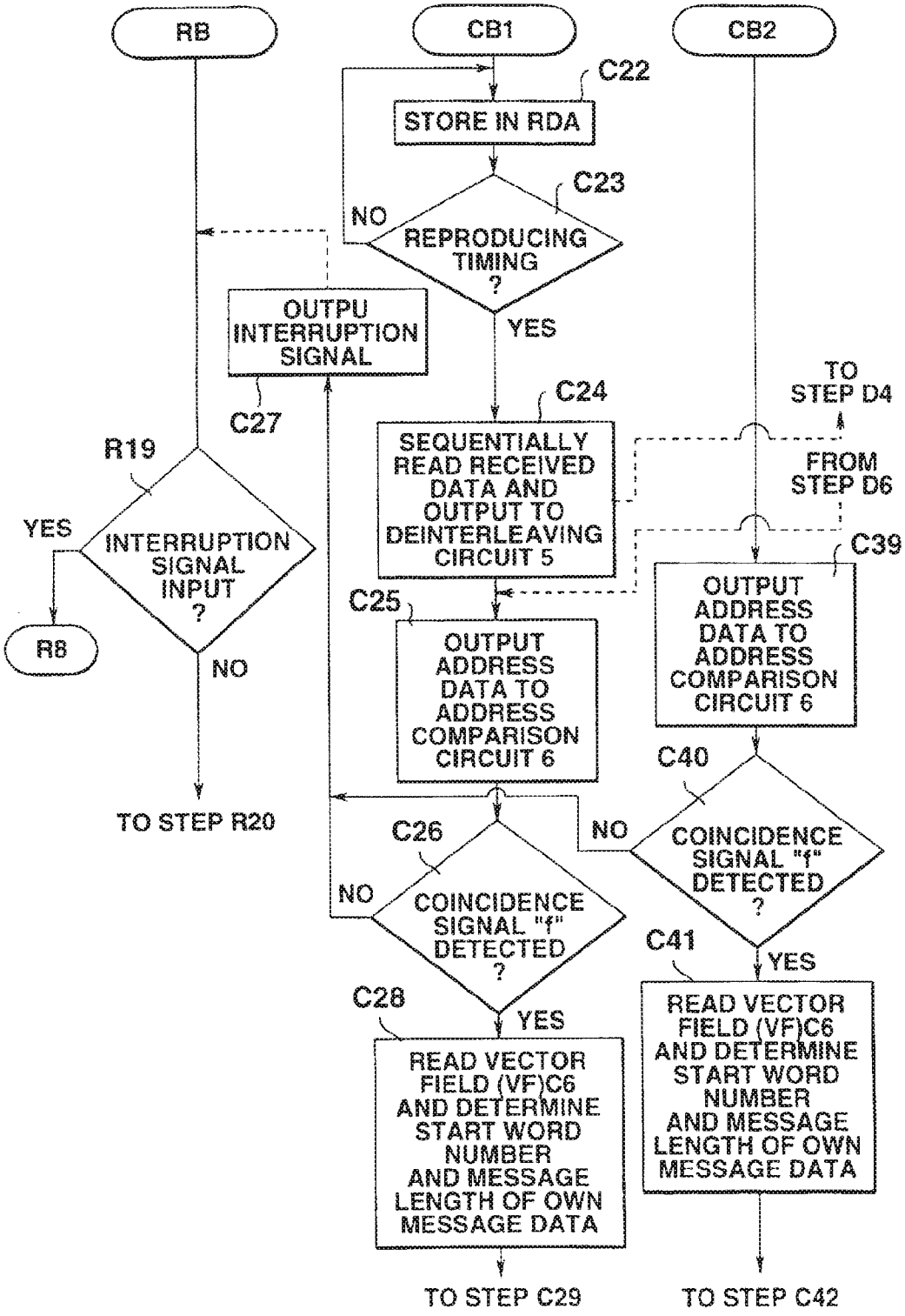

RB
CB1
CB2
C22
STORE IN RDA
C23
NO
REPRODUCING TIMING ?
YES
OUTPU INTERRUPTION SIGNAL
C27
C24
SEQUENTIALLY READ RECEIVED DATA AND OUTPUT TO DEINTERLEAVING CIRCUIT 5
TO STEP D4
FROM STEP D6
R19
YES
INTERRUPTION SIGNAL INPUT ?
R8
NO
TO STEP R20
C25
OUTPUT ADDRESS DATA TO ADDRESS COMPARISON CIRCUIT 6
C39
OUTPUT ADDRESS DATA TO ADDRESS COMPARISON CIRCUIT 6
C40
NO
COINCIDENCE SIGNAL "f" DETECTED ?
C26
NO
COINCIDENCE SIGNAL "f" DETECTED ?
C41
YES
C28
YES
READ VECTOR FIELD (VF)C6 AND DETERMINE START WORD NUMBER AND MESSAGE LENGTH OF OWN MESSAGE DATA
READ VECTOR FIELD (VF)C6 AND DETERMINE START WORD NUMBER AND MESSAGE LENGTH OF OWN MESSAGE DATA
TO STEP C29
TO STEP C42

FIG.21B

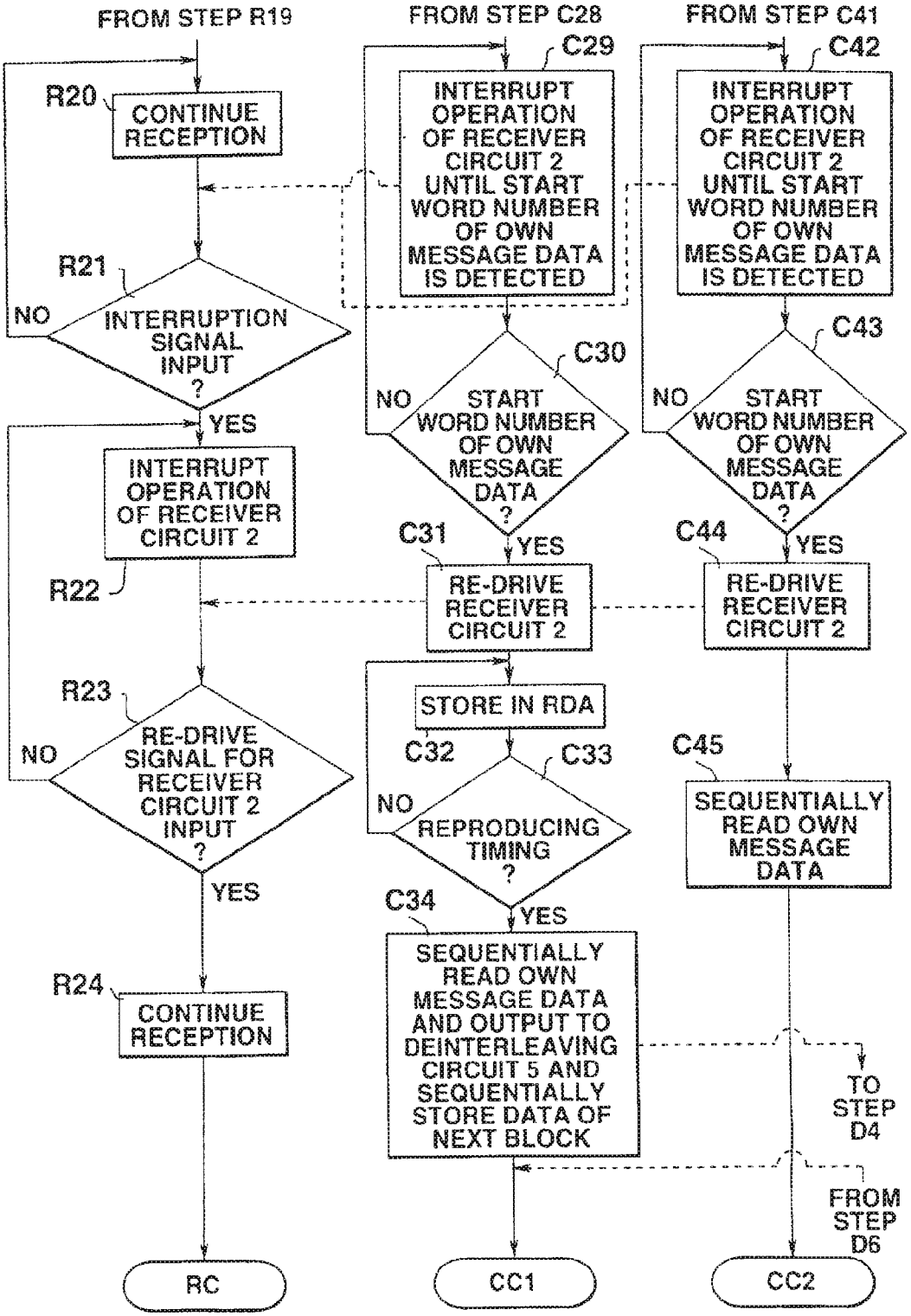

FROM STEP R19
FROM STEP C28
FROM STEP C41
R20
CONTINUE RECEPTION
C29
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2 UNTIL START WORD NUMBER OF OWN MESSAGE DATA IS DETECTED
C42
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2 UNTIL START WORD NUMBER OF OWN MESSAGE DATA IS DETECTED
R21
NO
INTERRUPTION SIGNAL INPUT ?
YES
C30
NO
START WORD NUMBER OF OWN MESSAGE DATA ?
C43
NO
START WORD NUMBER OF OWN MESSAGE DATA ?
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2
R22
C31
YES
RE-DRIVE RECEIVER CIRCUIT 2
C44
YES
RE-DRIVE RECEIVER CIRCUIT 2
R23
NO
RE-DRIVE SIGNAL FOR RECEIVER CIRCUIT 2 INPUT ?
STORE IN RDA
C32
C33
NO
REPRODUCING TIMING ?
C45
SEQUENTIALLY READ OWN MESSAGE DATA
YES
C34
YES
SEQUENTIALLY READ OWN MESSAGE DATA AND OUTPUT TO DEINTERLEAVING CIRCUIT 5 AND SEQUENTIALLY STORE DATA OF NEXT BLOCK
R24
CONTINUE RECEPTION
TO STEP D4
FROM STEP D6
RC
CC1
CC2

FIG.22

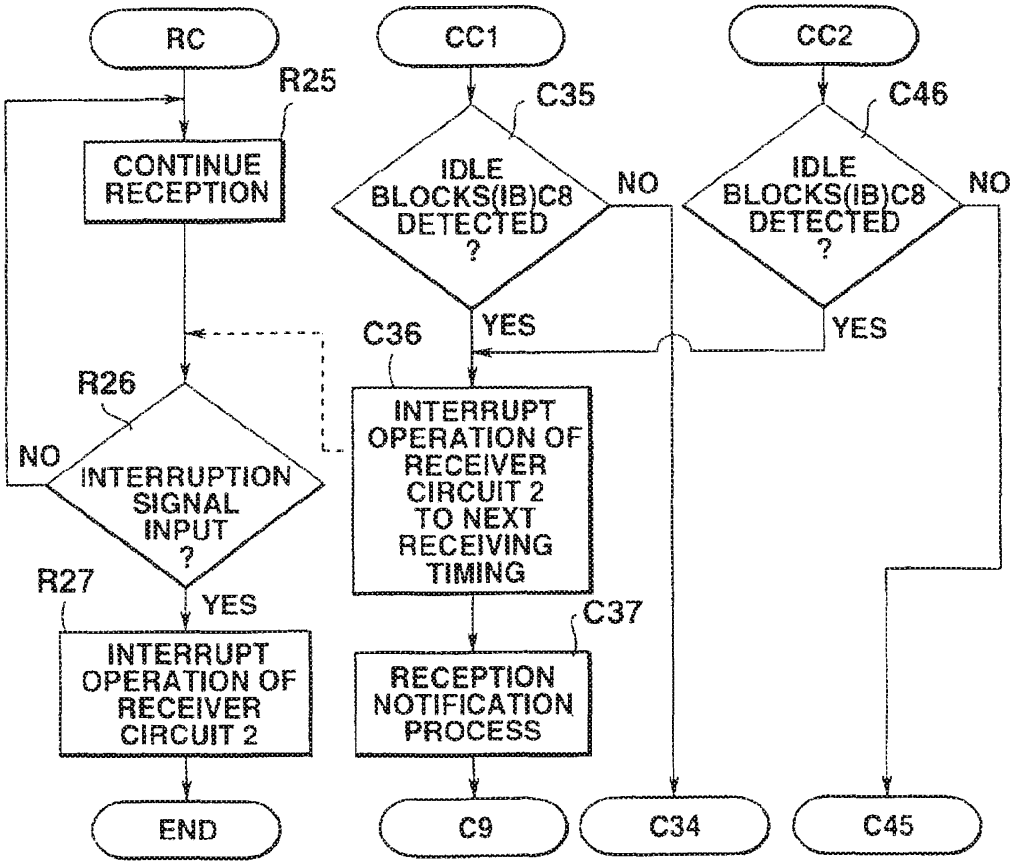

RC
R25
CONTINUE RECEPTION
R26
NO
INTERRUPTION SIGNAL INPUT ?
R27
YES
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2
END
CC1
C35
IDLE BLOCKS(IB)C8 DETECTED ?
NO
YES
C36
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2 TO NEXT RECEIVING TIMING
C37
RECEPTION NOTIFICATION PROCESS
C9
C34
CC2
C46
IDLE BLOCKS(IB)C8 DETECTED ?
NO
YES
C45

FIG.23

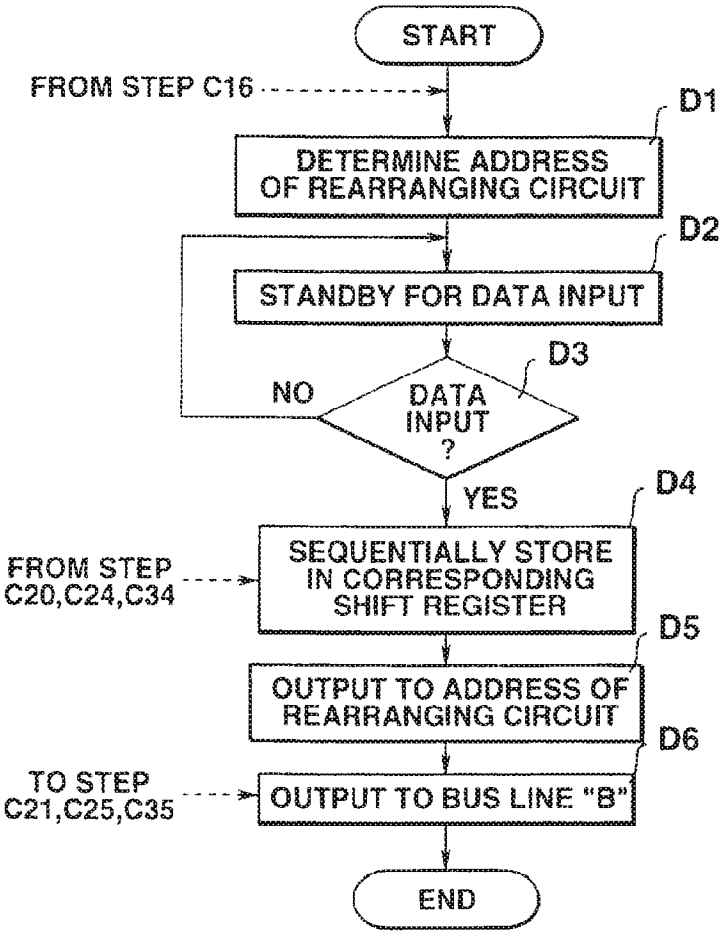

START
FROM STEP C16
D1
DETERMINE ADDRESS OF REARRANGING CIRCUIT
D2
STANDBY FOR DATA INPUT
D3
NO
DATA INPUT ?
YES
D4
FROM STEP C20,C24,C34
SEQUENTIALLY STORE IN CORRESPONDING SHIFT REGISTER
D5
OUTPUT TO ADDRESS OF REARRANGING CIRCUIT
D6
TO STEP C21,C25,C35
OUTPUT TO BUS LINE "B"
END

FIG.24

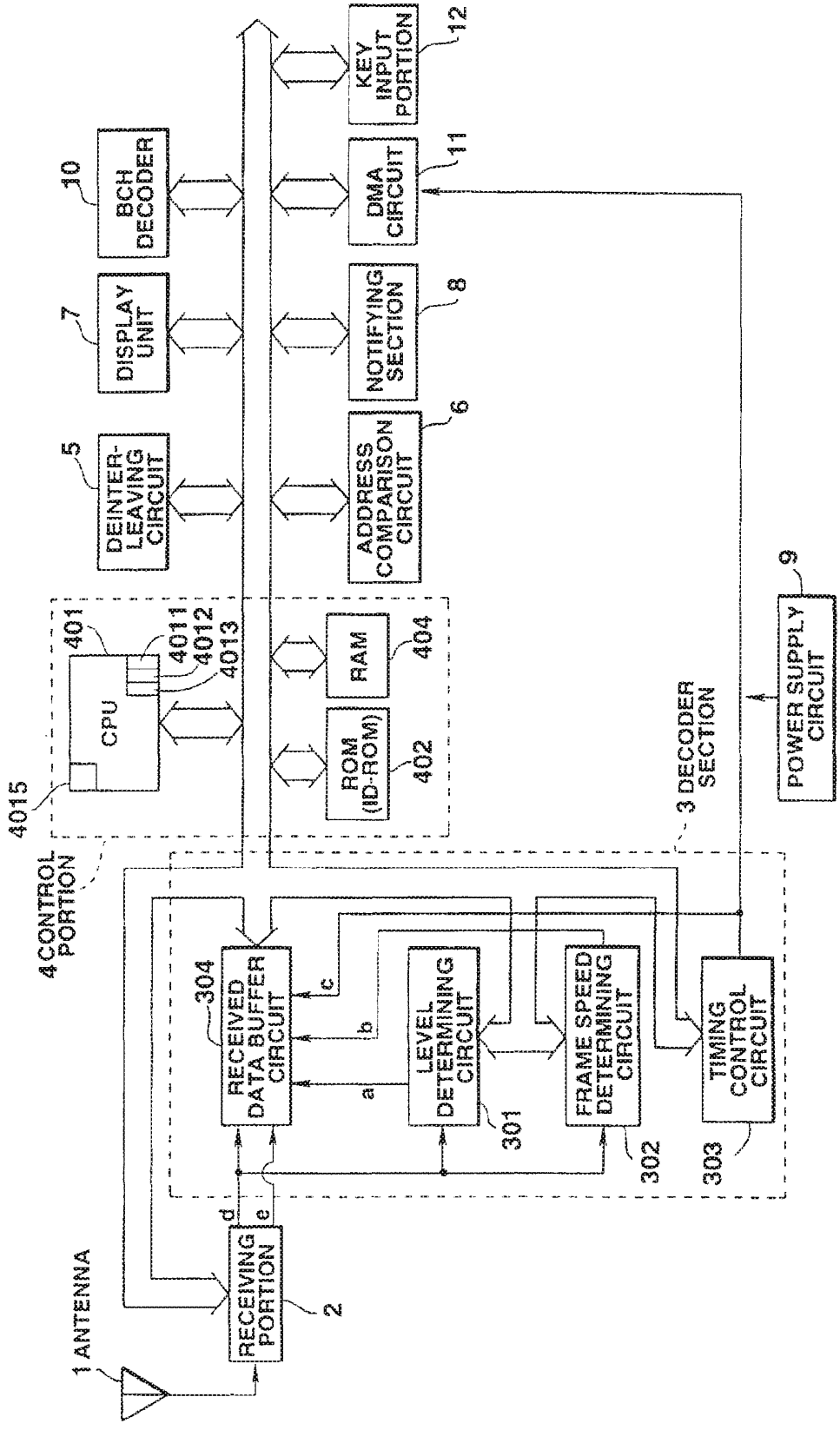

1 ANTENNA
RECEIVING PORTION
2
4 CONTROL PORTION
3 DECODER SECTION
CPU
401
4011
4012
4013
4015
ROM (ID-ROM)
402
RAM
404
DEINTER-LEAVING CIRCUIT
5
ADDRESS COMPARISON CIRCUIT
6
DISPLAY UNIT
7
NOTIFYING SECTION
8
POWER SUPPLY CIRCUIT
9
BCH DECODER
10
DMA CIRCUIT
11
KEY INPUT PORTION
12
RECEIVED DATA BUFFER CIRCUIT
304
LEVEL DETERMINING CIRCUIT
301
FRAME SPEED DETERMINING CIRCUIT
302
TIMING CONTROL CIRCUIT
303
a
b
c
d
e

FIG.25

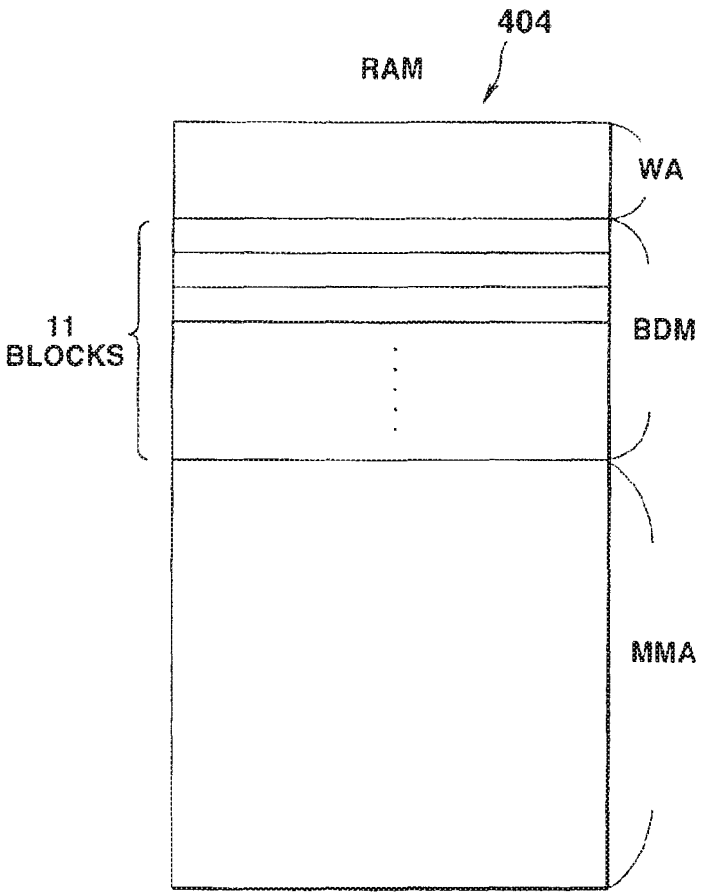


FIG.26A

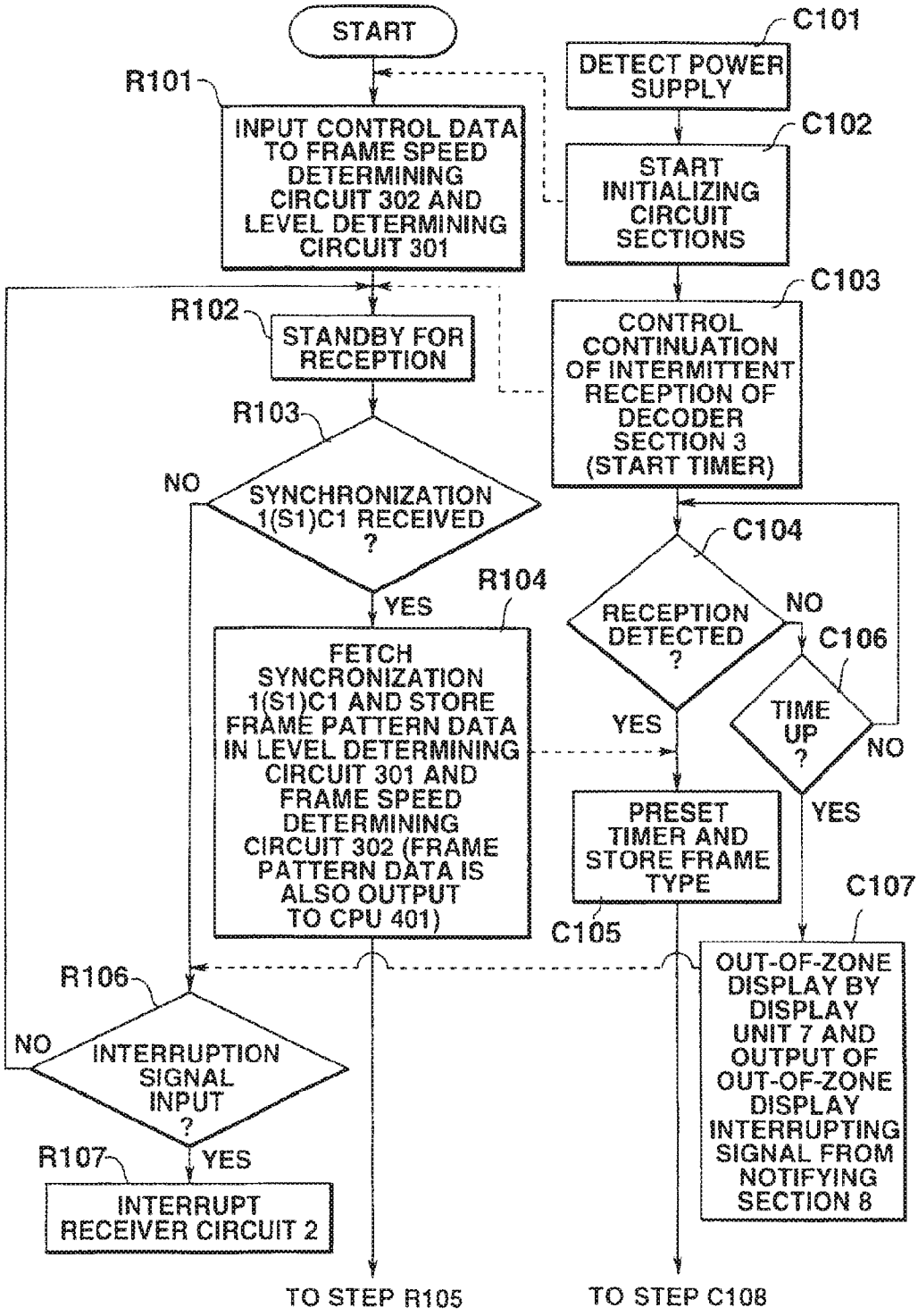

START
C101
DETECT POWER SUPPLY
R101
INPUT CONTROL DATA TO FRAME SPEED DETERMINING CIRCUIT 302 AND LEVEL DETERMINING CIRCUIT 301
C102
START INITIALIZING CIRCUIT SECTIONS
C103
CONTROL CONTINUATION OF INTERMITTENT RECEPTION OF DECODER SECTION 3 (START TIMER)
R102
STANDBY FOR RECEPTION
R103
NO
SYNCHRONIZATION 1(S1)C1 RECEIVED ?
YES
R104
FETCH SYNCRONIZATION 1(S1)C1 AND STORE FRAME PATTERN DATA IN LEVEL DETERMINING CIRCUIT 301 AND FRAME SPEED DETERMINING CIRCUIT 302 (FRAME PATTERN DATA IS ALSO OUTPUT TO CPU 401)
C104
RECEPTION DETECTED ?
NO
C106
TIME UP ?
NO
YES
YES
PRESET TIMER AND STORE FRAME TYPE
C105
C107
OUT-OF-ZONE DISPLAY BY DISPLAY UNIT 7 AND OUTPUT OF OUT-OF-ZONE DISPLAY INTERRUPTING SIGNAL FROM NOTIFYING SECTION 8
R106
NO
INTERRUPTION SIGNAL INPUT ?
R107
YES
INTERRUPT RECEIVER CIRCUIT 2
TO STEP R105
TO STEP C108

FIG.26B

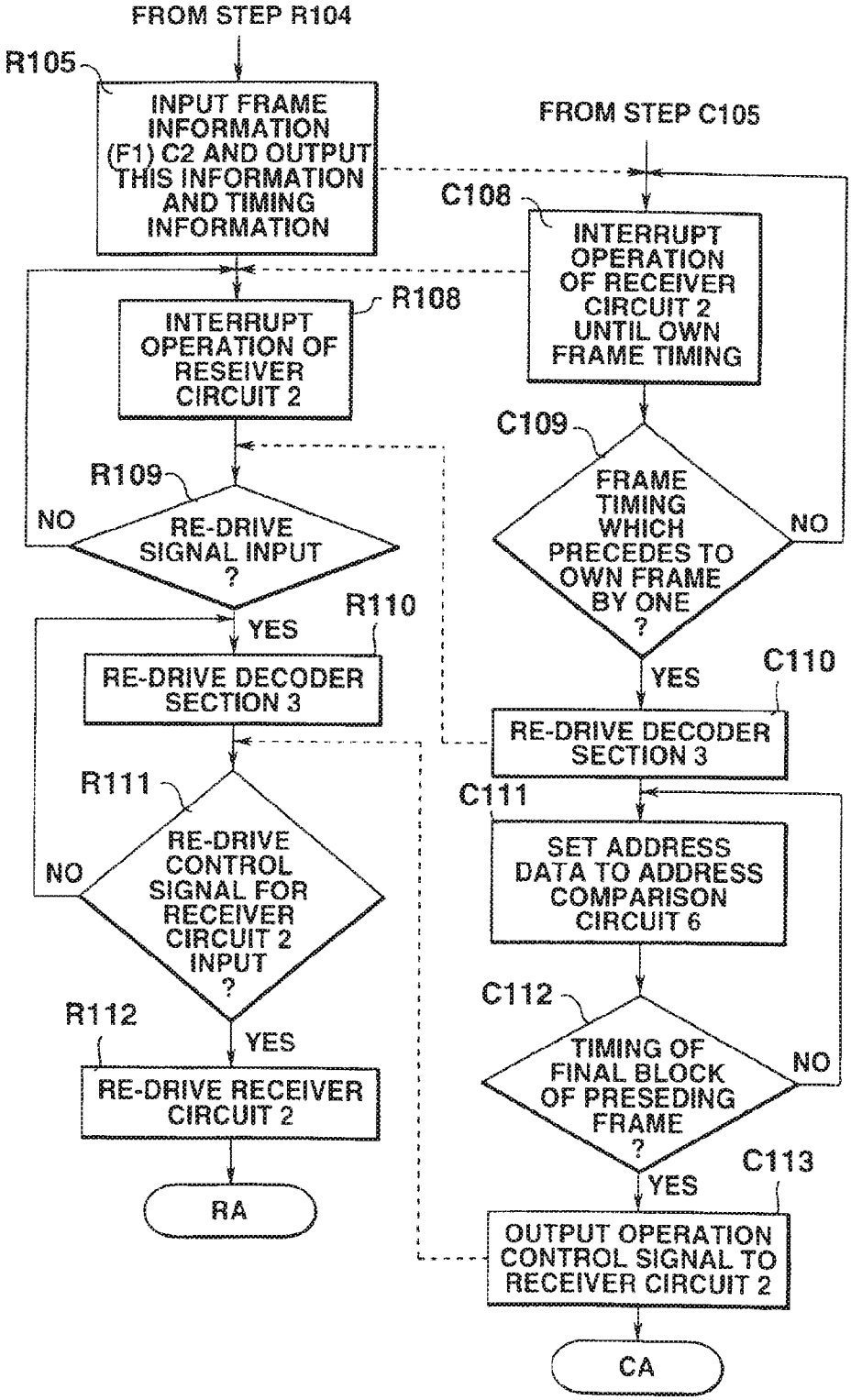

FROM STEP R104
R105
INPUT FRAME INFORMATION (F1) C2 AND OUTPUT THIS INFORMATION AND TIMING INFORMATION
R108
INTERRUPT OPERATION OF RESEIVER CIRCUIT 2
R109
RE-DRIVE SIGNAL INPUT ?
NO
YES
R110
RE-DRIVE DECODER SECTION 3
R111
RE-DRIVE CONTROL SIGNAL FOR RECEIVER CIRCUIT 2 INPUT ?
NO
R112
YES
RE-DRIVE RECEIVER CIRCUIT 2
RA
FROM STEP C105
C108
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2 UNTIL OWN FRAME TIMING
C109
FRAME TIMING WHICH PRECEDES TO OWN FRAME BY ONE ?
NO
YES
C110
RE-DRIVE DECODER SECTION 3
C111
SET ADDRESS DATA TO ADDRESS COMPARISON CIRCUIT 6
C112
TIMING OF FINAL BLOCK OF PRESEDING FRAME ?
NO
YES
C113
OUTPUT OPERATION CONTROL SIGNAL TO RECEIVER CIRCUIT 2
CA

FIG.27

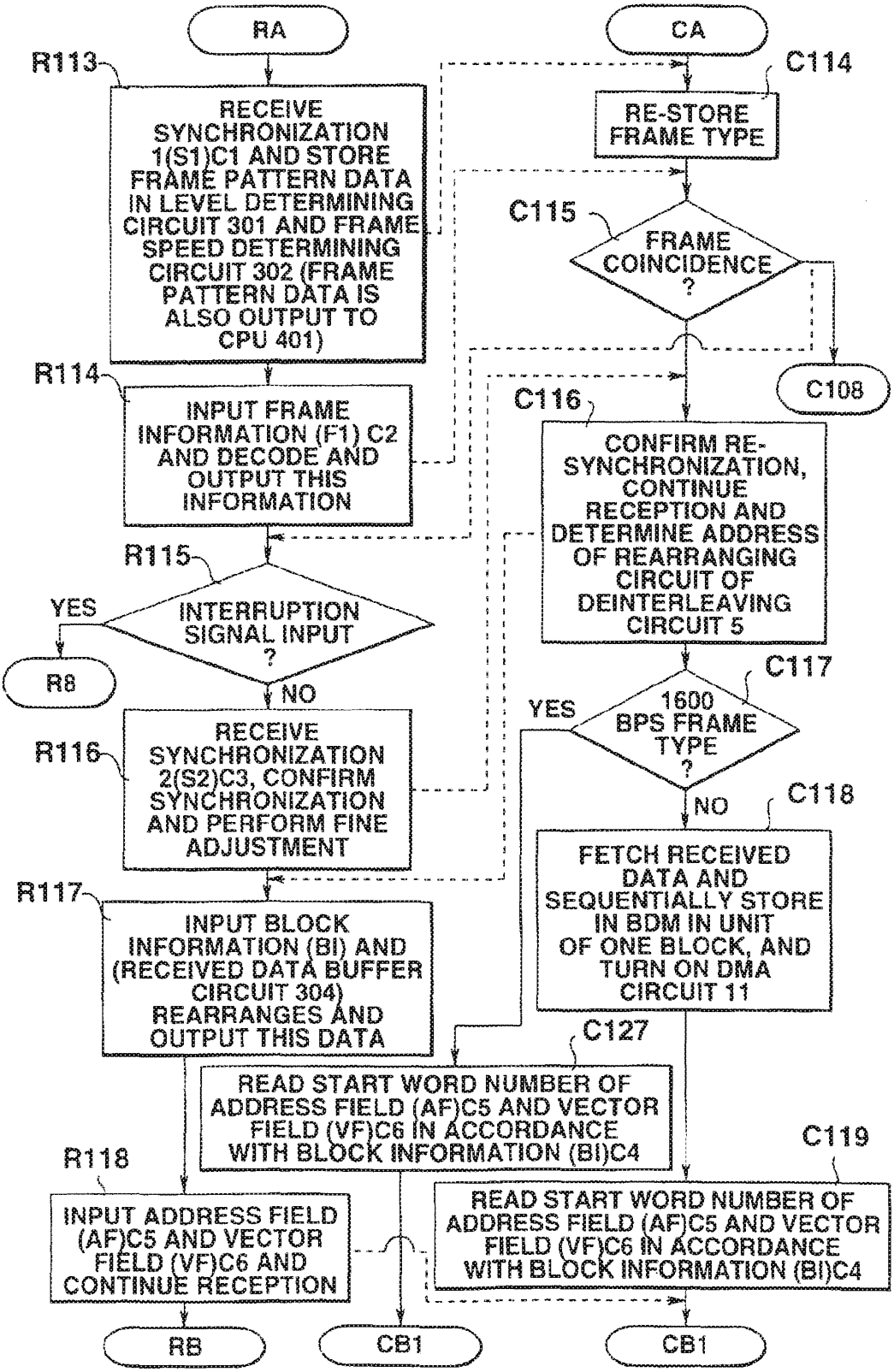

RA
CA
R113
RECEIVE SYNCHRONIZATION 1(S1)C1 AND STORE FRAME PATTERN DATA IN LEVEL DETERMINING CIRCUIT 301 AND FRAME SPEED DETERMINING CIRCUIT 302 (FRAME PATTERN DATA IS ALSO OUTPUT TO CPU 401)
C114
RE-STORE FRAME TYPE
C115
FRAME COINCIDENCE ?
C108
R114
INPUT FRAME INFORMATION (F1) C2 AND DECODE AND OUTPUT THIS INFORMATION
C116
CONFIRM RE-SYNCHRONIZATION, CONTINUE RECEPTION AND DETERMINE ADDRESS OF REARRANGING CIRCUIT OF DEINTERLEAVING CIRCUIT 5
R115
YES
INTERRUPTION SIGNAL INPUT ?
R8
NO
C117
YES
1600 BPS FRAME TYPE ?
R116
RECEIVE SYNCHRONIZATION 2(S2)C3, CONFIRM SYNCHRONIZATION AND PERFORM FINE ADJUSTMENT
NO
C118
FETCH RECEIVED DATA AND SEQUENTIALLY STORE IN BDM IN UNIT OF ONE BLOCK, AND TURN ON DMA CIRCUIT 11
R117
INPUT BLOCK INFORMATION (BI) AND (RECEIVED DATA BUFFER CIRCUIT 304) REARRANGES AND OUTPUT THIS DATA
C127
READ START WORD NUMBER OF ADDRESS FIELD (AF)C5 AND VECTOR FIELD (VF)C6 IN ACCORDANCE WITH BLOCK INFORMATION (BI)C4
C119
R118
INPUT ADDRESS FIELD (AF)C5 AND VECTOR FIELD (VF)C6 AND CONTINUE RECEPTION
READ START WORD NUMBER OF ADDRESS FIELD (AF)C5 AND VECTOR FIELD (VF)C6 IN ACCORDANCE WITH BLOCK INFORMATION (BI)C4
RB
CB1
CB1

FIG.28

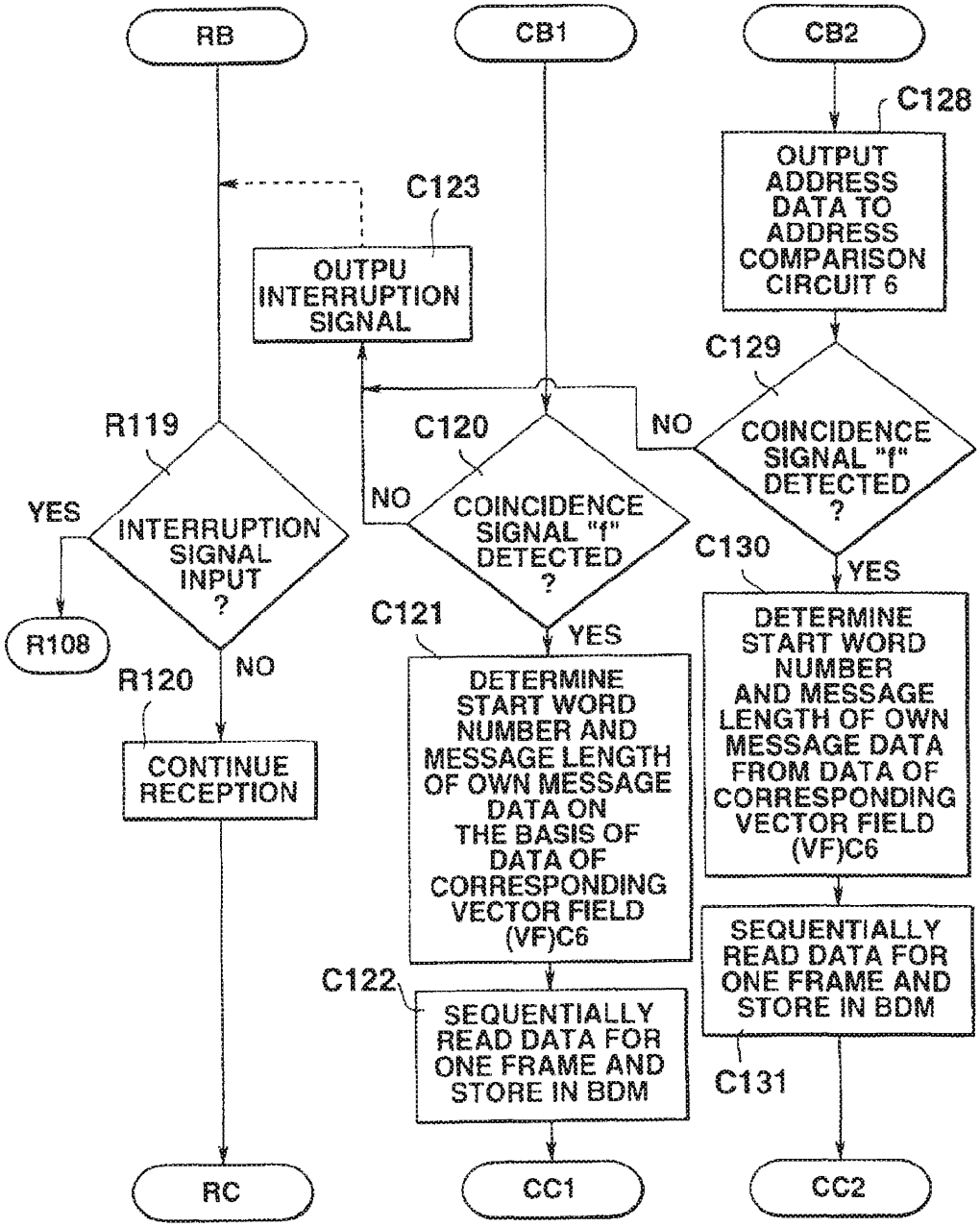

RB
CB1
CB2
C128
OUTPUT ADDRESS DATA TO ADDRESS COMPARISON CIRCUIT 6
C123
OUTPU INTERRUPTION SIGNAL
C129
COINCIDENCE SIGNAL "f" DETECTED ?
NO
YES
R119
INTERRUPTION SIGNAL INPUT ?
C120
COINCIDENCE SIGNAL "f" DETECTED ?
NO
C130
YES
YES
R108
C121
DETERMINE START WORD NUMBER AND MESSAGE LENGTH OF OWN MESSAGE DATA ON THE BASIS OF DATA OF CORRESPONDING VECTOR FIELD (VF)C6
DETERMINE START WORD NUMBER AND MESSAGE LENGTH OF OWN MESSAGE DATA FROM DATA OF CORRESPONDING VECTOR FIELD (VF)C6
NO
R120
CONTINUE RECEPTION
C122
SEQUENTIALLY READ DATA FOR ONE FRAME AND STORE IN BDM
SEQUENTIALLY READ DATA FOR ONE FRAME AND STORE IN BDM
C131
RC
CC1
CC2

FIG.29

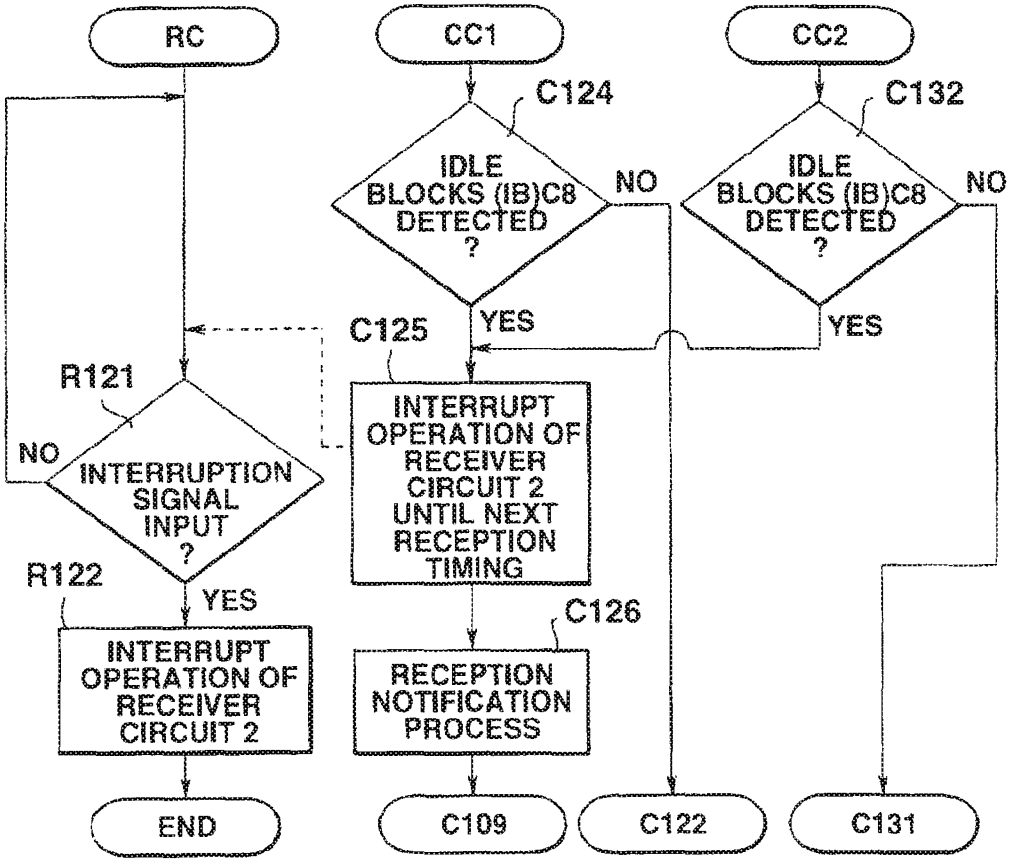

RC
CC1
CC2
C124
C132
IDLE BLOCKS (IB)C8 DETECTED ?
NO
YES
C125
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2 UNTIL NEXT RECEPTION TIMING
R121
INTERRUPTION SIGNAL INPUT ?
R122
INTERRUPT OPERATION OF RECEIVER CIRCUIT 2
C126
RECEPTION NOTIFICATION PROCESS
END
C109
C122
C131

FIG.30

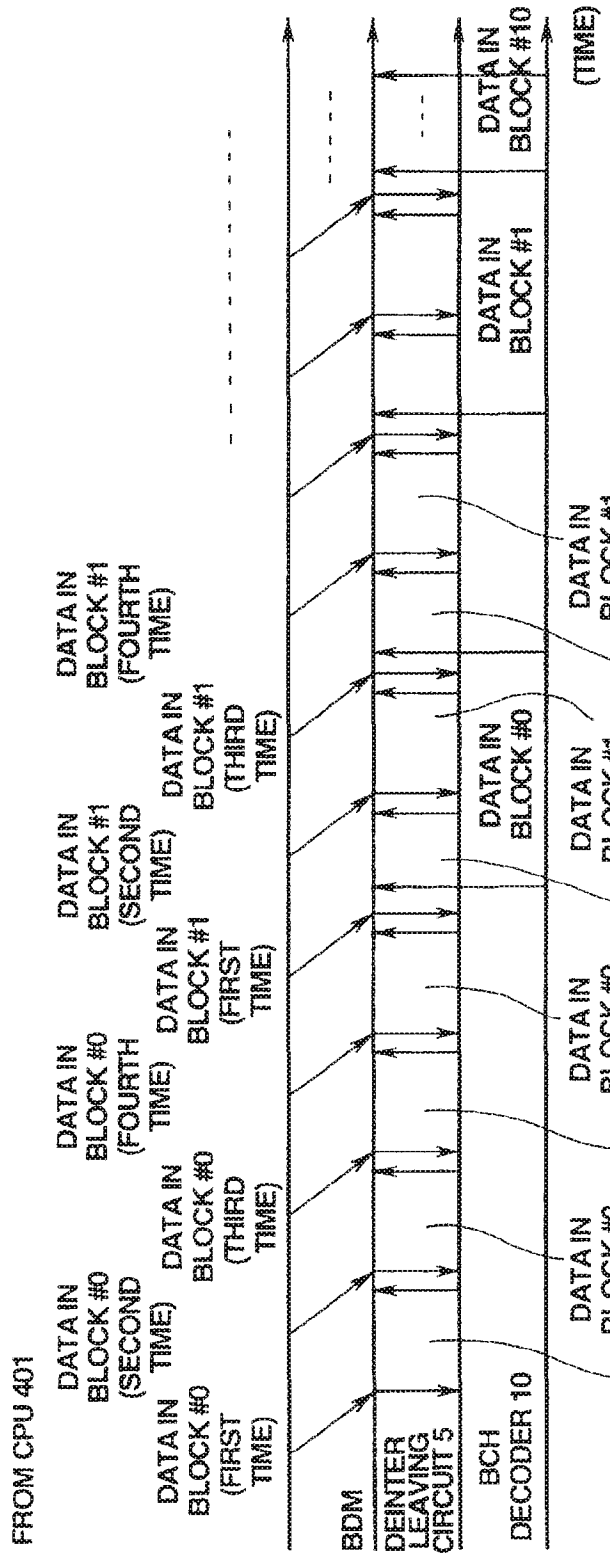

FROM CPU 401
BDM
DEINTER LEAVING CIRCUIT 5
BCH DECODER 10
DATA IN BLOCK #0 (FIRST TIME)
DATA IN BLOCK #0 (SECOND TIME)
DATA IN BLOCK #0 (THIRD TIME)
DATA IN BLOCK #0 (FOURTH TIME)
DATA IN BLOCK #1 (FIRST TIME)
DATA IN BLOCK #1 (SECOND TIME)
DATA IN BLOCK #1 (THIRD TIME)
DATA IN BLOCK #1 (FOURTH TIME)
DATA IN BLOCK #1
DATA IN BLOCK #10
(TIME)

FIG.31

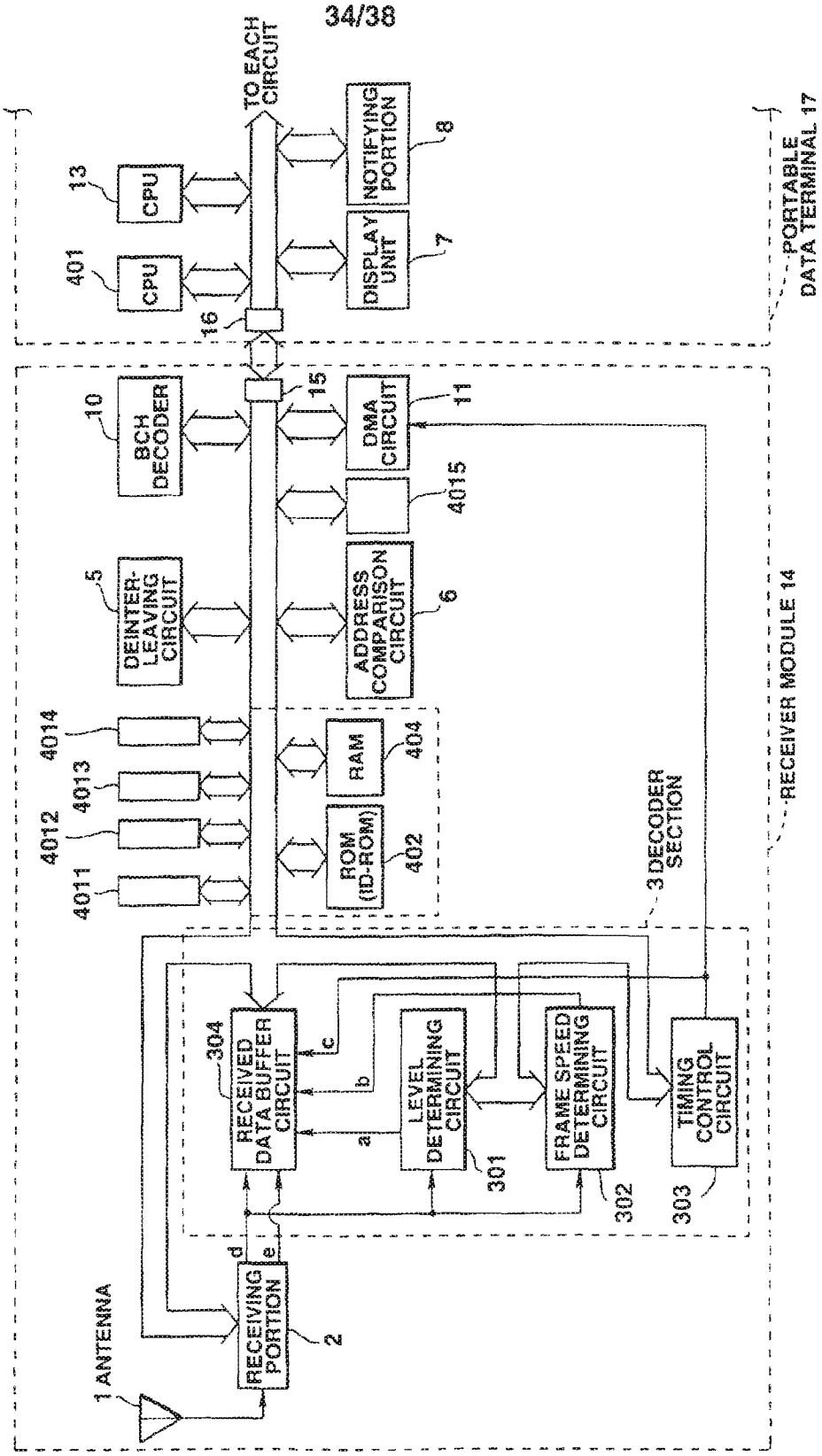

TO EACH CIRCUIT
CPU
CPU
NOTIFYING PORTION
DISPLAY UNIT
PORTABLE DATA TERMINAL 17
BCH DECODER
DMA CIRCUIT
DEINTER-LEAVING CIRCUIT
ADDRESS COMPARISON CIRCUIT
RAM
ROM (ID-ROM)
RECEIVER MODULE 14
DECODER SECTION
RECEIVED DATA BUFFER CIRCUIT
LEVEL DETERMINING CIRCUIT
FRAME SPEED DETERMINING CIRCUIT
TIMING CONTROL CIRCUIT
RECEIVING PORTION
ANTENNA

FIG.32

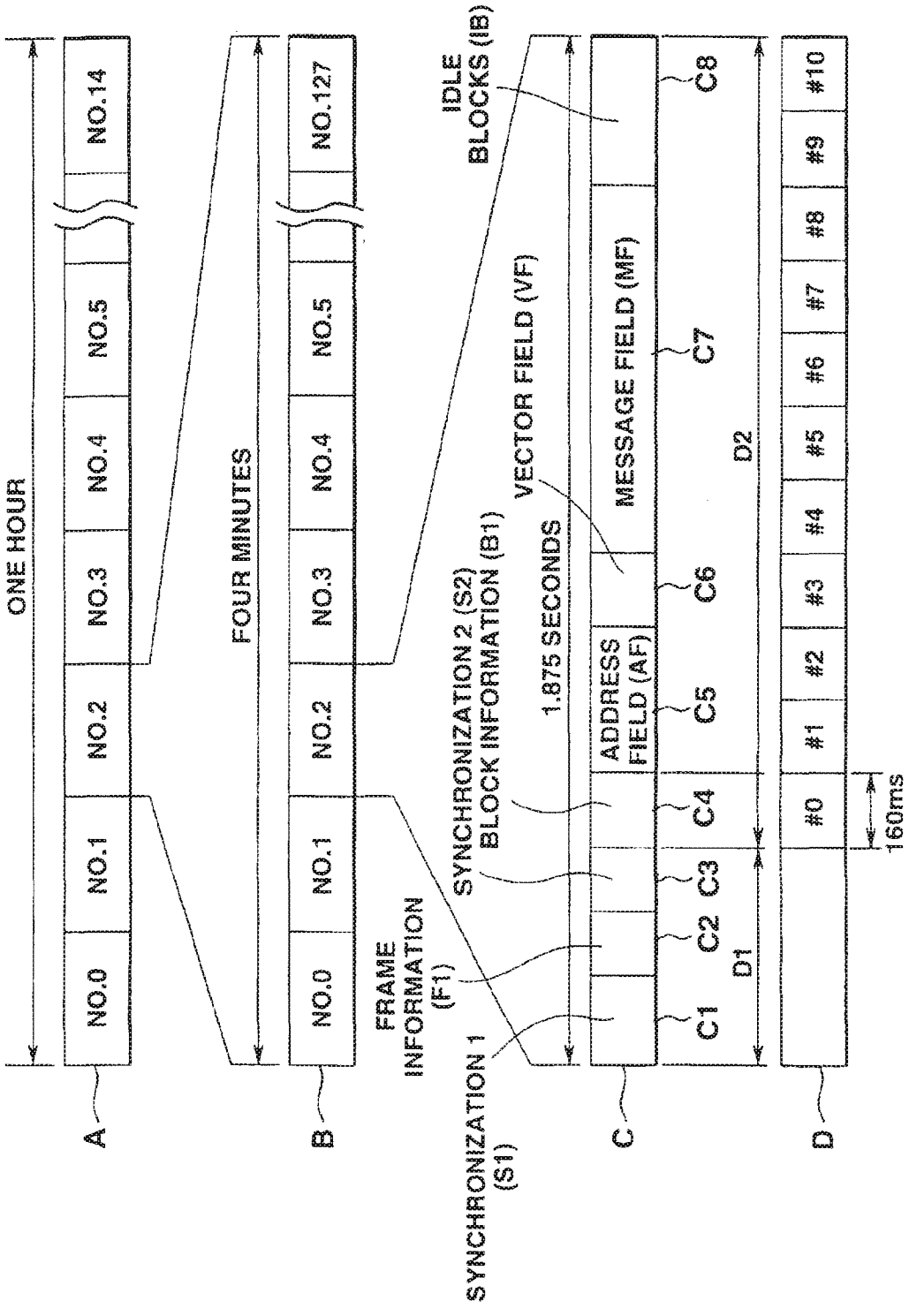

ONE HOUR
FOUR MINUTES
NO.0
NO.1
NO.2
NO.3
NO.4
NO.5
NO.14
NO.127
A
B
C
D
FRAME INFORMATION (F1)
SYNCHRONIZATION 1 (S1)
SYNCHRONIZATION 2 (S2) BLOCK INFORMATION (B1)
1.875 SECONDS
VECTOR FIELD (VF)
IDLE BLOCKS (IB)
ADDRESS FIELD (AF)
MESSAGE FIELD (MF)
C1
C2
C3
C4
C5
C6
C7
C8
D1
D2
#0
#1
#2
#3
#4
#5
#6
#7
#8
#9
#10
160ms

FIG.33

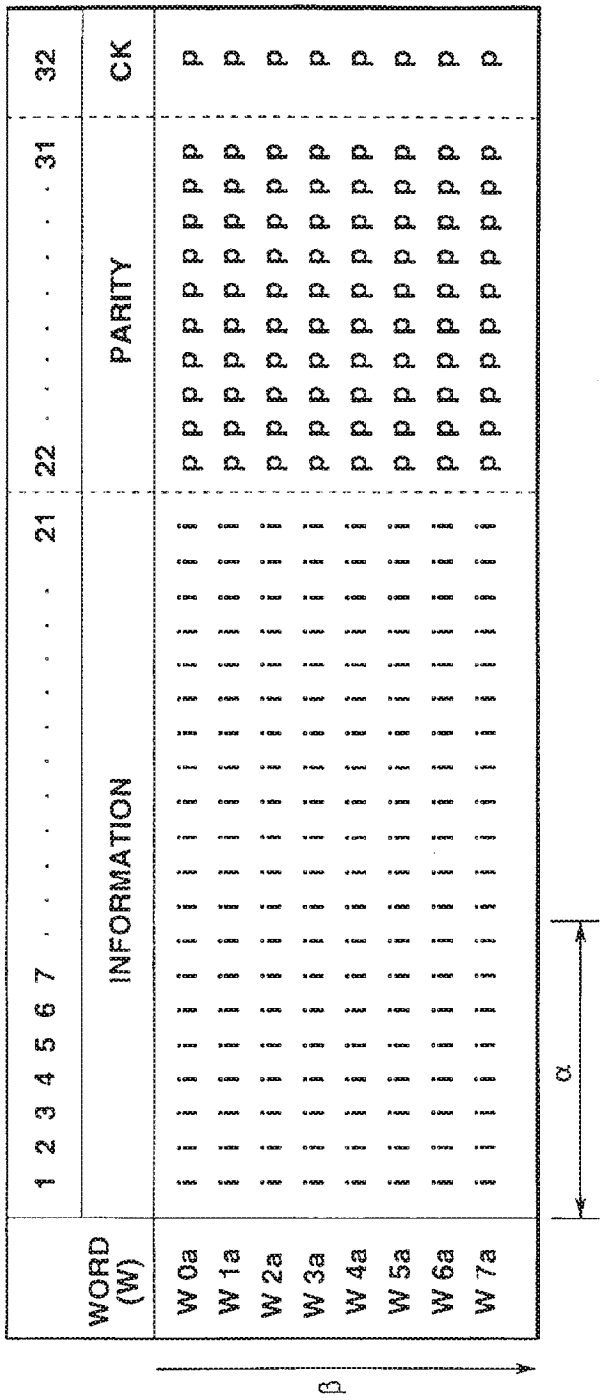

WORD (W)
1 2 3 4 5 6 7 . . . . . 21 22 . . . . . 31 32
INFORMATION
PARITY
CK
W 0a
W 1a
W 2a
W 3a
W 4a
W 5a
W 6a
W 7a
α
β

FIG.34

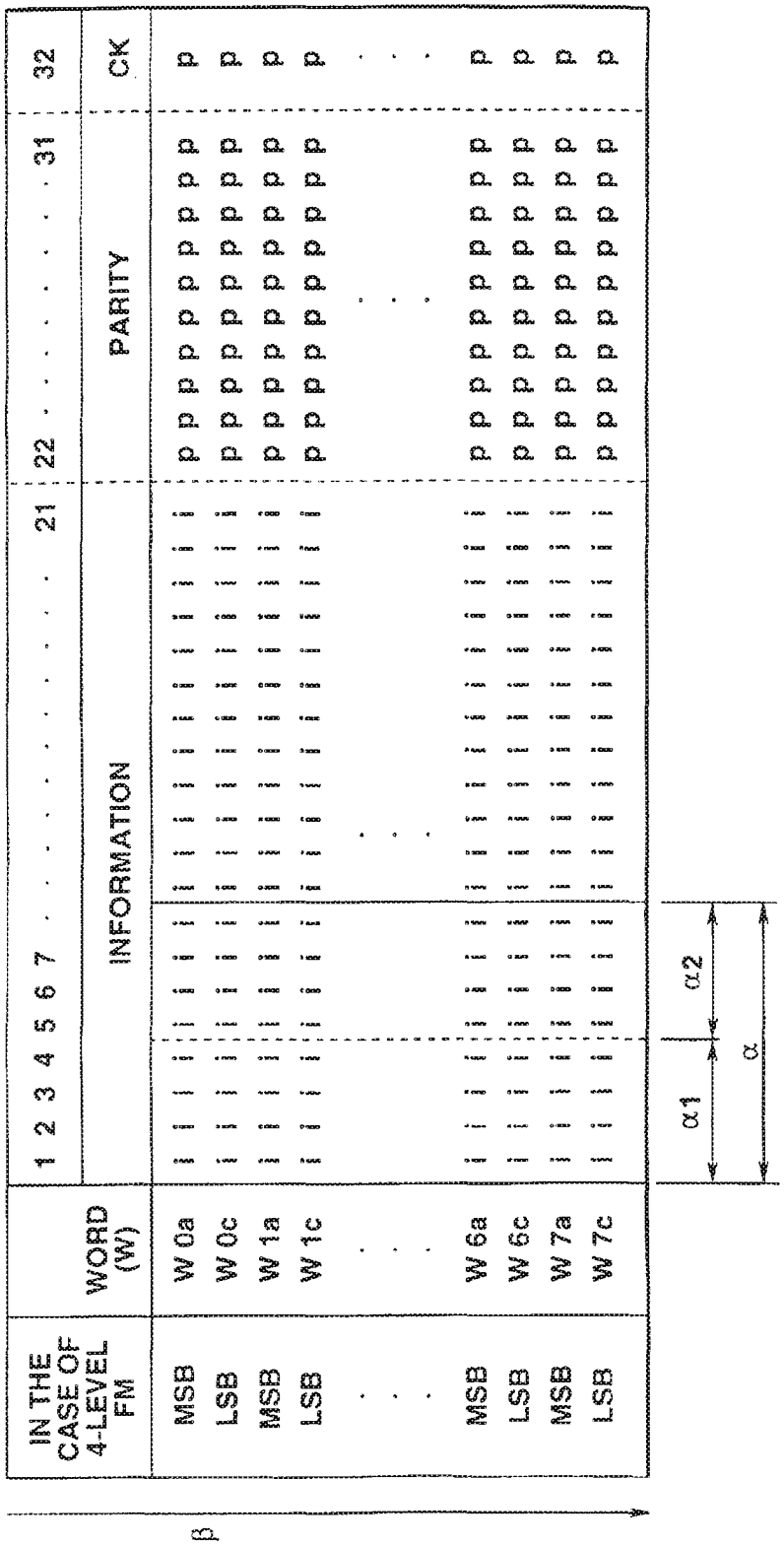
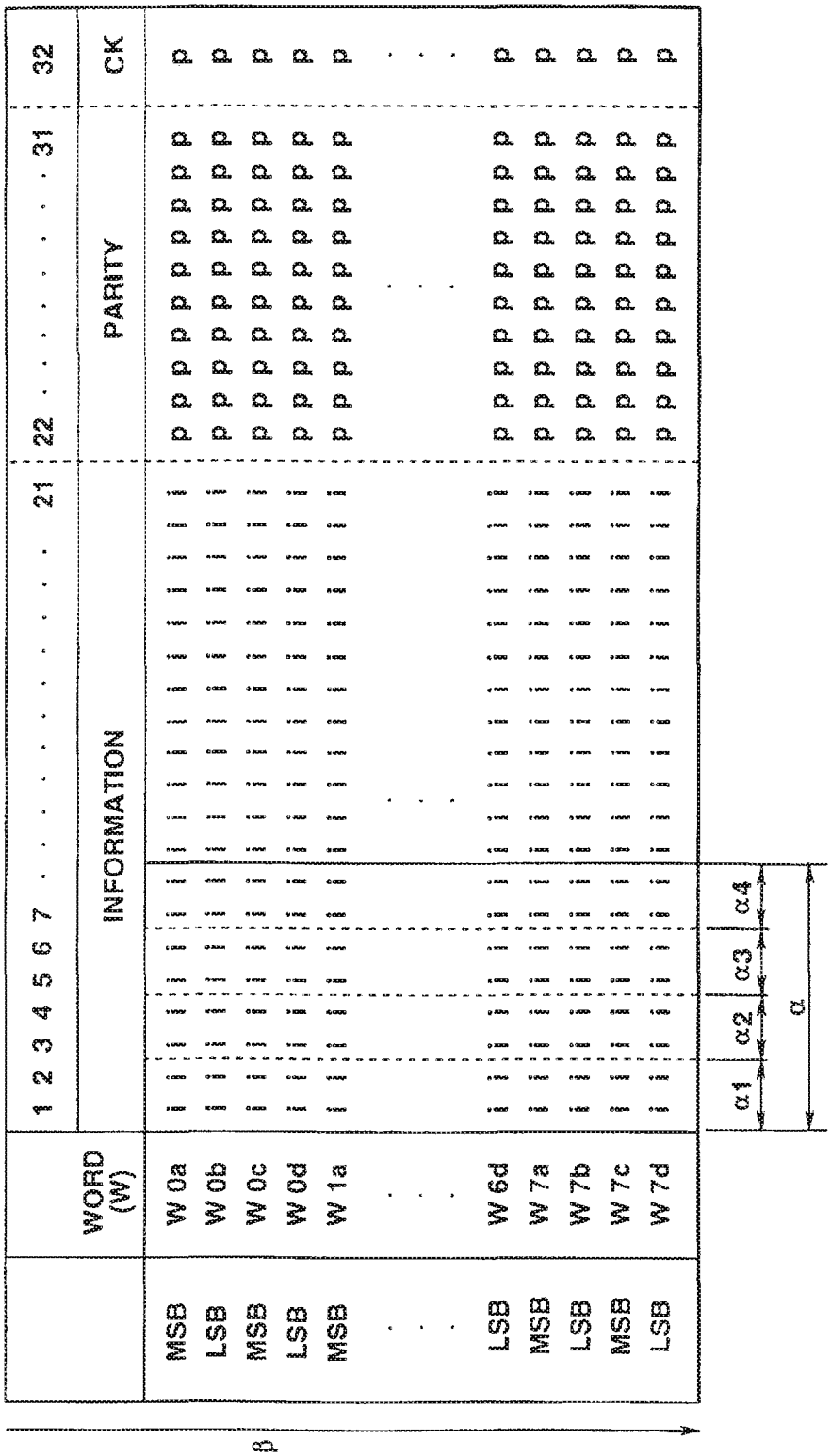

IN THE CASE OF 4-LEVEL FM
WORD (W)
1 2 3 4 5 6 7 21
INFORMATION
22 31
PARITY
32
CK
MSB
LSB
W 0a
W 0c
W 1a
W 1c
W 6a
W 6c
W 7a
W 7c
p
α1
α2
α
β

FIG.35


WORD (W)
INFORMATION
PARITY
CK
1 2 3 4 5 6 7 . . . . . 21 22 . . . . . 31 32
MSB
LSB
W 0a
W 0b
W 0c
W 0d
W 1a
W 6d
W 7a
W 7b
W 7c
W 7d
α1
α2
α3
α4
α
β

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/JP 96/03755

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04L1/12 H04Q7/18

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 264 205 A (NIPPON ELECTRIC CO) 20 April 1988	23
Y	see abstract	1-3,6-8
A	see column 2, line 5 - line 22 see column 5, line 5 - column 6, line 53; claims 6-11,13-16; figures 5-8	4,5,9-22

Y	WO 92 22162 A (BRITISH TELECOMM) 10 December 1992	4,5
A	see abstract see page 1, line 8 - page 3, line 6 see column 5, line 16 - column 7, line 6; figures 1,2	1-3,6,9

	-/--	

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4

Date of the actual completion of the international search	Date of mailing of the international search report
17 April 1997	06.05.97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Gries, T

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IPR2020-00034 Page 02052
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INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/JP 96/03755

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 117 500 A (DAVIS WALTER L ET AL) 26 May 1992	1-8
A	see abstract see column 3, line 35 - line 68; figures 1,3,4 see column 5, line 22 - column 6, line 10 see column 7, line 21 - line 46 see column 8, line 20 - column 11, line 37; claims	9-23
A	WO 90 08446 A (ATE CORP) 26 July 1990 see page 3, paragraph 1 - page 5, paragraph 1	1-22
A	US 5 168 493 A (NELSON LEONARD E ET AL) 1 December 1992 see page 2, line 4 - line 45; claims; figures	1-23
A	US 4 816 820 A (DAVIS WALTER L) 28 March 1989 see abstract see column 2, line 5 - line 28 see column 4, line 28 - column 5, line 7 see claims; figures	1-23
A	EP 0 344 149 A (MOTOROLA INC) 6 December 1989 see column 3, line 8 - line 47	1-23
A	US 5 196 842 A (GOMEZ FERNANDO A ET AL) 23 March 1993 see column 2, line 64 - column 3, line 39	21
A	US 5 309 154 A (MUN KYUNG T ET AL) 3 May 1994 see column 2, line 35 - line 60	21
A	US 5 347 268 A (NELSON LEONARD E ET AL) 13 September 1994 see abstract see column 2, line 48 - column 6, line 17; claims; figure 1	22

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IPR2020-00034 Page 02053
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INTERNATIONAL SEARCH REPORT

...formation on patent family members

Inter ...al Application No
PCT/JP 96/03755

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INTERNATIONAL SEARCH REPORT

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Inter nal Application No
PCT/JP 96/03755

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		JP 6101699 B	12-12-94
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		KR 9511489 B	05-10-95
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IPR2020-00034 Page 02055

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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : **H04Q 7/20, H04L 1/12** | **A3**

(11) International Publication Number: **WO 98/37713**

(43) International Publication Date: 27 August 1998 (27.08.98)

(21) International Application Number: PCT/SE98/00197

(22) International Filing Date: 3 February 1998 (03.02.98)

(30) Priority Data:
08/801,386 20 February 1997 (20.02.97) US

(71) Applicant: TELEFONAKTIEBOLAGET LM ERICSSON (publ) [SE/SE]; S–126 25 Stockholm (SE).

(72) Inventors: LABONTE, Sylvain; 380, Raymond, St–Bruno de Montarville, Quebec J3V 2S7 (CA). TURCOTTE, Eric; Apartment 1B, 460, Abelard, Verdun, Quebec H3E 1B5 (CA).

(74) Agent: ERICSSON RADIO SYSTEMS AB; Common Patent Dept., S–164 80 Stockholm (SE).

(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(88) Date of publication of the international search report:
12 November 1998 (12.11.98)

(54) Title: SUPPORT OF MULTIPLE MODULATION LEVELS FOR A CELLULAR PACKET CONTROL CHANNEL

(57) Abstract

A D–AMPS+ cellular communications air interface (50) is presented wherein a packet data control channel (40, 60) and packet data traffic channel (42, 62) are supported in addition to the conventional digital control channel (20) and digital traffic channel (22, 64). In particular, the packet data control channel and packet data traffic channel support multiple modulation level operation (high versus low). Procedures are provided for mobile station selection, as well as re–selection (102, 110), of either the high or low–level modulation for the packet channels. Procedures are further provided for facilitating a fall–forward (158, 164, 190, 194) to the high–level modulation packet data control channel, or a fall–backward (222, 232, 254) to the low–level modulation packet data control channel with respect to both uplink and downlink packet data communications.

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INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/SE 98/00197

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04Q7/20 H04L1/12

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 92 22162 A (BRITISH TELECOMM) 10 December 1992 see page 2, line 1 - page 4, line 6	1-7,12, 17,22
P,X	WO 97 15131 A (ERICSSON TELEFON AB L M ;ERICSSON GE MOBILE INC (US)) 24 April 1997 see page 16, line 2 - page 18, line 12 see page 19, line 28 - page 20, line 19	1-7,12, 17,22
P,X	WO 97 44926 A (SIEMENS AG ;SPLETT ARMIN (DE)) 27 November 1997 see page 2, line 35 - page 4, line 9	1-7,12, 17,22
A	WO 95 07578 A (QUALCOMM INC) 16 March 1995 see page 3, line 13 - page 4, line 12 see page 14, line 36 - page 15, line 2	1-7,12, 17,22

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29 September 1998	05/10/1998

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

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Inte ional Application No
PCT/SE 98/00197

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		ZA 9406674 A	02-05-1995

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(51) International Patent Classification 6 : G01R 31/08, H04H 27/10, H04L 27/10, 27/18, 5/16 — A1

(11) International Publication Number: **WO 98/59254**

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(21) International Application Number: PCT/US98/11107

(22) International Filing Date: 1 June 1998 (01.06.98)

(30) Priority Data:
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(54) Title: IMPROVED UNIVERSAL LAN POWER LINE CARRIER REPEATER SYSTEM AND METHOD

(57) Abstract

An improved local area network (LAN) to power line carrier (PLC) interface and protocol using FSK is described. This system provides improved data symmetry, higher data rates, lower bit error rates, improved synchronization and alignment of data, as well as improved carrier detection. The system provides high speed frequency shift key (FSK) modulation over the power line to achieve high data rates. Performance may be further improved by using a novel combination of FSK modulation and differential shift key (DFSK) modulation to provide an improved local area network (LAN) to power line carrier (PLC) interface and protocol using FSK and DFSK. DFSK is described and shown to provide improvements in the modulation and demodulation of data transferred over digital networks.

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IMPROVED UNIVERSAL LAN POWER LINE CARRIER REPEATER SYSTEM AND METHOD

Background of the Invention

Field of the Invention

This invention relates to Power Line Carrier (PLC) Local Area Network (LAN) repeaters in which LAN signal/data are transferred over the existing power lines of a building via power line carrier rather than through special cables which must be installed professionally. A PLC LAN repeater must (a) interface effectively with the LAN and its protocols, (b) achieve data rates over the power lines which are at least an order of magnitude faster than those of prior art PLC systems and (c) provide acceptable operation to a plurality of users. While many LAN (including Arcnet, Token Ring and RS-485) are in use and may be serviced by the instant invention, the Ethernet LAN will be examined to illustrate the interface and data rate requirements for this invention.

More specifically, this invention relates to systems for PLC LAN repeaters which employ a differential frequency shift key (DFSK) technique to increase data rates and noise immunity and system reliability. The use of DFSK technology improves the performance of PLC LAN repeaters by improving edge resolution; reducing the effective bandwidth requirements of the transmitted signal, thereby permitting increased data rate or narrower filter bandwidth; reducing the temperature coefficient and tuning requirements by AC coupling of the analog data; reducing startup transients in the data slicer; rejecting noise on the marking frequency; permitting special characters for compression or control purposes. This invention incorporates a number of other improvements over the existing technology, including: improved RF and IF filters to increase the data rate; synchronization of the data rate clock with the carrier frequency; a realignment bit every ninth bit; a group knowledge (ACK) which is frequency shift keyed (FSK) at a lower data rate; and carrier detection is accomplished without use of a Receive Signal Strength Indicator (RSSI), using special preamble and start characters. These improvements provide a complete modulation and demodulation system for PLC with significantly enhanced data quality.

Description of Related Art

The Ethernet IEEE 802.3 standard provides for mechanical and electrical standards and protocols for multiple users to share ("network") data transfer access to a common transmission medium or bus (the "ether" of a cable) but still maintain acceptable data access times and transmission rates. A user accesses the network through his node on the network, which is usually his computer/workstation with a hardware LAN interface physically connected to the network cable as the node. Proprietary network software (such as NetWare and Windows for Workgroups) runs with the workstation's operating system to manage the interface between the user's applications and the network. Individual users are provided unique ID/address codes so that only messages with the correct address preamble may be accepted and routed into their node/workstation while ignoring all others. The protocols also provide for detecting and managing collisions between the plurality of network users seeking simultaneous access to the network so that only one user may safely transmit data at a time. The software for implementing this Carrier Sense Multiple Access with Collision Detection protocol (CSMA/CD) is usually divided between firm embedded in the Ethernet interface cards and the proprietary workstation software.

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IN a peer-to-peer network configuration, two or more workstations may be networked together. Each user may communicate with any other user with network protocols arbitrating data collisions when more than one user seeks to initiate communication at a time. In the Ethernet specification, when a collision is detected, each user interface backs off for a "random" time before reattempting access (CSMA/CD). In a client-file server configuration, each user communicates with the server as well as directly with other users. Arbitration takes place between the users and the server.

Since a large number of users results in frequent data transfers as well as collision arbitration, the data rate of Ethernet must be very high to accommodate acceptable transmission time delays. Consequently, the IEEE 802.3 standard provides for data transmission at the rate of 10Mbps in packets of no more than 1,500 bytes. Such speeds are three orders of magnitude beyond prior art PLC data communication/LAN technology.

In addition, Ethernet mechanical standards provide for bidirectional communications either by coaxial cable ("thin/thick net") or by dual sets of Unshielded Twisted Pairs (one for each direction of data flow) called UTP or "10baseT" cable. Coaxial interfaces utilize a transceiver to interface between the bidirectional digital data of one computer and the RF data modulated signals of the coax/thin net. The 10BaseT medium accommodates the bidirectional data more directly by using 2 sets of twisted pairs (one for transmit and one for receive data). To achieve 10Mbps data throughput an interface standard similar to RS-485 (CCITT V.11) is employed, which provides for balanced, isolated and low impedance transmitters and differential receivers. The RS-485 standard provides for up to 32 transmitters and receivers networked on the same data line. Both coaxial and UTP communications interfaces/LAN cards have been reduced to low cost, high performance commercial products sourced by many companies.

The problem with LAN systems such as Ethernet is the installation expense for the cables which can exceed $100 per "node" or user. Often the old commercial structures are prohibitively difficult to retrofit. Other companies are periodically requiring reconfiguration of office space to accommodate changing commercial needs and require a less expensive and more friendly method for connecting and reconfiguring workstations to their LAN. And there are limitations as to the length of cable one can use. The instant invention provides a cost effective alternative to special cable installation by "repeating" the network via power line carrier data transmission over the AC power lines of a premises.

RF LAN repeaters have been offered in the 900 MHz range where sufficient bandwidth is available to transmit the 10Mbps signals. However, the 900 MHz systems are not only prohibitively expensive (at $600-800 per node) but also exhibit propagation problems and interference in commercial buildings where LAN systems are most commonly used and the software for managing a large number of users has been unacceptable, which (in addition to high cost) has detracted seriously from their widespread proliferation.

Summary of the Invention

The instant invention, however, provides both the interface for the commercial LAN card/port as well as the PLC repeater system capable of transferring data packets at sufficiently high rates and with collision

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detection/prevention firmware for transparency with respect to small and medium sized LAN systems at a competitive cost.

The PLC repeater/transreceiver comprises both a novel data transmitter and advanced data receiver with over 90 dB of gain, which together are capable of high bandwidth/data rate Frequency Shift Key (FSK) transmission data rates of DC to over 2 Mbps (million bits per second). RF PLC frequencies of 2-20 MHz combined with sufficient transmitter power and receiver sensitivity achieve adequate signal to noise ratios in AC power systems with high attenuation and noise. The over-90 dB sensitivity/RF range permits proper data transmission over the 3-phase power distribution system in industrial installations with capacitive loads and electrical equipment induced noise. The RF carrier frequencies in combination with the receiver sensitivity permit the signals to jump phases in residential 2-phase and industrial 3-phase distribution systems by means of the capacitance between phases in the wiring. The highly deviated (greater than 100kHz) FSK signal in combination with the high RF carrier frequency and 3 stages of RF and IF filtering in the receiver makes the data transmission very robust in the presence of electrical interference.

Multiple transceivers are capable of simultaneous operation at different RF carrier frequencies, permitting full duplex serial communication as well as multiple networks operating without interference on the same power line bus.

The LAN interface comprises 2 subsystems: (1) a bidirectional LAN card or port interface (a) for receiving (and storing in buffers) outgoing data packets in the LAN system format from a user's workstation for transmission to other LAN users and (b) for returning data packets in the LAN format to the same workstation card/port from other users, and (2) an asynchronous serial data transceiver (with data buffering) which (a) drives the PLC data transmitter with the outgoing data packets stored in the buffer by the port interface and (b) receives incoming data from the PLC data receiver originating from other users. The serial data transceiver is controlled by a system controller with firmware (i) to arbitrate collisions on the power line data bus with other users and (ii) to manage the bidirectional transfer of data packets: OUTGOING from LAN interface to serial data transceiver and INCOMING from serial data transceiver back to LAN interface. Commercial controllers are available for managing the entire repeater which contain both the asynchronous PLC serial port and some LAN interface ports such as RS-232 and RS-485, as well as parallel ports.

A relatively simple and low cost PLC LAN repeater networks workstations through their standard serial ports using software such as NetWare Lite. The PLC LAN repeater consists of a low cost but competent microcontroller with (1) an RS-232D port (115.2Kbaud) for connecting a built-in serial port to the users and (2) an asynchronous serial communications port which connects to the PLC transceiver. The onboard controller firmware manages the storage and retransmission of data packets in addition to collision arbitration and detection on the PLC bus. The PLC LAN repeater thus converts a two-user RS-232 peer-to-peer network into a more-than-two user network (like RS-485) without the user having to by a (more expensive and less common) RS-485 type of interface. The data rate for PLC bus could be 10 times higher than the limited 115.2 Kbaud of the conventional serial port, making this kind of PLC bus network capable of handling much larger data traffic than is possible with an ordinary RS-232 serial port network.

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Alternatively, personal computers (PCs), printers and other electronic devices can be networked together using this invention through standard parallel ports using standard interface protocol software and controllers, including but not limited to Windows 95.

The proliferation of embedded controllers in a plethora of electrical/electronic equipment can be effectively networked with control maintenance/security systems via PLC LAN repeater subsystems also embedded in the equipment, which repeaters network the serial port of the embedded controllers to a PLC LAN bus via the existing power cord of the equipment and the power distribution system of a premises. The inventors have applied this same concept of embedded PLC LAN repeater to many types of computers and related products, modems, industrial control systems and utility metering equipment. The instant invention facilitates the higher data rates and transmission integrity required by these systems.

For LANs using the RS-485 ports, a high-speed 485 interface is provided together with a controller for converting the data to PLC transceiver compatible rates and format.

A more complex configuration for Ethernet illustrates the scope of application of the universal repeater and utilizes a commercial Ethernet interface chip in combination with a microcontroller with global high-speed communications port for servicing the PLC transceiver. This provides a transparent PLC repeater which connects to the standard Ethernet ports of a workstation and, with NO additional software or hardware, permits multiple users to network over the existing power lines of a premises.

The versatility of configurations also supports Token Ring and Arcnet protocols, chiefly because the PLC transceiver is competent enough to handle sufficiently high data rates to permit transparent operation for smaller segments of the network.

Objects

Accordingly, it is an object of the invention to provide an advanced method and system of high data rate power line carrier transmission which supports the data rates required by local area networks.

It is an object to provide a method and system of interfacing power line carrier repeaters with conventional network cables or cards to convert LAN data to PLC repeater acceptable data and to convert PLC repeater data to LAN data.

It is a further object to provide a method and system of arbitrating multiple PLC LAN repeaters to permit efficient and exclusive access to a particular frequency/channel of the power line medium.

It is an object to provide a PLC transceiver which sends data with a bandwidth of DC to over 2 Mbps and which is therefore able to transfer wideband analog signals/data of DC to over 1 MHz bandwidth.

It is an object to provide an embedded PLC network repeater system capable of being interfaced with embedded controllers in equipment for networking said equipment with automation, control and diagnostics systems and general network services.

It is a further object of this invention to provide an embedded PLC network repeater system having an improved modulation technique, known as Differential Frequency Shift Key (DFSK) in conjunction with Frequency Shift Key (FSK) which is able to trigger data state changes with much improved resolution.

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A still further object of this invention is to provide an embedded PLC network repeater system having a DFSK modulation technique which by centering more energy around the carrier frequency minimizes the effective bandwidth required for a given data rate.

A further object of this invention is to provide an embedded PLC network repeater system employing improved RF and IF filters to provide wider and flatter pass bands while maintaining system data reliability with changing data compositions.

Another object of this invention is to provide an embedded PLC network repeater system employing a realignment bit at the end of each data byte to aid the re-synchronization of the receiver, thereby permitting increased data rates.

Another object of this invention is to provide an embedded PLC network repeater system with improved carrier detection and acknowledgment techniques.

An additional object of this invention is to provide an improved modulation and demodulation technique, known as Differential Frequency Shift Key (DFSK), for all networking media or electronic communications systems, including RF and wired media.

Additional objects, advantages and novel features of this invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art upon examination of the following or may be learned by the practice of this invention. The objects and advantages of this invention may be realized and attained by means of the instruments and combinations particularly pointed out in the appended claims.

These and other objects of the invention are achieved by an electronics system, which in its present preferred embodiment employs an innovative Differential Frequency Shift Key (DFSK) modulation technique to improve the reliability and achievable data rates of Local Area Network (LAN) communication between digital computer workstations across Power Lines or Power Line Carrier (PLC) mediums. While the preferred embodiment of the system is designed to operate at data rates of up to 2 million bits per second (2Mbps), even higher data rates are possible with some envisioned enhancements, and very high noise, jitter, temperature, and voltage drift immunity.

Brief Description of the Drawings

Figure 1 is a diagram of a PLC LAN repeater network.

Figure 2 is a block diagram of a PLC LAN repeater.

Figure 3 is a schematic of a LAN to Repeater Interface.

Figure 4 is a schematic of a PLC Repeater Transceiver.

Figure 5 is a schematic of a standard quadrature detector for the demodulation of FSK carrier signals.

Figure 6 is an illustration of the voltage output from the quadrature detector buffer amplifier 5-54 (V_{quad} 5-59), showing the variance of the voltage level with frequency change.

Figure 7a shows the schematic of a DC-coupled FSK data comparator. Figure 7b shows the ideal operation of the DC-coupled FSK data comparator. Figure 7c shows the operation of the DC-coupled FSK data comparator when there is signal drift.

Figures 8a, 8b, and 8c illustrate the operation and disadvantages of the traditional FSK data slicer 8-70.

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Figure 9a illustrates the DFSK data detector of the preferred embodiment of the invention which overcomes the limitations of prior detectors. Figure 9b shows the nature of DFSK V_{quad} signals as they are detected by a quadrature detector. Figure 9c shows the effect of temperature or data composition on the operation of the DFSK data detector. Figure 9d depicts a further modification/enhancement of the DFSK demodulator.

Figure 10 illustrates a comparison of the frequency spectrum of FSK with DFSK modulation and illustrates the improved bandwidth requirements of DFSK over FSK.

Figure 11 illustrates the implementation of DFSK modulation using a 5-state digital state machine.

Figure 12 illustrates a state machine improvement where the data rate is synchronized with the carrier frequency.

Figure 13 is a MC13158 receiver data book chart for the RSSI response which shows a limiting characteristic RSSI detection schemes and protocols based on RSSI signals.

Figure 14 illustrates several improvements achieved with the Acknowledge Comparator.

Figure 15 depicts a typical V_{quad} data and FSK ACK Data waveform which illustrates how DFSK permits the compatible use of FSK to produce special characters for group acknowledgment in a network.

Detailed Description of the Preferred Embodiment

A universal local area network (LAN) power line carrier (PLC) repeater system and method is described which provides: (1) a competent LAN repeater interface for converting high-speed LAN data to PLC serial data and high-speed PLC serial data to LAN data, (2) a high-speed PLC data transceiver for exchanging PLC data with other repeaters, and (3) a control system and method for controlling the interface and transceiver to arbitrate data communications on the PLC bus among the plurality of PLC repeaters. In the following description, the Ethernet LAN PLC repeater is set forth in specific detail in order to provide a thorough understanding of the invention in a non-trivial application. It will be apparent to one of ordinary skill in the art that these specific details are beyond what is necessary to practice the present invention. In other instances, well-known circuits, interfaces and software structures have not been shown in detail in order not to unnecessarily obscure the present invention.

Reference is first made to Figure 1 in which a plurality of workstations are networked together by means of PLC repeater s and the AC power system of a premises. Workstation 1-1 with its corresponding LAN card is connected via UTP 1-2 to LAN-PLC repeater 1-3 to the AC power line 1-4 of a premises which constitutes a PLC LAN bus in addition to distributing AC power to the various appliances, equipment and workstations (1-1, 1-7, 1-10) of the premises. Data from workstation 1-1 is repeated onto the PLC LAN bus 1-4 in proper format for LAN-PLC repeater 1-5 to receive said data and repeat it in LAN format via UTP 1-6 to workstation 1-7 and its corresponding LAN card. Workstations 1-1, 1-7 and 1-10 are operated by commercial LAN software which, at a minimum, supports a peer-to-peer configuration of users, thus permitting messages and files to be transferred between any two peers of the network. The LAN PLC repeater permits said data to be transferred between workstations "transparently," that is, without any additional effort or special instructions/software on the part of the workstation and its operating system. Therefore, workstation 1-7 receives the data originating from workstation 1-1 and confirms receipt thereof back to 1-1 via UTP 1-6, repeaters 1-5, AC power bus 1-4, repeater 1-3 and UTP 1-2.

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While two workstations networked together peer-to-peer constitute the minimum configuration of a network and do not require sophisticated network arbitration, many commercial network products assume that additional workstations, represented by 1-10, may be connected to the network, seeking network access simultaneous with other workstations and requiring CSMA/CD. In a PLC LAN repeater, arbitration protocols peculiar to the PLC environment need to be serviced transparently to the workstations/users.

Figure 1 also illustrates a segmented bus configuration comprising both a conventional hard-wired LAN bus segment 1-12 network and a PLC LAN interface 1-11. In this example, the LAN bus 1-12 networks physically proximate workstations together (not illustrated), while the PLC bus segment 1-4 could network physically less proximate or more mobile workstations 1-1, 1-7 and 1-10 to the network via PLC-LAN interface 1-11. Interface 1-11 is also a "repeater" similar in hardware to repeater 1-3, but may include software/firmware which identifies and repeats only those LAN packets/data addressed to workstations 1-1, 1-7 and 1-10 on the PLC LAN segment 1-4, thereby reducing the data traffic load on said PLC segment 1-4. In large networks involving many workstations, a plurality of PLC LAN segments 1-4, each operating on its exclusive PLC frequency and serviced by its respective PLC-LAN interface 1-11, may be networked together by means of the instant invention, while sharing the AC power distribution bus through frequency domain multiple access or other multiple techniques such as code division multiple access.

Referring still to Figure 1, other communication devices besides workstations may be represented by workstations 1-1, 1-7 and 1-10. For example, embedded microcontrollers 1-1 and 1-7 with communication ports could be networked through embedded repeaters 1-3 and 1-5 with a host controller 1-10 which monitors/controls the operation of the equipment hosting said microcontrollers. A relatively simple network communication and arbitration protocol could be administered by said host repeater 1-8. Such protocols have been developed for applications such as utility meter reading and industrial control systems.

Figure 2 is a block diagram of a LAN PLC Repeater 1-3. The LAN connection 1-2 to repeater 1-3 is made at RJ-45 connector 2-1, which is operably connected via connections 2-2 and isolator 2-3 to the differential transmit and receive ports 2-4 of LAN interface IC 2-5. Network Interface Controller (NIC) 2-5 (data sheets may be found in National Semiconductor's Local Area Network Databook, incorporated by reference) is a generic, multiple-sourced part which is common to most sophisticated LAN networks and contains the hardware registers, connections and logic/firmware to transmit and receive high bit rate LAN signals with standardized preambles, packet sizing and CSMA/CD collision arbitration. A standard RAM (Random Access Memory) 2-6 sufficient size is operably connected to NIC 2-5 via memory address and data bus 2-7 to store incoming and outgoing data packets: (1) incoming packets which have been received from LAN connection 1-2 and are waiting to be transmitted further by μC 2-9 and (2) outgoing packets which were received by μC 2-9 and are waiting to be transmitted back through LAN connection 2-1 to the network 1-2 or LAN card of a workstation 1-1. The repeater is controlled by μC 2-9, which is operably connected to NIC 2-5 via control, data and address lines 2-8, permitting the μC 2-9 to setup and control the NIC 2-5 and transfer data packets bidirectionally into/out of the packet buffer 2-6. In addition, μC 2-9 has communication ports, both parallel and serial, for communicating LAN data with wired and/or PLC interfaces. Some

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commercial μC's, such as the Intel 83C152 (an 8031 derivative, data sheets for which may be found in Intel's Bit Embedded Microcontroller Handbook, incorporated by reference) contain high-speed Global Serial Channels (GSC) 2-10 which are capable of 0.1 – 10 Mbps serial data transfer with CDMA/CD protocol registers and firmware at a reasonable cost, which facilitates data I/O for a high-speed PLC transceiver (2-11 through 2-17 or Figure 4), which is operably connected to the global series channel 2-10. Transmit data TXD from the incoming packet buffer 2-6 modulates an RF carrier at modulator 2-11 which drives transmitter 2-12, which transmitter is operably connected to the power line bus 1-4 via Filter 2-13 and RF coupler 2-14. Transmitter 2-12 is turned ON by transmit enable TXE only when data is transmitted, thus reducing the RF traffic on the AC line 1-4 during latent periods. Data receiver 2-16 is operably connected to AC bus 1-4 via RF coupler 2-14 and filter 2-15. Data-modulated RF from similar repeaters carried by power line 1-4 is received by the receiver 2-16, buffer by high-speed comparator 2-17 and transferred as RXD to global serial port receiver 2-10where μC 2-9 screens the preamble for ID codes/addresses and arbitrates the data for transmission on to the LAN interface. Unique ID codes repeater addresses may be either manually entered by dipswitch or automatically assigned by network supervisory software under automatic or user control. For example, manual entry ID code switches 2-22 operably connect to a port of the μC 2-9 via lines 2-21, and may be used to uniquely identify address and security bytes in preambles and/or determine arbitration backoff delay times, etc. Factory-burned ID codes can also be obtained with specialty or ASIC designs.

Figure 2 also illustrates alternate LAN and data sources for the PLC repeater. The μC 2-9 provides a standard serial comm port 2-20 which connects to a serial port interface 2-19 and connector 2-18, configuring repeater 1-3 into an RS-232D LAN repeater, in which the PLC data transceiver operates at substantially higher data rates (than the 115.2Kbaud RS-232D) to unburden the AC power bus 1-4 LAN. (The Network Interface Controller and associated parts would be removed, if unused in this alternate embodiment.) IN some network configurations, parallel port interface components could be operably connected in place of serial components 2-18 and 2-19 to a parallel port on μC2-9. Alternately, the GSC port 2-10 could be operably connected to an RS-485 LAN via a 2-19 interface like the LTC490, while the μC serial port 2-20 TxD and RxD lines could be operably connected to the TXD and RXD I/O 2-11 and 2-17 of the PLC transceiver. In its simplest embodiment, the TxD and RxD lines 2-20 may be operably connected to TXD and RXD lines 2-10, providing a repeater requiring μC; PLC transmitter 2-12 and receiver 2-16 have been operated simultaneously on different carrier frequencies to provide full duplex serial operation, if required by the LAN application. Alternately, the transmitter in a no μC system may be enabled only when data is transmitted, to permit PLC LAN operation with a single frequency.

Figure 3 presents a detailed working schematic of the LAN interface and 10 Mbps to 1 Mbps converter. J1 2-1 is the RJ-45 connector to the LAN line/card of a workstation. U3 2-3 is the Isolator/Filter for Ethernet 10Mbps lines. U1 2-5 is the NIC chip, a National DP83902A, the complete specs for which are found in National Semiconductor's Local Area Network Databook, already incorporated by reference, which also contains comprehensive documentation on the Ethernet IEEE 802.3 standard. Several Network Interface Controllers are available from various manufacturers for Ethernet as well as other popular network standards, such as Arcnet and Token Ring, which may be operably connected to μC U6 2-9 in place of Ethernet NIC 2-5 and the corresponding connectors 2-1 through 2-4.

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Referring still to Figure 3, an 8Kbyte RAM packet buffer U5 2-6 is operably connected via address latch U7 3-27 to the memory address and data ports of NIC 2-5. The size of buffer 2-6 may be enlarged or reduced somewhat to accommodate network data capacity, system operation and budgetary constraints. Repeater μC U6 2-9 is operably interfaced with NIC U1 2-5 via latches, U13, U14 3-25 & 3-26 and PAL U15 3-28. The timing diagrams and PAL 3-28 logic diagram are appended herewith in Appendix B. Additional functions 20 MHz clock 3-29, 10 MHz divider 3-30, status drivers 3-31 and status indicators D1, D2 and D3. While one enabling embodiment has been represented, those skilled in the art will appreciate that other approaches and simplifications can be implemented without departing from the method presented herein.

Referring to Figure 3 again, the μC 2-9 may contain masked ROM firmware or may be operably connected with external EPROM U9 3-9 for development purposes. A pseudo-code listing follows:

LAN PLC REPEATER PSEDUO-CODE FLOW SHEET

```
RESET ON POWER UP
STARTUP SEQUENCE
'Initialize µC sets up the communications registers for Manchester
'Encoding with CSMA/CD. A 16-bit CRC is selected and the preamble
'is set to 8 bits. The serial rate is set to 1.25Mbps.
INITIAZLIE µC
        GMOD Register
                Select Manchester Encoding
                Select CSMA/CD
                Enable CRC, Select 16-bit CRC
                Set preamble to 8 bits
        Baud Register
                Set serial rate at 1.25 Mbps
        Disable all interrupts
        Enable receiver
        Set transmit status register to normal operation
        Set address mask registers to don't care state
        Initialize SLOTTM (slot time register) to 2µs
'Initialize NIC divides the 8K buffer into 2 Xmit buffers and 20
'256 byte pages for the receive ring. Data is handled a byte at 'time and the FIFO to receive buffer ring occurs 8
bytes at a time.
'The CRC is appended by the transmitter. The receiver rejects 'errored packets. All valid packets are received.
INITIALIZE NIC
        Setup 8K xmit/rcvr buffer
        Setup 2 Xmit buffers of 1536 bytes each
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        Set remaining 5120 bytes as receive buffer ring
        SETUP NIC REGISTERS:
            Data Configuration Register
                Byte wide DMA transfer
                Normal operation
                FIFO set to 8 bytes
            Transmit Configuration Register
                CRC appended by transmitter
                Normal operation
                Normal backoff
            Receive Configuration Register
                Reject packets with receive errors
                Reject packets with fewer than 64 bytes
                Accept broadcast packets
                Accept all packets (promiscuous mode)
                Buffer packets to memory
    'The μC Receive Routine keeps track of the current NIC transmit
    'buffer then loads that buffer data as it is received in the
    'μC Receive FIFO.
    RECEIVE Routine: (μC ROUTINE for μC to send data to NIC)
        Choose free NIC transmit buffer
        IF NIC transmit buffers full, THEN
            Discard receiver and GOTO TRANSMIT
        Check Receive FIFO for Not Empty (NE) flag on μC
        Read byte from Receive FIFO
        Check Receive FIFO NE flag on μC
        IF FIFO Empty, THEN validate byte (No collision packet byte)
            IF transmit pending, THEN
                Restart backoff
            ELSE GOTO RECEIVE ROUTINE:
        ELSE GOTO READ ROUTINE (Valid Data Packet)

        READ ROUTINE: Write byte to NIC transmit buffer
            Read FIFO NE flag
            IF NE flag asserted, THEN GOTO READ ROUTINE
            ELSE write last data byte to NIC transmit RAM
```

```
                    (Packet has been read and written to NIC)
                Check receiver for receiver errors
                IF no errors, THEN
                    Instruct NIC to transmit Packet
                ELSE discard packet
                GOTO TRANSMIT
'The μC Transmit Routine checks its Global Serial Channel (GSC) for
'a not busy state.  If the GSC is not busy then the μC reads packet
'data from the NIC and loads the TX FIFO.
TRANSMIT ROUTINE:  (routine for μC to get data from NIC)
    IF NIC has received a valid packet, THEN
        IF Global Serial Channel (GSC) is not busy, THEN
            Get pointer to received packet
            Read 2 bytes from NIC
            Save 1st byte (this is a pointer to the next received packet)
            Read 2 bytes from NIC
            Save these bytes in variable ByteCount

            LOOP
                Wait TX FIFO Not Full (NF Flag)
                Read 1 byte from NIC
                Write 1 byte to μC TX FIFO
                Decrement ByteCount
            ENDLOOP (When ByteCount is zero)
    ELSE GOTO RECEIVE ROUTINE
```

An additional routine services AC PLC bus collision avoidance and access arbitration. The method requires each repeater (with data to send) seeking access to a particular frequency or channel of the AC LAN bus (1) to listen to the bus traffic and, upon detecting the termination of a third party transmission, (2) to wait a minimum of 20 μs plus a random additional time (in 5 μs increments) before transmitting a short access request. (3) Following the access request, the receiver listens for 15 μs and, upon detecting no other carrier, the repeater μC begins data transmission with confidence. The dipswitch 2-22 may be used to provide a unique backoff or wait time for each repeater in addition to providing a unique IC code/address.

The universal interface capabilities of the controller 2-9 with its parallel and serial ports provides the capability for embedding the PLC repeater in computers and equipment with embedded controllers which already

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connect to the AC power system of a premises, thereby networking the equipment with other similarly equipped devices and users simply by connecting the AC power. The physical size of such system and its associated cost could be reduced by utilizing the existing embedded controller and its serial port as the repeater controller and merely interfacing it to a compatible embedded PLC transceiver. The embedded controller would require the addition of appropriate network arbitration and control software/firmware. State-of-the-art design and manufacturing techniques reduce size and cost of repeater systems to attractive marketing levels.

Referring now to Figure 4, a versatile PLC data transmitter and receiver are shown which provide DC to 2 Mbps data rates. No Manchester or other encoding is required. Wideband data or analog signals may be transferred in original form. The data interface of the transceiver comprise four data lines: a transmit data input line GTXD, a transmitter enable input line TXE, a receive data output line GRXD and a carrier detect output line CARDET. These lines correspond to their counterparts at the Global Serial Channel 2-10 of the μC 2-9. GTXD data voltage levels are coupled to varactor diode D7, which is capacitively coupled to the frequency determining components C18 and C22 at the low-impedance port of oscillator 2-11, of which transistor Q3 4-33 forms the active element. Changes in reverse voltage across D7 result in corresponding inverse changes in the junction capacitance of D7 which change the resonant frequency of oscillation determined by L3 and the combination of C18 with the other capacitors C19 through C24. Driving the low-impedance port of oscillator 2-11 at the collector of Q3 4-33 minimizes the negative impact of differentiated DC voltage shifts on the delicate bias of Q3 4-33, which DC sifts correspond to differentiated data coupled through capacitors C19 and C22. The output of Q3 drives a class D output stage 2-12, which efficiently drives the power line through filter 2-13 and RF coupler 2-14. The several stages of transmitter drivers buffer the oscillator 2-11 from AC line capacitance and load changes. A class A transmitter output may be employed to reduce harmonics but with decreased efficiency. The transmitter enable TXE circuit 4-34 connects to the base of Q3 4-33 through D6 to turn the oscillator 2-11 off. The circuit of 4-34 may be configured as an inverter (for operation from a controller) or as a resetable monostable multivibrator (for enabling the transmitter only when data is presented to the data input).

Figure 4 also shows a data receiver 2-16 which is coupled by 2-14 RF coupler and filter 2-15 to the AC power bus. The filter 2-15 selects only the desired frequencies and matches the impedance of the AC line to that of the receiver input pin 1. The receiver 2-16 is a high performance superhetrodyne design with local oscillator, mixer, 2 stages of IF gain/filtering and limiter with quadrature detector, providing over 90 dB of RF gain with DC to 2 Mbps data response (Philips SA 636 version). The receiver 2-16 local oscillator supports either (1) crystals, (2) LC oscillators or (3) external oscillator/synthesizers. Use of a synthesizer permits controller 2-9 selection of LO frequencies for FDMA and frequency hopping configurations. Receiver 2-16 has both a data output and a competent FSI (Field Strength Indicator) output, which are buffered by high speed comparators 4-35 and 4-36 such as LM319 or LM360. It should be noted that an analog buffer can be connected to the demodulated signal output (pin9) of the receiver 2-16 for recovery of Wideband analog or composite analog/digital signals. The FSI CARDET output supports the RF carrier detect input of the repeater controller 2-9 for performing AC bus arbitration. The CARDET and GRXD buffered comparator outputs may be connected together in a wired AND configuration to provide

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data output only when BOTH the carrier is present AND data is present. The receiver 2-16 is so selective that multiple receivers and transmitters may be used simultaneously in a repeater to increase data rate, increase channels or network together AC power line LAN segments. The transmitter and receiver are fully capable of RF LAN operation which, in conjunction with the competent collision avoidance and arbitration, would provide competent RF LAN segments for many applications.

It should be noted that alternative commercial components of competent specifications can be used for the components specified herein. Although this invention has been illustrated in relation to a particular embodiment, it should not be considered so limited except by the appended claims.

Alternative embodiments of the PLC transceiver hardware can provide significant improvements in data rate while increasing system reliability. These alternatives employ a different modulation technique than the FSK described previously, where detection was done by analog comparator DC threshold adjustments in reference to an analog demodulated FSK data waveform. This previously described FSK modulation technique produced a waveform which at high data rate exhibits a ramping/semi-sinusoidal characteristic (instead of the ideal DC square waves produced at low data rates). The alternative embodiment, described following, uses a Differential Frequency Shift Key (DFSK) in conjunction with the FSK modulation technique. DFSK produces sharp data edges for triggering the data detector and further permits AC coupling of said data edges, improved speed of data demodulation, and increased data reliability – less subject to system temperature coefficients, while minimizing the required effective bandwidth for a given data rate by centering more energy around the carrier frequency.

Further improvements are incorporated in this alternative transceiver embodiment, including: improvements in RF and IF filters to provide wider and flatter pass bands while maintaining reliability with changing data compositions, an introduction of a realignment bit in the data to provide the means for allowing the receiver to re-synchronizing with each in-coming byte, improvements in carrier detection and acknowledgment, and an improved controller.

These improvements permit a dramatic improvement in data rate and bit error rate across the PLC interface, from previous speeds of 100 to 350 Kbps to 1-3 Mbps. The following discussion describes prior modulation circuits, their characteristics and the current best mode of the invention utilizing the DFSK modulation techniques.

Figure 5 illustrates a standard quadrature detector for demodulation of FSK carrier signals. The IF limited output 5-51 of a receiver IF section (for example as shown on Figure 4 at U1 2-16 pin 11) drives directly the first input 5-56 of a quadrature detector 5-50 (which is typically an analog Gilbert cell multiplier). Said IF limiter also drives loosely, through a small-valued, high-impedance capacitor C1 5-55, a quadrature tank circuit composed of an inductor L 5-56, an capacitor C 5-57 and a resistor R 5-58. The capacitor C1 5-55 is typically a small value, such as 5pF in order to avoid swamping the transfer function of the quadrature tank circuit. The typical values of L 5-56, C 5-57 and R 5-58 depend on the carrier frequency. For example: for a 10.7 MHz system L 5-56 would typically be 1.5μH, C 5-57 would typically be 139pF, and R 5-58 would typically be 2.2KΩ; while for a 20 MHz system L 5-56 would typically be 1.5μH, C 5-57 would typically be 39pF and R 5-58 would typically be 4.7kΩ. The

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quadrature tank circuit drives the second input 5-52 of the quadrature detector 5-50. The quadrature detector 5-50 is a multiplier which produces an output voltage QuadOut 5-53 that is the product of the two sine wave input signals. The double frequency output component of QuadOut 5-53 is filtered and amplified by the detector buffer amplifier 5-54, leaving the phase differential component V_{QUAD} 5-59 which varies in magnitude according to the frequency difference between the IF frequency received from a transmitter 5-51 and the quadrature tank resonant frequency determined by L 5-56 and C 5-57, as described in Figure 6. V_{REF} 5-66 is maintained at a voltage between the V_{QUAD} 5-59 FSK 1 and 0 levels, by the diodes D1 5-61 and D2 5-62. Comparator/Data Slicer 5-60 outputs data 5-64 at logic levels to a deserializer. The quality of the Data Slicer 5-60 is determined by how well it defines or recovers from V_{QUAD} 5-59 the edges of each data bit. Indeed, the quality of a complete modulation and demodulation system is determined by how faithfully data is transferred from the data transmitter to the data receiver. Prior data slicers exhibit two significant problems that are overcome by the present invention: (1) sensitivity to voltage drifts in V_{QUAD} 5-59, and (2) sensitivity to high data rates and data composition, as illustrated in the discussion and figures that follow.

Figure 6 illustrates that V_{QUAD} 5-59, the output of the quadrature detector buffer amplifier 5-54, varies lineraly with IF frequency within a 400KHz range. The attractive feature of this type of demodulator is that V_{QUAD} 5-59 is a DC level signal directly related to frequency, i.e., a 200KHz IF signal f_0 produces a +400 mV V_{QUAD} 5-59 signal and a +200 Khz IF signal f_1 produces a -400 mV V_{QUAD} 5-59 for low to intermediate data rates. The comparator 5-60 reference voltage V_{REF} 5-66 is maintained at a voltage corresponding to the virtual center frequency f_c between f_1 and f_0. Figure 6 also shows V_{QUAD} drift as a DC offset to the quadrature detector transfer characteristic at f_c about V_{REF}. V_{QUAD} drift is caused by the sum of temperature coefficient and long term frequency drifts of the transmitter and the receiver local oscillator in addition to the temperature coefficient and mechanical vibration drifts of the quadrature coil L 5-56 and capacitor C 5-57. The temperature coefficient drifts of quadrature detector 5-50, buffer 5-54 and comparator 5-60 are minor because V_{QUAD} is in the 400 mV range.

The prior DC coupled data slicer illustrated in Figure 7a may be less sensitive to data composition but is likely to be very sensitive to V_{QUAD} drifts. A second prior data slicer circuit, shown in Figure 8a, can track temperature coefficient and drift changes for low data rates, but no for high data rates or mixed data compositions.

At higher data rates, the V_{QUAD} buffer 5-54 slew rate combined with the time domain response limitations due to the bandwidth of the IF filters produce lower amplitude V_{QUAD} output signals are shown in Figure 7b. A lower data rate 3-bit long (0 0 0) V_{QUAD} signal is compared to a higher data rate single bit V_{QUAD} signal (0 1 0). While t1 through t3 is the period of a single high data rate bit, t1 through t7 is the period of a 3-bit long V_{QUAD} signal. At the higher data rate, the peak amplitude of V_{QUAD} at t2 and t4 is significantly lower than for the 3-bit long V_{QUAD} signal peak at t4 (and t10). The variation in V_{QUAD} peak voltage with data composition is significant enough to foil the operation of the V_{REF} bias circuit of Figure 5, but not that of Figure 7a, which illustrates a prior DC coupled data comparator with fixed reference (V_{REF}) as set by resistors R1 7-67 and R2 7-66. R1 7-67 and R2 7-66 are typically set to 1 kΩ. But while the DC coupled comparator of Figure 7a is able to slice the data from higher data rate or mixed data composition V_{QUAD} 7-68 signals illustrated in Figure 7b, it yet experiences significant data edge and bit

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width symmetry difficulties when encountering temperature coefficient and signal drifts. Figure 7c illustrates the negative effects of V_{QUAD} 7-68 drift on the data 7-69 signal. The width of the 0 bit is totally truncated form t1 to t3, while the width of the 1 bit is expanded accordingly.

Figures 8a through 8c illustrate the operation and disadvantages of the FSK data slicer 8-70 with tracking reference V_{REF} 8-71 provided by diodes D1 8-73 and D2 8-74 and hold capacitor C_{hold} 8-75. D1 8-73 and D2 8-74 become forward biased during the positive and negative peaks of the FSK V_{QUAD} 8-72 signal and ensure that C_{hold} 8-75 is charged to the peak FSK V_{QUAD} voltage value less the diode forward voltage drop (about 40 mV). Thus, if the gain of buffer 5-54 is adjusted to provide an 800 mV peak-to-peak V_{QUAD} signal to D1 8-73 and D2 8-74, C_{hold} 8-75 will be charged by D1 8-73 and D2 8-74 after a few lower data rate alternating bit cycles to an intermediate value of V_{REF} halfway between the 0-rail and 1-rail of V_{QUAD} 8-72 that ideally provides adequate comparator 8-70 "slicing" of data from V_{QUAD} 8-72, as illustrated in Figure 8b. However, as illustrated in Figure 8c, when lower amplitude high data rate signals are used (for which the peak amplitude of V_{QUAD} 8-72 is reduced below the forward voltage drop of D1 8-73 and D2 8-74) or when long strings of 1's or 0's present in the data, the slicer V_{REF} 8-71 begins to drift off of the ideal center voltage and causes corresponding data edge and width distortions as shown in Figure 8c. The width of high data rate bits at t2-t9 are significantly distorted. And while the string of 1's at t9 to t13 may have readjusted V_{REF} for a time, at t12 other drift factors such as diode D2 8-74 leakage or comparator 8-70 input bias currents have started changing the charge on C_{hold} 8-75 with the attendant drift of V_{REF} 8-71/

Figure 9a illustrates a DFSK data detector 9-77 which overcomes the limitations of prior detectors. Both comparator inputs 9-78 and 9-79 are DC biased identically by means of R1 9-80 and R2 9-81 through R3 9-82 and R4 9-83 to V_{REF} 9-88 and the V_{QUAD} 9-84 DFSK signal illustrated in Figure 9b is AC coupled to the inverting comparator 9-85 input (V_{QUAD} 9-78) through capacitor C3 9-86. C2 9-87 bypasses or filters V_{REF} 9-88 from the AC signals at both inputs 9-78 and 9-79 of the comparator 9-85 passed to V_{REF} 9-88 through R3 9-82 and R4 9-83. R3 9-82 (from the DFSK V_{QUAD} 9-78 signal) and through R4 9-83 (from the V_{+REF} 9-79 noninverting input of comparator 9-85).

Figure 9b illustrates the nature of DFSK V_{QUAD} signals as they are detected by a quadrature detector. Differential frequency signals may be characterized by a short decrease in frequency to represent a falling edge (or high to low logic level change) in data. The term "differential frequency shift key" arises because the DFSK V_{QUAD} data looks like the derivative or differential of the FSK data described in Figures 6, 7 and 8. A DFSK modulation technique will be described in Figure 11. Figure 9b represents the signals at the inverting input (V_{QUAD} 9-78), noninverting input V_{+REF} 9-79 (the dashed lined) and data output of data slicer comparator 9-85 of Figure 9a. The inverting input signals V_{QUAD} 9-78 comprise a DC component equal to V_{REF} 9-88 and an AC component equal to V_{QUAD}'s DFSK component. Thus, at t0 the carrier frequency is f_0, V_{QUAD} 9-84 is at its median level, and V_{QUAD} 9-78 is at V_{REF} 9-88, its DC level provided by R3 9-82. AT t1 to t4 a DFSK falling data edge signal is detected as a positive pulse at V_{QUAD} 9084 and transferred through C3 9-86 to V_{QUAD} 9-78. Meanwhile, at t0 V_{REF} 9-79 is more positive than V_{REF} 9-88 due to the voltage divider action of hysteresis resistor R_H 9-89 with R4 9-83 and the logic level 1 data output voltage of the comparator 9-85. R_H 9-89 and R4 9-89 and R4 9-83 are judiciously selected to provide sufficient

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hysteresis to permit noise reduction of half the V_{QUAD} 9-84 peak signal level or 200 mV (since the peak value of V_{QUAD} 9-78 is about 400 mV). Therefore, when the V_{QUAD} 9-78 signal rises at t2 to V_{+REF0}, comparator 9-85 output state toggles to logic 0 with a corresponding change in V_{-REF} 9-79 to V_{+REF}. At t4 V_{QUAD} 9-78 returns V_{REF} 9-88 until t5, when a negative going V_{QUAD} 9-78 voltage (1 level data edge) DFSK transition starts. At t6 V_{QUAD} 9-78 drops to the V_{-REF1} voltage, the comparator 9-85 data output again toggles from 0 to 1 logic level with a corresponding to a change in V_{+REF} 9-79 to V_{+REF0}, where the reference input of the comparator waits until the next 0 level t1 to t4 type V_{QUAD} 9-78 signal is detected.

Because the DFSK signal defines the edges of each data level change, there is no temperature drift or data composition component that foils the operation of the comparator 9-85 DATA output 9-90, as illustrated in Figure 9c. The time constant of C3 9-86 and R3 9-82 is selected to be long enough to pass DFSK V_{QUAD} to the inverting input of comparator 9-85 (V_{QUAD} 9-78) but short enough to reject short term DC drifts present V_{QUAD} 9-84 due to data composition changes and to adjust quickly to the transient DC change from noise to preamble exhibited upon initial receipt of a packet. The time-constant value (τ=R3 9-82 x C3 9-86) can be about 5 μs for data rats in the megabit range. Hysteresis in the comparator circuit (provided by R_H 9-89 and R4 9-83) provides the same noise rejection characteristics as ordinary FSK and in the instant circuit may be 400 mV total for an 800 mV peak-to-peak V_{QUAD} 9-84 signal. (input offset drifts in comparators are typically below the millivolt level, while signal levels are hundreds of millivolts.) Typically, in the current best mode of the invention C3 9-86 is 470 pF; C2 9-97 is .1 μF; R1 9-80 is 1 kΩ; R2 9-87 is 1 kΩ; R3 9-82 is 10 kΩ; R4 9-83 is 33 kΩ; and R_H 9-89 is 470 Ω.

A further modification to the DFSK demodulation scheme provides for peak detection of the demodulated data pulses, since the time location of DFSK peaks tend to be more stable with variation in real media amplitude and phase attenuation characteristics. A peak detector is illustrated in Figure 9d. The peak detector consists of two sets of analog voltage comparators 9-91, 9-92, 9-93 and 9-94, one set of which (9-93 and 9-94) detects the level of the peaks of the demodulated data signal (through C3 9-95 and R3 9-96) and another set of which (9-91 and 9-92) detects the zero-slope of the peaks by differentiating the demodulated signal (through C5 9097 and R5 9-98). The time constant of C3 9-95 and R3 9-96 is selected to be longer than the data time constant (τ = 470 pF x 10 kΩ · 4.7 μs), while the time constant of C5 9-97 and R5 9-98 (τ = 68 pF x 1 kΩ = 68 ns) is selected to be short with respect to the raw data waveform V_{QUAD} Bias and reference levels for the comparators are provided by R1 9-99, R2 9-100, R6 9-101, R7 9-102, R8 9-103, and R9 9-104 providing the upper and lower peak detection reference voltages DU 9-105 and DL 9-106 for AC-coupled data VD, permitting peak detection to be performed by comparators 9-93 and 9-94. R6 9-101 and R7 9-102 provide ZU 9-107 and ZL 9-108, the upper and lower references for zero slope detection by comparators 9-91 and 9-92. The open collector outputs of the comparators require pull-up resistors (R11 9-109, R12 9-110, and R13 9-111) and may be connected in a wired-NOR configuration, which for comparators 9-91 and 9-92 provides a 1 output for zero-slope signals. The peak and zero-slope outputs are then logically ANDed by NAND gates 9-112 and 9-113 to provide trigger pulses corresponding to the positive and negative peaks of the demodulated data signal. The positive peak pulse triggers the "0" state of the RS flip flop comprising gates 9-114 and 9-115 while the negative peak pulse triggers the "1" state of said RS

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flip flop. In the current best mode of the invention the components have the following values: C5 9-97 is 68 pF; C2 9-116 is .1 μF; C3 9-95 is 470 pF; R1 9-99 is 1 kΩ; R2 9-100 is 1 kΩ; R3 9-96 is 10kΩ; R5 9-98 is 1kΩ; R6 9-101 is 8.2Ω; R8 9-103 is 75Ω' R9 9-104 is 75Ω; R11 9-109 is 470Ω; R12 9-110 is 1kΩ; and R13 is 1kΩ. It should be noted that digital signal processing hardware and firmware can provide many of the demodulation and data detection functions described herein, but at the higher cost of DSP chips and A/D converter interfaces.

Figure 10 compares the frequency spectrum of FSK and DFSK modulation and illustrates the beneficial bandwidth consumption characteristic of DFSK over FSK. AT low data rates (Figure 10a) FSK is designed to produce a fixed shift or deviation determined by the two frequencies assigned to the '1' and '0' data bits, the deviation (difference) of which is determined by the demodulator transfer function or curve (illustrated in Figure 10 as f_0 and f_1). The power of the FSK transmission is divided equally (for data with equal averages of 1's and 0's) between the two frequencies. At high data rates (Figure 10b) FSK exhibits sidebands spaced from the center f_c. At high data rates (Figure 10d) DFSK exhibits sidebands of the same width as with FSK, but the magnitude of the sidebands is suppressed by as much as 10dB compared to FSK, requiring less filtering of transmitter sidebands and better propagation through receiver filters.

DFSK modulation of a carrier is easily implemented with a 5-state digital state machine (driven by a 4 x f_c clock) as illustrated in Figure 11a, because (1) only one carrier/clock frequency need be generated or synthesized (as opposed to two with FSK) and (2) the rising and falling edges of the data are used to skip or add a state to the state machine, producing a higher or lower differential frequency shift, respectively. In the case of the normal unmodulated carrier f_c (with 50/50 duty cycle), the state sequence for one carrier cycle is 1,2,3,4 with states 1 and 2 producing a high level and 3 and 4 producing a low level. A falling data edge '0' causes the state machine to add a fifth state 2' between states 2 and 3, producing the sequence of 1,2,2',3,4 and resulting in a lower differential frequency shift corresponding to falling edge '0'. Similarly, a rising data edge '1' causes the state machine to skip state 2, producing the sequence 1,3,4 and resulting in a higher differential frequency shift corresponding to rising edge '1'. Thus, the DFSK state machine and modulation technique effectively has 3 symbols: (1) the rising edge of data, (2) the falling edge of data, and (3) no data edges or state changes, which further distinguishes DFSK from other modulation techniques (FSK, QFSK, PSK, QPSK, etc.) that have 2 or 4 or more (even numbers) symbols, but not 3. It should be noted here that the 5-state digital state machine in practice employs more states to permit setup, synchronization and timing of data with carrier. Also, the assignment of data logic states to higher or lower differential frequency shifts may be reversed from the example herein without changing the substance of the invention.

Additional state machine modifications illustrated in Figure 11b permit selection of alternate data rates while keeping carrier frequency fixed by selecting a preset number n of carrier cycles per bit. A presetable divide by n counter may be added to the state machine to provide a data clock which is presetable submultiple of carrier frequency. Thus, a 6 MHz carrier would provide bit rates corresponding to n as follows: 1200 kbps for n=5, 600 kbps for n=10, 300 kbps for n=20, and 150 kbps for n=40. Selection of bit rate without changing carrier frequency by system controllers permits negotiation of bit rate for servicing a variety of device types on a network

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as well as accommodating varying power line propagation characteristics. For example, a lowest cost light switch node may be implemented with 150 kbps monolithic filters and no data rate negotiability, while a moderate price point printer node may be operated at 1200 kbps with discrete wideband filters and have negotiability designed into its controller. By initiating operation of the network at 150 kbps, the n for the printer and the switch would start at 40, but as soon as the device type and node address were broadcast for a printer node, the bit rate would be negotiated upward from n=40 to n=20 until n=5 or until the bit error rate became unacceptable for the conditions of the power line medium at that time, whereupon the n and corresponding data rate would back off to an acceptable selection.

An addition advantage of the DFSK modulator is that the state machine can be configured and instructed by a data controller to produce special DFSK characters for control or compression purposes. For example, two lower differential frequency shifts could be executed in sequence to represent a string of 1's while two higher differential frequency shifts in sequence could represent a string of 0's. This feature is not possible with FSK. The state machine has no limitations on its agility regarding which states it adds or skips, as instructed. The demodulator data slicer would require some additional comparator(s) and logic/circuitry to detect successive DFSK pulses of like polarity.

An additional modification to the carrier generation and modulation state machine includes increasing the number of states to permit Multiple DFSK techniques. For example, subdividing the original 5 states by 2 doubles the number of states to 10 half-states (with a corresponding doubling of clock frequency to 8 x f_c) and permits increasing the number of symbols by 2 by skipping or adding 1 or 2 half-states. Corresponding modifications to the receiver demodulator are required to detect the differing responses to the 1 and 2 half-state symbols. Since a 1 half-state shift produces half the differential frequency shift of a 2 half-state shift, a quadrature detector produces pulses of half the amplitude for the 1 half-state shift with reference to a 2 half-state shift, which is the normal shift for standard DFSK.

A further modification to the carrier generation and modulation state machine includes modulation shaping methods that more consistently define data edges at high bit rates, which modifications either prefix or append to data symbols (a) single whole shifts or (b) 1 or 2 half-state shifts which precompensate the quadrature detector's analog data output waveform for more accurate data slicing of each data bit sequence/combination.

DFSK, while discussed in this specification, primarily in a PLC application has many similar applications in other electronic communication system, including but not limited to: RF, wired, telephone line and the equivalent. Moreover, while this discussion of DFSK implies a workstation computer device, this technology can be applied, and should be considered within the scope of this patent, to any other electronic devices with communication capabilities, including but not limited to controllers, personal computers, fax machines, printers and telephonic systems.

Figure 12 illustrates the improvement in data bit timing accuracy achieved if the data rate is synchronized with the carrier frequency f_c and clock. Figure 12 shows two data bits of identical length or rate, XMIT DATA and XMIT DATA', but shifted in phase in reference to the CARRIER modulator. XMIT DATA falling edge X0 (and X0') and rising edge X1 meet the set up windows (low state) for the modulator state machine, while the rising edge X1'

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of XMIT DATA misses the setup window of the modulator state machine, delaying execution of the modulation for rising edge 1 to 1', to the next CARRIER cycle and producing a corresponding time delay/shift in rising edge RCVR DATA R1 vs. R1'. Received data bit width changes of 1 carrier cycle produce significant data errors at the high data rates of the instant invention, while prior system data rates, being at least an order of magnitude lower, have not observed this error source as significant. It should be especially noted that both rising and falling edges of data are sensitive to data synchronization with the carrier modulator and that the variation in bit width data error is especially exacerbated by data rates that are not related to the carrier frequency by an even multiple of carrier cycles. Therefore, synchronization of both data rate and phase with the carrier modulator eliminates synchronization granularity/jitter in the modulated carrier, enabling high data rates.

Another improvement that increases the reliability of detecting/receiving the bits in each byte provides a realignment bit at the end of each byte. The realignment bit resynchronizes the receiver's deserializer sampling clock with each incoming data byte to prevent clock timing skews between the transmitter data clock and the deserializer (receiver) clock, permitting low-cost clock references. This differs significantly from other packet transmission schemes such as Ethernet, which employ 20,00000 MHZ (1ppm) accurate clocks for tracking a 1500-byte-long packet. While the realignment bit improvement is similar in concept to RS-232 start and stop bits, it differs significantly from RS-232 in that (1) the polarity alternates from that of the last data bit of the byte to further distinguish its edge from the last bit, and (2) only one realignment bit per byte is required, effectively reducing the overall data rate throughput by only 11% (as compared with 25% for RS-232). This improvement permits reliable data transfers at higher data rates well beyond the 11% hit as well as increasing the maximum packet size, while still permitting the use of low-cost clock references/crystals.

Figure 13 illustrates another limiting characteristic of prior techniques using RSSI detection schemes and protocols based on RSSI signals. Figure 13 shows an MC13158 receiver data book chart for the RSSI response. In networks involving RF carrier transmissions, each node has a transmitter and a receiver, the operation of which is determined by the fundamental protocol of the network (client-server, peer-to-peer, etc.). For data transmission, only one transmitter at a time is permitted to be active on the medium and then only when the respective node has data to send. When not transmitting, each node's receiver is active, producing valid data or spurious noise depending on whether a valid transmission is present on the medium. Prior network arbitration protocols have used the presence or absence of carrier as detected by receiver RSSI circuits to determine (1) that the data output of a receiver is valid or spurious, or (2) that the medium is clear of other transmissions, permitting a node's transmitter access to the medium. In each instance the response time of the RSSI circuit limits the responsiveness of system protocols as illustrated in Figure 13. The response time exceeds 4 μs for rise time t_r (presence of carrier) and exceeds 25 μs for fall time t_f (absence of carrier) for stronger signals, varying down to 6 μs for weak signals. Since the length of a byte at 2 Mbps is 4 μs, the six times variation between rise and fall times and the long length of the fall time (exceeding 6 data bytes) create bandwidth consuming protocol delays for send/receive and intergap spacing operations when the RSSI signal is used to arbitrate transmissions.

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Then there are two other problems related to the nose level of the medium, and particularly that of the power line: (1) medium noise pulses trigger counterfeit RSSI signals and false arbitration attempts and (2) the signal-to-noise ratio on the medium changes from one environment to another and at different times of the day, making it difficult for an RSSI comparator circuit to adjust its reference to remain sensitive to normally attenuated signals while ignoring false triggers.

To overcome RSSI technique and circuit limitations and improve reliability of power line network arbitration the present preferred embodiment of the invention avoids the use of the RSSI signal altogether, relying instead on (1) validation of distinct data preambles to test for adequate signal-to-noise ratios and (2) special modulation symbols called FSK ACK (for Frequency Shift Key Acknowledgment) for permitting multiple nodes to acknowledge (respond) simultaneously to group polls by a network master. If the signal to noise ratio is at least 12 dB, a favorable bit error rate results in detection of valid packet preamble and start byte, packet length byte, unique node address, data payload and CRC, which together assure the reception of an accurate packet. Distinctive preamble and start bytes are chosen to permit competent comparison logic to distinguish preambles from power line noise. For example, sending a series of alternating ones and zeros (AAH) followed by a 31H (i.e., 1010101010010001) produces an acceptably unique combination for differentiating the start code from noise. Packet length bytes also provide reliable anticipation of the packet length and the end of the packet for arbitrating the next transmission by other network nodes with minimal intergap spacing. Similarly, the special FSK ACK packet described in Figure 15 permits discrimination against normal data as well as power line noise.

In relation to the detection of special FSK ACK symbols, Figure 14a illustrates several improvements over prior techniques, which are achieved by substantially increasing the IF frequency: (1) the demodulator linear frequency range is doubled, dramatically decreasing the sensitivity to the AC coupled DFSK data comparator to the temperature coefficient and mechanical tuning drifts; (2) the FSK ACKnowledgment signal detection is more robust by setting the corresponding comparator reference near a demodulator output "rail" which is also further from the DFSK carrier and noise; and (3) the IF filter is designed for flatter pass band and sharper skirts with substantially less expensive components. Extending the linear range of the quadrature demodulator transfer function (for IF frequency vs. V_{QUAD} voltage out) permits a wider range of temperature coefficient/mechanical drift and tolerance on parts from the transmitter to the receiver. Extending the frequency range of the demodulator rails also extends the FSK ACK frequency range, which is judiciously placed near or onto a rail, providing a more robust deviation in FSK ACK frequency from the DFSK carrier to help discriminate against noise in the carrier range. A DC coupled comparator (FSK data slicer) may then be employed because the rail tends to act as a limiter on V_{QUAD} as it responds to the FSK ACK frequency, permitting the FSK ACK comparator reference to be placed in the linear range next to a rail with sufficient margin to accommodate temperature coefficient drifts and noise, as illustrated in Figure 14b. Another reason the FSK comparator works well for FSK ACK detection is that the data rate of an FSK ACK signal is designed to be much lower than for DFSK data. Placing the IF at a substantially higher frequency also provides the advantage of making IF filter design more practical for obtaining wider and flatter pass bands (and sharper skirts for rejection of out of band interference) with economical commercial components.

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Figure 15 illustrates how DFSK permits the compatible use of FSK to produce special characters that may be used for group acknowledgment of requests for status of slave devices in a network. At t1 to t3 normal DFSK operation at the end of a packet is illustrated with corresponding DFSK DATA. During t3 to t4 the carrier of the master drops and the noise level of the medium creates false DATA which is rejected as invalid data by the receive data controller because it does not meet the start of packet requirements for a data packet nor does it meet the FSK ACK requirements for an ACK packet. But at t4 an FSK ACK packet begins in which the unmodulated DFSK carrier is employed as one frequency f0 for a byte (t4 to t5) and the second FSK ACK frequency acts as f1 for several bytes (t5 to t6). From t6 to t7 the ACK packet returns to f0 for the length of a byte, following which carrier transmission ceases and the data and ACK signals detect the noise level of the medium at t8 to t11. No realignment bit is required in the ACK packets. By reducing the data rate (from bits to bytes or to the lowest bit rate of the network) of the ACK protocol, at least two transmissions of equal strength may be detected simultaneously, which can occur when several remote devices in a network group respond simultaneously to a group poll. Frequencies must be within 10 kHz, which for a 5 MHZ carrier is a reasonable 0.2% (2000 PPM). Commercial crystals are available with 50 ppm tolerances at low cost. It may also be noted that the judicious use of the FSK ACK symbols and protocol avoids the use of the unreliable RSSI signal for group ACKs as described herein.

Because the FSK, ACK signal permits discrimination against normal data as well as medium noise, this advantage permits an FSK ACK packet to be employed, modified or unchanged, for other signaling applications in a network or control system. For example, in a master/slave network, the FSK ACK could provide an interrupt when a slave node requires the services of a master, which reduces polling frequency. The slave node's own address could be appended to the end of the DFSK trailer on the FSK ACK packet, reducing polling operations. Or in a peer to peer system, the FSK ACK could be used to notify other users of its intent to broadcast on the medium or to pass tokens. Changing the length of the FSK portions of the FSK ACK packet could provide control or identification data to other network devices.

It is to be understood that the above described embodiments of the invention are merely indicative of the inventors' current best mode of the invention and are illustrative of numerous and varied other embodiments which may constitute applications of the principles of the invention. Such other embodiments may be readily devised by those skilled in the art without departing from the spirit or scope of this invention and it is our intent that they be deemed within the scope of our invention.

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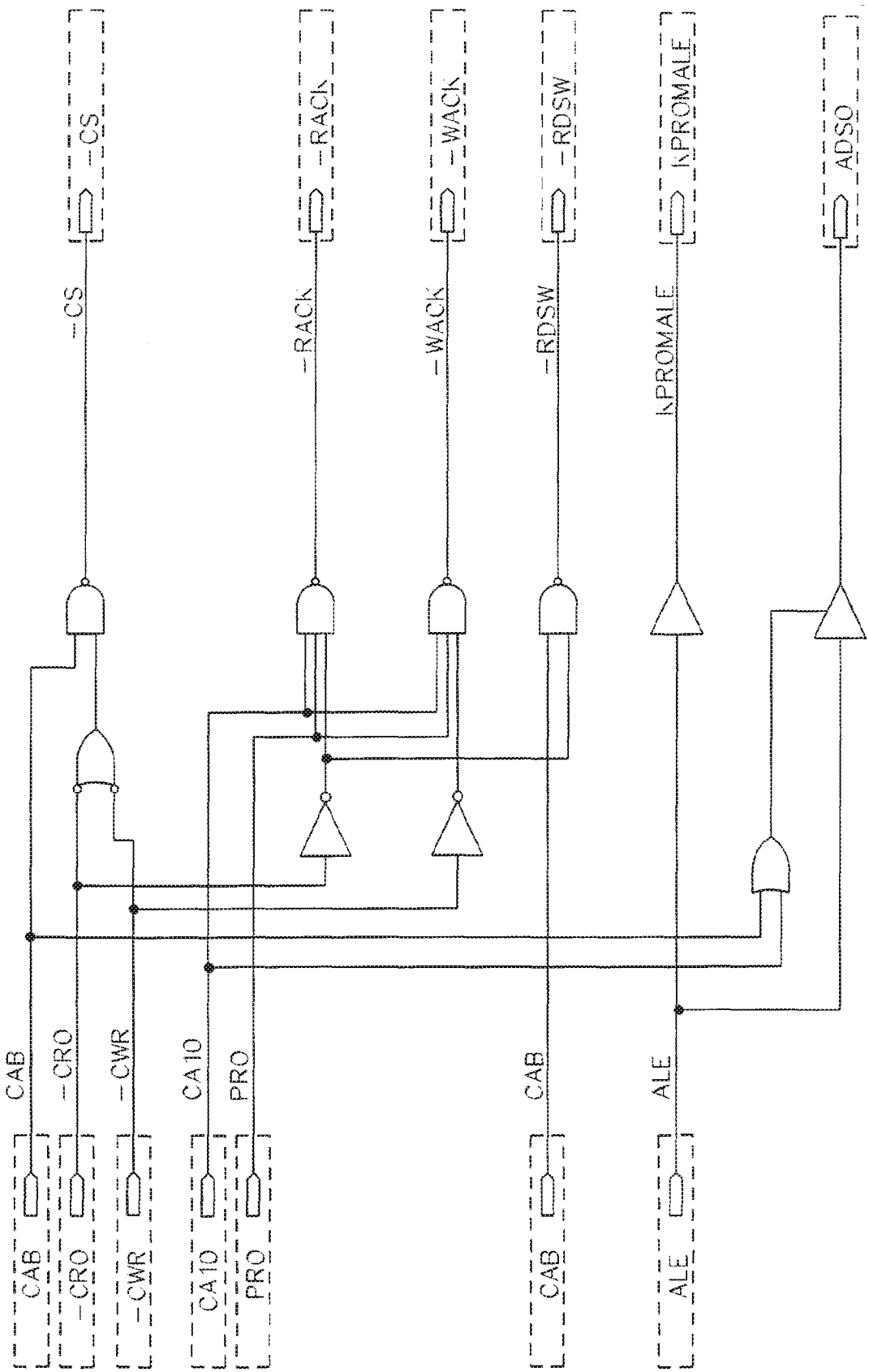

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ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
1	C	rackl	[,130]		130	<,0> <,0>	83902A Read Strobe to -ACK Low (2*bcyc + 30) only 2 wait states allowed
2	C	rackh	[,30]		30	<,0>	83902A Read Strobe to -ACK High
3	C	ackdv	[,55]		55	<,0>	83902A Acknowledge Low to Data Valid
4	C	rdz	[15,70]	15	70	<54.67,0.33>	83902A Read Strobe to Data TRI-STATE
5	C	ww	[50,]	50		<0,>	83902A Write Strobe Width from -ACK
6	C	rwds	[20,]	20		<0,>	83902A Register Write Data Setup
7	C	rwdh	[21,]	21		<0,>	83902A Register Write Data Hold
8	C	wackh	[,30]		30	<,0>	83902A Write High to -ACK High
9	C	wackl	[,130]		130	<,0>	83902A Write Low to -ACK Low
10	C	rsrs	[10,]	10		<0,>	83902A Register Select to Read Setup
11	C	rsrh	[0,]	0		<2.77,>	83902A Register Select Hold from Read
12	C	rswh	[0,]	0		<1.87,>	83902A Register Select Hold from Write
13	C	rsws	[15,]	15		<0,>	83902A Register Select to Write Setup (assumes ADS0 high when RA lines)
14	C	bch	[20,]	20		<5,>	83902A Bus Clock High Time
15	C	bcl	[20,]	20		<5,>	83902A Bus Clock Low Time
16	C	asds	[,30]		30	<,0>	83902A Address Strobe to Data Strobe (bcl+10)
17	C	bcrl	[,43]		43	<,0>	83902A Bus Clock to Read Strobe Low
18	C	bcrh	[,40]		40	<,0>	83902A Bus Clock to Read Strobe High
19	C	avrh	[132,]	132		<0,>	83902A Address Valid to Read Strobe High

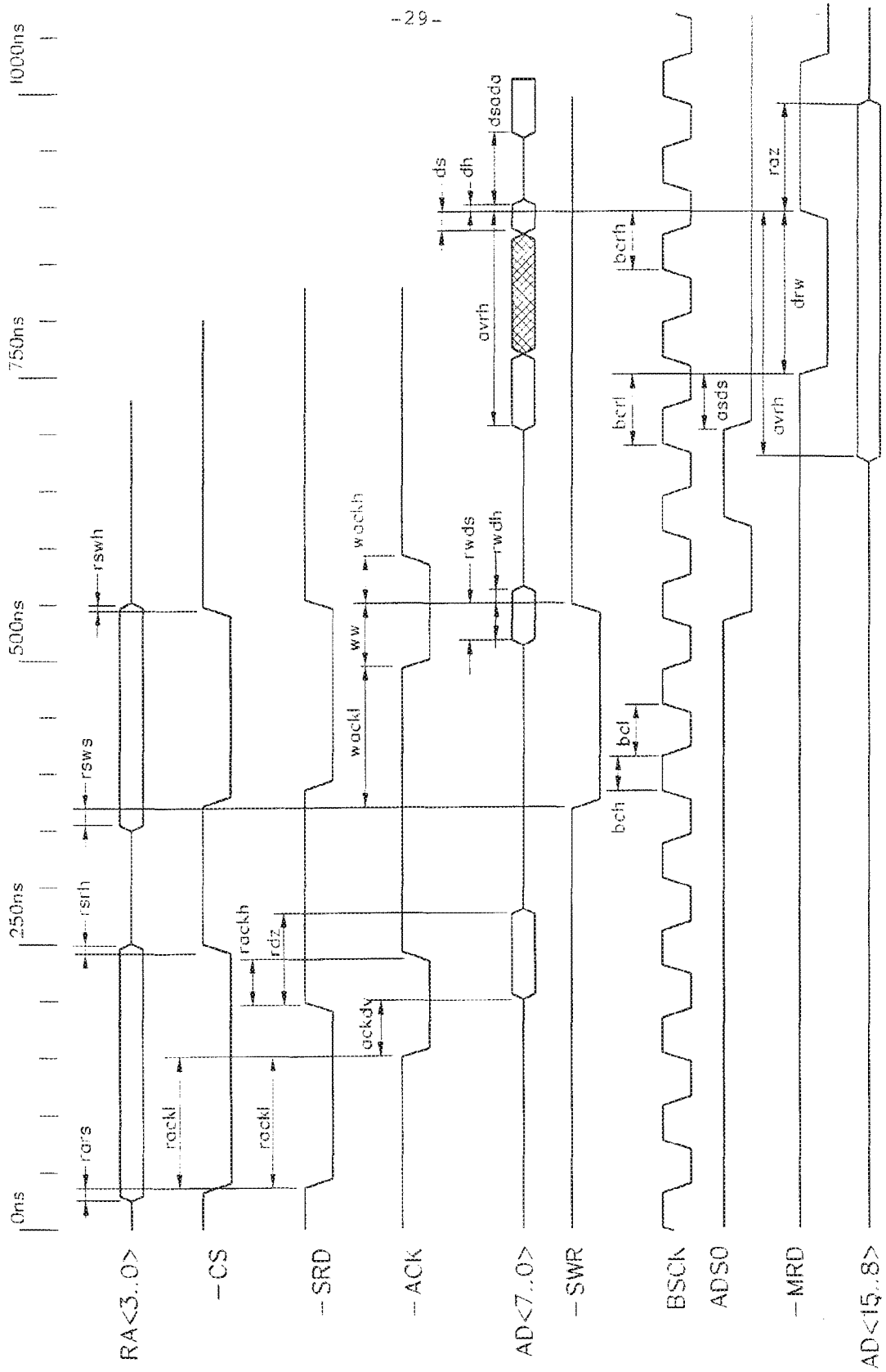
ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
20	C	avrh	[132,]	132		<0,>	83902A Address Valid to Read Strobe High
21	C	ds	[22,]	22		<0,>	83902A Data Setup to Read Strobe High
22	C	drw	[85,]	85		<12,>	83902A DMA Read Strobe Width Out
23	C	dh	[0,]	0		<3,>	83902A Data Hold from Read Strobe High
24	C	dsada	[40,]	40		<0,>	83902A Data Strobe to Address Active
25	C	raz	[90,]	90		<0,>	Memory Read High to Address TRI-STATE

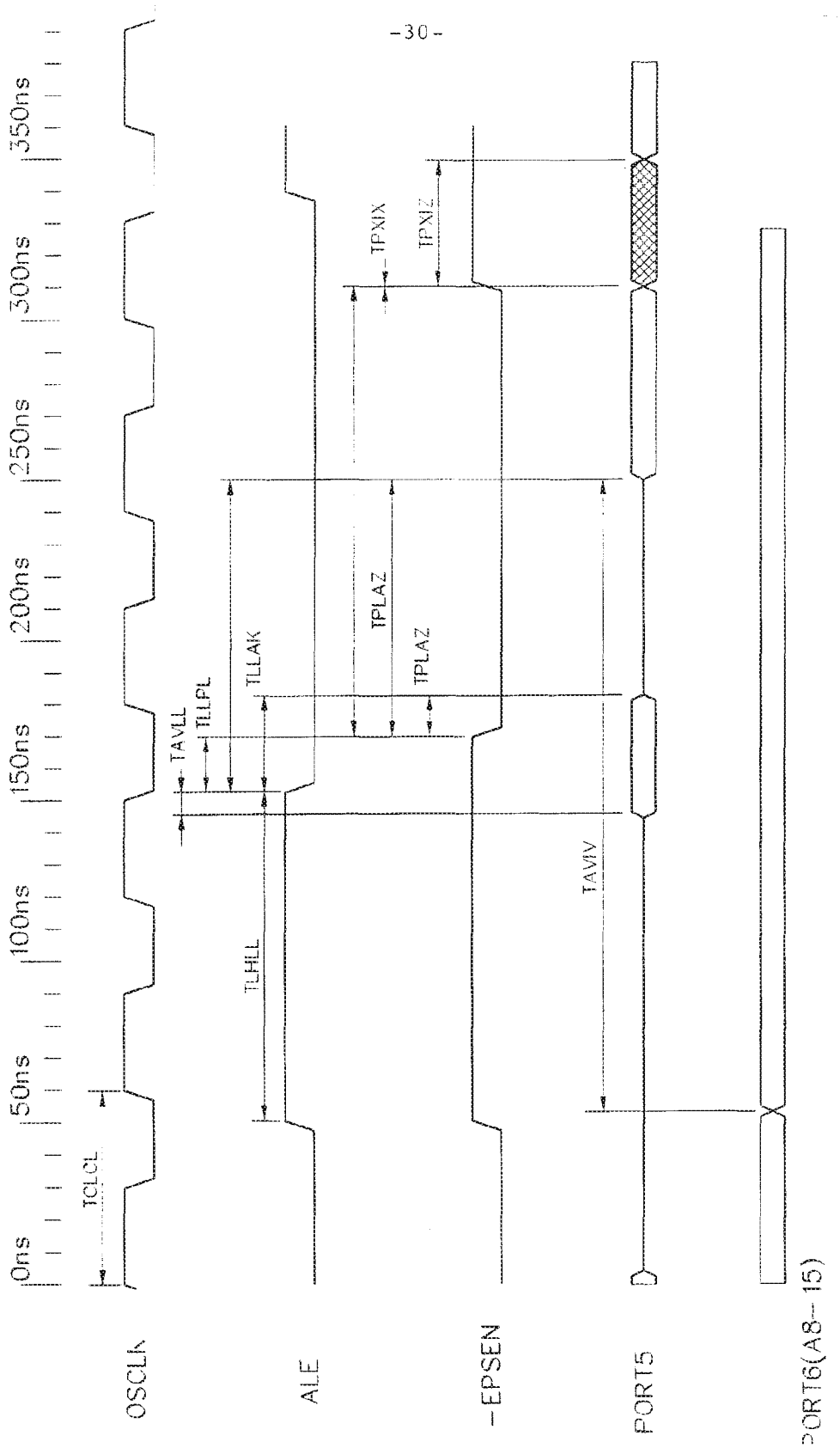
ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
1	C	TLHLL	[min(((2*T CLCL)-40)),]	81.21		<21.49,>	8X152 ALE PULSE WIDTH
2	C	tLL	[50,]	50		<52.70,>	8764 Chip DeSelect Width (87C64-1)
3	V	TCLCL	[60.61,]	60.61			8X152 OSCILLATOR CLOCK PERIOD
4	C	TCLCL	[60.61,]	60.61		<0,>	8x152 OSCILLATOR CLOCK PERIOD
5	C	TAVLL	[min((TCLCL-55)),]	5.61		<0,>	8X152 Address Valid to ALE Low
6	C	tAL	[25,]	25		<-19.39,>	8764 Address to -CE Latch Set-up
7	C	TLLAX	[min((TCLCL-35)),]	25.61		<5,>	8X152 Address Hold After ALE Low
8	C	tLA	[30,]	30		<0.61,>	8764 Address Hold from -CE Latch
9	C	TLLIV	[,min(((4*T CLCL)-100))]		142.42	<,45.41>	8X152 ALE Low to Valid Instruction In
10	C	tACL	[,150]		150	<,52.99>	8764 CE Latch Access Time
11	C	TLLPL	[min((TCLCL-40)),]	20.61		<0,>	8X152 ALE Low to -EPSEN Low
12	C	tCOE	[30,]	30		<-9.39,>	8764 ALE/-CE to Output Enable
13	C	TPLPH	[min(((3*T CLCL)-45)),]	136.82		<0,>	-EPSEN Pulse Width

ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
1	C	TLHLL	[min(((2*T CLCL)-40)),]	81.21		< 21.49, >	8X152 ALE PULSE WIDTH
2	V	TCLCL	[60.61,]	60.61			8X152 OSCILLATOR CLOCK PERIOD
3	C	TCLCL	[60.61,]	60.61		< 0, >	8x152 OSCILLATOR CLOCK PERIOD
4	C	TAVLL	[min((TCLC L-55)),]	5.61		< 0, >	8X152 Address Valid to ALE Low
5	C	TLLAX	[min((TCLC L-35)),]	25.61		< 5, >	8X152 Address Hold After ALE Low
6	C	TLLIV	[,min(((4*T CLCL)-100))]		142.42	< ,45.41 >	8X152 ALE Low to Valid Instruction In
7	C	TLLPL	[min((TCLC L-40)),]	20.61		< 0, >	8X152 ALE Low to -EPSEN Low
8	C	TPLPH	[min(((3*T CLCL)-45)),]	136.82		< 0, >	-EPSEN Pulse Width
9	C	TPLIV	[,min(((3*T CLCL)-105))]		76.82	< ,0.4 >	8X152 -EPSEN Low to Valid Instruction In
10	C	TPLAZ	[,10]		10	< ,0 >	8X152 -EPSEN Low to Address Float
11	C	TPXIX	[0,]	0		< 0, >	8X152 Input Instruction Hold After -EPSEN
12	C	TPXIZ	[,min(((5*T CLCL)-25))]		278.03	< ,242.43 >	8X152 Input Instruction Float After - EPSEN
13	C	TAVIV	[,min(((5*T CLCL)-105))]		198.03	< ,0 >	8X152 Address to Valid Instruction In

ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
1	C	TLHLL	[min(((2*TCLCL)-40)),]	81.21		<0,>	8X152 ALE PULSE WIDTH
2	V	TCLCL	[60.61,]	60.61			8X152 OSCILLATOR CLOCK PERIOD
3	C	TCLCL	[60.61,]	60.61		<0,>	8x152 OSCILLATOR CLOCK PERIOD
4	C	TAVLL	[min((TCLCL-55)),]	5.61		<0,>	8X152 Address Valid to ALE Low
5	C	TLLAX	[min((TCLCL-35)),]	25.61		<0,>	8X152 Address Hold After ALE Low
6	C	TLLDV	[,max(((8*TCLCL)-150))]			<,>	8X152 ALE Low to Valid Data In
7	C	TAVDV	[,max(((9*TCLCL)-165))]			<,>	8X152 Address to Valid Data In
8	C	TWHLH	[min((TCLCL-40)),max((TCLCL+40))]	20.61		<0,>	-RD or -WR High to ALE High
9	C	TLLWL	[min(((3*TCLCL)-50)),max(((3*TCLCL)	131.82		<0,><0,>	8X152 ALE Low to -RD or -WR Low
10	C	TRLRH	[min(((6*TCLCL)-100)),]	263.64		<0,>	8X152 -RD Pulse Width
11	C	TRLDV	[,max(((5*TCLCL)-165))]			<,>	8X152 -RD Low to Valid Data In
12	C	TRHDZ	[,max(((2*TCLCL)-70))]			<,>	8X152 Data Float after -RD
13	C	TRLAZ	[,0]		0	<,0>	8X152 -RD Low to Address Float
14	C	TRHDX	[0,]	0		<0,>	8X152 Data Hold after -RD
15	C	TAVWL	[min(((4*TCLCL)-130)),]	112.42		<25.01,>	8X152 Address to -RD or -WR Low

ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
16	C	TWLWH	[min(((6*TCLCL)-100)),]	263.64		<0,>	8X152 -WR Pulse Width


0ns
250ns
500ns
750ns
1000ns
RA<3..0>
-CS
-SRD
-ACK
AD<7..0>
-SWR
BSCK
ADS0
-MRD
AD<15..8>
rars
rackl
rackh
rdz
ackdy
rsth
rsws
rswh
wackl
wackh
ww
rwds
rwdh
ds
dh
dsada
avrh
bcrh
bcrl
asds
raz
drw
bcl
bch



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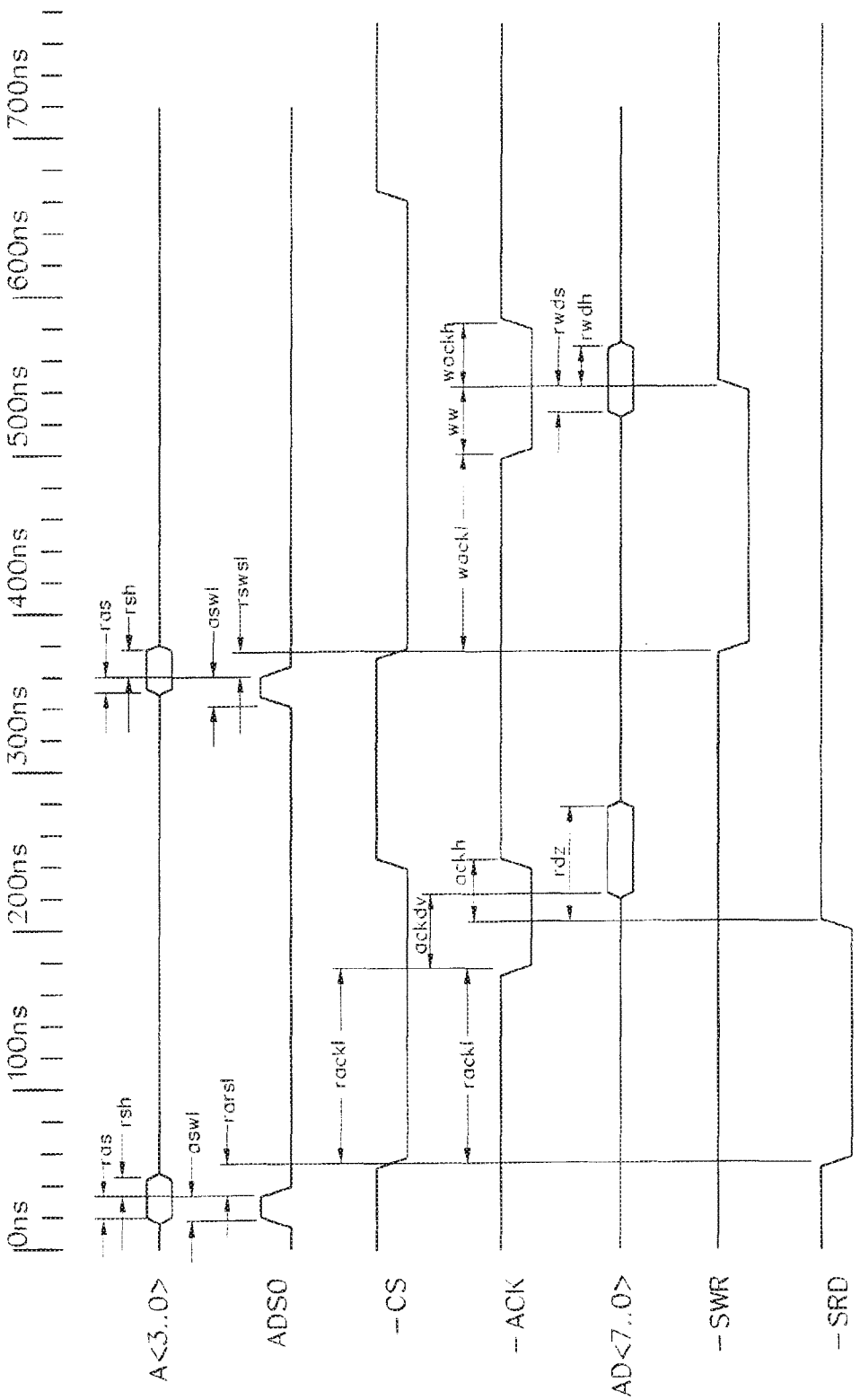
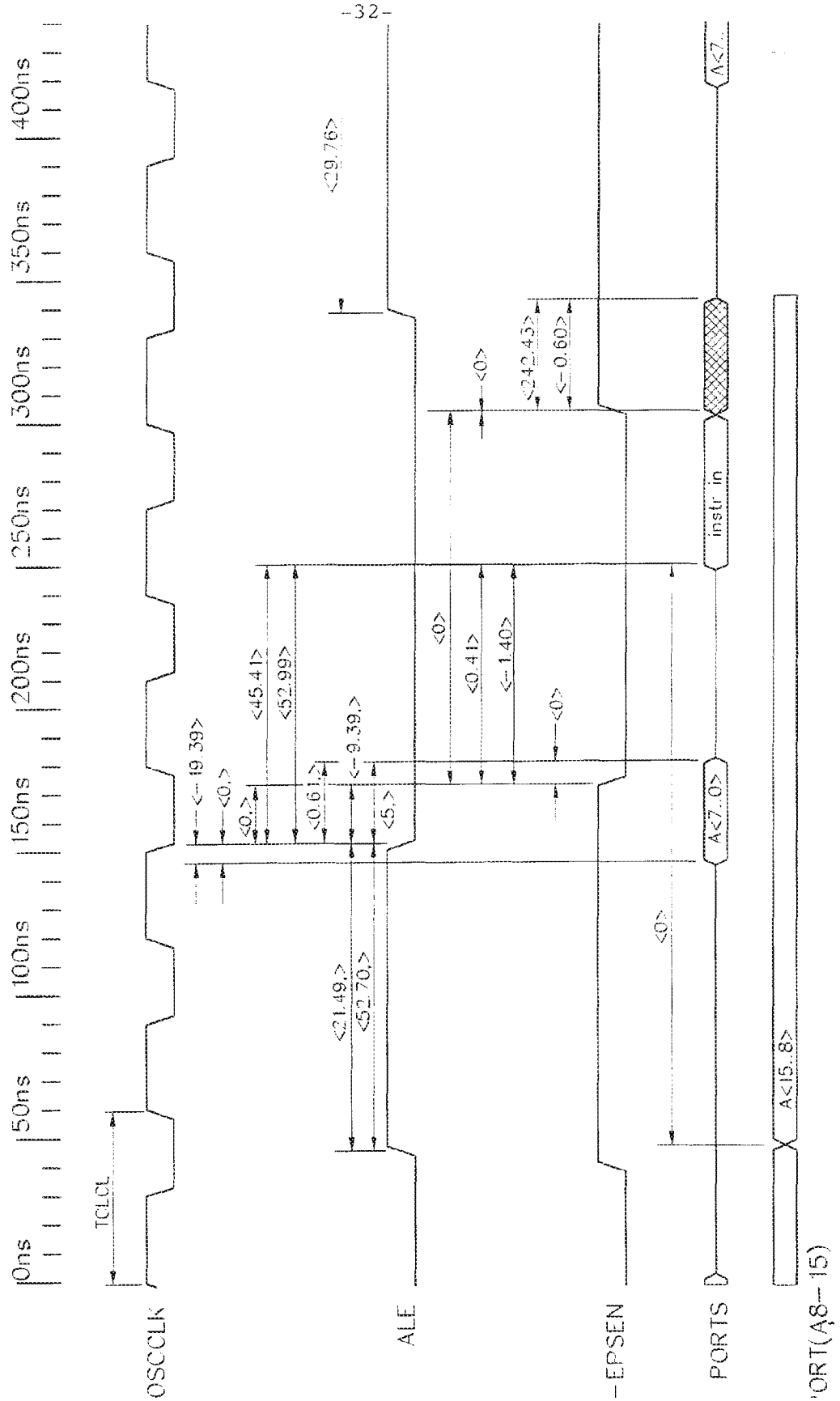
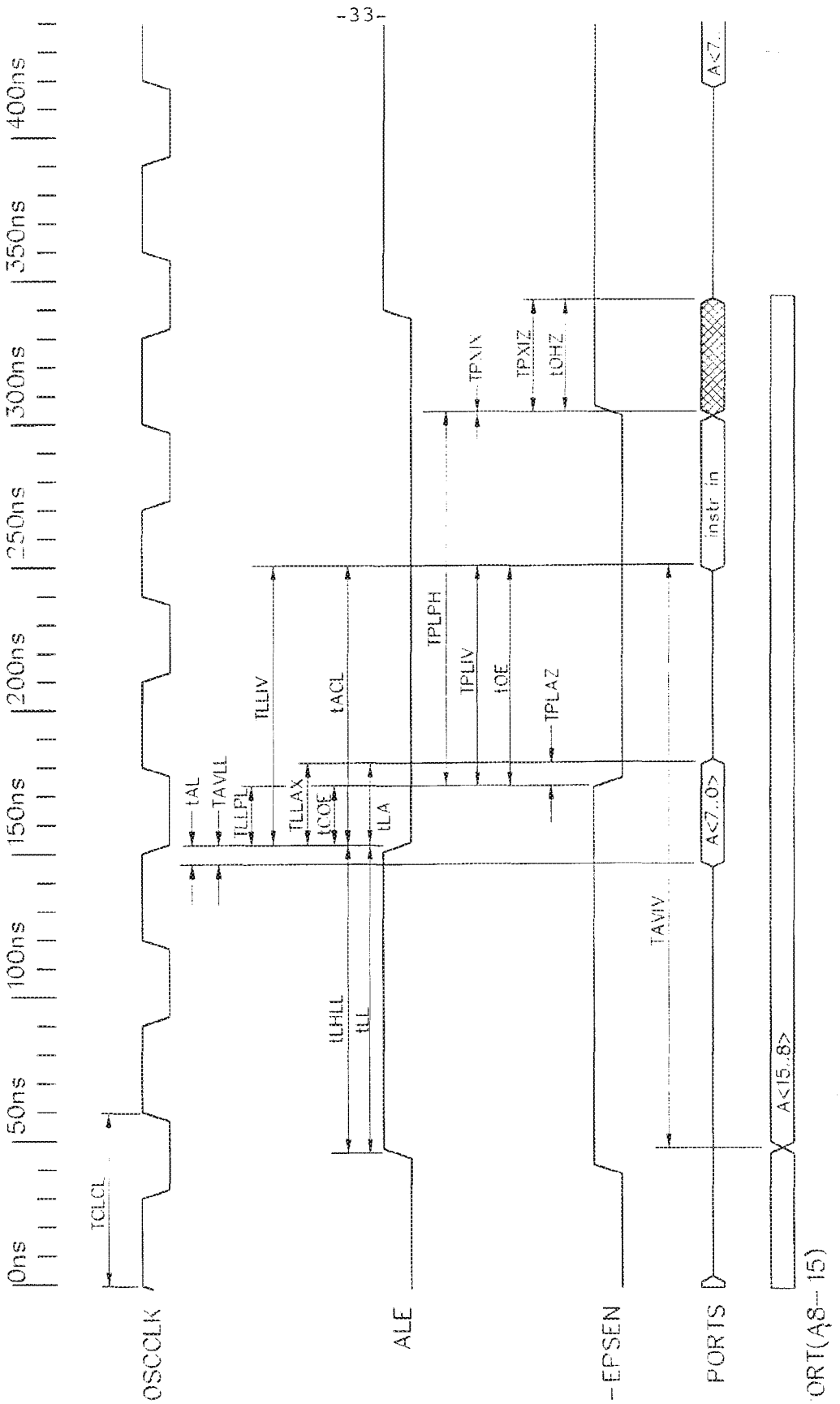

0ns
100ns
200ns
300ns
400ns
500ns
600ns
700ns
ras
rsh
aswl
rarsl
rackl
ackdy
ackh
rdz
wackl
ww
wackh
rwds
rwdh
rswsl
A<3..0>
ADS0
-CS
-ACK
AD<7..0>
-SWR
-SRD



SUBSTITUTE SHEET (RULE 26)



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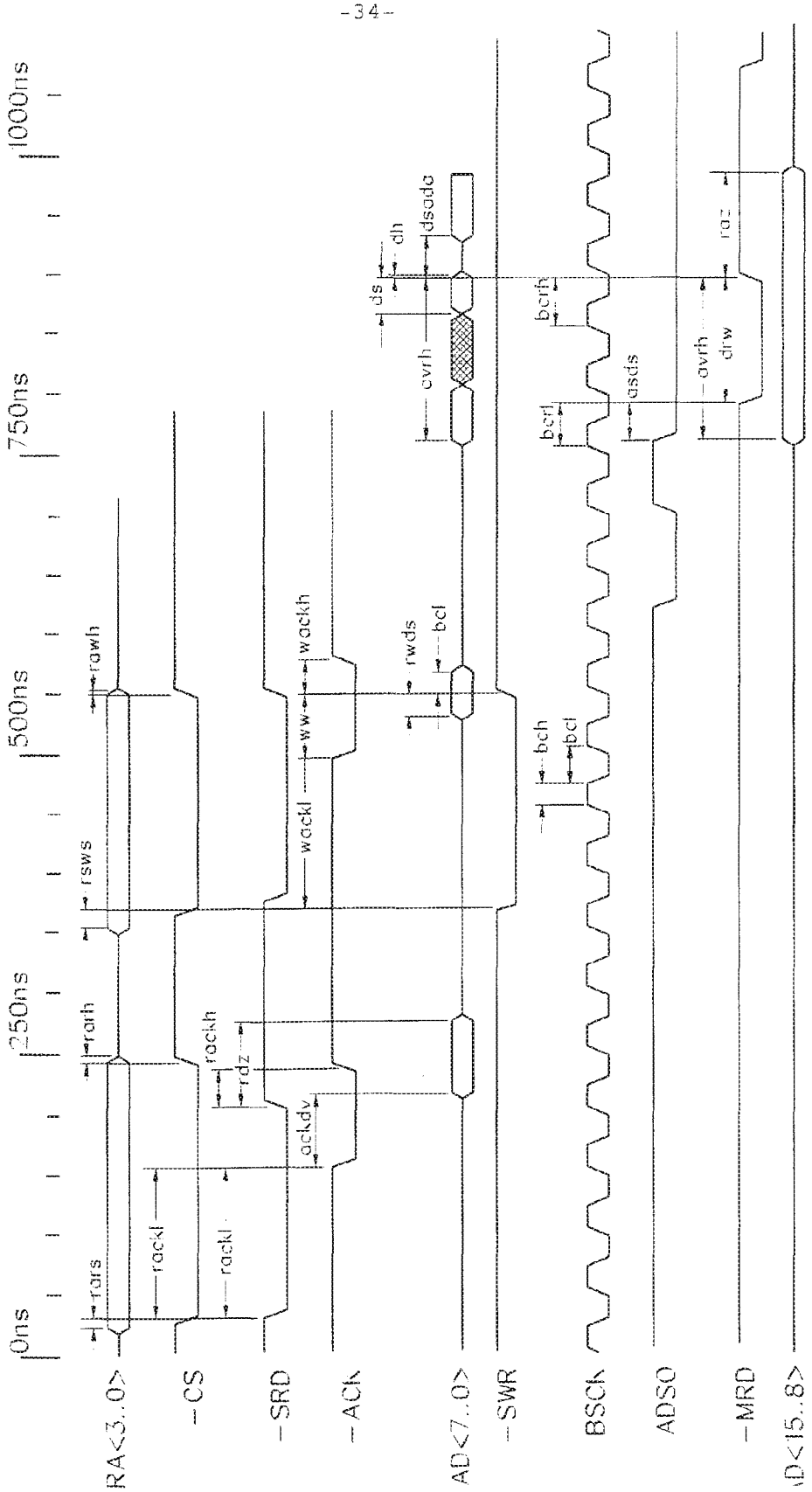
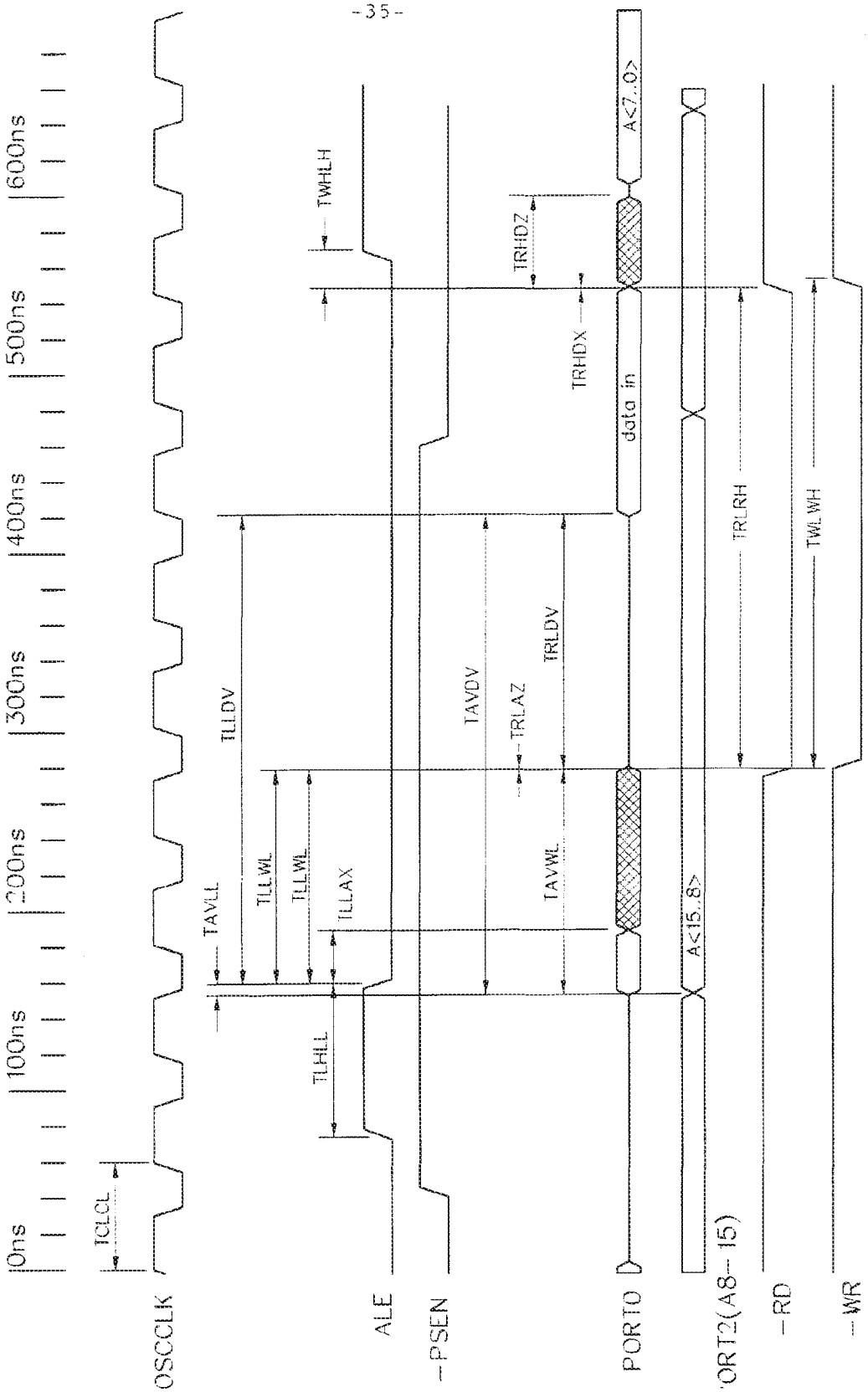
DEF0000524



SUBSTITUTE SHEET (RULE 26)



SUBSTITUTE SHEET (RULE 26)

WHAT IS CLAIMED IS:

1. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, each comprising:

a. an interface, connecting said repeater to an AC power line;

b. a transceiver, electrically connected to said coupler for receiving data from said coupler, wherein said transceiver further comprises:

i. a data modulator to convert digital data to analog data;

ii. a transmitter to receive the analog data from said data modulator and prepare the analog data for transmission on the power lines;

iii. a transmit filter receiving the analog data from said transmitter and filtering the resulting analog signal to transmission on the power lines;

iv. a receiver filter receiving an analog signal from the power lines;

v. a receiver receiving the filtered analog signal from said receiver filter and demodulating and digitizing said analog signal, wherein said demodulation incorporates frequency shift key (FSK) and differential frequency shift key (DFSK) technology; and

vi. a data buffer receiving said digitized data from said receiver;

c. controller, electronically connected to said transceiver, receiving data from said data buffer and sending data to said data modulator, to provide digital control to said transceiver; and

d. an interface electrically connected to said controller for transferring digital data to a computer.

2. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said transceiver further comprises:

a. a re-synchronizer to synchronize data received by said receiver.

3. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said transceiver receiver further comprises:

a. a DSFK data detector.

4. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said transceiver receiver further comprises:

a. an acknowledge signal created from a FSK carrier signal.

5. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said transceiver receiver further comprises:

a. a DFSK edge detector.

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6. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said transceiver receiver further comprises:

a. a DFSK peak detector.

7. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said controller further comprises:

a. a serializer/deserializer to serialize and deserialize the data as well as insert realignment bits and CRC logic.

8. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, comprising:

a. a means for coupling between a local area network and an AC power line for transmitting and receiving data;

b. a means for modulating a transmission carrier with network data and demodulating a transmission carrier to recover network data, said means including a means for performing differential frequency shift key modulation;

c. a means for providing noise immunity to the transferred data; and

d. a means for providing synchronization of the transferred data.

9. A local area network repeater system for transmitting and receiving network data between repeater, comprising a controller, wherein said controller includes a state machine which permits the selection of a wide range of data rates without requiring the modification of carrier frequency.

10. A local area computer network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, each comprising:

means for coupling a local area network interface to a local area computer network or network segment for transmitting a bi-directional network data stream, said data stream having a bitrate of up to 2 megabits per second and a data bandwidth approximately equal to said bitrate;

means for frequency shift key modulating a transmission carrier with said network data stream and demodulating said frequency shift key modulated transmission carrier to recover network data, said frequency shift key modulated transmission carrier having an instantaneous frequency bandwidth which is not substantially greater than the greater of either about twice said data bandwidth or the frequency deviation of said frequency shift key modulation, said means comprising a receiver chip which utilizes at least one stage of gain and filter, and said means providing at least about 90 decibels of gain;

means for coupling bi-directional network data between said network interface and said carrier modulation and demodulation means; and

means for coupling said transmission carrier to an AC power line to produce a power line carrier signal having a frequency in the range from about 2 to about 20 megahertz.

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11. A local area network repeater system as recited in claim 1 wherein said local area network interface comprises a network interface selected from the following:

Ethernet network interface controller means;

Token ring network interface controller means;

Arcnet network interface controller means;

RS-232 interface controller means;

RS-485 network interface controller means;

Serial data, open standard interface; and

Parallel data interface.

12. A local area network repeater system as recited in claim 1 wherein said transmission carrier modulation and demodulation means further comprises transmission means selected from the following:

Time domain multiple access means wherein carrier data modulation and transmission is alternated with carrier data demodulation and data reception, said modulation and demodulation carriers operating on the same frequency; and

Frequency domain multiple access means wherein said carrier data modulation and transmission utilizes one carrier frequency and said carrier data demodulation and reception utilizes a second frequency.

13. A local area network repeater system as recited in claim 1 further comprising repeater controller means for performing control functions selected from among the following:

initializing and controlling said network interface means, as required to permit transparent repeating of network data over the AC power line;

monitoring said data modulated transmission carriers and arbitrating data transmissions to permit only one repeater at a time to transmit a carrier of a particular frequency onto the AC power line; and

attaching and removing data preambles and addresses; reformatting data, encrypting and decrypting data, and providing alternate data communications ports.

14. A repeater system for transmission of high frequency computer data signals through an AC power line, the system comprising a plurality of repeaters, each repeater comprising:

means for coupling input signals and output signals to a signal port;

carrier modulation means for frequency shift key modulating a transmission carrier with said input signals to produce a modulated signal having a bitrate of up to 2 megabits per second and a data bandwidth approximately equal to said bitrate, said modulated signal having an instantaneous bandwidth which is not substantially greater than the greater of either about twice said data bandwidth or the frequency deviation of said frequency shift key modulation;

demodulation means for demodulating said modulated signal to recover said output signals, said modulation means further comprising means for changing the resonant frequency produced by an oscillator in response to an input signal by driving an output port of the oscillator;

said demodulation means further comprising means for providing at least about 90 decibels of gain;

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means for coupling bi-directional signals between said signal port and said carrier modulating and demodulation means; and

means for coupling said transmission carrier to the AC power line to produce a power line carrier signal having a frequency in the range from about 2 to about 20 megahertz.

15. A method for power line carrier data transmission, said method comprising the steps of:

generating a carrier signal at a frequency in the range of from about 2 to 20 megahertz;

frequency shift key modulating said carrier signal to provide a modulated carrier signal having a data bitrate of up to 2 megabits per second and a data bandwidth approximately equal to said bitrate, said modulated carrier signal having an instantaneous bandwidth which is not substantially greater than the greater of either about twice said data bandwidth or the frequency deviation of said frequency shift key modulation; and

coupling the frequency shift key modulated carrier signal onto an ac power line.

16. The method of claim 8, further comprising the steps of:

coupling the modulated carrier signal off of the AC power line; and

demodulating the carrier signal.

17. The method of claim 8, wherein said modulating step comprises modulating the carrier signal to correspond to a digital data signal.

18. The method of claim 8, wherein said modulating step comprises modulating the carrier signal to correspond to an analog data signal.

19. The method of claim 8, wherein said modulating step comprises buffering with multi-stage transmitter drivers.

20. The method of claim 9, wherein said demodulating step comprises filtering the carrier signal in stages.

21. The method of claim 8, further comprising the collision avoidance steps of:

listening for traffic on the AC power line; and

selecting between (a) transmitting an access request after detecting termination of a transmission, and (b) beginning data transmission after detecting no other traffic.

22. An embedded PLC communications system comprising a plurality of networked communications devices, each of said communications devices comprising:

an embedded microcontroller having a communication port;

carrier modulation means for frequency shift key modulating a transmission carrier with data signals from said communication port to produce a modulated carrier, said modulated carrier having a bitrate of up to 2 megabits per second and a data bandwidth approximately equal to said bitrate, said modulated carrier having an instantaneous bandwidth which is not substantially greater than the greater of either about twice said data bandwidth or the frequency deviation of said frequency shift key modulation; and

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DEF0000530

a receiver comprising a demodulator for demodulating said modulated carrier to recover corresponding data signal, said receiver comprising at least one intermediate frequency gain and filtering stage utilizing an intermediate frequency in the range from about 2 to about 20 megahertz and providing a receiver gain of at least about 90 decibels;

means for coupling said data signals between said communication port and said carrier modulation means; and

means for coupling said modulated carrier to an AC power line.

23. The system of claim 17, further comprising network arbitration and control means.

24. The system of Claim 17, wherein said means for coupling said transmission carrier to an AC power line comprises an existing AC power cord.

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DEF0000531

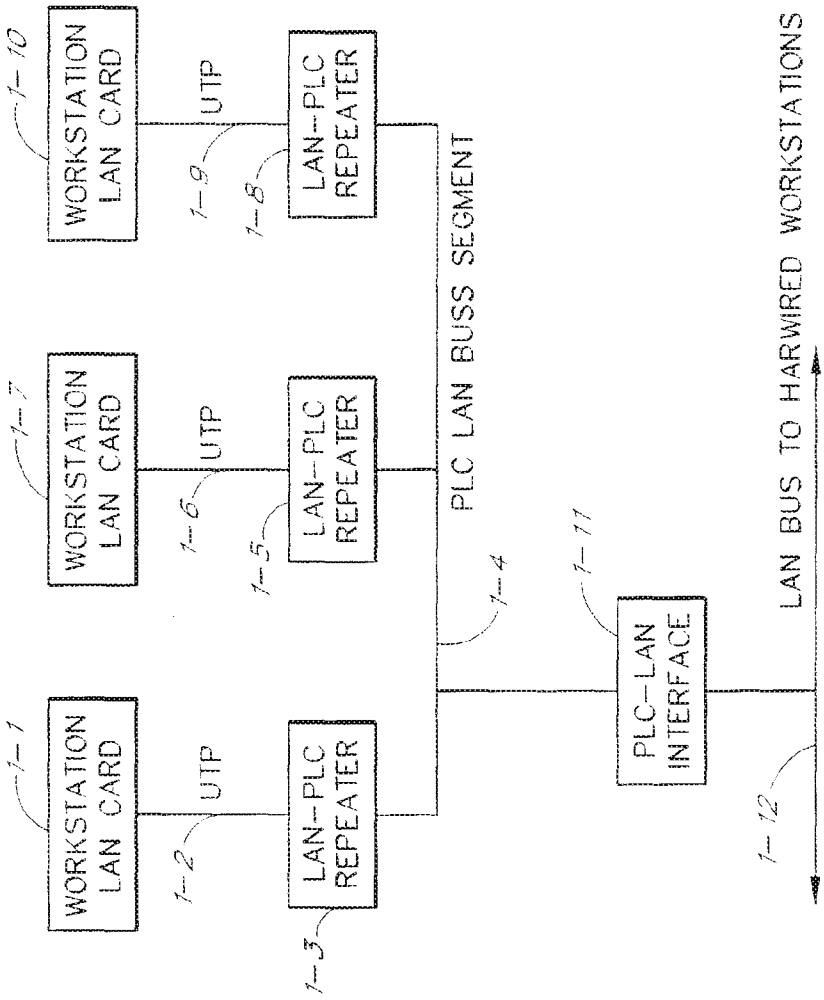

FIG. 1

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DEF0000532

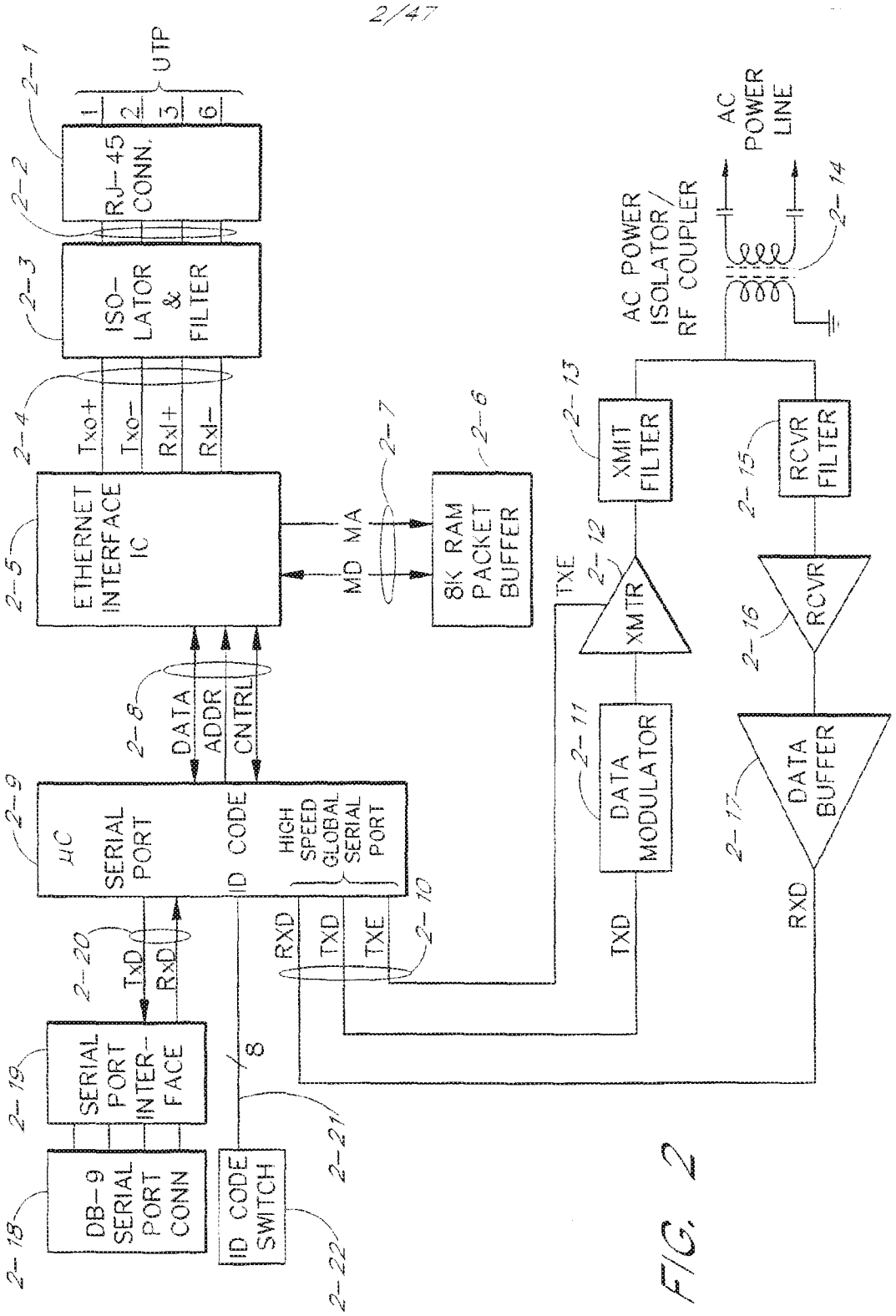

FIG. 2

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DEF0000533

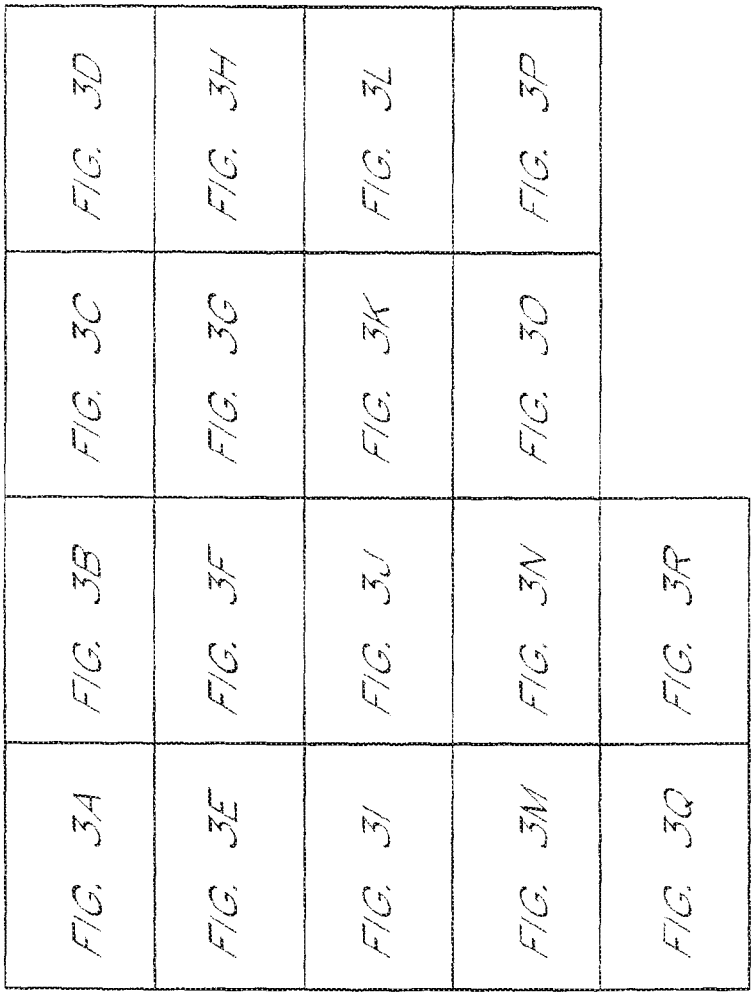

FIG. 3

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DEF0000534

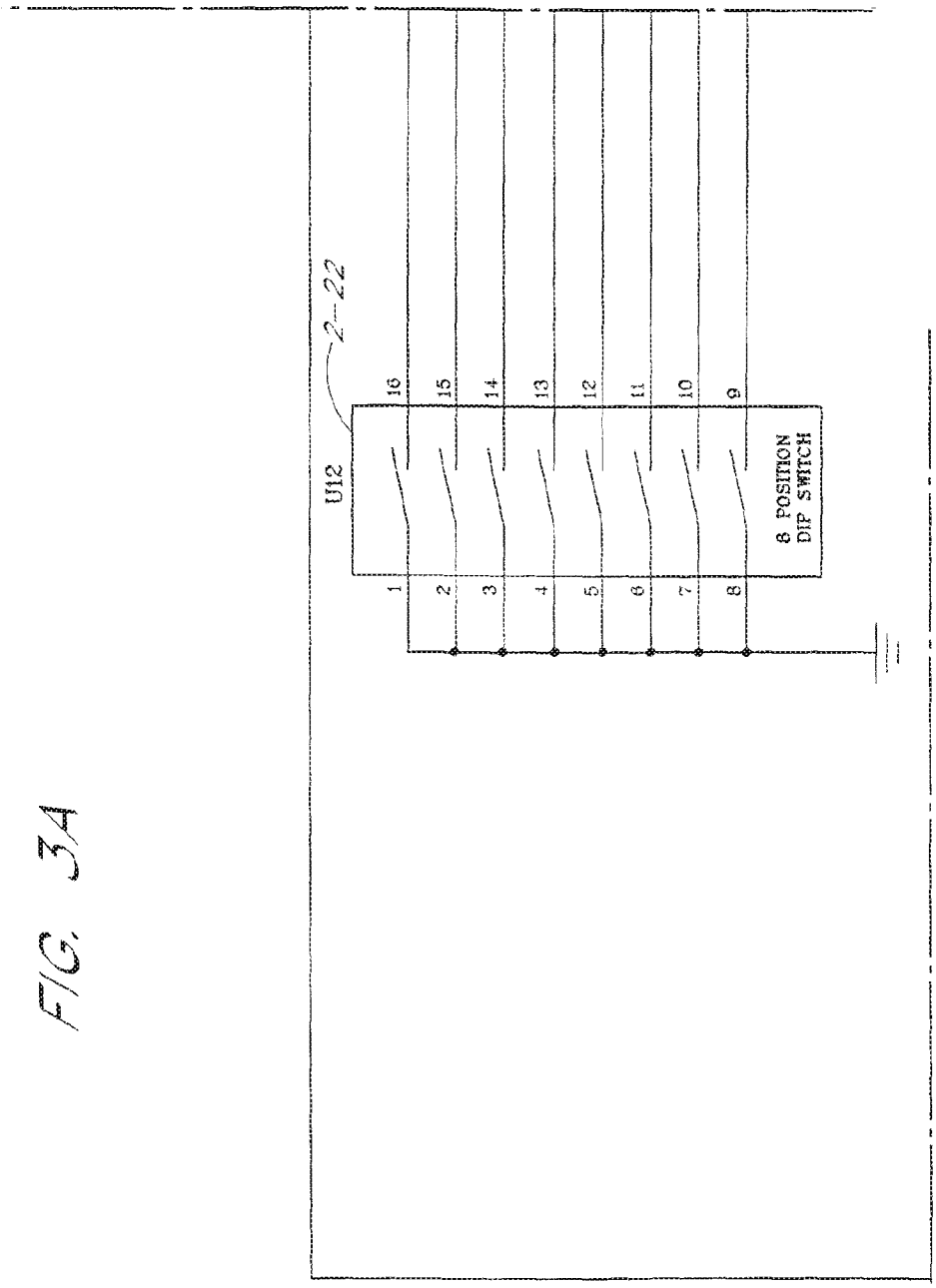
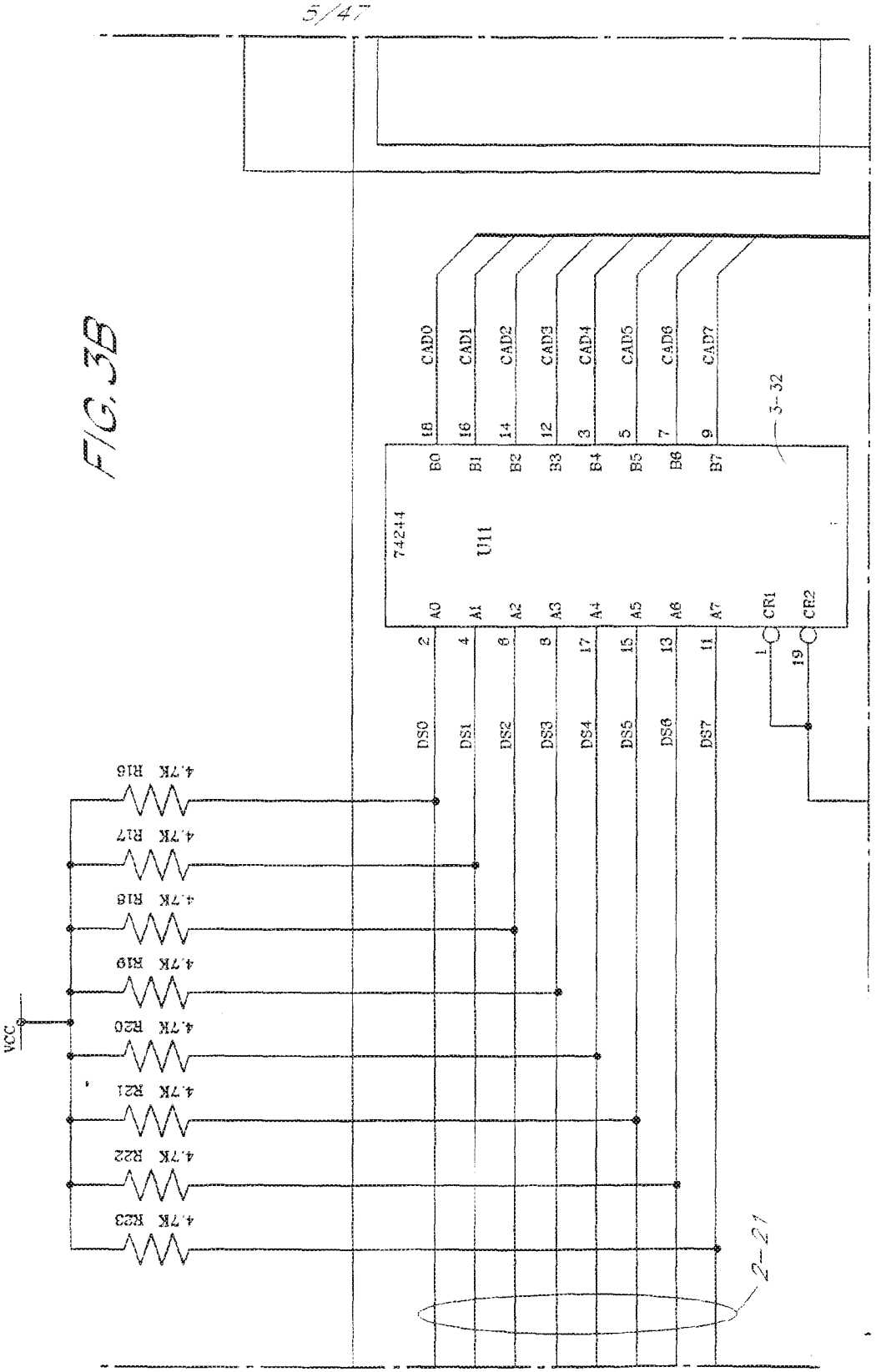


FIG. 34

FIG. 3B



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DEF0000536

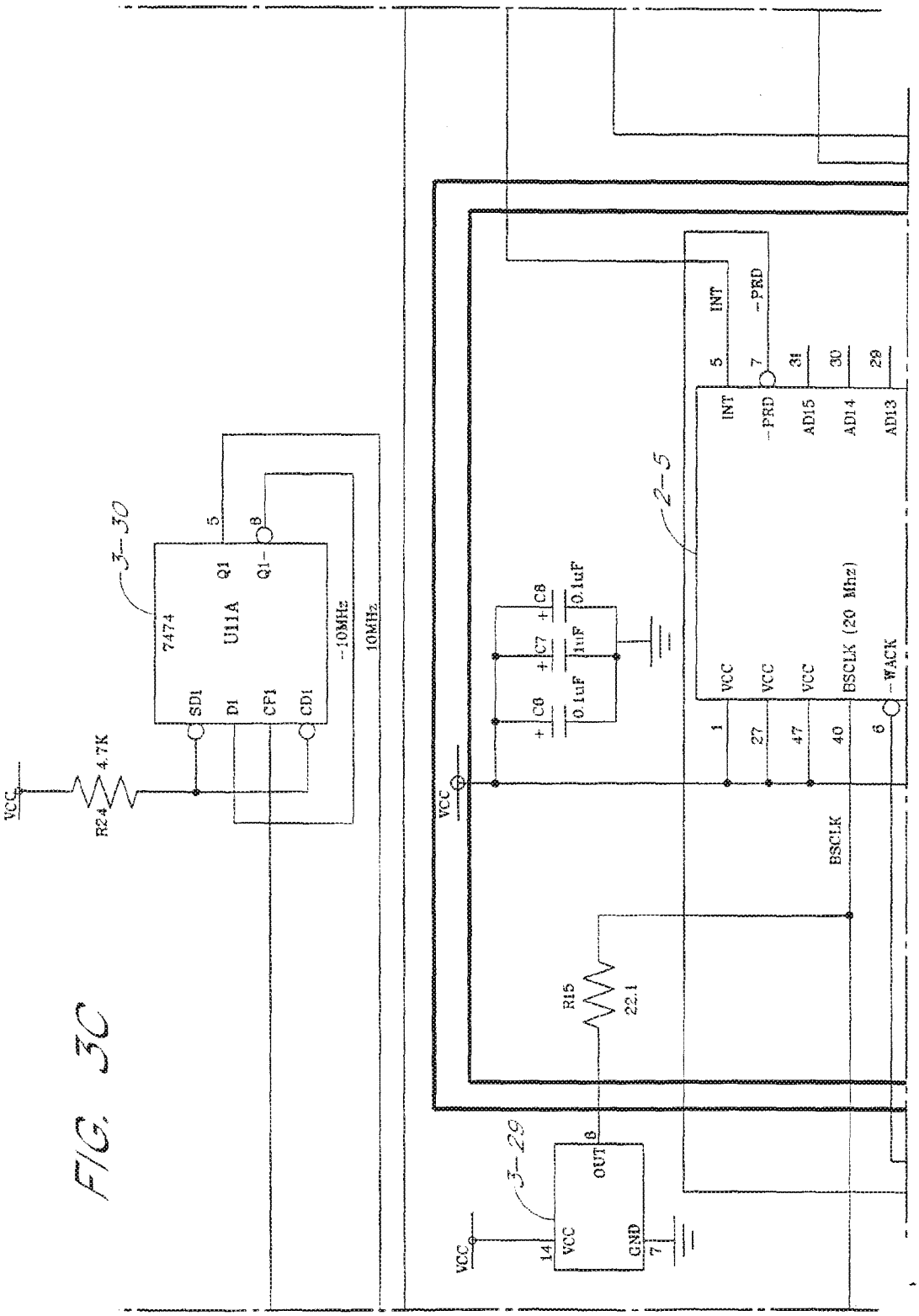

FIG. 3C

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DEF0000537

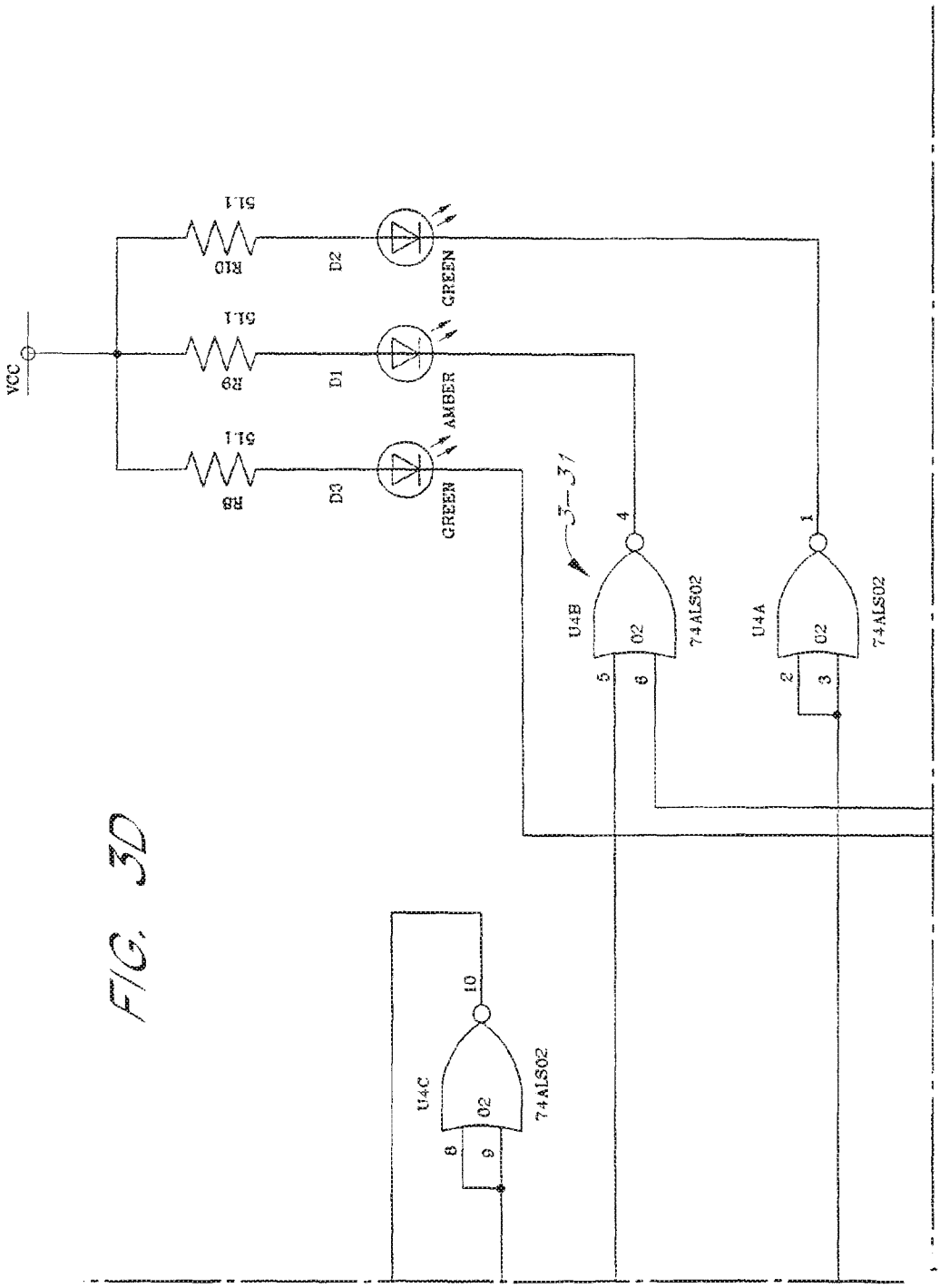
VCC
R10
510
D2
GREEN
R9
510
D1
AMBER
R8
510
D3
GREEN
U4B
74ALS02
U4A
74ALS02
U4C
74ALS02

FIG. 3D

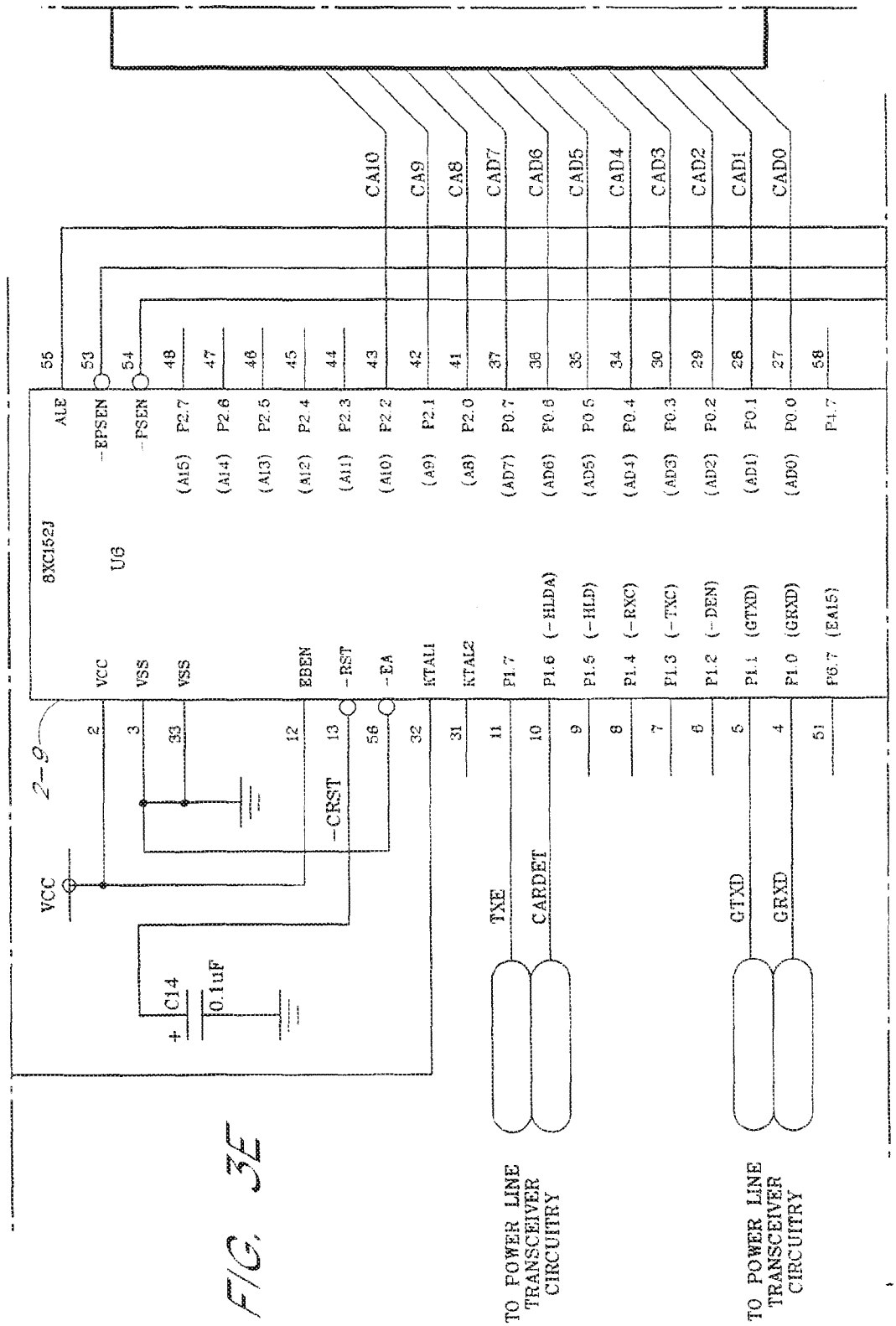

FIG. 3E

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DEF0000539

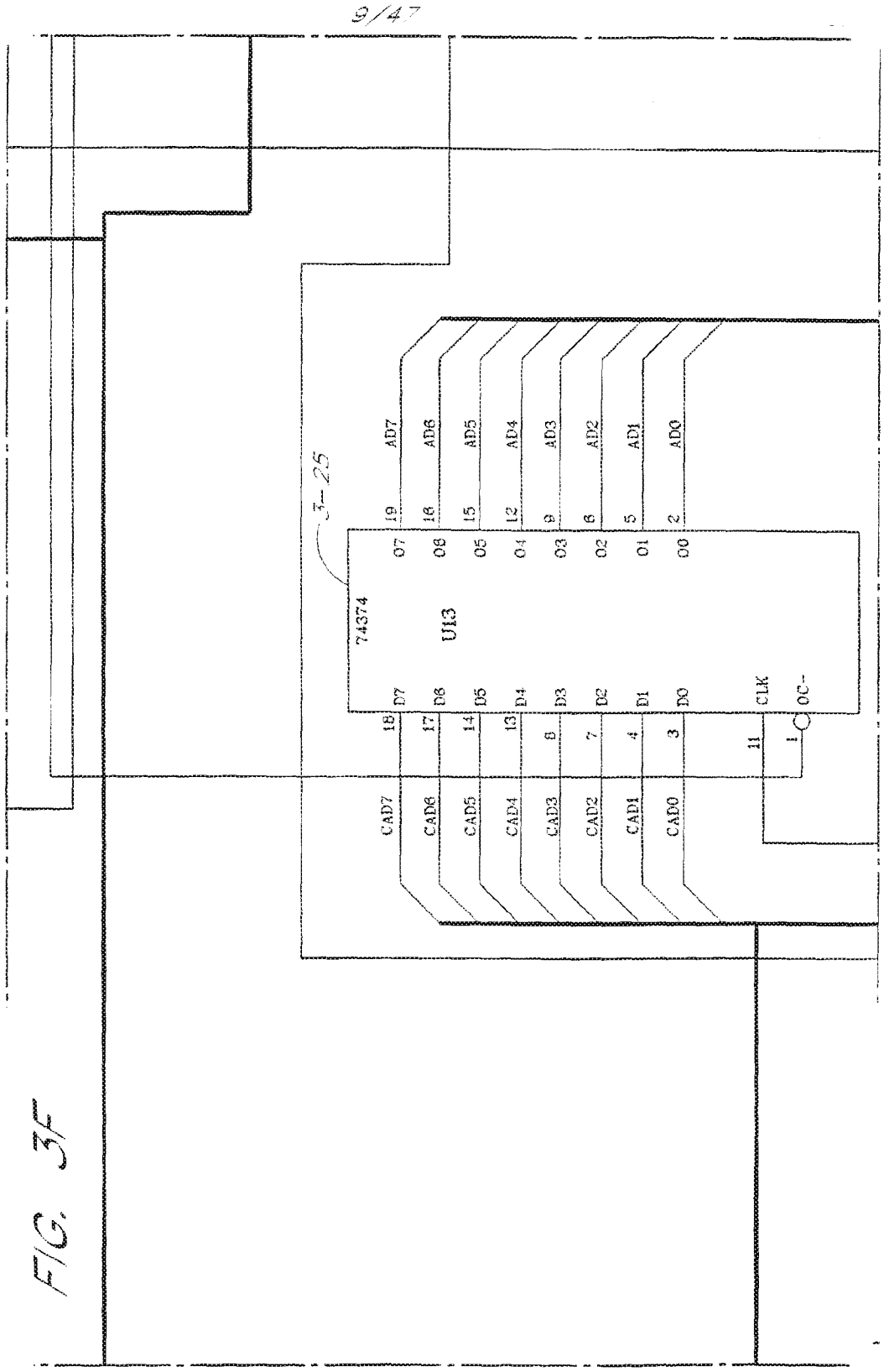
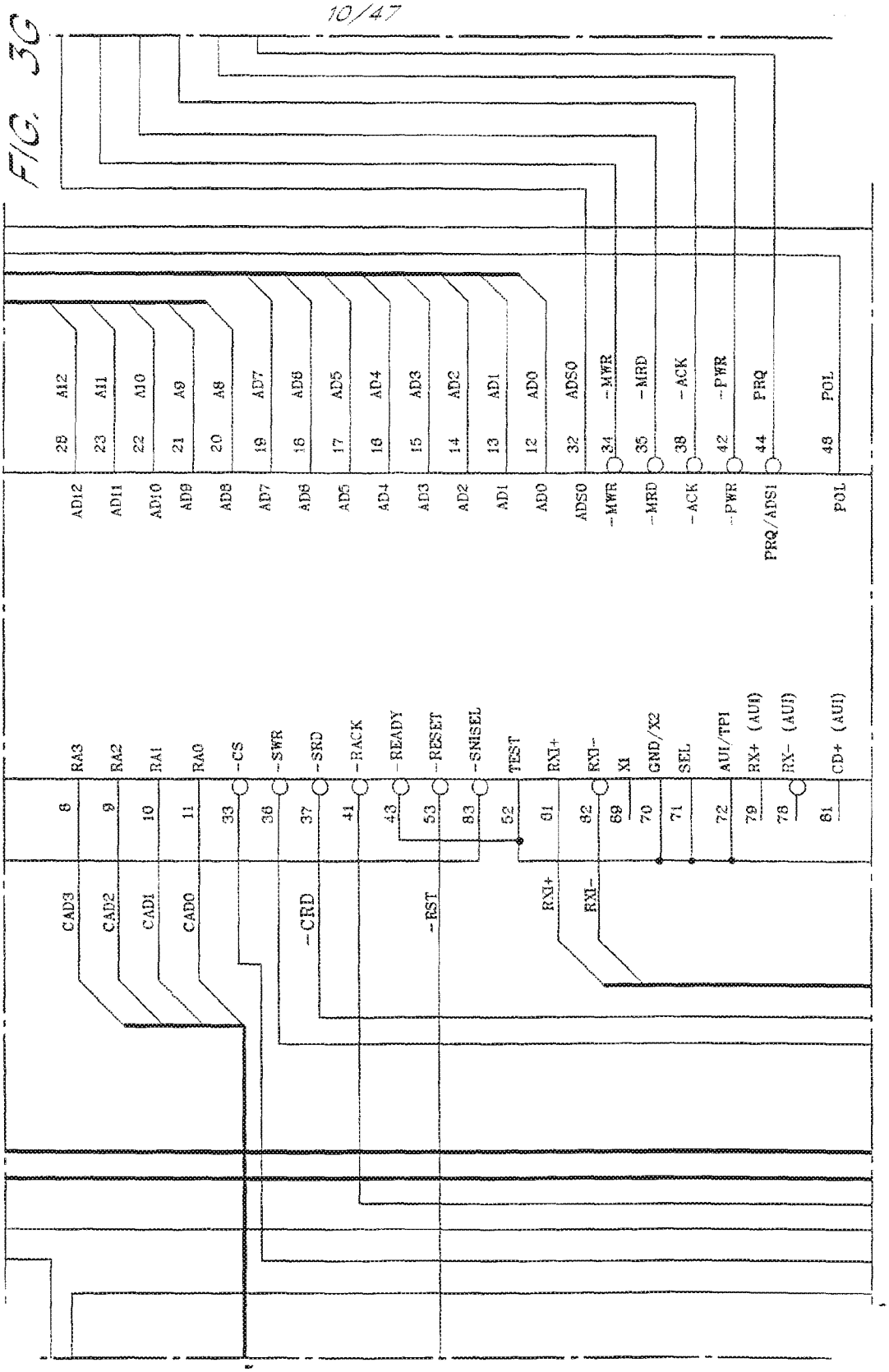

3-25
74374
U13
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
19
18
15
12
9
8
5
2
O7
O6
O5
O4
O3
O2
O1
O0
CAD7
CAD6
CAD5
CAD4
CAD3
CAD2
CAD1
CAD0
18
17
14
13
8
7
4
3
D7
D6
D5
D4
D3
D2
D1
D0
11
CLK
1
OC-

FIG. 3F

10/47

FIG. 3G



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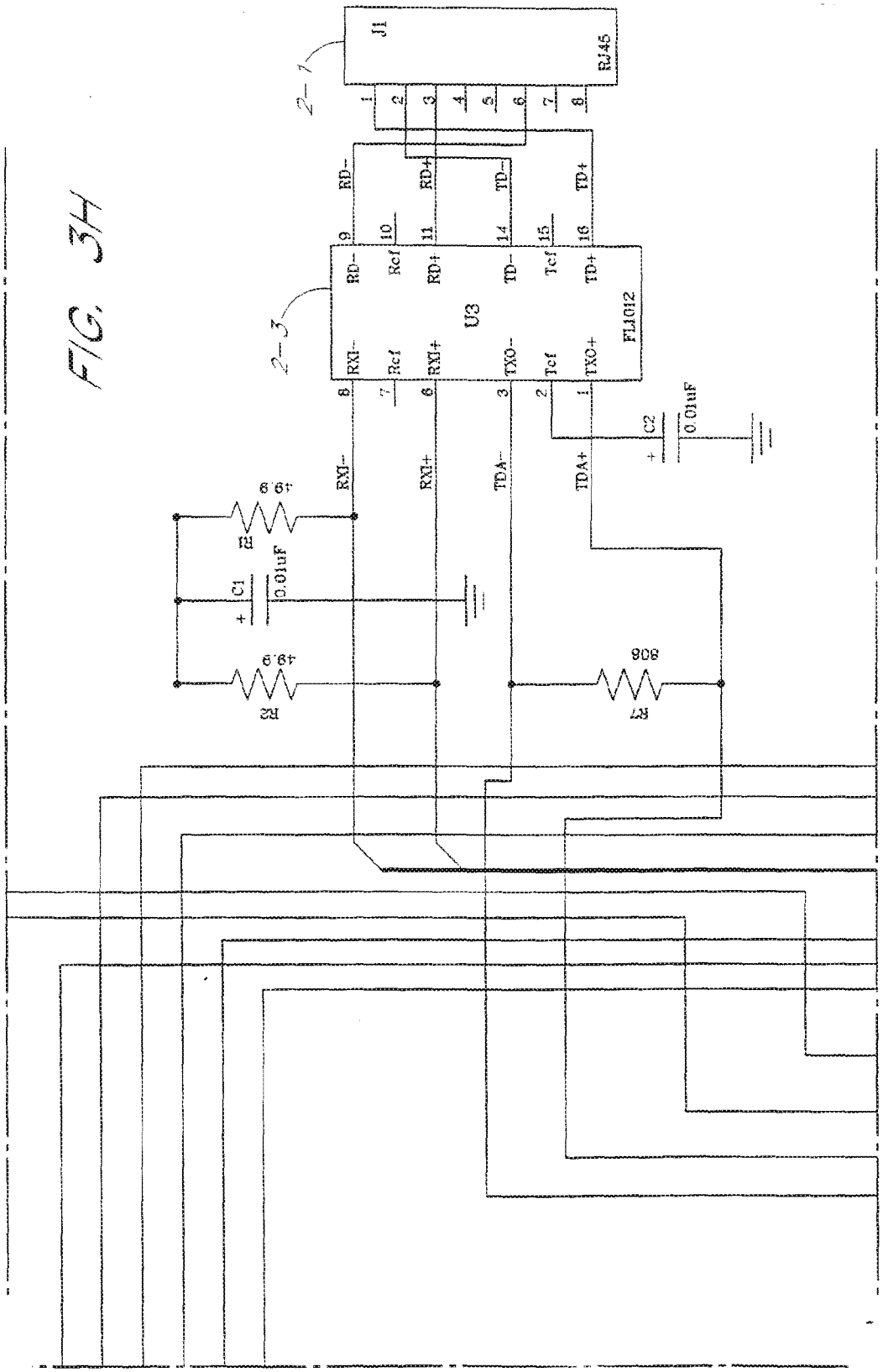
DEF0000541

FIG. 3H



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DEF0000542

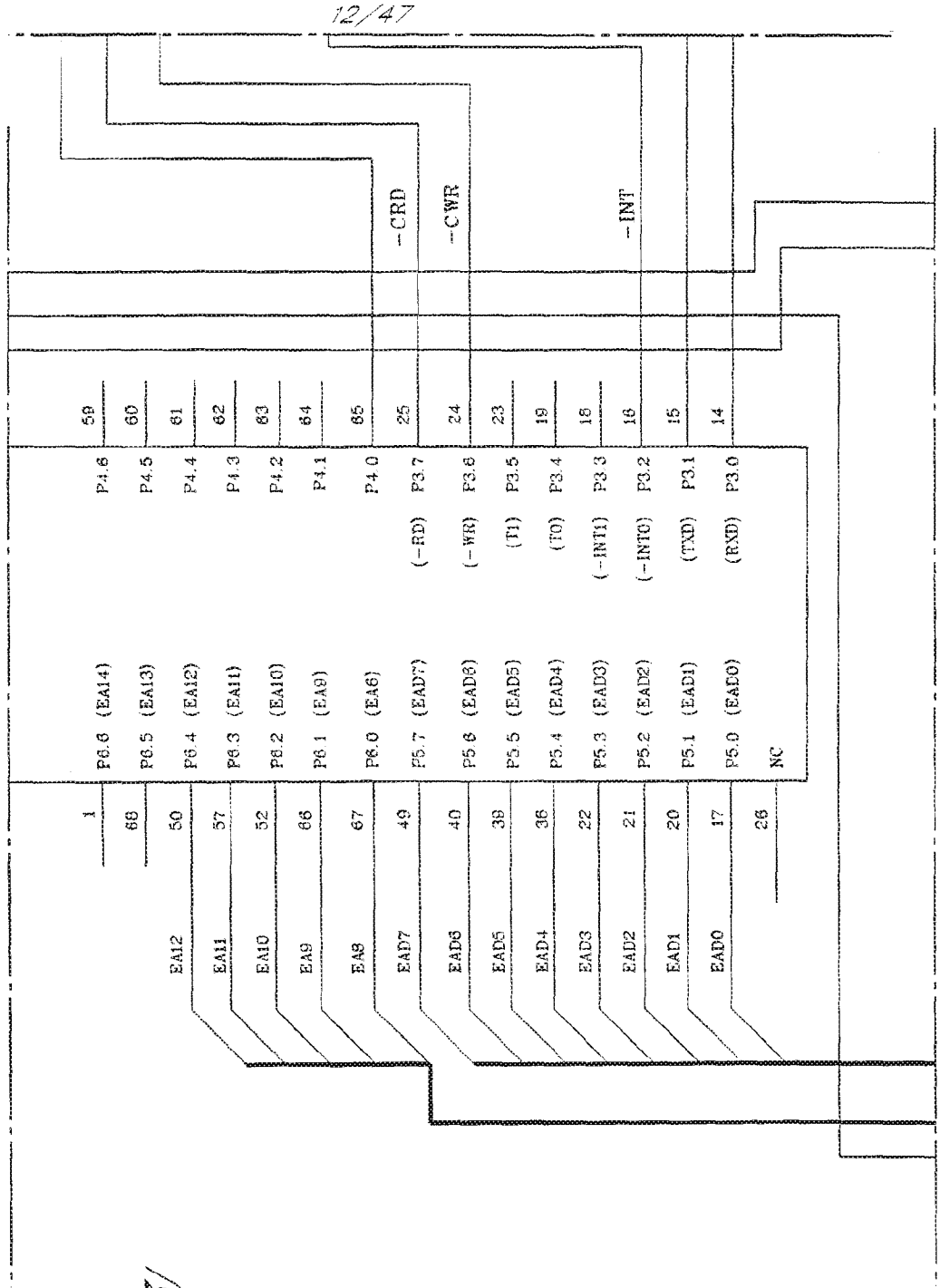

FIG. 3

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DEF0000543

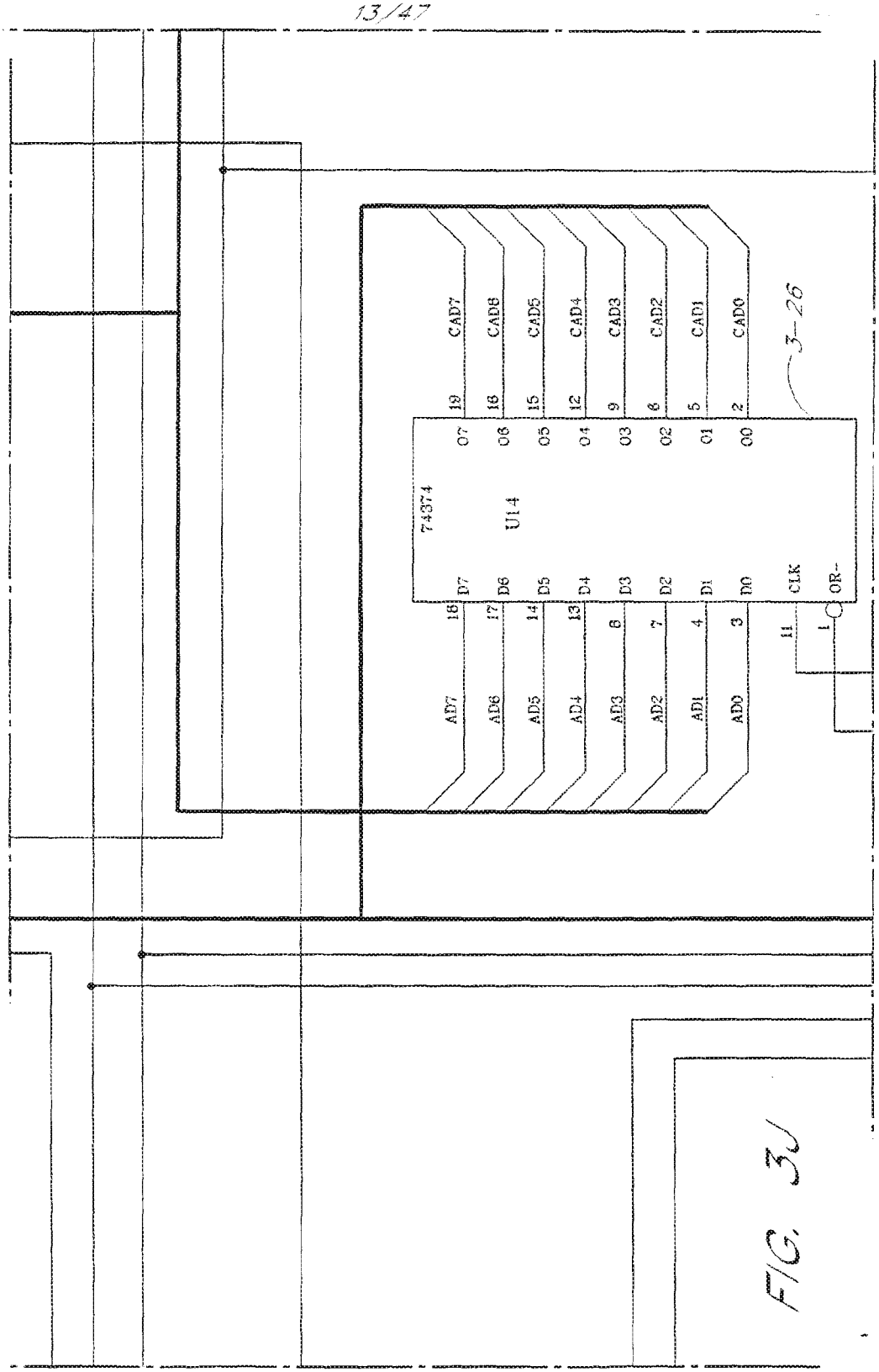

CAD7
CAD6
CAD5
CAD4
CAD3
CAD2
CAD1
CAD0
3-26
74374
U14
O7
O6
O5
O4
O3
O2
O1
O0
D7
D6
D5
D4
D3
D2
D1
D0
CLK
OR-
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0

FIG. 3J

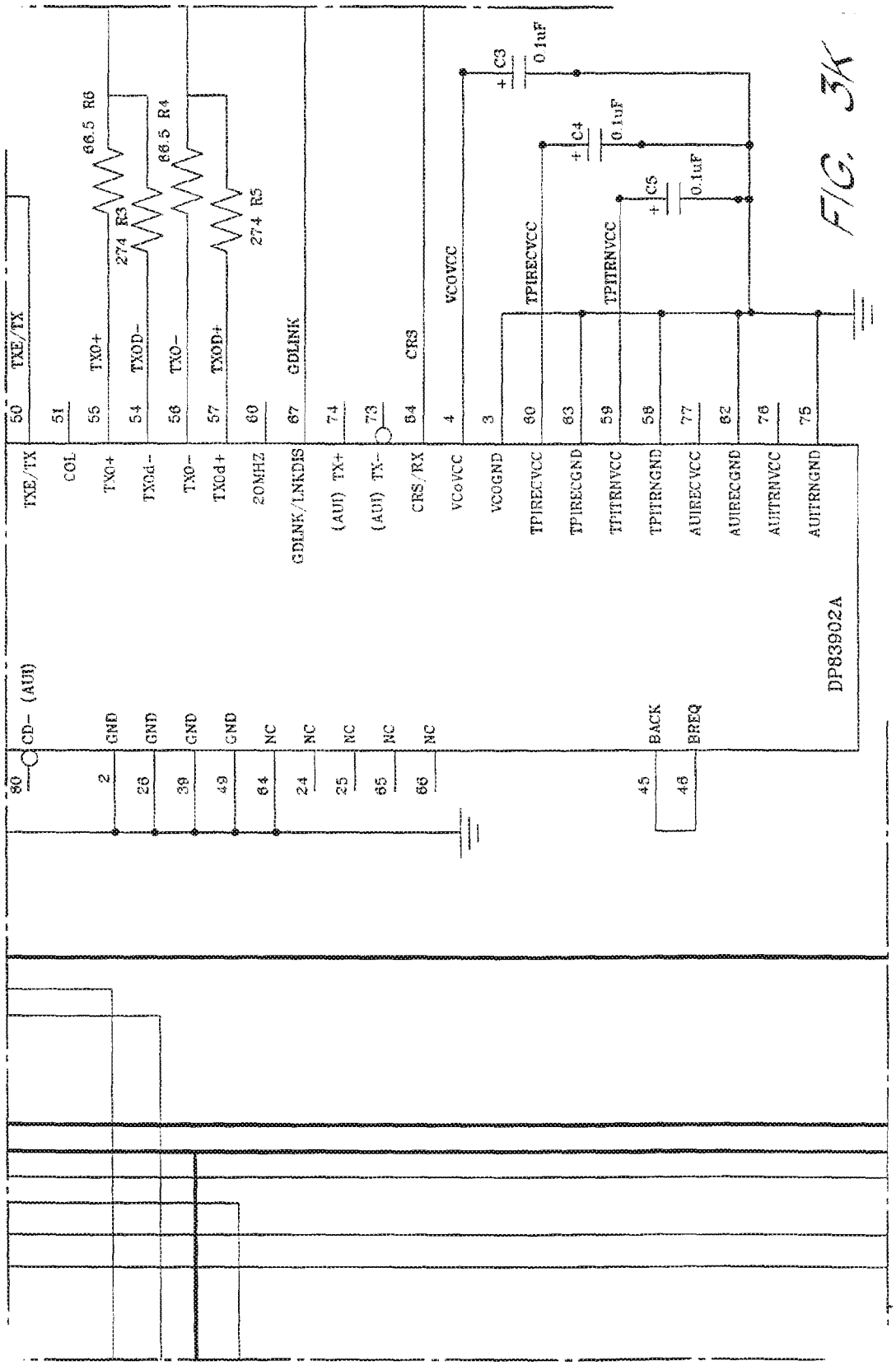
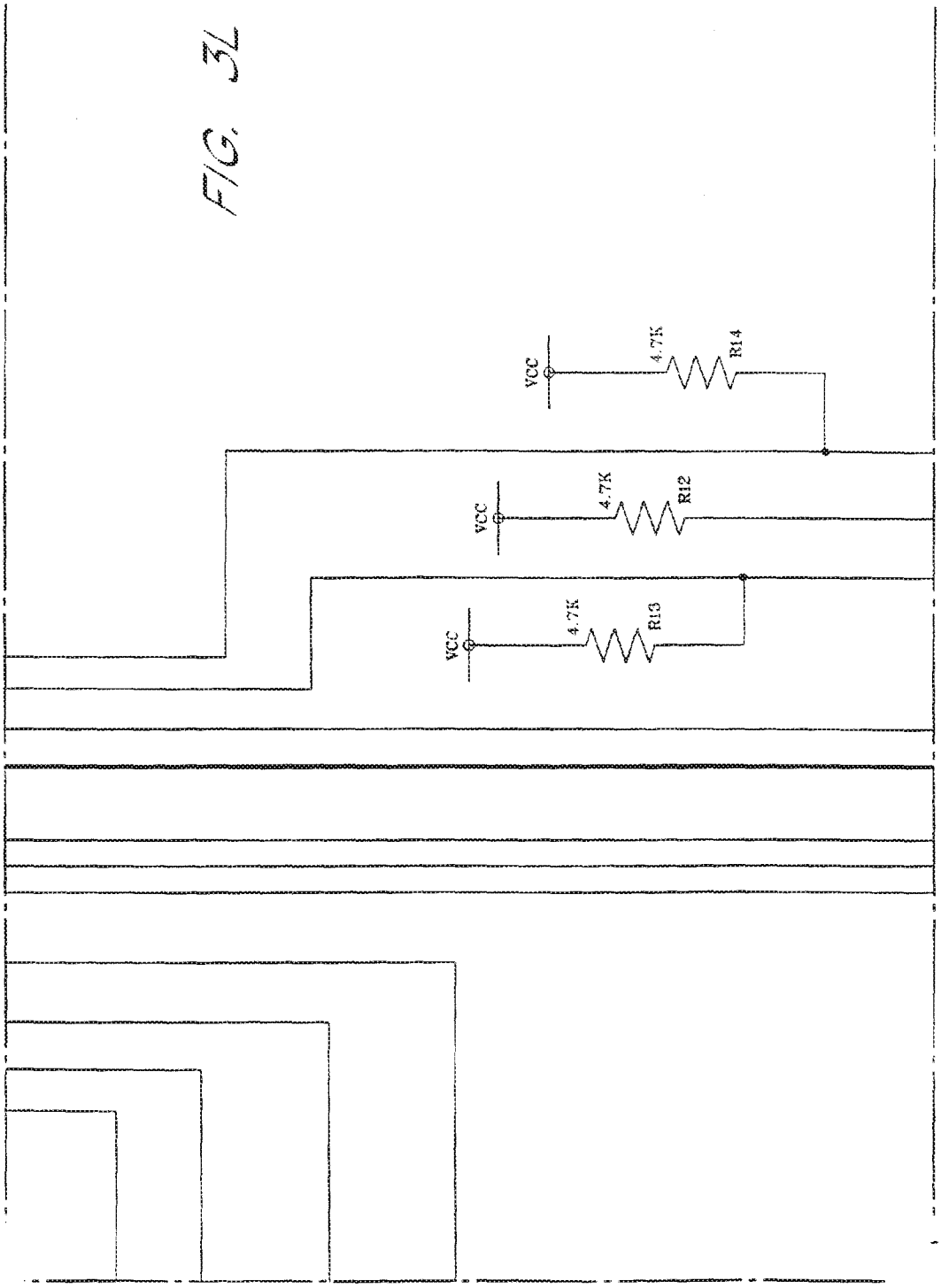

DP83902A
TXE/TX
COL
TXO+
TXOd-
TXO-
TXOd+
20MHZ
GDLINK/LNKDIS
(AUI) TX+
(AUI) TX-
CRS/RX
VCOVCC
VCOGND
TPIRECVCC
TPIRECGND
TPITRNVCC
TPITRNGND
AUIRECVCC
AUIRECGND
AUITRNVCC
AUITRNGND
CD- (AUI)
GND
NC
BACK
BREQ
66.5 R6
66.5 R4
274 R3
274 R5
C3
C4
C5
0.1uF

FIG. 3K

FIG. 3L



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DEF0000546

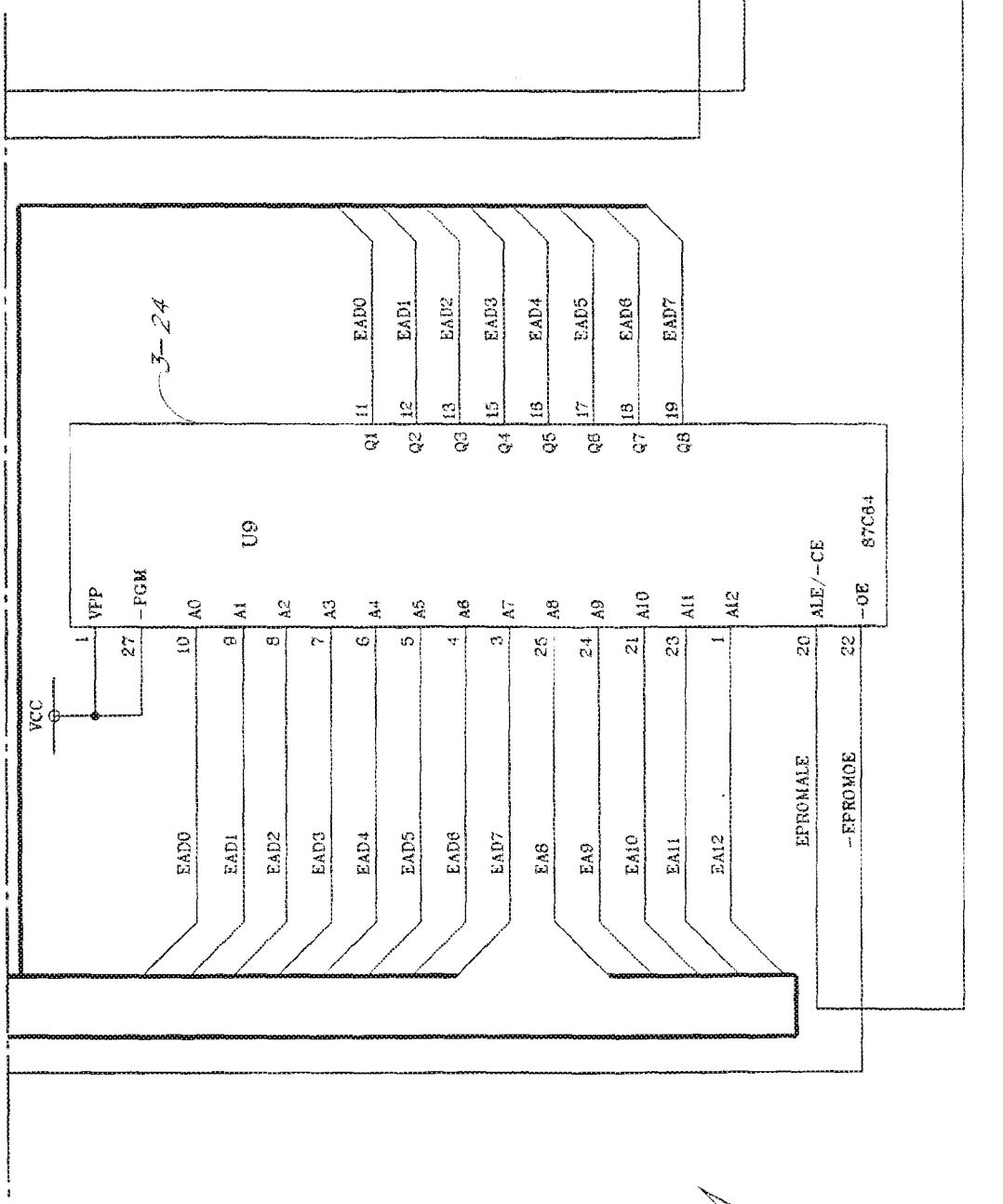

FIG. 3M

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DEF0000547

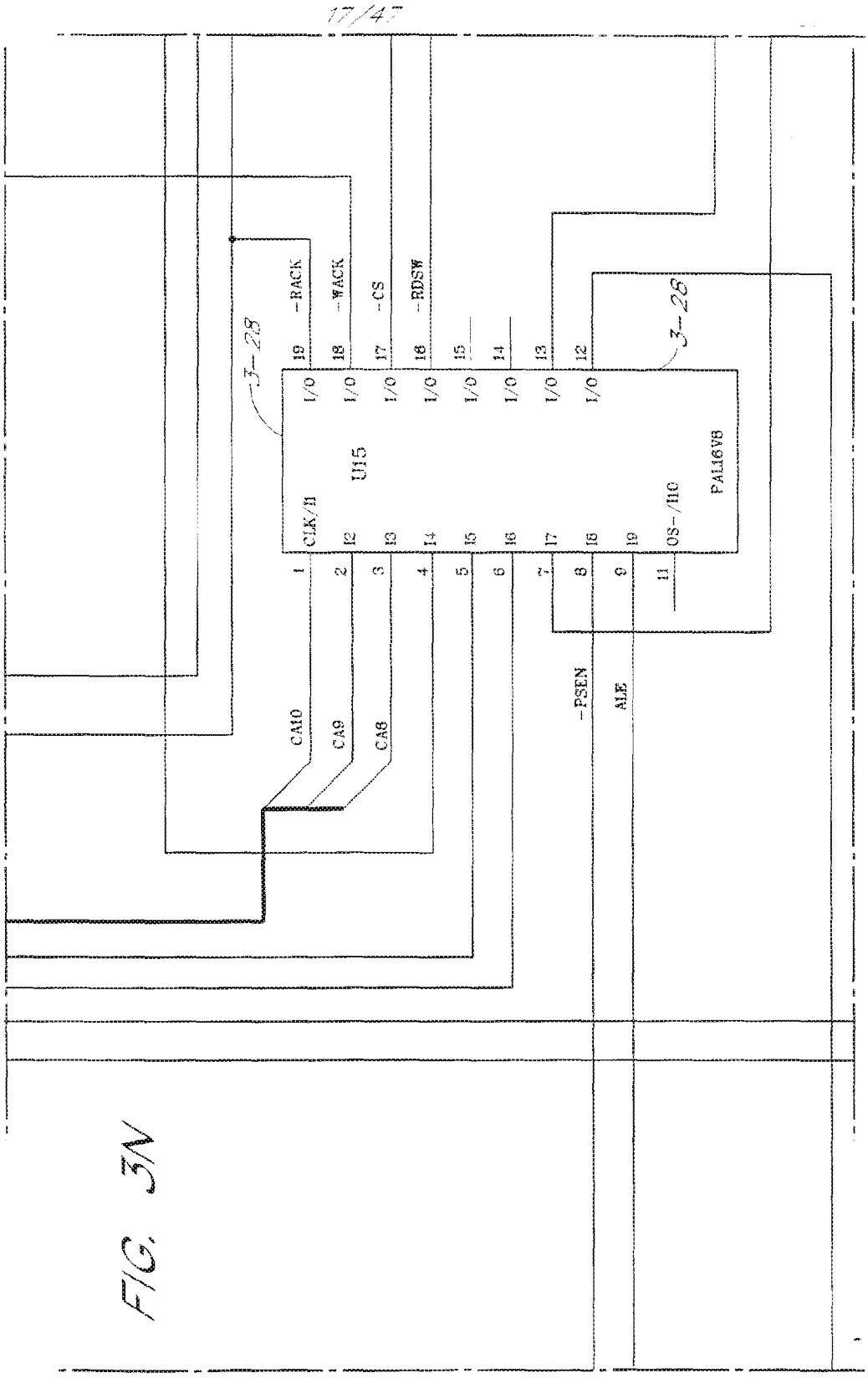

FIG. 3N

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DEF0000548

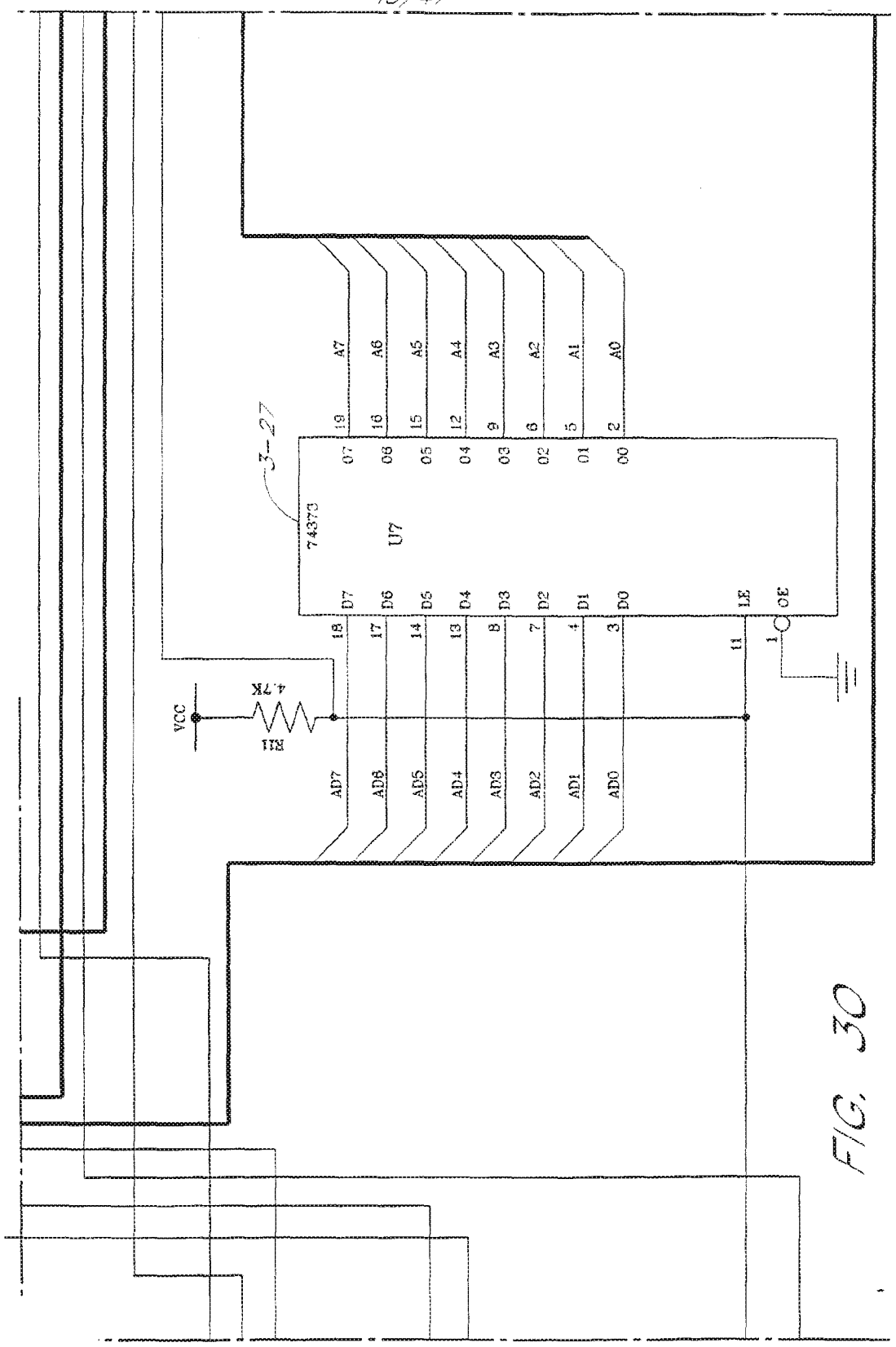
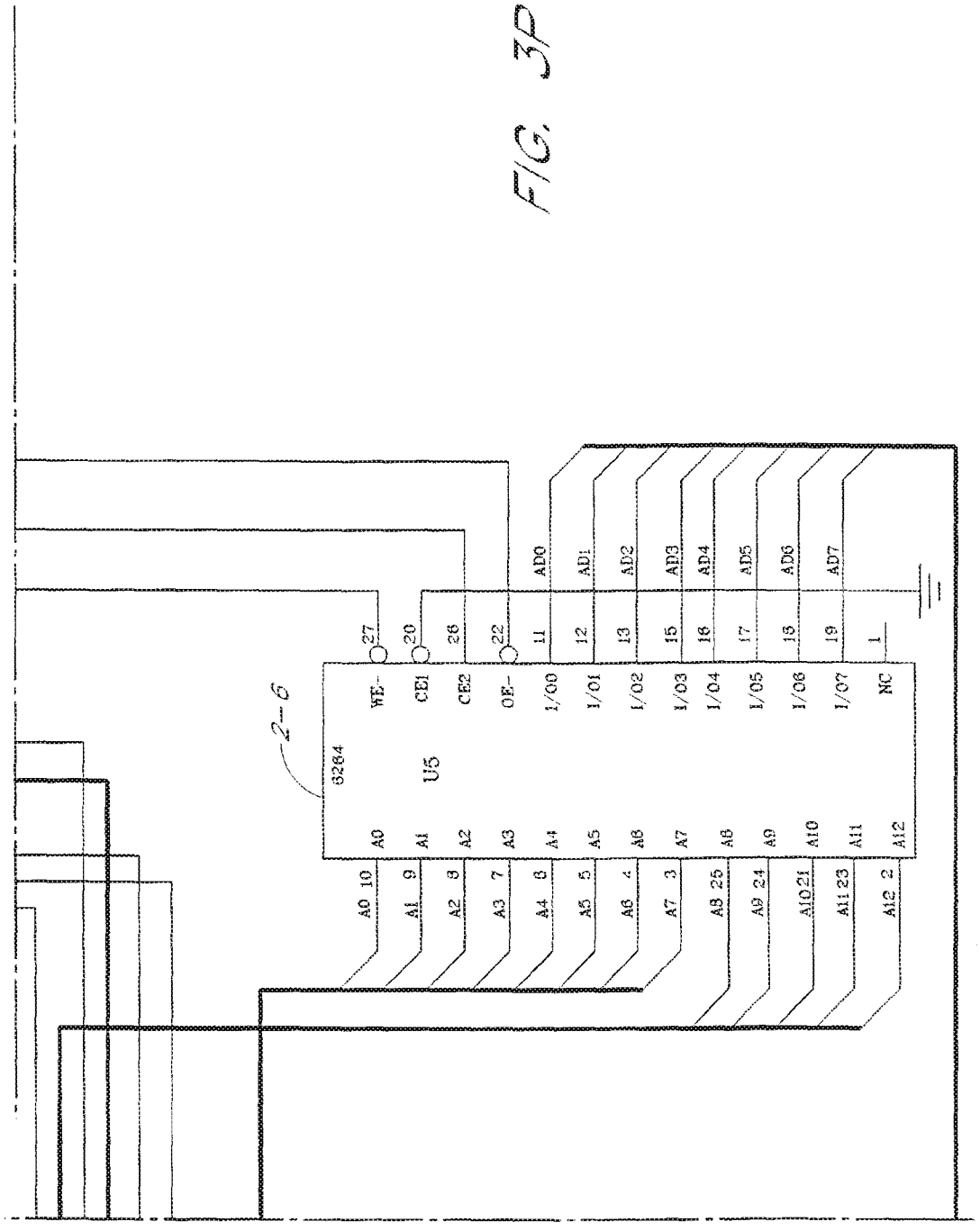

A7
A6
A5
A4
A3
A2
A1
A0
19
16
15
12
9
6
5
2
O7
O6
O5
O4
O3
O2
O1
O0
3-27
74373
U7
D7
D6
D5
D4
D3
D2
D1
D0
LE
OE
18
17
14
13
8
7
4
3
11
1
VCC
4.7K
R11
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0

FIG. 30

FIG. 3D



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DEF0000550

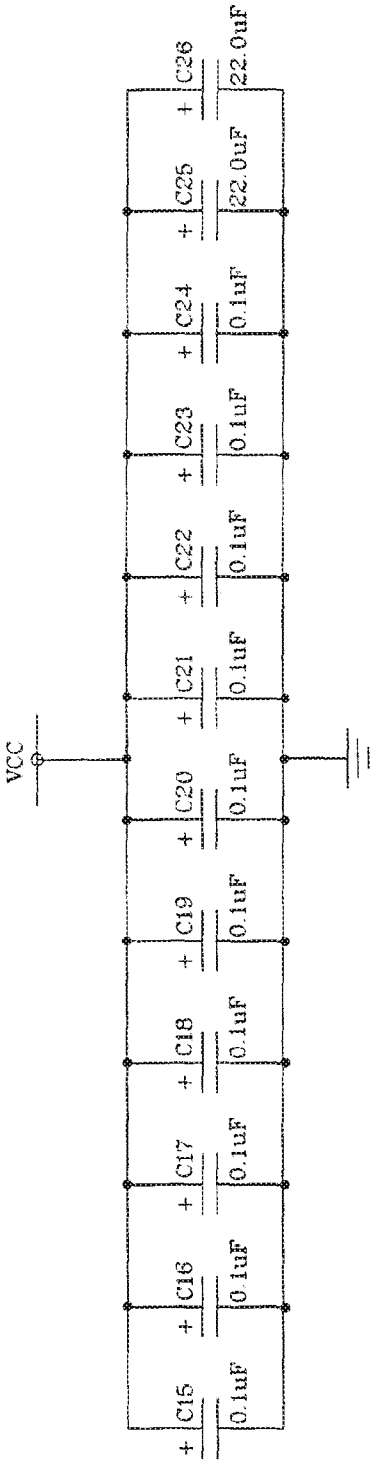
VCC
C15
0.1uF
C16
0.1uF
C17
0.1uF
C18
0.1uF
C19
0.1uF
C20
0.1uF
C21
0.1uF
C22
0.1uF
C23
0.1uF
C24
0.1uF
C25
22.0uF
C26
22.0uF

FIG. 3Q

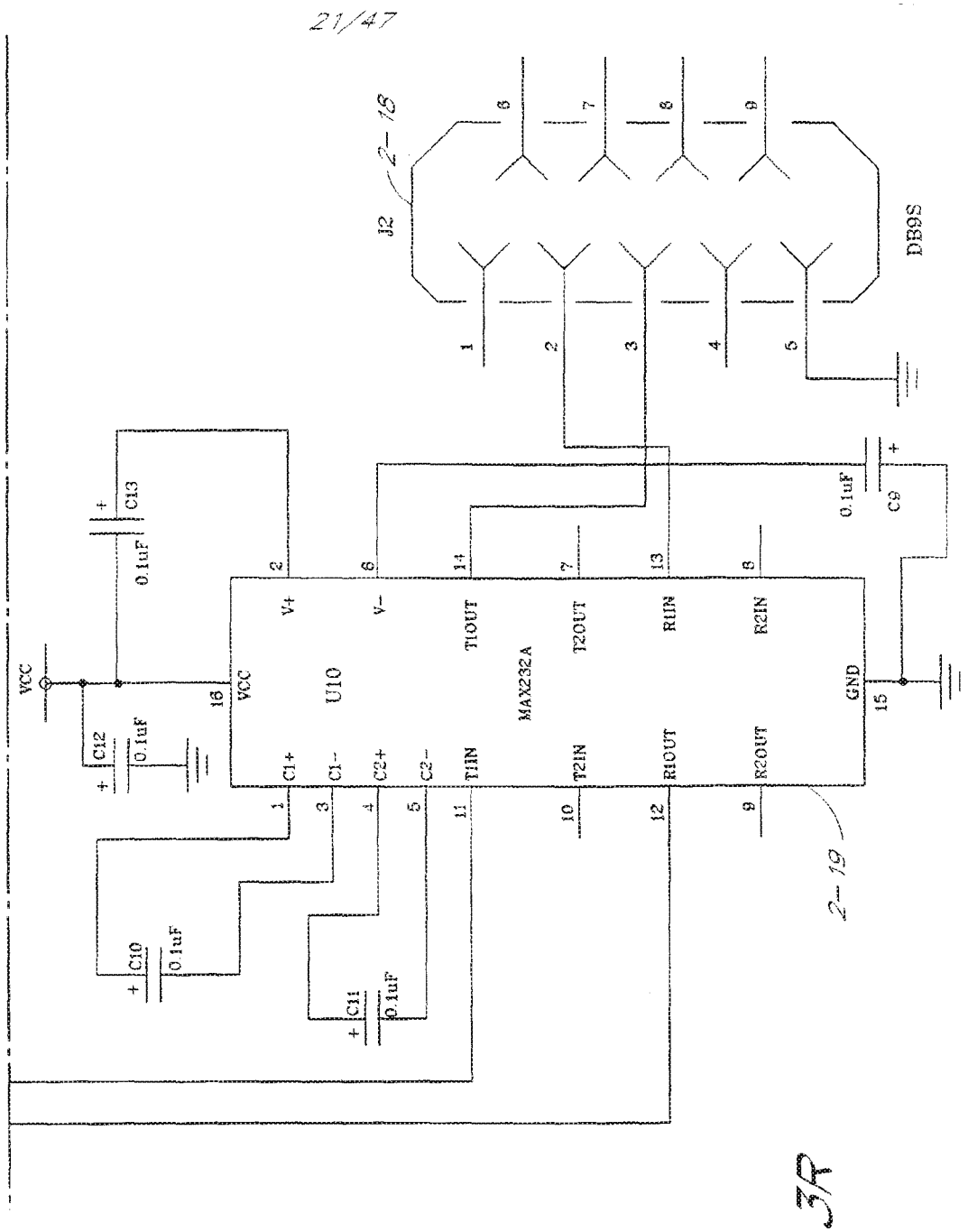
J2
2-18
DB9S
1
2
3
4
5
6
7
8
9
U10
MAX232A
VCC
V+
V-
T1OUT
T2OUT
R1IN
R2IN
GND
C1+
C1-
C2+
C2-
T1IN
T2IN
R1OUT
R2OUT
16
15
C13
C12
C10
C11
C9
0.1uF
2-19

FIG. 3B

FIG. 4A	FIG. 4B	FIG. 4C
FIG. 4D	FIG. 4E	FIG. 4F

FIG. 4

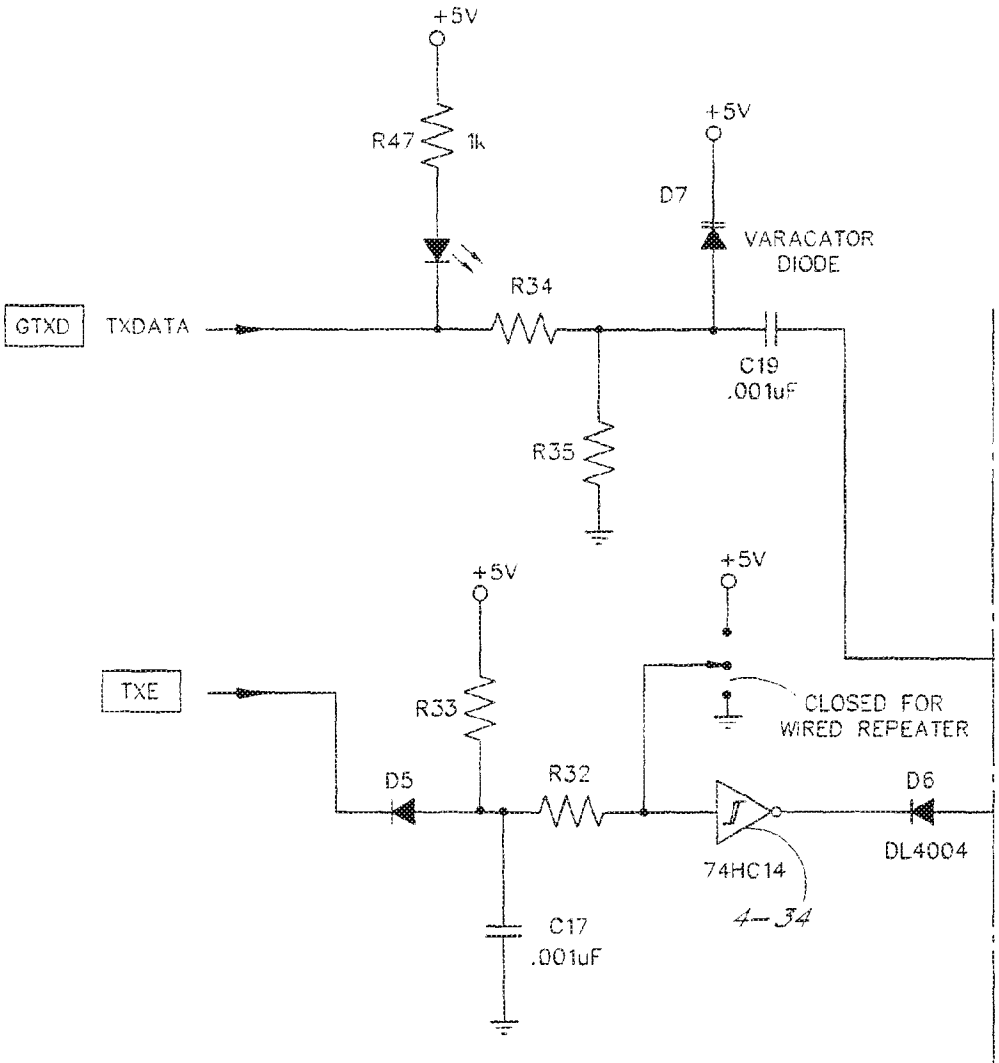

FIG. 4A

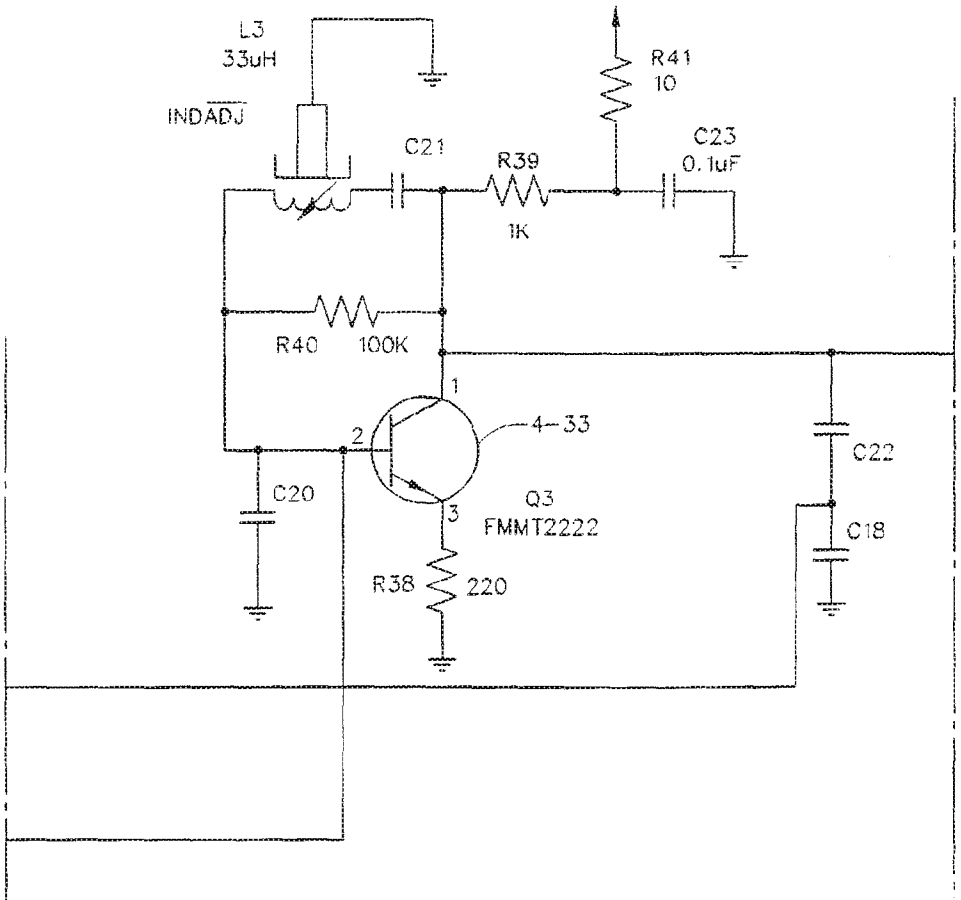

FIG. 4B

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DEF0000554

FIG. 4C

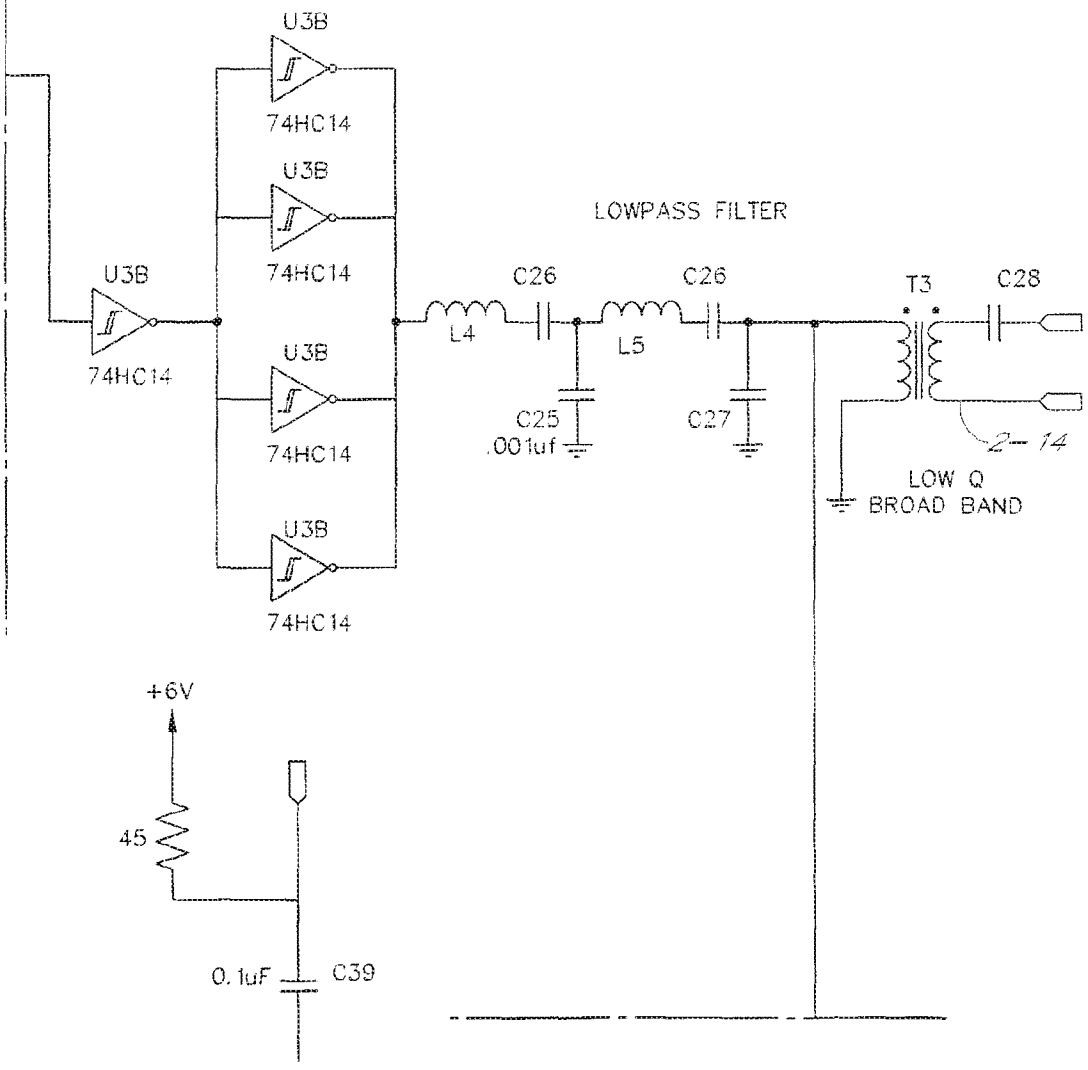
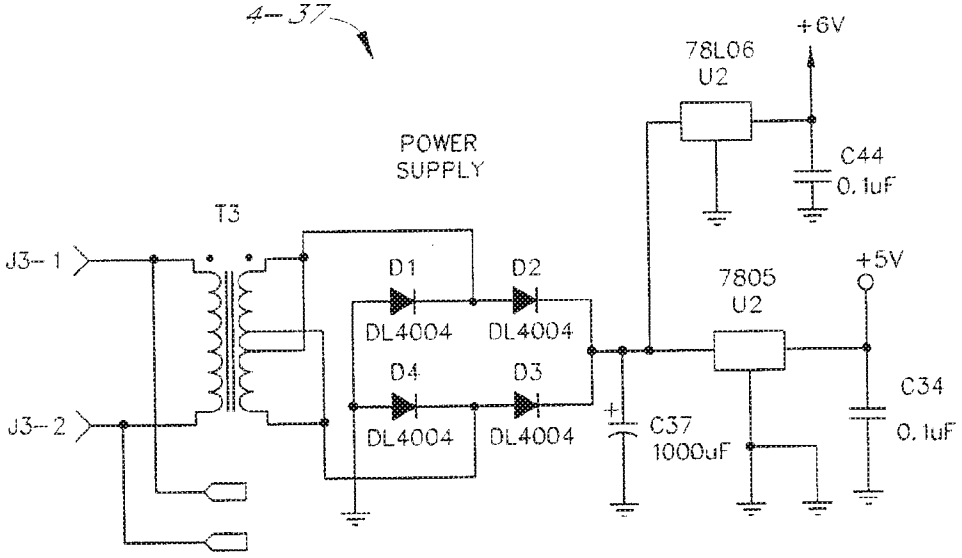

U3B
74HC14
U3B
74HC14
U3B
74HC14
U3B
74HC14
U3B
74HC14
LOWPASS FILTER
L4
C26
L5
C26
C25
.001uf
C27
T3
C28
2-14
LOW Q
BROAD BAND
+6V
45
0.1uF
C39

FIG. 4D



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DEF0000556

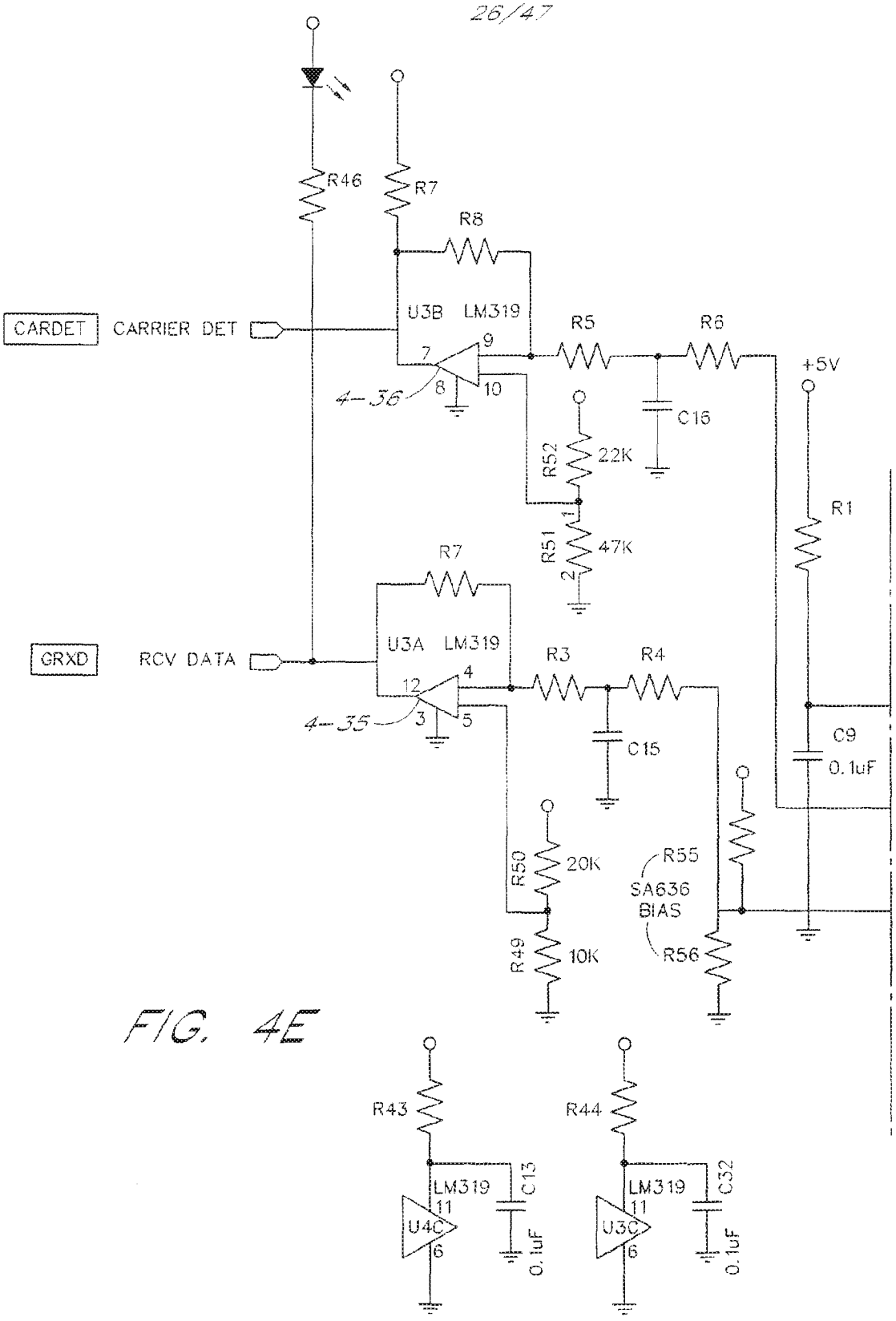
R46
R7
R8
CARDET
CARRIER DET
U3B LM319
7
9
8
10
4-36
R5
R6
+5V
C16
R52
22K
R1
R51
47K
2
1
R7
GRXD
RCV DATA
U3A LM319
12
4
3
5
4-35
R3
R4
C15
C9
0.1uF
R50
20K
R55
SA636
BIAS
R49
10K
R56
R43
R44
LM319
11
U4C
6
C13
0.1uF
LM319
11
U3C
6
C32
0.1uF

FIG. 4E

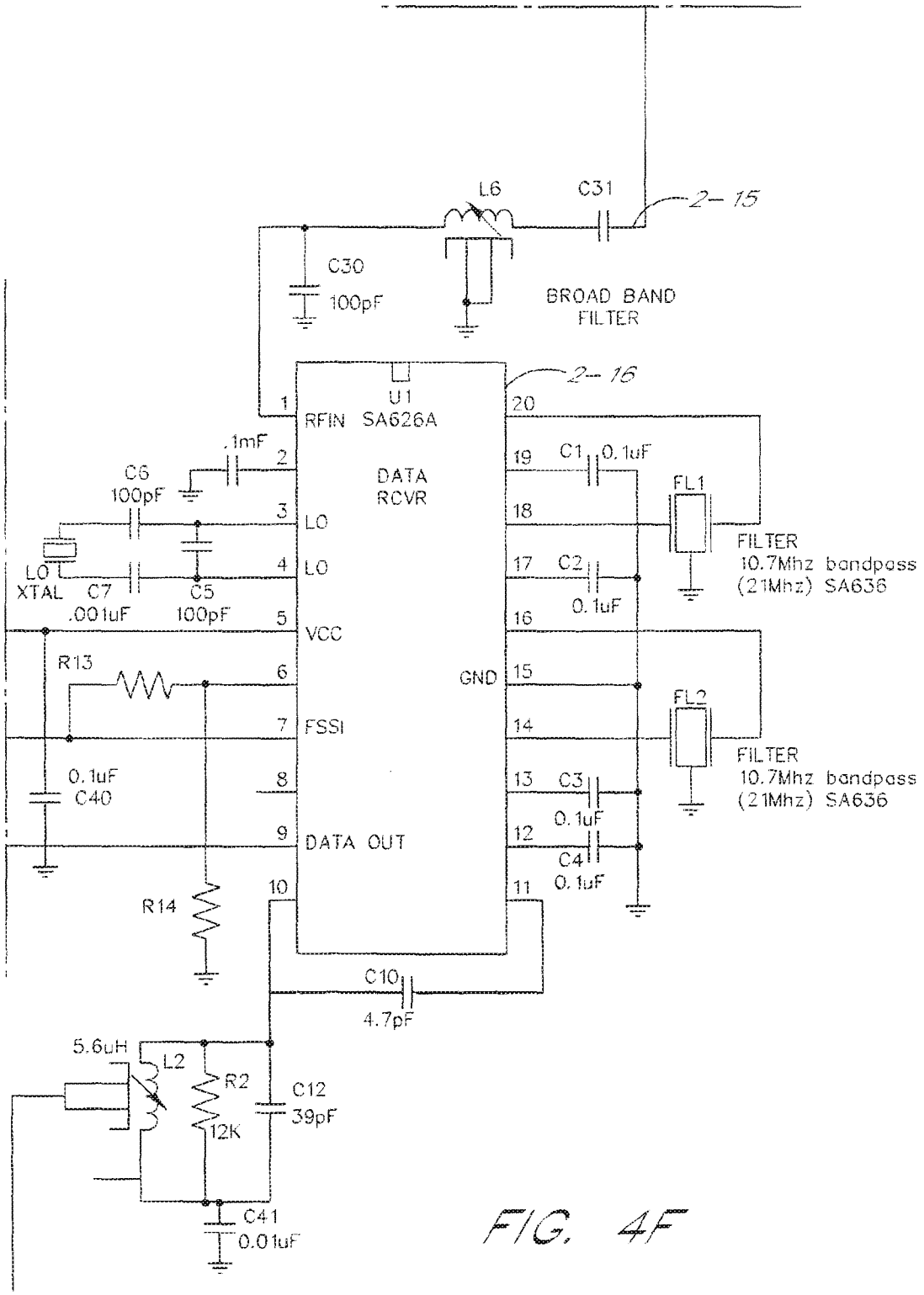
L6
C31
2-15
C30
100pF
BROAD BAND
FILTER
2-16
U1
RFIN SA626A
DATA
RCVR
.1mF
C6
100pF
LO
XTAL
C7
.001uF
C5
100pF
LO
LO
VCC
R13
FSSI
0.1uF
C40
DATA OUT
R14
C10
4.7pF
5.6uH
L2
R2
12K
C12
39pF
C41
0.01uF
C1
0.1uF
FL1
FILTER
10.7Mhz bandpass
(21Mhz) SA636
C2
0.1uF
GND
FL2
FILTER
10.7Mhz bandpass
(21Mhz) SA636
C3
0.1uF
C4
0.1uF

FIG. 4F

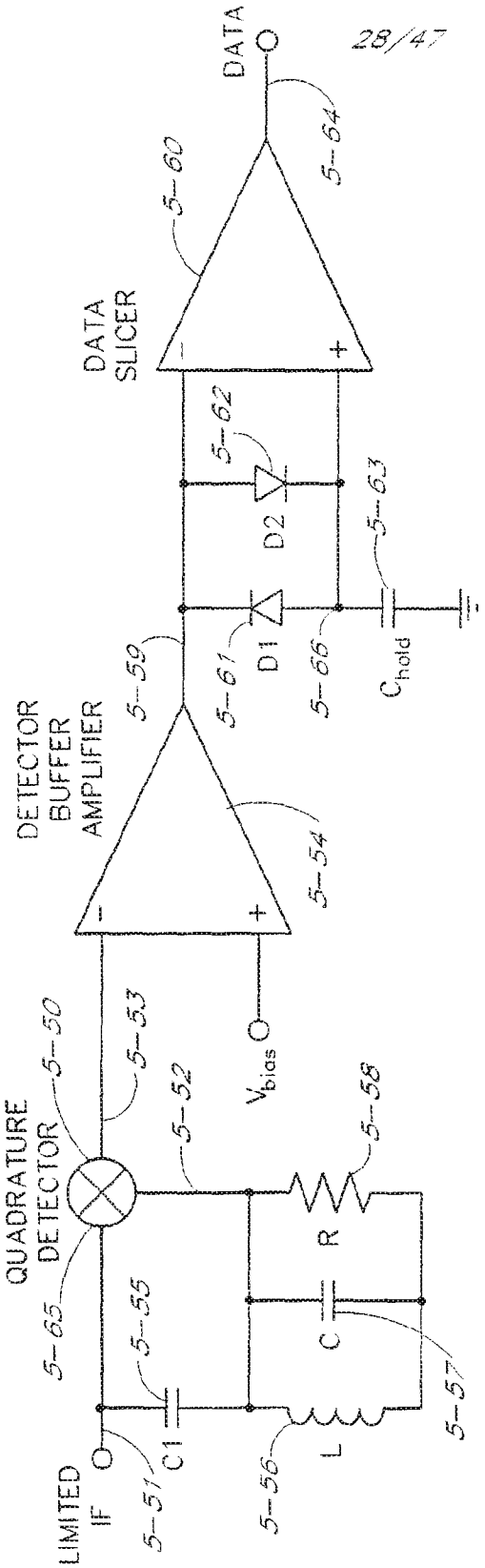

FIG. 5

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DEF0000559

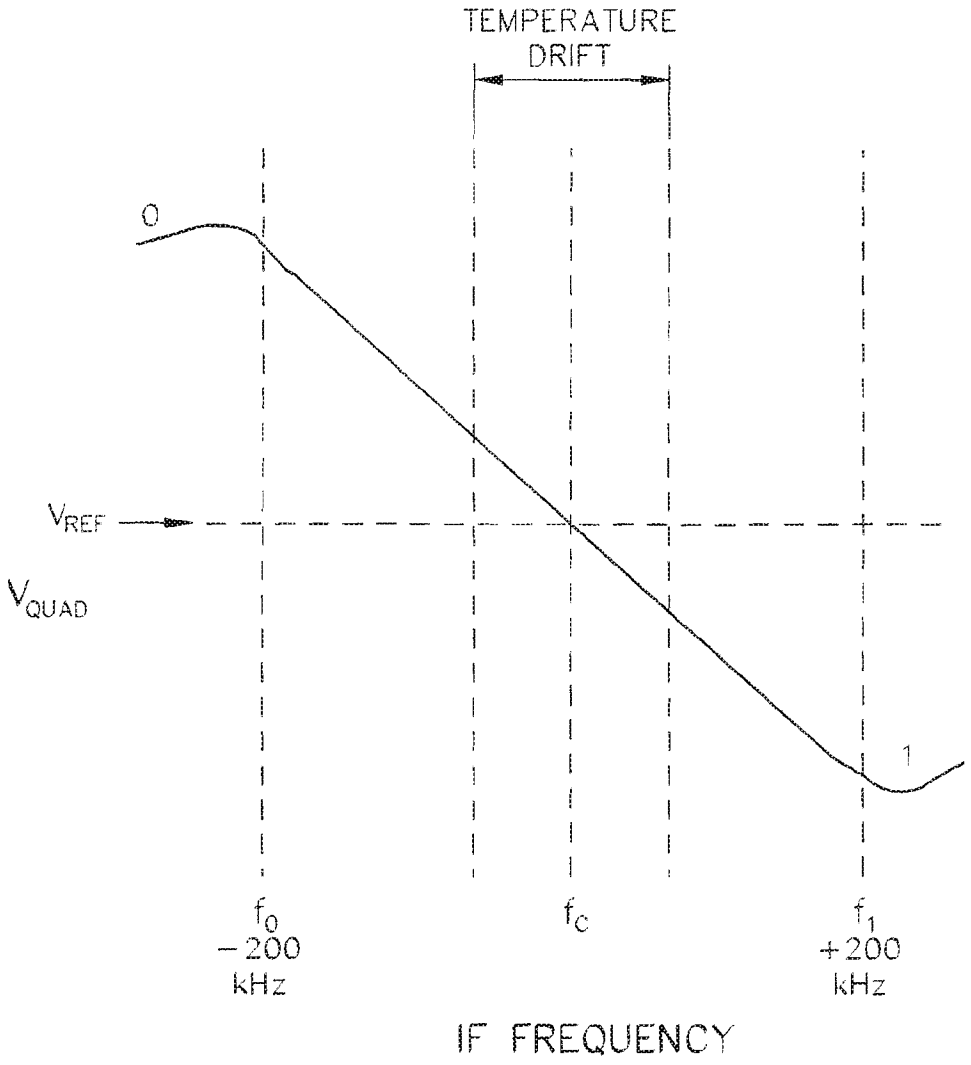

FIG. 6

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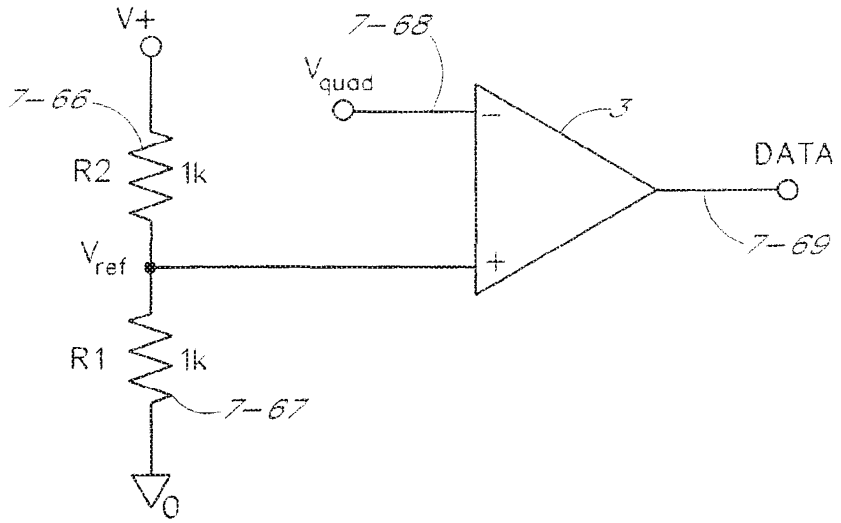
DEF0000560



DC-coupled FSK data comparator

FIG. 7A

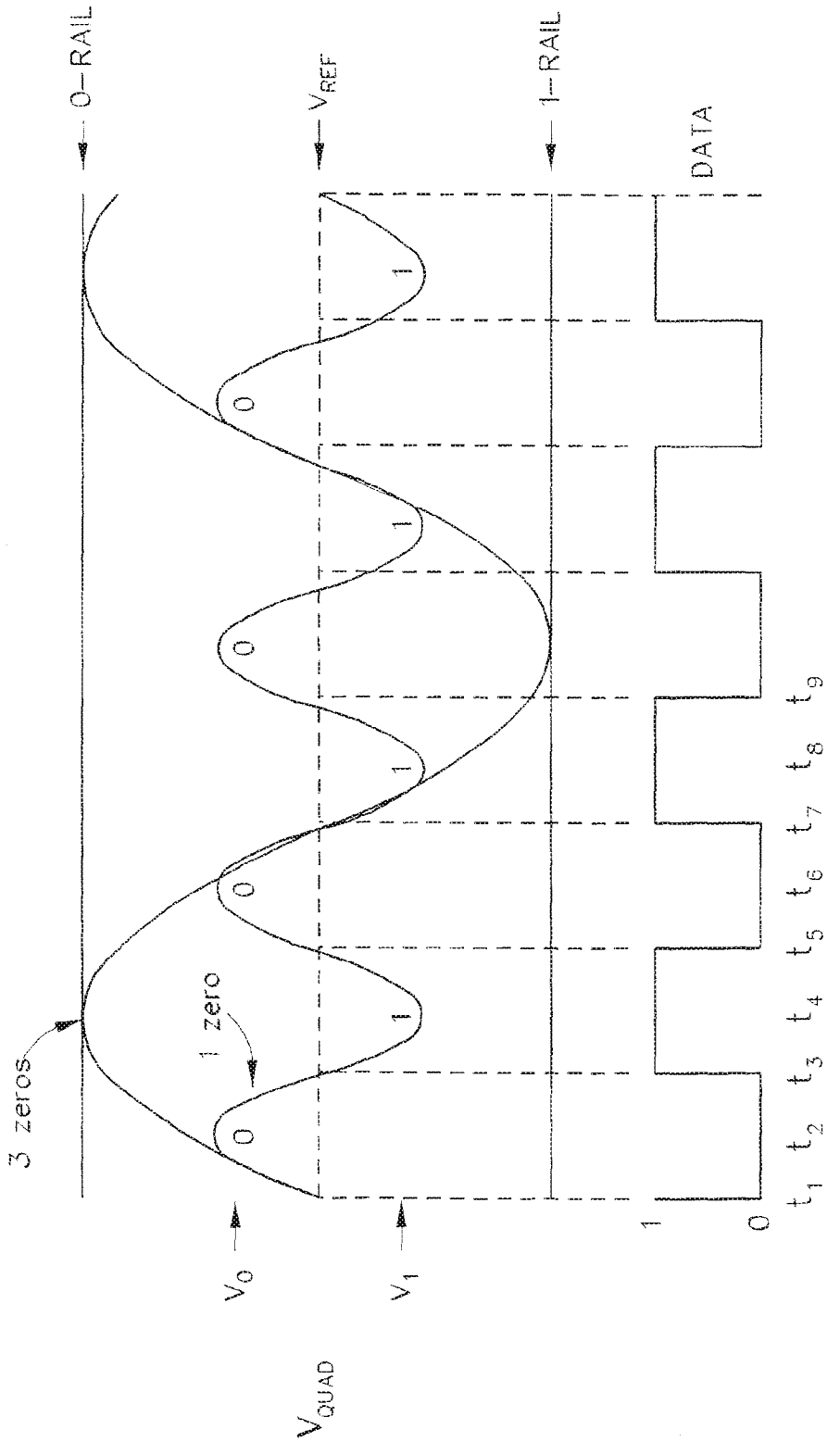


FIG. 7B

IDEAL OPERATION

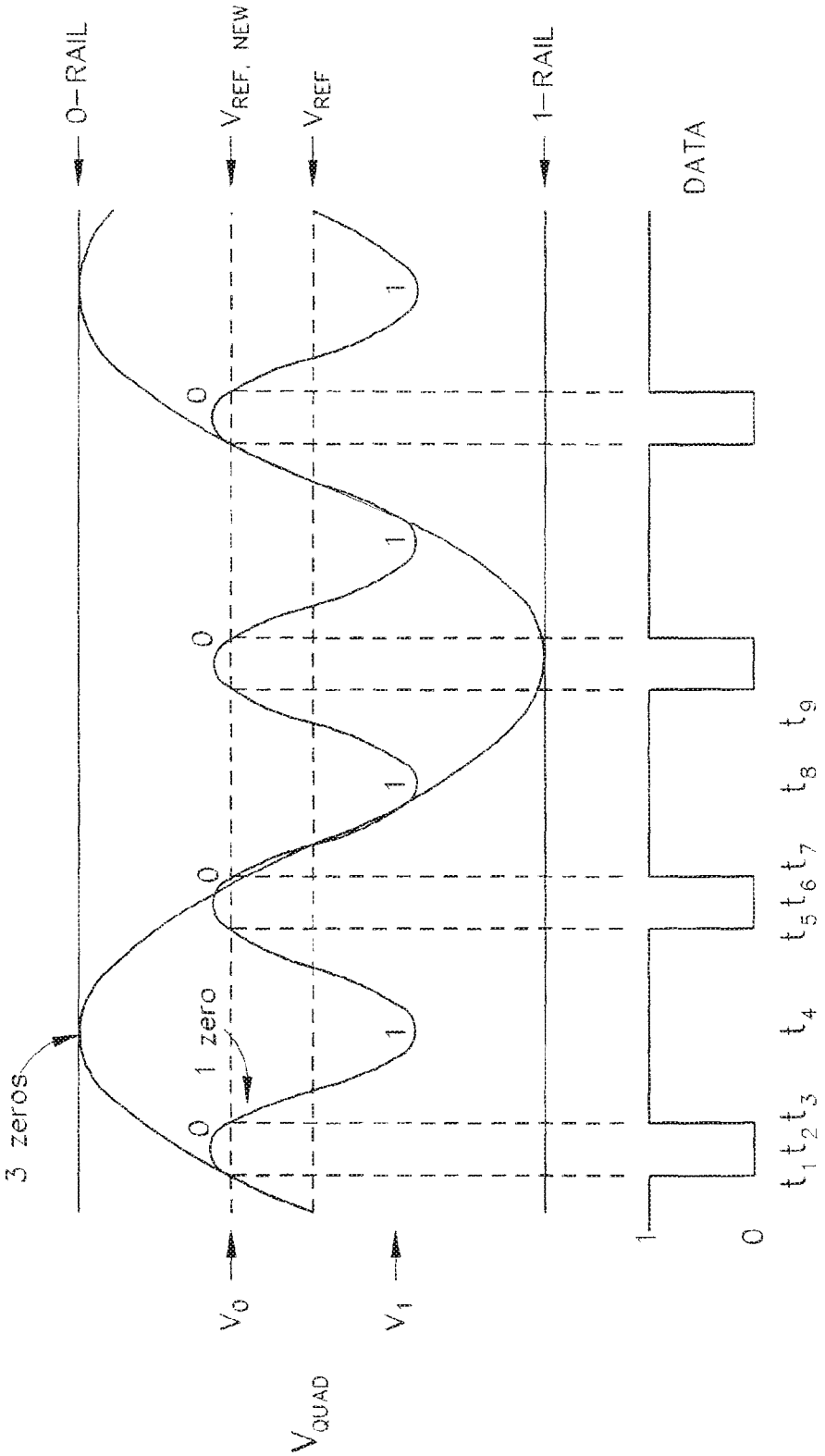
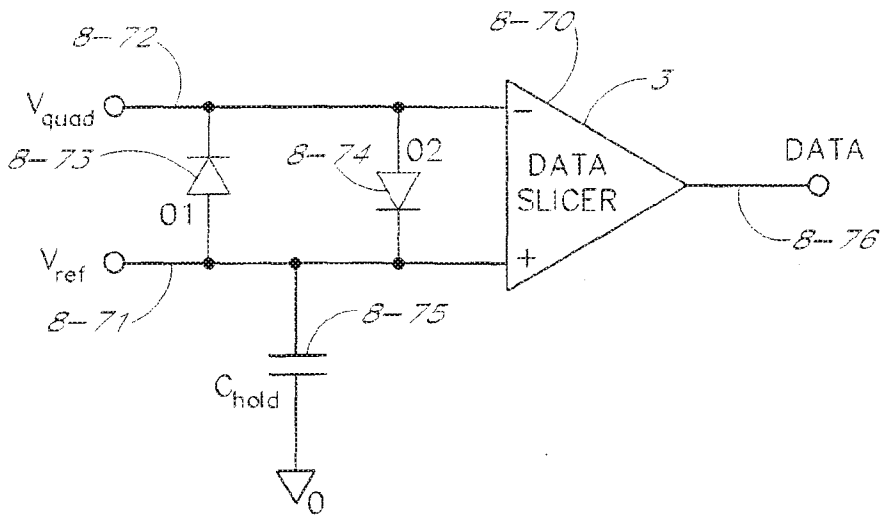


FIG. 7C

OPERATION WITH SIGNAL DRIFT



SLICER WITH TRACKING REFERENCE

FIG. 8A

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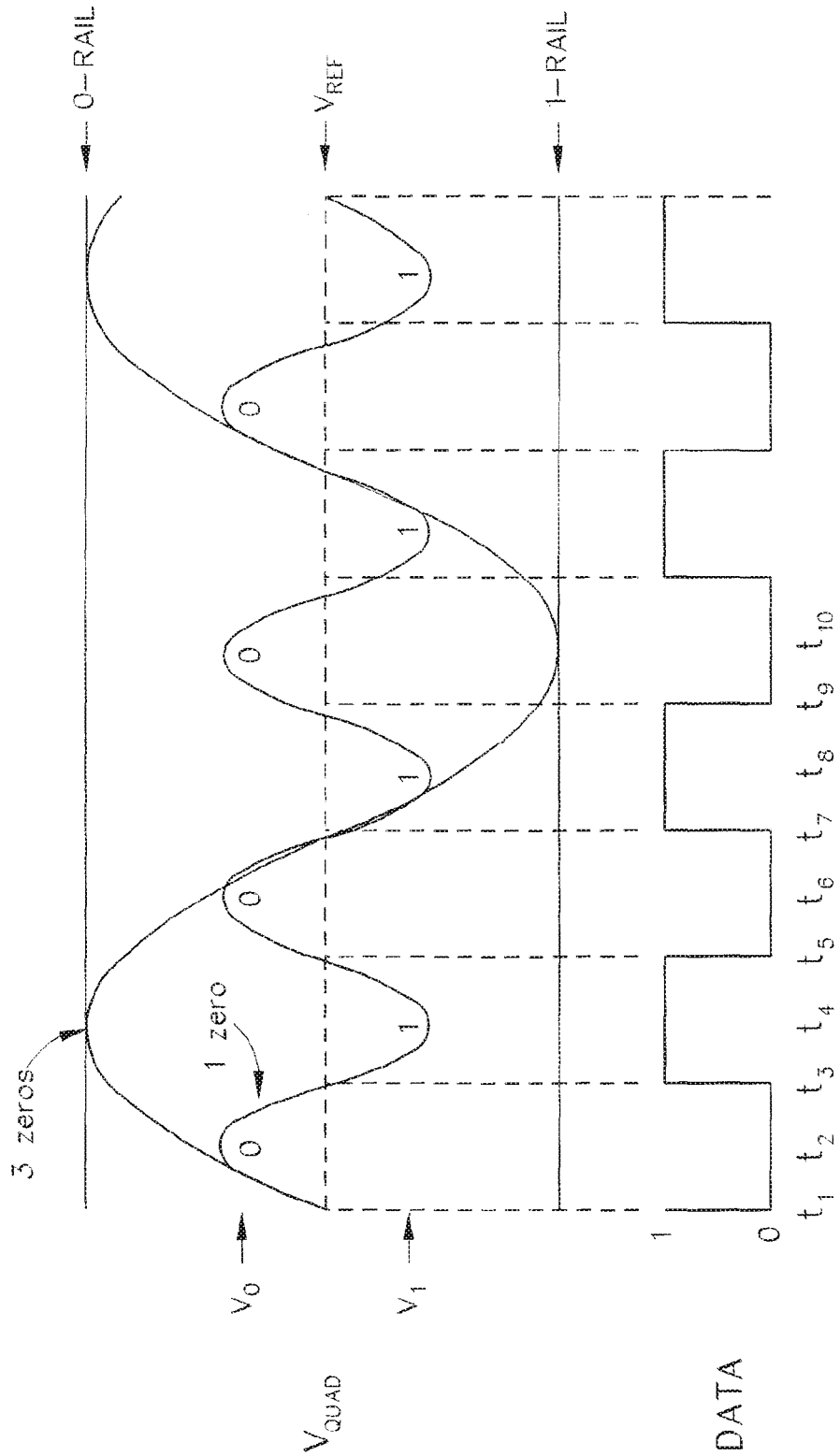
DEF0000564



IDEAL OPERATION

FIG. 8B

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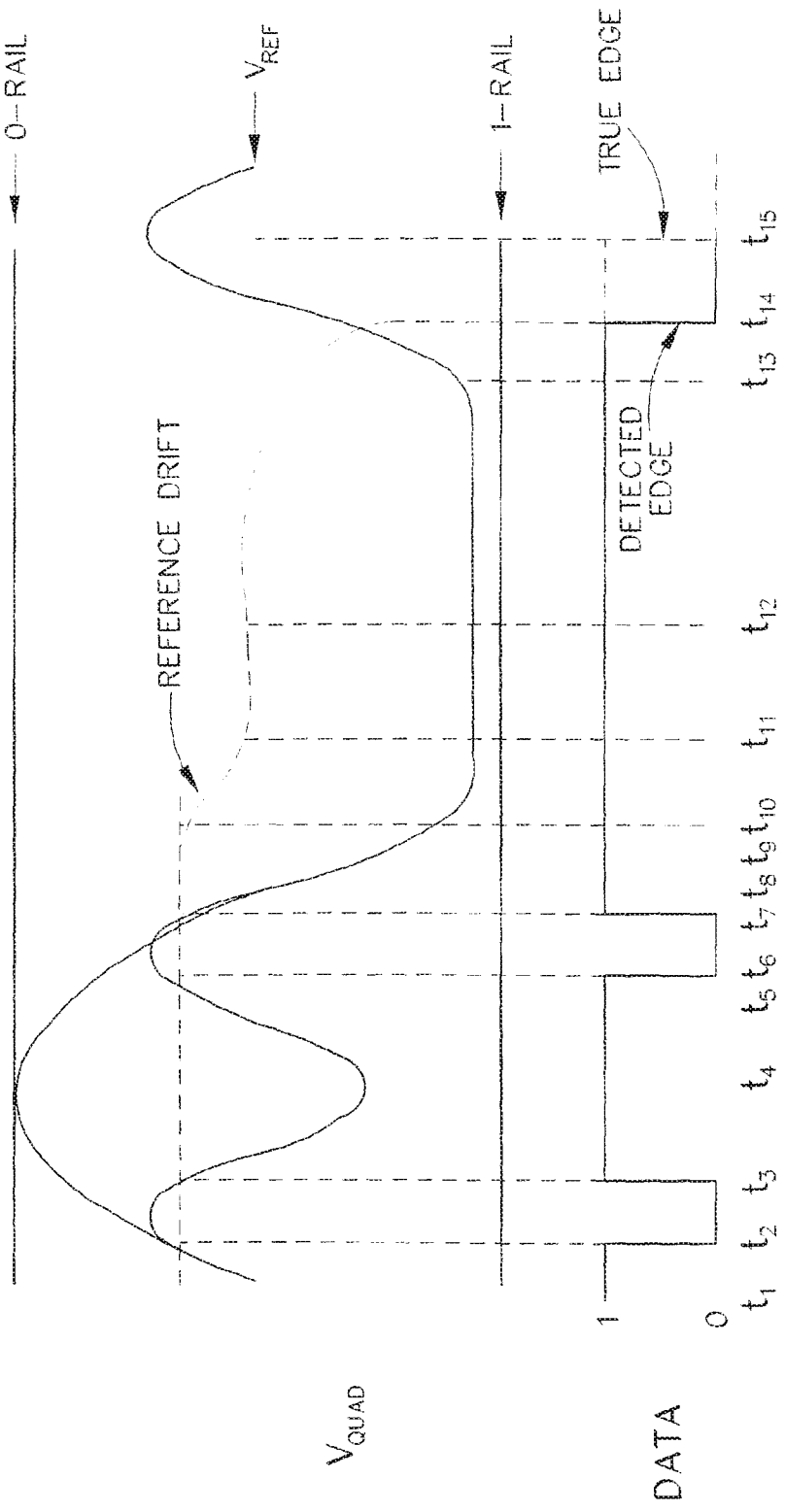
DEF0000565



OPERATION WITH REFERENCE DRIFT

FIG. 8C

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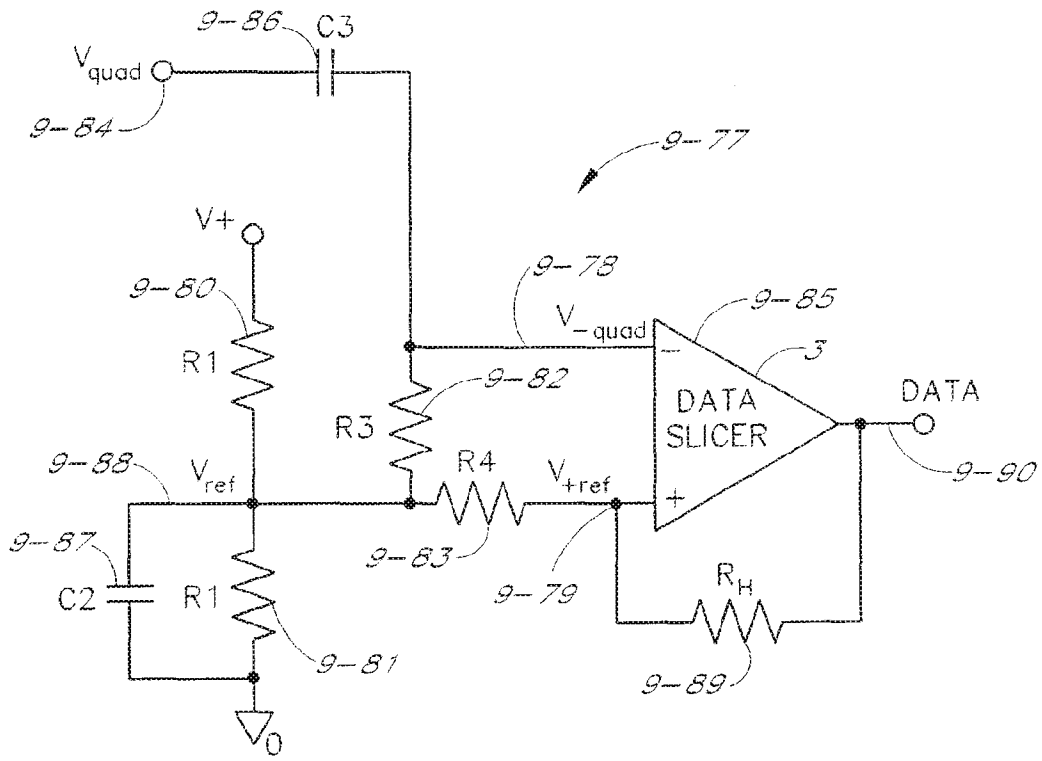
DEE0000566



AC-COUPLED SIGNAL

FIG. 9A

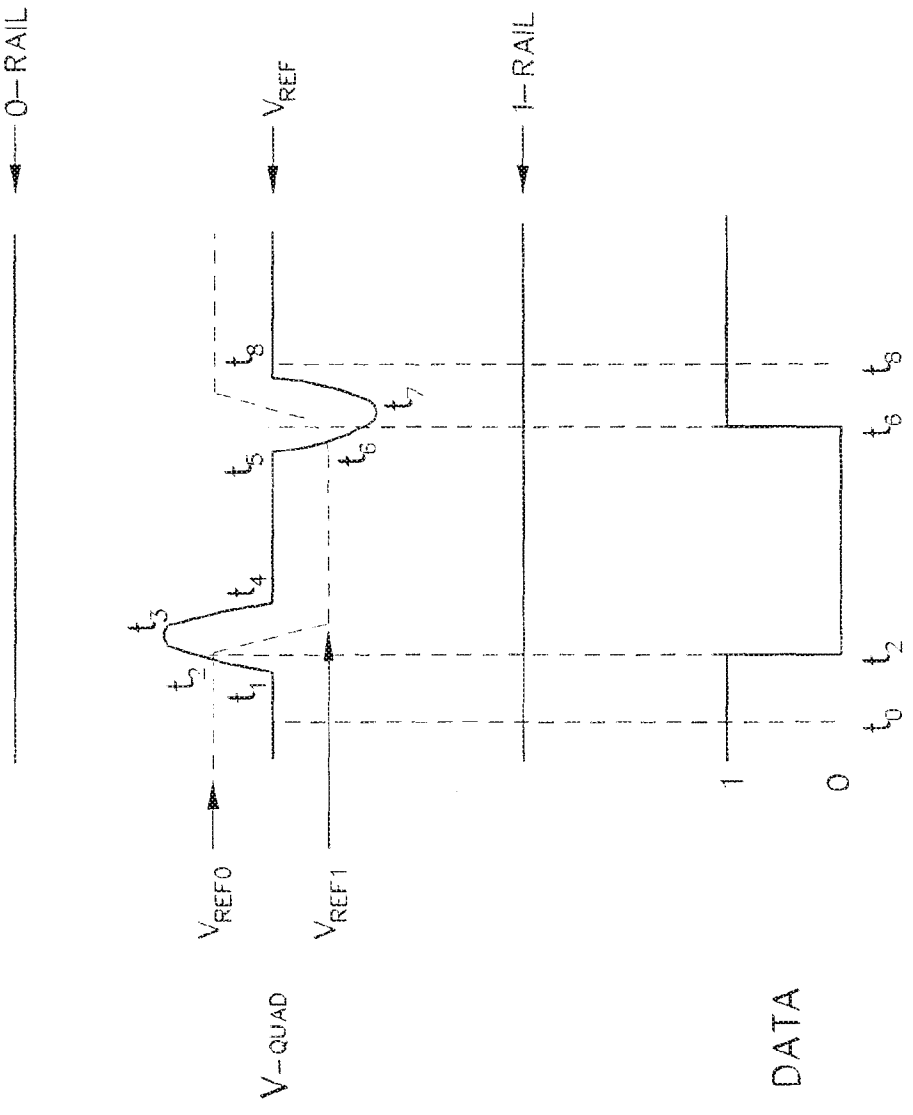


FIG. 9B

IPR2020-00034 Page 02138
DEF0000568

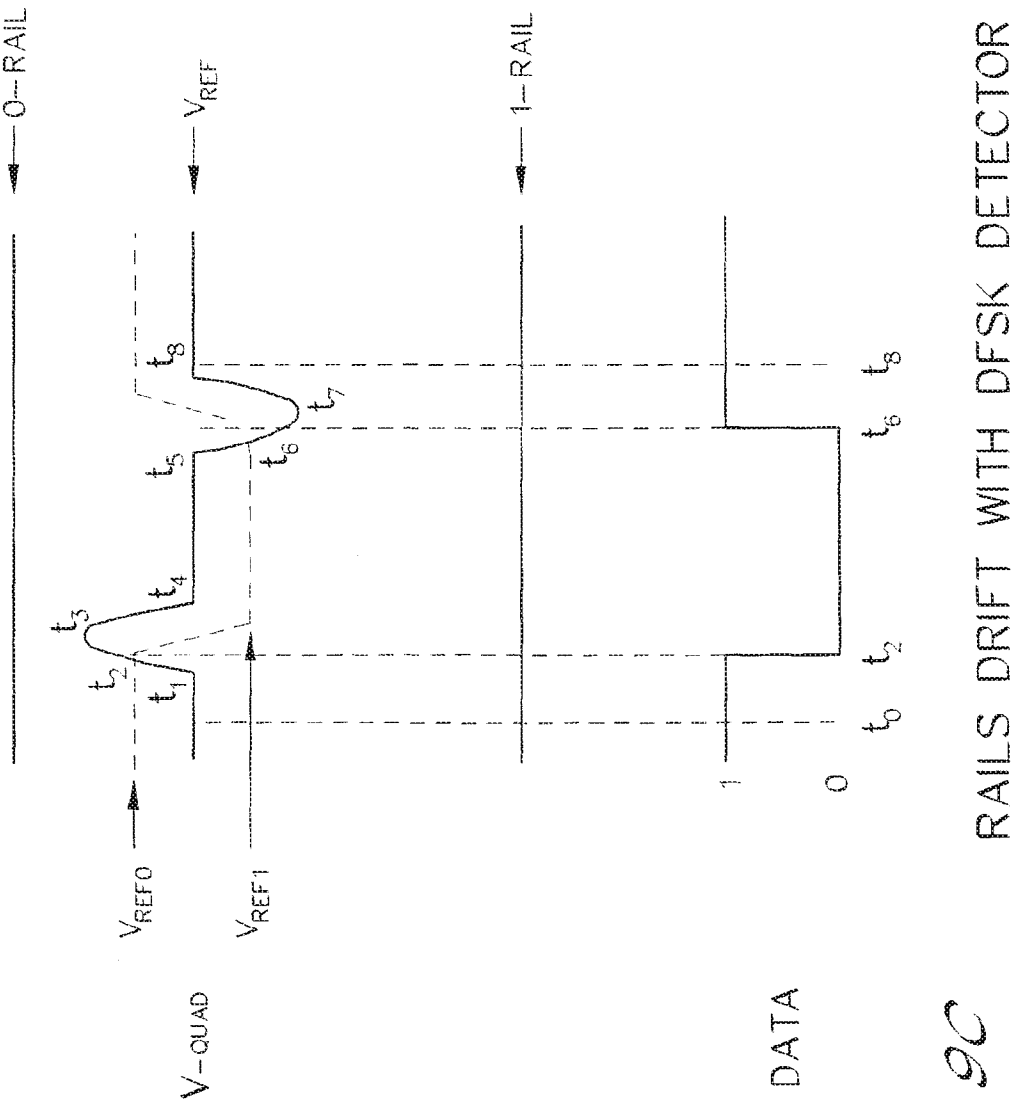


FIG. 9C

RAILS DRIFT WITH DFSK DETECTOR

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DEF0000569

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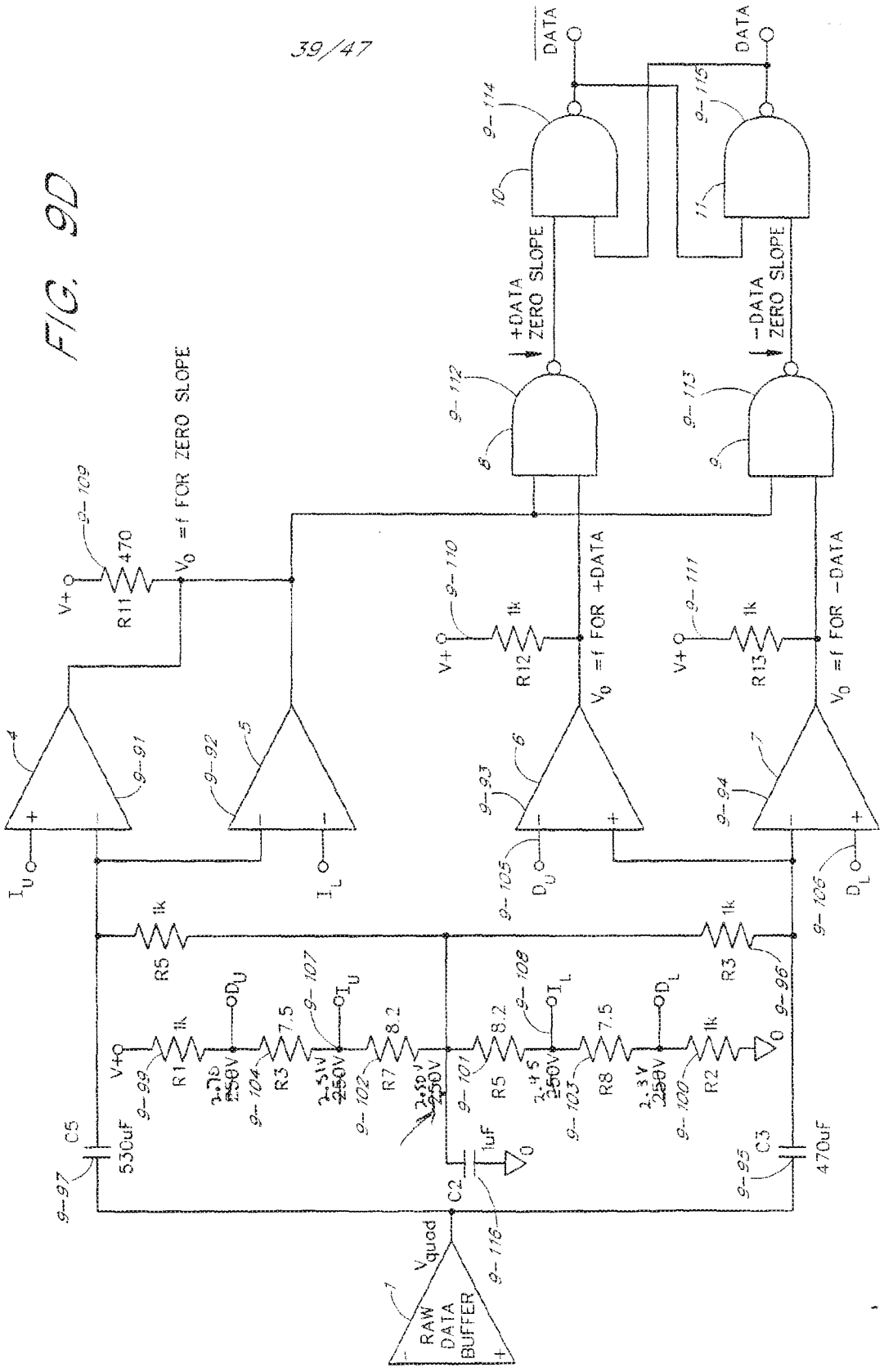
FIG. 9D



SUBSTITUTE SHEET (RULE 26)

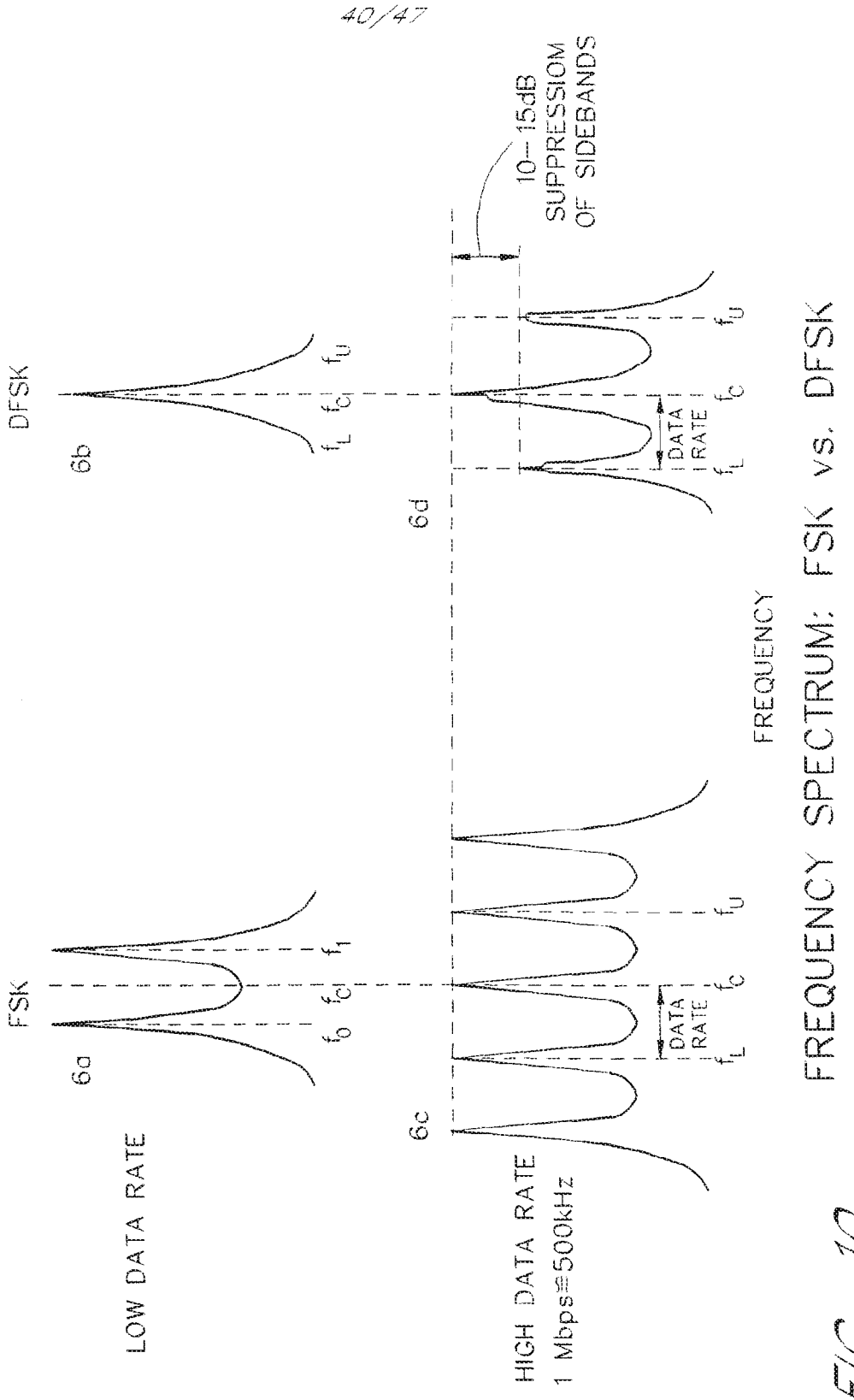


FIG. 10

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DEF0000571

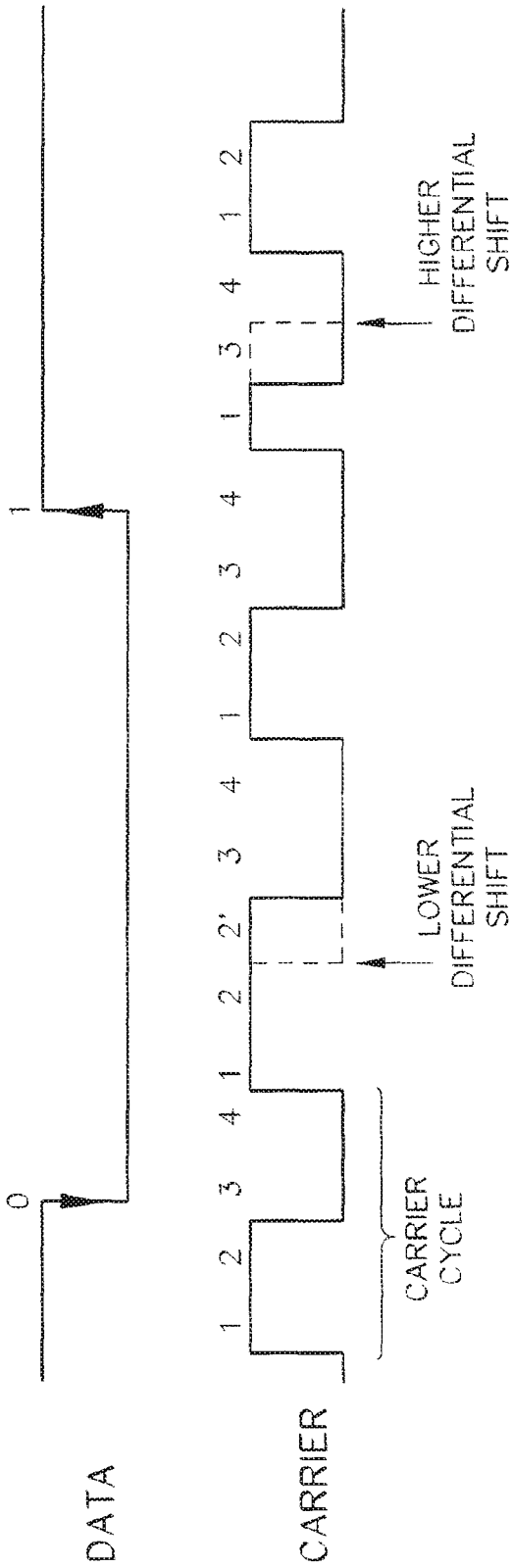

FIG. 11a

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DEF0000572

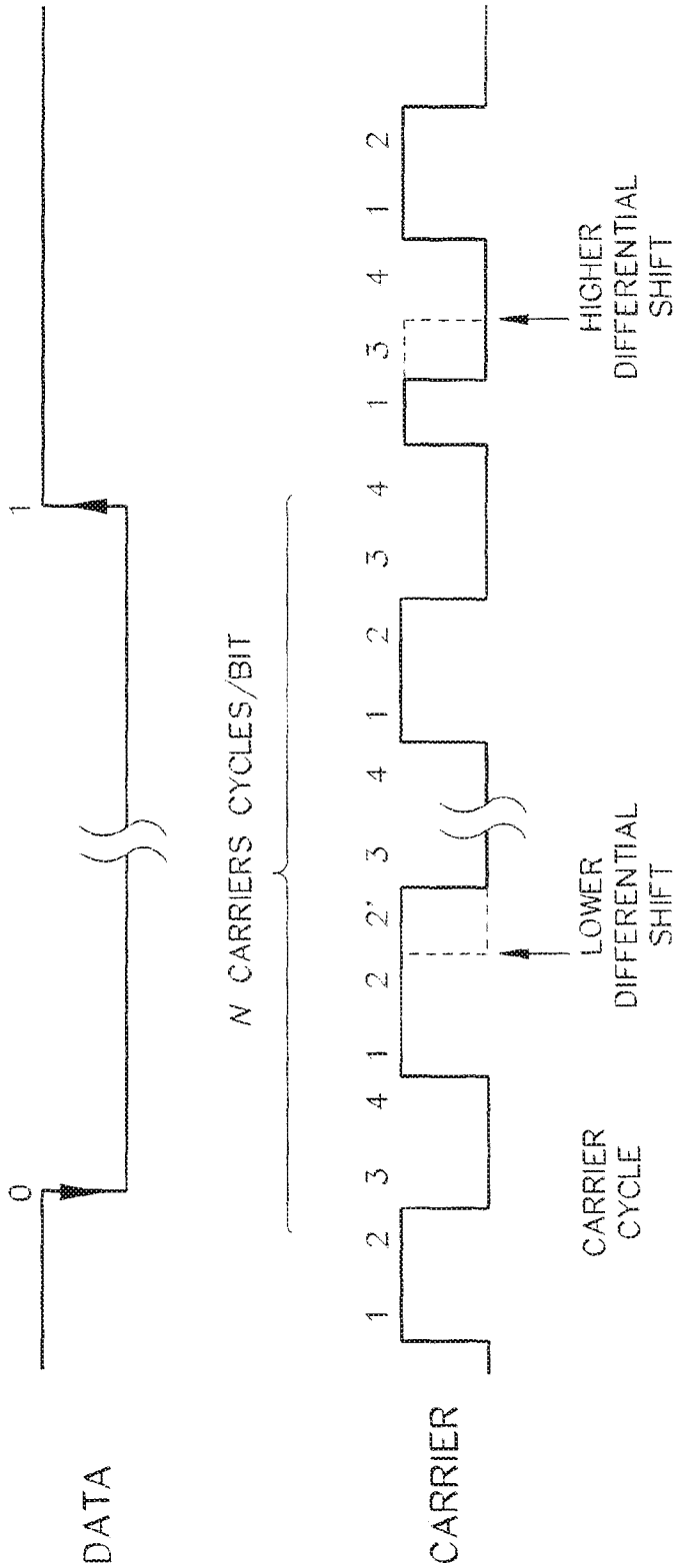

FIG. 11B

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DEF0000573

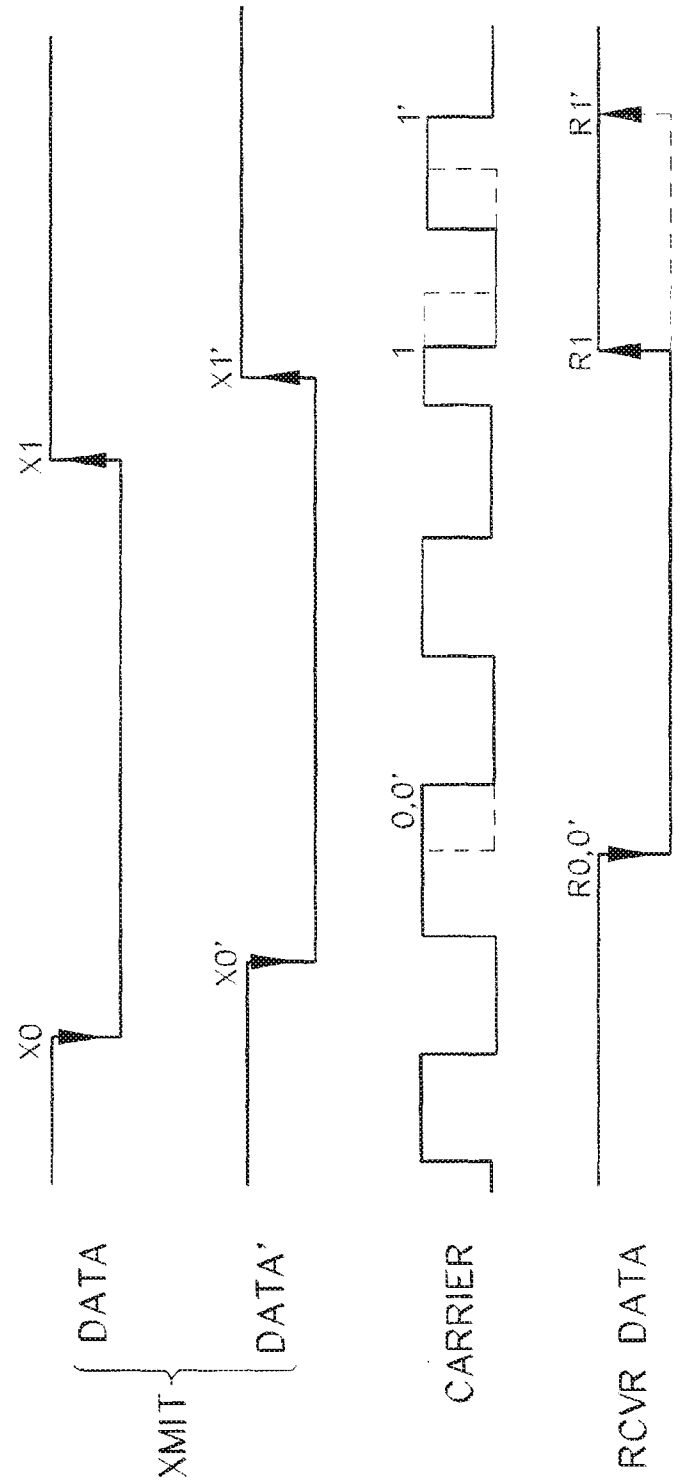

FIG. 12

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DEF0000574

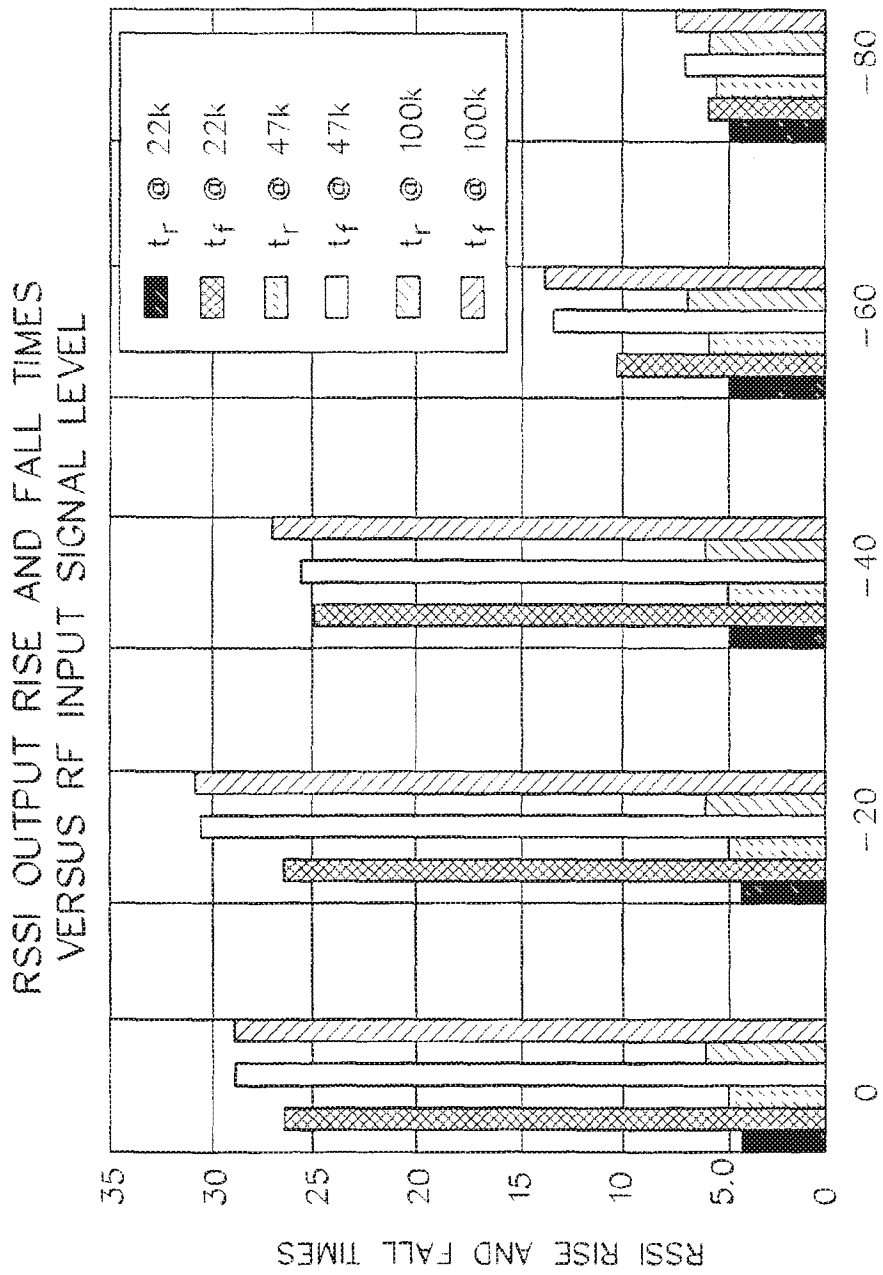
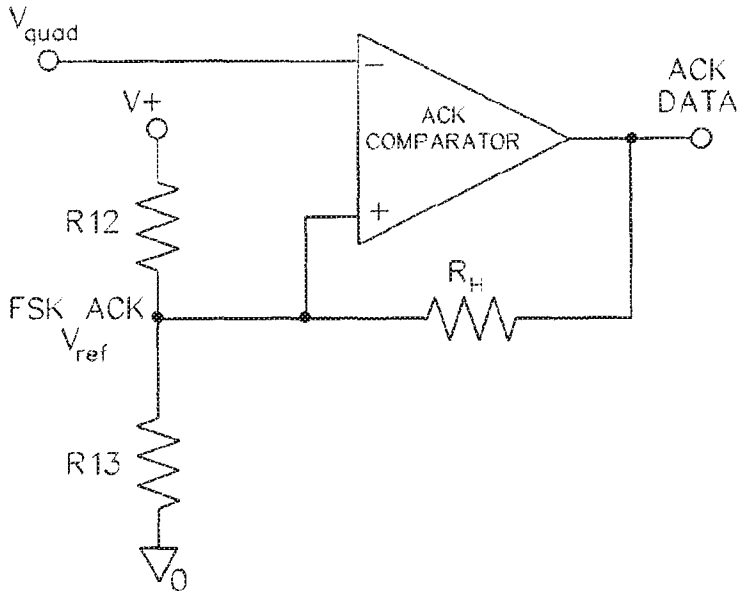


FIG. 13

IPR2020-00034 Page 02145
DEF0000575



ACK COMPARATOR

FIG. 14A

IPR2020-00034 Page 02146
DEF0000576

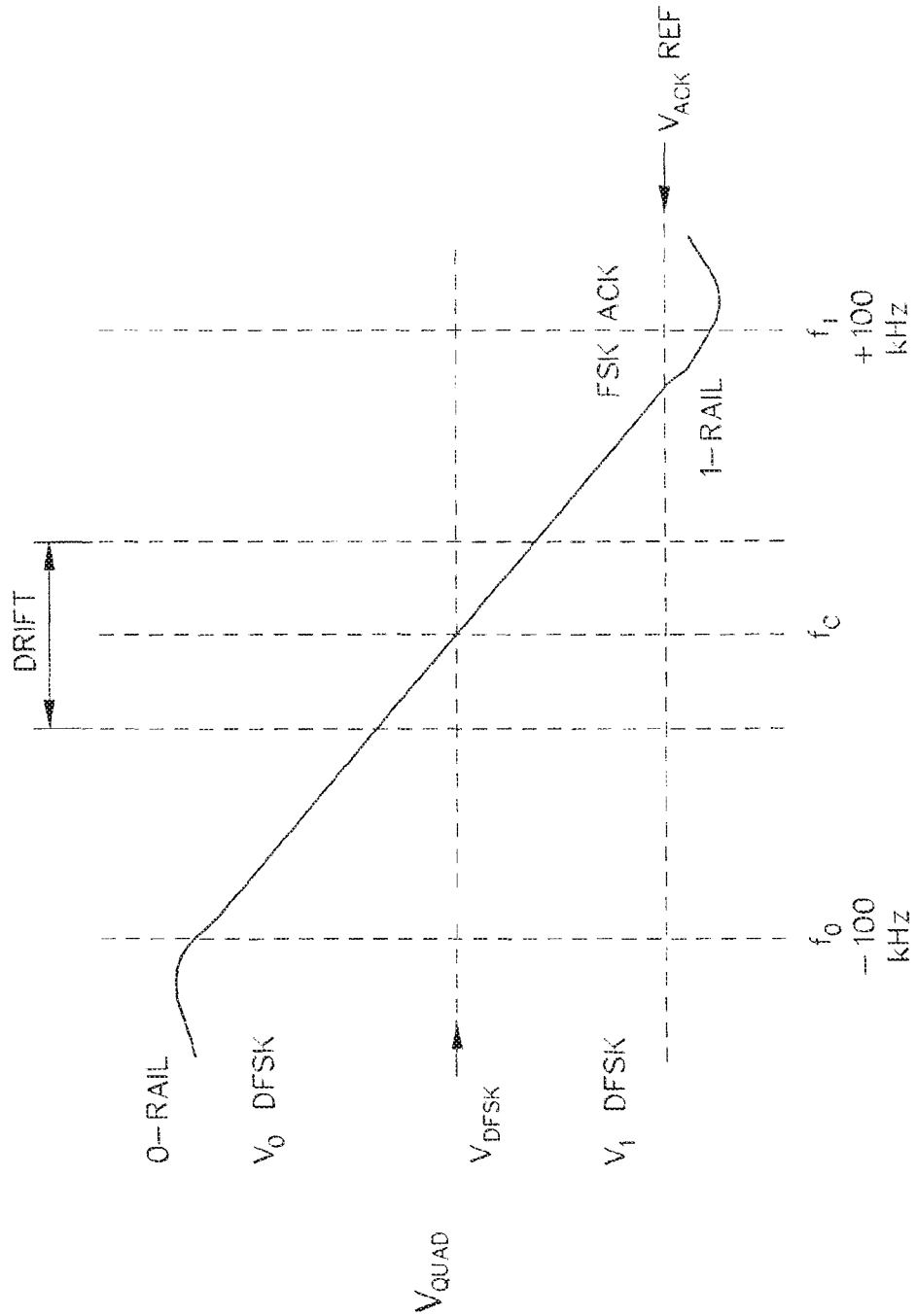


FIG. 14B

IPR2020-00034 Page 02147
DEF0000577

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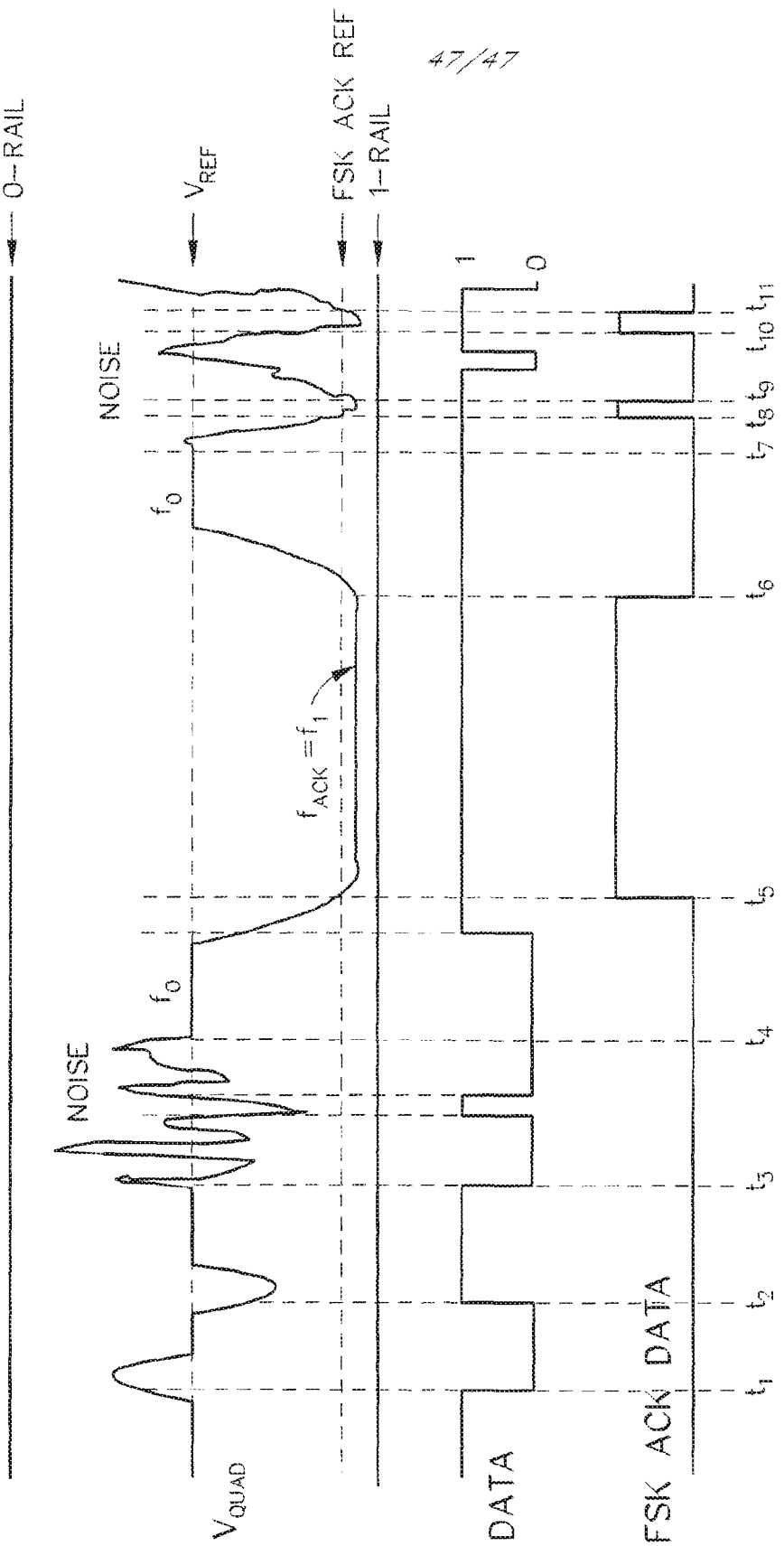

FIG. 15

IPR2020-00034 Page 02148
DEF0000578

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/11107

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G01R 31/08; H04H 27/10; H04L 27/10, 27/18, 5/16

US CL :Please See Extra Sheet.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 370/204, 205, 282, 284; 455/3.3, 403; 375/223, 244, 271, 272, 283, 303, 323, 329,330, 331, 332, 334, 346, 347, 350, 355

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4,580,276 A (ANDRUZZI et al) 01 April 1986, Fig. 2, Fig 4, and col. 8, lines 40-68.	1-24
Y	US 4,716,376 A (DAUDELIN) 29 December 1987, col. 1, line 65 to col.2, line 2.	1-24
Y	US 5,305,008 A (TURNER et al) 19 April 1994, col 10, line 47-56.	8
Y	US 4,001,692 A (FENWICK et al) 04 JAN 1977, col. 2, lines 5-7.	9

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search
26 AUGUST 1998

Date of mailing of the international search report
0 1 OCT 1998

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Authorized officer
STEVEN NGUYEN
Telephone No. (703) 308-8848

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/11107

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

370/204, 205, 282, 284; 455/3.3, 403; 375/223, 244, 271, 272, 283, 303, 323, 329,330, 331, 332, 334, 346, 347, 350, 355

Form PCT/ISA/210 (extra sheet)(July 1992)★

Electronic Acknowledgement Receipt

EFS ID:	33619229
Application Number:	90013808
International Application Number:	
Confirmation Number:	2211
Title of Invention:	SYSTEM AND METHOD OF COMMUNICATION USING AT LEAST TWO MODULATION METHODS
First Named Inventor/Applicant Name:	8023580
Customer Number:	6449
Filer:	Michael Vincent Battaglia/Keiko Shelton
Filer Authorized By:	Michael Vincent Battaglia
Attorney Docket Number:	3277-0114US-RXM1
Receipt Date:	05-SEP-2018
Filing Date:	12-SEP-2016
Time Stamp:	16:42:13
Application Type:	Reexam (Patent Owner)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Foreign Reference	F1_CA1081848.pdf	5984533 7fec4551dbf3ffb79ecda6be6f2ceb40b39b4f3b	no	52

Warnings:

Information:					
2	Foreign Reference	F2_CA2236686.pdf	1303344 59e567daa4e029ad0e4198e53bc910aece66e954	no	13
Warnings:					
Information:					
3	Foreign Reference	F3_EP0496427.pdf	1937713 96696f957131df73196d4fb184584482e835cea0	no	14
Warnings:					
Information:					
4	Foreign Reference	F4_EP0562875.pdf	18521678 336b820e7154b4c0c1900ff383c74a11fac1f074	no	179
Warnings:					
Information:					
5	Foreign Reference	F5_EP0584865.pdf	1856956 0632c4b8618eb0c014687ef226f9ea72085f5d3b	no	15
Warnings:					
Information:					
6	Foreign Reference	F6_EP0700175.pdf	310765 02d4161fbd77c55cd1630deecb7522aa18df5495	no	3
Warnings:					
Information:					
7	Foreign Reference	F7_EP0730251.pdf	3072760 c66b28e6976cb821030824b70325b550e5197c9c	no	27
Warnings:					
Information:					
8	Foreign Reference	F8_EP0772923.pdf	425994 2545df579c891782f09349c077f5595b84206bef	no	4
Warnings:					
Information:					

9	Foreign Reference	F9_EP0774850.pdf	4249608 4d97b640fe1cef860e47b342b9b29dd0e6b06118	no	38
Warnings:					
Information:					
10	Foreign Reference	F10_EP_0845916.pdf	2081461 29d1509a8fd4d9d3eec44abf3203c64961cbbd45	no	16
Warnings:					
Information:					
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Warnings:					
Information:					
12	Foreign Reference	F12_JPS59113515.pdf	526393 396ebac00c0e77aba31f0c8f9b661f3028201e17	no	5
Warnings:					
Information:					
13	Foreign Reference	F13_MX9603371A.pdf	2960446 b9b4a9b9424f97f8a3bc9cc156b56b11929 5a3d8	no	48
Warnings:					
Information:					
14	Foreign Reference	F14_WO_198302379.pdf	6411008 fd421d5e5f9667851090034463ec44a6978 9ac24	no	51
Warnings:					
Information:					
15	Foreign Reference	F15_WO_199105427.pdf	576869 608fe582af68242b21d34b4d2df2444ac1f7feef	no	12
Warnings:					
Information:					

16	Foreign Reference	F16_WO_199400943.pdf	2680335 b0933c2f07b4150e1ec1a1f25443d4348a544283	no	29
Warnings:					
Information:					
17	Foreign Reference	F17_WO_199419892.pdf	1844189 636b9b999f26678ac287d9d95a1d9ad2294fecb7	no	16
Warnings:					
Information:					
18	Foreign Reference	F18_WO_199628946.pdf	4145895 dc7d483ad7579b5109367a14b08ce9a7233b0ba3	no	39
Warnings:					
Information:					
19	Foreign Reference	F19_WO_199715131.pdf	912893 bd862bfdb1cc7bac3ed7293292795f9c4a3759c2	no	9
Warnings:					
Information:					
20	Foreign Reference	F20_WO_199724828.pdf	12025836 187f706713898cb3f32601f5189b267d5ebc6504	no	129
Warnings:					
Information:					
21	Foreign Reference	F21_WO_199837713.pdf	436446 93bd6584d3ccb08badf81a1891a7809bdb9d9d53	no	4
Warnings:					
Information:					
22	Foreign Reference	F22_WO_199859254.pdf	8140922 a8f32020e811746e84d3c930bd09fe43c3f277a2	no	91
Warnings:					
Information:					

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Warnings:					
Information:					
24	Non Patent Literature	3.pdf	1027893 de178e35e0944ddb4ae83031b45d3624e4f3d4a6	no	9
Warnings:					
Information:					
25	Non Patent Literature	4.pdf	517942 a71ac954e249368b0a3240ae7f472405ec874e11	no	4
Warnings:					
Information:					
26	Non Patent Literature	5.pdf	667915 277fe5b45ce841bf5d047c5a09b55fe5f05f9d5d	no	6
Warnings:					
Information:					
27	Non Patent Literature	6.pdf	8907334 47fc4253c33be37db9d4a59c16526e5f894801c9	no	12
Warnings:					
Information:					
28	Non Patent Literature	7.pdf	16221635 a8430c60350edb95c4b32e1e0216e33d6fbdc779	no	103
Warnings:					
Information:					
29	Non Patent Literature	8.pdf	1949017 746552a580d71a4b58212c7442d8155213a0c0f3	no	13
Warnings:					
Information:					

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Warnings:					
Information:					
31	Non Patent Literature	10.pdf	3573445 a8c72dbeb8a3d000d7f46ce68679ff911fe12752	no	11
Warnings:					
Information:					
32	Non Patent Literature	11.pdf	272763 04efea948de4659de6e4873496b2f19c541d18bb	no	31
Warnings:					
Information:					
33	Non Patent Literature	13.pdf	1091699 09151fe50821b284c5c85a9f5368879da199222b	no	5
Warnings:					
Information:					
34	Non Patent Literature	14.pdf	1001729 88e608410d88c5ecc440ccf4bae8d5b2a64e822f	no	5
Warnings:					
Information:					
35	Non Patent Literature	15.pdf	1464628 59a2d8674ee40258509b8ec3679ddc9e35da0894	no	24
Warnings:					
Information:					
36	Non Patent Literature	16.pdf	2174497 45c0ae16a430864adc48d8007ddeb8d98ca5f44e	no	24
Warnings:					
Information:					

37	Non Patent Literature	17.pdf	2383951 a4a8e3b80c1bfacc2296112e50b90049ba83098b	no	23
Warnings:					
Information:					
38	Non Patent Literature	18_A.pdf	1281826 e8bd5b6fad67d46d0889ed7bc41f12d5f4d6ba43	no	16
Warnings:					
Information:					
39	Non Patent Literature	18_B.pdf	781621 9d8629e49561e012a4226f473e916f1079476a4a	no	10
Warnings:					
Information:					
40	Non Patent Literature	18_C.pdf	1979097 1917c7d7f151b896a66a637ec84e785087a9d4a1	no	22
Warnings:					
Information:					
41	Non Patent Literature	18_D.pdf	920650 133fd136ee6fa4246250e63a63f4aac61377ba5b	no	11
Warnings:					
Information:					
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Warnings:					
Information:					
43	Non Patent Literature	19.pdf	975028 d67c55a865cfd6f0cc43a386faa2599fd56af026	no	5
Warnings:					
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44	Non Patent Literature	20.pdf	2241778 0ffed5b76d7d3f60f5e08a25a7a437b82d08b09a	no	11
Warnings:					
Information:					
45	Non Patent Literature	21.pdf	370019 b53c4b22144c966b5bee8ac94ede112c50d4ce3c	no	3
Warnings:					
Information:					
46	Non Patent Literature	22_A.pdf	10804805 360c8f04f9ed9b1d6926689b6fc472508e760cee	no	112
Warnings:					
Information:					
47	Non Patent Literature	22_B.pdf	1643633 c915a870dc1ffa797b8705b968bd7716a9e4befe	no	21
Warnings:					
Information:					
48	Non Patent Literature	24.pdf	1953518 0958deaac13c471dc073b126f538b38a05cd2844	no	8
Warnings:					
Information:					
49	Non Patent Literature	25.pdf	2472170 0cd8e2dc5c2cbf14cbb5bd7ec9fd7fec8d526b87	no	8
Warnings:					
Information:					
50	Non Patent Literature	26.pdf	2489178 7051ccd207bb4fc1741be57c495c44e34442eb96	no	9
Warnings:					
Information:					

51	Non Patent Literature	27.pdf	919923 fc00e8c1c244391828e6d8cb6624af25d4f1af97	no	5
Warnings:					
Information:					
52	Non Patent Literature	29.pdf	178723 c1b70a2a89ed31ade1734fe708e50d12ab9aa5e3	no	2
Warnings:					
Information:					
53	Non Patent Literature	30.pdf	3277207 2186a2fbe8a203707c3715f7e7932cc0ebf83c7b	no	16
Warnings:					
Information:					
54	Non Patent Literature	31.pdf	689731 9d6c00019963eef90e43e8664accf19f0fde0476	no	4
Warnings:					
Information:					
55	Non Patent Literature	32.pdf	291562 caf5255648c315bd494813a8b4591ab6995a1abc	no	2
Warnings:					
Information:					
56	Non Patent Literature	12_A.pdf	25160903 0bc16a10b4dc6bd46cbf70f0869cdd93241107a3	no	192
Warnings:					
Information:					
57	Non Patent Literature	12_B.pdf	25129954 dcc76ae34014f7bb4aca3ae6e08f6fd7e20e2b40	no	198
Warnings:					
Information:					

58	Non Patent Literature	12_C.pdf	25136224 65cc048288d069b11733e20a67dc63434b553628	no	201

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Total Files Size (in bytes):	238997454

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	90013808
Filing Date	2016-09-12
First Named Inventor	Bremer (U.S. Patent No. 8,023,580)
Art Unit	3992
Examiner Name	Yuzhen GE
Attorney Docket Number	3277-114US-RXM1

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4630286		1986-12-16	Betts	
	2	5436901		1995-07-25	Koopman	
	3	5450404		1995-09-12	Koopman et al.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	90013808
	Filing Date	2016-09-12
	First Named Inventor	Bremer (U.S. Patent No. 8,023,580)
	Art Unit	3992
	Examiner Name	Yuzhen GE
	Attorney Docket Number	3277-114US-RXM1

	9	5809060	B1	1998-09-15	Cafarella et al.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	90013808
	Filing Date	2016-09-12
	First Named Inventor	Bremer (U.S. Patent No. 8,023,580)
	Art Unit	3992
	Examiner Name	Yuzhen GE
	Attorney Docket Number	3277-114US-RXM1

	20	4807253		1989-02-21	Haganauer	
	21	4833696		1989-05-23	Ichiyoshi	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	90013808
	Filing Date	2016-09-12
	First Named Inventor	Bremer (U.S. Patent No. 8,023,580)
	Art Unit	3992
	Examiner Name	Yuzhen GE
	Attorney Docket Number	3277-114US-RXM1

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	32	5369637		1994-11-29	Richardson	
	33	5394259		1995-02-28	Takahara	
	34	5438686		1994-08-01	Gehri	
	35	5533069		1996-07-02	Fleek	
	36	5535229		1996-07-09	Hain, Jr., et al.	
	37	5584057		1996-12-10	Dent	
	38	5592480		1997-01-07	Carney	
	39	5602669		1997-02-11	Chaki	
	40	5615297		1997-03-25	Davis	
	41	5649295		1997-07-15	Shober et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	90013808
	Filing Date	2016-09-12
	First Named Inventor	Bremer (U.S. Patent No. 8,023,580)
	Art Unit	3992
	Examiner Name	Yuzhen GE
	Attorney Docket Number	3277-114US-RXM1

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	P802.11 Draft Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specification.	
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	Art Unit	3992
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	Attorney Docket Number	3277-114US-RXM1

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	Art Unit	3992
	Examiner Name	Yuzhen GE
	Attorney Docket Number	3277-114US-RXM1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Michael V. Battaglia/	Date (YYYY-MM-DD)	2018-09-05
Name/Print	Michael V. Battaglia	Registration Number	64,932

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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EFS ID:	33622429
Application Number:	90013808
International Application Number:	
Confirmation Number:	2211
Title of Invention:	SYSTEM AND METHOD OF COMMUNICATION USING AT LEAST TWO MODULATION METHODS
First Named Inventor/Applicant Name:	8023580
Customer Number:	6449
Filer:	Michael Vincent Battaglia/Keiko Shelton
Filer Authorized By:	Michael Vincent Battaglia
Attorney Docket Number:	3277-0114US-RXM1
Receipt Date:	05-SEP-2018
Filing Date:	12-SEP-2016
Time Stamp:	16:43:53
Application Type:	Reexam (Patent Owner)

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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New International Application Filed with the USPTO as a Receiving Office

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CERTIFICATE OF SERVICE

It is hereby certified that on this 10th day of December, 2018, the foregoing **NOTICE OF EXPIRATION OF '580 PATENT, REQUEST FOR A *PHILLIPS* CLAIM CONSTRUCTION OF CLAIMS 2 AND 59 OF THE '580 PATENT, AND SUPPLEMENTAL BRIEF** was served, by first-class U.S. Mail, on the attorney of record for the third-party Requesters Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc., at the following address:

J. Steven Baughman, Esq.
Ropes & Gray LLP
IPRM – Floor 43
Prudential Tower
800 Boylston Street
Boston, Massachusetts 02199-3600
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Facsimile: 202-383-8371

/Michael V. Battaglia/
Michael V. Battaglia
Reg. No. 64,932

cc: Nancy J. Linck, Ph.D.
Counsel for Rembrandt Wireless Technologies, LP

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In *Ex Parte* Reexamination of	:	Group Art Unit: 3992
Gordon F. BREMER	:	
Patent No.: 8,023,580 B2	:	Control No.: 90/013,808
Issued: September 20, 2011	:	

Reexam Request Filed: September 12, 2016

For: SYSTEM AND METHOD OF COMMUNICATION USING AT LEAST TWO MODULATION METHODS

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ATTN: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

NOTICE OF EXPIRATION OF '580 PATENT, REQUEST FOR A *PHILLIPS* CLAIM CONSTRUCTION OF CLAIMS 2 AND 59 OF THE '580 PATENT, AND SUPPLEMENTAL BRIEF

In this above-referenced reexamination of claims 2 and 59 of U.S. Patent No. 8,023,580 ("the '580 Patent"), Patent Owner Rembrandt timely filed its Appeal Brief on March 19, 2018. The Office has not yet filed its Answer. Rembrandt submits this paper to notify the Office that the '580 Patent expired on December 5, 2018, a fact that impacts the pending appeal. In view of the '580 Patent's expiration, Rembrandt requests that the Office (1) construe claims 2 and 59, including the "at least two types of modulation methods" limitations, under *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316, 75 USPQ2d 1321, 1329 (Fed. Cir. 2005), and (2) in view of the proper construction under *Phillips*, reconsider and withdraw its rejections.

In the event that the rejections are not withdrawn, Rembrandt respectfully submits that good cause exists for the Board to consider the arguments below because (i) the term of the '580

Patent had not expired when the Appeal Brief was filed on March 19, 2018, and the authority cited below with respect to claim construction of an expired patent did not become relevant until the '580 Patent expired on December 5, 2018, and (ii) the arguments below are consistent with arguments made in the Appeal Brief. *See, e.g.,* Appeal Brief at 48-49, 52-55, 84, 88-89, 116-117.

Significantly, the Office's rejections and supporting arguments in its Final Office Action ("FOA") are based on the wrong claim construction in view of the expiration of the '580 Patent. And, in this case, the differences between the Office's construction and that under *Phillips* dictate a different outcome, given that none of the references (including the primary reference Snell) discloses or would have suggested at least two different families of modulation.

The proper claim construction of the '580 Patent under *Phillips* is a question of law that was finally and conclusively resolved in Rembrandt's favor by the Federal Circuit in *Rembrandt Wireless Technologies v. Samsung Electronics Co.*, 853 F.3d 1370, 1375-77 (Fed. Cir. 2017) -- an appeal brought by Samsung (the Requestor of this reexamination). The criticisms raised by the Office to Rembrandt's construction of "different types" were raised by the Requestor and were rejected by the Federal Circuit. As a result, the proper construction of the '580 Patent under *Phillips* is now settled law, and the Office is required to apply the Federal Circuit's claim construction going forward in this matter. *See, e.g., In re CSB-System International*, 832 F.3d 1335, 1341 (Fed. Cir. 2016 ("When a patent expires during a reexamination proceeding, the PTO should thereafter apply the *Phillips* standard for claim construction."). The court in *CSB-System* cited *Facebook, Inc. v. Pragmatus AV, LLC*, 582 Fed. Appx. 864, 868-69 (Fed. Cir. 2014) and noted that the court in *Facebook* "appl[ied] the *Phillips* standard when patent expired after the

Board's reexamination decision pending appeal to the Federal Circuit". 832 F.3d at 1341; MPEP § 2258(I)(G) ("In a reexamination proceeding involving claims of an expired patent, claim construction pursuant to the principle set forth by the court in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316, 75 USPQ2d 1321, 1329 (Fed. Cir. 2005) … should be applied since the expired claim are not subject to amendment. …").

In the related district court litigation, *Rembrandt Wireless Technologies v. Samsung Electronics Co.*, 853 F.3d 1370, 1375-77 (Fed. Cir. 2017), both the district court and the Federal Circuit applied a *Phillips* claim construction and determined that the limitation "modulation method [] of a different type" in claims 2 and 59 required at least two "different families of modulation techniques, such as the FSK family of modulation methods and the QAM family of modulation methods." *Id.* at 1377. The Office in this reexamination and the Board in the related IPRs refused to construe "modulation method [] of a different type" to require at least two "different families of modulation techniques." Instead they construed the claims under an alleged "broadest reasonable interpretation" and determined that their construction did not require at least two "different families of modulation techniques."

Given that the '580 Patent has expired, application of the broadest reasonable interpretation is no longer proper and cannot stand. Thus, Rembrandt respectfully requests that the outstanding rejections be reconsidered in light of the expiration of the '580 Patent and of the proper construction of "at least two different types" to require at least two "different families of modulation techniques," as Rembrandt previously requested prior to the '580 Patent's expiration. *See, e.g.,* Rembrandt's Appeal Brief, at 39-56; Claim Construction Order (Exhibit F to Appeal Brief) and the documents cited in Rembrandt's Appeal Brief relating to claim construction

(including the two Akl declarations). Additionally, Rembrandt submits the Declaration of Dr. Christopher R. Jones (previously submitted in IPR2014-518 as Ex. 2214) (attached), in which Dr. Jones explains why the modulation methods disclosed in Boer do not satisfy the limitations of claims 2 and 59 that require different modulation types (ones that are not in the same family), when properly construed under *Phillips*. Jones Decl. ¶¶ 28-41, 44, & 55-62. Dr. Jones' testimony regarding Boer would apply with at least equal force to the disclosure of BPSK and QPSK in Snell and Harris.

Any fee required for this submission may be charged to Counsel's Deposit Account Number 02-2135.

Respectfully submitted,

Date: December 10, 2018 By: /Michael V. Battaglia/

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ROTHWELL, FIGG, ERNST & MANBECK, P.C.
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Attorney for Petitioner
Rembrandt Wireless Technologies, LP

cc: Nancy J. Linck, Ph.D.
Counsel for Rembrandt Wireless Technologies, LP

Electronic Acknowledgement Receipt

EFS ID:	34538242
Application Number:	90013808
International Application Number:	
Confirmation Number:	2211
Title of Invention:	SYSTEM AND METHOD OF COMMUNICATION USING AT LEAST TWO MODULATION METHODS
First Named Inventor/Applicant Name:	8023580
Customer Number:	6449
Filer:	Michael Vincent Battaglia/Keiko Shelton
Filer Authorized By:	Michael Vincent Battaglia
Attorney Docket Number:	3277-0114US-RXM1
Receipt Date:	10-DEC-2018
Filing Date:	12-SEP-2016
Time Stamp:	16:55:36
Application Type:	Reexam (Patent Owner)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Notice.pdf	115937 e372b3edea28c08e6fc1b38f498a2f1391f1fed3	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Reexam Certificate of Service	5	5
	Notice of concurrent proceeding(s)	1	4

Warnings:					
Information:					
2	Trans Letter filing of a response in a reexam	DEC.pdf	520765 36eb377d23c49de02d0c1772726000969fccd922	no	40
Warnings:					
Information:					
		Total Files Size (in bytes):	636702		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/013,808	09/12/2016	8023580	3277-0114US-RXM1	2211

6449 7590 12/21/2018

ROTHWELL, FIGG, ERNST & MANBECK, P.C.
607 14th Street, N.W.
SUITE 800
WASHINGTON, DC 20005

EXAMINER
GE, YUZHEN

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
12/21/2018	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/013,808* .

PATENT UNDER REEXAMINATION *8023580* .

ART UNIT *3992* .

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Notice of Intent to Issue Ex Parte Reexamination Certificate	**Control No.** 90/013,808	**Patent Under Reexamination** 8023580	
	Examiner YUZHEN GE	**Art Unit** 3992	**AIA Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☑ Prosecution on the merits is (or remains) closed in this *ex parte* reexamination proceeding. This proceeding is subject to reopening at the initiative of the Office or upon petition. *Cf.* 37 CFR 1.313(a). A Certificate will be issued in view of
   (a) ☑ Patent owner's communication(s) filed: 10 December 2018.
   (b) ☐ Patent owner's failure to file an appropriate timely response to the Office action mailed: _____.
   (c) ☐ Patent owner's failure to timely file an Appeal Brief (37 CFR 41.31).
   (d) ☐ The decision on appeal by the ☐ Board of Patent Appeals and Interferences ☐ Court dated _____
   (e) ☐ Other: _____.
2. The Reexamination Certificate will indicate the following:
   (a) Change in the Specification: ☐ Yes ☑ No
   (b) Change in the Drawing(s): ☐ Yes ☑ No
   (c) Status of the Claim(s):
      (1) Patent claim(s) confirmed: 2 and 59.
      (2) Patent claim(s) amended (including dependent on amended claim(s)): _____
      (3) Patent claim(s) canceled: _____.
      (4) Newly presented claim(s) patentable: _____.
      (5) Newly presented canceled claims: _____.
      (6) Patent claim(s) ☑ previously ☐ currently disclaimed: 32,34,40 and 43-44
      (7) Patent claim(s) not subject to reexamination: See Continuation Sheet.
3. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
4. ☑ Note the attached statement of reasons for patentability and/or confirmation. Any comments considered necessary by patent owner regarding reasons for patentability and/or confirmation must be submitted promptly to avoid processing delays. Such submission(s) should be labeled: "Comments On Statement of Reasons for Patentability and/or Confirmation."
5. ☐ Note attached NOTICE OF REFERENCES CITED (PTO-892).
6. ☐ Note attached LIST OF REFERENCES CITED (PTO/SB/08 or PTO/SB/08 substitute).
7. ☐ The drawing correction request filed on _____ is: ☐approved ☐disapproved.
8. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐None of the certified copies have
   ☐been received.
   ☐not been received.
   ☐been filed in Application No. _____.
   ☐been filed in reexamination Control No. _____.
   ☐been received by the International Bureau in PCT Application No. _____.

   * Certified copies not received: _____.
9. ☐ Note attached Examiner's Amendment.
10. ☐ Note attached Interview Summary (PTO-474).
11. ☐ Other: _____.

All correspondence relating to this reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this Office action.

/YUZHEN GE/ Primary Examiner, Art Unit 3992	/Drew Fischer/ /Stephen Stein/ SPE, Art Unit 3992 MQAS, CRU

cc: Requester (if third party requester)

Continuation of 2. (c) Status of the Claim(s)- (7) Patent claim(s) not subject to reexamination: 3,6-9,11-12,14-19,23-31,33,35-37,39,41-42,45-46,48-53,55-56,60,63-65,67-69 and 71-75

REEXAMINATION OF U.S. PATENT 8,023,580

Notice of Intent to Issue a Reexam Certificate (NIRC)

This NIRC addresses the *ex parte* reexamination of U.S. Patent No. 8,023,580 ("the `580 Patent).

I. PATENTABLE/CONFIRMED SUBJECT MATTER

Claims 2 and 59 are confirmed. Below is the reason for the confirmation:

As acknowledged by the Patent Owner, the `580 Patent expires on Dec. 5, 2018. As a result, the broadest reasonable interpretation of claim terms is no longer proper for the claims in this reexamination proceeding. The claim limitations, including the "at least two types of modulation methods" or "different types of modulation method," should be interpreted under Phillips v. AWH Corp., 415 F.3d 1303, 1316, 75 USPQ2d 1321, 1329 (Fed. Cir. 2005).

Federal Circuit, in Rembrandt Wireless Technologies v. Samsung Electronics Co., 853 F.3d 1370, 1375-77 (Fed. Cir. 2017), applied a Phillips claim construction and determined that the limitation "modulation method of a different type" in claims 2 and 59 required at least two "different families of modulation techniques, such as the FSK family of modulation methods and the QAM family of modulation methods." Id. at 1377.

Because the prior art on the record does not teach different types of modulation methods as different families of modulation techniques such as the FSK family of modulation methods and the QAM family of modulation methods, claims 2 and 59 are confirmed.

II. CONCLUSION

Patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a), to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving the '285 patent throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286. The third party requester is similarly apprised of the ability to disclose such proceedings.

All correspondence relating to this ex parte reexamination proceeding should be directed as follows:

By **U.S. Postal Service Mail** to:

Mail Stop Ex Parte Reexam
ATTN: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to:

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Central Reexamination Unit

By hand to:

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Alexandria, VA 22314

Registered users of EFS-Web may alternatively submit correspondence via the electronic filing system at https://efs.uspto.gov/efile/nwportal/efs-registered

Any inquiry concerning this communication or as to the status of this proceeding, should be directed to Yuzhen Ge at telephone number (571) 272-7636.

/YUZHEN GE/
Primary Examiner, Art Unit 3992
Central Reexamination Unit

Conferees:

/Drew Fischer/
Patent Reexamination Specialist, Art Unit 3992
Central Reexamination Unit

/Stephen Stein/
Managing Quality Assurance Specialist
Central Reexamination Unit

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/013,808	8023580
	Examiner	**Art Unit**
	YUZHEN GE	3992

CPC						
Symbol					**Type**	**Version**
H04L	/	5	/	1453	F	2013-01-01
H04L	/	27	/	0008	I	2013-01-01
H04L	/	25	/	0262	I	2013-01-01
H04L	/	1	/	206	I	2013-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	2	
/YUZHEN GE/ Primary Examiner, Art Unit 3992	19 December 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

U.S. Patent and Trademark Office — Part of Paper No.: 20181219

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/013,808	8023580
	Examiner	Art Unit
	YUZHEN GE	3992

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H04L	/	5	/	12

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
375	261

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
455	102					
332	108	119	151			

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	2	
/YUZHEN GE/ Primary Examiner, Art Unit 3992	19 December 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

U.S. Patent and Trademark Office

Part of Paper No.: 20181219

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/013,808	8023580
	Examiner	Art Unit
	YUZHEN GE	3992

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
2	2														
59	59														

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	2	
/YUZHEN GE/ Primary Examiner, Art Unit 3992	19 December 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

U.S. Patent and Trademark Office Part of Paper No.: 20181219

Reexamination	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/013,808	8023580
	Certificate Date	Certificate Number
		C1

Requester Correspondence Address: ☐ Patent Owner ☑ Third Party
ROPES & GRAY LLP IPRM DOCKETING - FLOOR 43 PRUDENTIAL TOWER 800 BOYLSTON STREET BOSTON, MA 02199-3600

LITIGATION REVIEW ☑	/YG/ (examiner initials)	19 December 2018 (date)
Case Name		Director Initials
Rembrandt Wireless Techs., LP v. SamsungElecs. Co., C.A. No. 2:13-cv-00213-JRG (E D. Tex.), closed.		SJS for JC
Rembrandt Wireless Techs., LP v. Samsung Elecs. Co., C.A. No. 2:16-cv-00170-JRG (E.D. Tex.), closed		
Rembrandt Wireless Techs., LP v. Samsung Elecs. Co., No. 2016-1729 (Fed. Cir), closed.		

COPENDING OFFICE PROCEEDINGS	
TYPE OF PROCEEDING	NUMBER
None	

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BIB DATA SHEET

CONFIRMATION NO. 2211

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
90/013,808	09/12/2016 RULE	375	3992	3277-0114US-RXM1

APPLICANTS

INVENTORS

8023580, Residence Not Provided;
REMBRANDT WIRELESS TECHNOLOGIES, LP, ARLINGTON, VA;
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SAMSUNG ELECTRONICS AMERICA, INC. (3RD PTY REQ.), RIDGEFIELD PARK, NJ;
ROPES & GRAY LLP PRUDENTIAL TOWER, BOSTON, MA

**** CONTINUING DATA ***************************

This application is a REX of 12/543,910 08/19/2009 PAT 8023580
which is a CON of 11/774,803 07/09/2007 PAT 7675965
which is a CON of 10/412,878 04/14/2003 PAT 7248626
which is a CIP of 09/205,205 12/04/1998 PAT 6614838
which claims benefit of 60/067,562 12/05/1997

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☐ No Verified and Acknowledged /YUZHEN GE/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
				79	7

ADDRESS

ROTHWELL, FIGG, ERNST & MANBECK, P.C.
607 14th Street, N.W.
SUITE 800
WASHINGTON, DC 20005
UNITED STATES

TITLE

SYSTEM AND METHOD OF COMMUNICATION USING AT LEAST TWO MODULATION METHODS

FILING FEE RECEIVED		
12000	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

US008023580C1

(12) EX PARTE REEXAMINATION CERTIFICATE (11446th)

United States Patent

Bremer

(10) Number: US 8,023,580 C1

(45) Certificate Issued: Jan. 15, 2019

(54) **SYSTEM AND METHOD OF COMMUNICATION USING AT LEAST TWO MODULATION METHODS**

(75) Inventor: **Gordon F. Bremer**, Clearwater, FL (US)

(73) Assignee: **REMBRANDT WIRELESS TECHNOLOGIES, LP**, Arlington, VA (US)

Reexamination Request:
No. 90/013,808, Sep. 12, 2016

Reexamination Certificate for:

Patent No.:	**8,023,580**
Issued:	**Sep. 20, 2011**
Appl. No.:	**12/543,910**
Filed:	**Aug. 19, 2009**

Related U.S. Application Data

(63) Continuation of application No. 11/774,803, filed on Jul. 9, 2007, now Pat. No. 7,675,965, which is a continuation of application No. 10/412,878, filed on Apr. 14, 2003, now Pat. No. 7,248,626, which is a continuation-in-part of application No. 09/205,205, filed on Dec. 4, 1998, now Pat. No. 6,614,838.

(60) Provisional application No. 60/067,562, filed on Dec. 5, 1997.

(51) **Int. Cl.**

H04L 5/12	(2006.01)
H04L 5/14	(2006.01)
H04L 27/00	(2006.01)
H04L 25/02	(2006.01)
H04L 1/20	(2006.01)

(52) **U.S. Cl.**
CPC ***H04L 5/1453*** (2013.01); ***H04L 1/206*** (2013.01); ***H04L 25/0262*** (2013.01); ***H04L 27/0008*** (2013.01)

(58) **Field of Classification Search**
None
See application file for complete search history.

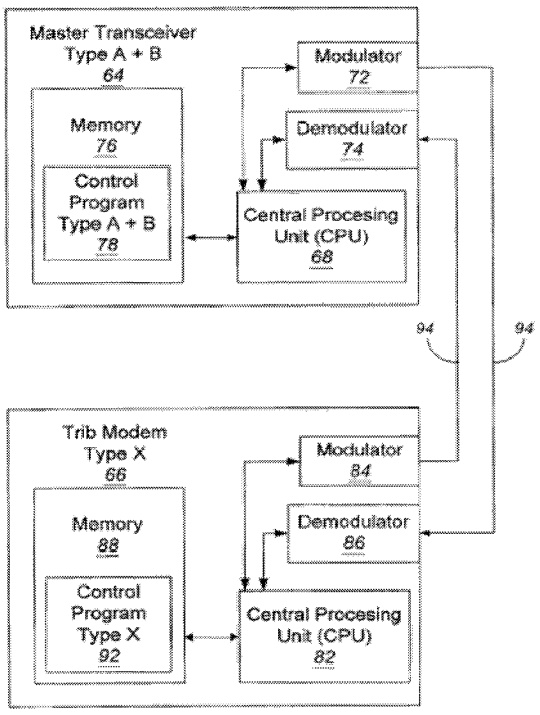
(56) **References Cited**

To view the complete listing of prior art documents cited during the proceeding for Reexamination Control Number 90/013,808, please refer to the USPTO's public Patent Application Information Retrieval (PAIR) system under the Display References tab.

Primary Examiner — Yuzhen Ge

(57) **ABSTRACT**

A device may be capable of communicating using at least two type types of modulation methods. The device may include a transceiver capable of acting as a master according to a master/slave relationship in which communication from a slave to a master occurs in response to communication from the master to the slave. The master transceiver may send transmissions discrete transmissions structured with a first portion and a payload portion. Information in the first portion may be modulated according to a first modulation method and indicate an impending change to a second modulation method, which is used for transmitting the payload portion. The discrete transmissions may be addressed for an intended destination of the payload portion.



EX PARTE REEXAMINATION CERTIFICATE

NO AMENDMENTS HAVE BEEN MADE TO THE PATENT

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims **2** and **59** is confirmed.

Claims **1**, **4-5**, **10**, **13**, **20-22**, **38**, **47**, **54**, **57**, **58**, **61-62**, **66**, **70** and **76-79** were previously cancelled.

Claims **24**, **26-28**, **31-37**, **39**, **40**, **42-46** and **48** were previously disclaimed.

Claims **3**, **6-9**, **11-12**, **14-19**, **23**, **25**, **29-30**, **41**, **49-53**, **55-56**, **60**, **63-65**, **67-69** and **71-75** were not reexamined.

* * * * *