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Data Communications, Computer Networks and Open Systems

Fourth Edition

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synchronous, character-oriented/bit-oriented, parity/CRC, etc. – by writing defined bit patterns into selected internal registers. We also referred to these circuits as **universal communication interface circuits**. Normally, a single circuit provides one, two or even four separate (full-duplex) transmission line interface circuits.

The device controlling the operation of the circuit – a microprocessor, for example – first programs the desired operating mode by writing a defined byte (bit pattern) into the **mode register**. The device is then made ready to transmit and/or receive characters/bytes by writing a second byte into a **command register**. The transmit and receive channels are always **double-buffered** which means that the controlling device has a full character (or byte) time to process each character (byte) prior to transmission or after reception, rather than a single bit time.

The names and functions of the most common devices are as follows:

- *Universal asynchronous receiver transmitter (UART)*
  - Start and stop bit insertion and deletion
  - Bit (clock) synchronization
  - Character synchronization
  - Parity bit generation and checking per character (BCC computed by controlling device)
- *Universal synchronous receiver transmitter (USRT)*
  - Low bit rate DPLL clock synchronization
  - Character synchronization
  - Synchronous idle character generation
  - Parity generation and checking per character (BCC computed by controlling device)
- *Universal synchronous/asynchronous receiver transmitter (USART)*
  - Can be programmed to operate as either a UART or a USRT
  - Has all the programmable features of both devices
- *Bit-oriented protocol circuits (BOPs)*
  - Opening and closing flag insertion and deletion
  - Zero bit insertion and deletion
  - CRC generation and checking
  - Idle pattern generation
- *Universal communications control circuits*
  - Can be programmed to operate either as a UART, a USRT, or a BOP
  - Has all the programmable features of each circuit

3.7 Communications control devices

In many data communication applications, a common requirement is to have a distributed community of terminals – personal computers, for example – that all require to access a central computing facility. This facility could operate a central

Figure 3.29 Simple terminal networks: (a) locally distributed; (b) remotely distributed.

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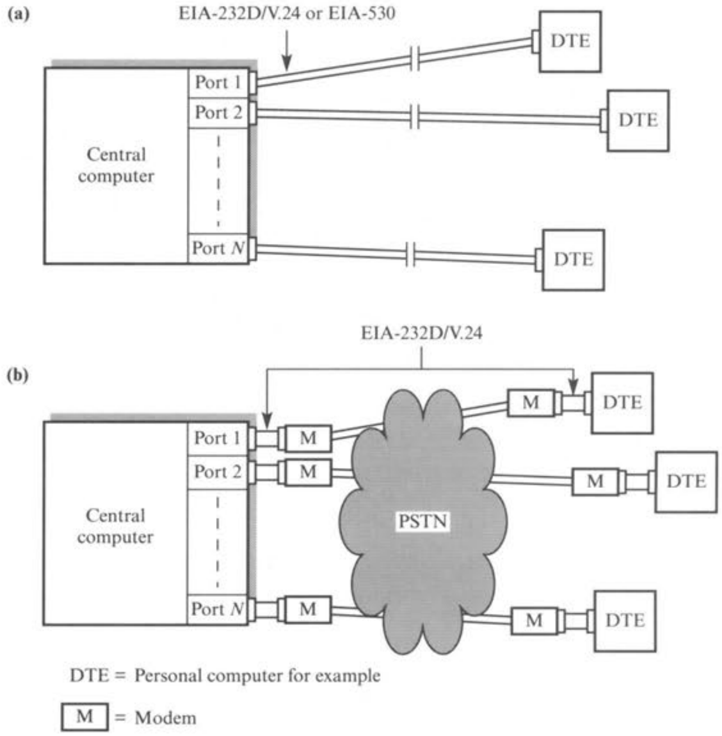

Figure 3.29 Simple terminal networks: (a) locally distributed; (b) remotely distributed.

electronic mail service for an enterprise, or house a central database to which the distributed community of terminals requires access.

If all the terminals are situated in different locations, the only solution is to provide a separate communications line for each terminal, as shown in Figure 3.29. In part (a) we assume that the terminals are distributed around a single establishment, whereas in part (b) we assume that they are each located in different establishments. In the latter case, it is likely that modems will be required operating over switched connections or leased lines, depending on the amount of data to be transferred and the frequency of calls. In the case of switched connections, the terminals will normally have autodial facilities associated with the communications interface.

For applications in which a number of terminals are located together, we can use a device known as a **multiplexer (MUX)** to minimize the number of transmission lines required. Such devices are used with a single transmission line that operates at a higher bit rate than the individual user terminal rates. As Figure 3.30 shows, we normally use a similar multiplexer at each end of the link. In this way the presence of the multiplexers is transparent to both the terminals and the central computer.

There are two types of multiplexer: **time-division multiplexers** and **statistical multiplexers**. A time-division multiplexer assigns each terminal a dedicated

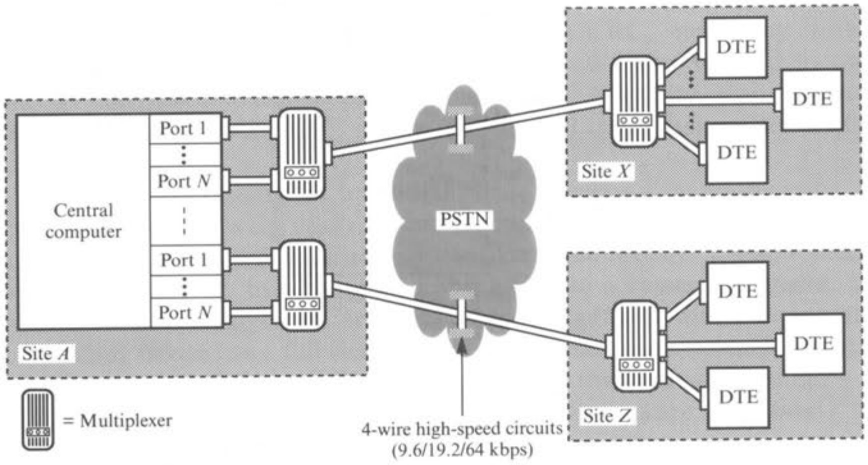

Figure 3.30 Multiplexer-based network schematic.

portion of the transmission capacity of the shared line. A statistical multiplexer allocates transmission capacity on an on-demand or statistical basis.

3.7.1 Time-division multiplexer

A typical time-division multiplexer application is shown in Figure 3.31(a). The terminals located in each establishment associated with an enterprise all require access to the central computer. We assume that each site has a large number of terminals that generate sufficient intersite traffic to justify high bit rate leased circuits being used to link the various sites to the central site. Typically, these are 64 kbps or higher, depending on the number of terminals.

Figure 3.31(b) shows the internal architecture of each MUX. Typically, each terminal operates in an asynchronous transmission mode and is connected to a UART. The controlling microprocessor within the MUX controls the transfer of characters between the UARTs and the high-speed link interface circuit. As the latter normally operates in a character-oriented synchronous transmission mode it will comprise a USRT.

To ensure that the presence of the MUXs is transparent to the terminals/computer, the transmission capacity associated with the high bit rate circuit is divided in such a way that the UARTs in the terminal and computer ports can operate at their programmed rate. This is achieved by a technique known as **rate adaption** which involves breaking the available link capacity into a number of frames as shown in Figure 3.31(c).

Each frame comprises *N* bytes such that the bit rate associated with a single byte position in each frame forms a suitable basic multiplexing rate. The bit rates associated with each terminal are then derived by using multiple bytes per frame. However, not all the bits in each byte are used for user data. The first bit in each byte is used for framing; a fixed repetitive bit pattern is sent in this bit position of

Figure 3.31 Time-division multiplexer principles: (a) application; (b) MUX schematic; (c) rate adaption.

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