and the rate of transmission. Thus, a different filter must be provided for each type or modulator implemented. Similar digital techniques may be used for both multifrequency (MF) and differential phase shift keyed (DPSK) modulation.

A modulation technique similar to that illustrated in Fig. 1 is utilized in the time shared multiline FSK modulator disclosed in U.S. Patent 3,697,892 to Lawrence et al which provides a specific type of FSK modulation for a set of lines. The multiline time-shared modulator, however, requires separate digital to analog converters for each line and a band pass filter for each line capable of eliminating undesired out of band frequency components generated in the modulation process. Because of these requirements, the multiline modulator is incapable of handling a wide variety of modulation techniques which may be used for any of the output lines. This is so because of the specific requirements for the individual output line band pass filters. In the patented device, each output line must, of necessity, be limited to one type of modulation. If it is desired to change the modulation characteristics for a given line, it becomes necessary to alter the characteristics of the connected band pass filter. This requirement severely limits the usefulness of the multiline modulator since the lines cannot be dynamically allocated to different modulation techniques.

Description of the Preferred Embodiment

Fig. 1 described in detail above illustrates the application of digital tone synthesis techniques in an FSK modulator. A digital value of phase $\theta(t)$ is accumulated and updated each processing cycle determined by fs where fs is the sampling rate of the resulting modulated digital line signal. The amount by which the phase is incremented each sample time, $\Delta\theta$, determines the slope of $\theta(t)$ and hence the instantaneous frequency of the sine wave generated. For binary FSK, one of two values of phase increment $\Delta\theta 0$ and $\Delta\theta 1$ are selected depending on the data which is to be transmitted. The frequency of the sine wave being generated is directly proportional to the value of $\Delta\theta$. $\Delta\theta$ and $\theta(t)$ are both digital signals and the accumulation is performed with conventional arithmetic components. The digital phase signal is scaled such that arithmetic overflow of the accumulator or buffer 18 corresponds to the normal modulo 360° property of the trignometric sine function.

The digital representation of phase θt is translated to a digital representation of sin $\theta(t)$ by means of the read only memory 19. The resulting digital amplitude signal is converted to analog by conventional digital to analog conversion techniques and subsequent analog filtering. The quantizing noise resulting from the conversion from digital to analog is removed by the analog filtering along with other unwanted frequency components introduced by the modulating technique.

In the FSK modulator illustrated in Fig. 1, as well

as in other conventional FSK modulators implemented with either analog or digital circuits, the instantaneous frequency of the transmitted signal is abruptly switched between two values in the course of being modulated by the input data signal. The abrupt transition in frequency causes an increase in the bandwidth of the transmitted signal over that actually required to communicate the data by the FM modulation process. When FSK data transmission over telephone channels is required, it is necessary to reduce the excessive bandwidth generated in two significant application areas. One in high speed FSK, 1200 to 1800 bits per second transmission, bandwidth reduction is necessary to comply with out of band signal regulations imposed by various regulatory agencies and two in full duplex transmission using a single physical channel, the received signal can, in many instances, be significantly smaller in amplitude than the local transmitted signal and the two frequency bands occupied by the two signals may be relatively close. This requires that the bandwidth of the transmitted signal be sharply reduced in order to prevent interference with the received signal.

Classically, FSK bandwidth reduction has been attained through band pass filtering of the transmitted signal. Some modulators have used premodulation filtering of the data signal; however, this approach has had limited application since it requires a linear FM modulator. Either of the above approaches for reducing unwanted signals introduced in the modulation process has a drawback in a digital implementation of the modulator since the arithmetic requirements of a digital filter greatly increase the functional complexity of the unit. For this reason, some digital modulators have used rather complex analog filters in their implementation.

A significant reduction in bandwidth can be achieved by eliminating the abrupt frequency transitions normally present in FSK modulation of binary data. This can be done by having the instantaneous frequency make a smooth or continuous transition in changing from one value to another. This is pointed out by Bettinger in "Digital Transmission for Mobile Radio", Electrical Communications, Vol. 47, No. 4, 1972 at page 225. Such an approach has been implemented by the use of a premodulation filter, as noted earlier, or by the application of a control signal or voltage to a linear modulator. This approach while producing a desirable result is not flexible in many uses and limits the utility of the modulator to a single baud rate and set of frequencies.

In a digital FSK modulator constructed according to the invention, a smooth transition in frequency is accomplished by storing in memory digital values which represent a predetermined trajectory for the instantaneous frequency to follow and selecting these values based on the interbaud time or time since the last data transition. Such an approach is viable only in a digital FSK modulator where the phase and rate of phase change can be accurately specified. The trajectory followed as the frequency is slewed from one value to another is selected to minimize the bandwidth of the modulated signal. Both the shape and the number of intermediate points in the trajectory, per bit time, are important parameters in this regard. Analysis and experiment has shown that a sinusoidal trajectory with eight points specified in time over the data bit give the best performance in terms of minimum transmit signal

bandwidth and minimum loss in receiver detectability. This does not, however, imply that an eight point sine wave trajectory is optimum in general. When this technique is implemented as shown in the modulator illustrated in Fig. 2, out of band signaling is reduced to the point where output filtering is no longer required and the sole filtering requirement is that necessitated by the digital modulation technique employed, that is, the removal of the quantizing noise. This may be accomplished by a simple RC filter.

The modulator illustrated in Fig. 2 is capable of providing the FSK modulation for a single line of a number of different types or frequencies of FSK modulation. It requires binary input data and a line control word signal which in the illustrated embodiment is a single line designating either one type of FSK modulator or another. If the one type is designated, the line will be at a voltage level indicating the binary 0 and if the other type is indicated, the line voltage will be at a voltage indicating a binary 1. This, of course, could be expanded by providing additional lines for designating the line control word. In addition, the clock generator 30 operating at a frequency fs provides two clock phase signals C1 and C2. These are illustrated graphically in the figure and are 180° out of phase with each other. The data signals, the line control word and the two clock signals are applied to an address generator 31. The address generator 31 also receives signals from three conductors 32A, 32B and 32C. These 3 conductors represent the three high order bits from a buffer register 32, the function of which will be described later on. Based on the inputs described above, address generator 31 logically derives an address which is

applied to a read only memory 33 to access during one-half of the clock cycle fs, a value $\Delta\tau$ and during the other half of the clock period fs, the value $\Delta\theta\tau$.

The contents of memory 33 are set out in the table of Fig. 3. This table is divided into two sections. It shows memory address i - i+9 which are associated with line control word 0 for one type of FSK modulator and memory addresses j - j+9 which are associated with line control word 1, another type of FSK modulator. Obviously, if additional types of FSK modulators are to be implemented, additional sections of memory would be necessary as well as additional lines for the line control word to distinguish the various FSK modulators being implemented. The conditions of the selection signals are indicated in the righthand columns of the table underneath the headings "Line Control Word, Data, τ, c1 and c2. During the first half of the clock cycle fs, that is, when c1 and c2 are 1, 0 respectively, the contents of addresses i and i+1 or j and j+1 depending on the line control word, will be selected if the three high order bits from buffer 32 are all zeroes or all ones and the data bit is 0 or 1, respectively, the contents from address i+1 or j+1, namely, all zeroes will be provided at the output of the read only memory during that particular fs clock cycle. If the contents of the three high order bits and the data bits are any other value, the contents of address i or j depending on the line control word will be selected. In this case, this value is an increment dividing the bit period τ into eight different values to provide as shown in Fig. 2A, eight different values of $\Delta\theta$ over a single bit period for causing the frequency of the output of the modulator to change values smoothly or

sinusoidally as discussed above. For example, if the sampling frequency fs of 18,000 cycles per second is selected, this would yield 30 samples per bit for a 600 bit per second line. Thus, a value of 120 for t/8 will provide eight substantially equal steps if the three high order bits of a 12 bit position register are examined. Therefore, the numerical value 120 will be stored in binary form in memory address i to implement a FSK modulation for a 600 bit per second data rate. During the first half of each cycle fs, this value under the conditions described above, that is, data not zero and the three high order bits from buffer 32 not all zero or data not one and the three high order bits from buffer 32 not all ones, will be added or subtracted to modify the contents of register 36. How this is accomplished will become apparent as the description of the circuit shown in Fig. 2 continues.

During the second half cycle of clock fs, that is, C1(0) and C2(1), the values Δθ1 through Δθ8 residing in address locations i+2 through i+9 will be added in a manner similar to that illustrated in Fig. 1 and described below to thus generate the actual output frequencies from the modulator. The form of the values Δθ1 through Δθ8 is illustrated in the graph shown in Fig. 2A. These values are selected to provide a smooth transition from the one frequency to the other.

The contents, under the conditions described above, from read only memory 33 are applied to one input of an adder circuit 34. The output of the adder circuit is selectively applied under control of clock 30 and a read write memory control circuit 35 to one of two registers 36 and 37. During the first half

of the clock period fs, the output of adder circuit 34 is inserted in register 36 under control of read write memory control circuit 35 and during the second half of the clock fs, the output of adder circuit 34 is inserted in register 37. Likewise, the contents of register 36 are added in adder 34 during the first half of the clock cycle from clock 30 with the output of read only memory 33 and during the second half cycle of clock 30, the contents of register 37 are added in adder 34 with the output from read only memory 33. The addition and readback occur under control of read write memory control circuit 35 at different portions of the output from clock circuit 30. Thus, during the first portion of each of the clock cycles, the contents of the registers 36 and 37 are added to the output of memory 33 by adder 34. After the addition takes place the sum of this addition is inserted into the registers 36 and 37. Read write memory control circuit 35 may take many forms as is well known in the prior art for controlling reading into and out of memory devices and is not shown in greater detail here since it is well known in the prior art. The contents of register 36 under control of the clock 30 C1 output are transferred to buffer 32 and the three high order bits of this register which may, for example, contain 12 bit positions are applied via conductors 32A, 32B and 32C to the address generator 31 and are used as described above for generating the address within read only memory 33 of the data which must be applied during each clock cycle to adder 34.

An adder control circuit 38 responds to the output of clock 30 and the data input to control the function of adder 34; that is, whether an addition or subtraction takes place. During the first half of the clock period of clock 30, an

addition or subtraction will take place depending upon the direction of change of the data. If the data changes from a 1 value to a 0 value, the contents of register 36 must be decremented and if the data changes from a 0 to a 1, the contents of register 36 must be incremented. Adder control 38 includes an AND circuit 39 having one input connected to the data line and another input connected to the C1 output of the clock 30. The output of AND circuit 39 is connected via an OR circuit 40 to a control input of adder 34. When the data is 1 and during the first half of the clock period of clock 30, AND circuit 39 provides an output via OR circuit 40 which causes the adder to increment or add. When the data is zero, the output of AND gate 39 is down and this signal level causes adder circuit 34 to decrement. The specific implementation of this control is well known in the art and is not further described here. During the second half of clock 30, the C2 output is connected via OR circuit 40 to the control input of adder 34 and causes the adder to increment during this second half of the clock period. Buffer 32 is loaded under control of the C1 output of clock 30, thus, after the contents of register 36 have been modified as described above, the new value calculated is loaded into buffer 32 where it will be available for the next cycle of clock 30 during the next sampling period.

The output of adder 34 is applied to a θ to sine θ conversion circuit 41 which may be a read only memory loaded with precomputed values of sine θ to perform the conversion. Such devices are well known in the prior art and readily available and are illustrated throughout this specification in block form only. The output of θ to sine θ converter 41 is applied to a register 42. Register 42 is strobed under

control of the C2 clock from clock generator circuit 30 and the contents applied at that time to a conventional digital to analog converter 43. The output of digital to analog converter 43 pulses a simple RC filter 44 which is designed solely to remove the quantizing noise introduced by modulation process. It is obvious from the above description that the modulator may be changed from any group of frequencies to some other group of frequencies simply by changing the line control word and storing the appropriate values for that group in the read only memory 33 since the filter 44 is the same for all values, it need not be changed or switchable.

The basic processing time in Fig. 2 is divided into two parts, C1 and C2. During C1 time, a running accumulation of bit time is calculated. During C2 time, a phase accumulation is calculated as is done in the conventional digital modulator illustrated in Fig. 1, with the exception that the values of $\Delta\theta$ are selected from memory on the basis of the bit time τ from register 32. If a data transition occurs, during C1 time, numerical value which at the sampling rate will provide eight substantially equal detectably different outputs from register 32 is selected from the $\Delta\tau$ memory and added or subtracted depending on the data input. The baud time accumulation is made sharing the same adder 34 as is used for the phase accumulation. The digital value of baud time is prevented from underrunning, that is, going below the all zero state when $\Delta\tau$ is subtracted or overrunning, that is, going above the all one state when $\Delta\tau$ is added. This is accomplished by the all zero condition stored in memory location i+1 or j+1 since adding or subtracting all zeroes to any number does not change it. This memory

address is selected on the basis of the conditions shown in the table of Fig. 3, namely, data 1 and τ all one or data 0 and τ all zero. In both of these conditions, an under or over run could occur. Therefore, the zero value is added to the value of τ contained in register 36 during each processing cycle. With this control, the baud time value changes from an all zero state to an all one state in eight equal steps spanning the complete bit time when the data changes from a 0 to a 1. Thereafter, the baud time remains at the all one state until the data changes back to zero. At which time, $\Delta\tau$ is subtracted and τ is permitted to increment to the all zero state.

At the end of C1 time, the highest three bits of τ are transferred to register 32 and used to address the $\Delta\theta$ memory during C2 time. The three highest bits of τ select one of the 8 values of $\Delta\theta$ to be accumulated as τ traverses from one data state to the other. As indicated in Fig. 2A, the values of $\Delta\theta$ addressed by τ produce a smooth or sinusoidal trajectory in the instantaneous frequency of the transmitted signal. The phase accumulation, phase to sine conversion, and digital to analog conversion are performed in the same manner as for the conventional modulator illustrated in Fig. 1.

Fig. 4 is a schematic diagram of a differential phase shift keyed modulator compatible in implementation with the FSK modulator described above with respect to Fig. 2. The implementation in Fig. 4 provides a narrow band modulation in which the generated transmit signal spectra are sufficiently narrow as not to require subsequent filtering for transmission over telephone lines or similar transmission media. The

only requirement being a simple RC filter to remove the quantizing noise associated with the digital generation of the signals and conversion to analog form.

The implementation of the DPSK modulator illustrated in Fig. 4 is structurally similar to the FSK modulator illustrated in Fig. 2. Since the two modulation techniques are compatible with each other, the major differences are in the nature of the signals stored in the read only memory. In view of this similarity, the reference numerals used in Fig. 2 will be used in part in connection with the description of this figure. In the DPSK modulator, the clock 30-1 operating at a sampling frequency fs provides five outputs during each sampling time. These outputs are illustrated graphically in the figure. The first output C1 occurs during the first quarter of the period of clock 30. The second output C2 occurs during the second quarter, the third output C3 occurs during the third quarter and the fourth and fifth outputs occur during the fourth quarter. The fourth output C4 occupying the first half of the fourth quarter and the fifth output, C5, occupying the last half of the fourth quarter. The clock outputs C1-C5 are applied to the address generator 31-1 along with the three high order bits from the τ buffer 32-1. The line control word and one of the two simultaneously provided data bits for a four phase DPSK modulation. The modulation contemplated in this modulator is a conventional four-phase DPSK modulation in which two bits of a binary digital signal are simultaneously encoded. The first bit D0 defining the sign of the differential phase change and the second bit D1 defining the magnitude of the change. In this modulator, the magnitude bit is applied to address generator 31 for selecting along with the other inputs

the appropriate address within the memory 33-1.

The output of address generator 31-1 selects an address during each of the five processing cycles of clock period 30-1 and reads the data stored in that address from the read only memory 33-1. This data is applied to one input of an adder 34-1. Two feedback register 36-1 and 37-1 similar to the registers 36 and 37 of Fig. 2 are connected from the output of the adder 34-1 to the other input of the adder 34-1 and selectively entered therein by the clock signals from clock generator 30-1 which are applied to a read write control circuit 35-1. The contents of register 36-1 are applied to adder 34-1 during clock time C1 and added to the contents supplied from read only memory 33-1 then reinserted into register 36-1. At the end of this clock period, the contents of register 36-1 are also inserted into buffer 32-1 and are used as previously described for generating the address in address generator 31-1 along with the other inputs applied thereto. How these particular inputs access specific data in the memory will be described later in connection with the description of Fig. 5 which includes a table of the memory and the selection signals.

During the second clock period, C2, the contents of register 37-1 are added to the data supplied from read only memory 33-1 and then reinserted in the register 37-1. This step is repeated during the third clock period C3. During clock period C3, the adder 34-1 will either add or subtract depending upon the sign of the D0 data bit applied to the adder control circuit 38-1. If the sign bit is negative, adder control circuit 38-1 will provide an appropriate signal to adder 34-1 causing a subtraction to take place. If the sign bit is positive, an addition will take place. The

arrangement of adder control circuit 38-1 will be described below.

During the fourth clock period C4, the contents of register 37-1 are added to the signal supplied by the read only memory 33-1, passed through θ to sin θ conversion read only memory 41-1 and inserted in a buffer 45 which is under control of a read-write and clear control circuit 46. Circuit 46 responds to clock pulses C4, C5 and C1. During clock pulse C4 the output from θ to sin θ conversion circuit 41-1 is inserted into buffer 45. The contents of register 37-1 are not altered at this time. That is, the summation during the fourth clock period C4 does not alter the contents of buffer 37-1. This is effected by read/write control circuit 35-1 in response to the C4 clock pulse. During the fifth clock pulse C5, the signals supplied from read only memory 33-1 are subtracted from the contents of register 37-1 under control of circuit 38-1. The output of adder 34-1 is passed through θ to sin θ conversion circuit 41-1 and applied to one input of an adder 47. The other input of adder 47 is connected to buffer 45 which during clock time C5 is read into the other input of adder 47 under control of read/write and clear circuit 46. The output of adder 47 is inserted in register 42-1 which at the trailing edge of clock time C5 is applied to a digital to analog converter 43-1 which has its output connected to filter 44-1.

Adder control circuit 38-1 is provided with an OR gate 48 having two inputs connected to the C1 and C2 outputs of clock generator 30-1. The output of OR gate 48 is connected to one input of another OR gate 49 which has its output connected to the control input of adder 34-1. When this output is in a 1 state, that is when either clock pulse C1 or C2 are present, adder 34-1 will add the contents applied at its two inputs.

When the output of OR circuit 49 is 0, the contents applied to the two inputs will be subtracted. An AND gate 50 has one input connected to the D0 data bit line said a second input connected to the C3 clock output of clock generator 30-1. When the data bit D0 is 1, during clock period C3, AND gate 50 provides an output which is applied via OR circuit 49 to cause adder 34-1 to assume the adding mode, if the data bit is 0 indicating the negative sign, the adder will be controlled to perform a subtraction. A third input to OR circuit 49 is connected to the C4 output of clock generator 30-1 and causes an addition to occur during the C4 clock time. Summarizing adder 34-1 under control of adder control circuit 38-1 performs an addition during C1, C2, and C4 times regardless of the circumstances. During C3 time it performs an addition, when the D0 bit is positive and a subtraction when the D0 bit is negative. During C5 time, a subtraction is always performed.

The modulator of Fig. 4 is specifically configured to perform the function of a four-phase modulator such as the IBM* 3872 and the Bell* 201 modems and is based on encoding two bits of data per baud by the differential phase between bauds as indicated in the table below.

D0	D1	Phase Differential
1	1	+45
1	0	+135
0	1	-45
0	0	-135

As with the FSK modulation previously described, abrupt transitions in phase between bauds in DPSK modulation produce modulated output signals containing excessive out of band frequencies. A significant reduction in the bandwidth of the output signal can be achieved by

*Trade Marks

having the $\Delta\theta$ increments between the bauds vary in a smooth manner. Additional reductions in bandwidth can be obtained by combining amplitude modulation with the phase modulation. The above attributes are obtained through a widely used approach which employs a modulated signal consisting of using two phase modulated carriers, each with envelope modulation. Abrupt phase changes are made when the envelope of the particular carrier is zero. The equivalent modulated signal has a smooth phase transition and can be written with the following form.

$$L(t) = E(\tau) \cos [wct + \theta m + \phi(\tau)]$$

where Wc = carrier frequency

θm = arbitrary phase angle (not significant since the modulation is on a differential phase)

$E(\tau)$ = envelope or amplitude function

and $\phi(\tau)$ = Phasing function which describes the phase change between bauds.

The direct but straightforward approach to implementing the above line signal requires a digital multiplier to accomplish the amplitude modulation. Such an approach would significantly increase the complexity of the transmitter. Multiplication is avoided by taking advantage of the ability to accurately control phase angle within the transmitter signal flow. The technique used is described below. Let

$$L(t) = E(\tau) \cos [\theta(t)]$$

where $\theta(t) = Wct + \theta m + \phi(\tau)$

and assume $E(\tau)$ is scaled to a maximum level of 1.

then $E(\tau) \cos \theta(t) = 1/2 \{\cos [\theta(t)+\cos^{-1}E(\tau)]+\cos[\theta(t)-\cos^{-1}E(\tau)]\}$

or $L(t) = \cos [\theta(t) + \theta 0(\tau)] + \cos [\theta(t) - \theta 0(\tau)]$

where $\theta 0(\tau)$ is an offset angle equal to $\cos^{-1}[1/2\ E(\tau)]$

Amplitude modulation is accomplished by generating two phase modulated sinusoids properly displaced in phase by $2\theta 0(\tau)$ and transmitting their vector sum as described above in connection with the Fig. 4. The processing period as described for the line is segmented into five parts. During the first part, C1, a running accumulation of interbaud time τ is made. This is similar to the accumulation performed with respect to the FSK modulator described above. However, in the case of DPSK modulation, τ can be allowed to overflow since a phase change is made in each baud time. As in the case of FSK, the three most significant bits of τ are used. Thus, $E(\tau)$ and $\phi(\tau)$ are each defined by eight discrete values per baud. See the graphs in Figs. 4A, B and C.

During the second time periods, C2 of the processing cycle $\theta(t)$ is incremented by an amount $\Delta\theta c$ which corresponds to that part of the phase accumulation due to the carrier frequency Wct. During the third processing time period, C3, $\theta(t)$ is changed by an amount $\Delta\phi(\tau)$ which generates the smooth transition $\phi(\tau)$ in phase change over the baud time. Again, this may be seen from the graphs in Figs. 4A-C. $\Delta\phi(\tau)$ is determined by τ and the magnitude of the phase change to be made which is determined by the D1 data bit. The sign of $\Delta\phi(\tau)$ is determined by the D0 data bit which controls the sign of the adder via the adder control circuit 38-1. During the fourth and fifth processing times of each cycle, the offset angle $\theta 0(\tau)$ is selected from memory. The particular value selected is determined by the value of τ and the magnitude of the phase change by the data bit D1. The magnitude of $\theta 0(\tau)$ is independent of the sign of the change. During the fourth C4 time, the sum $\theta(t) + \theta 0(\tau)$ is calculated and converted to an amplitude value which is placed

in buffer 45. During the fifth time period, C5, $\theta(t) - \theta0(\tau)$ is calculated and converted to an amplitude value and added to the contents of buffer 45 in adder circuit 47, to thus produce the composite modulated signal at the end of C5 time. The output of adder 47 is inserted in the register 42-1 and gated to the digital to analog converter 43-1 at the appropriate time by the trailing edge of the C5 clock pulse from clock generator 30-1. the output of the digital analog converter 43-1 pulses filter 44-1 to provide the signal on the line. The filter, a simple RC filter, removes the quantizing noise introduced by the digital generation process.

The memory contents for read only memory 33-1 are illustrated in Fig. 5. A single bit line control word which may assume two states, 0 and 1. Two sets of values are stored. Each occupy 44 addresses in the memory. The first set i-i+33 are associated with modulation type LCW = 0. The selection process or logic required in the address generator 31-1 for each of the addresses and the data input supplied thereto are illustrated in the table alongside each of the address locations.

Address i includes a value T/8 which for the sampling frequency selected will when successively added to the contents in buffer 36-1, reduce the substantially equally spaced detectable outputs from buffer 32-1 which are applied to the address generator 31-1 during a single baud time. The contents of address i are obtained during the clock time C1 of each sampling cycle. The data content of the D1 bit and the values from the τ buffer 32-1 have no consequence. Thus, during each baud time register 36-1 counts up by the predetermined value T/8 which is selected based on the baud rate of the information and

the sampling frequency fs by 8 detectably different outputs in the three high order bits of the τ buffer 32-1 substantially equally spaced across the baud time. Address i+1 contains a value $\Delta\theta c$ which in the circuit disclosed in Fig. 4 produces the carrier frequency when incrementally added in the $\theta(t)$ register 37-1. This particular quantity is provided during the second or C2 clock time and the value again of τ and the value of the D1 bit are immaterial. The value selected for $\Delta\theta c$ is dependent upon the carrier frequency of the modulation.

The contents of memory addresses i+2 through i+9 contain the $\Delta\theta(\tau)$'s necessary to provide a smooth transition in eight successive steps where the phase is to be advanced or retarded by 135° as determined by D0 for the selected baud rate and carrier frequency defined by line control word zero. The particular value selected from these addresses is determined by the three high order bits from the τ buffer 32-1. These are illustrated in the table. One of these values is selected during the third clock time of each sampling period C-3, depending upon the value of the τ buffer 32-1. Addresses i+10 through i+17 contain similar values for $\Delta\theta(\tau)$ for a smooth transition of + or -45° and are selected on the same basis and during the same clocking period as addresses i+2 through i+9. These values are selected if the D1 bit is a 1 instead of a 0.

As previously stated, the values of $\theta 0(\tau)$ are the same during the fourth and fifth cycles, therefore a single set of values for $\theta 0(\tau)$ is provided in address i+18 through i+25 for a phase change of 135° and another set of values for $\theta 0(\tau)$ is provided in address i+26 through i+33 for a phase change of 45° depending upon the status of bit D1. One or the other of these groups of values for $\theta 0(\tau)$ is selected during the

C4 and C5 processing periods. The particular one selected from each of the groups is determined by the value of τ buffer 32-1. More specifically, the three high order bits contained in the buffer. During the C4 period the value read from memory 33-1 is added to the contents of register 37-1 and stored in buffer 45 after being converted in θ to sin θ conversion circuit 41-1, and during the C5 processing period, the value of $\theta 0(\tau)$ read from memory 33-1 is subtracted from the contents of register 37-1, converted in θ to sine θ conversion circuit 41-1 and at that time added to the contents previously stored in buffer 45 in the adder 47.

The memory includes another set of addresses j through j+33 for a second type of DPSK modulator identified by line control word one. These values are similar to the values described above in addresses i through i+33, however, the particular values stored will depend upon the carrier frequency and the baud rate for the modulator. If additional modulation frequencies and baud rates are to be implemented, additional blocks of memory addresses will be required and the line control word will have to be expanded to uniquely identify which is to be selected by the address generator 31-1. While the modulation process has been described in terms of 4-phase modulation, it is extendable to higher levels of phase modulation such as 8-phase by providing suitable functions for $\Delta\phi(\tau)$ and $\theta 0(\tau)$ as will be well understood by those skilled in the art.

In some instances such as where low baud rates are used or where less stringent out of baud signal reduction requirements are stipulated, the amplitude modulation described and illustrated may be eliminated. This may be accomplished by eliminating the

processing steps performed furing the c4 and c5 clock times. In this event, the circuit components following θ/sin θ conversion circuit 41-1 would be identical to those following the corresponding circuit 41 in Fig. 2.

In addition, the circuit illustrated in Fig. 4 and described above may be used to perform an amplitude modulation only. This may be accomplished by eliminating the processing step which occurs in the c3 clock time. This would eliminate the addition of the phase components $\Delta\phi(\tau)$. In this instance, no structural changes are required except for the elimination or suppression of the c3 clock time and processing steps which occur therein.

The modulator illustrated in Fig. 6 is specifically arranged to perform a multifrequency modulation similar to what is commonly known as touchtone signalling. In this form of signalling, pairs of selected frequencies are simultaneously transmitted to convey information. If four A and four B frequencies are available, and one A and one B frequency are simultaneously transmitted, sixteen different paired frequency combinations are available for transmitting data. These may typically transmit ten numeric digits and six control characters.

The modulator has the same general format as modulators previously described. Four parallel data bits are required to identify two tones, one of which is selected from a group of four and the other of which is selected from another group of four. These are indicated in the drawing as D0 through D3 and are applied directly to the address generator 31-2. A clock generator 30-2 provides a sampling frequency fs having two phases C1, C2. The C1 phase occupies the first half of the clock period and the C2 phase occupies the second

half of the period of clock 30-2. Both of these signals are applied to address generator 31-2 which based on the input signals generates an address for accessing phase information stored in a read only memory 33-2. Read only memory 33-2 includes two sets of values $\Delta\theta 1$ and $\Delta\theta 2$ which are the increments of phase and are similar to those described in the previous modulators. The value of $\Delta\theta$ selected thus determines the frequency of the tone which will be generated by the modulator.

The contents of read only memory 33-2 are illustrated in tabular form in Fig. 7. In address locations i through i+15, the selection signals include the line control word, data bits D0 through D3, and the two clock phases C1 and C2. The eight addresses i through i+7 are associated with one of A and B frequencies each including four different frequencies and the addresses i+8 through i+15 are associated with another set. These sets are identified by the line control word being zero or one. The data bits D0 and D1 define the A frequency which must be generated. The generation of the A frequency occurs during the first half of the clock period indicated by C1 being in a positive state and C0 in a negative state. The generation of the B frequency is accomplished during the second half of the clock period. This may be seen in the table.

The particular configuration of the D0 and D1 bits selects one of four values of $\Delta\theta 1$ and the configuration of the D2 and D3 bits selects one of four values of $\Delta\theta 2$, selections being made from addresses i through i+7 on the basis of the line control word and from the $\Delta\theta 1$ group on the basis of the C1 clock pulse and from the $\Delta\theta 2$ group on the basis of the C2 clock pulse. As previously stated, the nature of the data stored and the location i+8 through i+15 is similar

differing only in the values stored. The selection signals except for the line control word are substantially similar.

The contents of the read only memory 33-2 accessed by the output of address generator 31-2 are applied to one input of an adder circuit 34-2. The adder circuit 34-2 in this modulator is always operated in the add mode and the adder control circuit 38-2 produces this result since the two clock pulses are applied to an OR circuit 52 which has its output connected to one of two inputs of an AND circuit 53. The other input of the AND circuit is connected to a positive source of voltage and provides one level at all times since the clock pulses C1 and C2 are positive in alternate half-cycles of the clock generator 30-2. The other control circuit 38-2 was inserted primarily to indicate the compatibility with the other modulator forms disclosed and described above.

The output of adder 34-2 is selectively applied to one of two registers 36-2 or 37-2 under control of a read/write control circuit 35-2 which responds to clock pulses C1 and C2. When clock pulse C1 is received, register 36-2 is connected to the output of adder circuit 34-2 and when clock pulse C2 is received, register 37-2 is connected to the output of adder circuit 34-2. The outputs of registers 36-2 and 37-2 are connected to the other input of adder circuit 34-2 and are controlled by read/write control circuit 35-2 in the same manner as the input from adder 34-2. Thus, during the first clock cycle, $\Delta\theta 1$ selected by the inputs previously described is added to the contents of register 36-2 and reinserted in register 36-2. During the second half-cycle of the clock period, $\Delta\theta 2$ as previously described, is added to the contents of register 37-2.

The output of adder 34-2 is applied to a θ to sine θ conversion circuit 41-2 identical to the circuits previously described. The output of the conversion circuit is connected to a register 45-1 which is under control of a read/write control circuit 46-1 which responds to clock pulses C1 and C2. During clock pulse C1, the output of the converter circuit 41-2 is inserted in register 45-1. During clock pulse C2, the contents previously stored in register 45-1 is applied to one input of an adder circuit 47-1. The other input of adder circuit 47-1 is connected to converter 41-2 and forms the sum of the two values applied to the two inputs. The output of adder 47-1 is connected to another register 42-2 which is gated at the trailing edge of clock pulse C2 to a digital to analog converter 43-2 which has its output connected to a simple RC filter 44-2.

The modulator described above in Fig. 6 is useful for multifrequency or parallel tone generation which may be applicable for data transmission or auto dialing. These applications use sufficiently low baud rates as not to require the bandwidth reduction techniques used in the two previously described modulators. If higher baud rates are required, the technique described in connection with Fig. 2 may be used. One of four tones are generated from each of two bands depending on a baud of data consisting of four bits. The processing period is divided into two segments C1 and C2. During the C1 segment, bits D0 and D1 select one of four values of $\Delta\theta$ from the memory, the value of $\Delta\theta$ determines the frequency of the tone which will be generated. The value of tone 1, $\theta 1(t)$ stored in register 36-2, is incremented during each C1 time and converted to an amplitude value $\sin \theta 1(t)$ and placed in the buffer register 45-1. During C2 time, the phase of the

second tone, θ2(t) is incremented by a value Δθ determined by input bits D2 and D3. The amplitude of the second tone sin θ2(t) stored in register 37-2 is added to the contents of buffer register 45-1 to produce the next two tone transmitted signal at the end of C2 time.

Fig. 8 discloses an overall block diagram for a multiline multimode modulator which is capable of servicing n input and n output lines substantially simultaneously by a time sharing technique of the modulator. The modulator is capable of providing different varieties of three major types of modulations for any mix of the n lines. The modulation types provided are multifrequency, frequency shift keyed and differential phase shift key modulation. A number of different varieties of each of the types of modulators may be implemented as will become apparent as the description continues.

The multiline multimode modulator includes an input multiplexer 60 connected to n multiwire input lines or cables L1 through Ln. The multiplexer outputs are connected via an OR circuit 61 to a multimode modulator 62 where the signals from each of the n lines are sequentially modulated as required for the particular line. The modulated signals from the multimode modulator 62 are applied to a second multiplexer 63 which distributes the modulated signals to the appropriate output lines 1-n via individual RC filters 64-1 through 64-n. Filters 64-1 through 64-n are identical and each are simple RC filters whose sole function is to remove the quantizing noise from the digital to analog conversion process. A master clock circuit 65 provides control signals to multiplexers 60 and 63 as well as to the multimode modulator 62. In addition, master clock circuit 65 provides control signals to a line control word

memory unit 66 which provides signals to the multimode modulator 62 and the master clock circuit 65. Multiplexers 60 and 63 operate in synchronism under control of master clock circuit 65, thus input lines 1-n are sequentially connected through the multimode modulator 62 to output lines 1-n, respectively. The line control word memory unit 66 includes n address each identified with one of the input lines L1-n and in which is stored a line control word identifying the precise modulation required for that line. That is, which type of modulator it is and which variety of modulator of that type is being serviced for that line at that time. The line control words may be changed as requirements for modulation for any line are changed. This may be done manually or automatically as will become apparent as the description continues.

The master clock 65 and the line control memory unit 66 are illustrated in detail in Fig. 9 since these units provide all of the control signals for the multiplexers 60 and 63 and the multimode modulator 62.

A clock generator 67 operates at a frequency nfs where fs is the sampling frequency per line and n is the number of lines which must be sampled. Except for the actual frequency utilized, this clock is similar to clock 30-1 of Fig. 4 and provides during each clock period, five outputs illustrated below the clock in graphic form. The first output is positive during the first quarter of the period and negative during the remainder of the period. The second output is positive only during the second quarter of the period. The third output is positive only during the third quarter of the period. The fourth and fifth outputs are positive during the first and second halves of the fourth quarter, respectively. The one

output from clock generator 67 is applied to a binary counter 68 which is arranged to count as high as n and recycle thus incrementing one count during each period of clock generator 67. The output of binary counter 68 are applied to a decoder circuit 69 which provides the enabling outputs for operating multiplexers 60 and 63 since the outputs of decoder 69 sequentially identify one of the n lines. The outputs of binary counter 68 are also applied via gate circuits 70 to latches 71 to provide a binary output identifying the lines. The output of latches 71 are applied directly to the multimode modulator 62 and the use of this output will be described later.

In additon, the outputs of binary counter 68 are utilized as addresses for accessing the random access line control word memory 72. Thus, each time binary counter 68 increments to a new value, a new word is read out of random access line control word memory 72 and provided on the data output bus 73. Random access line control word memory 72 is also provided with a data input bus and write control circuits whereby line control words may be inserted into the random access memory as needed or desired from some external source such as a computer 74 illustrated in the drawings. Typically, computer 74 may also be the source of the data which is being transmitted over lines L1 through Ln. Alternatively, the line control words may be inserted from a locally associated terminal connected to the data bus and the write control circuits and need only supply the address location and the data to be stored therein.

The data output on bus 73 from random access line control word memory 72 is applied to a decoder circuit 75 which provides one of three outputs identifying the modulation type. The outputs are labeled MT1, MT2 and MT3. The outputs of MT1-MT3 are

applied to the multimode modulator 62 as will be apparent in connection with the description of Fig. 10. The data output bus 73 is also applied to the multimode modulator 62 and the use of these signals will be described in connection with the description of Fig. 10.

The MT1 output from decoder 75 is connected to two AND gates 76-1 and 76-2. The output MT2 is connected to two AND gates 77-1 and 77-2 and the output MT3 is connected to five AND gates 78-1 through 78-5. Gates 78-1 through 78-5 are connected to outputs 1-5 respectively from clock generator 67 and provide five sequential outputs when the line control word decoded indicates a differential phase shift keyed modulation function must take place for that line. The outputs of the gate 78-1 through 78-5 for convenience have been labeled A, B, C, D1 and D2, respectively. These pulses in the description which follows will be considered clock pulses appearing during a single sampling period for processing purposes in the circuit of Fig. 10 which is a detailed block diagram of the multimode modulator 62. These signals are applied to the modulator 62 as seen in Fig. 10 in the places indicated by the above alphabetic labels. Outputs 1 and 2 of clock generator 67 are connected to an OR circuit 79 which has its output connected to AND gates 67-1 and 77-1. Outputs 3, 4 and 5 from clock generator 67 are connected to OR circuit 80 which has its output connected to AND gates 76-2 and 77-2. AND gates 77-1 and 77-2 provide outputs A1 and B1 respectively when the modulation required is FSK while AND gates 76-1 and 76-2 provide outputs A2 and B2 when the modulation required is multifrequency. The timings provided by the signals from these AND gates may be determined from the graphs shown below clock generator 67.

Clocks A1 and B1 occupy the first and second halves of a sampling period, and are active during a FSK modulation. Clocks A2 and B2 occupy the first and second halves of a sampling period and are provided when a multi-frequency modulation takes place for a given line. Clocks A, B, C, D1, and D2 are provided when a DPSK modulation is taking place for a given line and are identical in timing during a single clock period as shown in the graphs below clock generator 67.

The multimode modulator illustrated in Fig. 10 is similar in many respects to the DPSK modulator illustrated in Fig. 4. However, it utilizes three separate address generators, each similar to those previously described and three adder control circuits similar to those previously described and selection gates under control of the signals MT1 through MT3 illustrated in Fig. 9 and previously described.

A three section address generator 80 having a first section 80-1 for generating addresses based on the input data for the selection of signals from the memory suitable for producing multifrequency tone pairs; a section 80-2 for generating addresses suitable for the selection of data for generating differential phase shift keyed signals; and a section 80-3 suitable for generating addresses for accessing data suitable for generating frequency shift keyed signals is connected to the output as indicated of OR circuit 61 which provides up to four data lines in parallel. The sections are also connected to the A1, B1, A2, B2, A, B, C, D1 and D2 clock signals from the master clock 65; to the line control words from the data output bus 73 of random access line control word memory 72; and to a τ register 32-2 similar to the τ registers previously

described in connection with the description of Figs. 2 and 4 and which will be described in detail below. Section 80-1 may be identical to the address generator 31-2 illustrated in Fig. 6. Section 80-2 may be identical to the address generator 31-1 illustrated in Fig. 4 and section 80-3 may be identical to the address generator 31 illustrated in Fig. 2. The outputs of sections 80-1 through 80-3 are connected by gates 81-1 through 81-3 to the control input of a read only memory 82 which contains all the information in read only memories 33, 33-1 and 33-2 of Figs. 2, 4 and 6, respectively.

The three section adder control circuit 83 provides adder control for each of the three modulation modes, and includes a first section 83-1 for providing the adder control function for differential phase shift keyed modulation, a second section 83-2 for providing adder control for frequency shift keyed modulation and a third section 83-3 for performing adder control for multifrequency modulation. The inputs to each of these sections are identical to the corresponding adder control circuits shown in Figs. 2, 4 and 6. Each of the sections is connected by a switch 84 under control of the MT1 through MT3 outputs from decoder 75 to the control input of an adder 34-3 which is similar to adders 34-1 through 34-2 shown in the previous figures.

The output of read only memory 82 is connected to one of the inputs of adder 34-3. The output of adder 34-3 is connected to the data input bus of a random access memory 85 and the output bus of random access memory 85 is connected to the other input of adder 34 and to a τ buffer 32-2 similar to the τ buffers 32 and 32-1 shown in Figs. 2 and 4, respectively. Random access memory 85 contains two address locations for

each of the n lines serviced by the multiline, multifrequency modulator. Which of these addresses is selected is controlled by an address generator and read/write control circuit 35-3 which responds to the LC output from latches 71 and the clock signals A1, B1, A2, B2, A, B, C, D1 and D2 from master clock circuit 65.

For example, if the multiline, multimode modulator is serving four lines, the output of binary counter 68 will be provided on two lines which may be 00, 10, 01 and 11 depending upon which line is being serviced. These two lines may be used as the high order bits of the address in random access memory 85. The low order bit for the address will be selected as a function of the clock signals, A1, A2, and A indicating a 0 low order bit and the other clock pulses indicating a 1 low order bit. During clock times D1 and D2, a read operation only takes place. The output of random access memory 85 in addition to being connected to the other input of adder circuit 34-3 is connected to a τ buffer 32-2 which is loaded during the A and the A1 clock pulse times. The three high order bits from buffer 32-2 are applied to address generators 80-2 and 80-3 and perform the same functions in these address generator sections as they performed in the single line versions described in Figs. 2 and 4. The output of adder 34-3 is applied to a $\theta/\sin\theta$ conversion circuit 41-3 similar to all of the previously described $\theta/\sin\theta$ conversion circuits. The remainder of the circuit is functionally similar to that of Fig. 4 and includes a register 45-2 connected to the output of $\theta/\sin\theta$ conversion circuit 41-3 for receiving the output therefrom under control of a read/write and clear circuit 46-2 and supplying an input to a second adder circuit 47-2 which is also connected to the output of circuit 41-3. A

register 42-3 is connected to adder 47-2 and supplies when gated a digital to analog converter circuit 433. Read/write and clear control circuit 462 is responsive to clock pulses A, A1, A2, B2, D1 and D2. During clock pulses A and A1, the register is cleared to thus cause adder circuit 472 to directly pass the output of conversion circuit 41-3 to the register 42-3 without alteration since in these instances, the function performed by the adder circuit 47-2 is not needed or desired. During the D1 and A2 clock times, the contents from conversion circuit 41-3 are read into the register 45-2 and during the D2 and B2 clock pulses, the contents of register 45-2 are read into the adder circuit 47-2 where they are added to the then available contents from conversion circuit 41-3. The output from digital to analog converter circuit 43-3 is applied to the input of multiplexer 63 illustrated in Fig. 8 and under control of the master clock signals from clock 65, it is distributed to the appropriate output line 1-n via the simple RC filters 64-1 through 64-n.

The three major modulation techniques implemented in Fig. 10 are identical to the three modulation techniques illustrated and described with respect to Figs. 2, 4 and 6. The only difference being that the address generator for accessing read only memory 82 is expanded to encompass all of the various modulation types, the clock is expanded to provide each of the clocking signals, the adder control circuit 83 is expanded to provide the three different types of addition control previously described and the switch 84 is provided to connect the appropriate adder control signals as indicated by the signals from the master clock 65. The only other addition is the expansion of random access memory 85 to include

two address positions for each of the lines handled by the multiline, multimode modulator. Since only two address positions are required for each line, random access memory 85 is general purpose and the only signals needed to select the appropriate addresses are those signals from master clock 65 which identify the line currently being serviced and those clocking signals necessary to control the function of the memory 85. The remaining circuits are, as previously stated, identical to those of Figs. 4 and 6. Insofar as the modulation technique described in Fig. 2 is concerned, the adder 47-2 and the register 45-2 and control 46-2 are superfluous and the reason for providing the reset signal as stated above, is to remove these circuits in those instances where the frequency shift key modulation is being implemented. Since in those instances, zero is inserted in the register 45-2 and an addition of zero to the digital signals provided by the converter circuit 45-3 passes those signals on through to register 42-3 unchanged.

It is obvious that this circuit provides substantial savings in cost since expanding it to 16 or more lines merely required minor additions to the read/only memory 82 to store the factors of the different types of modulation required and the expansion of the random access memory 85 to include two registers for each of the lines serviced.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A multiline multimode modulator for substantially simultaneously modulating a plurality of different signals onto a plurality of different output lines and in which one of n different modulations of m types may be selected for any of the output lines comprising:

a master clock means operating at a clock frequency substantially higher than the baud rate for any of the modulations to be performed and providing a first clock output at the said frequency and selectively one of m multiphase clock output signals during each period of said clock frequency;

a line control word memory including read and write control means and a number of addresses at least equal to the number of lines to be serviced for storing line control words which uniquely define the modulation to be performed for the line corresponding to the address location and responsive to said first clock output for providing line control words in a predetermined seuqence;

a digital multimode modulator including a memory for storing digital numerical values representing the modulation parameters for each of the said n different modulations, digital processing circuits connected to said memory for receiving the stored digital numerical values provided thereby and responsive to the data to be modulated, the line control word signals and the selected one of m multi-phase clock output signals for generating a modulated output signal as a function of the above said signals, and an address generator responsive to the data signals to be modulated, the line control and word signals, the digital processing circuits and the selected one of m multiphase clock output signals for generating a predetermined plurality of sequential address signals for supplying the memory contents of the associated addresses to the said digital processing circuits; and

multiplexing means responsive to said first clock output for supplying in sequence signals from one of a plurality of sources to said digital multimode modulators and supplying the output from said

multimode modulator in sequence to one of a plurality of lines.

2. A multiline multimode modulator as set forth in claim 1 in which the modulation performed for any line may be changed by writing a new line control word defining the new modulation into the address in the line control word memory associated with the line.

3. A multiline multimode modulator as set forth in claim 2 in which said m multiphase clock outputs is at least two and one provides two clock phases for controlling as FSK modulation and the other provides at least three clock phases for controlling a DPSK modulation.

4. A multiline multimode modulator as set forth in claim 3 in which said digital processing circuits includes common circuits for each of the m modulation types and a read/write memory including a pair of registers for each line for storing calculated parameters and selectively during each cycle of operation by the said line control word signals and clock phase signals.

5. A multiline multimode modulator for substantially simultaneously modulating a plurality of different signals onto a plurality of different output lines and in which one of n different modulations of m types may be selected for any of the output lines comprising:

a master clock means operating at a first clock frequency (nfs) in which fs is substantially higher than the baud rate for any of the modulations to be performed and n is equal to the number of output lines and providing a first clock output at the said clock frequency and selectively one of m multiphase clock output signals during each period of said clock frequency;

a line control word memory including read and write control means and a number of addresses at least equal to the number of lines to be serviced for storing line control words which uniquely define the modulations to be performed for the line corresponding to the address location and responsive to said first clock frequency for providing line control words in a predetermined sequence;

a digital multimode modulator including a memory for storing digital numerical values representing the modulation parameters for

each of the said n different modulations, said parameters for each of said n different modulators including a plurality of numerical values for each of the possible signal transitions which are selected at least once within each interbaud time in which a transition occurs to cause said transition to follow substantially reduced out of band frequency components, digital processing circuits connected to said memory for receiving the stored digital numerical values provided thereby and responsive to the data to be modulated, the line control word signals and the selected one of m multiphase clock output signals for generating a modulated output signal as a function of the above said signals, and an address generator responsive to the data signals to be modulated, the line control word signals, the digital processing circuits and the selected one of m multiphase clock output signals for generating a predetermined plurality of sequential address signals for supplying the memory contents of the associated addresses to the said digital processing circuits; and

multiplexing means responsive to said first clock output for supplying in sequence signals from one of a plurality of sources to said digital multimode modulators and supplying the output from said multimode modulator in sequence to one of a plurality of lines.

6. A multiline multimode modulator as set forth in claim 5 in which the modulation performed for any line may be changed by writing a new line control word defining the new modulation into the address in the line control word memory associated with the line.

7. A multiline multimode modulator as set forth in claim 6 in which said m multiphase clock outputs is at least two and one provides two clock phases for controlling as FSK modulation and the other provides at least three clock phases for controlling a DPSK modulation.

8. A multiline multimode modulator as set forth in claim 7 in which said digital processing circuits includes common circuits for each of the m modulation types and a read/write memory including a pair of registers for each line for storing calculated parameters and

selectively during each cycle of operation by the said line control word signals and clock phase signals.

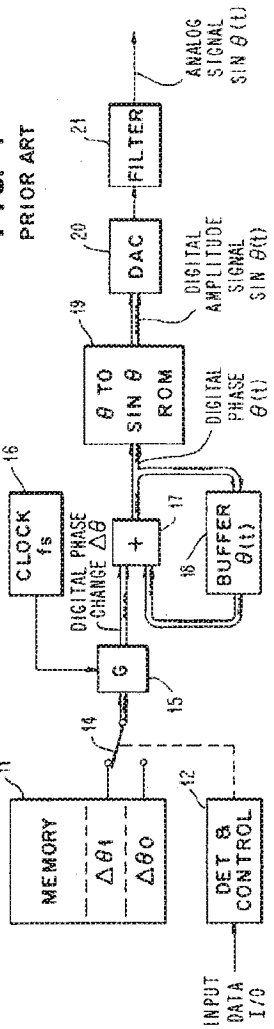

FIG. 1
PRIOR ART

FIG. 1A

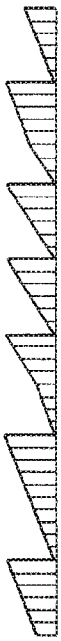

FIG. 1B

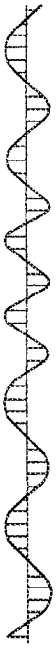

FIG. 1C

PATENT AGENT

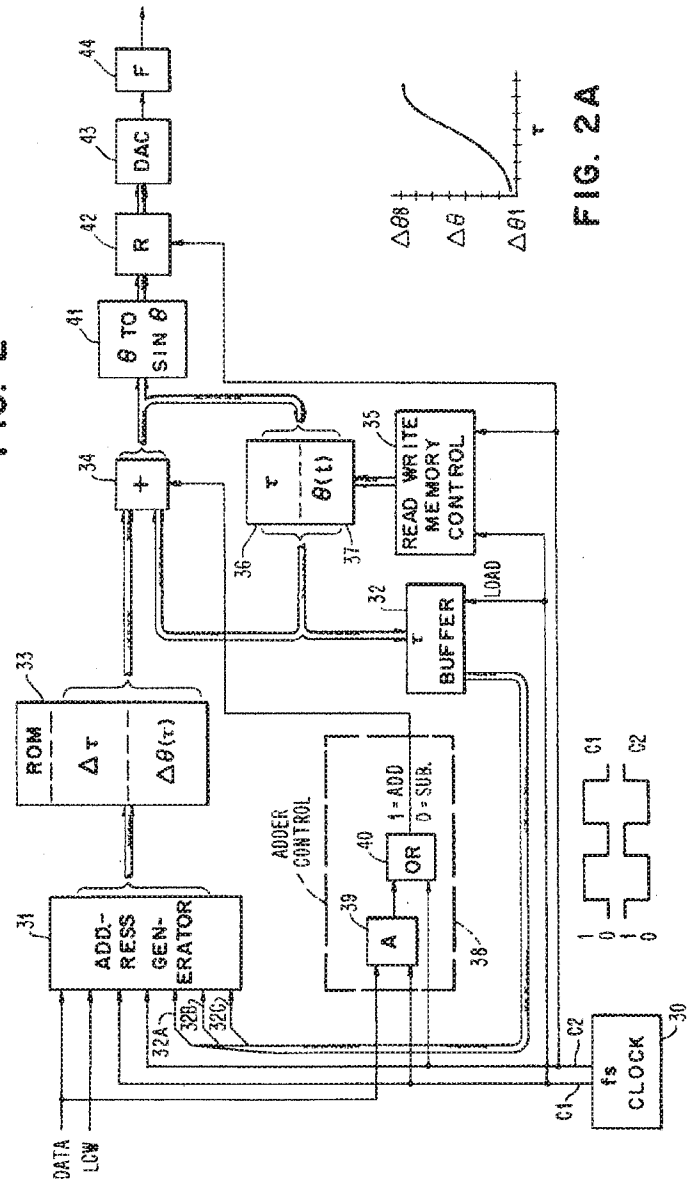

FIG. 2

FIG. 2A

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FIG. 3

MEMORY ADDRESS	MEMORY CONTENTS	LCW	DATA	$\overbrace{A\ B\ C}^{\tau}$	C1	C2
i	T/θ FOR LINE TYPE 1	0	X	$[A+B+C]\cdot\overline{A\cdot B\cdot C}$	1	0
i+1	000·····00	0	0 1	0 0 0 1 1 1	1	0
i+2	$\Delta\theta 1$ FOR TYPE 1	0	X	0 0 0	0	1
i+3	$\Delta\theta 2$ " " "	0	X	0 0 1	0	1
i+4	$\Delta\theta 3$ " " "	0	X	0 1 0	0	1
i+5	$\Delta\theta 4$ " " "	0	X	0 1 1	0	1
i+6	$\Delta\theta 5$ " " "	0	X	1 0 0	0	1
i+7	$\Delta\theta 6$ " " "	0	X	1 0 1	0	1
i+8	$\Delta\theta 7$ " " "	0	X	1 1 0	0	1
i+9	$\Delta\theta 8$ " " "	0	X	1 1 1	0	1
MEMORY ADDRESS	MEMORY CONTENTS	LCW	DATA	$\overbrace{A\ B\ C}^{\tau}$	C1	C2
j	T/θ FOR LINE TYPE 2	1	X	$[A+B+C]\cdot\overline{A\cdot B\cdot C}$	1	0
j+1	000·····00	1	0 1	0 0 0 1 1 1	1	0
j+2	$\Delta\theta 1$ FOR TYPE 2	1	X	0 0 0	0	1
j+3	$\Delta\theta 2$ " " "	1	X	0 0 1	0	1
j+4	$\Delta\theta 3$ " " "	1	X	0 1 0	0	1
j+5	$\Delta\theta 4$ " " "	1	X	0 1 1	0	1
j+6	$\Delta\theta 5$ " " "	1	X	1 0 0	0	1
j+7	$\Delta\theta 6$ " " "	1	X	1 0 1	0	1
j+8	$\Delta\theta 7$ " " "	1	X	1 1 0	0	1
j+9	$\Delta\theta 8$ " " "	1	X	1 1 1	0	1

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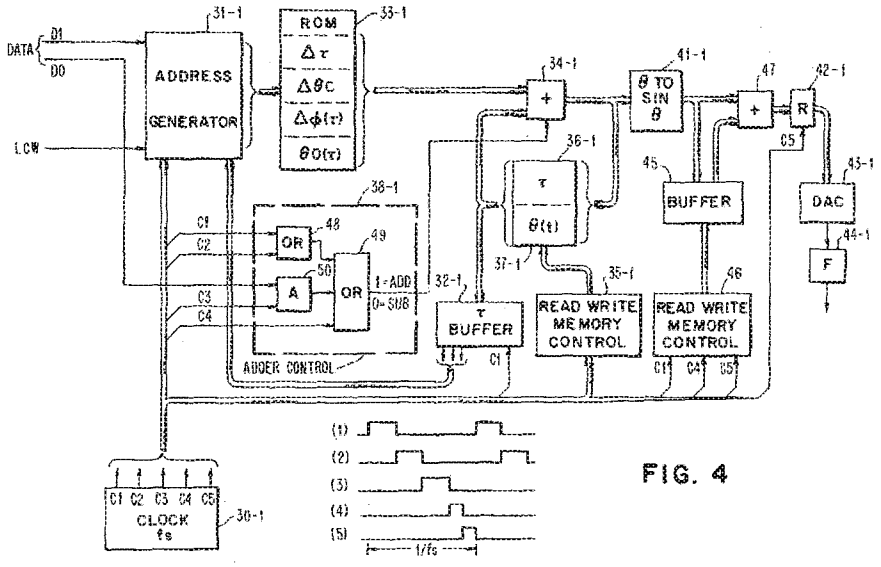

FIG. 4

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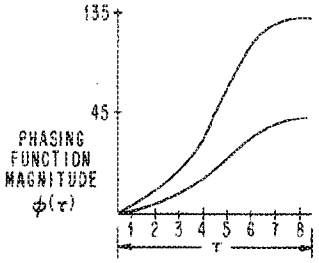

FIG. 4A

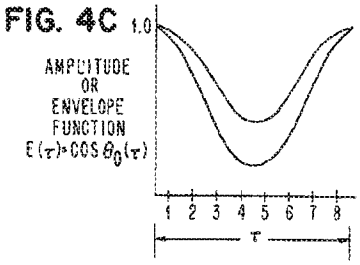

FIG. 4C

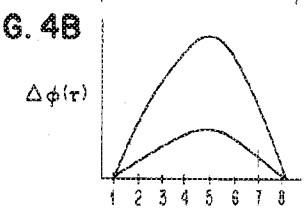

FIG. 4B

FIG. 7

MEMORY ADDRESS	MEMORY CONENTS	LCW	DO	D1	D2	D3	C1	C2
i	$\Delta\theta 1$ FOR LINE TYPE 1 fA1	0	0	0	X	X	1	0
i+1	$\Delta\theta 1$ FOR LINE TYPE 1 fA2	0	0	1	X	X	1	0
i+2	$\Delta\theta 1$ " fA3	0	1	0	X	X	1	0
i+3	$\Delta\theta 1$ " fA4	0	1	1	X	X	1	0
i+4	$\Delta\theta 2$ " fB1	0	X	X	0	0	0	1
i+5	$\Delta\theta 2$ " fB2	0	X	X	0	1	0	1
i+6	$\Delta\theta 2$ " fB3	0	X	X	1	0	0	1
i+7	$\Delta\theta 2$ " fB4	0	X	X	1	1	0	1
i+8	$\Delta\theta 1$ FOR LINE TYPE 2 fA1	1	0	0	X	X	1	0
i+9	$\Delta\theta 1$ " fA2	1	0	1	X	X	1	0
i+10	$\Delta\theta 1$ " fA3	1	1	0	X	X	1	0
i+11	$\Delta\theta 1$ " fA4	1	1	1	X	X	1	0
i+12	$\Delta\theta 2$ " fB1	1	X	X	0	0	0	1
i+13	$\Delta\theta 2$ " fB2	1	X	X	0	1	0	1
i+14	$\Delta\theta 2$ " fB3	1	X	X	1	0	0	1
i+15	$\Delta\theta 2$ " fB4	1	X	X	1	1	0	1

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MEMORY ADDRESS	MEMORY CONTENTS	LCW	DATA	CLOCK	τ		
					A	B	C
i	T/8 FOR LINE TYPE 1 = ($\Delta\tau$)	0	X	C1	X	X	X
i + 1	$\Delta\theta$C FOR LINE TYPE 1	0	X	C2	X	X	X
i + 2	$\Delta\phi(\tau)_1$ FOR LINE TYPE 1 135°	0	0	C3	0	0	0
i + 3	$\Delta\phi(\tau)_2$ " " " " "	0	0	C3	0	0	1
i + 9	$\Delta\phi(\tau)_8$ FOR LINE TYPE 1 135°	0	0	C3	1	1	1
i + 10	$\Delta\phi(\tau)_1$ " " " " 45°	0	1	C3	0	0	0
i + 11	$\Delta\phi(\tau)_2$ " " " " "	0	1	C3	0	0	1
i + 17	$\Delta\phi(\tau)_8$ FOR LINE TYPE 1 45°	0	1	C3	1	1	1
i + 18	$\theta 0(\tau)_1$ FOR LINE TYPE 1 135°	0	0	C4/C5	0	0	0
i + 19	$\theta 0(\tau)_2$ " " " " "	0	0	C4/C5	0	0	1
i + 25	$\theta_0(\tau)_8$ FOR LINE TYPE 1 135°	0	0	C4/C5	1	1	1
i + 26	$\theta_0(\tau)_1$ " " " " 45°	0	1	C4/C5	0	0	0
i + 27	$\theta_0(\tau)_2$ " " " " "	0	1	C4/C5	0	0	1
i + 33	$\theta_0(\tau)_8$ FOR LINE TYPE 1 45°	0	1	C4/C5	1	1	1
j	T/8 FOR LINE TYPE 2	1	X	C1	X	X	X
j + 1	$\Delta\theta$C FOR LINE TYPE 2	1	X	C2	X	X	X
j + 2	$\Delta\phi(\tau)_1$ FOR LINE TYPE 2 135°	1	0	C3	0	0	0
j + 9	$\Delta\phi(\tau)_8$ FOR LINE TYPE 2 135°	1	0	C3	1	1	1
j + 10	$\Delta\phi(\tau)_1$ " " " " 45°	1	1	C3	0	0	0
j + 17	$\Delta\phi(\tau)_8$ FOR LINE TYPE 2 45°	1	1	C3	1	1	1
j + 18	$\theta_0(\tau)_1$ " " " " 135°	1	0	C4/C5	0	0	0

FIG. 5

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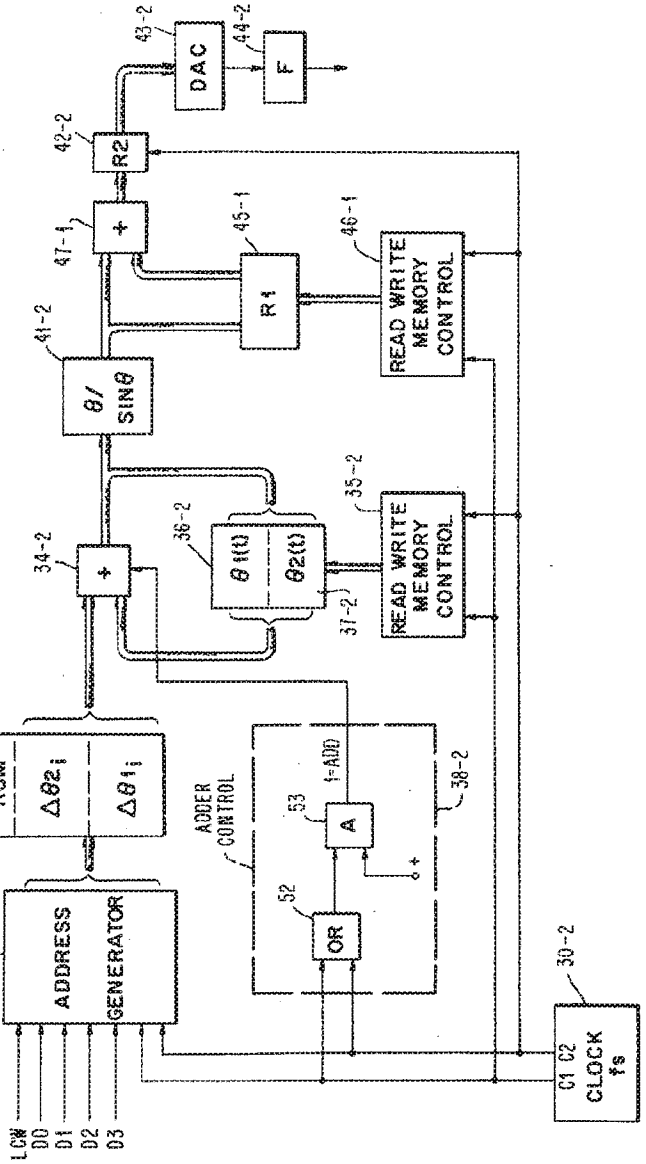
FIG. 6



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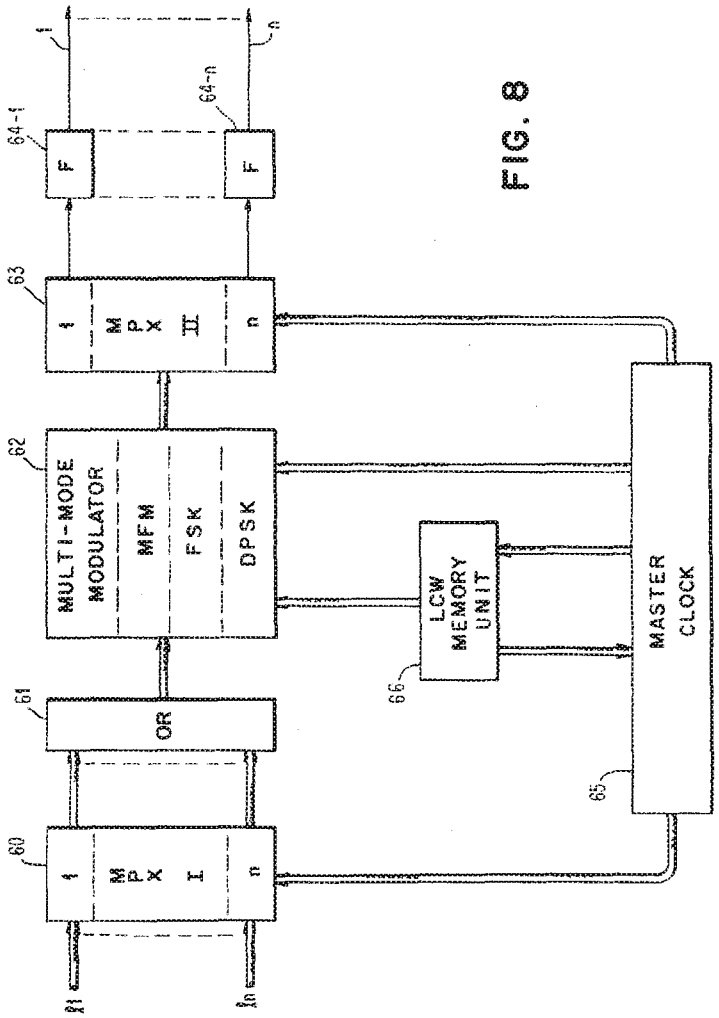

FIG. 8

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FIG. 9

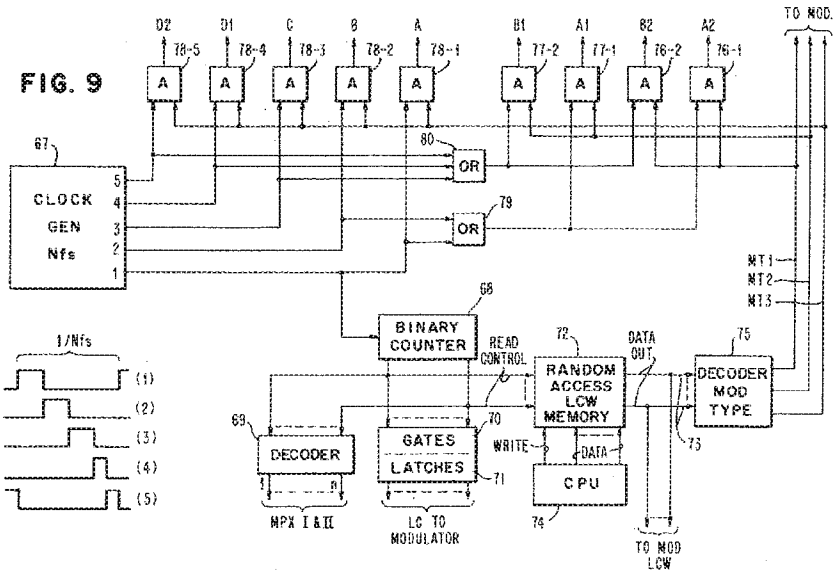

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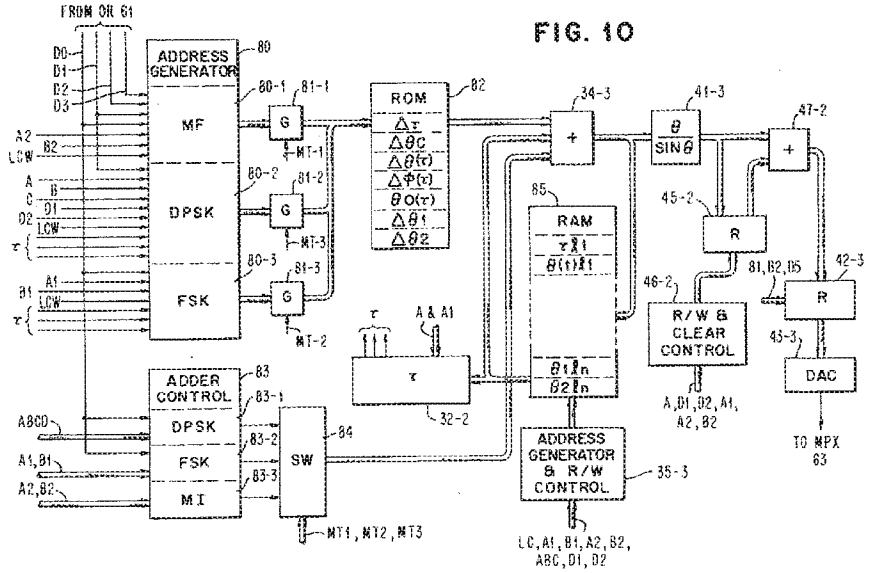
FIG. 10



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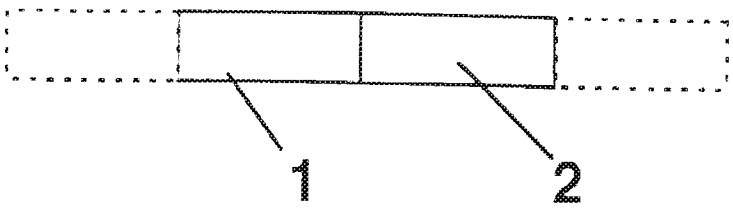
(54) **EMETTEUR-RECEPTEUR DE TRAMES MULTIMODULATION**
(54) **MULTI-MODULATION FRAME EMITTER/RECEIVER**



(57) La présente invention porte sur une trame multimodulation qui comprend au moins un premier intervalle de temps (1) et un second intervalle de temps (2) qui suit le premier. Ce premier et ce second intervalle de temps (1 et 2) sont définis par une première modulation et par une seconde modulation respectivement. La trame est caractérisée par le fait que le dernier symbole de constellation du premier intervalle de temps défini par la première modulation coïncide en phase et en amplitude avec l'un des symboles de la seconde modulation.

(57) The present invention refers to a multi-modulation frame including at least a first time interval (1) and a second time interval (2), following the first time interval (1). Said first and second time intervals (1 and 2) are defined by a first modulation and by a second modulation respectively. The frame is characterised in that a last constellation symbol from the first time interval with the first modulation coincides in phase and amplitud with a symbol from the second modulation.

ABSTRACT

The present invention refers to a multi-modulation frame including at least a first time interval (1) and a second time interval (2), following the first time interval (1). Said first and second time intervals (1 and 2) are defined by a first modulation and by a second modulation respectively. The frame is characterised in that a last constellation symbol from the first time interval with the first modulation coincides in phase and amplitud with a symbol from the second modulation.

MULTI-MODULATION FRAME EMITTER/RECEIVER

OBJECT OF THE INVENTION

The present invention refers to a multi-modulation frame and also to an emitter and a receiver in order to emit and receive the said multi-modulation frame. The emitter and/or receptor, according to the invention, may be embodied, for example, in the unit of a portable radio-communications system. A frame is defined as a signal which includes successive time intervals. A multi-modulation frame is characterised in that it includes at least two time intervals, each of which being defined by respective modulations which are different from each other.

STATE OF THE ART

A frame of the type defined above, can be used, for example, in the D.E.C.T. standard (Digital Enhanced Cordless Telecommunications) of the E.T.S.I. (European Telecommunications Standards Institute) with the objective of increasing the traffic capacity in at least one channel, or temporary interval, without changing the modulation defined for other channels.

For example, and referring to the drawings in figures 1, 2A and 2B, a first time interval, 1, is defined by a GFSK (Frequency Shift Keying) modulation already used in the D.E.C.T. and another time interval 2 is defined by a π/4DQPSK (π/4-Differential Phase Shift Keying). The two modulations define respective constellations which appear in figure 2A and 2B in relation to predefined references.

In the D.E.C.T. standard the modulated signal is delimited by a spectral pattern within which the modulated signal must be circumscribed.

When use is made of two modulations in the same frame, for example, the modulations which appear in figures 2A and 2B, the resulting signal defines a spectrum which does not enter into the predefined DECT pattern.

CHARACTERISATION OF THE INVENTION

A first object of the present invention is to define a multi-modulation frame, which defines a spectrum which is circumscribed in a limited amplitude spectral pattern.

A second object of the invention is to define an emitter of a multi-modulation frame, according to the invention.

A third object of the invention is to define a receiver of a multi-modulation frame, according to the invention.

Consequently, a multi-modulation frame, according to the present invention, including at least a first time interval and a second time interval which follows the said first time interval, the first and second time intervals being defined by first and second modulations respectively, are characterised in that a last symbol of the constellation of the first time interval with the first modulation coincides in phase and amplitude with a symbol from the second modulation.

The result being that in all of the successive frames there is no "modulation skipping".

An emitter to produce the said frame includes first and second modulation means to modulate data according to the said first and second modulations respectively, and means for placing, in the initial phase values of the said second modulation means, through a first symbol of the second time interval, the phase of a last symbol produced by the said first modulation means in the said first time interval.

For example, in the case of GFSK and π/4DQPSK modulations, the means for placing in the initial values include:

- means for computing the phase of the last symbol of the GFSK modulation in the first time interval,

- means for selectively selecting, during the second time interval:

the phase of the symbol previous to the π/4DQPSK modulation when the posterior symbol is not the first symbol of that π/4DQPSK modulation in the first time interval, and

the phase of the computed symbol when the posterior symbol is the first symbol of said π/4DQPSK modulation,

with the aim of computing a π/4DQPSK modulation symbol.

A receiver to receive the said frame consists of first and second demodulation means to demodulate modulated data, according to those first and second modulations respectively, and means for placing, in the initial phase values of the said second demodulation means, the phase of the last symbol received by the said first demodulation means in the first time interval.

BRIEF DESCRIPTION OF THE DRAWINGS

A more detailed explanation of the present invention is given in the following description based on the attached drawings in which:

- figure 1 shows the format of a multi-modulation frame;

- figures 2A and 2B show the constellations relative to GFSK and π/4DQPSK modulations respectively;

- figure 3 shows two constellations and arrows pointing out the correspondence between the two constellations, according to the invention;

- figure 4 shows a block diagram of a multi-modulation frame emitter, according to the invention; and

- figure 5 shows a block diagram of a multi-modulation frame receiver, according to the invention.

DESCRIPTION OF THE INVENTION

The emitter, according to the invention, cancels out the "modulation skipping", or discontinuities which appear, according to the state of the art, in each of the successive frames. With reference to figures 2A and 2B, the respective constellations of the two modulations which are assigned in a single frame must, according to the invention, satisfy the following criteria: the respective phases and modules of all the symbols of one of the two constellations must correspond to respective phases and modules of the other constellation. Thus, for example, with reference to figures 2A and 2B, all the symbols of the GFSK modulation (figure 2A) correspond to some of the symbols of the constellation π/4DQPSK (figure 2B) as a result of a "rotation" of the GFSK constellation.

In more general terms, an adaptation of a constellation to another constellation needs to adapt the modules and phases of all the symbols of one of the two constellations to some of the modules and phases of the other constellation. The arrows in figure 3 more clearly show, according to the invention, the correspondence in phase and module of two constellations.

The following description refers to two GFSK and π/4DQPSK modulations which have equal modules although the invention can be applied to all other modulations, such as for example, nPSK (PSK, 4PSK, 8PSK, ...), nFSK, nGMSK, etc. In the case where a placing in correspondence in module of the two modulations were necessary, use can be made of a measuring circuit for the modules of at least some of the

symbols of one of the two modulations, and a gain control circuit which regulates the amplitude modules of the other modulation in order to regulate the modules of one of the constellations in relation to the module of the other modulation. The module measuring circuit and the gain control circuit are placed in the two demodulation chains respectively.

On the other hand, the invention is described for a particular case, according to which only two modulations are assigned within the same frame, although they can be assigned in other environments in which more than two modulations exist within one single frame.

The emitter of the invention, shown in figure 4, includes a demultiplexor (21), a first GFSK modulator (28), a second π/4DQPSK modulator (26), a control unit (29), a phase computer (30) and two multiplexors (31 and 33). In a conventional way the π/4DQPSK modulator (26) includes a symbol association unit (22), a correspondence table (23), an adder (24) a delay line (32) and an IQ quadrature signals generator (25). The control unit (29) assures the sequencing of the operation of the different circuits shown in figure 3.

Binary data are produced by a data source (20) to form a data stream. According to the format of the chosen frame, the GFSK modulation will be assigned to one part of the frame and the π/4DQPSK modulation will be assigned to the other part. A control unit (29) output is assigned to the π/4DQPSK modulation. A control unit (29) output is assigned to an input to the demultiplexor (21), the two outputs of which selectively and alternately receive the binary data produced by the source (20), for the data to be selectively modulated with GFSK (28) modulation or π/4DQPSK (26) modulation, depends on the position of the said data modulations within the frame. When the GFSK modulation is assigned to the data, the control unit (29) assigns a control signal to the multiplexor (33), which is reproduced at the signal output of the GFSK (28) modulator, in the form of IQ signals.

The π/4DQPSK modulator operates in the following way. The symbol association unit (22) associates a dephasing, with each two bits of the binary data, which is memorised in the table (23), and which defines a phase variation in relation to a previous phase. The previous phase and the dephasing are added, using the delay line (32) and the adder (24) to produce a current phase signal which is assigned to the IQ signals generator

(25). The generator (25) produces signals in IQ quadrature. Thus when the π/4DQPSK modulation is assigned to the data, the control unit (29) assigns a control signal to the multiplexor (33), which reproduces at its output the π/4DQPSK (26) modulator output signal in the form of IQ signals.

According to the invention the emitter in figure 4 includes means for placing in the initial phase values of the π/4DQPSK modulator, for a first symbol of the second time interval (2) with π/4DQPSK (26) modulation, the phase of a last symbol produced by the GFSK modulator in the first time interval (1). These means for placing the initial values include the phase computer (30) which computes the phase of the last symbol of the GFSK modulation, just before the first symbol with π/4DQPSK modulation. The phase of the last symbol of the GFSK modulation which is computed by the circuit (30) is assigned to an adder (24) input through the multiplexor (31), in correspondence with the first symbol of the time interval with π/4DQPSK modulation. For this reason the control unit (29) assigns a control signal to the multiplexor (31) in order to validate the phase computer (30) output in correspondence with this first symbol of the π/4DQPSK modulation. Thus, during the time interval with π/4DQPSK modulation, the phase of the previous symbol of the π/4DQPSK modulation is selectively selected when the posterior symbol is not the first symbol of the time interval with π/4DQPSK modulation, and the phase of the symbol computed by the computer (30) when the posterior symbol is the first symbol of the time interval with π/4DQPSK modulation.

The result is that the frame obtained with the emitter of the invention includes a first time interval and a second time interval which follows the first time interval, the first and second time intervals being defined by the first GFSK modulation and the second π/4DQPSK modulation respectively. Also, the phase of a last constellation symbol from the first interval with GFSK modulation coincides with a phase of a constellation symbol of the π/4DQPSK modulation.

It should be noted that the GFSK modulator (28) and the π/4DQPSK modulator (26) include respective filters, Gaussian for example, and a raised cosine root, with different temporal delays between them. In order to avoid this delay difference, a single filter can be used at the emitter output in figure 4, without integrating filters in the modulators (28 and 25). On the other

hand, if filters are used on the modulators (26 and 25), a fixed delay is assigned to the signal received when it is directed to the symbol association unit (22).

The receiver, according to the invention, is shown in figure 5. It includes a demultiplexor (40), a control unit (41), a GFSK demodulator (42), two multiplexors (43 and 44) and a π/4DQPSK demodulator (50). The demodulator (50) includes a delay line (45) a π phase shifter (46), a multiplier (48) and a detector (47). The control unit (41) assigns a control signal to the demultiplexor (40) in such a way hat the frame, according to the invention, which is received is selectively and alternatively assigned to the modulators (42 and 50). The control unit (41) assigns this control signal to the demultiplexor on the basis of the format of the frame in such a way that the first time interval with GFSK modulation is assigned to the demodulator (42), and that the second time interval, with π/4DQPSK modulation is assigned to the demodulator (50). For this reason the control unit (41) is synchronised using bits produced at the demodulator (42) output.

Noting $e^{i\varphi}n$, the nth symbol of the π/4DQPSK modulation, it follows that, through the link including the delay line (45), the phase shifterr (46) and the multiplier (48), the output of the multiplier (48) produces a signal $e^{\Delta i\varphi}n$ representative of the phase shift between the previous range symbol (n-1) and the current range symbol (n). The detector (47) produces a sequence of bits on the basis of the phase shifting signal $e^{\Delta i\varphi}n$. According to the invention, for a first symbol of the second time interval, the control unit (41) selects the signal assigned to the GFSK demodulator input, for placing the initial values of the demodulator (50) phase, in the phase of a last symbol received in the first time interval. For this reason, the control unit (41) selects, through the multiplexor (44), the signal assigned to the demodulator (42) in order to assign it to the phase shifter (46) when the last symbol of the first time interval is assigned to the said demodulator (42). After the first symbol of the second time interval, that is for all the other symbols of the second time interval, the delay line (45) output is assigned to the phase shifter (46) input. Thus the initialisation phase of the demodulator (50) corresponds to the phase of the last symbol received by the demodulator (42).

In the case where the placing in module correspondence of the two modulations is necessary, a gain control circuit can be used with a

predefined gain value which is a function of the known modules of the two modulations and which regulates the modules of one of the two constellations, in order that that constellation coincides with the other modulation. This gain control circuit is placed in the corresponding demodulation chain.

CLAIMS

1 - Multi-modulation frame, including at least a first time interval (1) and a second time interval (2) which follows the said first time interval (1), the first and second time intervals (1 and 2) being defined by first and second modulations respectively, characterised in that a last symbol of the first time interval constellation with the first modulation coincides in phase and amplitude with a symbol from the second modulation.

2 - Multi-modulation frame, according to claim 1, characterised in that the said first modulation is a GFSK modulation, and the said second modulation is a π/4DQPSK modulation.

3 - Emitter for producing a frame, according to claim 1, characterised in that it includes first and second modulation means (26 and 28) for the modulating data according to the first and second modulations respectively, and means (29,30,31) for placing in the initial phase values of the said second modulation means (26), for a first symbol of the second time interval, the phase of a last symbol produced by the said first modulation means (28) in the said first time interval (1).

4 - Emitter, according to claim 3, for producing a frame according to claim 2, characterised in that the said means for placing in the initial values include:

- means (30) for computing of the phase of the last symbol of the GFSK modulation, in the first time interval (1),

- means (29 and 30) for selectively selecting, during the second time interval:

the phase of the previous symbol of the π/4DQPSK modulation when the posterior symbol is not the first symbol of the said π/4DQPSK modulation in the first time interval (1), and

the phase of the computed symbol, when the posterior symbol is the first symbol of the said π/4DQPSK modulation,

with the aim of computing a π/4DQPSK modulation symbol.

5 - Receiver for receiving a frame according to claim 1, characterised in that it includes first and second demodulation means (42 and 50) for the demodulation of modulated data, according to the said first and second modulations respectively, and means (41 and 44) for placing in the initial phase values of the said second demodulation means (50), for a first symbol

of the second time interval (2), the phase of a last symbol received by the said first demodulation means (28) in the first time interval (1).

6 - Receiver according to claim 5, characterised in that it includes gain control means.

7 - Unit of a radio-communications system with the mobiles including an emitter according to claim 3.

8 - Unit of a radio-communications system with the mobiles including a receiver according to claim 5.

FIG 1

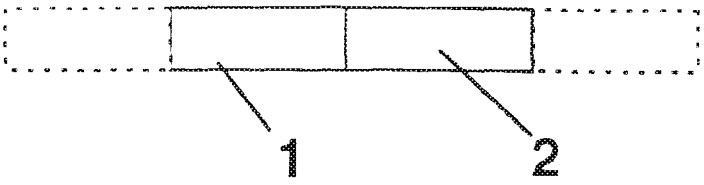


FIG.2A

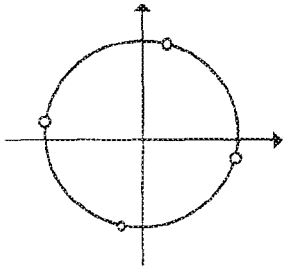


FIG.2B

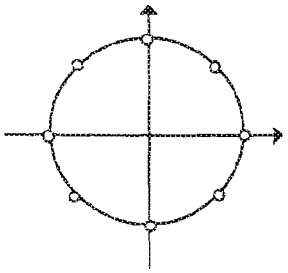


FIG.3

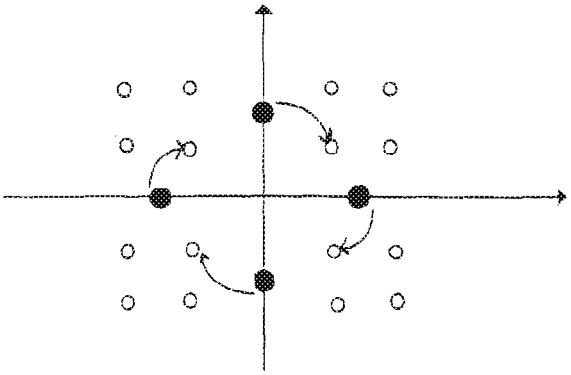


FIG. 4

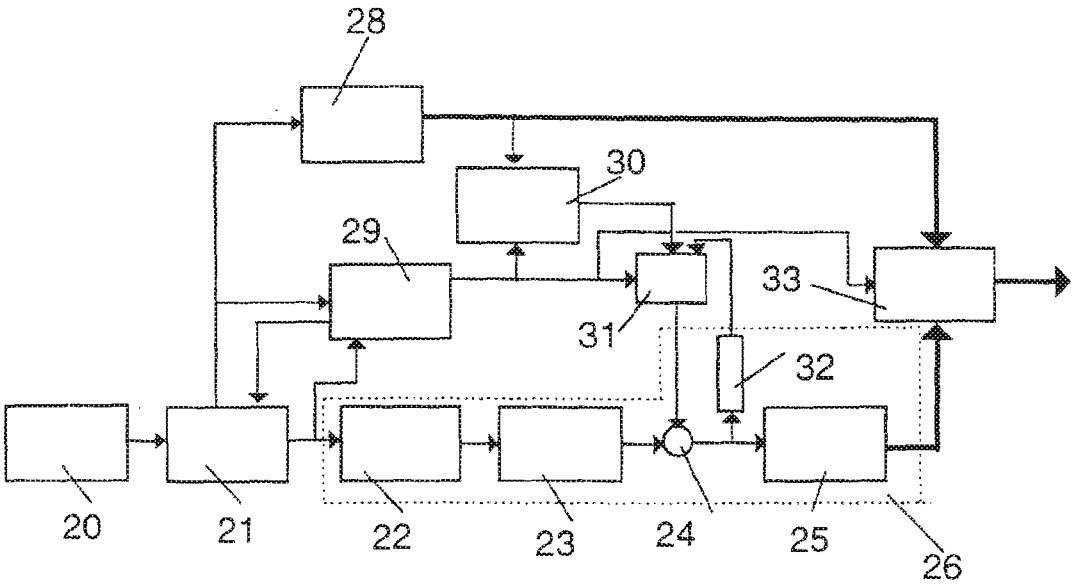
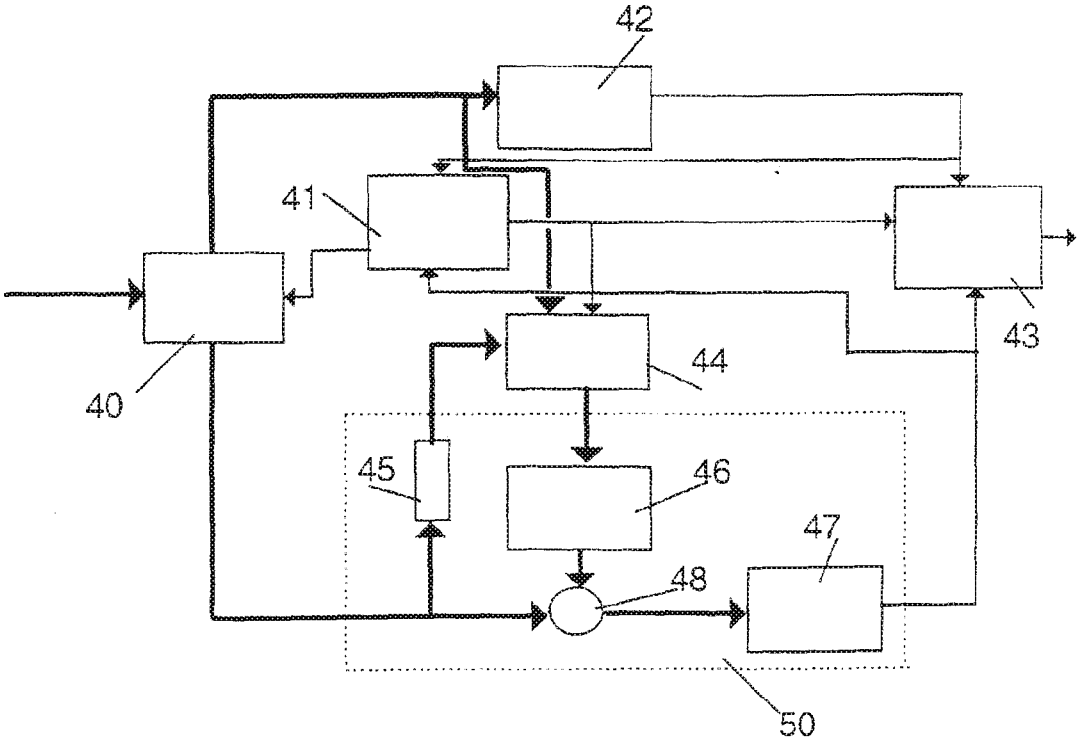


FIG.5



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(21) Application number: **92101190.4**

(22) Date of filing: **24.01.1992**

(54) **System for transmitting and receiving aural information and modulated data**

Einrichtung zum Senden und Empfangen von Audiosignalen und modulierten Daten

Système d'émission et de réception de signaux audio et de données modulées

(84) Designated Contracting States:
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GB-A- 2 067 877
US-A- 4 805 208
US-A- 4 876 696

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Description

[0001] This invention relates to an installation for transmitting modulated data and aural information and to a receiver for responding to transmitted aural information and modulated data, where the information is labelled to represent aural information or modulated data and, if modulated data, to represent the characteristics of such modulated data and whether the aural information has been transformed into digital format and the modulated data has been processed.

[0002] From US-A-4,805,208 a bit compression system for a telephone modem utilising differential phase shift modulation of a low-frequency tone carrier to transmit dibit or tribit values is known. The modem compression system tribit extracts the dibit or values from digital samples of the tone carrier and transmits assembled data bits in a data-stream containing solely the data bits encoded by the modem. At the receiving end, a modem decompressor reconstructs the digitised samples of the tone carrier using the dibit or tribit values.

[0003] US-A-4,876,696 discloses a transmission system for transmitting modem signals, or multi-frequency signals together with speech signals over the same digital transmission line. The system includes a transmitter which has a first coder that efficiently encodes a speech signal to produce a first coded output, a detector for detecting a multi-frequency signal or modem signal, a second encoder which produces a second coded output from the multi-frequency signal or modem signal, and a selector for selecting either the first or second coded output in response to the output of the detector. The systems also includes a receiver which has a separator for separating the received signal into the first and second coded outputs, a first decoder for decoding the first coded output and a second decoder for decoding the second coded output.

[0004] GB-A-2,067,877 shows a digital telephone subscriber station in a digital telecommunications network having analogue facsimile transmission device connected via a digital modem to a multiplexer/demultiplexer for combining or separating transmitted or received subsidiary channels. One of the two subsidiary channels carries telephone signals and the other carries facsimile transmission signals.

[0005] There is an ever increasing use of transmission lines for the transmission and reception of information in various forms. Transmission lines have been used to transmit aural information (such as voice or music) for many years. Transmission lines have more recently been used to transmit and receive modulated data such as modem data and facsimile images.

[0006] With the proliferation of the different kinds of information transmitted and received through the transmission lines, it has become progressively difficult to process this information. For instance, apparatus has had to be provided for communicating with the information sources to determine the particular type of information, such as aural information or modulated data, which is being transmitted. This has interrupted the transmission of information such as aural information or modulated data through the transmission lines.

[0007] Another difficulty which is progressively been encountered is that the communication to determine the type of information being transmitted has required that the different types of information (such as aural information and modulated data) be transmit on different lines. This has resulted in the duplication of charges for transmitting the different types of information between a transmitting location and a receiving location.

[0008] It is the object of the invention to provide an installation for transmitting modulated data and aural information and a receiver for responding to such type of signals in which the aural information and modulated data are transmitted without any communication between the transceiver system and the source of the aural information or the modulated data to interrupt the transmission of the aural information or modulated data.

[0009] This object is attained by the features of claim 1 and 9, respectively.

[0010] By this invention, an installation is provided which overcomes the inadequacies specified above. The transmitter process for the transmission of different types of information, such as aural information (voice or music), which may be made through a single transmission line. The receiver also determines, on a transparent basis, the particular type of information being transmitted through the line at any instant and provides for a processing of this information in accordance with the type of information (aural information or modulated data) being processed. The system in total is transparent, because it provides this determination transmission without interrupting the transmission of the information from the information sources.

[0011] In one embodiment of the invention, aural information (such as voice or music) and modulated data (such as the end of the new introductory portion of the specification) as facsimile or modem) information are converted at a transmitter from analog to digital form. The modulated data has an individual one of a plurality of different baud rates. A controller separately identifies the digitized aural information and modulated data and, if modulated data, identifies the baud rate of such modulated data. The aural information is separately transformed (as by digital signal processing). For modulated data, the information is separately processed in accordance with the different baud rates.

[0012] The individual ones of encoded aural information and modulated data are then introduced to a common line for packetizing. The beginning of each packet is labelled to identify whether the packet contains aural information (such as music or voice) or modulated data (such as modem or facsimile information) and, if modulated data, the particular baud rate of such information. An individual code identifies the end of each packet. The packetized information is then multiplexed in a common

bus with other packetized aural information and modulated data.

[0013] At a receiver connected to the common bus, the multiplexed information is separated into the different packets. The packetized information representing individual ones of aural information (such as music or voice) and modulated data (such as modem or facsimile information) is separated, in accordance with the packet labels, into aural and modulated data lines and, if modulated data, is introduced to an individual one of different modulators each operative at an individual one of the different baud rates. The aural information is then transformed substantially to its original form at the transmitter and the facsimile information is separately processed in accordance with its baud rate.

[0014] In the drawings:

Figure 1 is a diagram schematically illustrating a system for processing information such as aural information and modulated data and schematically illustrating where the sub-systems of this invention fit in such a system;

Figure 2 is a block diagram schematically illustrating the construction of an embodiment of a transmitter included in the sub-system of this invention for transmitting different types of information, such as aural information and modulated data, through a common transmission line;

Figure 3 is a block diagram schematically illustrating in further detail the construction of equipment included in the embodiment of Figure 2 for processing modulated data;

Figure 4 is a schematic view of a packet of information transmitted through the common transmission line by the sub-system shown in Figures 2 and 3; and

Figure 5 is a block diagram schematically illustrating the construction of an embodiment of a receiver which is included in the sub-system of this invention and which is operative upon the signals passing through the common transmission line to recover the different types of information such as aural information and modulated data such as facsimile.

[0015] Figure 1 is a block diagram schematically illustrating a system for processing information such as aural information and modulated data and schematically illustrating where the sub-systems of this invention fit in such a system. In the system shown in Figure 1, aural information (such as voice or music) in analog form (schematically illustrated at 100) is introduced from a source of aural information 102 (such as a telephone) to an aural/modulated data module 104 included in the sub-system of this invention. Information on a sheet of paper 106 is processed into digital form (schematically illustrated at 108) as by a facsimile machine 110. A modem 112 in the facsimile machine 110 converts the digital information 108 to an analog form 114 for introduction to the aural/modulated data module 104. Although facsimile information is shown specifically in Figure 1, the data information may be any type of modulated data as shown at 110 and 128 including facsimile information, modulated synchronous data, modulated asynchronous data and modulated data from local area networks. Furthermore, although the sources 102, 110 and 128 are shown separately in Figure 1, it will be appreciated that aural information (such as voice or music) and modulated data (such as modem or facsimile) may be obtained from a single source introduced to the aural/modulated data module 104 over a common line.

[0016] The aural/modulated data module 104 converts the analog information (such as voice, music, modem and facsimile) into a digital form schematically illustrated at 116. A packetizer 118 then produces packets 120 of the digital information. The packets 120'of the digital information are introduced to a multiplexer 122 which also receives packets of information from other packetizers, (e.g. packetizer 124) as from other sources 125 of data or alternatively from a digitized aural source. A modem 126 receives the information from another source such as a personal computer 126 and introduces such information to the module 104 for processing. It will be appreciated that the personal computer 126 is shown only schematically and that the modem 128 may receive digital information from a number of different types of sources such as a data terminal, a data multiplexer or a local area network. For example, the information introduced to the modem 128 may be digitized aural information, demodulated facsimile information, synchronous data, asynchronous data and data from local area networks.

[0017] In one embodiment of the invention, a transmitter system generally indicated at 10 (Figure 2) is provided. The system includes a source 12 of a first type of information such as voice or music and a source 14 of a second type of information such as facsimile or modem. The information from the sources 12 and 14 is introduced to a codec 16 which may be constructed in a manner well known in the art. Although the sources 12 and 14 are shown separately, it will be appreciated that information such as aural information and modulated data may be obtained from a single source introduced to the codec 16 over a common line.

[0018] The codec 16 converts analog information from the sources 12 and 14 to digital information representative of such analog information. The digitized information then passes through a switch 18 to a discriminator 20. It will be appreciated that the analog information may first pass through the switch and then be converted to digital information without departing from the scope of the invention.

[0019] The discriminator 20 operates to identify different types of information such as aural information and modulated data. For example, one way of distinguishing between aural information such as voice and modulated data such as facsimile is on the basis of variations in the

frequency of the signals representing the aural information. For example, voice information has a variable frequency (such as between 300 hertz and 2000 hertz) dependent upon the pitch of the spoken word. The pitch of a person's voice varies considerably even in the spoken word depending upon such factors as the speaker's emotions. On the other hand, facsimile information is provided at one of a plurality of constant baud rates.

[0020] Signals pass from the discriminator 20 to the switch 18 (Figure 2) to direct the switch to pass the signals coming in to the switch either to a transformer 22 of aural information or to demodulator equipment 24 depending upon whether the in-coming signals have a variable frequency or a constant frequency. The transformer 22 transforms the aural signals (such as by digital signal processing) in a manner well known in the art.

[0021] Although the modulated data signals have a constant baud rate, this baud rate may be different for different types of modulators such as those used in facsimile equipment. For example, a first type of modulator may provide binary bits at a rate of ninety six hundred per second (9600/sec.) or at a baud rate of twenty four hundred (2400/sec.), assuming four (4) bits in each symbol. Alternatively, the first type of modulator may provide binary bits at a rate of seventy two hundred per second (7200/sec.) or twenty four hundred baud (2400/sec), assuming three (3) bits per symbol. A second type of modulator may provide binary bits at a rate of forty eight hundred per second (4800/sec.) or sixteen hundred baud (1600/sec.) with three (3) bits per symbol. Alternatively, the second modulator may provide binary bits at a rate of twenty four hundred per second (2400/sec.) or twelve hundred baud (1200/sec.) with two (2) bits per symbol. A third type of modulator may provide bits at a rate of three hundred per second (300/sec.) or three hundred baud (300/sec.) with one (1) bit per symbol.

[0022] In addition to determining on the basis of a constant frequency that the information is from, for example, facsimile equipment, the discriminator 20 (Figure 2) determines the baud rate of the facsimile signals, partly on the basis of bandwidth, to identify the particular type of modulator being used by the facsimile. For example, since the bandwidth of the third modulator (300 binary bits/second) is relatively narrow, the discriminator is able to identify data at 300 binary bits/second on the basis of this narrow bandwidth. The discriminator 20 is able to identify data at the other baud rates on the basis of encodings which are included in such facsimile data and which identify the different baud rates. These encodings are known in the art as "P2" or period two, an alternating pattern. The discriminator 20 then activates the demodulator 24 to provide signals at the proper rate. The demodulator 24 then processes the signals in accordance with the identification from the discriminator 20.

[0023] Figure 3 illustrates in additional detail the relationship between the discriminator 20 and the demodulator 24 (shown in broken lines in Figure 2). As will be seen, the demodulator 24 includes three (3) demodulators 26, 28 and 30. The demodulator 26 provides facsimile signals at baud rates of 2400 symbols/second (but with alternative bit rates of 9600/sec. and 7200/sec). The demodulator 28 alternatively provides facsimile signals at baud rates of 1600 symbols/sec. (4800 bits per second) and 1200 symbols/sec. (2400 bits per second). The demodulator 30 provides facsimile signals at a baud rate of 300 symbols/sec. (with a bit rate of 300/sec.). Although the demodulators 26, 28 and 30 are shown in Figure 3 as separate units, different demodulator functions such as those performed by the demodulators 26, 28 and 30 may be performed in a single unit.

[0024] The discriminator 20 selectively activates individual ones of the demodulators 26, 28 and 30 in accordance with the bandwidth of the data and the information represented by the encoding P2. For example, the demodulator 30 has a narrow bandwidth. When the discriminator 20 detects a narrow bandwidth, it activates only the demodulator 30. When the demodulator 26 is activated in accordance with the encoding (or preamble) P2, the discriminator 20 selects the baud rate of 2400/sec. on the basis of either 4 bits per baud or 3 bits per baud. When the demodulator 24 is activated in accordance with the encoding (or preamble) P2, the discriminator 20 selects between the baud rates of 1600/sec. and 1200/sec. The encoding (or preamble) P2 is well known in the art.

[0025] The demodulator 24 also provides another important function. It converts the 8 kilohertz sample rate of the codec to a sample rate which constitutes an integral multiple of each of the baud rates from the demodulators 26, 28 and 30. For example, the demodulator 26 operates at a sample rate of 7.2 kilohertz; the demodulator 28 operates at a sample rate of 4.8 kilohertz; and the demodulator 30 operates at a sample rate of 2.4 kilohertz. The sampling rate of various types of demodulators is between 2.4 and 7.2 kilohertz.

[0026] The discriminator 20 is able to provide the discrimination discussed above in a minimal period of time. For example, the discriminator 20 is able to provide this discrimination in a time no greater than one hundred (100) milliseconds. In this way, the discriminator 20 does not impede the transmission of information, whether aural information or modulated data, between the transmitter 10 and the receiver 60 shown in Figure 5. Furthermore, the discriminator 20, the transformer 22 of aural information and the demodulator 24 operate without interrupting the operation of the source 12 of aural information and the source 14 of modulated data.

[0027] The signals from the transformer 22 of aural information and the demodulator 24 pass through a summer 32 (Figure 2) and a common line 34 to a packetizer 36. The packetizer 36 corresponds to the packetizer 118 in Figure 1. The summer 34, the discriminator 20, the transformer 22 of aural information, the demod-

ulator 24 and the codec 16 may be considered to be included in the aural/modulated data module 104 of Figure 1 as indicated in broken lines in Figure 2.

[0028] The packetizer 36 converts the signals into time-spaced packets of information. The packetizing of information is well known in the art. A typical packet is generally indicated at 40 in Figure 4. As shown, a packet 40 consists of a sequence of bytes each formed from a plurality of bits such as eight (8) bits. Each byte is shown schematically in Figure 4 by a different horizontal area. Bytes 40a, 40b and 40c are illustratively shown schematically in Figure 4. The bits in each byte are passed sequentially by the packetizer 36 and each successive byte is then passed sequentially. For example, the bits in byte 40a are passed sequentially, then the bits in byte 40b and thereafter the bits in byte 40c.

[0029] The beginning of each packet 40 of information is defined by a label 42 (shown schematically as a horizontal area in Figure 4). The label 42 is provided with a binary code to identify whether the information in the packet 40 is aural information or modulated data and, if modulated data, to identify the particular modulator used and the particular one of the alternatives in the particular modulator if the modulator has two (2) alternatives. The packet 40 has a code 43 at the end to identify the end of the packet.

[0030] The packets of information from the packetizer 36 pass through a line 44 (Figure 2) to a multiplexer 46 corresponding to the multiplexer 122 in Figure 1. The multiplexer receives packets of signals through a line 48 from another source of information such as a source of data or of transformed aural information. The data may be demodulated facsimile, synchronous data, asynchronous data or data from a local area network. The multiplexer 46 sequentially passes signals to a transmission line 50 on a time-sharing basis from the lines 44 and 48. It will be appreciated that signals from a number of different information sources (whether aural information or modulated data) may be introduced in packets through lines (corresponding to the lines 44 and 48) to the multiplexer 46 for passage on a time-sharing basis through the transmission line 50.

[0031] Figure 5 illustrates a system, generally indicated at 60, for receiving, decoding and restoring the information such as aural information (e.g. voice or music) and modulated data (e.g. facsimile or modem). The system 60 receives the packets, including the packets 40 of information passing through the transmission line 50 and includes a stage 62 for channeling the different packets 40 to different routes corresponding to the lines 44 and 48 in Figure 2. The stage 62 may be constructed in a conventional manner. The signals packetized by the packetizer 36 in Figure 2 pass from the de-multiplexer 62 through a line 63 to a depacketizer 64 which detects the label 42 in the packet 40 (Figure 4) to identify whether the information in the packet is aural information or modulated data and, if modulated data such as facsimile, to identify the baud rate. The signals from the de-multiplexer 62 also pass through a line 65 to a depacketizer (not shown) which depacketizes the packets from the packetizer 124 in Figure 1.

[0032] The results of the label detection by the depacketizer 64 are introduced to a controller 66 which operates to activate a transformer of aural information 68 if the information in the packet 40 is aural information. The transformer 68 then transforms the information in the packet 40 (as by digital signal processing). The construction of the transformer 68 is well known in the art. If the information in the packet 40 is demodulated data, the controller 66 activates a modulator 70 which processes the demodulated data. The modulator 70 provides this processing by interpreting the modem type contained in the packet head and by then processing the demodulated data at the particular baud rate and bit rate in the packet 40 in accordance with such interpretation.

[0033] The signals from the transformer 68 and the modulator 70 are introduced to a summer 71 which introduces the signals to a common line 72. The signals then pass to a codec 74 which may be constructed in a conventional manner. The codec 74 converts the signals from digital to analog form to obtain a recovery of the original information at the transmitter 10 (Figure 2). The transformer aural information 68, the controller 66, the modulator 70, the summer 71 and the codec 74 may be included in the aural/modulated data module 104 of Figure 1 as indicated in broken lines in Figure 5.

[0034] The apparatus described above has certain important advantages. It detects whether information being transmitted is aural information (such as voice or music) or modulated data (such as facsimile or modem) and, if modulated data, the particular baud and bit rate of the modulated data. The apparatus then separately transforms (as by digital signal processing) the aural information and separately processes the modulated data in accordance with the baud rate of the modulated data. The apparatus provides such detection and processing without interrupting the generation of the aural information and/or modulated data by the sources for such information. The apparatus is further advantageous in that it provides for the transmission of the transformed aural information and the processed modulated data through a single transmission line.

[0035] The apparatus constituting this invention is also advantageous in that it converts the modulated data to rates constituting an integral multiple of the different baud rates, constituting an integral multiple of the different baud rates. Another significant advantage of the apparatus constituting this invention is that it provides packets of the transmitted information and labels each packet to identify whether the packet contains transformed aural information (such as voice or music) or processed modulated data (such as modem or facsimile) and, if processed modulated data, the baud and binary bit rate of such processed modulated data.

[0036] The receiver of this invention also has certain

important advantages. For example, it receives the packetized information on the single transmission line and identifies, from the label in each packet, whether the information in the packet is digitized aural information or modulated data and, if modulated data, the particular baud and bit rate of such modulated data. The apparatus is further advantageous in separately transforming (as by digital signal processing) the aural information in accordance with such identification and in processing the demodulated data in accordance with the baud and bit rate of such information. The apparatus is also advantageous in that it restores the processed modulated data to its original form and the transformed aural information to substantially its original form.

[0037] Although this invention has been disclosed and illustrated with reference to particular embodiments, the principles involved are susceptible for use in numerous other embodiments which will be apparent to persons skilled in the art. The invention is, therefore, to be limited only as indicated by the scope of the appended claims.

Claims

1. An installation for transmitting modulated data information and aural information included in a signal introduced thereto,
characterized by:

controller means (20) responsive to the modulated data information and to the aural information for identifying whether the introduced signal includes aural information or modulated data information and, if modulated data information, the characteristics of such modulated data information;

first means (22) operatively coupled to the controller means (20) for transforming the aural information;

second means (24) operatively coupled to the controller means (20) for processing the modulated data information in accordance with its characteristics; and

packetizer means (36)

for packetizing individual ones of the transformed aural information and the processed modulated data information; and

for labelling the resulting packetized information to identify whether such packetized information is aural information or modulated data information and, if modulated data information, the characteristics of such modulated data information.

2. An installation as set forth in claim 1, wherein:

the modulated data information is provided by a data source (14);

the aural information is provided by an aural information source (12); and

the controller means (20) is responsive to the modulated data information and to the aural information, without interrupting the operation of the data source (14) for providing the modulated data information and of the aural information source (12) for providing the aural information.

3. An installation as set forth in claim 1 or 2, wherein the controller means (20) is operative to identify the aural information by a variable frequency and to identify the modulated data information by one of a plurality of constant frequencies and is operative to identify the characteristics of the modulated data information.

4. An installation as set forth in claim 1, further comprising a common line (34,44,50) for transmitting the transformed aural information and the processed modulated data information, wherein:

the packetizer means (36) is connected to a part (34) of the common line for receiving unpacketized and unlabelled transformed aural information and processed modulated data information; and

the packetizer means (36) is connected to another part (44) of the common line for transmitting packetized and labelled individual ones of the transformed aural information and the processed modulated data information.

5. An installation as set forth in claim 1, wherein:

the packetizer means (36) includes first packetizer means (118) for producing time-spaced packets of the transformed aural information and the processed modulated data information,

the installation further comprising:

second packetizer means (124) for producing time-spaced packets of aural information or modulated data information provided by another source (125); and

multiplexer means (122) operative to multiplex between the time-spaced packets

from the first packetizer means (118) and the second packetizer means (124).

6. An installation as set forth in any of claims 1-5, wherein:

the modulated data information includes facsimile information, the facsimile information having different baud and bit rates;

the controller means (20) is operative to identify the facsimile information and the different baud and bit rates of such facsimile information; and

the packetizer means (36) is operative to label the facsimile information and the baud and bit rates of facsimile information.

7. A receiver for receiving aural information and modulated data information transmitted on a common line where the information is in packets, where the information is labelled to indicate the presence of aural information or modulated data information and, if modulated data information, to indicate the presence of the characteristics of such modulated data information, and where the aural information has been transformed and the modulated data information has been processed,
characterized by:

first means (64) for depacketizing the received transformed aural information and the received processed modulated data information;

second means (66) for detecting the labelling of the depacketized information to identify whether the depacketized information is aural information or modulated data information and, if modulated data information, the characteristics of such modulated data information,

third means (68) for operating upon the transformed aural information to recover the aural information before transformation; and

fourth means (70) for operating upon the processed modulated data information to recover the modulated data information before processing,

wherein the second means (66) activates the third means (68) and the fourth means (70), in accordance with the detection of the labelling to obtain recovery of the aural information and the modulated data information.

8. A receiver as set forth in claim 7, wherein the aural information and the modulated data information are converted from an analogue form to a digital form before transmission to the receiver,
the receiver further comprising fifth means (74) for restoring the aural information and the modulated data information from the digital form to the analogue form.

9. A receiver as set forth in claim 8, wherein:

the modulated data information includes facsimile information, the facsimile information having different baud and bit rates;

the labelling identifies the different baud and bit rates of the facsimile information; and

the fourth means (70) is responsive to the different baud and bit rates of the facsimile information to recover the facsimile information.

10. A receiver as set forth in claim 9, wherein:

the aural and the facsimile information are converted from an analogue form to a digital from before transmission; and

the fifth means (74) restores the recovered aural and facsimile information from the digital form to the analogue form.

Patentansprüche

1. Einrichtung zum Übertragen von modulierten Dateninformationen und Toninformationen, die in einem in sie eingeleiteten Signal enthalten sind,
gekennzeichnet durch:
eine Steuereinrichtung (20), die auf die modulierten Dateninformationen und die Toninformationen anspricht und bestimmt, ob das eingeleitete Signal Toninformationen oder modulierte Dateninformationen enthält, und, im Fall von Dateninformationen, die Eigenschaften dieser modulierten Dateninformationen bestimmt:

eine erste Einrichtung (22), die funktionell mit der Steuereinrichtung (20) verbunden ist, um die Toninformationen umzuwandeln;
eine zweite Einrichtung (24), die funktionell mit der Steuereinrichtung (20) verbunden ist, um die modulierten Dateninformationen entsprechend ihren Eigenschaften zu verarbeiten; und
eine Paketiereinrichtung (36), die:

einzelne der umgewandelten Toninformationen und der verarbeiteten modulierten Dateninformationen paketiert; und
die entstehenden paketierten Informatio-

nen etikettiert, um anzugeben, ob es sich bei diesen paketierten Informationen um Toninformationen oder modulierte Dateninformationen handelt, und, im Fall von modulierten Dateninformationen, die Eigenschaften dieser modulierten Dateninformationen anzugeben.

2. Einrichtung nach Anspruch 1, wobei:

die modulierten Dateninformationen durch eine Datenquelle (14) bereitgestellt werden;

die Toninformationen durch eine Toninformationsquelle (12) bereitgestellt werden; und

die Steuereinrichtung (20) auf die modulierten Dateninformationen und die Toninformationen anspricht, ohne die Funktion der Datenquelle (14), die die modulierten Dateninformationen bereitstellt, und der Toninformationsquelle (12), die die Toninformationen bereitstellt, zu unterbrechen.

3. Einrichtung nach Anspruch 1 oder 2, wobei die Steuereinrichtung (20) die Toninformationen anhand einer veränderlichen Frequenz identifiziert und die modulierten Dateninformationen anhand einer Vielzahl konstanter Frequenzen identifiziert und die Eigenschaften der modulierten Dateninformationen identifiziert.

4. Einrichtung nach Anspruch 1, die des Weiteren eine gemeinsame Leitung (34, 44, 50) zum Senden der umgewandelten Toninformationen und der verarbeiteten modulierten Dateninformationen umfasst, wobei:

die Paketiereinrichtung (36) mit einem Teil (34) der gemeinsamen Leitung verbunden ist, um nicht paketierte und nicht etikettierte umgewandelte Toninformationen und verarbeitete modulierte Dateninformationen zu empfangen; und

die Paketiereinrichtung (36) mit einem anderen Teil (44) der gemeinsamen Leitung verbunden ist, um einzelne paketierte und etikettierte der umgewandelten Toninformationen und der verarbeiteten modulierten Dateninformationen zu senden.

5. Einrichtung nach Anspruch 1, wobei:
die Paketiereinrichtung (36) eine erste Paketiereinrichtung (118) enthält, die zeitlich beabstandete Pakete der umgewandelten Toninformationen und der verarbeiteten modulierten Dateninformationen erzeugt,
wobei die Einrichtung des Weiteren umfasst:

eine zweite Paketiereinrichtung (124), die zeitlich beabstandete Pakete von Toninformationen oder modulierten Dateninformationen erzeugt, die von einer anderen Quelle (125) bereitgestellt werden; und

eine Multiplexiereinrichtung (122), die zwischen den zeitlich beabstandeten Paketen von der ersten Paketiereinrichtung (118) und der zweiten Paketiereinrichtung (124) multiplexiert.

6. Einrichtung nach einem der Ansprüche 1 - 5, wobei:

die modulierten Dateninformationen Fax-Informationen enthalten, wobei die Fax-informationen unterschiedliche Baud- und Bit-Raten haben;

die Steuereinrichtung (20), die Fax-Informationen und die unterschiedlichen Baud- und Bit-Raten dieser Fax-Informationen identifiziert; und

die Paketiereinrichtung (36), die Fax-Informationen sowie die Baud- und Bit-Raten der Fax-Informationen etikettiert.

7. Empfänger zum Empfangen von Toninformationen und modulierten Dateninformationen, die auf einer gemeinsamen Leitung gesendet werden, wobei die Informationen in Paketen vorliegen, und wobei die Informationen etikettiert sind, um das Vorhandensein von Toninformationen oder modulierten Dateninformationen anzuzeigen, und im Fall von modulierten Dateninformationen, das Vorhandensein der Eigenschaften dieser modulierter Dateninformationen anzuzeigen, und wobei die Toninformationen umgewandelt worden sind und die modulierten Dateninformationen verarbeitet worden sind,
gekennzeichnet durch:

eine erste Einrichtung (64), die die empfangenen umgewandelten Toninformationen und die empfangenen verarbeiteten modulierten Dateninformationen entpaketiert;

eine zweite Einrichtung (66), die die Etikettierung der entpaketierten Informationen erfasst, um zu bestimmen, ob es sich bei den entpaketierten Informationen um Toninformationen oder modulierte Dateninformationen handelt, und im Fall von modulierten Dateninformationen, die Eigenschaften dieser modulierten Dateninformationen zu bestimmen,

eine dritte Einrichtung (68), die auf die umgewandelten Toninformationen einwirkt, um die Toninformationen vor der Umwandlung wieder-

zugewinnen; und

eine vierte Einrichtung (70), die auf die verarbeiteten modulierten Dateninformationen einwirkt, um die modulierten Dateninformationen vor der Verarbeitung wiederzugewinnen,

wobei die zweite Einrichtung (66) die dritte Einrichtung (68) und die vierte Einrichtung (70) entsprechend der Erfassung der Etikettierung aktiviert, um die Wiedergewinnung der Toninformationen und der modulierten Dateninformationen auszuführen.

8. Empfänger nach Anspruch 7, wobei die Toninformationen und die modulierten Dateninformationen vor dem Senden zu dem Empfänger aus einer analogen Form in eine digitale Form umgewandelt werden,
der Empfänger des Weiteren eine fünfte Einrichtung (74) umfasst, die die Toninformationen und die modulierten Dateninformationen aus der digitalen Form wieder in die analoge Form bringt.

9. Empfänger nach Anspruch 8, wobei:

die modulierten Dateninformationen Fax-Informationen enthalten und die Fax-Informationen unterschiedliche Baud- und Bit-Raten haben;

die Etikettierung die Baud- und Bit-Raten der Fax-Informationen angibt; und

die vierte Einrichtung (70) auf die unterschiedlichen Baud- und Bitraten der Fax-Informationen anspricht, um die Fax-Informationen wiederzugewinnen.

10. Empfänger nach Anspruch 9, wobei:

die Ton- und die Fax-Informationen vor dem Senden aus einer analogen Form in eine digitale Form umgewandelt werden; und

die fünfte Einrichtung (74) die wiedergewonnenen Ton- und Fax-Informationen aus der digitalen Form wieder in die analoge Form bringt.

Revendications

1. Système pour transmettre des données modulées et des informations audio contenues dans un signal introduit dans le système,
caractérisé par :

un moyen contrôleur (20) sensible aux données modulées et aux informations audio pour identifier si le signal introduit comprend des informations audio ou des données modulées et, si ce sont des données modulées, les caractéristiques de telles données modulées,
un premier moyen (22) raccordé de façon opérationnelle au moyen contrôleur (20) pour transformer les informations audio,
un second moyen (24) raccordé de façon opérationnelle au moyen contrôleur (20) pour traiter les données modulées conformément à leurs caractéristiques et
un moyen assembleur de paquets (36)

pour mettre en paquets les informations individualisées résultant des informations audio transformées et des données modulées traitées et
pour étiqueter les informations assemblées résultantes pour identifier si de telles informations assemblées sont des informations audio ou des données modulées et, si ce sont des données modulées, les caractéristiques de telles données modulées.

2. Système selon la revendication 1 dans lequel :

les données modulées sont fournies par une source de données (14),

les informations audio sont fournies par une source d'informations audio (12) et

le moyen contrôleur (20) est sensible aux données modulées et aux informations audio sans interrompre le fonctionnement de la source de données (14) fournissant les données modulées et de la source d'informations audio (12) fournissant les informations audio.

3. Système selon la revendication 1 ou la revendication 2 dans lequel le moyen contrôleur (20) fonctionne pour identifier les informations audio grâce à une fréquence variable et pour identifier les données modulées grâce à l'une de leurs multiples fréquences constantes et fonctionne pour identifier les caractéristiques des données modulées.

4. Système selon la revendication 1, comprenant en outre une ligne commune (34, 44, 50) pour transmettre les informations audio transformées et les données modulées traitées, dans lequel :

le moyen assembleur de paquets (36) est raccordé à une partie (34) de la ligne commune pour recevoir des informations audio transformées et des données modulées traitées, non assemblées en paquets et non étiquetées et

le moyen assembleur de paquets (36) est raccordé à une autre partie (44) de la ligne commune pour transmettre des informations individualisées assemblées en paquets et étiquetées à partir des informations audio transformées et des données modulées traitées.

5. Système selon la revendication 1, dans lequel :

le moyen assembleur de paquets (36) comprend un premier moyen assembleur de paquets (118) pour produire des paquets espacés dans le temps à partir des informations audio transformées et des données modulées traitées,

le système comprenant en outre :

un second moyen assembleur de paquets (124) pour produire des paquets espacés dans le temps à partir d'informations audio ou de données modulées fournies par une autre source (125) et

un moyen multiplexeur (122) fonctionnant pour multiplexer entre les paquets espacés dans le temps provenant du premier moyen assembleur de paquets (118) et du second moyen assembleur de paquets (124).

6. Système selon l'une quelconque des revendications 1 à 5 dans lequel :

les données modulées comprennent des signaux de télécopie, les signaux de télécopie ayant différents débits en bauds et débits binaires,

le moyen contrôleur (20) fonctionne pour identifier les signaux de télécopie ainsi que les différents débits en bauds et débits binaires de tels signaux de télécopie et

le moyen assembleur de paquets (36) fonctionne pour étiqueter les signaux de télécopie ainsi que les débits en bauds et les débits binaires des signaux de télécopie.

7. Récepteur pour recevoir les informations audio et les données modulées transmises sur une ligne commune où les informations sont en paquets, où les informations sont étiquetées pour indiquer la présence d'informations audio ou de données modulées et, si ce sont des données modulées, pour indiquer la présence des caractéristiques de telles données modulées, et où les informations audio ont été transformées et où les données modulées ont été traitées,
caractérisé par :

un premier moyen (64) pour désassembler les informations audio transformées reçues et les données modulées traitées reçues,
un deuxième moyen (66) pour détecter l'étiquetage des informations désassemblées pour identifier si les informations désassemblées sont des informations audio ou des données modulées et, si ce sont des données modulées, les caractéristiques de telles données modulées,
un troisième moyen (68) pour opérer sur les informations audio transformées afin de rétablir les informations audio avant transformation et
un quatrième moyen (70) pour opérer sur les données modulées traitées afin de rétablir les données modulées avant traitement,

dans lequel le deuxième moyen (66) active le troisième moyen (68) et le quatrième moyen (70) conformément à la détection de l'étiquetage pour obtenir la récupération des informations audio et des données modulées.

8. Récepteur selon la revendication 7, dans lequel les informations audio et les données modulées passent par conversion d'une forme analogique à une forme numérique avant transmission au récepteur, le récepteur comprenant en outre un cinquième moyen (74) pour rétablir les informations audio et les données modulées de la forme numérique à la forme analogique.

9. Récepteur selon la revendication 8, dans lequel :

les données modulées comprennent des signaux de télécopie, les signaux de télécopie ayant des débits en bauds et des débits binaires différents,

l'étiquetage identifie les différents débits en bauds et débits binaires des signaux de télécopie et

le quatrième moyen (70) est sensible aux différents débits en bauds et

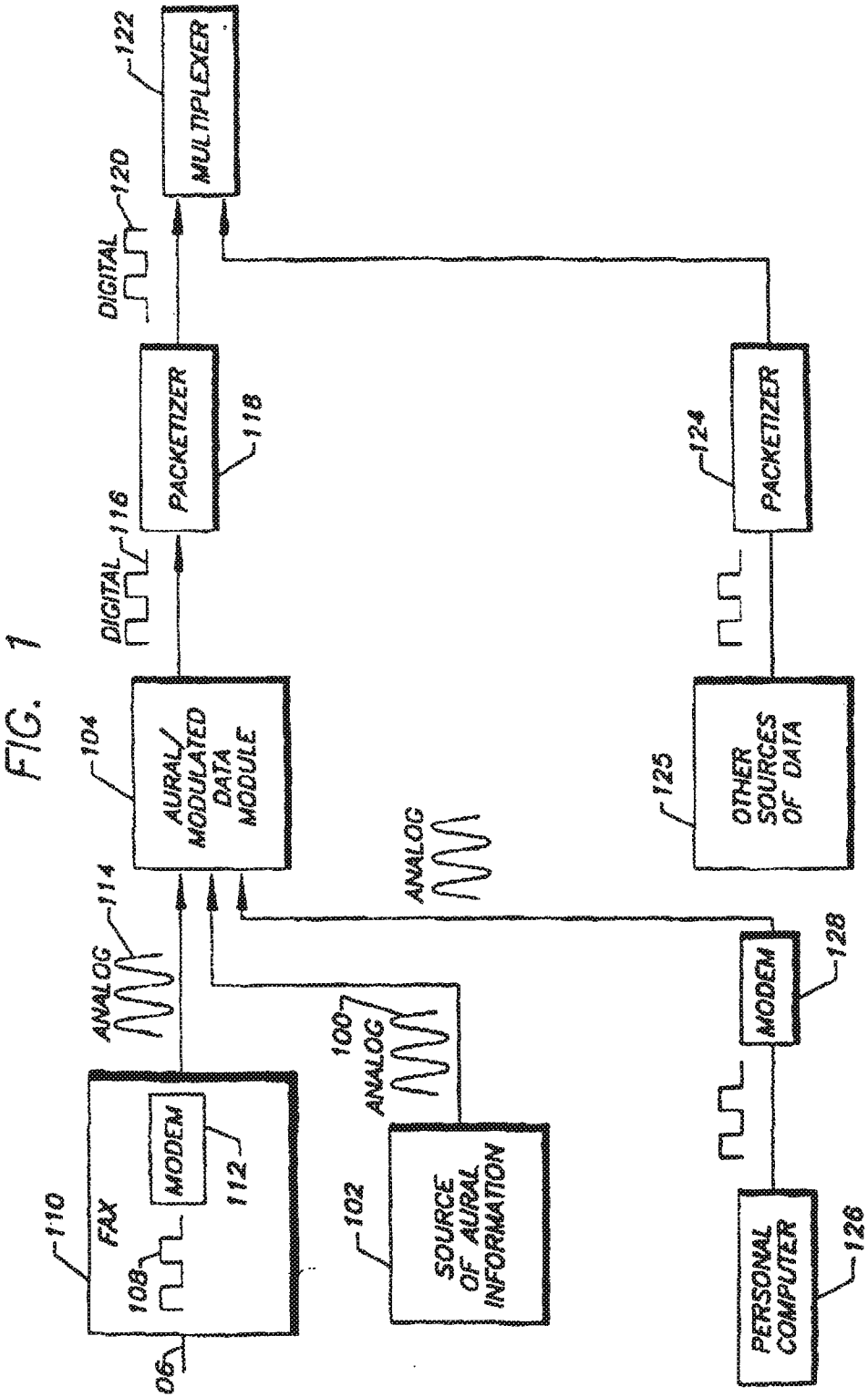
débits binaires des signaux de télécopie pour récupérer les signaux de télécopie.

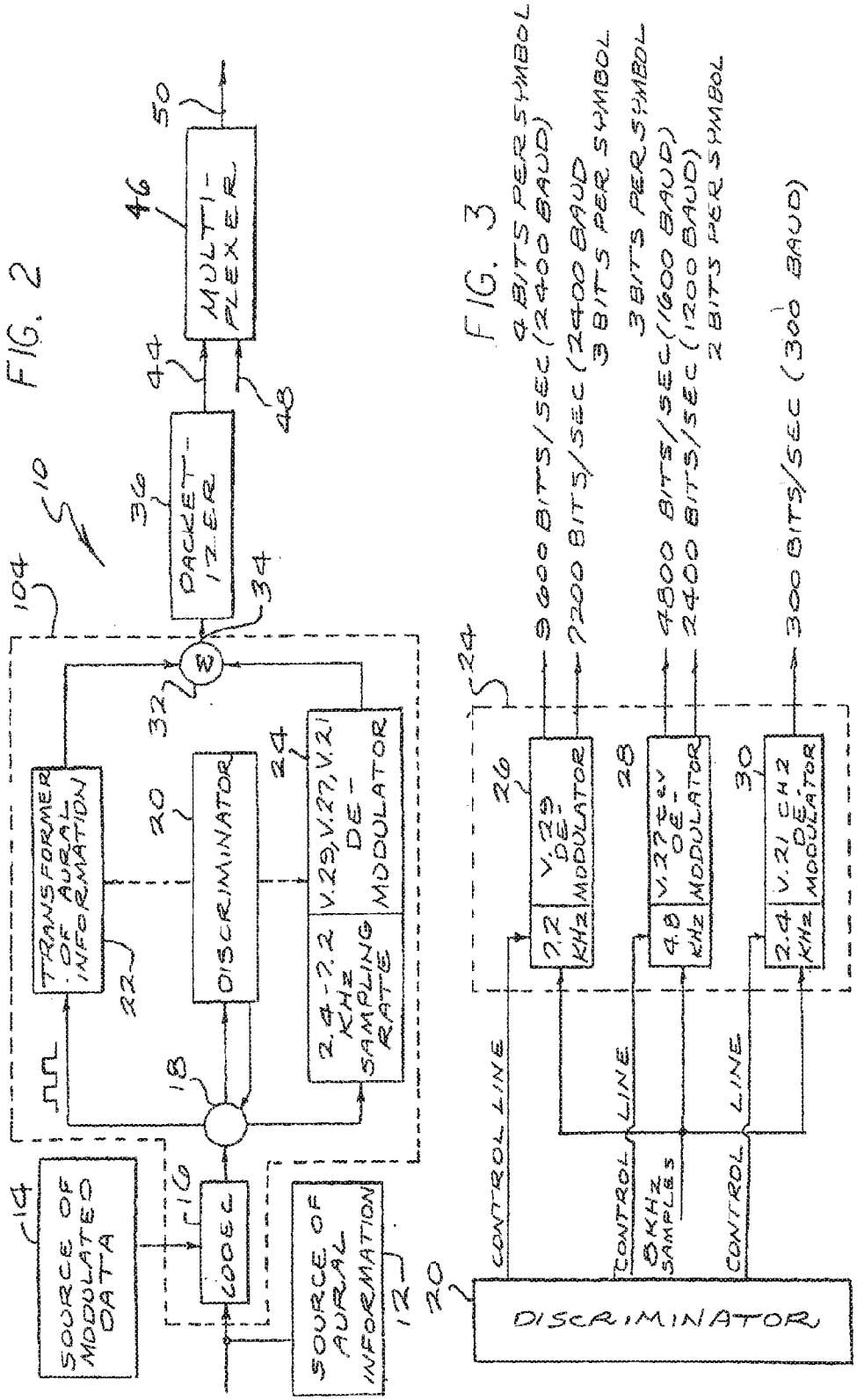
10. Récepteur selon la revendication 9, dans lequel :

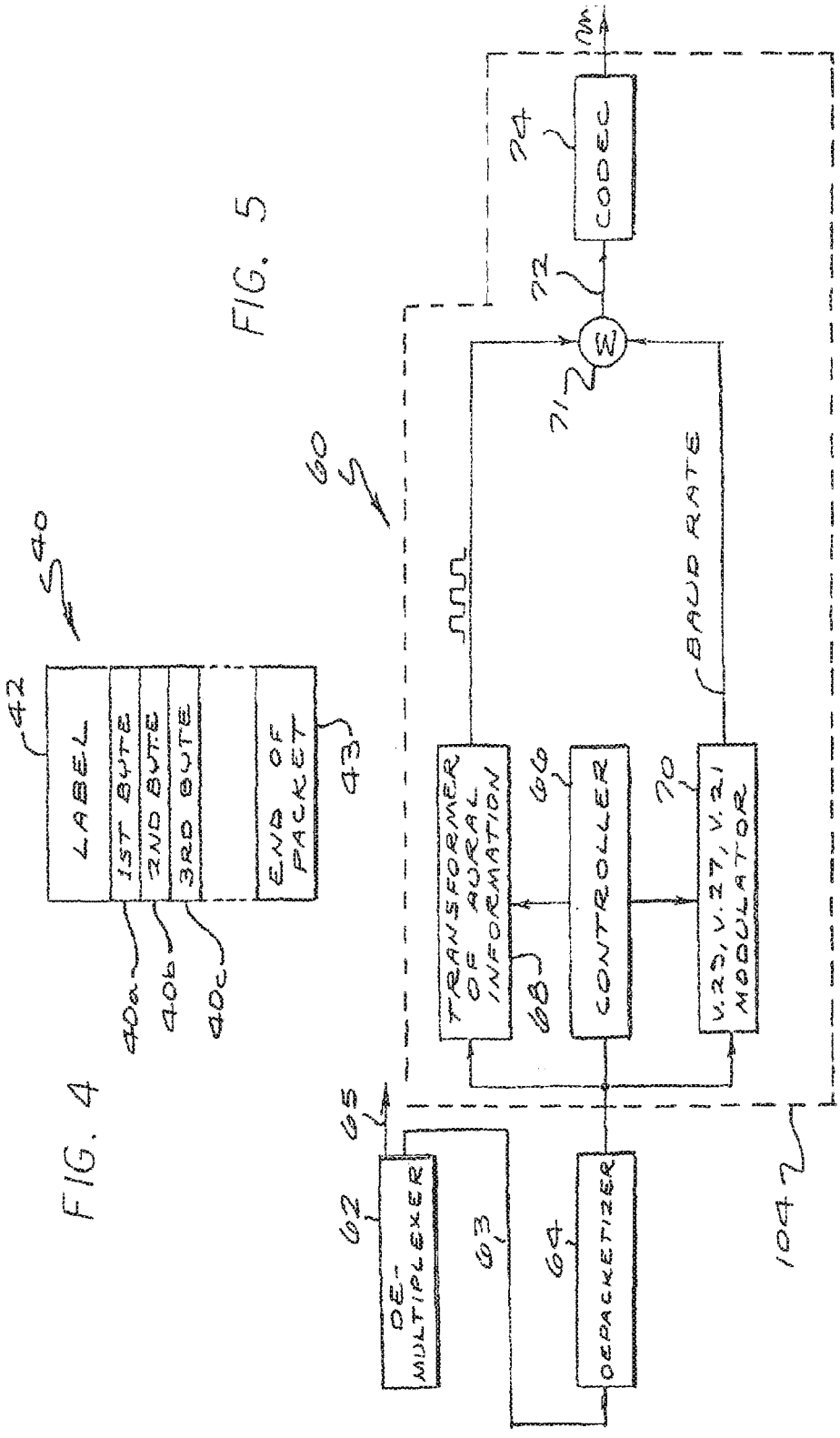
les informations audio et les signaux de télécopie passent par conversion d'une forme analogique à une forme numérique avant transmission et

le cinquième moyen (74) rétablit les informations audio et les signaux de télécopie récupérés de la forme numérique à la forme analogique.

FIG. 1






40
42
LABEL
1ST BYTE
2ND BYTE
3RD BYTE
END OF PACKET
43
40a
40b
40c
FIG. 4
60
TRANSFORMER OF AURAL INFORMATION
66
CONTROLLER
70
V.29, V.27, V.21 MODULATOR
BAUD RATE
68
71
72
CODEC
74
DE-MULTIPLEXER
62
63
64
DEPACKETIZER
65
104
FIG. 5

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(54) Multiresolution QAM system

Mehrfachauflösungs-QAM-System

Système MAQ à multi-résolution

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Description

[0001] The present invention relates to a communication system for transmission/reception of a digital signal through modulation of its carrier wave and demodulation of the modulated signal.

[0002] Digital communication systems have been used in various fields. Particularly, digital video signal transmission techniques have been improved remarkably.

[0003] Among them is a digital TV signal transmission method. So far, such digital TV signal transmission system are in particular use for e.g. transmission between TV stations. They will soon be utilized for terrestrial and/or satellite broadcast service in every country of the world.

[0004] The TV broadcast systems including HDTV, PCM music, FAX, and other information service are now demanded to increase desired data in quantity and quality for satisfying millions of sophisticated viewers. In particular, the data has to be increased in a given bandwidth of frequency allocated for TV broadcast service. The data to be transmitted is always abundant and provided as much as handled with up-to-date techniques of the time. It is ideal to modify or change the existing signal transmission system corresponding to an increase in the data amount with time.

[0005] However, the TV broadcast service is a public business and cannot go further without considering the interests and benefits of viewers. It is essential to have any new service appreciable with existing TV receivers and displays. More particularly, the compatibility of a system is much desired for providing both old and new services simultaneously or one new service which can be intercepted by either of the existing and advanced receivers.

[0006] It is understood that any new digital TV broadcast system to be introduced has to be arranged for data extension in order to respond to future demands and technological advantages and also, for compatible action to allow the existing receivers to receive transmissions.

[0007] The expansion capability and compatible performance of prior art digital TV system will be explained.

[0008] A digital satellite TV system is known in which NTSC TV signals compressed to an about 6 Mbps are multiplexed by time division modulation of 4 PSK and transmitted on 4 to 20 channels while HDTV signals are carried on a single channel. Another digital HDTV system is provided in which HDTV video data compressed to as small as 15 Mbps are transmitted on a 16 or 32 QAM signal through ground stations.

[0009] Such a known satellite system permits HDTV signals to be carried on one channel by a conventional manner, thus occupying a band of frequencies equivalent to same channels of NTSC signals. This causes the corresponding NTSC channels to be unavailable during transmission of the HDTV signal. Also, the compatibility between NTSC and HDTV receivers or displays is hardly concerned and data expansion capability needed for matching a future advanced mode is utterly disregarded.

[0010] Such a common terrestrial HDTV system offers an HDTV service on conventional 16 or 32 QAM signals without any modification. In any analogue TV broadcast service, there are developed a lot of signal attenuating or shadow regions within its service area due to structural obstacles, geographical inconveniences, or signal interference from a neighbor station. When the TV signal is an analogue form, it can be intercepted more or less at such signal attenuating regions although its reproduced picture is low in quality. If TV signal is a digital form, it can rarely be reproduced at an acceptable level within the regions. This disadvantage is critically hostile to the development of any digital TV system.

[0011] The article "Multi resolution Source and Channel Coding for Digital Broadcast of HDTV" G K.M.Uz et al from Signal Processing of HDTV,III edited H.Yasude et al 1992 Elsevier, discloses a 2 resolution HDTV signal modulated using a 64-QAM scheme.

[0012] EP-A-0,485,108 discloses a modulation scheme using constellation mapping to provide differing levels of error protection to the most important data elements.

[0013] EP-A-0,485,105 discloses a scheme for coding HDTV signals in which the television signal is divided into two data streams which are then mapped so as to provide different amounts of error protection.

[0014] EP-A-0 448 492 discloses a device for the transmission of digital data with at least two levels of protection and corresponding reception device. The transmission system using COFDM (Coding orthogonal Frequency Division Multiplex) techniques.

[0015] The present invention provides an OFDM (Orthogonal Frequency Division Multiplex) receiver as defined in the appended claim.

[0016] The present invention can thereby provide a communication system arranged for compatible use for both the existing NTSC and introducing HDTV broadcast services, particularly via satellite and also, for minimizing signal attenuating or shadow regions of its service area on the grounds.

[0017] A communication system incorporating an embodiment of the present invention intentionally varies signal points, which used to be disposed at uniform intervals, to perform the signal transmission/reception. For example, if applied to a QAM signal, the communication system comprises two major sections: a transmitter having a signal input circuit, a modulator circuit for producing m numbers of signal points, in a signal vector field through modulation of a plurality of out-of-phase carrier waves using an input signal supplied from the input circuit, and a transmitter circuit for transmitting a resultant modulated signal; and a receiver having an input circuit for receiving the modulated signal, a demodulator circuit for demodulating one-bit signal points of a

QAM carrier wave, and an output circuit.

[0018] In operation, the input signal containing a first data stream of n values and a second data stream is fed to the modulator circuit of the transmitter where a modified m-bit QAM carrier wave is produced representing m signal points in a vector field. The m signal points are divided into n signal point groups to which the n values of the first data stream are assigned respectively. Also, data of the second data stream are assigned to m/n signal points or sub groups of each signal point group. Then, a resultant transmission signal is transmitted from the transmitter circuit. Similarly, a third data stream can be propagated.

[0019] At the p-bit demodulator circuit, p>m, of the receiver, the first data stream of the transmission signal is first demodulated through dividing p signal points in a signal space diagram into n signal point groups. Then, the second data stream is demodulated through assigning p/n values to p/n signal points of each corresponding signal point group for reconstruction of both the first and second data streams. If the receiver is at P=n, the n signal point groups are reclaimed and assigned the n values for demodulation and reconstruction of the first data stream.

[0020] Upon receiving the same transmission signal from the transmitter, a receiver equipped with a large sized antenna and capable of large-data modulation can reproduce both the first and second data streams. A receiver equipped with a small sized antenna and capable of small-data modulation can reproduce the first data stream only. Accordingly, the compatibility of the signal transmission system will be ensured. When the first data stream is an NTSC TV signal or low frequency band component of an HDTV signal and the second data stream is a high frequency band component of the HDTV signal, the small-data modulation receiver can reconstruct the NTSC TV signal and the large-data modulation receiver can reconstruct the HDTV signal. As understood, a digital NTSC/HDTV simultaneously broadcast service will be feasible using the compatibility of the signal transmission system of the present invention.

[0021] More specifically, the communication system of the present invention comprises: a transmitter having a signal input circuit, a modulator circuit for producing m signal points, in a signal vector field through modulation of a plurality of out-of-phase carrier waves using an input signal supplied from the input, and a transmitter circuit for transmitting a resultant modulated signal, in which the main procedure includes receiving an input signal containing a first data stream of n values and a second data stream, dividing the m signal points of the signal into n signal point groups, assigning the n values of the first data stream to the n signal point groups respectively, assigning data of the second data stream to the signal points of each signal point group respectively, and transmitting the resultant modulated signal; and a receiver having an input circuit for receiving the modulated signal, a demodulator circuit for demodulating p signal points of a QAM carrier wave, and an output circuit, in which the main procedure includes dividing the p signal points into n signal point groups, demodulating the first data stream of which n values are assigned to the n signal point groups respectively, and demodulating the second data stream of which p/n values are assigned to p/n signal points of each signal point group respectively. For example, a transmitter 1 produces a modified m-bit QAM signal of which first, second, and third data streams, each carrying n values, are assigned to relevant signal point groups with a modulator 4. The signal can be intercepted and reproduced the first data stream only by a first receiver 23, both the first and second data streams by a second receiver 33, and all the first, second, and third streams by a third receiver 43.

[0022] More particularly, a receiver capable of demodulation of n-bit data can reproduce n bits from a multiple-bit modulated carrier wave carrying an m-bit data where m>n, thus allowing the communication system to have compatibility and capability of future extension. Also, a multi-level signal transmission will be possible by shifting the signal points of QAM so that a nearest signal point to the origin point of I-axis and Q-axis coordinates is spaced nf from the origin where f is the distance of the nearest point from each axis and n is more than 1.

[0023] Accordingly, a compatible digital satellite broadcast service for both the NTSC and HDTV systems will be feasible when the first data stream carries an NTSC signal and the second data stream carries a difference signal between NTSC and HDTV. Hence, the capability of corresponding to an increase in the data amount to be transmitted will be ensured. Also, at the ground, its service area will be increased while signal attenuating areas are decreased.

[0024] The present invention will be further described hereinafter with reference to the following description of exemplary embodiments and the accompanying drawings, in which:

Fig. 1 is a schematic view of the entire arrangement of a signal transmission system showing a first embodiment of the present invention;

Fig. 2 is a block diagram of a transmitter of the first embodiment;

Fig. 3 is a vector diagram showing a transmission signal of the first embodiment;

Fig. 4 is a vector diagram showing a transmission signal of the first embodiment;

Fig. 5 is a view showing an assignment of binary codes to signal points according to the first embodiment;

Fig. 6 is a view showing an assignment of binary codes to signal point groups according to the first embodiment;

Fig. 7 is a view showing an assignment of binary codes to signal points in each signal point group according to the first embodiment;

Fig. 8 is a view showing another assignment of bi-

nary codes to signal point groups and their signal points according to the first embodiment;
Fig. 9 is a view showing threshold values of the signal point groups according to the first embodiment;
Fig. 10 is a vector diagram of a modified 16 QAM signal of the first embodiment;
Fig. 11 is a graphic diagram showing the relation between antenna radius r_2 and transmission energy ratio n according to the first embodiment;
Fig. 12 is a view showing the signal points of a modified 64 QAM signal of the first embodiment;
Fig. 13 is a graphic diagram showing the relation between antenna radius r_3 and transmission energy ratio n according to the first embodiment;
Fig. 14 is a vector diagram showing signal point groups and their signal points of the modified 64 QAM signal of the first embodiment;
Fig. 15 is an explanatory view showing the relation between A_1 and A_2 of the modified 64 QAM signal of the first embodiment;
Fig. 16 is a graph diagram showing the relation between antenna radius r_2, r_3 and transmission energy ratio n_{16}, n_{64} respectively according to the first embodiment;
Fig. 17 is a block diagram of a digital transmitter of the first embodiment;
Fig. 18 is a signal space diagram of a 4 PSK modulated signal of the first embodiment;
Fig. 19 is a block diagram of a first receiver of the first embodiment;
Fig. 20 is a signal space diagram of a 4 PSK modulated signal of the first embodiment;
Fig. 21 is a block diagram of a second receiver of the first embodiment;
Fig. 22 is a vector diagram of a modified 16 QAM signal of the first embodiment;
Fig. 23 is a vector diagram of a modified 64 QAM signal of the first embodiment;
Fig. 24 is a flow chart showing an action of the first embodiment;
Figs. 25(a) and 25(b) are vector diagrams showing an 8 and a 16 QAM signal of the first embodiment respectively;
Fig. 26 is a block diagram of a third receiver of the first embodiment;
Fig. 27 is a view showing signal points of the modified 64 QAM signal of the first embodiment;
Fig. 28 is a flow chart showing another action of the first embodiment;
Fig. 29 is a schematic view of the entire arrangement of a signal transmission system showing a third embodiment of the present invention;
Fig. 30 is a block diagram of a first video encoder of the third embodiment;
Fig. 31 is a block diagram of a first video decoder of the third embodiment;
Fig. 32 is a block diagram of a second video decoder of the third embodiment;
Fig. 33 is a block diagram of a third video decoder of the third embodiment;
Fig. 34 is an explanatory view showing a time multiplexing of D_1, D_2, and D_3 signals according to the third embodiment;
Fig. 35 is an explanatory view showing another time multiplexing of the D_1, D_2, and D_3 signals according to the third embodiment;
Fig. 36 is an explanatory view showing a further time multiplexing of the D_1, D_2, and D_3 signals according to the third embodiment;
Fig. 37 is a schematic view of the entire arrangement of a signal transmission system showing a fourth embodiment of the present invention;
Fig. 38 is a vector diagram of a modified 16 QAM signal of the third embodiment;
Fig. 39 is a vector diagram of the modified 16 QAM signal of the third embodiment;
Fig. 40 is a vector diagram of a modified 64 QAM signal of the third embodiment;
Fig. 41 is a diagram of assignment of data components on a time base according to the third embodiment;
Fig. 42 is a diagram of assignment of data components on a time base in TDMA action according to the third embodiment;
Fig. 43 is a block diagram of a carrier reproducing circuit of the third embodiment;
Fig. 44 is a diagram showing the principle of carrier wave reproduction according to the third embodiment;
Fig. 45 is a block diagram of a carrier reproducing circuit for reverse modulation of the third embodiment;
Fig. 46 is a diagram showing an assignment of signal points of the 16 QAM signal of the third embodiment;
Fig. 47 is a diagram showing an assignment of signal points of the 64 QAM signal of the third embodiment;
Fig. 48 is a block diagram of a carrier reproducing circuit for 16x multiplication of the third embodiment;
Fig. 49 is an explanatory view showing a time multiplexing of D_{V1}, D_{H1}, D_{V2}, D_{H2}, D_{V3}, and D_{H3} signals according to the third embodiment;
Fig. 50 is an explanatory view showing a TDMA time multiplexing of D_{V1}, D_{H1}, D_{V2}, D_{H2}, D_{V3}, and D_{H3} signals according to the third embodiment;
Fig. 51 is an explanatory view showing another TDMA time multiplexing of the D_{V1}, D_{H1}, D_{V2}, D_{H2}, D_{V3}, and D_{H3} signals according to the third embodiment;
Fig. 52 is a diagram showing a signal interference region in a known transmission method according to the fourth embodiment;
Fig. 53 is a diagram showing signal interference regions in a multi-level signal transmission method according to the fourth embodiment;

Fig. 54 is a diagram showing signal attenuating regions in the known transmission method according to the fourth embodiment;
Fig. 55 is a diagram showing signal attenuating regions in the multi-level signal transmission method according to the fourth embodiment;
Fig. 56 is a diagram showing a signal interference region between two digital TV stations according to the fourth embodiment;
Fig. 57 is a diagram showing an assignment of signal points of a modified 4 ASK signal of the fifth embodiment;
Fig. 58 is a diagram showing another assignment of signal points of the modified 4 ASK signal of the fifth embodiment;
Figs. 59(a) and 59(b) are diagrams showing assignment of signal points of the modified 4 ASK signal of the fifth embodiment;
Fig. 60 is a diagram showing another assignment of signal points of the modified 4 ASK signal of the fifth embodiment when the C/N rate is low;
Fig. 61 is a block diagram of a transmitter of the fifth embodiment;
Figs. 62(a) and 62(b) are diagrams showing frequency distribution profiles of an ASK modulated signal of the fifth embodiment;
Fig. 63 is a block diagram of a receiver of the fifth embodiment;
Fig. 64 is a block diagram of a video signal transmitter of the fifth embodiment;
Fig. 65 is a block diagram of a TV receiver of the fifth embodiment;
Fig. 66 is a block diagram of another TV receiver of the fifth embodiment;
Fig. 67 is a block diagram of a satellite-to-ground TV receiver of the fifth embodiment;
Fig. 68 is a diagram showing an assignment of signal points of an 8 ASK signal of the fifth embodiment;
Fig. 69 is a block diagram of a video encoder of the fifth embodiment;
Fig. 70 is a block diagram of a video encoder of the fifth embodiment containing one divider circuit;
Fig. 71 is a block diagram of a video decoder of the fifth embodiment;
Fig. 72 is a block diagram of a video decoder of the fifth embodiment containing one mixer circuit;
Fig. 73 is a diagram showing a time assignment of data components of a transmission signal according to the fifth embodiment;
Fig. 74(a) is a block diagram of a video decoder of the fifth embodiment;
Fig. 74(b) is a diagram showing another time assignment of data components of the transmission signal according to the fifth embodiment;
Fig. 75 is a diagram showing a time assignment of data components of a transmission signal according to the fifth embodiment;
Fig. 76 is a diagram showing a time assignment of data components of a transmission signal according to the fifth embodiment;
Fig. 77 is a diagram showing a time assignment of data components of a transmission signal according to the fifth embodiment;
Fig. 78 is a block diagram of a video decoder of the fifth embodiment;
Fig. 79 is a diagram showing a time assignment of data components of a three-level transmission signal according to the fifth embodiment;
Fig. 80 is a block diagram of another video decoder of the fifth embodiment;
Fig. 81 is a diagram showing a time assignment of data components of a transmission signal according to the fifth embodiment;
Fig. 82 is a block diagram of a video decoder for D_1 signal of the fifth embodiment;
Fig. 83 is a graphic diagram showing the relation between frequency and time of a frequency modulated signal according to the fifth embodiment;
Fig. 84 is a block diagram of a magnetic record/playback apparatus of the fifth embodiment;
Fig. 85 is a graphic diagram showing the relation between C/N and level according to the second embodiment;
Fig. 86 is a graphic diagram showing the relation between C/N and transmission distance according to the second embodiment;
Fig. 87 is a block diagram of a transmission of the second embodiment;
Fig. 88 is a block diagram of a receiver of the second embodiment;
Fig. 89 is a graphic diagram showing the relation between C/N and error rate according to the second embodiment;
Fig. 90 is a diagram showing signal attenuating regions in the three-level transmission of the fifth embodiment;
Fig. 91 is a diagram showing signal attenuating regions in the four-level transmission of a sixth embodiment;
Fig. 92 is a diagram showing the four-level transmission of the sixth embodiment;
Fig. 93 is a block diagram of a divider of the sixth embodiment;
Fig. 94 is a block diagram of a mixer of the sixth embodiment;
Fig. 95 is a diagram showing another four-level transmission of the sixth embodiment;
Fig. 96 is a view of signal propagation of a known digital TV broadcast system;
Fig. 97 is a view of signal propagation of a digital TV broadcast system according to the sixth embodiment;
Fig. 98 is a diagram showing a four-level transmission of the sixth embodiment;
Fig. 99 is a vector diagram of a 16 SRQAM signal

of the third embodiment;
Fig. 100 is a vector diagram of a 32 SRQAM signal of the third embodiment;
Fig. 101 is a graphic diagram showing the relation between C/N and error rate according to the third embodiment;
Fig. 102 is a graphic diagram showing the relation between C/N and error rate according to the third embodiment;
Fig. 103 is a graphic diagram showing the relation between shift distance n and C/N needed for transmission according to the third embodiment;
Fig. 104 is a graphic diagram showing the relation between shift distance n and C/N needed for transmission according to the third embodiment;
Fig. 105 is a graphic diagram showing the relation between signal level and distance from a transmitter antenna in terrestrial broadcast service according to the third embodiment;
Fig. 106 is a diagram showing a service area of the 32 SRQAM signal of the third embodiment;
Fig. 107 is a diagram showing a service area of the 32 SRQAM signal of the third embodiment;
Fig. 108 is a diagram showing a frequency distribution profile of a TV signal of the third embodiment;
Fig. 109 is a diagram showing a time assignment of the TV signal of the third embodiment;
Fig. 110 is a diagram showing a principle of C-CDM of the third embodiment;
Fig. 111 is a view showing an assignment of codes according to the third embodiment;
Fig. 112 is a view showing an assignment of an extended 36 QAM according to the third embodiment;
Fig. 113 is a view showing a frequency assignment of a modulation signal according to the fifth embodiment;
Fig. 114 is a block diagram showing a magnetic recording/playback apparatus according to the fifth embodiment;
Fig. 115 is a block diagram showing a transmitter/receiver of a portable telephone according to the eighth embodiment;
Fig. 116 is a block diagram showing base stations according to the eighth embodiment;
Fig. 117 is a view illustrating communication capacities and traffic distribution of a conventional system;
Fig. 118 is a view illustrating communication capacities and traffic distribution according to the eighth embodiment;
Fig. 119(a) is a diagram showing a time slot assignment of a conventional system;
Fig. 119(b) is a diagram showing a time slot assignment according to the eighth embodiment;
Fig. 120(a) is a diagram showing a time slot assignment of a conventional TDMA system;
Fig. 120(b) is a diagram showing a time slot assignment according to a TDMA system of the eighth embodiment;
Fig. 121 is a block diagram showing a one-level transmitter/receiver according to the eighth embodiment;
Fig. 122 is a block diagram showing a two-level transmitter/receiver according to the eighth embodiment;
Fig. 123 is a block diagram showing an OFDM type transmitter/receiver according to the ninth embodiment;
Fig. 124 is a view illustrating a principle of the OFDM system according to the ninth embodiment;
Fig. 125(a) is a view showing a frequency assignment of a modulation signal of a conventional system;
Fig. 125(b) is a view showing a frequency assignment of a modulation signal according to the ninth embodiment;
Fig. 126(a) is a view showing a frequency assignment of a transmission signal of the ninth embodiment;
Fig. 126(b) is a view showing a frequency assignment of a receiving signal according to the ninth embodiment;
Fig. 127 is a block diagram showing a transmitter/receiver according to the ninth embodiment;
Fig. 128 is a block diagram showing a Trellis encoder according to the fifth embodiment;
Fig. 129 is a view showing a time assignment of effective symbol periods and guard intervals according to the ninth embodiment;
Fig. 130 is a graphic diagram showing a relation between C/N rate and error rate according to the ninth embodiment;
Fig. 131 is a block diagram showing a magnetic recording/playback apparatus according to the fifth embodiment;
Fig. 132 is a view showing a recording format of track on the magnetic tape and a travelling of a head;
Fig. 133 is a block diagram showing a transmitter/receiver according to the third embodiment;
Fig. 134 is a diagram showing a frequency assignment of a conventional broadcasting;
Fig. 135 is a diagram showing a relation between service area and picture quality in a three-level signal transmission system according to the third embodiment;
Fig. 136 is a diagram showing a frequency assignment in case the multi-level signal transmission system according to the third embodiment is combined with an FDM;
Fig. 137 is a block diagram showing a transmitter/receiver according to the third embodiment, in which Trellis encoding is adopted; and
Fig. 138 is a block diagram showing a transmitter/receiver according to the ninth embodiment, in which a part of low frequency band signal is trans-

mitted by OFDM.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiment 1

[0025] One embodiment of the present invention will be described referring to the relevant drawings.

[0026] Fig. 1 shows the entire arrangement of a signal transmission system according to the present invention. A transmitter 1 comprises an input unit 2, a divider circuit 3, a modulator 4, and a transmitter unit 5. In action, each input multiplex signal is divided by the divider circuit 3 into three groups, a first data stream D1, a second data stream D2, a third data stream D3, which are then modulated by the modulator 4 before transmitted from the transmitter unit 5. The modulated signal is sent up from an antennal 6 through an uplink 7 to a satellite 10 where it is intercepted by an uplink antenna 11 and amplified by a transponder 12 before transmitted from a downlink antenna 13 towards the ground.

[0027] The transmission signal is then sent down through three downlinks 21, 32, and 41 to a first 23, a second 33, and a third receiver 43 respectively. In the first receiver 23, the signal intercepted by an antenna 22 is fed through an input unit 24 to a demodulator 25 where its first data stream only is demodulated, while the second and third data streams are not recovered, before transmitted further from an output unit 26.

[0028] Similarly, the second receiver 33 allows the first and second data streams of the signal intercepted by an antenna 32 and fed from an input unit 34 to be demodulated by a demodulator 35 and then, summed by a summer 37 to a single data stream which is then transmitted further from an output unit 36.

[0029] The third receiver 43 allows all the first, second, and third data streams of the signal intercepted by an antenna 42 and fed from an input unit 44 to be demodulated by a demodulator 45 and then, summed by a summer 47 to a single data stream which is then transmitted further from an output unit 46.

[0030] As understood, the three discrete receivers 23, 33, and 43 have their respective demodulators of different characteristics such that their outputs demodulated from the same frequency band signal of the transmitter 1 contain data of different sizes. More particularly, three different but compatible data can simultaneously be carried on a given frequency band signal to their respective receivers. For example, each of three, existing NTSC, HDTV, and super HDTV, digital signals is divided into a low, a high, and a super high frequency band components which represent the first, the second, and the third data stream respectively. Accordingly, the three different TV signals can be transmitted on a one-channel frequency band carrier for simultaneous reproduction of a medium, a high, and a super high resolution TV image respectively.

[0031] In service, the NTSC TV signal is intercepted by a receiver accompanied with a small antenna for demodulation of a small-sized data, the HDTV signal is intercepted by a receiver accompanied with a medium antenna for demodulation of medium-sized data, and the super HDTV signal is intercepted by a receiver accompanied with a large antenna for demodulation of large-sized data. Also, as illustrated in Fig. 1, a digital NTSC TV signal containing only the first data stream for digital NTSC TV broadcasting service is fed to a digital transmitter 51 where it is received by an input unit 52 and modulated by a demodulator 54 before transmitted further from a transmitter unit 55. The demodulated signal is then sent up from an antennal 56 through an uplink 57 to the satellite 10 which in turn transmits the same through a downlink 58 to the first receiver 23 on the ground.

[0032] The first receiver 23 demodulates with its demodulator 25 the modulated digital signal supplied from the digital transmitter 51 to the original first data stream signal. Similarly, the same modulated digital signal can be intercepted and demodulated by the second 33 or third receiver 42 to the first data stream or NTSC TV signal. In summary, the three discrete receivers 23, 33, and 43 all can intercept and process a digital signal of the existing TV system for reproduction.

[0033] The arrangement of the signal transmission system will be described in more detail.

[0034] Fig. 2 is a block diagram of the transmitter 1, in which an input signal is fed across the input unit 2 and divided by the divider circuit 3 into three digital signals containing a first, a second, and a third data stream respectively.

[0035] Assuming that the input signal is a video signal, its low frequency band component is assigned to the first data stream, its high frequency band component to the second data stream, its super-high frequency band component to the third data stream. The three different frequency band signals are fed to a modulator input 61 of the modulator 4. Here, a signal point modulating/changing circuit 67 modulates or changes the positions of the signal points according to an externally given signal. The modulator 4 is arranged for amplitude modulation on two 90°-out-of-phase carriers respectively which are then summed to a multiple QAM signal. More specifically, the signal from the modulator input 61 is fed to both a first 62 and a second AM modulator 63. Also, a carrier wave of $\cos(2\pi fct)$ produced by a carrier generator 64 is directly fed to the first AM modulator 62 and also, to a $\pi/2$ phase shifter 66 where it is 90° shifted in phase to a $\sin(2\pi fct)$ form prior to transmitted to the second AM modulator 63. The two amplitude modulated signals from the first and second AM modulators 62, 63 are summed by a summer 65 to a transmission signal which is then transferred to the transmitter unit 5 for output. The procedure is well known and will no further be explained.

[0036] The QAM signal will now be described in a

common 8x8 or 16 state constellation referring to the first quadrant of a space diagram in Fig. 3. The output signal of the modulator 4 is expressed by a sum vector of two, $A\cos 2\pi fct$ and $B\cos 2\pi fct$, vectors 81, 82 which represent the two 90°-out-of-phase carriers respectively. When the distal point of a sum vector from the zero point represents a signal point, the 16 QAM signal has 16 signal points determined by a combination of four horizontal amplitude values a_1, a_2, a_3, a_4 and four vertical amplitude values b_1, b_2, b_3, b_4. The first quadrant in Fig. 3 contains four signal points 83 at C_{11}, 84 at C_{12}, 85 at C_{22}, and 86 at C_{21}.

[0037] C_{11} is a sum vector of a vector $0\text{-}a_1$ and a vector $0\text{-}b_1$ and thus, expressed as $C_{11} = a_1\cos 2\pi fct - b_1\sin 2\pi fct - A\cos(2\pi fct + d\pi/2)$.

[0038] It is now assumes that the distance between 0 and a_1 in the orthogonal coordinates of Fig. 3 is A_1, between a_1 and a_2 is A_2, between 0 and b_1 is B_1, and between b_1 and b_2 is B_2.

[0039] As shown in Fig. 4, the 16 signal points are allocated in a vector coordinate, in which each point represents a four-bit pattern thus to allow the transmission of four bit data per period or time slot.

[0040] Fig. 5 illustrates a common assignment of two-bit patterns to the 16 signal points.

[0041] When the distance between two adjacent signal points is great, it will be identified by the receiver with much ease. Hence, it is desired to space the signal points at greater intervals. If two particular signal points are allocated near to each other, they are rarely distinguished and error rate will be increased. Therefore, it is most preferred to have the signal points spaced at equal intervals as shown in Fig. 5, in which the 16 QAM signal is defined by $A_1 = A_2/2$.

[0042] The transmitter 1 of the embodiment is arranged to divide an input digital signal into a first, a second, and a third data or bit stream. The 16 signal points or groups of signal points are divided into four groups. Then, 4 two-bit patterns of the first data stream are assigned to the four signal point groups respectively, as shown in Fig. 6. More particularly, when the two-bit pattern of the first data stream is 11, one of four signal points of the first signal point group 91 in the first quadrant is selected depending on the content of the second data stream for transmission. Similarly, when 01, one signal point of the second signal point group 92 in the second quadrant is selected and transmitted. When 00, one signal point of the third signal point group 93 in the third quadrant is transmitted and when 10, one signal point of the fourth signal point group 94 in the fourth quadrant is transmitted. Also, 4 two-bit patterns in the second data stream of the 16 QAM signal, or e.g. 16 four-bit patterns in the second data stream of a 64-state QAM signal, are assigned to four signal points or sub signal point groups of each of the four signal point groups 91, 92, 93, 94 respectively, as shown in Fig. 7. It should be understood that the assignment is symmetrical between any two quadrants. The assignment of the signal points to the four groups 91, 92, 93, 94 is determined by priority to the two-bit data of the first data stream. As the result, two-bit data of the first data stream and two-bit data of the second data stream can be transmitted independently. Also, the first data stream will be demodulated with the use of a common 4 PSK receiver having a given antenna sensitivity. If the antenna sensitivity is higher, a modified type of the 16 QAM receiver of the present invention will intercept and demodulate both the first and second data stream with equal success.

[0043] Fig. 8 shows an example of the assignment of the first and second data streams in two-bit patterns.

[0044] When the low frequency band component of an HDTV video signal is assigned to the first data stream and the high frequency component to the second data stream, the 4 PSK receiver can produce an NTSC-level picture from the first data stream and the 16- or 64-state QAM receiver can produce an HDTV picture from a composite reproduction signal of the first and second data streams.

[0045] Since the signal points are allocated at equal intervals, there is developed in the 4 PSK receiver a threshold distance between the coordinate axes and the shaded area of the first quadrant, as shown in Fig. 9. If the threshold distance is A_{T0}, a PSK signal having an amplitude of A_{T0} will successfully be intercepted. However, the amplitude has to be increased to a three times greater value or $3A_{T0}$ for transmission of a 16 QAM signal while the threshold distance A_{T0} being maintained. More particularly, the energy for transmitting the 16 QAM signal is needed nine times greater than that for sending the 4 PSK signal. Also, when the 4 PSK signal is transmitted in a 16 QAM mode, energy waste will be high and reproduction of a carrier signal will be troublesome. Above all, the energy available for satellite transmitting is not abundant but strictly limited to minimum use. Hence, no large-energy-consuming signal transmitting system will be put into practice until more energy for satellite transmission is available. It is expected that a great number of the 4 PSK receivers are introduced into the market as digital TV broadcasting is soon in service. After introduction to the market, the 4 PSK receivers will hardly be shifted to higher sensitivity models because a signal intercepting characteristic gap between the two, old and new, models is high. Therefore, the transmission of the 4 PSK signals must not be abandoned.

[0046] In this respect, a new system is desperately needed for transmitting the signal point data of a quasi 4 PSK signal in the 16 QAM mode with the use of less energy. Otherwise, the limited energy at a satellite station will degrade the entire transmission system.

[0047] The present invention resides in a multiple signal level arrangement in which the four signal point groups 91, 92, 93 94 are allocated at a greater distance from each other, as shown in Fig. 10, for minimizing the energy consumption required for 16 QAM modulation of quasi 4 PSK signals.

[0048] For clearing the relation between the signal receiving sensitivity and the transmitting energy, the arrangement of the digital transmitter 51 and the first receiver 23 will be described in more detail referring to Fig. 1.

Both the digital transmitter 51 and the first receiver 23 are formed of known types for data transmission or video signal transmission e.g. in TV broadcasting service. As shown in Fig. 17, the digital transmitter 51 is a 4 PSK transmitter equivalent to the multiple-bit QAM transmitter 1, shown in Fig. 2, without AM modulation capability. In operation, an input signal is fed through an input unit 52 to a modulator 54 where it is divided by a modulator input 121 to two components. The two components are then transferred to a first two-phase modulator circuit 122 for phase modulation of a bass carrier and a second two-phase modulator circuit 123 for phase modulation of a carrier which is 90° out of phase with the base carrier respectively. Two outputs of the first and second two-phase modulator circuits 122, 123 are then summed by a summer 65 to a composite modulated signal which is further transmitted from a transmitter unit 55.

[0049] The resultant modulated signal is shown in the space diagram of Fig. 18.

[0050] It is known that the four signal points are allocated at equal distances for achieving optimum energy utilization. Fig. 18 illustrates an example where the four signal points 125, 126, 127, 128 represent 4 two-bit patterns, 11, 01, 00, and 10 respectively. It is also desired for successful data transfer from the digital transmitter 51 to the first receiver 23 than the 4 PSK signal from the digital transmitter 51 has an amplitude of not less than a given level. More specifically, when the minimum amplitude of the 4 PSK signal needed for transmission from the digital transmitter 51 to the first receiver 23 of 4 PSK mode, or the distance between 0 and a_1 in Fig. 18 is A_{T0}, the first receiver 23 successfully intercept any 4 PSK signal having an amplitude of more than A_{T0}.

[0051] The first receiver 23 is arranged to receive at its small-diameter antenna 22 a desired or 4 PSK signal which is transmitted from the transmitter 1 or digital transmitter 51 respectively through the transponder 12 of the satellite 10 and demodulate it with the demodulator 24. In more particular, the first receiver 23 is substantially designed for interception of a digital TV or data communications signal of 4 PSK or 2 PSK mode.

[0052] Fig. 19 is a block diagram of the first receiver 23 in which an input signal received by the antenna 22 from the satellite 12 is fed through the input unit 24 to a carrier reproducing circuit 131 where a carrier wave is demodulated and to a $\pi/2$ phase shifter 132 where a 90° phase carrier wave is demodulated. Also, two 90°-out-of-phase components of the input signal are detected by a first 133 and a second phase detector circuit 134 respectively and transferred to a first 136 and a second discrimination/demodulation circuit 137 respectively. Two demodulated components from their respective discrimination/demodulation circuits 136 and 137, which have separately been discriminated at units of time slot by means of timing signals from a timing wave extracting circuit 135, are fed to a first data stream reproducing unit 232 where they are summed to a first data stream signal which is then delivered as an output from the output unit 26.

[0053] The input signal to the first receiver 23 will now be explained in more detail referring to the vector diagram of Fig. 20. The 4 PSK signal received by the first receiver 23 from the digital transmitter 51 is expressed in an ideal form without transmission distortion and noise, using four signal points 151, 152, 153, 154 shown in Fig. 20.

[0054] In practice, the real four signal points appear in particular extended areas about the ideal signal positions 151, 152, 153, 154 respectively due to noise, amplitude distortion, and phase error developed during transmission. If one signal point is unfavorably displaced from its original position, it will hardly be distinguished from its neighbor signal point and the error rate will thus be increased. As the error rate increases to a critical level, the reproduction of data becomes less accurate. For enabling the data reproduction at a maximum acceptable level of the error rate, the distance between any two signal points should be far enough to be distinguished from each other. If the distance is $1A_{R0}$, the signal point 151 of a 4 PSK signal at close to a critical error level has to stay in a first discriminating area 155 denoted by the hatching of Fig. 20 and determined by $|0 \cdot a_{R1}| \geq A_{R0}$ and $|0 \cdot b_{R1}| \geq A_{R0}$. This allows the signal transmission system to reproduce carrier waves and thus, demodulate a wanted signal. When the minimum radius of the antenna 22 is set to r_0, the transmission signal of more than a given level can be intercepted by any receiver of the system. The amplitude of a 4 PSK signal of the digital transmitter 51 shown in Fig. 18 is minimum at A_{T0} and thus, the minimum amplitude A_{R0} of a 4 PSK signal to be received by the first receiver 23 is determined equal to A_{T0}. As the result, the first receiver 23 can intercept and demodulate the 4 PSK signal from the digital transmitter 51 at the maximum acceptable level of the error rate when the radius of the antenna 22 is more than r_0. If the transmission signal is of modified 16- or 64-state QAM mode, the first receiver 23 may find difficult to reproduce its carrier wave. For compensation, the signal points are increased to eight which are allocated at angles of $(\pi/4+n\pi/2)$ as shown in Fig. 25(a) and its carrier wave will be reproduced by a 16x multiplication technique. Also, if the signal points are assigned to 16 locations at angles of $n\pi/8$ as shown in Fig. 25(b), the carrier of a quasi 4 PSK mode 16 QAM modulated signal can be reproduced with the carrier reproducing circuit 131 which is modified for performing 16x frequency multiplication. At the time, the signal points in the transmitter 1 should be arranged to satisfy $A_1/(A_1+A_2)=\tan(\pi/8)$.

[0055] Here, a case of receiving a QPSK signal will

be considered. Similarly to the manner performed by the signal point modulating/changing circuit 67 in the transmitter shown in Fig. 2, it is also possible to modulate the positions of the signal points of the QPSK signal shown in Fig. 18 (amplitude-modulation, pulse-modulation, or the like). In this case, the signal point demodulating unit 138 in the first receiver 23 demodulates the position modulated or position changed signal. The demodulated signal is outputted together with the first data stream.

[0056] The 16 PSK signal of the transmitter 1 will now be explained referring to the vector diagram of Fig. 9. When the horizontal vector distance A_1 of the signal point 83 is greater than A_{T0} of the minimum amplitude of the 4 PSK signal of the digital transmitter 51, the four signal points 83, 84, 85, 86 in the first quadrant of Fig. 9 stay in the shaded or first 4 PSK signal receivable area 87. When received by the first receiver 23, the four points of the signal appear in the first discriminating area of the vector field shown in Fig. 20. Hence, any of the signal points 83, 84, 85, 86 of Fig. 9 can be translated into the signal level 151 of Fig. 20 by the first receiver 23 so that the two-bit pattern of 11 is assigned to a corresponding time slot. The two-bit pattern of 11 is identical to 11 of the first signal point group 91 or first data stream of a signal from the transmitter 1. Equally, the first data stream will be reproduced at the second, third, or fourth quadrant. As the result, the first receiver 23 reproduces two-bit data of the first data stream out of the plurality of data streams in a 16-, 32-, or 64-state QAM signal transmitted from the transmitter 1. The second and third data streams are contained in four segments of the signal point group 91 and thus, will not affect on the demodulation of the first data stream. They may however affect the reproduction of a carrier wave and an adjustment, described later, will be needed.

[0057] If the transponder of a satellite supplies an abundance of energy, the forgoing technique of 16 to 64-state QAM mode transmission will be feasible. However, the transponder of the satellite in any existing satellite transmission system is strictly limited in the power supply due to its compact size and the capability of solar batteries. If the transponder or satellite is increased in size thus weight, its launching cost will soar. This disadvantage will rarely be eliminated by traditional techniques unless the cost of launching a satellite rocket is reduced to a considerable level. In the existing system, a common communications satellite provides as low as 20 W of power supply and a common broadcast satellite offers 100 W to 200 W at best. For transmission of such a 4 PSK signal in the symmetrical 16-state QAM mode as shown in Fig. 9, the minimum signal point distance is needed $3A_{T0}$ as the 16 QAM amplitude is expressed by $2A_1=A_2$. Thus, the energy needed for the purpose is nine times greater than that for transmission of a common 4 PSK signal, in order to maintain compatibility. Also, any conventional satellite transponder can hardly provide a power for enabling such a small antenna of the 4 PSK first receiver to intercept a transmitted signal therefrom. For example, in the existing 40W system, 360W is needed for appropriate signal transmission and will be unrealistic in the respect of cost.

[0058] It would be under stood that the symmetrical signal state QAM technique is most effective when the receivers equipped with the same sized antennas are employed corresponding to a given transmitting power. Another novel technique will however be preferred for use with the receivers equipped with different sized antennas.

[0059] In more detail, while the 4 PSK signal can be intercepted by a common low cost receiver system having a small antenna, the 16 QAM signal is intended to be received by a high cost, high quality, multiple-bit modulating receiver system with a medium or large sized antenna which is designed for providing highly valuable services, e.g. HDTV entertainments, to a particular person who invests more money. This allows both 4 PSK and 16 QAM signals, if desired, with a 64 DMA, to be transmitted simultaneously with the help of a small increase in the transmitting power.

[0060] For example, the transmitting power can be maintained low when the signal points are allocated at $A_1=A_2$ as shown in Fig. 10. The amplitude A(4) for transmission of 4 PSK data is expressed by a vector 96 equivalent to a square root of $(A_1+A_2)^2+(B_1+B_2)^2$. Then,

$$|A(4)|^2=A_1^2+B_1^2=A_{T0}^2+A_{T0}^2=2A_{T0}^2$$

$$|A(16)|^2=(A_1+A_2)^2+(B_1+B_2)^2=4A_{T0}^2+4A_{T0}^2=B_{T0}^2$$

$$|A(16)|/|A(4)|=2$$

[0061] Accordingly, the 16 QAM signal can be transmitted at a two times greater amplitude and a four times greater transmitting energy than those needed for the 4 PSK signal. A modified 16 QAM signal according to the present invention will not be demodulated by a common receiver designed for symmetrical, equally distanced signal point QAM. However, it can be demodulated with the second receiver 33 when two threshold A_1 and A_2 are predetermined to appropriate values. At Fig. 10, the minimum distance between two signal points in the first segment of the signal point group 91 is A_1 and $A_2/2A_1$ is established as compared with the distance $2A_1$ of 4 PSK. Then, as $A_1=A_2$, the distance becomes 1/2. This explains that the signal receiving sensitivity has to be two times greater for the same error rate and four times greater for the same signal level. For having a four times greater value of sensitivity, the radius r_2 of the antenna 32 of the second receiver 33 has to be two times greater than the radius r_1 of the antenna 22 of the first receiver 23 thus satisfying $r_2=2r_1$. For example, the antenna 32 of the second receiver 33 is 60 cm diameter when the antenna 22 if the first receiver 23 is 30 cm. In this man-

ner, the second data stream representing the high frequency component of an HDTV will be carried on a signal channel and demodulated successfully. As the second receiver 33 intercepts the second data stream or a higher data signal, its owner can enjoy a return of high investment. Hence, the second receiver 33 of a high price may be accepted. As the minimum energy for transmission of 4 PSK data is predetermined, the ratio n_{16} of modified 16 APSK transmitting energy to 4 PSK transmitting energy will be calculated to the antenna radius r_2 of the second receiver 33 using a ratio between A_1 and A_2 shown in Fig. 10.

[0062] In particular, n_{16} is expressed by $((A_1+A_2)/A_1)^2$ which is the minimum energy for transmission of 4 PSK data. As the signal point distance suited for modified 16 QAM interception is A_2, the signal point distance for 4 PSK interception is $2A_1$, and the signal point distance ratio is $A_2/2A_1$, the antenna radius r_2 is determined as shown in Fig. 11, in which the curve 101 represents the relation between the transmitting energy ratio n_{16} and the radius r_2 of the antenna 22 of the second receiver 23.

[0063] Also, the point 102 indicates transmission of common 16 QAM at the equal distance signal state mode where the transmitting energy is nine times greater and thus will no more be practical. As apparent from the graph of Fig. 11, the antenna radius r_2 of the second receiver 23 cannot be reduced further even if n_{16} is increased more than 5 times.

[0064] The transmitting energy at the satellite is limited to a small value and thus, n_{16} preferably stays not more than 5 times the value, as denoted by the hatching of Fig. 11. The point 104 within the hatching area 103 indicates, for example, that the antenna radius r_2 of a two times greater value is matched with a 4x value of the transmitting energy. Also, the point 105 represents that the transmission energy should be doubled when r_2 is about 5x greater. Those values are all within a feasible range.

[0065] The value of n_{16} not greater than 5x value is expressed using A_1 and A_2 as:

$$n_{16} = ((A_1+A_2)/A_1)^2 \leq 5$$

Hence, $A_2 \leq 1.23A_1$.

[0066] If the distance between any two signal point group segments shown in Fig. 10 is 2A(4) and the maximum amplitude is 2A(16), A(4) and A(16)-A(4) are proportional to A_1 and A_2 respectively. Hence, $(A(16))^2 \leq 5(A(14))^2$ is established.

[0067] The action of a modified 64 ASPK transmission will be described as the third receiver 43 can perform 64-state QAM demodulation.

[0068] Fig. 12 is a vector diagram in which each signal point group segment contains 16 signal points as compared with 4 signal points of Fig. 10. The first signal point group segment 91 in Fig. 12 has a 4x4 matrix of 16 signal points allocated at equal intervals including the point 170. For providing compatibility with 4 PSK, $A_1 \geq A_{TO}$ has to be satisfied. If the radius of the antenna 42 of the third receiver 43 is r_3 and the transmitting energy is n_{64}, the equation is expressed as:

$$r_3^2 = \{6^2/(n-1)\}r_1^2$$

[0069] This relation between r_3 and n of a 64 QAM signal is also shown in the graphic representation of Fig. 13.

[0070] It is under stood that the signal point assignment shown in Fig. 12 allows the second receiver 33 to democulate only two-bit patterns of 4 PSK data. Hence, it is desired for having compatibility between the first, second, and third receivers that the second receiver 33 is arranged capable of demodulating a modified 16 QAM form from the 64 QAM modulated signal.

[0071] The compatibility between the three discrete receivers can be implemented by three-level grouping of signal points, as illustrated in Fig. 14. The description will be made referring to the first quadrant in which the first signal point group segment 91 represents the two-bit pattern 11 of the first data stream.

[0072] In particular, a first sub segment 181 in the first signal point group segment 91 is assigned the two-bit pattern 11 of the second data stream. Equally, a second 182, a third 183, and a fourth sub segment 184 are assigned 01, 00, and 10 of the same respectively. This assignment is identical to that shown in Fig. 7.

[0073] The signal point allocation of the third data stream will now be explained referring to the vector diagram of Fig. 15 which shows the first quadrant. As shown, the four signal points 201, 205, 209, 213 represent the two-bit pattern of 11, the signal points 202, 206, 210, 214 represent 01, the signal points 203, 207, 211, 215 represent 00, and signal points 204, 208, 212, 216 represent 10. Accordingly, the two-bit patterns of the third data stream can be transmitted separately of the first and second data streams. In other words, two-bit data of the three different signal levels can be transmitted respectively.

[0074] As understood, the present invention permits not only transmission of six-bit data but also interception of three, two-bit, four-bit, and six-bit, different bit length data with their respective receivers while the signal compatibility remains between three levels.

[0075] The signal point allocation for providing compatibility between the three levels will be described.

[0076] As shown in Fig. 15, $A_1 \geq A_{TO}$ is essential for allowing the first receiver 23 to receive the first data stream.

[0077] It is needed to space any two signal points from each other by such a distance that the sub segment signal points, e.g. 182, 183, 184, of the second data stream shown in Fig. 15 can be distinguished from the signal point 91 shown in Fig. 10.

[0078] Fig. 15 shows that they are spaced by $2/3A_2$.

In this case, the distance between the two signal points 201 and 202 in the first sub segment 181 is $A_2/6$. The transmitting energy needed for signal interception with the third receiver 43 is now calculated. If the radius of the antenna 32 is r_3 and the needed transmitting energy is n_{64} times the 4 PSK transmitting energy, the equation is expressed as:

$$r_3^2=(12r_1)^2/(n-1)$$

This relation is also denoted by the curve 211 in Fig. 16. For example, if the transmitting energy is 6 or 9 times greater than that for 4 PSK transmission at the point 223 or 222, the antenna 32 having a radius of 8x or 6x value respectively can intercept the first, second, and third data streams for demodulation. As the signal point distance of the second data stream is close to $2/3A_2$, the relation between r_1 and r_2 is expressed by:

$$r_2^2=(3r_1)^2/(n-1)$$

Therefore, the antenna 32 of the second receiver 33 has to be a little bit increased in radius as denoted by the curve 223.

[0079] As understood, while the first and second data streams are transmitted trough a traditional satellite which provides a small signal transmitting energy, the third data stream can also be transmitted through a future satellite which provides a greater signal transmitting energy without interrupting the action of the first and second receivers 23, 33 or with no need of modification of the same and thus, both the compatibility and the advancement will highly be ensured.

[0080] The signal receiving action of the second receiver 33 will first be described. As compared with the first receiver 23 arranged for interception with a small radius r_1 antenna and demodulation of the 4 PSK modulated signal of the digital transmitter 51 or the first data stream of the signal of the transmitter 1, the second receiver 33 is adopted for perfectly demodulating the 16 signal state two-bit data, shown in Fig. 10, or second data stream of the 16 QAM signal from the transmitter 1. In total, four-bit data including also the first data stream can be demodulated. The ratio between A_1 and A_2 is however different in the two transmitters. The two different data are loaded to a demodulation controller 231 of the second receiver 33, shown in Fig. 21, which in turn supplies their respective threshold values to the demodulating circuit for AM demodulation.

[0081] The block diagram of the second receiver 33 in Fig. 21 is similar in basic construction to that of the first receiver 23 shown in Fig. 19. The difference is that the radius r_2 of the antenna 32 is greater than r_1 of the antenna 22. This allows the second receiver 33 to identify a signal component involving a smaller signal point distance. The demodulator 35 of the second receiver 33 also contains a first 232 and a second data stream reproducing unit 233 in addition to the demodulation controller 231. There is provided a first discrimination/reproduction circuit 136 for AM demodulation of modified 16 QAM signals. As understood, each carrier is a four-bit signal having two, positive and negative, threshold values about the zero level. As apparent from the vector diagram, of Fig. 22, the threshold values are varied depending on the transmitting energy of a transmitter since the transmitting signal of the embodiment is a modified 16 QAM signal. When the reference threshold is TH_{16}, it is determined by, as shown in Fig. 22:

$$TH_{16} = (A_1+A_2/2)/(A_1+A_2)$$

[0082] The various data for demodulation including A_1 and A_2 or TH_{16}, and the value m for multiple-bit modulation are also transmitted from the transmitter 1 as carried in the first data stream. The demodulation controller 231 may be arranged for recovering such demodulation data through statistic process of the received signal.

[0083] A way of determining the shift factor A_1/A_2 will described with reference to Fig. 26. A change of the shift factor A_1/A_2 causes a change of the threshold value. Increase of a difference of a value of A_1/A_2 set at the receiver side from a value of A_1/A_2 set at the transmitter side will increase the error rate. Referring to Fig. 26, the demodulated signal from the second data stream reproducing unit 233 may be fed back to the demodulation controller 231 to change the shift factor A_1/A_2 in a direction to increase the error rate. By this arrangement, the third receiver 43 may not demodulate the shift factor A_1/A_2, so that the circuit construction can be simplified. Further, the transmitter may not transmit the shift factor A_1/A_2, so that the transmission capacity can be increased. This technique can be applied also to the second receiver 33.

[0084] The demodulation controller 231 has a memory 231a for storing therein different threshold values (i. e., the shift factors, the number of signal points, the synchronization rules, etc.) which correspond to different channels of TV broadcast. When receiving one of the channels again, the values corresponding to the receiving channel will be read out of the memory to thereby stabilize the reception quickly.

[0085] If the demodulation data is lost, the demodulation of the second data stream will hardly be executed. This will be explained referring to a flow chart shown in Fig. 24.

[0086] Even if the demodulation data is not available, demodulation of the 4 PSK at Step 313 and of the first data stream at Step 301 can be implemented. At Step 302, the demodulation data retrieved by the first data stream reproducing unit 232 is transferred to the demodulation controller 231. If m is4 or 2 at Step 303, the demodulation controller 231 triggers demodulation of 4 PSK or 2 PSK at Step 313. If not, the procedure moves

to Step 310. At Step 305, two threshold values TH_8 and TH_{16} are calculated. The threshold value TH_{16} for AM demodulation is fed at Step 306 from the demodulation controller 231 to both the first 136 and the second discrimination/reproduction circuit 137. Hence, demodulation of the modified 16 QAM signal and reproduction of the second data stream can be carried out at Steps 307 and 315 respectively. At Step 308, the error rate is examined and if high, the procedure returns to Step 313 for repeating the 4 PSK demodulation.

[0087] As shown in Fig. 22, the signal points 85, 83, are aligned on a line at an angle of $\cos(\omega t+n\pi/2)$ while 84 and 86 are off the line. Hence, the feedback of a second data stream transmitting carrier wave data from the second data stream reproducing unit 233 to a carrier reproducing circuit 131 is carried out so that no carrier needs to be extracted at the timing of the signal points 84 and 86.

[0088] The transmitter 1 is arranged to transmit carrier timing signals at intervals of a given time with the first data stream for the purpose of compensation for no demodulation of the second data stream. The carrier timing signal enables to identify the signal points 83 and 85 of the first data stream regardless of demodulation of the second data stream. Hence, the reproduction of carrier wave can be triggered by the transmitting carrier data to the carrier reproducing circuit 131.

[0089] It is then examined at Step 304 of the flow chart of Fig. 24 whether m is 16 or not upon receipt of such a modified 64 QAM signal as shown in Fig. 23. At Step 310, it is also examined whether m is more than 64 or not. If it is determined at Step 311 that the received signal has no equal distance signal point constellation, the procedure goes to Step 312. The signal point distance TH_{64} of the modified 64 QAM signal is calculated from:

$$TH_{64} = (A_1+A_2/2)/(A_1+A_2)$$

This calculation is equivalent to that of TH_{16} but its resultant distance between signal points is smaller.

[0090] If the signal point distance in the first sub segment 181 is A_3, the distance between the first 181 and the second sub segment 182 is expressed by (A_2-2A_3). Then, the average distance is $(A_2-2A_3)/(A_1+A_2)$ which is designated as d_{64}. When d_{64} is smaller than T_2 which represents the signal point. discrimination capability of the second receiver 33, any two signal points in the segment will hardly be distinguished from each other. This judgement is executed at Step 313. If d_{64} is out of a permissive range, the procedure moves back to Step 313 for 4 PSK mode demodulation. If d_{64} is within the range, the procedure advances to Step 305 for allowing the demodulation of 16 QAM at Step 307. If it is determined at Step 308 that the error rate is too high, the procedure goes back to Step 313 for 4 PSK mode demodulation.

[0091] When the transmitter 1 supplied a modified 8 QAM signal such as shown in Fig. 25(a) in which all the signal points are at angles of $\cos(2\pi f+n\cdot\pi/4)$, the carrier waves of the signal are lengthened to the same phase and will thus be' reproduced with much ease. At the time, two-bit data of the first data stream are demodulated with the 4-PSK receiver while one-bit data of the second data stream is demodulated with the second receiver 33 and the total of three-bit data can be reproduced.

[0092] The third receiver 43 will be described in more detail. Fig. 26 shows a block diagram of the third receiver 43 similar to that of the second receiver 33 in Fig. 21. The difference is that a third data stream reproducing unit 234 is added and also, the discrimination/reproduction circuit has a capability of identifying eight-bit data. The antenna 42 of the third receiver 43 has a radius r_3 greater than r_2 thus allowing smaller distance state signals, e.g. 32- or 64-state QAM signals, to be demodulated. For demodulation of the 64 QAM signal, the first discrimination/reproduction circuit 136 has to identify 8 digital levels of the detected signal in which seven different threshold levels are involved. As one of the threshold values is zero, three are contained in the first quadrant.

[0093] Fig. 27 shows a space diagram of the signal in which the first quadrant contains three different threshold values.

[0094] As shown in Fig. 27, when the three normalized threshold values are $TH1_{64}$, $TH2_{64}$, and $TH3_{64}$, they are expressed by:

$$TH1_{64} = (A_1+A_3/2)/(A_1+A_2)$$

$$TH2_{64} = (A_1+A_2/2)/(A_1+A_2)$$

and

$$TH3_{64} = (A_1+A_2-A_3/2)/(A_1+A_2).$$

[0095] Through AM demodulation of a phase detected signal using the three threshold values, the third data stream can be reproduced like the first and second data stream explained with Fig. 21. The third data stream contains e.g. four signal points 201, 202, 203, 204 at the first sub segment 181 shown in Fig. 23 which represent 4 values of two-bit pattern. Hence, six digits or modified 64 QAM signals can be demodulated.

[0096] The demodulation controller 231 detects the value m, A_1, A_2, and A_3 from the demodulation data contained in the first data stream demodulated at the first data stream reproducing unit 232 and calculates the three threshold values $TH1_{64}$, $TH2_{64}$, and $TH3_{64}$ which are then fed to the first 136 and the second discrimination/reproduction circuit 137 so that the modified 64 QAM signal is demodulated with certainty. Also, if the democulation data have been scrambled, the modified

64 QAM signal can be demodulated only with a specific or subscriber receiver. Fig. 28 is a flow chart showing the action of the demodulation controller 231 for modified 64 QAM signals. The difference from the flow chart for demodulation of 16 QAM shown in Fig. 24 will be explained. The procedure moves from Step 304 to Step 320 where it is examined whether m=32 or not. If m=32, demodulation of 32 QAM signals is executed at Step 322. If not, the procedure moves to Step 321 where it is examined whether m=64 or not. If yes, A_3 is examined at Step 323. If A_3 is smaller than a predetermined value, the procedure moves to Step 305 and the same sequence as of Fig. 24 is implemented. If it is judged at Step 323 that A_3 is not smaller than the predetermined value, the procedure goes to Step 324 where the threshold values are calculated. At Step 325, the calculated threshold values are fed to the first and second discrimination/reproduction circuits and at Step 326, the demodulation of the modified 64 QAM signal is carried out. Then, the first, second, and third data streams are reproduced at Step 327. At Step 328, the error rate is examined. If the error rate is high, the procedure moves to Step 305 where the 16 QAM demodulation is repeated and if low, the demodulation of the 64 QAM is continued.

[0097] The action of carrier wave reproduction needed for execution of a satisfactory demodulating procedure will now be described. The scope of the present invention includes reproduction of the first data stream of a modified 16 or 64 QAM signal with the use of a 4 PSK receiver. However, a common 4 PSK receiver rarely reconstructs carrier waves, thus failing to perform a correct demodulation. For compensation, some arrangements are necessary at both the transmitter and receiver sides.

[0098] Two techniques for the compensation are provided according to the present invention. A first technique relates to transmission of signal points aligned at angles of $(2n-1)\pi/4$ at intervals of a given time. A second technique offers transmission of signal points arranged at intervals of an angle of $n\pi/8$.

[0099] According to the first technique, the eight signal points including 83 and 85 are aligned at angles of $\pi/4$, $3\pi/4$, $5\pi/4$, and $7\pi/4$, as shown in Fig. 38. In action, at least one of the eight signal points is transmitted during sync time slot periods 452, 453, 454, 455 arranged at equal intervals of a time in a time slot gap 451 shown in the time chart of Fig. 38. Any desired signal points are transmitted during the other time slots. The transmitter 1 is also arranged to assign a data for the time slot interval to the sync timing data region 499 of a sync data block, as shown in Fig. 41.

[0100] The content of a transmitting signal will be explained in more detail referring to Fig. 41. The time slot group 451 containing the sync time slots 452, 453, 454, 455 represents a unit data stream or block 491 carrying a data of Dn.

[0101] The sync time slots in the signal are arranged at equal intervals of a given time determined by the time slot interval or sync timing data. Hence, when the arrangement of the sync time slots is detected, reproduction of carrier waves will be executed slot by slot through extracting the sync timing data from their respective time slots.

Such a sync timing data S is contained in a sync block 493 accompanied at the front end of a data frame 492, which is consisted of a number of the sync time slots denoted by the hatching in Fig. 41. Accordingly, the data to be extracted for carrier wave reproduction are increased, thus allowing the 4 PSK receiver to reproduce desired carrier waves at higher accuracy and efficiency.

[0102] The sync block 493 comprises sync data regions 496, 497, 498,---containing sync data S1, S2, S3,---respectively which include unique words and demodulation data. The phase sync signal assignment region 499 is accompanied at the end of the sync block 493, which holds a data of I_T including information about interval arrangement and assignment of the sync time slots.

[0103] The signal point data in the phase sync time slot has a particular phase and can thus be reproduced by the 4 PSK receiver. Accordingly, I_T in the phase sync signal assignment region 499 can be retrieved without error thus ensuring the reproduction of carrier waves at accuracy.

[0104] As shown in Fig. 41, the sync block 493 is followed by a demodulation data block 501 which contains democulation data about threshold voltages needed for demodulation of the modified multiple-bit QAM signal. This data is essential for demodulation of the multiple-bit QAM signal and may preferably be contained in a region 502 which is a part of the sync block 493 for ease of retrieval.

[0105] Fig. 42 shows the assignment of signal data for transmission of burst form signals through a TDMA method.

[0106] The assignment is distinguished from that of Fig. 41 by the fact that a guard period 521 is inserted between any two adjacent Dn data blocks 491, 491 for interruption of the signal transmission. Also, each data block 491 is accompanied at front end a sync region 522 thus forming a data block 492. During the sync region 522, the signal points at a phase of $(2n-1)\pi/4$ are only transmitted. Accordingly, the carrier wave reproduction will be feasible with the 4 PSK receiver. More specifically, the sync signal and carrier waves can be reproduced through the TDMA method.

[0107] The carrier wave reproduction of the first receiver 23 shown in Fig. 19 will be explained in more detail referring to Figs. 43 and 44. As shown in Fig. 43, an input signal is fed through the input unit 24 to a sync detector circuit 541 where it is sync detected. A demodulated signal from the sync detector 541 is transferred to an output circuit 542 for reproduction of the first data stream. A data of the phase sync signal assignment data region 499 (shown in Fig. 41) is retrieved with an extracting timing controller circuit 543 so that the timing of

sync signals of (2n-1)π/4 data can be acknowledged and transferred as a phase sync control pulse 561 shown in Fig. 44 to a carrier reproduction controlling circuit 544. Also, the demodulated signal of the sync . detector circuit 541 is fed to a frequency multiplier circuit 545 where it is 4x multiplied prior to transmitted to the carrier reproduction controlling circuit 544. The resultant signal denoted by 562 in Fig. 44 contains a true phase data 563 and other data. As illustrated in a time chart 564 of Fig. 44, the phase sync time slots 452 carrying the (2n-1)π/4 data are also contained at equal intervals. At the carrier reproducing controlling circuit 544, the signal 562 is sampled by the phase sync control pulse 561 to produce a . phase sample signal 565 which is then converted through sample-hold action to a phase signal 566. The phase signal 566 of the carrier reproduction controlling circuit 544 is fed across a loop filter 546 to a VCO 547 where its relevant carrier wave is reproduced. The reproduced carrier is then sent to the sync detector circuit 541.

[0108] In this manner, the signal point data of the (2n-1)π/4 phase denoted by the shaded areas in Fig. 39 is recovered and utilized so that a correct carrier wave can be reproduced by 4x or 16x frequency multiplication. Although a plurality of phases are reproduced at the time, the absolute phases of the carrier can be successfully be identified with the used of a unique word assigned to the sync region 496 shown in Fig. 41.

[0109] For transmission of a modified 64 QAM signal such as shown in Fig. 40, signal points in the phase sync areas 471 at the (2n-1)π/4 phase denoted by the hatching are assigned to the sync time slots 452, 452b, etc. Its carrier can be reproduced hardly with a common 4 PSK receiver but successfully with the first receiver 23 of 4 PSK mode provided with the carrier reproducing circuit of the embodiment.

[0110] The foregoing carrier reproducing circuit is of COSTAS type. A carrier reproducing circuit of reverse modulation type will now be explained according to the embodiment.

[0111] Fig. 45 shows a reverse modulation type carrier reproducing circuit according to the present invention, in which a received signal is fed from the input unit 24 to a sync detector circuit 541 for producing a demodulated signal. Also, the input signal is delayed by a first delay circuit 591 to a delay signal. The delay signal is then transferred to a quadrature phase modulator circuit 592 where it is reverse demodulated by the demodulated signal from the sync detector circuit 541 to a carrier signal. The carrier signal is fed through a carrier reproduction controller circuit 544 to a phase comparator 593. A carrier wave produced by a VCO 547 is delayed by a second delay circuit 594 to a delay signal which is also fed to the phase comparator 593. At the phase comparator 594, the reverse demodulated carrier signal is compared in phase with the delay signal thus producing a phase difference signal. The phase difference signal sent through a loop filter 546 to the VCO 547 which in turn produces a carrier wave arranged in phase with the received carrier wave. In the same manner as of the COSTAS carrier reproducing circuit shown in Fig. 43, an extracting timing controller circuit 543 performs sampling of signal points contained in the hatching areas of Fig. 39. Accordingly, the carrier wave of a 16 or 64 QAM signal can be reproduced with the 4 PSK demodulator of the first receiver 23.

[0112] The reproduction of a carrier wave by 16x frequency multiplication will be explained. The transmitter 1 shown in Fig. 1 is arranged to modulate and transmit a modified 16 QAM signal with assignment of its signal points at nπ/8 phase as shown in Fig. 46. At the first receiver 23 shown in Fig. 19, the carrier wave can be reproduced with its COSTAS carrier reproduction controller circuit containing a 16x multiplier circuit 661 shown in Fig. 48. The signal points at each nπ/8 phase shown in Fig. 46 are processed at the first quadrant b the action of the 16x multiplier circuit 661, whereby the carrier will be reproduced by the combination of a loop filter 546 and a VCO 541. Also, the absolute phase may be determined from 16 different phases by assigning a unique word to the sync region.

[0113] The arrangement of the 16x multiplier circuit will be explained referring to Fig. 48. A sum signal and a difference signal are produced from the demodulated signal by an adder circuit 662 and a subtracter circuit 663 respectively and then, multiplied each other by a multiplier 664 to a cos 2θ signal. Also, a multiplier 665 produces a sin 2θ signal. The two signals are then multiplied by a multiplier 666 to a sin 4θ signal.

[0114] Similarly, a sin 8θ signal is produced from the two, sin 2θ and cos 2θ, signals by the combination of an adder circuit 667, a subtracter circuit 668, and a multiplier 670. Furthermore, a sin 16θ signal is produced by the combination of an adder circuit 671, a subtracter circuit 672, and a multiplier 673. Then, the 16x multiplication is completed.

[0115] Through the foregoing 16x multiplication, the carrier wave of all the signal points of the modified 16 QAM signal shown in Fig. 46 will successfully be reproduced without extracting particular signal points.

[0116] However, reproduction of the carrier wave of the modified 64 QAM signal shown in Fig. 47 can involve an increase in the error rate due to dislocation of some signal points from the sync areas 471.

[0117] Two techniques are known for compensation for the consequences. One is inhibiting transmission of the signal points dislocated from the sync areas. This causes the total amount of transmitted data to be reduced but allows the arrangement to be facilitated. The other is providing the sync time slots as described in Fig. 36. In more particular, the signal points in the nπ/8 sync phase areas, e.g. 471 and 471a, are transmitted during the period of the corresponding sync time slots in the time slot group 451. This triggers an accurate synchronizing action during the period thus minimizing phase error.

[0118] As now understood, the 16x multiplication allows the simple 4 PSK receiver to reproduce the carrier wave of a modified 16 or 64 QAM signal. Also, the insertion of the sync time slots causes the phasic accuracy to be increased during the reproduction of carrier waves from a modified 64 QAM signal.

[0119] As set forth above, the signal transmission system of the present invention is capable of transmitting a plurality of data on a single carrier wave simultaneously in the multiple signal level arrangement.

[0120] More specifically, three different level receivers which have discrete characteristics of signal intercepting sensitivity and demodulating capability are provided in relation to one single transmitter so that any one of them can be selected depending on a wanted data size to be demodulated which is proportional to the price. When the first receiver of low resolution quality and low price is acquired together with a small antenna, its owner can intercept and reproduce the first data stream of a transmission signal. When the second receiver of medium resolution quality and medium price is acquired together with a medium antenna, its owner can intercept and reproduce both the first and second data streams of the signal. When the third receiver of high resolution quality and high price is acquired with a large antenna, its owner can intercept and reproduce all the first, second, and third data streams of the signal.

[0121] If the first receiver is a home-use digital satellite broadcast receiver of low price, it will overwhelmingly be welcome by a majority of viewers. The second receiver accompanied with the medium antenna costs more and will be accepted by not common viewers but particular people who wants to enjoy HDTV services. The third receiver accompanied with the large antenna at least before the satellite output is increased, is not appropriated for home use and will possibly be used in relevant industries. For example, the third data stream carrying super HDTV signals is transmitted via a satellite to subscriber cinemas which can thus play video tapes rather than traditional movie films and run movies business at low cost.

[0122] When the present invention is applied to a TV signal transmission service, three different quality pictures are carried on one signal channel wave and will offer compatibility with each other. Although the first embodiment refers to a 4 PSK, a modified 8 QAM, a modified 16 QAM, and a modified 64 QAM signal, other signals will also be employed with equal success including a 32 QAM, a 256 QAM, an 8 PSK, a 16 PSK, a 32 PSK signal. It would be understood that the present invention is not limited to a satellite transmission system and will be applied to a terrestrial communications system or a cable transmission system.

Embodiment 2

[0123] A second embodiment of the present invention is featured in which the physical multi-level arrangement of the first embodiment is divided into small levels through e.g. discrimination in error correction capability, thus forming a logic multi-level construction. In the first embodiment, each multi-level channel has different levels in the electric signal amplitude or physical demodulating capability. The second embodiment offers different levels in the logic reproduction capability such as error correction. For example, the data D_1 in a multi-level channel is divided into two, $D_{1\text{-}1}$ and $D_{1\text{-}2}$, components and $D_{1\text{-}1}$ is more increased in the error correction capability than $D_{1\text{-}2}$ for discrimination. Accordingly, as the error detection and correction capability is different between $D_{1\text{-}1}$ and $D_{1\text{-}2}$ at demodulation, $D_{1\text{-}1}$ can successfully be reproduced within a given error rate when the C/N level of an original transmitting signal is as low as disenabling the reproduction of $D_{1\text{-}2}$. This will be implemented using the logic multi-level arrangement.

[0124] More specifically, the logic multi-level arrangement is consisted of dividing data of a modulated multi-level channel and discriminating distances between error correction codes by mixing error correction codes with product codes for varying error correction capability. Hence, a more multi-level signal can be transmitted.

[0125] In fact, a D_1 channel is divided into two sub channels $D_{1\text{-}1}$ and $D_{1\text{-}2}$ and a D_2 channel is divided into two sub channels $D_{2\text{-}1}$ and $D_{2\text{-}2}$.

[0126] This will be explained in more detail referring to Fig. 87 in which $D_{1\text{-}1}$ is reproduced from a lowest C/N signal. If the C/N rate is d at minimum, three components $D_{1\text{-}2}$, $D_{2\text{-}1}$ and $D_{2\text{-}2}$ cannot be reproduced while $D_{1\text{-}1}$ is reproduced. If C/N is not less than c, $D_{1\text{-}2}$ can also be reproduced. Equally, when C/N is b, $D_{2\text{-}1}$ is reproduced and when C/N is a, $D_{2\text{-}2}$ is reproduced. As the C/N rate increases, the reproducible signal levels are increased in number. The lower the C/N, the fewer the reproducible signal levels. This will be explained in the form of relation between transmitting distance and reproducible C/N value referring to Fig. 86. In common, the C/N value of a received signal is decreased in proportion to the distance of transmission as expressed by the real line 861 in Fig. 86. It is now assumed that the distance from a transmitter antenna to a receiver antenna is La when C/N=a, Lb when C/N=b, Lc when C/N=c, Ld when C/N=d, and Le when C/N=e. If the distance from the transmitter antenna is greater than Ld, $D_{1\text{-}1}$ can be reproduced as shown in Fig. 85 where the receivable area 862 is denoted by the hatching. In other words, $D_{1\text{-}1}$ can be reproduced within a most extended area. Similarly, $D_{1\text{-}2}$ can be reproduced in an area 863 when the distance is not more than Lc. In this area 863 containing the area 862, $D_{1\text{-}1}$ can with no doubt be reproduced. In a small area 864, $D_{2\text{-}1}$ can be reproduced and in a smallest area 865, $D_{2\text{-}2}$ can be reproduced. As understood, the different data levels of a channel can be reproduced corresponding to degrees of declination in the C/N rate. The logic multi-level arrangement of the signal transmission system of the present invention can provide the same effect as of a traditional analogue transmission

system in which th amount of receivable data is gradually lowered as the C/N rate decreases.

[0127] The construction of the logic multi-level arrangement will be described in which there are provided two physical levels and two logic levels. Fig. 87 is a block diagram of a transmitter 1 which is substantially identical in construction to that shown in Fig. 2 and described previously in the first embodiment and will no further be explained in detail. The only difference is that error correction code encoders are added as abbreviated to ECC encoders. The divider circuit 3 has four outputs 1-1, 1-2, 2-1, and 2-2 through which four signals D_{1-1}, D_{1-2}, D_{2-1}, and D_{2-2} divided from an input signal are delivered. The two signals D_{1-1} and D_{1-2} are fed to two, main and sub, ECC encoders 872a, 873a of a first ECC encoder 871a respectively for converting to error correction code forms.

[0128] The main ECC encoder 872a has a higher error correction capability than that of the sub ECC encoder 873a. Hence, D_{1-1} can be reproduced at a lower rate of C/N than D_{1-2} as apparent from the CN-level diagram of Fig. 85. More particularly, the logic level of D_{1-1} is less affected by declination of the C/N than that of D_{1-2}. After error correction code encoding, D_{1-1} and D_{1-2} are summed by a summer 874a to a D_1 signal which is then transferred to the modulator 4. The other two signals D_{2-1} and D_{2-2} of the divider circuit 3 are error correction encoded by two, main and sub, ECC encoders 872b, 873b of a second ECC encoder 871b respectively and then, summed by a summer 874b to a D_2 signal which is transmitted to the modulator 4. The main ECC encoder 872b is higher in the error correction capability than the sub ECC encoder 873b. The modulator 4 in turn produces from the two, D_1 and D_2, input signals a multi-level modulated signal which is further transmitted from the transmitter unit 5. As understood, the output signal from the transmitter 1 has two physical levels D_1 and D_2 and also, four logic levels D_{1-1}, D_{1-2}, D_{2-1}, and D_{2-2} based on the two physical levels for providing different error correction capabilities.

[0129] The reception of such a multi-level signal will be explained. Fig. 88 is a block diagram of a second receiver 33 which is almost identical in construction to that shown in Fig. 21 and described in the first embodiment. The second receiver 33 arranged for intercepting multi-level signals from the transmitter 1 shown in Fig. 87 further comprises a first 876a and a second ECC decoder 876b, in which the demodulation of QAM, or any of ASK, PSK, and FSK if desired, is executed.

[0130] As shown in Fig. 88, a receiver signal is demodulated by the demodulator 35 to the two, D_1 and D_2, signals which are then fed to two dividers 3a and 3b respectively where they are divided into four logic levels D_{1-1}, D_{1-2}, D_{2-1}, and D_{2-2}. The four signals are transferred to the first 876a and the second ECC decoder 876b in which D_{1-1} is error corrected by a main ECC decoder 877a, D_{1-2} by a sub ECC decoder 878a, D_{2-1} by a main ECC decoder 877b, D_{2-2} by a sub ECC decoder 878b before all sent to the summer 37. At the summer 37, the four, D_{1-1}, D_{1-2}, D_{2-1}, and D_{2-2}, error corrected signals are summed to a signal which is then delivered from the output unit 36.

[0131] Since D_{1-1} and D_{2-1} are higher in the error correction capability than D_{1-2} and D_{2-2} respectively, the error rate remains less than a given value although C/N is fairly low as shown in Fig. 85 and thus, an original signal will be reproduced successfully.

[0132] The action of discriminating the error correction capability between the main ECC decoders 877a, 877b and the sub ECC decoders 878a, 878b will now be described in more detail. It is a good idea for having a difference in the error correction capability to use in the sub ECC decoder a common coding technique, e.g. Reed-Solomon or BCH method, having a standard code distance and in the main ECC decoder, another encoding technique in which the distance between correction codes is increased using Reed-Solomon codes, their product codes, or other long-length codes. A variety of known techniques for increasing the error correction code distance have been introduced and will no more explained. The present invention can be associated with any known technique for having the logic multi-level arrangement.

[0133] The logic multi-level arrangement will be explained in conjunction with a diagram of Fig. 89 showing the relation between C/N and error rate after error correction. As shown, the straight line 881 represents D_{1-1} at the C/N and error rate relation and the line 882 represents D_{1-2} at same.

[0134] As the C/N rate of an input signal decreases, the error rate increases after error correction. If C/N is lower than a given value, the error rate exceeds a reference value Eth determined by the system design standards and no original data will normally be reconstructed. When C/N is lowered to less than e, the D_1 signal fails to be reproduced as expressed by the line 881 of D_{1-1} in Fig. 89. When e≤C/N<d, D_{1-1} of the D_1 signal exhibits a higher error rate than Eth and will not be reproduced.

[0135] When C/N is d at the point 885d, D_{1-1} having a higher error correction capability than D_{1-2} becomes not higher in the error rate than Eth and can be reproduced. At the time, the error rate of D_{1-2} remains higher than Eth after error correction and will no longer be reproduced.

[0136] When C/N is increased up to c at the point 885c, D_{1-2} becomes not higher in the error rate than Eth and can be reproduced. At the time, D_{2-1} and D_{2-2} remain in no demodulation state. After the C/N rate is increased further to b', the D_2 signal becomes ready to be demodulated.

[0137] When C/N is increased to b at the point 885b, D_{2-1} of the D_2 signal becomes not higher in the error rate than Eth and can be reproduced. At the time, the error rate of D_{2-2} remains higher than Eth and will not be reproduced. When C/N is increased up to a at the point

885a, $D_{2\text{-}2}$ becomes not higher than Eth and can be reproduced.

[0138] As described above, the four different signal logic levels divided from two, D_1 and D_2, physical levels through discrimination of the error correction capability between the levels, can be transmitted simultaneously.

[0139] Using the logic multi-level arrangement of the present invention in accompany with a multi-level construction in which at least a part of the original signal is reproduced even if data in a higher level is lost, digital signal transmission will successfully be executed without losing the advantageous effect of an analogue signal transmission in which transmitting data is gradually decreased as the C/N rate becomes low.

[0140] Thanking to up-to-data image data compression techniques, compressed image data can be transmitted in the logic multi-level arrangement for enabling a receiver station to reproduce a higher quality image than that of an analogue system and also, with not sharply but at steps declining the signal level for ensuring signal interception in a wider area. The present invention can provide an extra effect of the multi-layer arrangement which is hardly implemented by a known digital signal transmission system without deteriorating high quality image data.

Embodiment 3

[0141] A third embodiment of the present invention will be described referring to the relevant drawings.

[0142] Fig. 29 is a schematic total view illustrating the third embodiment in the form of a digital TV broadcasting system. An input video signal 402 of super high resolution TV image is fed to an input unit 403 of a first video encoder 401. Then, the signal is divided by a divider circuit 404 into three, first, second, and third, data streams which are transmitted to a compressing circuit 405 for data compression before further delivered.

[0143] Equally, other three input video signals 406, 407, and 408 are fed to a second 409, a third 410, and a fourth video encoder 411 respectively which all are arranged identical in construction to the first video encoder 401 for data compression.

[0144] The four first data streams from their respective encoders 401, 409, 410, 411 are transferred to a first multiplexer 413 of a multiplexer 412 where they are time multiplexed by TDM process to a first data stream multiplex signal which is fed to a transmitter 1.

[0145] Apart or all of the four second data streams from their respective encoders 401, 409, 410, 411 are transferred to a second multiplexer 414 of the multiplexer 412 where they are time multiplexed to a second data stream multiplex signal which is then fed to the transmitter 1. Also, a part or all of the four third data streams are transferred to a third multiplexer 415 where they are time multiplexed to a third data stream multiplex signal which is then fed to the transmitter 1.

[0146] The transmitter 1 performs modulation of the three data stream signals with its modulator 4 by the same manner as described in the first embodiment. The modulated signals are sent from a transmitter unit 5 through an antenna 6 and an uplink 7 to a transponder 12 of a satellite 10 which in turn transmits it to three different receivers including a first receiver 23.

[0147] The modulated signal transmitted through a downlink 21 is intercepted by a small antenna 22 having a radius r_1 and fed to a first data stream reproducing unit 232 of the first receiver 23 where its first data stream only is demodulated. The demodulated first data stream is then converted by a first video decoder 421 to a traditional 425 or wide-picture NTSC or video output signal 426 of low image resolution.

[0148] Also, the modulated signal transmitted through a downlink 31 is intercepted by a medium antenna 32 having a radius r_2 and fed to a first 232 and a second data stream reproducing unit 233 of a second receiver 33 where its first and second data streams are demodulated respectively. The demodulated first and second data streams are then summed and converted by a second video decoder 422 to an HDTV or video output signal 427 of high image resolution and/or to the video output signals 425 and 426.

[0149] Also, the modulated signal transmitted through a downlink 41 is intercepted by a large antenna 42 having a radius r_3 and fed to a first 232, a second 233, and a third data stream reproducing unit 234 of a third receiver 43 where its first, second, and third data streams are demodulated respectively. The demodulated first, second, and third data streams are then summed and converted by a third video decoder 423 to a super HDTV or video output signal 428 of super high image resolution for use in a video theater or cinema. The video output signals 425, 426, and 427 can also be reproduced if desired. A common digital TV signal is transmitted from a conventional digital transmitter 51 and when intercepted by the first receiver 23, will be converted to the video output signal 426 such as a low resolution NTSC TV signal.

[0150] The first video encoder 401 will now be explained in more detail referring to the block diagram of Fig. 30. An input video signal of super high resolution is fed through the input unit 403 to the divider circuit 404 where it is divided into four components by sub-band coding process. In more particular, the input video signal is separated through passing a horizontal lowpass filer 451 and a horizontal highpass filter 452 of e.g. QMF mode to two, low and high, horizontal frequency components which are then subsampled to a half of their quantities by two subsamplers 453 and 454 respectively. The low horizontal component is filtered by a vertical lowpass filter 455 and a vertical highpass filter 456 to a low horizontal low vertical component or H_LV_L signal and a low horizontal high vertical component or H_LV_H signal respectively. The two, H_LV_L and H_LV_H, signals are then subsampled to a half by two subsamplers 457 and 458 respectively and transferred to the compressing cir-

cuit 405.

[0151] The high horizontal component is filtered by a vertical lowpass filter 459 and a vertical highpass filter 460 to a high horizontal low vertical component or H_HV_L signal and a high horizontal high vertical component or H_HV_H signal respectively. The two, H_HV_L and H_HV_H, signals are then subsampled to a half by two subsamplers 461 and 462 respectively and transferred to the compressing circuit 405.

[0152] H_LV_L signal is preferably DCT compressed by a first compressor 471 of the compressing circuit 405 and fed to a first output 472 as the first data stream.

[0153] Also, H_LV_H signal is compressed by a second compressor 473 and fed to a second output 464. H_HV_L signal is compressed by a third compressor 463 and fed to the second output 464.

[0154] H_HV_H signal is divided by a divider 465 into two, high resolution (H_HV_H1) and super high resolution (H_HV_H2), video signals which are then transferred to the second output 464 and a third output 468 respectively.

[0155] The first video decoder 421 will now be explained in more detail referring to Fig. 31. The first data stream or D_1 signal of the first receiver 23 is fed through an input unit 501 to a descrambler 502 of the first video decoder 421 where it is descrambled. The descrambled D_1 signal is expanded by an expander 503 to H_LV_L which is then fed to an aspect ratio changing circuit 504. Thus, H_LV_L signal can be delivered through an output unit 505 as a standard 500, letterbox format 507, widescreen 508, or sidepanel format NTSC signal 509. The scanning format may be of non-interlace or interlace type and its NTSC mode lines may be 525 or doubled to 1050 by double tracing. When the received signal from the digital transmitter 51 is a digital TV signal of 4 PSK mode, it can also be converted by the first receiver 23 and the first video decoder 421 to a TV picture. The second video decoder 422 will be explained in more detail referring to the block diagram of Fig. 32. The D_1 signal of the second receiver 33 is fed through a first input 521 to a first expander 522 for data expansion and then, transferred to an oversampler 523 where it is sampled at 2x. The oversampled signal is filtered by a vertical lowpass filter 524 to H_LV_L. Also, the D_2 signal of the second receiver 33 is fed through a second input 530 to a divider 531 where it is divided into three components which are then transferred to a second 532, a third 533, and a fourth expander 534 respectively for data expansion. The three expanded components are sampled at 2x by three oversamplers 535, 536, 537 and filtered by a vertical highpass 538, a vertical lowpass 539, and a vertical highpass filter 540 respectively. Then, H_LV_L from the vertical lowpass filter 524 and H_LV_H from the vertical highpass filter 538 are summed by an adder 525, sampled by an oversampler 541, and filtered by a horizontal lowpass filter 542 to a low frequency horizontal video signal. H_HV_L from the vertical lowpass filter 539 and H_HV_H1 from the vertical highpass filter 540 are summed by an adder 526, sampled by an oversampler 544, and filtered by a horizontal highpass filter 545 to a high frequency horizontal video signal. The two, high and low frequency, horizontal video signal are then summed by an adder 543 to a high resolution video signal HD which is further transmitted through an output unit 546 as a video output 547 of e.g. HDTV format. If desired a traditional NTSC video output can be reconstructed with equal success.

[0156] Fig. 33 is a block diagram of the third video decoder 423 in which the D_1 and D_2 signals are fed through a first 521 and a second input 530 respectively to a high frequency band video decoder circuit 527 where they are converted to an HD signal by the same manner as above described. The D_3 signal is fed through a third input 551 to a super high frequency band video decoder circuit 552 where it is expanded, descrambled, and composed to H_HV_H2 signal. The HD signal of the high frequency band video decoder circuit 527 and the H_HV_H2 signal of the super high frequency band video decoder circuit 552 are summed by a summer 553 to a super high resolution TV or S-HD signal which is then delivered through an output unit 554 as a super resolution video output 555.

[0157] The action of multiplexing in the multiplexer 412 shown in Fig. 29 will be explained in more detail. Fig. 34 illustrates a data assignment in which the three, first, second, and third, data streams D_1, D_2, D_3 contain in a period of T six NTSC channel data L1, L2, L3, L4, L5, L6, six HDTV channel data M1, M2, M3, M4, M5, M6 and six S-HDTV channel data H1, H2, H3, H4, H5, H6 respectively. In action, the NTSC or D_1 signal data L1 to L6 are time multiplexed by TDM process during the period T. More particularly, H_LV_L of D_1 is assigned to a domain 601 for the first channel. Then, a difference data M1 between HDTV and NTSC or a sum of H_LV_H, H_HV_L, and H_HV_H1 is assigned to a domain 602 for the first channel. Also, a difference data H1 between HDTV and super HDTV or H_HV_H2 (See Fig. 30) is assigned to a domain 603 for the first channel.

[0158] The selection of the first channel TV signal will now be described. When intercepted by the first receiver 23 with a small antenna coupled to the first video decoder 421, the first channel signal is converted to a standard or widescreen NTSC TV signal as shown in Fig. 31. When intercepted by the second receiver 33 with a medium antenna coupled to the second video decoder 422, the signal is converted by summing L1 of the first data stream D_1 assigned to the domain 601 and M1 of the second data stream D_2 assigned to the domain 602 to an HDTV signal of the first channel equivalent in program to the NTSC signal.

[0159] When intercepted by the third receiver 43 with a large antenna coupled to the third video decoder 423, the signal is converted by summing L1 of D_1 assigned to the domain 601, M1 of D_2 assigned to the domain 602, and H_1 of D_3 assigned to the domain 603 to a super HDTV signal of the first channel equivalent in program to the NTSC signal. The other channel signals can be

reproduced in an equal manner.

[0160] Fig. 35 shows another data assignment L1 of a first channel NTSC signal is assigned to a first domain 601. The domain 601 which is allocated at the front end of the first data stream D_1, also contains at front a data S11 including a descrambling data and the demodulation data described in the first embodiment. A first channel HDTV signal is transmitted as L1 and M1. M1 which is thus a difference data between NTSC and HDTV is assigned to two domains 602 and 611 of D_2. If L_1 is a compressed NTSC component of 6 Mbps, M1 is as two times higher as 12 Mbps. Hence, the total of L1 and M1 can be demodulated at 18 Mbps with the second receiver 33 and the second video decoder 423. According to current data compression techniques, HDTV compressed signals can be reproduced at about 15 Mbps. This allows the data assignment shown in Fig. 35 to enable simultaneous reproduction of an NTSC and HDTV first channel signal. However, this assignment allows no second channel HDTV signal to be carried. S21 is a descrambling data in the HDTV signal. A first channel super HDTV signal component comprises L1, M1, and H1. The difference data H1 is assigned to three domains 603, 612, and 613 of D_3. If the NTSC signal is 6 Mbps, the super HDTV is carried at as high as 36 Mbps. When a compressed rate is increased, super HDTV video data of about 2000 scanning line for reproduction of a cinema size picture for commercial use can be transmitted with an equal manner.

[0161] Fig. 36 shows a further data assignment in which H1 of a super HDTV signal is assigned to six times domains. If a NTSC compressed signal is 6 Mbps, this assignment can carry as nine times higher as 54 Mbps of D_3 data. Accordingly, super HDTV data of higher picture quality can be transmitted.

[0162] The foregoing data assignment makes the use of one of two, horizontal and vertical, polarization planes of a transmission wave. When both the horizontal and vertical polarization planes are used, the frequency utilization will be doubled. This will be explained below.

[0163] Fig. 49 shows a data assignment in which D_{V1} and D_{H1} are a vertical and a horizontal polarization signal of the first data stream respectively, D_{V2} and D_{H2} are a vertical and a horizontal polarization signal of the second data stream respectively, and D_{V3} and D_{H3} are a vertical and a horizontal polarization signal of the third data stream respectively. The vertical polarization signal D_{V1} of the first data stream carries a low frequency band or NTSC TV data and the horizontal polarization signal D_{H1} carries a high frequency band or HDTV data. When the first receiver 23 is equipped with a vertical polarization antenna, it can reproduce only the NTSC signal. When the first receiver 23 is equipped with an antenna for both horizontally and vertically polarized waves, it can reproduce the HDTV signal through summing L1 and M1. More specifically, the first receiver 23 can provide compatibility between NTSC and HDTV with the use of a particular type antenna.

[0164] Fig. 50 illustrates a TDMA method in which each data burst 721 is accompanied at front a syne data 731 and a card data 741. Also, a frame sync data 720 is provided at the front of a fame. Like channels are assigned to like time slots. For example, a first time slot 750 carries NTSC, HDTV, and super HDTV data of the first channel simultaneously. The six time slots 750, 750a, 750b, 750c, 750d, 750e are arranged independent from each other. Hence, each station can offer NTSC, HDTV, and/or supper HDTV services independently of the other stations through selecting a particular channel of the time slots. Also, the first receiver 23 can reproduce an NTSC signal when equipped with a horizontal polarization antenna and both NTSC and HDTV signals when equipped with a compatible polarization antenna. In this respect, the second receiver 33 can reproduce a super HDTV at lower resolution while the third receiver 43 can reproduce a full super HDTV signal. According to the third embodiment, a compatible signal transmission system will be constructed. It is understood that the data assignment is not limited to the burst mode TDMA method shown in Fig. 50 and another method such as time division multiplexing of continuous signals as shown in Fig. 49 will be employed with equal success. Also, a data assignment shown in Fig. 51 will permit a HDTV signal to be reproduced at high resolution.

[0165] As set forth above, the compatible digital TV signal transmission system of the third embodiment can offer three, super HDTV, HDTV, and conventional NTSC, TV broadcast services simultaneously. In addition, a video signal intercepted by a commercial station or cinema can be electronized.

[0166] The modified QAM of the embodiments is now termed as SRQAM and its error rate will be examined.

[0167] First, the error rate in 16 SRQAM will be calculated. Fig. 99 shows a vector diagram of 16 SRQAM signal points. As apparent from the first quadrant, the 16 signal points of standard 16 QAM including 83a, 83b, 84a, 83a are allocated at equal intervals of 2δ.

[0168] The signal point 83a is spaced δ from both the I-axis and the Q-axis of the coordinate. It is now assumed that n is a shift value of the 16 SRQAM. In 16 SRQAM, the signal point 83a of 16 QAM is shifted to a signal point 83 where the distance from each axis is $n\delta$. The shift value n is thus expressed as:

$$0<n<3.$$

[0169] The other signal points 84a and 86a are also shifted to two points 84 and 86 respectively.

[0170] If the error rate of the first data stream is Pe_1, it is obtained from:

$$Pe_{1\text{-}16} = \frac{1}{4}\left(\mathrm{erfc}\left(\frac{n\delta}{\sqrt{2\sigma}}\right) + \mathrm{erfc}\left(\frac{3\delta}{\sqrt{2\sigma}}\right)\right.$$

$$= \frac{1}{8}\,\mathrm{erfc}\left(\frac{n\sqrt{\rho}}{\sqrt{9+n^2}}\right)$$

Also, the error rate Pe_2 of the second data stream is obtained from:

$$Pe_{2\text{-}16} = \frac{1}{2}\,\mathrm{erfc}\left(\frac{\frac{3\text{-}n}{2}\delta}{\sqrt{2\sigma}}\right)$$

$$= \frac{1}{4}\,\mathrm{erfc}\left(\frac{3\text{-}n}{2\sqrt{9+n^2}}\sqrt{\rho}\right)$$

[0171] The error rate of 36 or 32 SRQAM will be calculated. Fig. 100 is a vector diagram of a 36 SRQAM signal in which the distance between any two 36 QAM signal points is 28.

[0172] The signal point 83a of 36 QAM is spaced δ from each axis of the coordinate. It is now assumed that n is a shift value of the 16 SRQAM. In 36 SRQAM, the signal point 83a is shifted to a signal point 83 where the distance from each axis is $n\delta$. Similarly, the nine 36 QAM signal points in the first quadrant are shifted to points 83, 84, 85, 86, 97, 98, 99, 100, 101 respectively. If a signal point group 90 comprising the nine signal points is regarded as a single signal point, the error rate Pe_1 in reproduction of only the first data stream D_1 with a modified 4 PSK receiver and the error rate Pe_2 in reproduction of the second data stream D_2 after discriminating the nine signal points of the group 90 from each other, are obtained respectively from:

$$Pe_{1\text{-}32} = \frac{1}{6}\,\mathrm{erfc}\left(\frac{n\delta}{\sqrt{2\sigma}}\right)$$

$$= \frac{1}{6}\,\mathrm{erfc}\left(\sqrt{\frac{6\rho}{5}} \times \frac{n}{\sqrt{n^2+2n+25}}\right)$$

$$Pe_{2\text{-}32} = \frac{2}{3}\,\mathrm{erfc}\left(\frac{5\text{-}n}{4\sqrt{2}}\,\frac{\delta}{\rho}\right)$$

$$= \frac{2}{3}\,\mathrm{erfc}\left(\sqrt{\frac{3\rho}{40}} \times \frac{5\text{-}n}{\sqrt{n^2+2n+25}}\right)$$

[0173] Fig. 101 shows the relation between error rate Pe and C/N rate in transmission in which the curve 900 represents a conventional or not modified 32 QAM signal. The straight line 905 represents a signal having $10^{-1.5}$ of the error rate. The curve 901a represents a D_1 level 32 SRQAM signal of the present invention at the shift rate n of 1.5. As shown, the C/N rate of the 32 SRQAM signal is 5 dB lower at the error rate of $10^{-1.5}$ than that of the conventional 32 QAM. This means that the present invention allows a D_1 signal to be reproduced at a given error rate when its C/N rate is relatively low.

[0174] The curve 902a represents a D_2 level SRQAM signal at n=1.5 which can be reproduced at the error rate of $10^{-1.5}$ only when its C/N rate is 2.5 dB higher than that of the conventional 32 QAM of the curve 900. Also, the curves 901b and 902b represent D_1 and D_2 SRQAM signals at n=2.0 respectively. The curves 902c represents a D_2 SRQAM signal at n=2.5. It is apparent that the C/N rate of the SRQAM signal at the error rate of $10^{-1.5}$ is 5dB, 8dB, and 10dB higher at n=1.5, 2.0, and 2.5 respectively in the D_1 level and 2.5 dB lower in the D_2 level than that of a common 32 QAM signal.

[0175] Shown in Fig. 103 is the C/N rate of the first and second data streams D_1, D_2 of a 32 SRQAM signal which is needed for maintaining a constant error rate against variation of the shift n. As apparent, when the shift n is more than 0.8, there is developed a clear difference between two C/N rates of their respective D_1 and D_2 levels so that the multi-level signal, namely first and second data, transmission can be implemented successfully. In brief, n>0.85 is essential for multi-level data transmission of the 32 SRQAM signal of the present invention.

[0176] Fig. 102 shows the relation between the C/N rate and the error rate for 16 SRQAM signals. The curve 900 represents a common 16 QAM signal. The curves 901a, 901b, 901c and D_1 level or first data stream 16 SRQAM signals at n=1.2, 1.5, and 1.8 respectively. The curves 902a, 902b, 902c are D_2 level or second data stream 16 SRQAM signals at n=1.2, 1.5, and 1.8 respectively.

[0177] The C/N rate of the first and second data streams D_1, D_2 of a 16 SRQAM signal is shown in Fig. 104, which is needed for maintaining a constant error rate against variation of the shift n. As apparent, when the shift n is more than 0.9 (n>0.9), the multi-level data transmission of the 16 SRQAM signal will be executed.

[0178] One example of propagation of SRQAM signals of the present invention will now be described for use with a digital TV terrestrial broadcast service. Fig. 105 shows the relation between the signal level and the distance between a transmitter antenna and a receiver antenna in the terrestrial broad cast service. The curve 911 represents a transmitted signal from the transmitter antenna of 1250 feet high. It is assumed that the error rate essential for reproduction of an applicable digital TV signal is $10^{-1.5}$. The hatching area 912 represents a noise interruption. The point 910 represents a signal reception limit of a conventional 32 QAM signal at C/N=15 dB where the distance L is 60 miles and a digital HDTV signal can be intercepted at minimum.

[0179] The C/N rate varies 5 dB under a worse receiving condition such as bad weather. If a change in the relevant condition, e.g. weather, attenuates the C/N rate, the interception of an HDTV signal will hardly be ensured. Also, geographical conditions largely affect the propagation of signals and a decrease of about 10 dB at least will be unavoidable. Hence, successful signal

interception within 60 miles will never be guaranteed and above all, a digital signal will be propagated harder than an analogue signal. It would be understood that the service area of a conventional digital TV broadcast service is less dependable.

[0180] In case of the 32 SRQAM signal of the present invention, three-level signal transmission system is constituted as shown in Figs. 133 and 137. This permits a low resolution NTSC signal of MPEG level to be carried on the 1-1 data stream $D_{1\text{-}1}$, a medium resolution TV data of e.g. NTSC system to be carried on the 1-2 data stream $D_{1\text{-}2}$, and a high frequency component of HDTV data to be carried on the second data stream D_2. Accordingly, the service area of the 1-2 data stream of the SRQAM signal is increased to a 70 mile point 910a while of the second data stream remains within a 55 mile point 910b, as shown in Fig. 105. Fig. 106 illustrates a computer simulation result of the service area of the 32 SRQAM signal of the present invention, which is similar to Fig. 53 but explains in more detail. As shown, the regions 708, 703c, 703a, 703b, 712 represent a conventional 32 QAM receivable area, a 1-1 data level $D_{1\text{-}1}$ receivable area, a 1-2 data level $D_{1\text{-}2}$ receivable area, a second data level D_2 receivable area, and a service area of a neighbor analogue TV station respectively. The conventional 32 QAM signal data used in this drawing is based on a conventionally disclosed one.

[0181] For common 32 QAM signal, the 60-mile-radius service area can be established theoretically. The signal level will however be attenuated by geographical or weather conditions and particularly, considerably declined at near the limit of the service area.

[0182] If the low frequency band TV component of MPEG1 grade is carried on the 1-1 level $D_{1\text{-}1}$ data and the medium frequency band TV component of NTSC grade on the 1-2 level $D_{1\text{-}2}$ data and high frequency band TV component of HDTV on the second level D_2 data, the service area of the 32 SRQAM signal of the present invention is increased by 10 miles in radius for reception of an EDTV signal of medium resolution grade and 18 miles for reception of an LDTV signal of low resolution grade although decreased by 5 miles for reception of an HDTV signal of high resolution grade, as shown in Fig. 106. Fig. 107 shows a service area in case of a shift factor n or s = 1.8. Fig. 135 shows the service area of Fig. 107 in terms of area.

[0183] More particularly, the medium resolution component of a digital TV broadcast signal of the SRQAM mode of the preset invention can successfully be intercepted in an unfavorable service region or shadow area where a conventional medium frequency band TV signal is hardly propagated and attenuated due to obstacles. Within at least the predetermined service area, the NTSC TV signal of the SRQAM mode can be intercepted by any traditional TV receiver. As the shadow or signal attenuating area developed by building structures and other obstacles or by interference of a neighbor analogue TV signal or produced in a low land is decreased to a minimum, TV viewers or subscribers will be increased in number.

[0184] Also, the HDTV service can be appreciated by only a few viewers who afford to have a set of high cost HDTV receiver and display, according to the conventional system. The system of the present invention allows a traditional NTSC, PAL, or SECAM receiver to intercept a medium resolution component of the digital HDTV signal with the use of an additional digital tuner. A majority of TV viewers can hence enjoy the service at less cost and will be increased in number. This will encourage the TV broadcast business and create an extra social benefit.

[0185] Furthermore, the signal receivable area for medium resolution or NTSC TV service according to the present invention is increased about 36% at n=2.5, as compared with the conventional system, As the service area thus the number of TV viewers is increased, the TV broadcast business enjoys an increasing profit. This reduces a risk in the development of a new digital TV business which will thus be encouraged to put into practice.

[0186] Fig. 107 shows the service area of a 32 SRQAM signal of the present invention in which the same effect will be ensured at n=1.8. Two service areas 703a, 703b of D_1 and D_2 signals respectively can be determined in extension for optimum signal propagation by varying the shift n considering a profile of HDTV and NTSC receiver distribution or geographical features. Accordingly, TV viewers will satisfy the service and a supplier station will enjoy a maximum of viewers.

[0187] This advantage is given when:

$$n>1.0$$

Hence, if the 32 SRQAM signal is selected, the shift n is determined by:

$$1<n<5$$

Also, if the 16 SRQAM signal is employed, n is determined by:

$$1<n<3$$

[0188] In the SRQAM mode signal terrestrial broadcast service in which the first and second data levels are created by shifting corresponding signal points as shown in Figs. 99 and 100, the advantage of the present invention will be given when the shift n in a 16, 32, or 64 SRQAM signal is more than 1.0.

[0189] In the above embodiments, the low and high frequency band components of a video signal are transmitted as the first and second data streams. However, the transmitted signal may be an audio signal. In this case, low frequency or low resolution components of an audio signal may be transmitted as the first data stream, and high frequency or high resolution components of the audio signal may be transmitted as the second data stream. Accordingly, it is possible to receive high C/N portion in high sound quality and low C/N portion in low sound quality. This can be utilized in PCM broadcast, radio, portable telephone and the like. In this case, the broadcasting area or communication distance can be

expanded as compared with the conventional systems.

[0190] Furthermore, the third embodiment can incorporate a time division multiplexing (TDM) system as shown in Fig. 133. Utilization of the TDM makes it possible to increase the number of subchannels. An ECC encoder 743a and an ECC encoder 743b, provided in two subchannels, differentiate ECC code gains so as to make a difference between thresholds of these two subchannels. Whereby, an increase of channel number of the multi-level signal transmission can be realized. In this case, it is also possible to provide two Trellis encoders 743a, 743b as shown in Fig. 137 and differentiate their code gains. The explanation of this block diagram is substantially identical to that of later described block diagram of Fig. 131 which shows the sixth embodiment of the present invention and, therefore, will not described here.

[0191] In a simulation of Fig. 106, there is provided 5 dB difference of a coding gain between 1-1 subchannel $D_{1\text{-}1}$ and 1-2 subchannel $D_{1\text{-}2}$.

[0192] An SRQAM is the system applying a C-CDM (Constellation-Code Division Multiplex) of the present invention to a rectangle-QAM. A C-CDM, which is a multiplexing method independent of TDM or FDM, can obtain subchannels by dividing a constellation-code corresponding a code. An increase of the number of codes will bring an expansion of transmission capacity, which is not attained by TDM or FDM alone, while maintaining almost perfect compatibility with conventional communication apparatus. Thus C-CDM can bring excellent effects.

[0193] Although above embodiment combines the C-CDM and the TDM, it is also possible to combine the C-CDM with the FDM (Frequency Division Multiplex) to obtain similar modulation effect of threshold values. Such a system can be used for a TV broadcasting, and Fig. 108 shows a frequency distribution of a TV signal. A spectrum 725 represents a frequency distribution of a conventional analogue, e.g. NTSC, broadcasting signal. The largest signal is a video carrier 722. A color carrier 723 and a sound carrier 724 are not so large. There is known a method of using an FDM for dividing a digital broadcasting signal into two frequencies. In this case, a carrier is divided into a first carrier 726 and a second carrier 727 to transmit a first 720 and a second signal 721 respectively. An interference can be lowered by placing first and second carriers 726, 727 sufficiently far from the video carrier 722. The first signal 720 serves to transmit a low resolution TV signal at a large output level, while the second signal 721 serves to transmit a high resolution TV signal at a small output level. Consequently, the multi-level signal transmission making use of an FDM can be realized without being bothered by obstruction.

[0194] Fig. 134 shows an example of a conventional method using a 32 QAM system. As the subchannel A has a larger output than the subchannel B, a threshold value for the subchannel A, i.e. a threshold 1, can be set small 4~5 dB than a threshold value for the subchannel B, i.e. a threshold 2. Accordingly, a two-level broadcasting having 4~5 dB threshold difference can be realized. In this case, however, a large reduction of signal reception amount will occur if the receiving signal level decreases below the threshold 2. Because the second signal 721a, having a large information amount as shaded in the drawing, cannot be received in such a case and only the first signal 720a, having a small information amount, is received. Consequently, a picture quality brought by the second level will be extremely worse.

[0195] However, the present invention resolves this problem. According to the present invention, the first signal 720 is given by 32 SRQAM mode which is obtained through C-CDM modulation so that the subchannel A is divided into two subchannels 1 of A and 2 of A. The newly added subchannel 1 of A, having a lowest threshold value, carries a low resolution component. The second signal 721 is also given by 32 SRQAM mode, and a threshold value for the subchannel 1 of B is equalized with the threshold 2.

[0196] With this arrangement, the region in which a transmitted signal is not received when the signal level decreases below the threshold 2 is reduced to a shaded portion of the second signal 721a in Fig. 108. As the subchannel 1 of B and the subchannel A are both receivable, the transmission amount is not so much reduced in total. Accordingly, a better picture quality is reproduced even in the second level at the signal level of the threshold 2.

[0197] By transmitting a normal resolution component in one subchannel, it becomes possible to increase the number of multiple level and expand a low resolution service area. This low-threshold subchannel is utilized for transmitting important information such as sound information, sync information, headers of respective data, because these information carried on this low-threshold subchannel can be surely received. Thus stable reception is feasible. If a subchannel is newly added in the second signal 721 in the same manner, the level number of multi-level transmission can be increased in the service area. In the case where an HDTV signal has 1050 scanning lines, an new service area equivalent to 775 lines can be provided in addition to 525 lines.

[0198] Accordingly, the combination of the FDM and the C-CDM realizes an increase of service area. Although above embodiment divides a subchannel into two, it is needless to say it will also be preferable to divide it into three or more.

[0199] Next, a method of avoiding obstruction by combining the TDM and the C-CDM will be explained. As shown in Fig. 109, an analogue TV signal includes a horizontal retrace line portion 732 and a video signal portion 731. This method utilizes a low signal level of the horizontal retrace line portion 732 and non-display of obstruction on a picture plane during this period. By synchronizing a digital TV signal with an analogue TV signal, horizontal retrace line sync slots 733, 733a of the

horizontal retrace line portion 732 can be used for transmission of an important, e.g. a sync, signal or numerous data at a high output level. Thus, it becomes possible to increase data amount or output level without increasing obstruction. The similar effect will be expected even if vertical retrace line sync slots 737, 737a are provided synchronously with vertical retrace line portions 735, 735a.

[0200] Fig. 110 shows a principle of the C-CDM. Furthermore, Fig. 111 shows a code assignment of the C-CDM equivalent to an expanded 16 QAM. Fig. 112 shows a code assignment of the C-CDM equivalent to an expanded 36 QAM. As shown in Figs. 110 and 111, a 256 QAM signal is divided into four, 740a, 740b, 740c, 740d, levels which have 4, 16, 64, 256 segments, respectively. A signal code word 742d of 256 QAM on the fourth level 740d is "11111111" of 8 bit. This is split into four code words 741a, 741b, 741c, and 741d of 2-bit ---- i.e. "11", "11", "11", "11", which are then allocated on signal point regions 742a, 742b, 742c, 742d of first, second, third, fourth levels 740a, 740b, 740c, 740d, respectively. As a result, subchannels 1, 2, 3, 4 of 2 bit are created. This is termed as C-CDM (Constellation-Code Division Multiplex). Fig. 111 shows a detailed code assignment of the C-CDM equivalent to expanded 16 QAM , and Fig. 112 shows a detailed code assignment of the C-CDM equivalent to expanded 36 QAM. As the C-CDM is an independent multiplexing system, it can be combined with the conventional FDM (Frequency Division Multiplex) or TDM (Time Division Multiplex) to further increase the number of subchannels. In this manner, the C-CDM system realizes a novel multiplexing system. Although the C-CDM is explained by using a rectangle QAM, other modulation system having signal points, e.g. QAM, PSK, ASK, and even FSK if frequency regions are regarded as signal points, can be also used for this multiplexing in the same manner.

Embodiment 4

[0201] A fourth embodiment of the present invention will be described referring to the relevant drawings.

[0202] Fig. 37 illustrates the entire arrangement of a signal transmission system of the fourth embodiment, which is arranged for terrestrial service and similar in both construction and action to that of the third embodiment shown in Fig. 29. The difference is that the transmitter antenna 6 is replaced with a terrestrial antenna 6a and the receiver antennas 22, 23, 24 are replaced with also three terrestrial antennas 22a, 23a, 24a. The action of the system is identical to that of the third embodiment and will no more be explained. The terrestrial broadcast service unlike a satellite service depends much on the distance between the transmitter antenna 6a to the receiver antennas 22a, 32a, 42a. If a receiver is located far from the transmitter, the level of a received signal is low. Particularly, a common multi-level QAM signal can hardly be demodulated by the receiver which thus reproduces no TV program.

[0203] The signal transmission system of the present invention allows the first receiver 23 equipped with the antenna 22a, which is located at a far distance as shown in Fig. 37, to intercept a modified 16 or 64 QAM signal and demodulate at 4 PSK mode the first data stream or D_1 component of the received signal to an NTSC video signal so that a TV program picture of medium resolution can be displayed even if the level of the received signal is relatively low.

[0204] Also, the second receiver 33 with the antenna 32a is located at a medium distance from the antenna 6a and can thus intercept and demodulate both the first and second data streams or D_1 and D_2 components of the modified 16 or 64 QAM signal to an HDTV video signal which in turn produces an HDTV program picture.

[0205] The third receiver 43 with the antenna 42a is located at a near distance and can intercept and demodulate the first, second, and third data streams or D_1, D_2, and D_3 components of the modified 16 or 64 QAM signal to a super HDTV video signal which in turn produces a super HDTV picture in quality to a common movie picture.

[0206] The assignment of frequencies is determined by the same manner as of the time division multiplexing shown in Figs. 34, 35, and 36. Like Fig. 34, when the frequencies are assigned t first to sixth channels, L1 of the D_1 component carries an NTSC data of the first channel, M1 of the D2 component carries an HDTV difference data of the first channel, and H1 of the D_3 component carries a super HDTV difference data of the first channel. Accordingly, NTSC, HDTV, and super HDTV data all can be carried on the same channel. If D_2 and D_3 of the other channels are utilized as shown in Figs. 35 and 36, more data of HDTV and super HDTV respectively can be transmitted for higher resolution display.

[0207] As understood, the system allows three different but compatible digital TV signals to be carried on a single channel or using D_2 and D_3 regions of other channels. Also, the medium resolution TV picture data of each channel can be intercepted in a wider service area according to the present invention.

[0208] A variety of terrestrial digital TV broadcast systems employing a 16 QAM HDTV signal of 6 MHz bandwidth have been proposed. Those are however not compatible with the existing NTSC system and thus, have to be associated with a simulcast technique for transmitting NTSC signals of the same program on another channel. Also, such a common 16 QAM signal limits a service area. The terrestrial service system of the present invention allows a receiver located at a relatively far distance to intercept successfully a medium resolution TV signal with no use of an additional device nor an extra channel.

[0209] Fig. 52. shows an interference region of the service area 702 of a conventional terrestrial digital HDTV broadcast station 701. As shown, the service area 702 of the conventional HDTV station 701 is inter-

sected with the service area 712 of a neighbor analogue TV station 711. At the intersecting region 713, an HDTV signal is attenuated by signal interference from the analogue TV station 711 and will thus be intercepted with less consistency.

[0210] Fig. 53 shows an interference region associated with the multi-level signal transmission system of the present invention. The system is low in the energy utilization as compared with a conventional system and its service area 703 for HDTV signal propagation is smaller than the area 702 of the conventional system. In contrary, the service area 704 for digital NTSC or medium resolution TV signal propagation is larger than the conventional area 702. The level of signal interference from a digital TV station 701 of the system to a neighbor analogue TV station 711 is equivalent to that from a conventional digital TV station, such as shown in Fig. 52.

[0211] In the service area of the digital TV station 701, there are three interference regions developed by signal interference from the analogue TV station 711. Both HDTV and NTSC signals can hardly be intercepted in the first region 705. Although fairly interfered, an NTSC signal may be intercepted at an equal level in the second region 706 denoted by the left down hatching. The NTSC signal is carried on the first data stream which can be reproduced at a relatively low C/N rate and will thus be minimum affected when the C/N rate is declined by signal interference from the analogue TV station 711.

[0212] At the third region 707 denoted by the right down hatching, an HDTV signal can also be intercepted when signal interference is absent while the NTSC signal can constantly be intercepted at a low level.

[0213] Accordingly, the overall signal receivable area of the system will be increased although the service area of HDTV signals becomes a little bit smaller than that of the conventional system. Also, at the signal attenuating regions produced by interference from a neighbor analogue TV station, NTSC level signals of an HDTV program can successfully be intercepted as compared with the conventional system where no HDTV program is viewed in the same area. The system of the present invention much reduces the size of signal attenuating area and when increases the energy of signal transmission at a transmitter or transponder station, can extend the HDTV signal service area to an equal size to the conventional system. Also, NTSC level signals of a TV program can be intercepted more or less in a far distance area where no service is given by the conventional system or a signal interference area caused by an adjacent analogue TV station.

[0214] Although the embodiment employs a two-level signal transmission method, a three-level method such as shown in Fig. 78 will be used with equal success. If an HDTV signal is divided into three picture levels-HDTV, NTC, and low resolution NTSC, the service area shown in Fig. 53 will be increased from two levels to three levels where the signal propagation is extended radially and outwardly. Also, low resolution NTSC signals can be received at an acceptable level at the first signal interference region 705 where NTSC signals are hardly be intercepted in the two-level system. As understood, the signal interference is also involved from a digital TV station to an analogue TV station.

[0215] The description will now be continued, provided that no digital TV station should cause a signal interference to any neighbor analogue TV station. According to a novel system under consideration in U.S.A., no-use channels of the existing service channels are utilized for HDTV and thus, digital signals must not interfere with analogue signals. For the purpose, the transmitting level of a digital signal has to be decreased lower than that shown in Fig. 53. If the digital signal is of conventional 16 QAM or 4 PSK mode, its HDTV service area 708 becomes decreased as the signal interference region 713 denoted by the cross hatching is fairly large as shown in Fig. 54. This results in a less number of viewers and sponsors, whereby such a digital system will have much difficulty to operate for profitable business.

[0216] Fig. 55 shows a similar result according to the system of the present invention. As apparent, the HDTV signal receivable 703 is a little bit smaller than the equal area 708 of the conventional system. However, the lower resolution or NTSC TV signal receivable area 704 will be increased as compared with the conventional system. The hatching area represents a region where the NTSC level signal of a program can be received while the HDTV signal of the same is hardly intercepted. At the first interference region 705, both HDTV and NTSC signals cannot be intercepted due to signal interference from an analogue station 711.

[0217] When the level of signals is equal, the multi-level transmission system of the present invention provides a smaller HDTV service area and a greater NTSC service area for interception of an HDTV program at an NTSC signal level. Accordingly, the overall service area of each station is increased and more viewers can enjoy its TV broadcasting service. Furthermore, HDTV/NTSC compatible TV business can be operated with economical advantages and consistency. It is also intended that the level of a transmitting signal is increased when the control on averting signal interference to neighbor analogue TV stations is lessened corresponding to a sharp increase in the number of home-use digital receivers. Hence, the service area of HDTV signals will be increased and in this respect, the two different regions for interception of HDTV/NTSC and NTSC digital TV signal levels respectively, shown in Fig. 55, can be adjusted in proportion by varying the signal point distance in the first and/or second data stream. As the first data stream carries information about the signal point distance, a multi-level signal can be received with more certainty.

[0218] Fig. 56 illustrates signal interference between two digital TV stations in which a neighbor TV station 701a also provides a digital TV broadcast service, as compared with an analogue station in Fig. 52. Since the level of a transmitting signal becomes high, the HDTV

service or high resolution TV signal receivable area 703 in increased to an extension equal to the service area 702 of an analogue TV system.

[0219] At the intersecting region 714 between two service areas of their respective stations, the received signal can be reproduced not to an HDTV level picture with the use of a common directional antenna due to signal interference but to an NTSC level picture with a particular directional antenna directed towards a desired TV station. If a highly directional antenna is used, the received signal from a target station will be reproduced to an HDTV picture. The low resolution signal receivable area 704 is increased larger than the analogue TV system service area 702 and a couple of intersecting regions 715, 716 developed by the two low resolution signal receivable areas 704 and 704a of their respective digital TV stations 701 and 701a permit the received signal from antenna directed one of the two stations to be reproduced to an NTSC level picture.

[0220] The HDTV service area of the multi-level signal transmission system of the present invention itself will be much increased when applicable signal restriction rules are withdrawn in a coming digital TV broadcast service maturity time.

[0221] At the time, the system of the present invention also provides as a wide HDTV signal receivable area as of the conventional system and particularly, allows its transmitting signal to be reproduced at an NTSC level in a further distance or intersecting areas where TV signals of the conventional system are hardly intercepted. Accordingly, signal attenuating or shadow regions in the service area will be minimized.

Embodiment 5

[0222] A first embodiment of the present invention resides in amplitude modulation or ASK procedure. Fig. 57 illustrates the assignment of signal points of a 4-level ASK signal according to the fifth embodiment, in which four signal points are denoted by 721, 722, 723, and 724. The four-level transmission permits a 2-bit data to be transmitted in every cycle period. It is assumed that the four signal points 721, 722, 723, 724 represent two-bit patterns 00, 01, 10, 11 respectively.

[0223] For ease of four-level signal transmission of the embodiment, the two signal points 721, 722 are designated as a first signal point group 725 and the other two 723, 724 are designated as a second signal point group 726. The distance between the two signal point groups 725 and 726 is then determined wider than that between any two adjacent signal points. More specifically, the distance L_0 between the two signals 722 and 723 is arranged wider than the distance L between the two adjacent points 721 and 722 or 723 and 724. This is expressed as:

$$L_0 > L$$

Hence, the multi-level signal transmission system of the embodiment is based on $L_0>L$. The embodiment is however not limited to $L_0>L$ and $L=L_0$ will be employed temporarily or permanently depending on the requirements of design, condition, and setting.

[0224] The two signal point groups are assigned one-bit patterns of the first data stream D_1, as shown in Fig. 59(a). More particularly, a bit 0 of binary system is assigned to the first signal point group 725 and another bit 1 to the second signal point group 726. Then, a one-bit pattern of the second data stream D_2 is assigned to each signal point. For example, the two signal points 721, 723 are assigned $D_2=0$ and the other two signal points 722 and 724 are assigned $D_2=1$. Those are thus expressed by two bits per symbol.

[0225] The multi-level signal transmission of the present invention can be implemented in an ASK mode with the use of the foregoing signal point assignment. The system of the present invention works in the same manner as of a conventional equal signal point distance technique when the signal to noise ratio or C/N rate is high. If the C/N rate becomes low and no data can be reproduced by the conventional technique, the present system ensures reproduction of the first data stream D_1 but not the second data stream D_2. In more detail, the state at a low C/N is shown in Fig. 60. The signal points transmitted are displaced by a Gaussian distribution to ranges 721a, 722a, 723a, 724a respectively at the receiver side due to noise and transmission distortion. Therefore, the distinction between the two signals 721 and 722 or 723 and 724 will hardly be executed. In other words, the error rate in the second data stream D_2 will be increased. As apparent from Fig. 60, the two signal points 721, 722 are easily distinguished from the other two signal points 723, 724. The distinction between the two signal point groups 725 and 726 can thus be carried out with ease. As the result, the first data stream D_1 will be reproduced at a low error rate.

[0226] Accordingly, the two different level data D_1 and D_2 can be transmitted simultaneously. More particularly, both the first and second data streams D_1 and D_2 of a given signal transmitted through the multi-level transmission system can be reproduced at the area where the C/N rate is high and the first data stream D_1 only can be reproduced in the area where the C/N rate is low.

[0227] Fig. 61 is a block diagram of a transmitter 741 in which an input unit 742 comprises a first data stream input 743 and a second data stream input 744. A carrier wave from a carrier generator 64 is amplitude modulated by a multiplier 746 using an input signal fed across a processor 745 from the input unit 743. The modulated signal is then band limited by a filter 747 to an ASK signal of e.g. VSB mode which is then delivered from an output unit 748.

[0228] The waveform of the ASK signal after filtering will now be examined. Fig. 62(a) shows a frequency spectrum of the ASK modulated signal in which two sidebands are provided on both sides of the carrier frequency band. One of the two sidebands is eliminated with the filter 474 to produce a signal 749 which contains

a carrier component as shown in Fig. 62(b). The signal 749 is a VSB signal and if the modulation frequency band is f_0, will be transmitted in a frequency band of about $f_0/2$. Hence, the frequency utilization becomes high. Using VSB mode transmission, the ASK signal of two bit per symbol shown in Fig. 60 can thus carry in the frequency band an amount of data equal to that of 16 QAM mode at four bits per symbol.

[0229] Fig. 63 is a block diagram of a receiver 751 in which an input signal intercepted by a terrestrial antenna 32a is transferred through an input unit 752 to a mixer 753 where it is mixed with a signal from a variable oscillator 754 controlled by channel selection to a lower medium frequency signal. The signal from the mixer 753 is then detected by a detector 755 and filtered by an LPF 756 to a baseband signal which is transferred to a discriminating/reproduction circuit 757. The discrimination/reproduction circuit 757 reproduces two, first D_1 and second D_2, data streams from the baseband signal and transmit them further through a first 758 and a second data stream output 759 respectively.

[0230] The transmission of a TV signal using such a transmitter and a receiver will be explained. Fig. 64 is a block diagram of a video signal transmitter 774 in which a high resolution TV signal, e.g. an HDTV signal, is fed through an input unit 403 to a divider circuit 404 of a first video encoder 401 where it is divided into four high/low frequency TV signal components denoted by e.g. H_LV_L, H_LV_H, H_HV_L, and H_HV_H. This action is identical to that of the third embodiment previously described referring to Fig. 30 and will no more be explained in detail. The four separate TV signals are encoded respectively by a compressor 405 using a known DPCMDCT variable length code encoding technique which is commonly used e.g. in MPEG. Meanwhile, the motion compensation of the signal is carried out at the input unit 403. The compressed signals are summed by a summer 771 to two, first and second, data streams D_1, D_2. The low frequency video signal component or H_LV_L signal is contained in the first data stream D_1. The two data stream signals D_1, D_2 are then transferred to a first 743 and a second data stream input 744 of a transmitter unit 741 where they are amplitude modulated and summed to an ASK signal of e.g. VSB mode which is propagated from a terrestrial antenna for broadcast service.

[0231] Fig. 65 is a block diagram of a TV receiver for such a digital TV broadcast system. A digital TV signal intercepted by a terrestrial antenna 32a is fed to an input 752 of a receiver 781. The signal is then transferred to a detection/demodulation circuit 760 where a desired channel signal is selected and demodulated to two, first and second, data streams D_1, D_2 which are then fed to a first 758 and a second data stream output 759 respectively. The action in the receiver unit 751 is similar to that described previously and will no more be explained in detail. The two data streams D_1, D_2 are sent to a divider unit 776 in which D_1 is divided by a divider 777 into two components; one or compressed H_LV_L is transferred to a first input 521 of a second video decoder 422 and the other is fed to a summer 778 where it is summed with D_2 prior to transfer to a second input 531 of the second video decoder 422. Compressed H_LV_L is then sent from the first input 521 to a first expander 523 where it is expanded to H_LV_L of the original length which is then transferred to a video mixer 548 and an aspect ratio changing circuit 779. When the input TV signal is an HDTV signal, H_LV_L represents a wide-screen NTSC signal. When the same is an NTSC signal, H_LV_L represents a lower resolution video signal, e.g. MPEG1, that an NTSC level.

[0232] The input TV signal of the embodiment is an HDTV signal and H_LV_L becomes a wide-screen NTSC signal. If the aspect ratio of an available display is 16:9, H_LV_L is directly delivered through an output unit as a 16:9 video output 426. If the display has an aspect ratio of 4:3, H_LV_L is shifted by the aspect ratio changing circuit 779 to a letterbox or sidepanel format and then, delivered from the output unit 780 as a corresponding format video output 425.

[0233] The second data stream D_2 fed from the second data stream output 759 to the summer 778 is summed with the output of the divider 777 to a sum signal which is then fed to the second input 531 of the second video decoder 422. The sum signal is further transferred to a divider circuit 531 while it is divided into three compressed forms of H_LV_H, H_HV_L, and H_HV_H. The three compressed signals are then fed to a second 535, a third 536, and a fourth expander 537 respectively for converting by expansion to H_LV_H, H_HV_L, and H_HV_H of the original length. The three signals are summed with H_LV_L by the video mixer 548 to a composite HDTV signal which is fed through an output 546 of the second video decoder to the output unit 780. Finally, the HDTV signal is delivered from the output unit 780 as an HDTV video signal 427.

[0234] The output unit 780 is arranged for detecting an error rate in the second data stream of the second data stream output 759 through an error rate detector 782 and if the error rate is high, delivering H_LV_L of low resolution video data systematically.

[0235] Accordingly, the multi-level signal transmission system for digital TV signal transmission and reception becomes feasible. For example, if a TV signal transmitter station is near, both the first and second data streams of a received signal can successfully be reproduced to exhibit an HDTV quality picture. If the transmitter station is far, the first data stream can be reproduced to H_LV_L which is converted to a low resolution TV picture. Hence, any TV program will be intercepted in a wider area and displayed at a picture quality ranging from HDTV to NTSC level.

[0236] Fig. 66 is a block diagram showing another arrangement of the TV receiver. As shown, the receiver unit 751 contains only a first data stream output 768 and thus, the processing of the second data stream or HDTV data is not needed so that the overall construction can be minimized. It is a good idea to have the first video

decoder 421 shown in Fig. 31 as a video decoder of the receiver. Accordingly, an NTSC level picture will be reproduced. The receiver is fabricated at much less cost as having no capability to receive any HDTV level signal and will widely be accepted in the market. In brief, the receiver can be used as an adapter tuner for interception of a digital TV signal with giving no modification to the existing TV system including a display.

[0237] The TV receiver 781 may have a further arrangement shown in Fig. 67, which serves as both a satellite broadcast receiver for demodulation of PSK signals and a terrestrial broadcast receiver for demodulation of ASK signals. In action, a PSK signal received by a satellite antenna 32 is mixed by a mixer 786 with a signal from an oscillator 787 to a low frequency signal which is then fed through an input unit 34 to a mixer 753 similar to one shown in Fig. 63. The low frequency signal of PSK or QAM mode in a given channel of the satellite TV system is transferred to a modulator 35 where two data streams D_1 and D_2 are reproduced from the signal. D_1 and D_2 are sent through a divider 788 to a second video decoder 422 where they are converted to a video signal which is then delivered from an output unit 780. Also, a digital or analogue terrestrial TV signal intercepted by a terrestrial antenna 32a is fed through an input unit 752 to the mixer 753 where one desired channel is selected by the same manner as described in Fig. 63 and detected to a low frequency base band signal. The signal of analogue form is sent directly to the demodulator 35 for demodulation. The signal of digital form is then fed to a discrimination/reproducing circuit 757 where two data streams D_1 and $D\underline{2}$ are reproduced from the signal. D_1 and $D\underline{2}$ are converted by the second video decoder 422 to a video signal which is then delivered further. A satellite analogue TV signal is transferred to a video demodulator 788 where it is AN modulated to an analogue video signal which is then delivered from the output unit 780. As understood, the mixer 753 of the TV receiver 781 shown in Fig. 67 is arranged compatible between two, satellite and terrestrial, broadcast services. Also, a receiver circuit including a detector 755 and an LPF 756 for AM modulation of an analogue signal can be utilized compatible with a digital ASK signal of the terrestrial TV service. The major part of the arrangement shown in Fig. 67 is arranged for compatible use, thus minimizing a circuitry construction.

[0238] According to the embodiment, a 4-level ASK signal is divided into two, D_1 and D_2, level components for execution of the one-bit mode multi-level signal transmission. If an 8-level ASK signal is used as shown in Fig. 68, it can be transmitted in a one-bit mode three-level, D_1, D_2, and D_3, arrangement. A shown in Fig. 68, D_1 is assigned to eight signal points 721a, 721b, 722a, 722b, 723a, 723b, 724a, 724b, each pair representing a two-bit pattern, D_2 is assigned to four small signal point groups 721, 722, 723, 724, each two groups representing a two-bit pattern, and D_3 is assigned to two large signal point groups 725 and 726 representing a two-bit pattern. More particularly, this is equivalent to a form in which each of the four signal points 721, 722, 723, 724 shown in Fig. 57 is divided into two components thus producing three different level data.

[0239] The three-level signal transmission is identical to that described in the third embodiment and will no further be explained in detail.

[0240] In particular, the arrangement of the video encoder 401 of the third embodiment shown in Fig. 30 is replaced with a modification of which block diagram is Fig. 69. The operation of the modified arrangement is similar and will no longer be explained in detail. Two video signal divider circuits 404 and 404a which may be sub-band filters are provided forming a divider unit 794. The divider unit 794 may also be arranged more simple a shown in the block diagram of Fig. 70, in which a signal passes across one signal divider circuit two times at time division mode. More specifically, a video signal of e.g. HDTV or super HDTV from the input unit 403 is time-base compressed by a time-base compressor 795 and fed to the divider circuit 404 where it is divided into four components, H_HV_H-H, H_HV_L-H, and H_LV_H-H, and H_LV_L-H at a first cycle. At the time, four switches 765, 765a, 765b, 765c remain turned to the position 1 so that H_HV_H-H, H_HV_L-H, and H_LV_H-H are transmitted to a compressing circuit 405. Meanwhile, H_LV_L-H is fed back through the terminal 1 of the switch 765c to the time-base compressor 795. At a second cycle, the four switches 765, 765a, 765b, 765c turned to the position 2 and all the four components of the divider circuit 404 are simultaneously transferred to the compressing circuit 405. Accordingly, the divider unit 796 of Fig. 70 arranged for time division processing of an input signal can be constructed in a simpler dividing circuit form.

[0241] At the receiver side, such a video decoder as described in the third embodiment and shown in Fig. 30 is needed for three-level transmission of a video signal. More particularly, a third video decoder 423 is provided which contains two mixers 556 and 556a of different processing capability as shown in the block diagram of Fig. 71.

[0242] Also, the third video decoder 423 may be modified in which the same action is executed with one single mixer 556 as shown in Fig. 72. At the first timing, five switches 765, 765a, 765b, 765c, 765d remains turned to the position 1. Hence, H_LV_L, H_LV_H, H_HV_L, and H_HV_H are fed from a first 522, a second 522a, a third 522b and a fourth expander 522c to through their respective switches to the mixer 556 where they are mixed to a single video signal. The video signal which represents H_LV_L-H of an input high resolution video signal is then fed back through the terminal 1 of the switch 765d to the terminal 2 of the switch 765c. At the second timing, the four switches 765, 765a, 765b, 765c are turned to the point 2. Thus, H_HV_H-H, H_HV_L-H, H_LV_H-H, and H_LV_L-H are transferred to the mixer 556 where they are mixed to a single video signal which is then sent across the terminal 2 of the switch 765d to the output unit 554 for

further delivery.

[0243] In this manner of time division processing of a three-level signal, two mixers can be replaced with one mixer.

[0244] More particularly, four components H_LV_L, H_LV_H, H_HV_L, H_HV_H are fed to produce H_LV_L-H at the first timing. Then, H_LV_H-H, H_HV_L-H, and H_HV_H-H are fed at the second timing delayed from th first timing and mixed with H_LV_L-H to a target video signal. It is thus essential to perform the two actions at an interval of time.

[0245] If the four components are overlapped each other or supplied in a variable sequence, they have to be time-base adjusted to a given sequence through using memories accompanied with their respective switches 765, 765a, 765b, 765c. In the foregoing manner, a signal is transmitted from the transmitter at two different timing periods as shown in Fig. 73 so that no time-base controlling circuit is needed in the receiver which is thus arranged more compact.

[0246] As shown in Fig. 73, D_1 is the first data stream of a transmitting signal and H_LV_L, H_LV_H, H_HV_L, and H_HV_H are transmitted on D_1 channel at the period of first timing. Then, at the period of second timing, H_LV_H, H_HV_L, and H_HV_H are transmitted on D_2 channel. As the signal is transmitted in a time division sequence, the encoder in the receiver can be arranged more simple.

[0247] The technique of reducing the number of the expanders in the decoder will now be explained. Fig. 74 (b) shows a time-base assignment of four data components 810, 810a, 810b, 810c of a signal. When other four data components 811, 811a, 811b, 811c are inserted between the four data components 811, 811a, 811b, 811c respectively, the latter can be transmitted at intervals of time. In action, the second video decoder 422 shown in Fig. 74(a) receives the four components of the first data stream D_1 at a first input 521 and transfers them through a switch 812 to an expander 503 one after another. More particularly, the component 810 first fed is expanded during the feeding of the component 811 and after completion of processing the component 810, the succeeding component 810a is fed. Hence, the expander 503 can process a row of the components at time intervals by the same time division manner as of the mixer, thus substituting the simultaneous action of a number of expanders.

[0248] Fig. 75 is a time-base assignment of data components of an HDTV signal, in which $H_LV_L(1)$ of an NTSC component of the first channel signal for a TV program is allocated to a data domain 821 of D_1 signal. Also, H_LV_H, H_HV_L, and H_HV_H carrying HDTV additional components of the first channel signal are allocated to three domains 821a, 821b, 821c of D_2 signal respectively. There are provided other data components 822, 822a, 822b, 822c between the data components of the first channel signal which can thus be expanded with an expander circuit during transmission of the other data. Hence, all the data components of one channel signal will be processed by a single expander capable of operating at a higher speed.

[0249] Similar effects will be ensured by assignment of the data components to other domains 821, 821a, 821b, 821c as shown in Fig. 76. This becomes more effective in transmission and reception of a common 4 PSK or ASK signal having no different digital levels.

[0250] Fig. 77 shows a time-base assignment of data components during physical two-level transmission of three different signal level data: e.g. NTSC, HDTV, and super HDTV or low resolution NTSC, standard resolution NTSC, and HDTV. For example, for transmission of three data components of low resolution NTSC, standard NTSC, and HDTV, the low resolution NTSC or H_LV_L is allocated to the data domain 821 of D_1 signal. Also, H_LV_H, H_HV_L, and H_HV_H of the standard NTSC component are allocated to three domains 821a, 821b, 821c respectively. H_LV_H-H, H_HV_L-H, and H_HV_H-H of the HDTV component are allocated to domains 823, 823a, and 823b respectively.

[0251] The foregoing assignment is associated with such a logic level arrangement based on discrimination in the error correction capability as described in the second embodiment. More particularly, H_LV_L is carried on D^{1-1} channel of the D_1 signal. The D_{1-1} channel is higher in the error correction capability than D_{1-2} channel, as described in the second embodiment. The D_{1-1} channel is higher in the redundancy but lower in the error rate than the D_{1-2} channel and the date 821 can be reconstructed at a lower C/N rate than that of the other data 821a, 821b, 821c. More specifically, a low resolution NTSC component will be reproduced at a far location from the transmitter antenna or in a signal attenuating or shadow area, e.g. the interior of a vehicle. In view of the error rate, the data 821 of D_{1-1} channel is less affected by signal interference than the other data 821a, 821b, 821c of D_{1-2} channel, while being specifically discriminated and stayed in a different logic level; as described in the second embodiment. While D_1 and D_2 are divided into two physically different levels, the levels determined by discrimination of the distance between error correcting codes are arranged different in the logic level.

[0252] The demodulation of D_2 data requires a higher C/N rate than that for D_1 data. In action, H_LV_L or low resolution NTSC signal can at least be reproduced in a distant or lower C/N service area. H_LV_H, H_HV_L, and H_HV_H can in addition be reproduced at a lower C/N area. Then, at a high C/N area, H_LV_H-H, H_HV_L-H, and H_HV_H-H components can also be reproduced to develop an HDTV signal. Accordingly, three different level broadcast signals can be played back. This method allows the signal receivable area shown in Fig. 53 to increase from a double region to a triple region, as shown in Fig. 90, thus ensuring higher opportunity for enjoying TV programs

[0253] Figs. 78 is a block diagram of the third video decoder arranged for the time-base assignment of data shown in Fig. 77, which is similar to that shown in Fig. 72 except that the third input 551 for D_3 signal is elimi-

nated and the arrangement shown in Fig. 74(a) is added.

[0254] In operation, both the D_1 and D_2 signals are fed through two input units 521, 530 respectively to a switch 812 at the first timing. As their components including H_LV_L are time divided, they are transferred in a sequence by the switch 812 to an expander 503. This sequence will now be explained referring to the time-base assignment of Fig. 77. A compressed form of H_LV_L of the first channel is first fed to the expander 503 where it is expanded. Then, H_LV_H, H_HV_L, and H_HV_H are expanded. All the four expanded components are sent through a switch 812a to a mixer 556 where they are mixed to produce H_LV_L-H. H_LV_L-H is then fed back from the terminal 1 of a switch 765a through the input 2 of a switch 765 to the H_LV_L input of the mixer 556.

[0255] At the second timing, H_LV_H-H, H_HV_L-H, and H_HV_H-H of the D_2 signal shown in Fig. 77 are fed to the expander 503 where they are expanded before transferred through the switch 821a to the mixer 556. They are mixed by the mixer 556 to an HDTV signal which is fed through the terminal 2 of the switch 765a to the output unit 521 for further delivery. The time-base assignment of data components for transmission, shown in Fig. 77, contributes to the simplest arrangement of the expander and mixer. Although Fig. 77 shows two, D_1 and D_2, signal levels, four-level transmission of a TV signal will be feasible using the addition of a D_3 signal and a super resolution HDTV signal.

[0256] Fig. 79 illustrates a time-base assignment of data components of a physical three-level, D_1, D_2, D_3, TV signal, in which data components of the same channel are so arranged as not to overlap with one another with time. Fig. 80 is a block diagram of a modified video decoder 423, similar to Fig. 78, in which a third input 521a is added. The time-base assignment of data components shown in Fig. 79 also contributes to the simple construction of the decoder.

[0257] The action of the modified decoder 423 is almost identical to that shown in Fig. 78 and associated with the time-base assignment shown in Fig. 77 and will no more be explained. It is also possible to multiplex data components on the D_1 signal as shown in Fig. 81. However, two data 821 and 822 are increased higher in the error correction capability than other data components 821a, 812b, 812c, thus staying at a higher signal level. More particularly, the data assignment for transmission is made in one physical level but two logic level relationship. Also, each data component of the second channel is inserted between two adjacent data components of the first channel so that serial processing can be executed at the receiver side and the same effects as of the time-base assignment shown in Fig. 79 will thus be obtained.

[0258] The time-base assignment of data components shown in Fig. 81 is based on the logic level mode and can also be carried in the physical level mode when the bit transmission rate of the two data components 821 and 822 is decreased to 1/2 or 1/3 thus to lower the error rate. The physical level arrangement is consisted of three different levels.

[0259] Fig. 82 is a block diagram of another modified video decoder 423 for decoding of the D_1 signal time-base arranged as shown in Fig. 81, which is simpler in construction than that shown in Fig. 80. Its action is identical to that of the decoder shown in Fig. 80 and will be no more explained.

[0260] As understood, the time-base assignment of data components shown in Fig. 81 also contributes to the similar arrangement of the expander and mixer. Also, four data components of the D_1 signal are fed at respective time slices to a mixer 556. Hence, the circuitry arrangement of the mixer 556 or a plurality of circuit blocks such as provided in the video mixer 548 of Fig. 32 may be arranged for changing the connection therebetween corresponding to each data component so that they become compatible in time division action and thus, minimized in circuitry construction.

[0261] Accordingly, the receiver can be minimized in the overall construction.

[0262] It would be understood that the fifth embodiment is not limited to ASK modulation and the other methods including PSK and QAM modulation, such as described in the first, second, and third embodiments, will be employed with equal success.

[0263] Also, FSK modulation will be eligible in any of the embodiments. For example, the signal points of a multiple-level FSK signal consisting of four frequency components f1, f2, f3, f4 are divided into groups as shown in Fig. 58 and when the distance between any two groups are spaced from each other for ease of discrimination, the multi-level transmission of the FSK signal can be implemented, as illustrated in Fig. 83.

[0264] More particularly, it is assumed that the frequency group 841 of f1 and f2 is assigned D_1=0 and the group 842 of f3 and f4 is assigned D_1=1. If f1 and f3 represent 0 at D_2 and f2 and f4 represent 1 at D_2, two-bit data transmission, one bit at D_1 or D_2, will be possible as shown in Fig. 83. When the C/N rate is high, a combination of D_1=0 and D_2=1 is reconstructed at t=t3 and a combination of D_1=1 and D_2=0 at t=t4. When the C/N rate is low, D_1=0 only is reproduced at t=t3 and D_1=1 at t=t4. In this manner, the FSK signal can be transmitted in the multi-level arrangement. This multi-state FSK signal transmission is applicable to each of the third, fourth, and fifth embodiments.

[0265] The fifth embodiment may also be implemented in the form of a magnetic record/playback apparatus of which block diagram shown in Fig. 84 because its ASK mode action is appropriate to magnetic record and playback operation.

Embodiment 6

[0266] A sixth embodiment of the present invention is applicable to a magnetic recording and playback appa-

ratus. Although the above-described fifth embodiment applies the present invention to a multiple-level recording ASK data transmission system, it is also feasible in the same manner to adopt this invention in a magnetic recording and playback apparatus of a multi-level ASK recording system. A multi-level magnetic recording can be realized by incorporating the C-CDM system of the present invention to PSK, FCK, and QAM, as well as ASK.

[0267] First of all, the method of realizing a multi-level recording in a 16 QAM or 32 QAM magnetic recording playback. apparatus will be explained with reference to the C-CDM system of the present invention. Fig. 84 is a circuit block diagram showing a QAM system incorporating C-CDM modulator. Hereinafter, a QAM system being multiplexed by the C-CDM modulator is termed as SRQAM.

[0268] As shown in Fig. 84, an input video signal, e. g. an HDTV signal, to a magnetic record/playback apparatus 851 is divided and compressed by a video encoder 401 into a low frequency band signal through a first video encoder 401a and a high frequency band signal through a second video encoder 401b respectively. Then, a low frequency band component, e.g. H_LV_L, of the video signal is fed to a first data stream input 743 of an input section 742 and a high frequency band component including H_HV_H is fed to a second data stream input 744 of the same. The two components are further transferred to a modulator 749 of a modulator/demodulator unit 852. The first data stream input 743 adds an error correcting code to the low frequency band signal in an ECC 743a. On the other hand, the second data stream fed into the second data stream input 744 is 2 bit in case of 16 SRQAM, 3 bit in case of 36 SRQAM, and 4 bit in case of 64 SRQAM. After an error correcting code being encoded in an ECC 744a, this signal is supplied to a Trellis encoder 744b in which a Trellis encoded signal having a ratio 1/2 in case of 16 SRQAM, 2/3 in case of 32 SRQAM, and 3/4 in case of 64 SRQAM is produced. A 64 SRQAM signal, for example, has a first data stream of 2 bit and a second data stream of 4 bit. A Trellis encoder of Fig. 128 allows this 64 SRQAM signal to perform a Trellis encoding of ratio 3/4 wherein 3 bit data is converted into 4 bit data. Thus redundancy increases and a data rate decreases, while error correcting capability increases. This results in the reduction of an error rate in the same data rate. Accordingly, transmittable information amount of the recording/playback system or transmission system will increase substantially.

[0269] It is, however, possible to constitute the first data stream input 743 to exclude a Trellis encoder as shown in Fig. 84 of this sixth embodiment because the first data stream has low error rate inherently. This will be advantageous in view of simplification of circuit configuration. The second data stream, however, has a narrow inter-code distance as compared with the first data stream and, therefore, has a worse error rate. The Trellis encoding of the second data stream improves such a worse error rate. It is no doubt that an overall circuit configuration becomes simple if the Trellis encoding of the first data stream is eliminated. An operation for modulation is almost identical to that of the transmitter of the fifth embodiment shown in Fig. 64 and will be no more explained. A modulated signal of the modulator 749 is fed into a recording/playback circuit 853 in which it is AC biased by a bias generator 856 and amplified by an amplifier 857a. Thereafter, the signal is fed to a magnetic head 854 for recording onto a magnetic tape 855.

[0270] A format of the recording signal is shown in a recording signal frequency assignment of Fig. 113. A main, e.g. 16 SRQAM, signal 859 having a carrier of frequency fc records information, and also a pilot f_p signal 859a having a frequency 2fc is recorded simultaneously. Distortion in the recording operation is lowered as a bias signal 859b having a frequency f_{BIAS} adds AC bias for magnetic recording. Two of three-level signals shown in Fig. 113 are recorded in multiple state. In order to reproduce these recorded signals, two thresholds Th-1-2, Th-2 are given. A signal 859 will reproduce all of two levels while a signal 859c will reproduce D_1 data only, depending on the C/N level of the recording/playback.

[0271] A main signal of 16 SRQAM will have a signal point assignment shown in Fig. 10. Furthermore, a main signal of 36 SRQAM will have a signal point assignment shown in Fig. 100. In reproduction of this signal, both the main signal 859 and the pilot signal 859a are reproduced through the magnetic head 854 and amplified by an amplifier 857b. An output signal of the amplifier 857b is fed to a carrier reproduction circuit 858 in which a filter 858a separates the frequency of the pilot signal f_p having a frequency 2f0 and a 1/2 frequency divider 858b reproduces a carrier of frequency f0 to transfer it to a demodulator 760. This reproduced carrier is used to demodulate the main signal in the demodulator 760. Assuming that a magnetic recording tape 855, e.g. HDTV tape, is of high C/N rate, 16 signal points are discriminatable and thus both D_1 and D_2 are demodulated in the demodulator 760. Subsequently, a video decoder 402 reproduce all the signals. An HDTV VCR can reproduce a high bit-rate TV signal such as a 15 Mbps HDTV signal. The low the C/N rate, the cheaper the cost of a video tape. So far, a VHS tape in the market is inferior more than 10 dB in the C/N rate to a full-scale broadcast tape. If a video tape 855 is of low C/N rate, it will not be able to discriminate all the 16 or 32 valued signal points. Therefore the first data stream D_1 can be reproduced, while a 2 bit, 3 bit, or 4 bit data stream of the second data stream D_2 cannot be reproduced. Only 2 bit data stream of the first data stream is reproduced. If a two-level HDTV video signal is recorded and reproduced, a low C/N tape having insufficient capability of reproducing a high frequency band video signal can output only a low rate low frequency band video signal of the first data stream, specifically e.g. a 7 Mbps wide NTSC TV signal.

[0272] As shown in a block diagram of Fig. 114, the

second data stream output 759, the second data stream input 744, and the second video decoder 402a can be eliminated in order to provide customers one aspect of lower grade products. In this case, a recording/playback apparatus 851, dedicated to a low bit rate, will include a modulator such as a modified QPSK which modulates and demodulates the first data stream only. This apparatus allows only the first data stream to be recorded and reproduced. Specifically, a wide NTSC grade video signal can be recorded and reproduced.

[0273] Above-described high C/N rate video tape 855 capable of recording a high bit-rate signal, e.g. HDTV signal, will be able to use in such a low bit-rate dedicated magnetic recording/playback apparatus but will reproduce the first data stream D_1 only. That is, the wide NTSC signal is outputted, while the second data stream is not reproduced. In other words, one recording/playback apparatus having a complicated configuration can reproduce a HDTV signal and the other recording/playback apparatus having a simple configuration can reproduce a wide NTSC signal if a given video tape 855 includes the same multi-level HDTV signal. Accordingly in case of two-level multiple state, four combinations will be realized with perfect compatibility among two tapes having different C/N rates and two recording/playback apparatus having different recording/playback data rates. This will bring remarkable effect. In this case, an NTSC dedicated apparatus will be simple in construction as compared with an HDTV dedicated apparatus. In more detail, a circuit scale of EDTV decoder will be 1/6 of that of HDTV decoder. Therefore, a low function apparatus can be realized at fairly low cost. Realization of two, HDTV and EDTV, types recording/playback apparatus having different recording/reproducing capability of picture quality will provide various type products ranging in a wide price range. Users can freely select a tape among a plurality of tapes, from an expensive high C/N rate tape to a cheaper low C/N rate tape, as occasion demands so as to satisfy required picture quality. Not only maintaining perfect compatibility but obtaining expandable capability will be attained and further compatibility with a future system will be ensured. Consequently, it will be possible to establish long-lasting standards for recording/playback apparatus. Other recording methods will be used in the same manner. For example, a multi-level recording will be realized by use of phase modulation explained in the first and third embodiments. A recording using ASK explained in the fifth embodiment will also be possible. A multiple state will be realized by converting present recording from two-level to four-level and dividing into two groups as shown in Figs. 59(c) and 59(d).

[0274] A circuit block diagram for ASK is identical to that disclosed in Fig. 84. Besides embodiments already described, a multi-level recording will be also realized by use of multiple tracks on a magnetic tape. Furthermore, a theoretical multi-level recording will be feasible by differentiating the error correcting capability so as to discriminate respective data.

[0275] Compatibility with future standards will be described below. A setting of standards for recording/playback apparatus such as VCR is normally executed by taking account of the most highest C/N rate tape available in practice. The recording characteristics of tapes progresses rapidly. For example, the C/N rate has been improved more than 10 dB compared with the tape used 10 years ago. If supposed that new standards will be established after 10 to 20 years due to an advancement of tape property, a conventional method will encounter with difficulty in maintaining compatibility with older standards. New and old standards, in fact, used to be one-way compatible or non-compatible with each other. On the contrary, in accordance with the present invention, the standards are first of all established for recording and/or reproducing the first data stream and/or second data stream on present day tapes. Subsequently, if the C/N rate is improved magnificently in future, an upper level data stream, e.g. a third data stream, will be added without any difficulty as long as the present invention is incorporated in the system. For example, a super HDTV VCR capable of recording or reproducing a three-level 64 SRQAM signal will be realized while maintaining perfect compatibility with the conventional standards. A magnetic tape, recording first to third data streams in compliance with new standards, will be able to use, of cause, in the older two-level magnetic recording/playback apparatus capable of recording and/or reproducing only first and second data streams. In this case, first and second data streams can be reproduced perfectly although the third data stream is left non-reproduced. Therefore, an HDTV signal can be reproduced. For these reasons, the merit of expanding recording data amount while maintaining compatibility between new and old standards is expected.

[0276] Returning to the explanation of reproducing operation of Fig. 84, the magnetic head 854 and the magnetic reproduction circuit 853 reproduce a reproducing signal from the magnetic tape 855 and feeds it to the modulation/demodulation circuit 852. The demodulating operation is almost identical with that of first, third, and fourth embodiments and will no further be explained. The demodulator 760 reproduces the first and second data streams D_1 and D_2. The second data stream D_2 is error corrected with high code gain in a Trellis-decoder 759b such as a Vitabi decoder, so as to be low error rate. The video decoder 402 demodulates D_1 and D_2 signals to output an HDTV video signal.

[0277] Fig. 131 is a block diagram showing a three-level magnetic recording/playback apparatus in accordance with the present invention which includes one theoretical level in addition to two physical levels. This system is substantially the same as that of Fig. 84. The difference is that the first data stream is further divided into two subchannels by use of a TDM in order to realize a three-level construction.

[0278] As shown in Fig. 131, an HDTV signal is sep-

arated first of all into two, medium and low frequency band video signals D_{1-1} and D_{1-2}, through a 1-1 video encoder 401c and a 1-2 video encoder 401d and, thereafter, fed into a first data stream input 743 of an input section 742. The data stream D_{1-1} having a picture quality of MPEG grade is error correcting coded with high code gain in an ECC encoder 743a, while the data stream D_{1-2} is error correcting coded with normal code gain in an ECC encoder 743b. D_{1-1} and D_{1-2} are time multiplexed together in a TDM 743c to be one data stream D_1. D_1 and D_2 are modulated into two-level signal in a C-CDM 749 and then recorded on the magnetic tape 855 through the magnetic head 854.

[0279] In playback operation, a recording signal reproduced through the magnetic head 854 is demodulated into D_1 and D_2 by the C-CDM demodulator 760 in the same manner as in the explanation of Fig. 84. The first data stream D_1 is demodulated into two, D_{1-1} and D_{1-2}, subchannels through the TDM 758c provided in the first data stream output 758. D_{1-1} data is error corrected in an ECC decoder 758a having high code gain. Therefore, D_{1-1} data can be demodulated at a lower C/N rate as compared with D_{1-2} data. A 1-1 video decoder 402a decodes the D_{1-1} data and outputs an LDTV signal. On the other hand, D_{1-2} data is error corrected in an ECC decoder 758b having normal code gain. Therefore, D_{1-2} data has a threshold value of high C/N rate compared with D_{1-1} data and thus will not be demodulated when a signal level is not large. D_{1-2} data is then demodulated in a 1-2 video decoder 402d and summed with D_{1-1} data to output an EDTV signal of wide NTSC grade.

[0280] The second data stream D_2 is Vitabi demodulated in a Trellis decoder 759b and error corrected at an ECC decoder 759a. Thereafter, D_2 data is converted into a high frequency band video signal through a second video decoder 402b and, then, summed with D_{1-1} and D_{1-2} data to output an HDTV signal. In this case, a threshold value of the C/N rate of D_2 data is set larger than that of C/N rate of D_{1-2} data. Accordingly, D_{1-1} data, i.e. an LDTV signal, will be reproduced from a tape 855 having a smaller C/N rate. D_{1-1} and D_{1-2} data, i.e. an EDTV signal, will be reproduced from a tape 855 having a normal C/N rate. And, D_{1-1}, D_{1-2}, and D_2 data, i.e. an HDTV signal, will be reproduced from a tape 855 having a high C/N rate.

[0281] Three-level magnetic recording/playback apparatus can be realized in this manner. As described in the foregoing description, the tape 855 has an interrelation between C/N rate and cost. The present invention allows users to select a grade of tape in accordance with a content of TV program they want to record because video signals having picture qualities of three grades can be recorded and/or reproduced in accordance with tape cost.

[0282] Next, an effect of multi-level recording will be described with respect to fast feed playback. As shown in a recording track diagram of Fig. 132, a recording track 855a having an azimuth angle A and a recording track 855b having an opposite azimuth angle B are alternately arrayed on the magnetic tape 855. The recording track 855a has a recording region 855c at its central portion and the remainder as D_{1-2} recording regions 855d, as denoted in the drawing. This unique recording pattern is provided on at least one of several recording tracks. The recording region 855c records one frame of LDTV signal. A high frequency band signal D_2 is recorded on a D_2 recording region 855e corresponding to an entire recording region of the recording track 855a. This recording format causes no novel effect against a normal speed recording/playback operation.

[0283] A fast feed reproduction in a reverse direction does not allow a magnetic head trace 855f having an azimuth angle A to coincide with the magnetic track as shown in the drawing. As the present invention provides the D_{1-1} recording region 855c at a central narrow region of the magnetic tape as shown in Fig. 132, this region only is surely reproduced although it occurs with a predetermined probability. Thus reproduced D_{1-1} signal can democulate an entire picture plane of the same time although its picture quality is an LDTV of MPEG1 level. In this manner several to several tens LDTV signals per second can be reproduced with perfect picture images during the fast feed playback operation, thereby enabling users to surely confirm picture images during the fast feed operation.

[0284] A head trace 855g corresponds to a head trace in the reverse playback operation, from which it is understood only a part of the magnetic track is traced in the reverse playback operation. The recording/playback format shown in Fig. 132 however allows, even in such a reverse playback operation, to reproduce D_{1-1} recording region and, therefore, an animation of LDTV grade is outputted intermittently.

[0285] Accordingly, the present invention makes it possible to record a picture image of LDTV grade within a narrow region on the recording track, which results in intermittent reproduction of almost perfect still pictures with picture quality of LDTV grade during normal and reverse fast feed playback operations. Thus, the users can easily confirm picture imaged even in high-speed searching.

[0286] Next, another method will be described to respond a higher speed fast feed playback operation. A D_{1-1} recording region 855c is provided as shown at lower right of Fig. 132, so that one frame of LDTV signal is recorded thereon. Furthermore, a narrow D_{1-1}·D_2 recording region 855h is provided at a part of the D_{1-1} recording region 855c. A subchannel D_{1-1} in this region records a part of information relating to the one frame of LDTV signal. The remainder of the LDTV information is recorded on the D_2 recording region 855j of the D_{1-1}·D_2 recording region 855h in a duplicated manner. The subchannel D_2 has a data recording capacity 3 to 5 times as much as the subchannel D_{1-1}. Therefore, subchannels D_{1-1} and D_2 can record one frame information of LDTV signal on a smaller, 1/3~1/5, area of the

recording tape. As the head trace can be recorded in a further narrower regions 855h, 855j, both time and area are decreased into 1/3~1/5 as compared with a head trace time T_{S1}. Even if the trace of head is further inclined by increasing the fast feed speed amount, the probability of entirely tracing this region will be increased. Accordingly, perfect LDTV picture images will be intermittently reproduced even if the fast feed speed is increased up to 3 to 5 times as fast as the case of the subchannel D_{1-1} only.

[0287] In case of a two-level VCR, this method is useless in reproducing the D_2 recording region 855j and therefore this region will not be reproduced in a high-speed fast feed playback operation. On the other hand, a three-level high performance VCR will allow users to confirm a picture image even if a fast feed playback operation is executed at a faster, 3 to 5 as fast as the two-level VCR, speed. In other words, not only excellent picture quality is obtained in accordance with cost but a maximum fast feed speed capable of reproducing picture images can be increased in accordance with the cost.

[0288] Although this embodiment utilizes a multi-level modulation system, it is needless to say that a normal, e.g. 16 QAM, modulation system can also be adopted to realize the fast feed playback operation in accordance with the present invention as long as an encoding of picture images is of multiple type.

[0289] A recording method of a conventional non-multiple digital VCR, in which picture images are highly compressed, disperses video data uniformly. Therefore, it was not possible in a fast feed playback operation to reproduce all the picture images on a picture plane of the same time. The picture reproduced was the one consisting of plurality of picture image blocks having non-coincided time bases with each other. The present invention, however, provides a multi-level HDTV VCR which can reproduce picture image blocks having coincided time bases on an entire picture plane during a fast feed playback operation although its picture quality is of LDTV grade.

[0290] The three-level recording in accordance with the present invention will be able to reproduce a high resolution TV signal such as HDTV signal when the recording/playback system has a high C/N rate. Meanwhile, a TV signal of EDTV grade, e.g. a wide NTSC signal, or a TV signal of LDTV grade, e.g. a low resolution NTSC signal, will be reproduced when the recording/playback system has a low C/N rate or poor function.

[0291] As is described in the foregoing description, the magnetic recording/playback apparatus in accordance with the present invention can reproduce picture images consisting of the same content even if the C/N rate is low or an error rate is high, although the resolution or the picture quality is relatively low.

Embodiment 7

[0292] A seventh embodiment of the present invention will be described for execution of four-level video signal transmission. A combination of the four-level signal transmission and the four-level video data construction will create a four-level signal service area as shown in Fig. 91. The four-level service area is consisted of, from innermost, a first 890a, a second 890b, a third 890c, and a fourth signal receiving area 890d. The method of developing such a four-level service area will be explained in more detail.

[0293] The four-level arrangement can be implemented by using four physically different levels determined through modulation or four logic levels defined by data discrimination in the error correction capability. The former provides a large difference in the C/N rate between two adjacent levels and the C/N rate has to be increased to discriminate all the four levels from each other. The latter is based on the action of demodulation and a difference in the C/N rate between two adjacent levels should stay at minimum. Hence, the four-level arrangement is best constructed using a combination of two physical levels and two logic levels. The division of a video signal into four signal levels will be explained.

[0294] Fig. 93 is a block diagram of a divider circuit 3 which comprises a video divider 895 and four compressors 405a, 405b, 405c, 405d. The video divider 895 contains three dividers 404a, 404b, 404c which are arranged identical to the divider circuit 404 of the first video encoder 401 shown in Fig. 30 and will be no more explained. An input video signal is divided by the dividers into four components, H_LV_L of low resolution data, H_HV_H of high resolution data, and H_LV_H and H_HV_L for medium resolution data. The resolution of H_LV_L is a half that of the original input signal.

[0295] The input video signal is first divided by the divider 404a into two, high and low, frequency band components, each component being divided into two, horizontal and vertical, segments. The intermediate between the high and low frequency ranges is a dividing point according to the embodiment. Hence, if the input video signal is an HDTV signal of 1000-line vertical resolution, H_LV_L has a vertical resolution of 500 lines and a horizontal resolution of a half value.

[0296] Each of two, horizontal and vertical, data of the low frequency component H_LV_L is further divided by the divider 404c into two frequency band segments. Hence, an H_LV_L segment output is 250 lines in the vertical resolution and 1/4 of the original horizontal resolution. This output of the divider 404c which is termed as an LL signal is then compressed by the compressor 405a to a D_{1-1} signal.

[0297] The other three higher frequency segments of H_LV_L are mixed by a mixer 772c to an LH signal which is then compressed by the compressor 405b to a D_{1-2} signal. The compressor 405b may be replaced with three compressors provided between the divider 404c

and the mixer 772c.

[0298] H_LV_H, H_HV_L, and H_HV_H form the divider 404a are mixed by a mixer 772a to an H_HV_H-H signal. If the input signal is as high as 1000 lines in both horizontal and vertical resolution, H_HV_H-H has 500 to 1000 lines of a horizontal and a vertical resolution. H_HV_H-H is fed to the divider 404b where it is divided again into four components.

[0299] Similarly, H_LV_L from the divider 404b has 500 to 750 lines of a horizontal and a vertical resolution and transferred as an HL signal to the compressor 405c. The other three components, H_LV_H, H_HV_L, and H_HV_H, from the divider 404b have 750 to 1000 lines of a horizontal and a vertical resolution and are mixed by a mixer 772b to an HH signal which is then compressed by the compressor 405d and delivered as a D_{202} signal. After compression, the HL signal is delivered as a $D_{2\text{-}1}$ signal. As the result, LL or $D_{1\text{-}1}$ carries a frequency data of 0 to 250 lines, LH or $D_{1\text{-}2}$ carries a frequency data from more than 250 lines up to 500 lines, HL or $D_{2\text{-}1}$ carries a frequency data of more than 500 lines up to 750 lines, and HH or $D_{2\text{-}2}$ carries a frequency data of more than 750 lines to 1000 lines so that the divider circuit 3 can provide a four-level signal. Accordingly, when the divider circuit 3 of the transmitter 1 shown in Fig. 87 is replaced with the divider circuit of Fig. 93, the transmission of a four-level signal will be implemented.

[0300] The combination of multi-level data and multi-level transmission allows a video signal to be at steps declined in the picture quality in proportion to the C/N rate during transmission, thus contributing to the enlargement of the TV broadcast service area. At the receiving side, the action of demodulation and reconstruction is identical to that of the second receiver of the second embodiment shown in Fig. 88 and will be no more explained. In particular, the mixer 37 is modified for video signal transmission rather than data communications and will now be explained in more detail.

[0301] As described in the second embodiment, a received signal after demodulated and error corrected, is fed as a set of four components $D_{1\text{-}1}$, $D_{1\text{-}2}$, $D_{2\text{-}1}$, $D_{2\text{-}2}$ to the mixer 37 of the second receiver 33 of Fig. 88.

[0302] Fig. 94 is a block diagram of a modified mixer 33 in which $D_{1\text{-}1}$, $D_{1\text{-}2}$, $D_{2\text{-}1}$, $D_{2\text{-}2}$ are explained by their respective expanders 523a, 523b, 523c, 523d to an LL, and LH, an HL, and an HH signal respectively which are equivalent to those described with Fig. 93. If the bandwidth of the input signal is 1, LL has a bandwidth of 1/4, LL+LH has a bandwidth of 1/2, LL+LH+HL has a bandwidth of 3/4, and LL+LH+HL+HH has a bandwidth of 1. The LH signal is then divided by a divider 531a and mixed by a video mixer 548a with the LL signal. An output of the video mixer 548a is transferred to an H_LV_L terminal of a video mixer 548c. The video mixer 531a is identical to that of the second decoder 527 of Fig. 32 and will be no more explained. Also, the HH signal is divided by a divider 531b and fed to a video mixer 548b. At the video mixer 548b, the HH signal is mixed with the HL signal to an H_HV_H-H signal which is then divided by a divider 531c and sent to the video mixer 548c. At the video mixer 548c, H_HV_H-H is combined with the sum signal of LH and LL to a video output. The video output of the mixer 33 is then transferred to the output unit 36 of the second receiver shown in Fig. 88 where it is converted to a TV signal for delivery. If the original signal has 1050 lines of vertical resolution or is an HDTV signal of about 1000-line resolution, its four different signal level components can be intercepted in their respective signal receiving areas shown in Fig. 91.

[0303] The picture quality of the four different components will be described in more detail. The illustration of Fig. 92 represents a combination of Figs. 86 and 91. As apparent, when the C/N rate increases, the overall signal level of amount of data is increased from 862d to 862a by steps of four signal levels $D_{1\text{-}1}$, $D_{1\text{-}2}$, $D_{2\text{-}1}$, $D_{2\text{-}2}$.

[0304] Also, as shown in Fig. 95, the four different level components LL, LH, HL, and HH are accumulated in proportion to the C/N rate. More specifically, the quality of a reproduced picture will be increased as the distance from a transmitter antenna becomes small. When L=Ld, LL component is reproduced. When L=Lc, LL+LH signal is reproduced. When L=Lb, LL+LH+HL signal is reproduced. When L=La, LL+LH+HL+HH signal is reproduced. As the result, if the bandwidth of the original signal is 1, the picture quality is enhanced at 1/4 increments of bandwidth from 1/4 to 1 depending on the receiving area. If the original signal is an HDTV of 1000-line vertical resolution, a reproduced TV signal is 250, 500, 750, and 1000 lines in the resolution at their respective receiving areas. The picture quality will thus be varied at steps depending on the level of a signal. Fig. 96 shows the signal propagation of a conventional digital HDTV signal transmission system, in which no signal reproduction will be possible when the C/N rate is less than V0. Also, signal interception will hardly be guaranteed at signal interference regions, shadow regions, and other signal attenuating regions, denoted by the symbol x, of the service area. Fig. 97 shows the signal propagation of an HDTV signal transmission system of the present invention. As shown, the picture quality will be a full 1000-line grade at the distance La where C/N=a, a 750-line grade at the distance Lb where C/N=b, a 500-line grade at the distance Lc where C/N=c, and a 250-line grade at the distance Ld where C/N=d. Within the distance La, there are shown unfavorable regions where the C/N rate drops sharply and no HDTV quality picture will be reproduced. As understood, a lower picture quality signal can however be intercepted and reproduced according to the multi-level signal transmission system of the present invention. For example, the picture quality will be a 750-line grade at the point B in a building shadow area, a 250-line grade at the point D in a running train, a 750-line grade at the point F in a ghost developing area, a 250-line grade at the point G in a running car, a 250-line grade at the point L in a neighbor signal interference area. As set forth above,

the signal transmission system of the present invention allows a TV signal to be successfully received at a grade in the area where the conventional system is poorly qualified, thus increasing its service area. Fig. 98 shows an example of simultaneous broadcasting of four different TV programs, in which three quality programs C, B, A are transmitted on their respective channels $D_{1\text{-}2}$, $D_{2\text{-}1}$, $D_{2\text{-}2}$ while a program D identical to that of a local analogue TV station is propagated on the $D_{1\text{-}1}$ channel. Accordingly, while the program D is kept available at simulcast service, the other three programs can also be distributed on air for offering a multiple program broadcast service.

Embodiment 8

[0305] Hereinafter, an eighth embodiment of the present invention will be explained referring to the drawings. The eighth embodiment employs a multi-level signal transmission system of the present invention for transmission/reception in a cellular telephone system.

[0306] Fig. 115 is a block diagram showing a transmitter/receiver of a portable telephone, in which a telephone conversation sound inputted across a microphone 762 is compressed and coded in a compressor 405 into multi-level, D_1, D_2, and D_3, data previously described. These D_1, D_2, and D_3 data are time divided in a time division circuit 765 into predetermined time slots and, then, modulated in a modulator 4 into a multi-level, e.g. SRQAM, signal previously described. Thereafter, an antenna sharing unit 764 and an antenna 22 transmit a carrier wave carrying a modulated signal, which will be intercepted by a base station later described and further transmitted to other base stations or a central telephone exchanger so as to communicate with other telephones.

[0307] On the contrary, the antenna 22 receives transmission radio waves from other base stations as communication signals from other telephones. A received signal is demodulated in a multiple-level, e.g. SRQAM, type demodulator 45 into D_1, D_2, and D_3 data. A timing circuit 767 detects timing signals on the basis of demodulated signals. These timing signals are fed into the time division circuit 765. Demodulated signals D_1, D_2, and D_3 are fed into an expander 503 and expanded into a sound signal, which is then transmitted to a speaker 763 and converted into sound.

[0308] Fig. 116 shows a block diagram exemplarily showing an arrangement of base stations, in which three base stations 771, 772, and 773 locate at center of respective receiving cells 768, 769, and 770 of hexagon or circle. These base stations 771, 772, and 773 respectively has a plurality of transmitter/receiver units 761a~761j each similar to that of Fig. 115 so as to have data communication channels equivalent to the number of these transmitter/receiver units. A base station controller 774 is connected to all the base stations and always monitors a communication traffic amount of each base station. Based on the monitoring result, the base station controller 774 carries out an overall system control including allocation of channel frequencies to respective base stations or control of receiving cells of respective base stations.

[0309] Fig. 117 is a view showing a traffic distribution of communication amount in a conventional, e.g. QPSK, system. A diagram d=A shows data 774a and 774b having frequency utilization efficiency 2 bit/Hz, and a diagram d=B shows data 774c having frequency utilization efficiency 2 bit/Hz. A summation of these data 774a, 774b, and 774c becomes a data 774d, which represents a transmission amount of Ach consisting of receiving cells 768 and 770. Frequency utilization efficiency of 2 bit/Hz is uniformly distributed. However, density of population in an actual urban area is locally high in several crowded areas 775a, 775b, and 775c which include buildings concentrated.. A data 774e representing a communication traffic amount shows several peaks at locations just corresponding to these crowded areas 775a, 775b, and 775c, in contrast with other area having small communication amount. A capacity of a conventional cellular telephone was uniformly set to 2 bit/Hz frequency efficiency at entire region as shown by the data 774d irrespective of actual traffic amount TF shown by the data 774e. It is not effective to give the same frequency efficiency regardless of actual traffic amount. In order to compensate this ineffectiveness, the conventional systems have allocated many frequencies to the regions having a large traffic amount, increased channel number, or decreased the receiving cell of the same. However, an increase of channel number is restricted by the frequency spectrum. Furthermore, conventional multi-level, e.g. 16 QAM or 64 QAM, mode transmission systems increase transmission power. A reduction of receiving cell will induce an increase in number of base stations, which will increase installation cost.

[0310] It is ideal for the improvement of an overall system efficiency to increase the frequency efficiency of the region having a larger traffic amount and decrease the frequency efficiency of the region having a smaller traffic amount. A multi-level signal transmission system in accordance with the present invention realizes this ideal modification. This will be explained with reference to Fig. 118 showing a communication amount & traffic distribution in accordance with the eighth embodiment of the present invention.

[0311] More specifically, Fig. 118 shows communication amounts of respective receiving cells 770b, 768, 769, 770, and 770a taken along a line A-A'. The receiving cells 768 and 770 utilize frequencies of a channel group A, while the receiving cells 770b, 769, and 770a utilize frequencies of a channel group B which does not overlap with the channel group A. The base station controller 774 shown in Fig. 116 increases or decreases channel number of these channels in accordance with the traffic amount of respective receiving cells. In Fig. 118, a diagram d=A represents a distribution of a com-

munication amount of the A channel. A diagram d=B represents a distribution of a communication amount of the B channel. A diagram d=A+B represents a distribution of a communication amount of all the channels. A diagram TF represents a communication traffic amount, and a diagram P shows a distribution of buildings and population.

[0312] The receiving cells 768, 769, and 770 employ the multi-level, e.g. SRQAM, signal transmission system. Therefore, it is possible to obtain a frequency utilization efficiency of 6 bit/Hz, three times as large as 2 bit/Hz of QPSK, in the vicinity of the base stations as denoted by data 776a, 776b, and 776c. Meanwhile, the frequency utilization efficiency decreases at steps from 6 bit/Hz to 4 bit/Hz, and 4 bit/Hz to 2 bit/Hz, as it goes to suburban area. If the transmission power is insufficient, 2 bit/Hz areas become narrower than the receiving cells, denoted by dotted lines 777a, 777b, 777c, of QPSK. However, an equivalent receiving cell will be easily obtained by slightly increasing the transmission power of the base stations.

[0313] Transmitting/receiving operation of a mobile station capable of responding to a 64 SRQAM signal is carried out by use of modified QPSK, which is obtained by set a shift amount of SRQAM to S=1, at the place far from the base station, by use of 16 SRQAM at the place not so far from the same, and 64 SRQAM at the nearest place. Accordingly, the maximum transmission power does not increase as compared with QPSK.

[0314] Furthermore, 4 SRQAM type transmitter/receiver, whose circuit configuration is simplified as shown in a block diagram of Fig. 121, will be able to communicate with other telephones while maintaining compatibility. That will be the same in 16 SRQAM type transmitter/receiver shown in a block diagram of Fig. 122. As a result, three different type telephones having different modulation systems will be provided. Small in size and light in weight is important for portable telephones. In this regard, the 4 SRQAM system having a simple circuit configuration will be suitable for the users who want a small and light telephone although its frequency utilization efficiency is low and therefore cost of call may increase. In this manner, the present invention system can suit for a wide variety of usage.

[0315] As is explained above, the transmission system having a distribution like d=A+B of Fig. 118, whose capacity is locally altered, is accomplished. Therefore, an overall frequency utilization efficiency will be much effectively improved if layout of base stations is determined to fit for the actual traffic amount denoted by TF. Especially, effect of the present invention will be large in a micro cell system, whose receiving cells are smaller and therefore numerous sub base stations are required. Because a large number of sub base stations can be easily installed at the place having a large traffic amount.

[0316] Next, data assignment of each time slot will be explained referring to Fig, 119, wherein Fig. 119(a) shows a conventional time slot and Fig. 119(b) shows a time slot according to the eighth embodiment. The conventional system performs a down, i.e. from a base station to a mobile station, transmission as shown in Fig. 119(a), in which a sync signal S is transmitted by a time slot 780a and transmission signals to respective portable phones of A, B, C channels by time slots 780b, 780c, 780d respectively at a frequency A. On the other hand, an up, i.e. from the mobile station to the base station, transmission is performed in such a manner that a sync signal S, and transmission signals of a, b, c channels are transmitted by time slots 781a, 781b, 781c, 781d at a frequency B.

[0317] The present invention, which is characterized by a multi-level, e.g. 64 SRQAM, signal transmission system, allows to have three-level data consisting of D_1, D_2, D_3 of 2 bit/Hz as shown in Fig. 119(b). As both of A_1 and A_2 data are transmitted by 16 SRQAM, their time slots have two times data rate as shown by slots 782b, 782c and 783b, 783c. It means the same quality sound can be transmitted by a half time. Accordingly, a time width of respective time slots 782b, 782c becomes a half. In this manner, two times transmission capacity can be acquired at the two-level region 776c shown in Fig. 118, i.e. in the vicinity of the base station.

[0318] In the same way, time slots 782g, 783g carry out the transmission/reception of E1 data by use of a 64 SRQAM signal. As the transmission capacity is three times, one time slot can be used for three channels of E_1, E_2, E_3. This would be used for a region further close to the base station. Thus, up to three times communication capacity can be obtained at the same frequency band. An actual transmission efficiency, however, would be reduced to 90%. It is desirable for enhancing the effect of the present invention to coincide the transmission amount distribution according to the present invention with the regional distribution of the actual traffic amount as perfect as possible.

[0319] In fact, an actual urban area consists of a crowded building district and a greenbelt zone surrounding this building area. Even an actual suburb area consists of a residential district and fields or a forest surrounding this residential district. These urban and suburb areas resemble the distribution of the TF diagram. Thus, the application of the present invention will be effective.

[0320] Fig. 120 is a diagram showing time slots by the TDMA method, wherein Fig. 120(a) shows a conventional method and Fig. 120(b) shows the present invention. The conventional method uses time slots 786a, 786b for transmission to portable phones of A, B channels at the same frequency and time slots 787a, 787b for transmission from the same, as shown in Fig. 120(a).

[0321] On the contrary, 16 SRQAM mode of the present invention uses a time slot 788a for reception of A_1 channel and a time slot 788c for transmission to A_1 channel as shown in Fig. 120(b). A width of the time slot becomes approximately 1/2. In case of 64 SRQAM mode, a time slot 788i is used for reception of D_1 chan-

nel and a time slot 7881 is used for transmission to D_1 channel. A width of the time slot becomes approximately 1/3.

[0322] In order to save electric power, a transmission of E_1 channel is executed by use of a normal 4 SRQAM time slot 788r while reception of E_1 channel is executed by use of a 16 SRQAM time slot 788p being a 1/2 time slot. Transmission power is surely suppressed, although communication cost may increase due to a long occupation time. This will be effective for a small and light portable telephone equipped with a small battery or when the battery is almost worn out.

[0323] As is described in the foregoing description, the present invention makes it possible to determine the distribution of transmission capacity so as to coincide with an actual traffic distribution, thereby increasing substantial transmission capacity. Furthermore, the present invention allows base stations or mobile stations to freely select one among two or three transmission capacities. If the frequency utilization efficiency is selected lower, power consumption will be decreased. If the frequency utilization efficiency is selected higher, communication cost will be saved. Moreover, adoption of a 4 SRQAM mode having smaller capacity will simplify the circuitry and reduce the size and cost of the telephone. As explained in the previous embodiments, one characteristics of the present invention is that compatibility is maintained among all of associated stations. In this manner, the present invention not only increases transmission capacity but allows to provide customers a wide variety of series from a super mini telephone to a high performance telephone.

Embodiment 9

[0324] Hereinafter, a ninth embodiment of the present invention will be described referring to the drawings. The ninth embodiment employs this invention in an OFDM transmission system. Fig. 123 is a block diagram of an OFDM transmitter/receiver, and Fig. 124 is a diagram showing a principle of an OFDM action. An OFDM is one of FDM and has a better efficiency in frequency utilization as compared with a general FDM, because an OFDM sets adjacent two carriers to be quadrature with each other. Furthermore, an OFDM can bear multipath obstruction such as ghost and, therefore, may be applied in the future to the digital music broadcasting or digital TV broadcasting.

[0325] As shown in the principle diagram of Fig. 124, an OFDM converts an input signal by a serial to parallel converter 791 into a data being disposed on a frequency axis 793 at intervals of 1/ts, so as to produce subchannels 794a~794e. This signal is inversely FFT converted by a modulator 4 having an inverse FFT 40 into a signal on a time axis 799 to produce a transmission signal 795. This inverse FFT signal is transmitted during an effective symbol period 796 of the time period ts. A guard interval 797 having an amount tg is provided between respective symbol periods.

[0326] A transmitting/receiving action of an HDTV signal in accordance with this ninth embodiment will be explained referring to the block diagram of Fig. 123, which shows a hybrid OFDM-CCDM system. An inputted HDTV signal is separated by a video encoder 401 into three-level, a low frequency band $D_{1\text{-}1}$, a medium-low frequency band $D_{1\text{-}2}$, and a high-medium-low frequency band D_2, video signals, and fed into an input section 742.

[0327] In a first data stream input 743, a $D_{1\text{-}1}$ signal is ECC encoded with high code gain and a $D_{1\text{-}2}$ signal is ECC encoded with normal code gain. A TDM 743 performs time division multiplexing of $D_{1\text{-}1}$ and $D_{1\text{-}2}$ signals to produce a D_1 signal, which is then fed to a D_1 serial to parallel converter 791d in a modulator 852a. The D_1 signal consists of n pieces of parallel data, which are inputted into first inputs of n pieces of C-CDM modulator 4a, 4b,---respectively.

[0328] On the other hand, the high frequency band signal D_2 is fed into a second data stream input 744 of the input section 742, in which the D_2 signal is ECC (Error Correction Code) encoded in an ECC 744a and then Trellis encoded in a Trellis encoder 744b. Thereafter, the D_2 signal is supplied to a D_2 serial to parallel converter 791b of the modulator 852a and converted into n pieces of parallel data, which are inputted into second inputs of the n pieces of C-CDM modulator 4a, 4b,---respectively.

[0329] The C-CDM modulators 4a, 4b, 4c---respectively produces 16 SRQAM signal on the basis of the D_1 data of the first data stream input and the D_2 data of the second data stream input. These n pieces of C-CDM modulator respectively has a carrier different from each other. As shown in Fig. 124, carriers 794a, 794b, 794c,---are arrayed on the frequency axis 793 so that adjacent two carriers are 90°-out-of-phase with each other. Thus C-CDM modulated n pieces of modulated signal are fed into the inverse FFT circuit 40 and mapped from the frequency axis dimension 793 to the time axis dimension 790. Thus, time signals 796a, 796b ---, having an effective symbol length ts, are produced. There is provided a guard interval zone 797a of Tg seconds between the effective symbol time zones 796a and 796b, in order to reduce multipath obstruction. Fig. 129 is a graph showing a relationship between time axis and signal level. The guard time Tg of the guard interval band 797a is determined by taking account of multipath affection and usage of signal. By setting the guard time Tg longer than the multipath affection time, e.g. TV ghost, modulated signals from the inverse FFT circuit 40 are converted by a parallel to serial converter 4e into one signal and, then, transmitted from a transmitting circuit 5 as an RF signal.

[0330] Next, an action of a receiver 43 will be described. A received signal, shown as time-base symbol signal 796e of Fig. 124, is fed into an input circuit 24 of Fig. 123. Then, the received signal is converted into a digital signal in a demodulator 852b and further changed

into Fourier coefficients in an FFT 40a. Thus, the signal is mapped from the time axis 799 to the frequency axis 793a as shown in Fig. 124. That is, the time-base symbol signal is converted into frequency-base carriers 794a, 794b,---. As these carriers are in quadrature relationship with each other, it is possible to separate respective modulated signals. Fig. 125(b) shows thus demodulated 16 SRQAM signal, which is then fed to respective C-CDM demodulators 45a, 45b,--of a C-CDM demodulator 45, in which demodulated 16 SRQAM signal is demodulated into multi-level sub signals D_1, D_2. These sub signals D_1 and D_2 are further demodulated by a D_1 parallel to serial converter 852a and a D_2 parallel to serial converter 852b into the original D_1 and D_2 signals.

[0331] Since the signal transmission system is of C-CDM multi-level shown in 125(b), both D_1 and D_2 signals will be level shown in 125(b), both D_1 and D_2 signals will be demodulated under better receiving condition but only D_1 signal will be demodulated under worse, e.g. low C/N rate, receiving condition. Demodulated D_1 signal is demodulated in an output section 757. As the D_{1-1} signal has higher ECC code gain as compared with the D_{1-2} signal, an error signal of the D_{1-1} signal is reproduced even under worse receiving condition.

[0332] The D_{1-1} signal is converted by a 1-1 video decoder 402c into a low frequency band signal and outputted as an LDTV, and the D_{1-2} signal is converted by a 1-2 video decoder 402d into a medium frequency band signal and outputted as EDTV.

[0333] The D_2 signal is Trellis decoded by a Trellis decoder 759b and converted by a second video decoder 402b into a high frequency band signal and outputted as an HDTV signal. Namely, an LDTV signal is outputted in case of the low frequency band signal only. An EDTV signal of wide NTSC grade is outputted if the medium frequency band signal is added to the low frequency band signal, and an HDTV signal is produced by adding low, medium, and high frequency band signals. As well as the previous embodiment, a TV signal having a picture quality depending on a receiving C/N rate can be received. Thus, the ninth embodiment realizes a novel multi-level signal transmission system by combining an OFDM and a C-CDM, which was not obtained by the OFDM alone.

[0334] An OFDM is certainly strong against multipath such as TV ghost because the guard time Tg can absorb an interference signal of multipath. Accordingly, the OFDM is applicable to the digital TV broadcasting for automotive vehicle TV receivers. Meanwhile, no OFDM signal is received when the C/N rate is less than a predetermined value because its signal transmission pattern is not of a multi-level type.

[0335] However the present invention can solve this disadvantage by combining the OFDM with the C-CDM, thus realizing a graditional degradation depending on the C/N rate in a video signal reception without being disturced by multipath.

[0336] When a TV signal is received in a compartment of a vehicle, not only the reception is disturbed by multipath but the C/N rate is deteriorated. Therefore, the broadcast service area of a TV broadcast station will not be expanded as expected if the countermeasure is only for multipath.

[0337] On the other hand, a reception of TV signal of at least LDTV grade will be ensured by the combination with the multi-level transmission C-CDM even if the C/N rate is fairly deteriorated. As a picture plane size of an automotive vehicle TV is normally less than 100 inches, a TV signal of an LDTV grade will provide a satisfactory picture quality. Thus, the LDTV grade service area of automotive vehicle TV will largely expanded. If an OFDM is used in an entire frequency band of HDTV signal, the present semiconductor technologies cannot prevent circuit scale from increasing so far.

[0338] Now, an OFDM method of transmitting only D_{1-1} of low frequency band TV signal will be explained below. As shown in a block diagram in Fig. 138, a medium frequency band component D_{1-2} and a high frequency band component D_2 of an HDTV signal are multiplexed in a C-CDM modulator 4a, and then transmitted at a frequency band A through an FDM 40d.

[0339] On the other hand, a signal received by a receiver 43 is first of all frequency separated by an FDM 40e and, then, demodulated by a C-CDM demodulator 4c of the present invention. Thereafter, thus C-CDM demodulated signal is reproduced into medium and high frequency components of HDTV in the same way as in Fig. 123. An operation of a video decoder 402 is identical to that of embodiments 1, 2, and 3 and will no more be explained.

[0340] Meanwhile, the D_{1-1} signal, a low frequency band signal of MPEG 1 grade of HDTV, is converted by a serial to parallel converter 791 into a parallel signal and fed to an OFDM modulator 852c, which executes a QPSK or 16 QAM modulation. Subsequently, the D_{1-1} signal is converted by an inverse FFT 40 into a time-base signal and transmitted at a frequency band B through the FDM 40d.

[0341] On the other hand, a signal received by the receiver 43 is frequency separated in the FDM 40e and, then, converted into a number of frequency-base signals in an FFT 40a of the OFDM modulator 852d. Thereafter, frequency-base signals are demodulated in respective demodulators 4a, 4b,---and are fed into a parallel to serial converter 882a, wherein a D_{1-1} signal is demodulated. Thus, a D_{1-1} signal of LDTV grade is outputted from the receiver 43.

[0342] In this manner, only an LDTV signal is OFDM modulated in the multi-level signal transmission. The system of Fig. 138 makes it possible to provide a complicated OFDM circuit only for an LDTV signal. A bit rate of LDTV signal is 1/20 of that of an HDTV. Therefore, the circuit scale of the OFDM will be reduced to 1/20, which results in an outstanding reduction of overall circuit scale.

[0343] An OFDM signal transmission system is strong against multipath and will soon be applied to a mobile station, such as a portable TV, an automotive vehicle TV, or a digital music broadcast receiver, which is exposed under strong and variable multipath obstruction. For such usages a small picture size of less than 10 inches, 4 to 8 inches, is the mainstream. It will be thus guessed that the OFDM modulation of a high resolution TV signal such as HDTV or EDTV will bring less effect. In other words, the reception of a TV signal of LDTV grade would be sufficient for an automotive vehicle TV.

[0344] On the contrary, multipath is constant at a fixed station such as a home TV. Therefore, a countermeasure against multipath is relatively easy. Less effect will be brought to such a fixed station by OFDM unless it is in a ghost area. Using OFDM for medium and high frequency band components of HDTV is not advantageous in view of present circuit scale of OFDM which is still large.

[0345] Accordingly, the method of the present invention, in which OFDM is used only for a low frequency band TV signal as shown in Fig. 138, can widely reduce the circuit scale of the OFDM to less than 1/10 without losing inherent OFDM effect capable of largely reducing multiple obstruction of LDTV when received at a mobile station such as an automotive vehicle.

[0346] Although the OFDM modulation of Fig. 138 is performed only for D_{1-1} signal, it is also possible to modulate both D_{1-1} and D_{1-1} by OFDM. In such a case, a C-CDM two-level signal transmission is used for transmission of D_{1-1} and D_{1-2}. Thus, a multi-level broadcasting being strong against multipath will be realized for a vehicle such as an automotive vehicle. Even in a vehicle, the graditional graduation will be realized in such a manner that LDTV and SDTV signals are received with picture qualities depending on receiving signal level or antenna sensitivity.

[0347] The multi-level signal transmission according to the present invention is feasible in this manner and produces various effects as previously described. Furthermore, if the multi-level signal transmission of the present invention is incorporated with an OFDM, it will become possible to provide a system strong against multipath and to alter data transmission grade in accordance with receivable signal level change.

[0348] The multi-level signal transmission method of the present invention is intended to increase the utilization of frequencies but may be suited for not all the transmission systems since causing some type receivers to be declined in the energy utilization. It is a good idea for use with a satellite communications system for selected subscribers to employ most advanced transmitters and receivers designed for best utilization of applicable frequencies and energy. Such a specific purpose signal transmission system will not be bound by the present invention.

[0349] The present invention will be advantageous for use with a satellite or terrestrial broadcast service which is essential to run in the same standards for as long as 50 years. During the service period, the broadcast standards must not be altered but improvements will be provided time to time corresponding to up-to-date technological achievements. Particularly, the energy for signal transmission will surely be increased on any satellite. Each TV station should provide a compatible service for guaranteeing TV program signal reception to any type receivers ranging from today's common ones to future advanced ones. The signal transmission system of the present invention can provide a compatible broadcast service of both the existing NTSC and HDTV systems and also, ensure a future extension to match mass data transmission.

[0350] The present invention concerns much on the frequency utilization than the energy utilization. The signal receiving sensitivity of each receiver is arranged different depending on a signal state level to be received so that the transmitting power of a transmitter needs not be increased largely. Hence, existing satellites which offer a small energy for reception and transmission of a signal can best be used with the system of the present invention. The system is also arranged for performing the same standards corresponding to an increase in the transmission energy in the future and offering the compatibility between old and new type receivers. In addition, the present invention will be more advantageous for use with the satellite broadcast standards.

[0351] The multi-level signal transmission method of the present invention is more preferably employed for terrestrial TV broadcast service in which the energy utilization is not crucial, as compared with satellite broadcast service. The results are such that the signal attenuating regions in a service area which are attributed to a conventional digital HDTV broadcast system are considerably reduced in extension and also, the compatibility of an HDTV receiver or display with the existing NTSC system is obtained. Furthermore, the service area is substantially increased so that program suppliers and sponsors can appreciate more viewers. Although the embodiments of the present invention refer to 16 and 32 QAM procedures, other modulation techniques including 64, 128, and 256 QAM will be employed with equal success. Also, multiple PSK, ASK, and FSK techniques will be applicable as described with the embodiments.

[0352] A combination of the TDM with the SRQAM of the present invention has been described in the above. However, the SRQAM of the present invention can be combined also with any of the FDM, CDMA and frequency dispersal communications systems.

Claims

1. An OFDM Orthogonal Frequency Division Multiplex receiver comprising:

a Fast Fourier transformer (FFT;40a) for converting a received signal into a group of modulation signals of a plurality of carriers (794; f1, f2, f3, ...) by applying a Fourier transformation;
a demodulator (45) for demodulating said modulation signals;
an error correcting section (757) for error correcting the demodulation signals demodulated by said demodulator;

wherein said demodulator (45) is adapted to demodulate said modulation signal in a first mode as a signal consisting of n signal points (83-86) in a constellation (91-94) into an n-value signal to reproduce a first data stream, and in a second mode, to demodulate said modulation signal as a signal consisting of m signal points in a constellation into an m-value signal to reproduce a second data stream, where m in an integer larger than n, said demodulator (45) selecting between said first and second modes according to said received signal.

Patentansprüche

1. Eine OFDM Orthogonal-Frequenz-Divisions-Multiplex-Empfangsvorrichtung umfassend:

einen Fast-Fourier-Transformator (FFT; 40a) zum Konvertieren eines empfangenen Signals in eine Gruppe von Modulationssignalen einer Vielzahl von Trägern (794; f1, f2, f3,...) durch Anwendung einer Fourier-Transformation;
einen Demodulator (45) zum Demodulieren der genannten Modulationssignale;
eine Fehlerkorrektureinheit (757) zur Fehlerkorrektur der von dem genannten Demodulator demodulierten Demodulationssignale;

wobei der genannte Demodulator (45) ausgestaltet ist zum Demodulieren des genannten Modulationssignals in einem ersten Modus als ein Signal, das aus n Signalpunkten (83-86) in einer Konstellation (91, 94) besteht, in ein n-wertiges Signal, um einen ersten Datenstrom zu erzeugen, und in einem zweiten Modus zum Demodulieren des genannten Demodulationssignals als ein Signal, das aus m Signalpunkten besteht in einer Konstellation, in ein m-wertiges Signal, um einen zweiten Datenstrom zu erzeugen,
wobei m eine ganze Zahl größer als n ist und wobei der genannte Demodulator (45) zwischen dem genannten ersten und zweiten Modus entsprechend dem genannten empfangenen Signal auswählt.

Revendications

1. Récepteur multiplex à division par frequences orthogonales, comportant :

un transformateur Fourier rapide (FFT; 40a) pour convertir un signal reçu en un groupe de signaux de modulation d'une pluralité de porteurs ((794; f1, f2, f3...) en appliquant une transformation de Fourier;
un démodulateur pour démoduler lesdits signaux de modulation;
une section de correction d'erreurs (757) pour corriger des erreurs dans les signaux de demodulation, démodulés par ledit démodulateur;

ledit démodulateur (45) étant conçu de façon à démoduler ledit signal de modulation, selon un premier mode, en tant que signal consistant en n points de signal (83-86) en une constellation (91-94) en un signal de n-valeurs afin de produire un premier flux de données et, en un second mode , de démoduler ledit signal de modulation en tant que signal consistant de m points de signal en une constellation en signal en m-valeurs, afin de produire un second flux de données, où m est un chiffre entier plus grand que n, ledit démodulateur (45) sélectionnant l'un ou l'autre desdits premier et second modes selon le signal reçu.

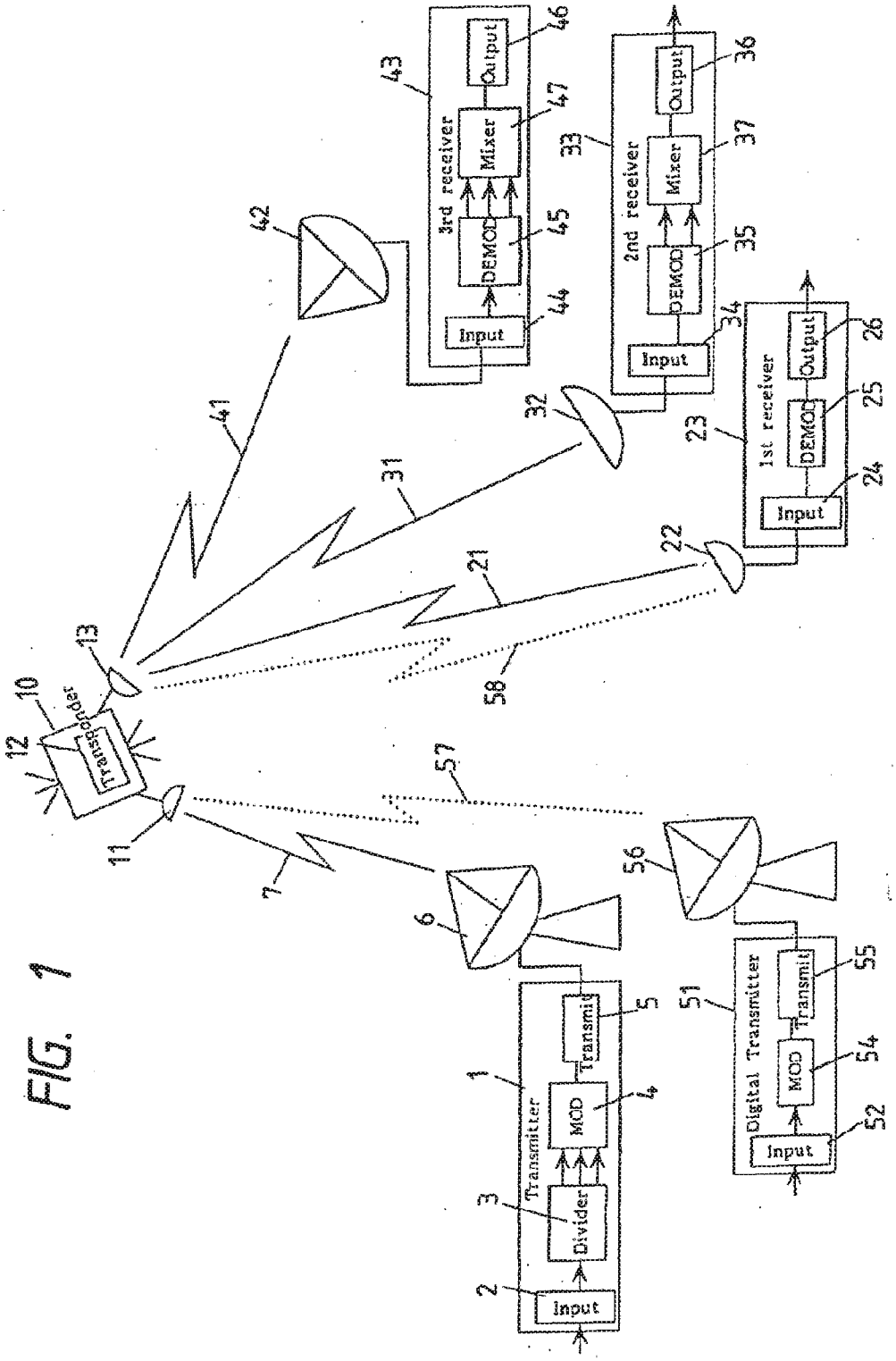
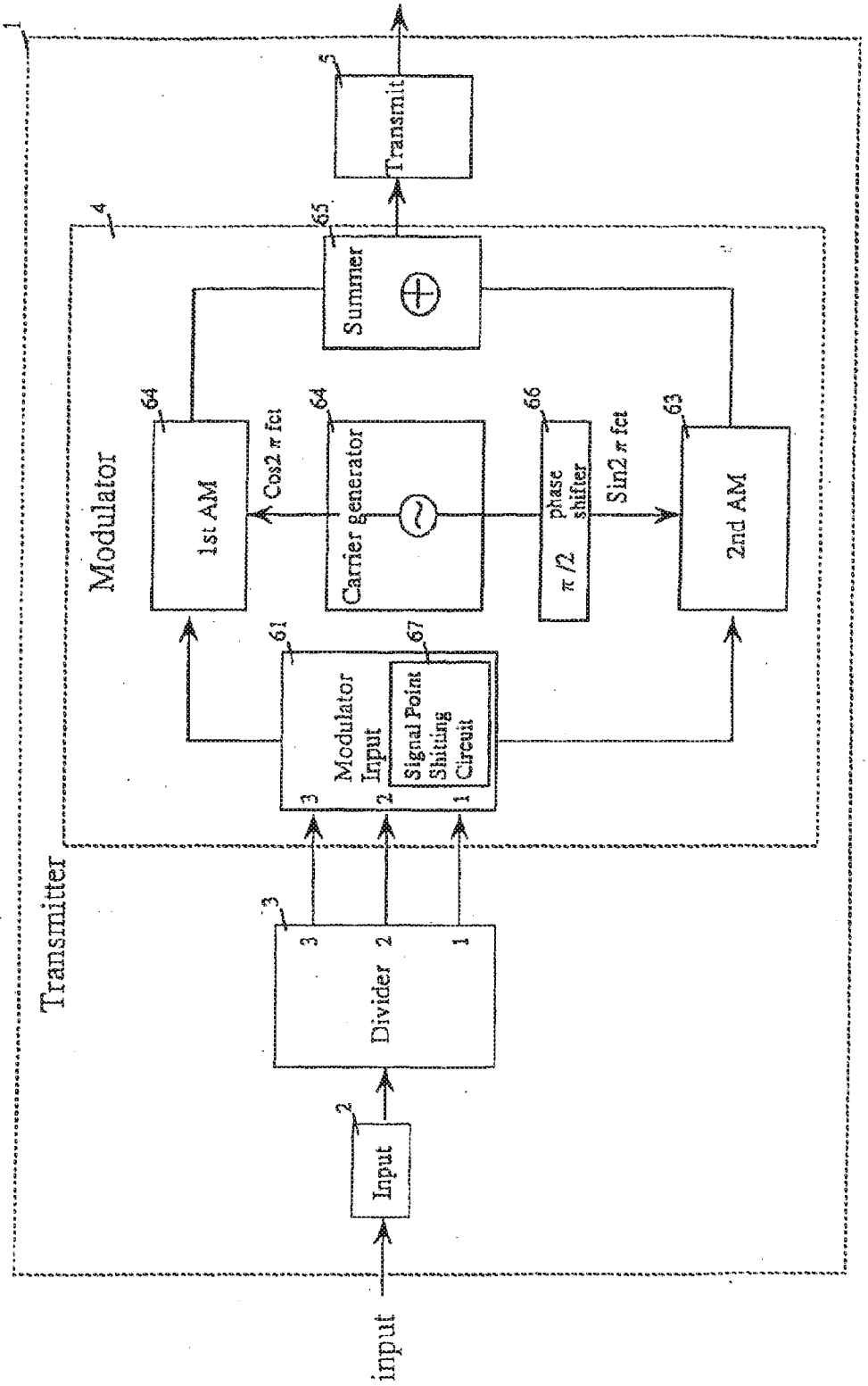


FIG. 1

FIG. 2



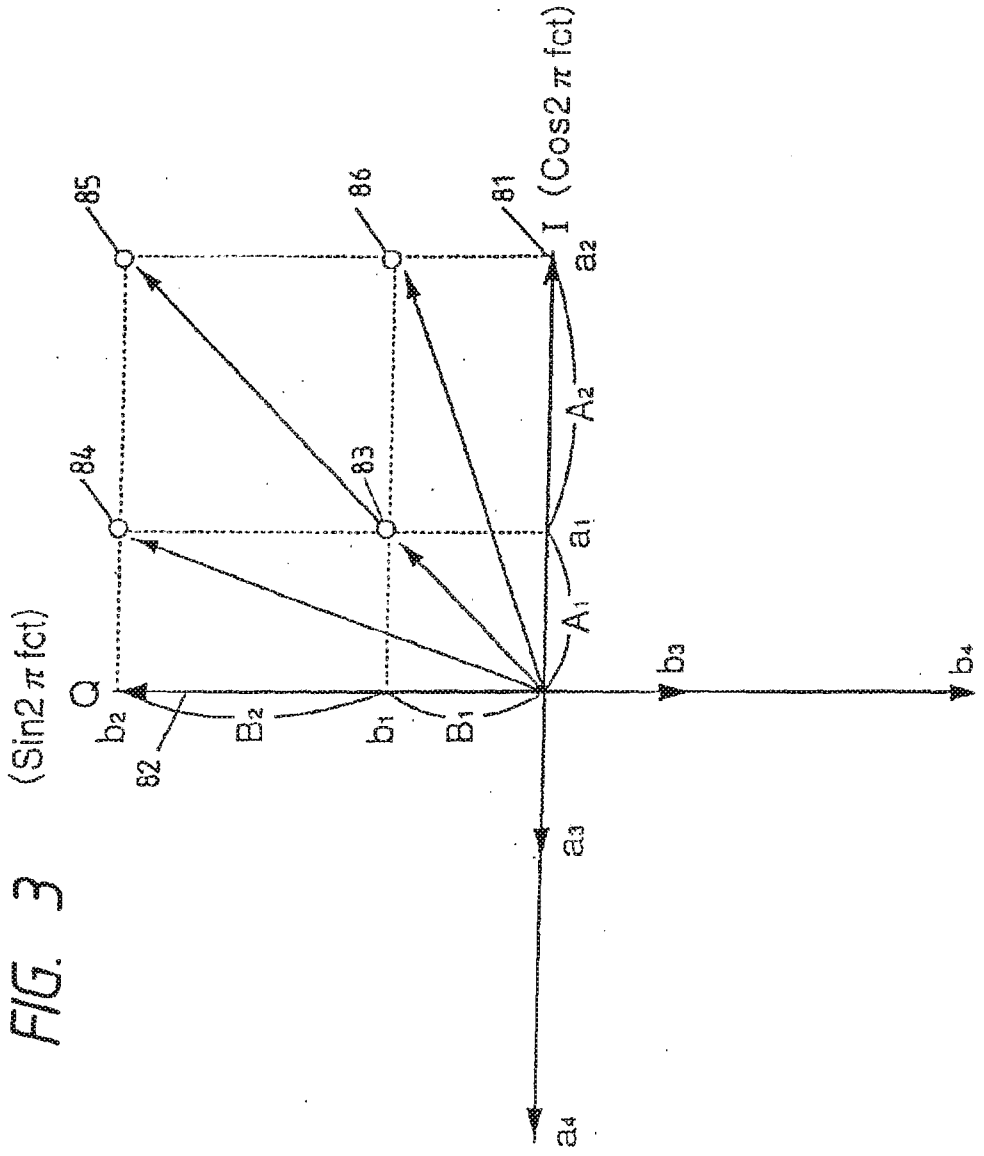


FIG. 3

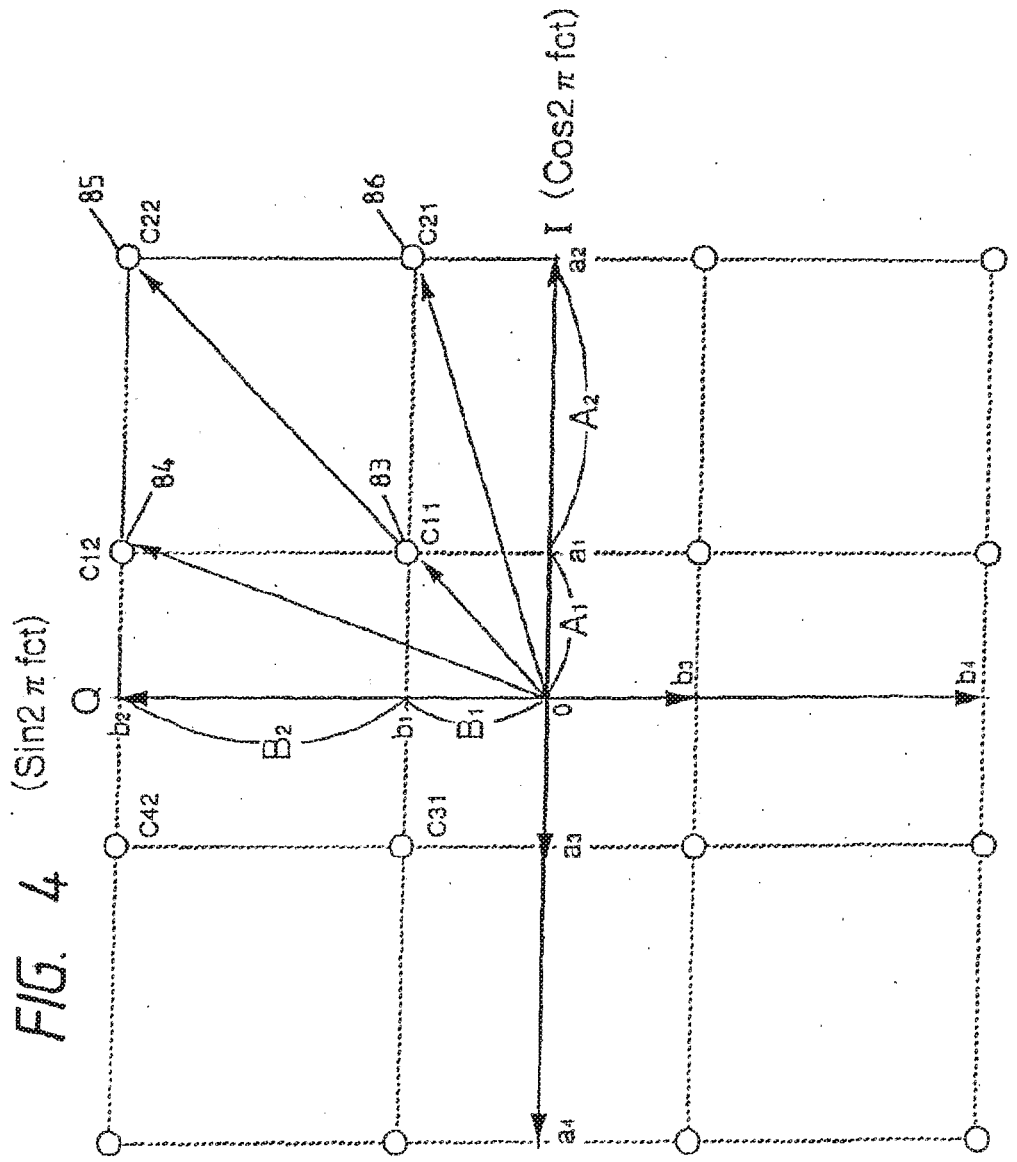


FIG. 4

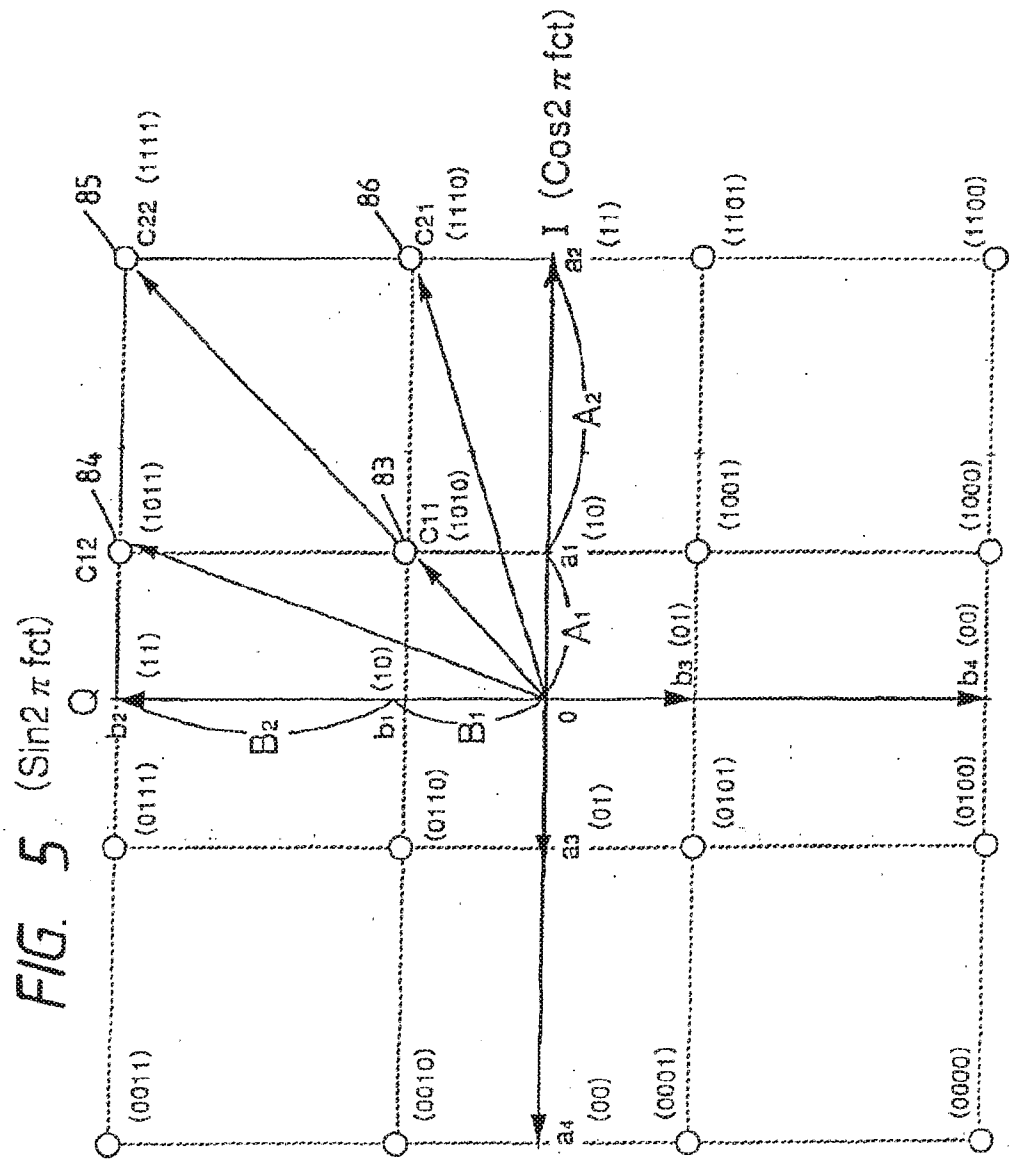

I (Cos2 π fct)
Q (Sin2 π fct)
85
86
84
83
C22 (1111)
C21 (1110)
C12
C11 (1010)
(1011)
(1101)
(1100)
(1001)
(1000)
(0111)
(0110)
(0101)
(0100)
(0011)
(0010)
(0001)
(0000)
a2 (11)
a1 (10)
a3 (01)
a4 (00)
A1
A2
B1
B2
b1 (10)
b2 (11)
b3 (01)
b4 (00)
0

FIG. 5

FIG. 6

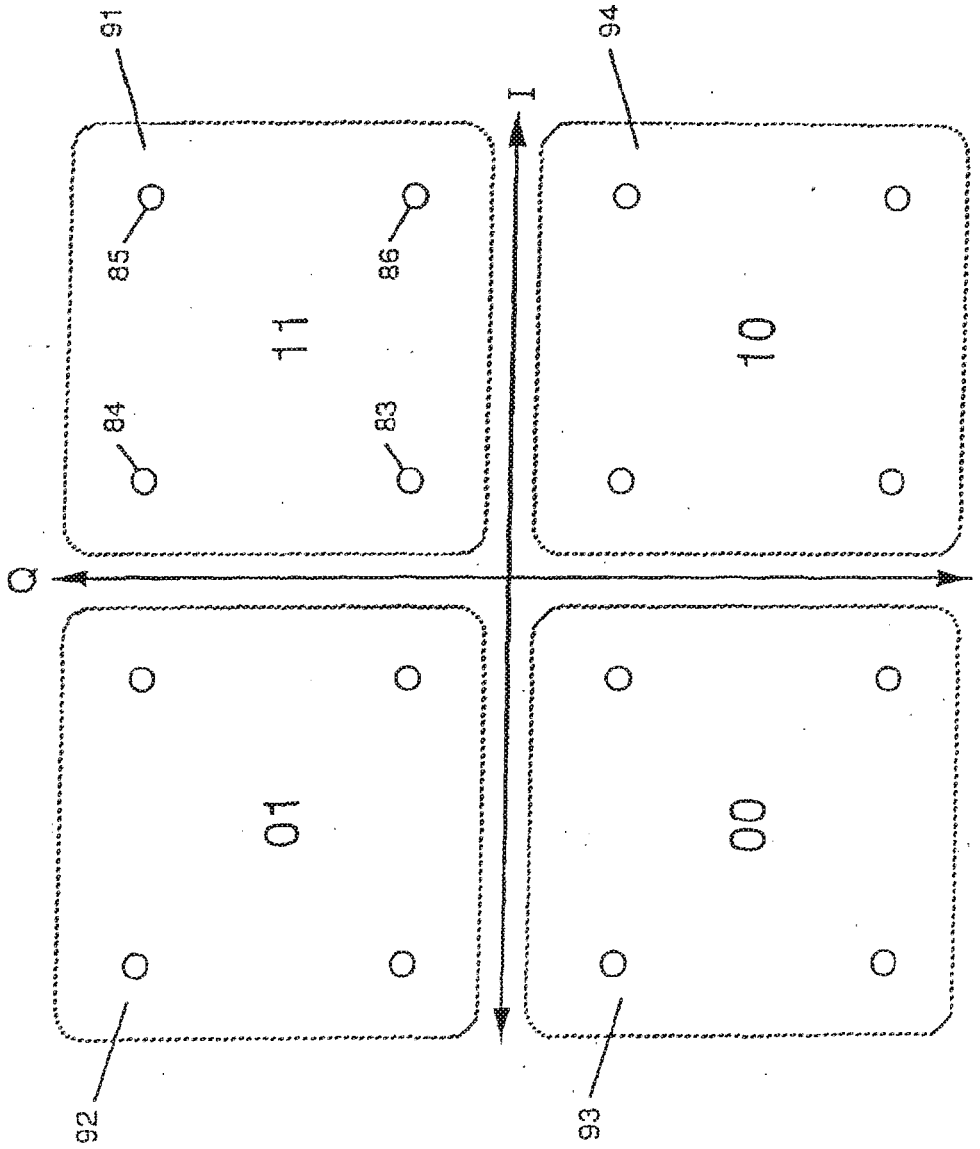


FIG. 7

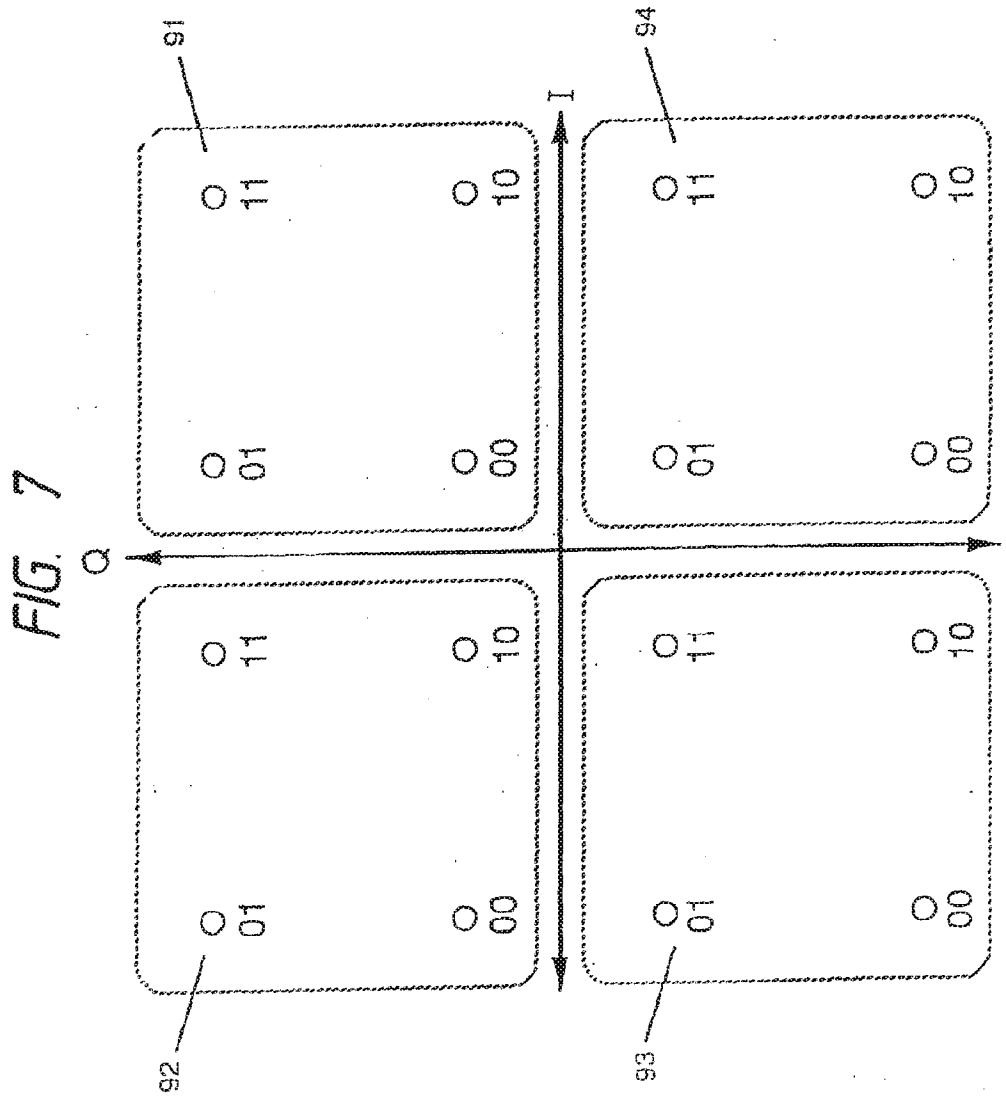


FIG. 8

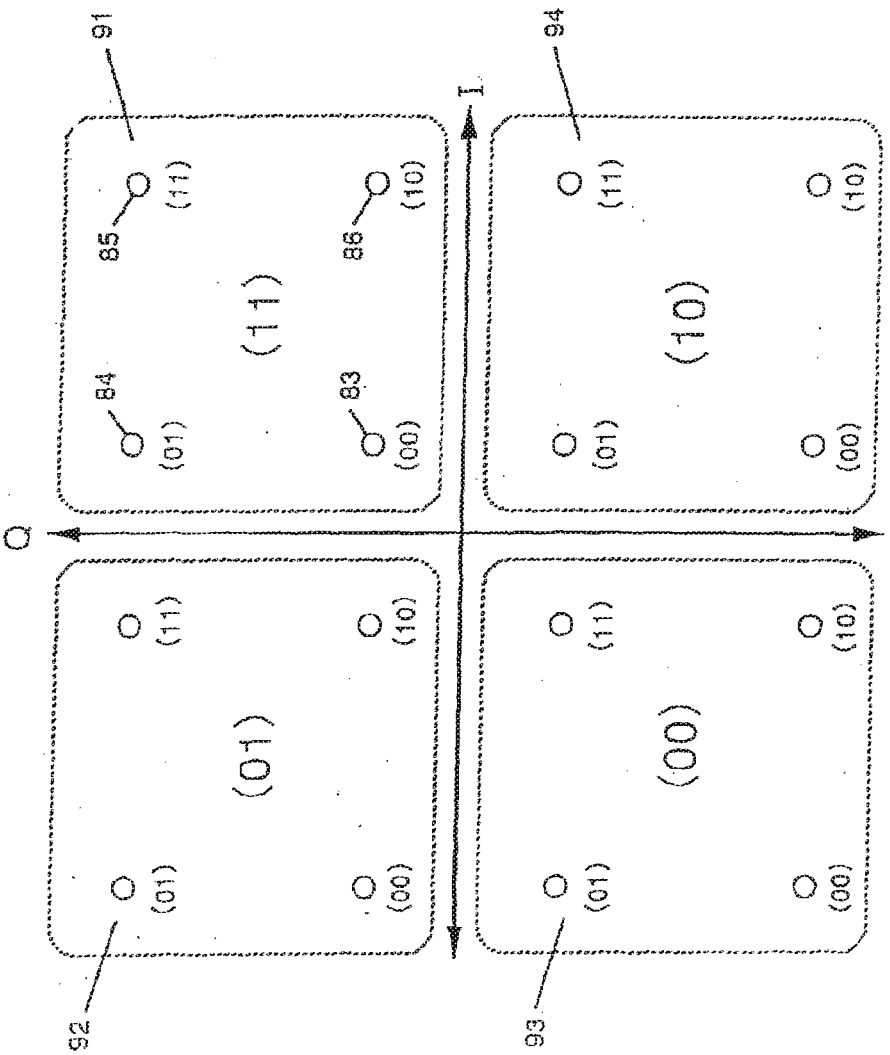


FIG. 9

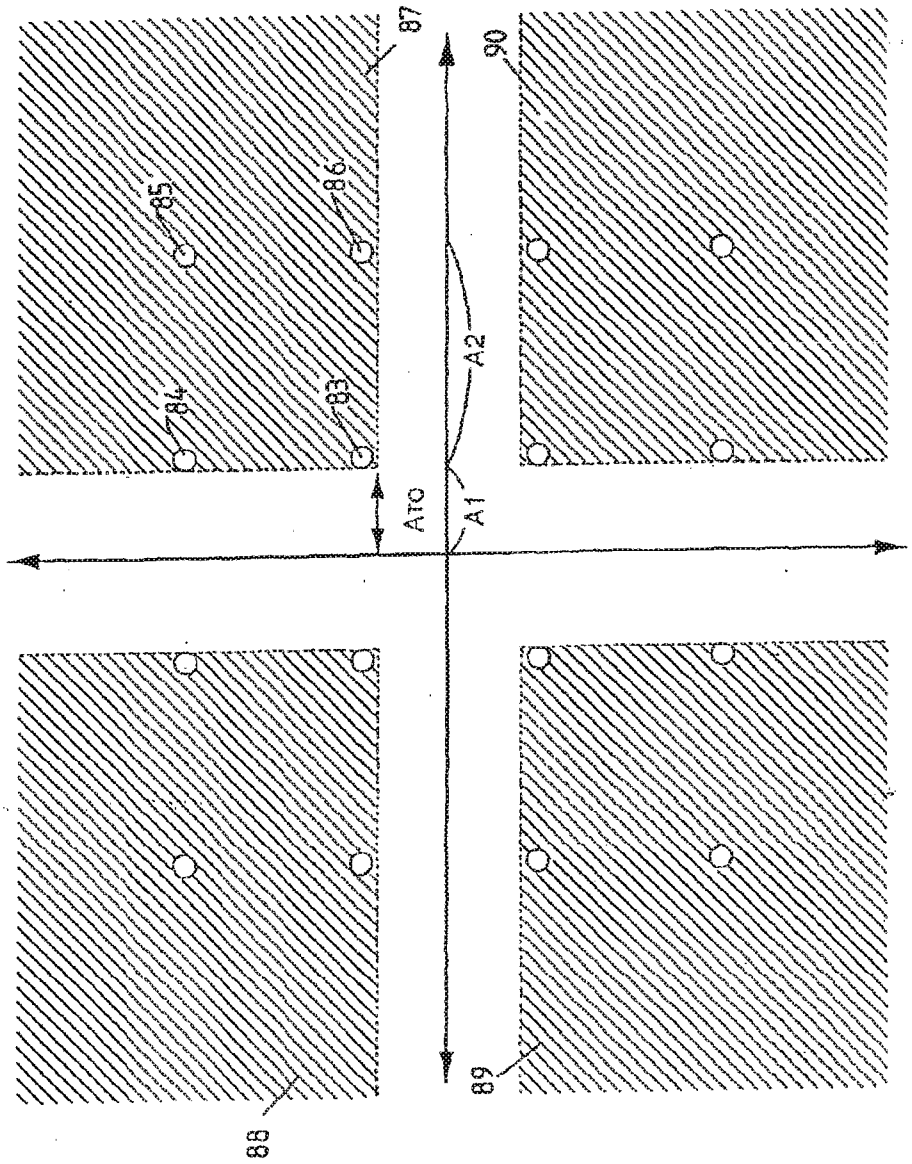


FIG. 10

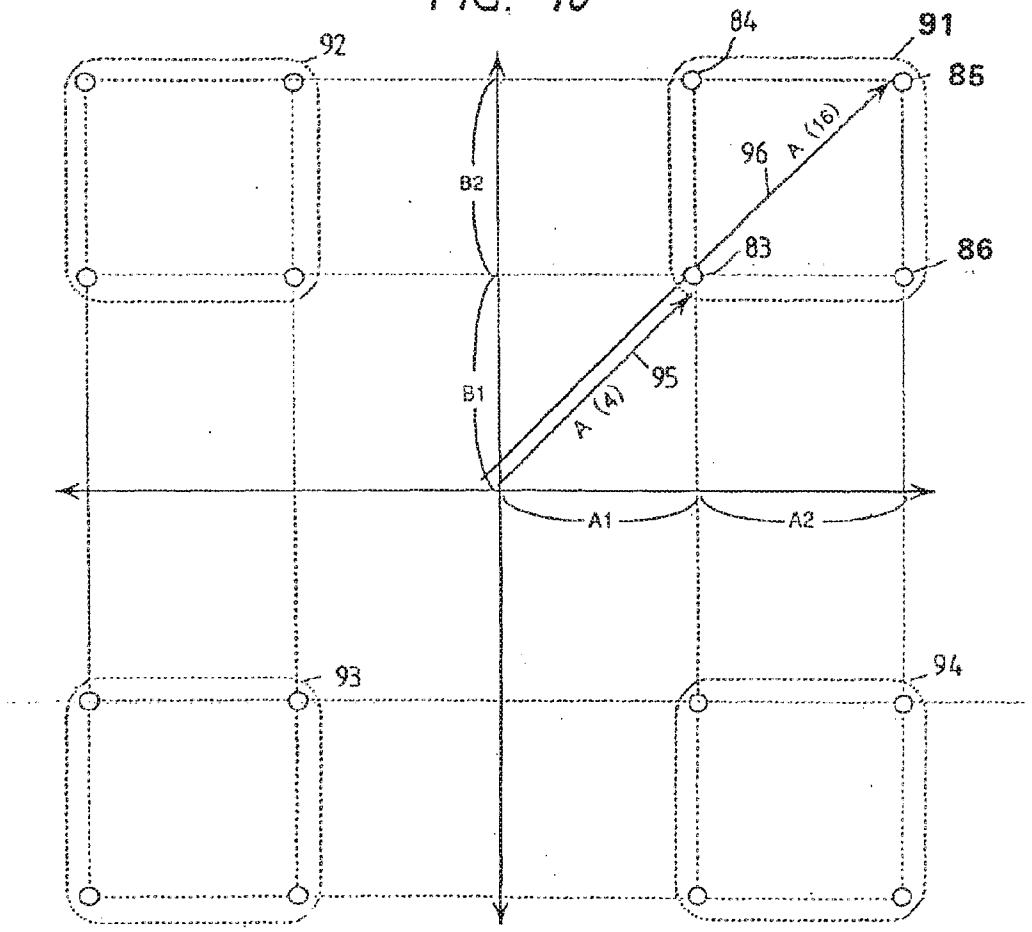


FIG. 11

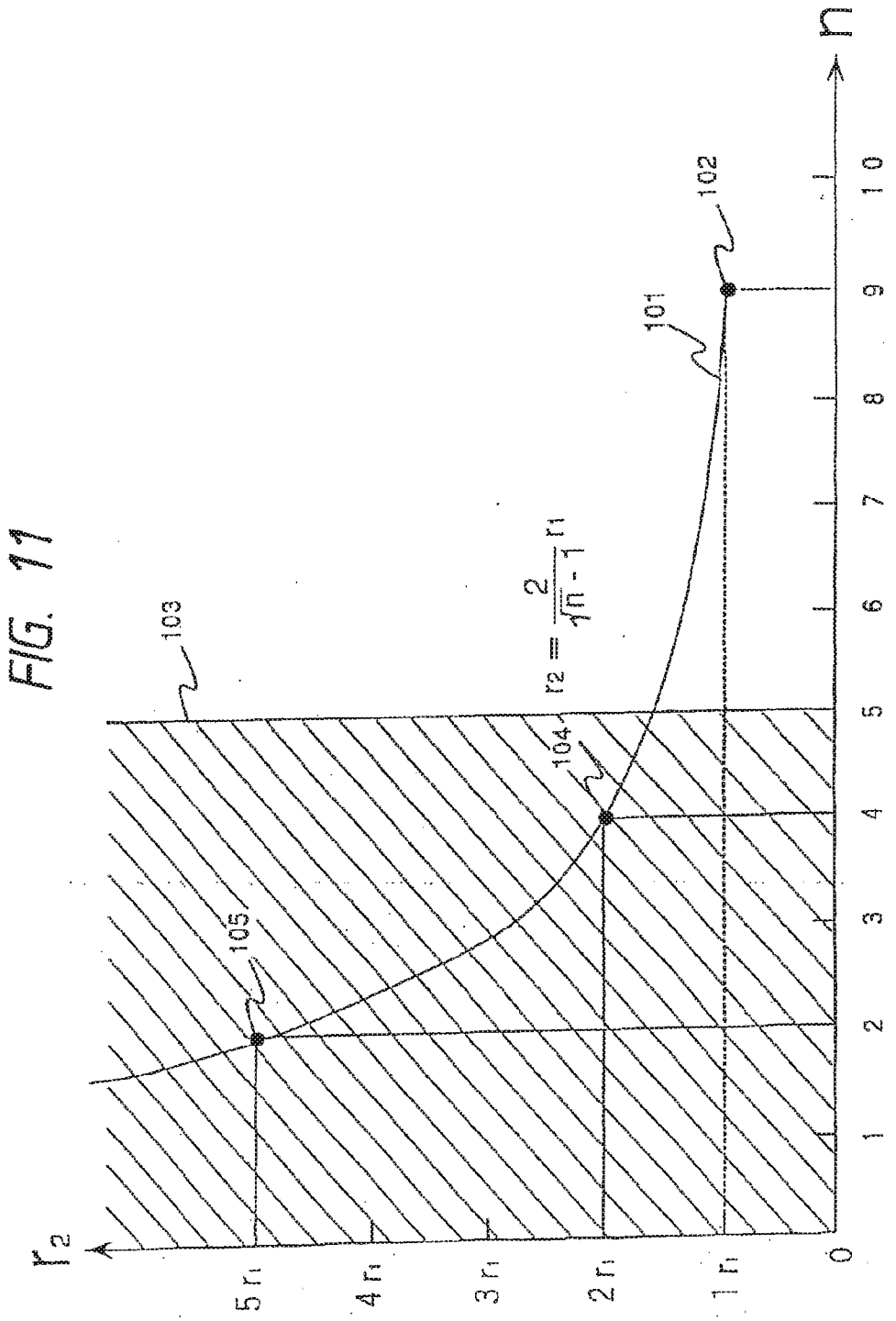


FIG. 12

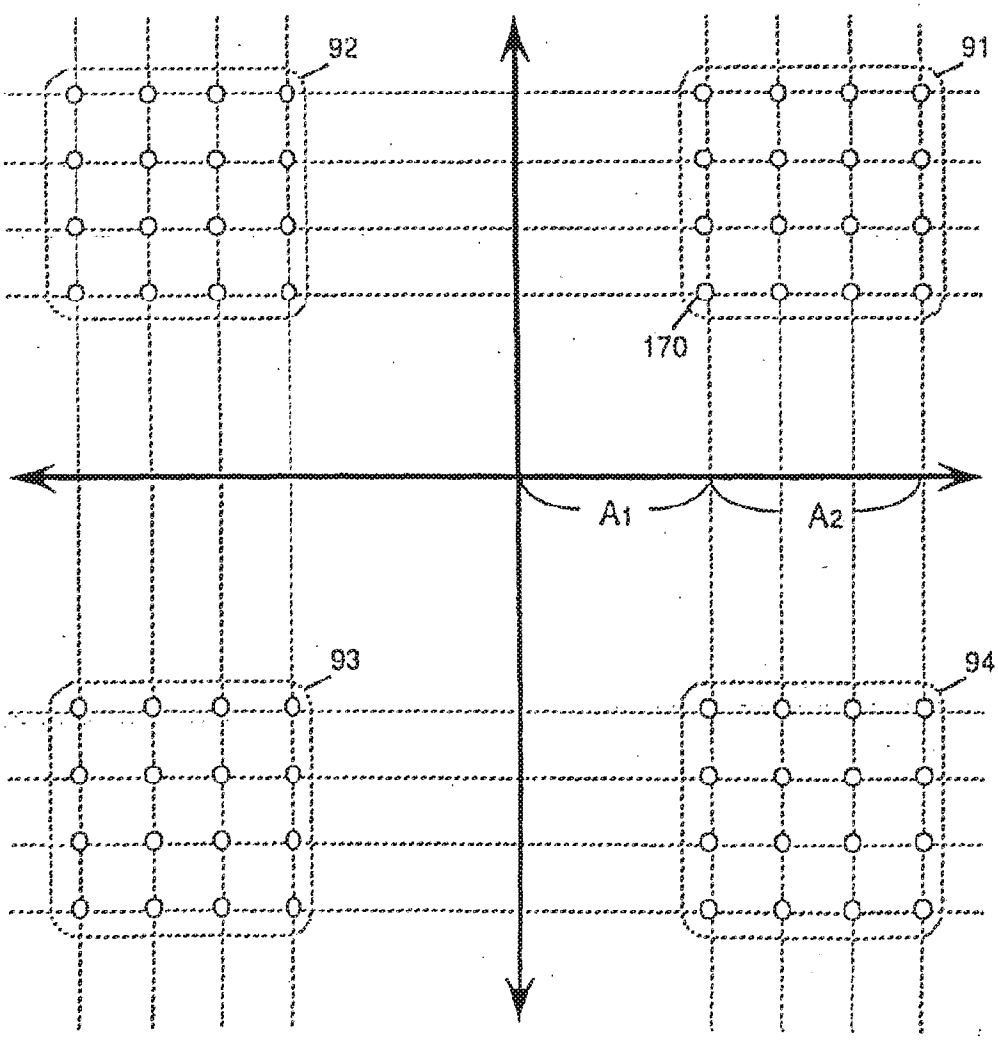
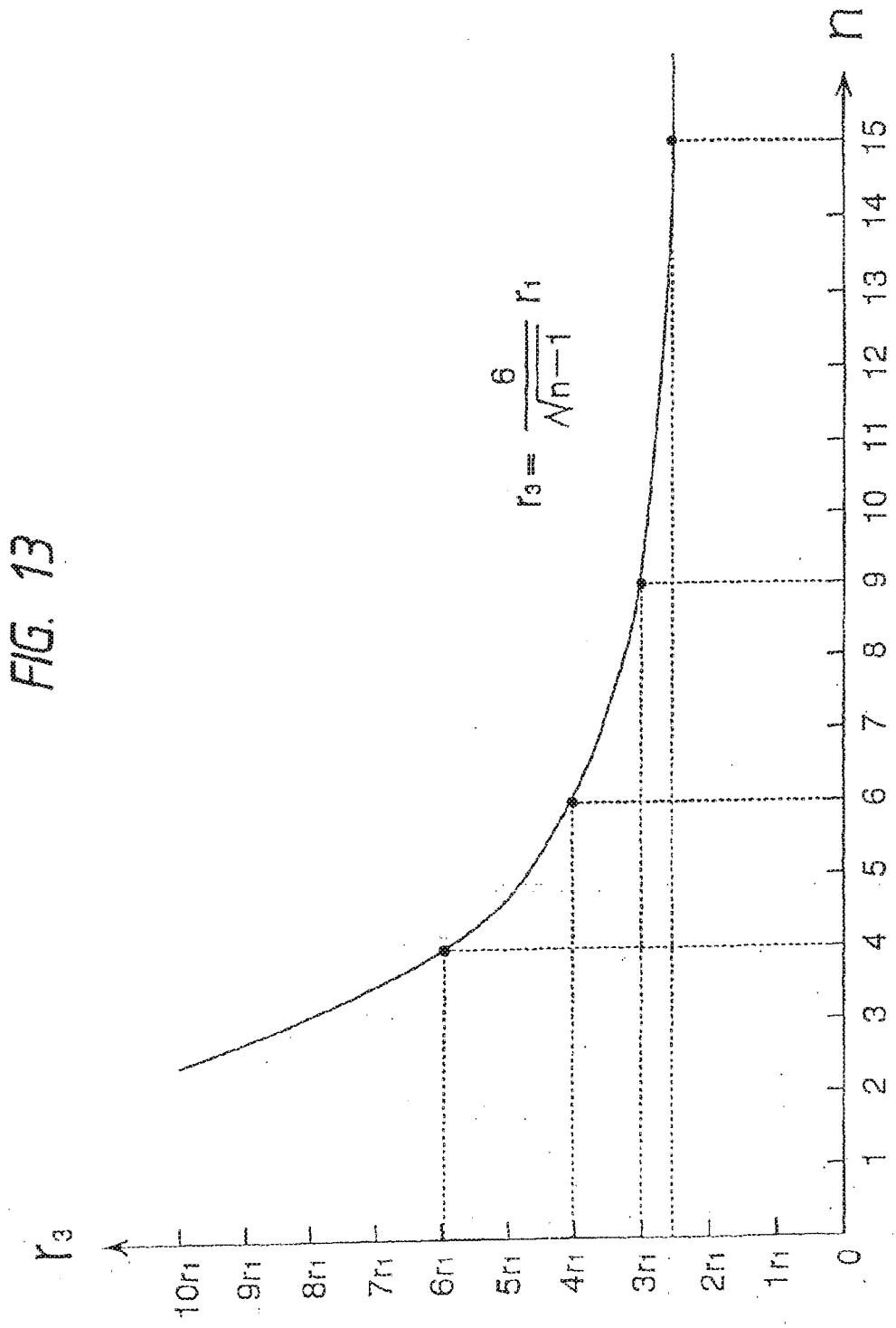


FIG. 13



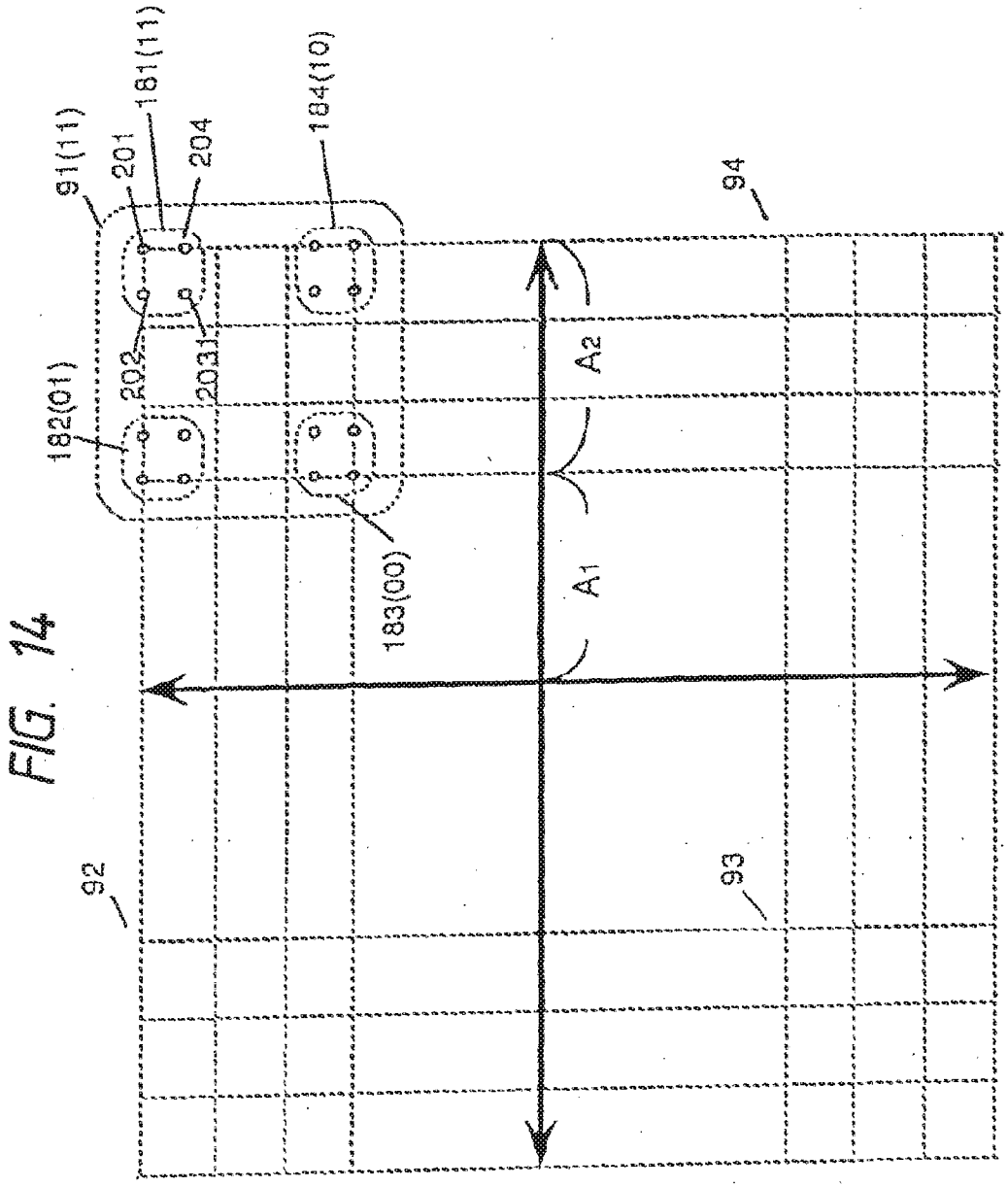


FIG. 14

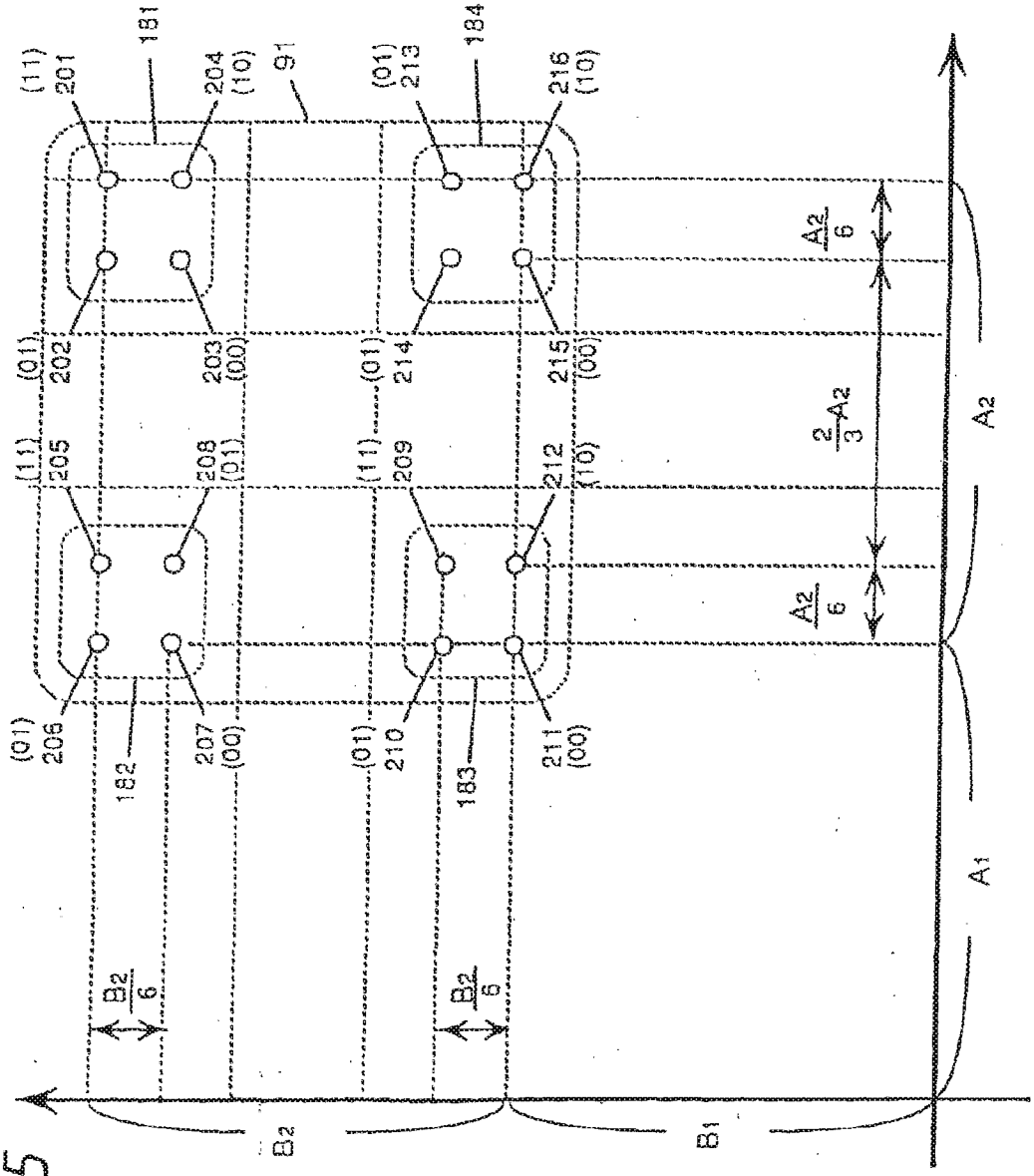


FIG. 15

FIG. 16

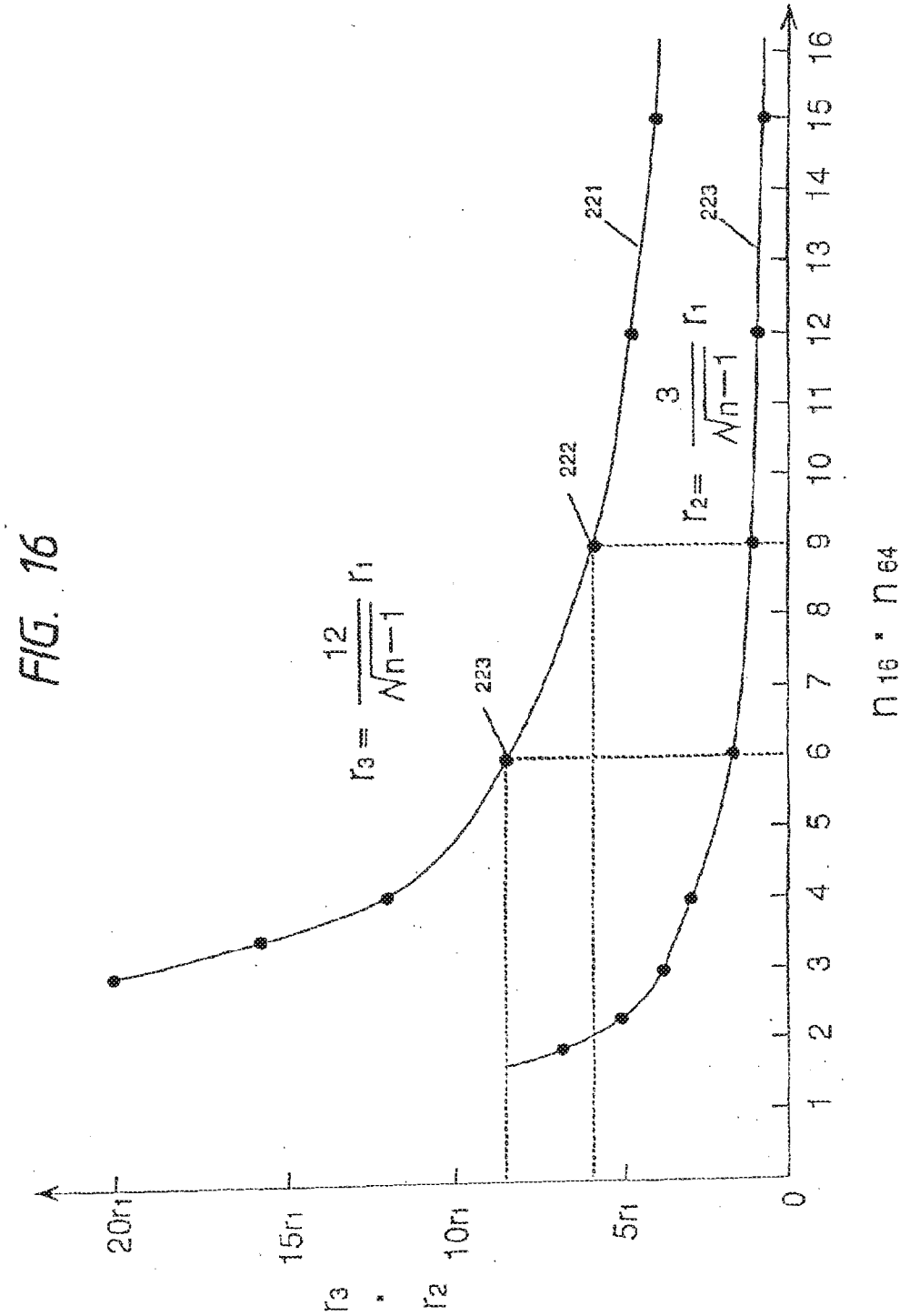


FIG. 17

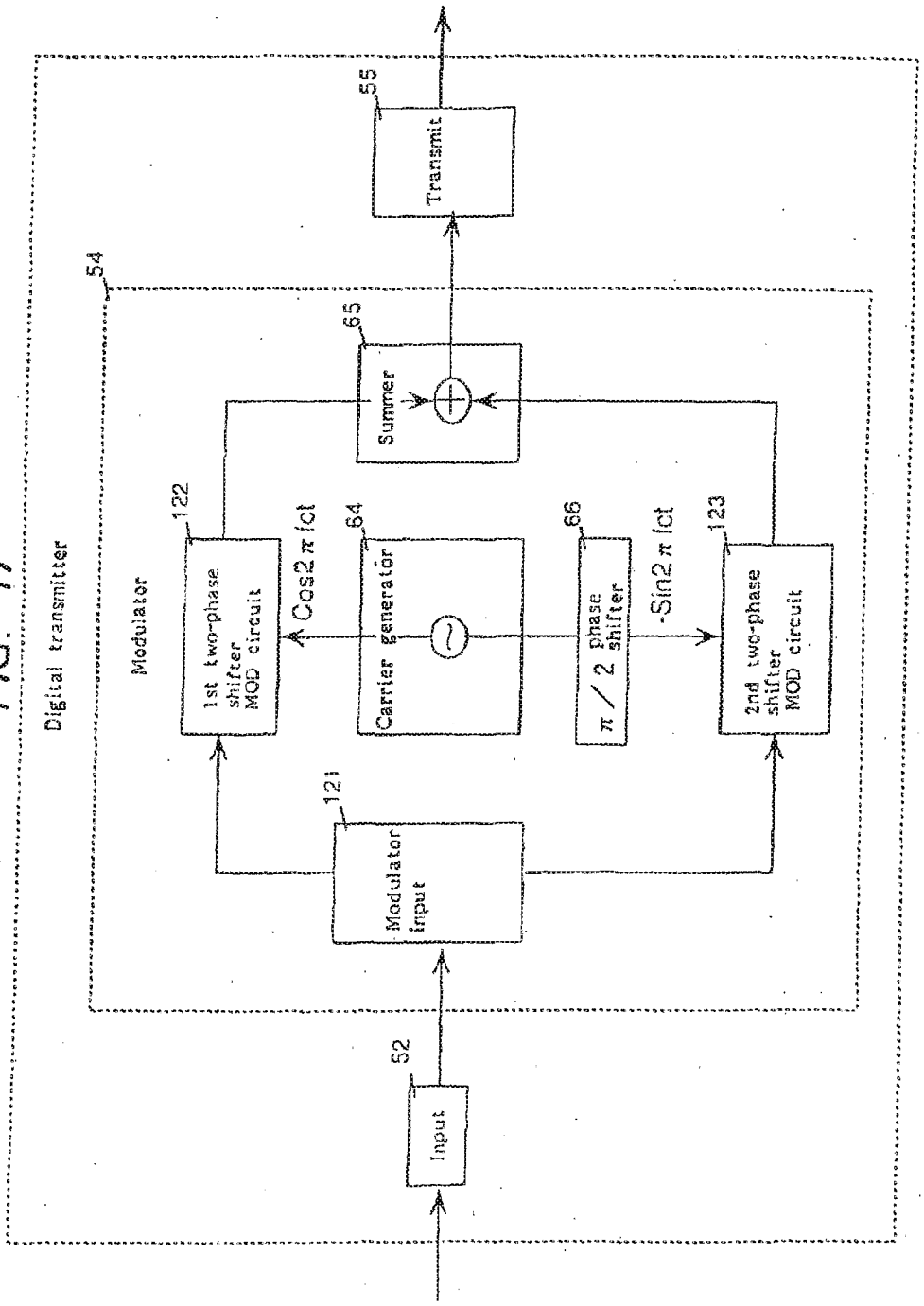


FIG. 18

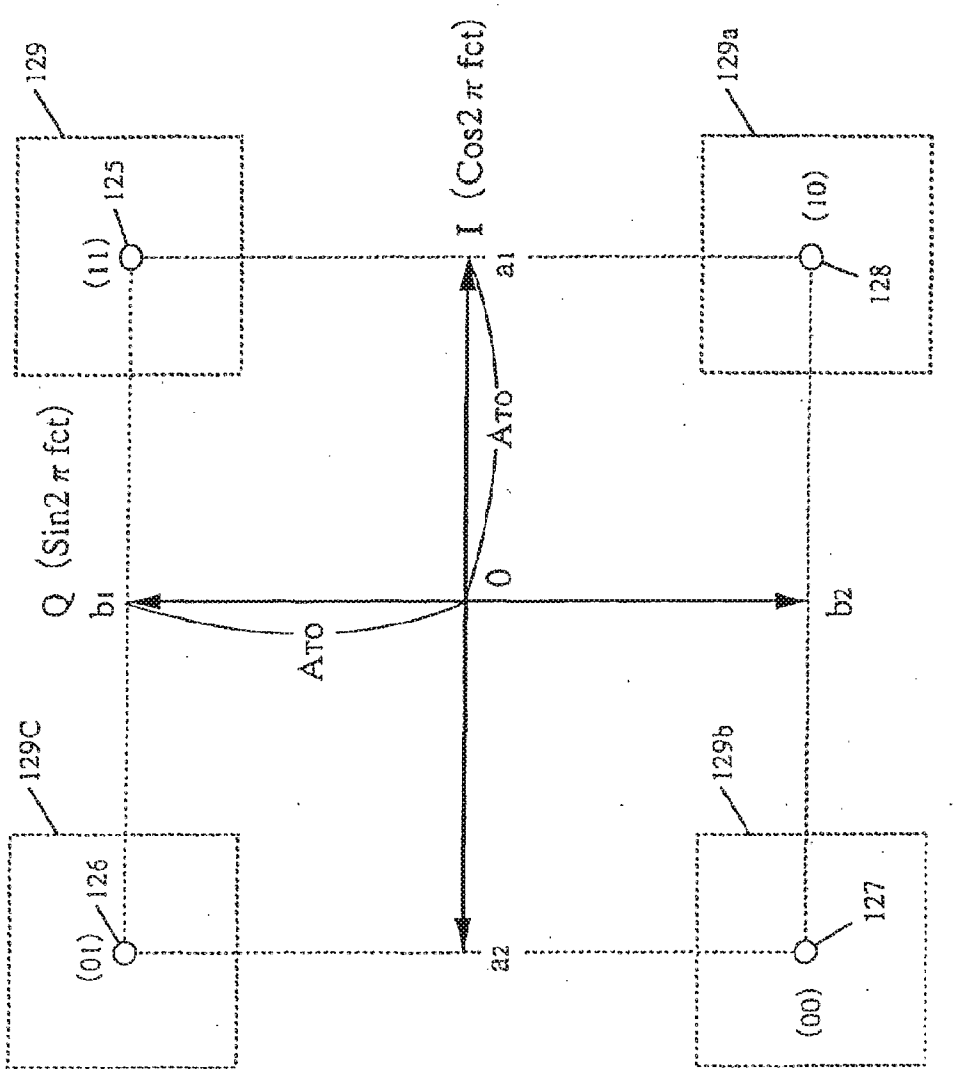


FIG. 19

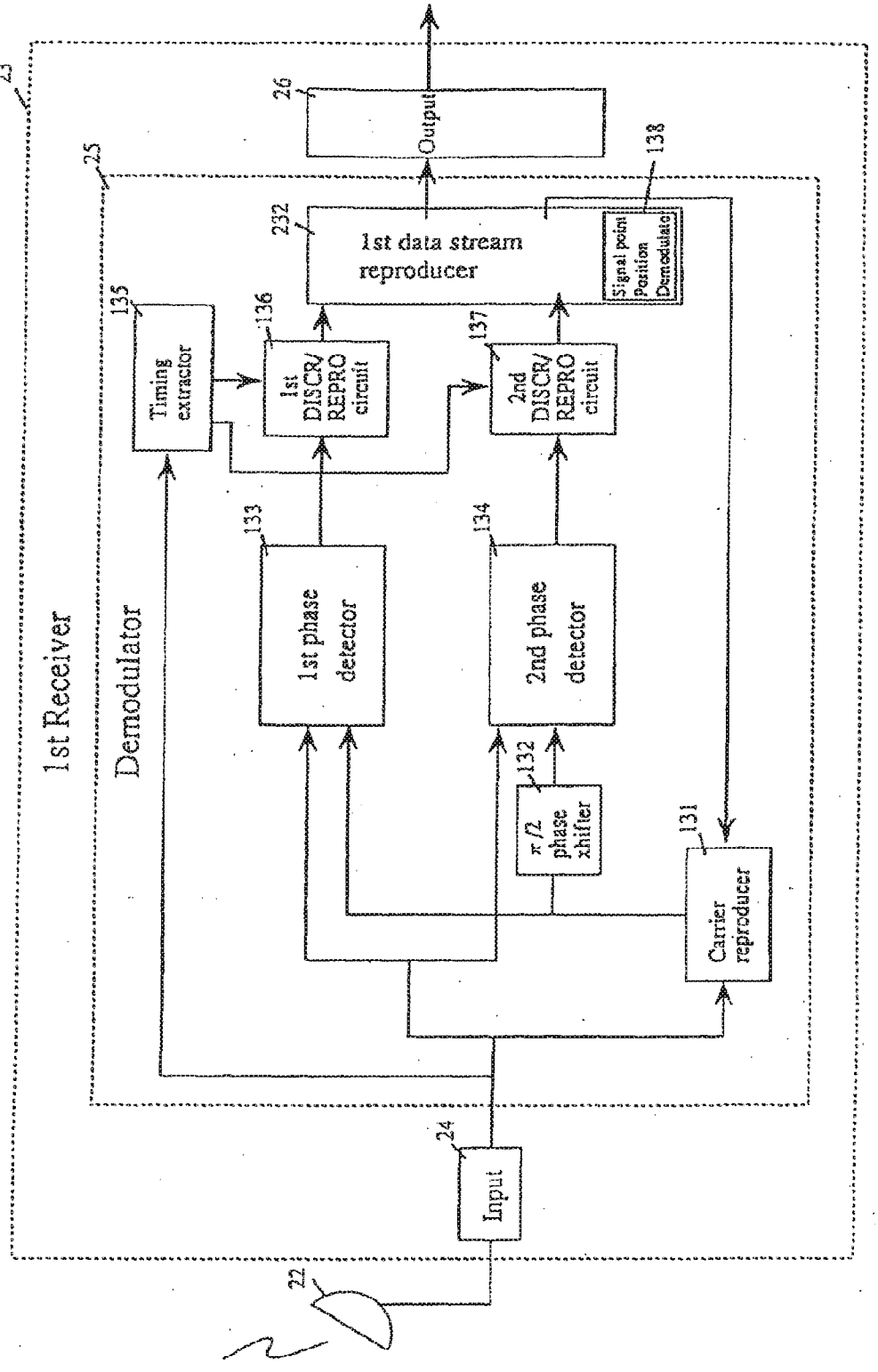


FIG. 20

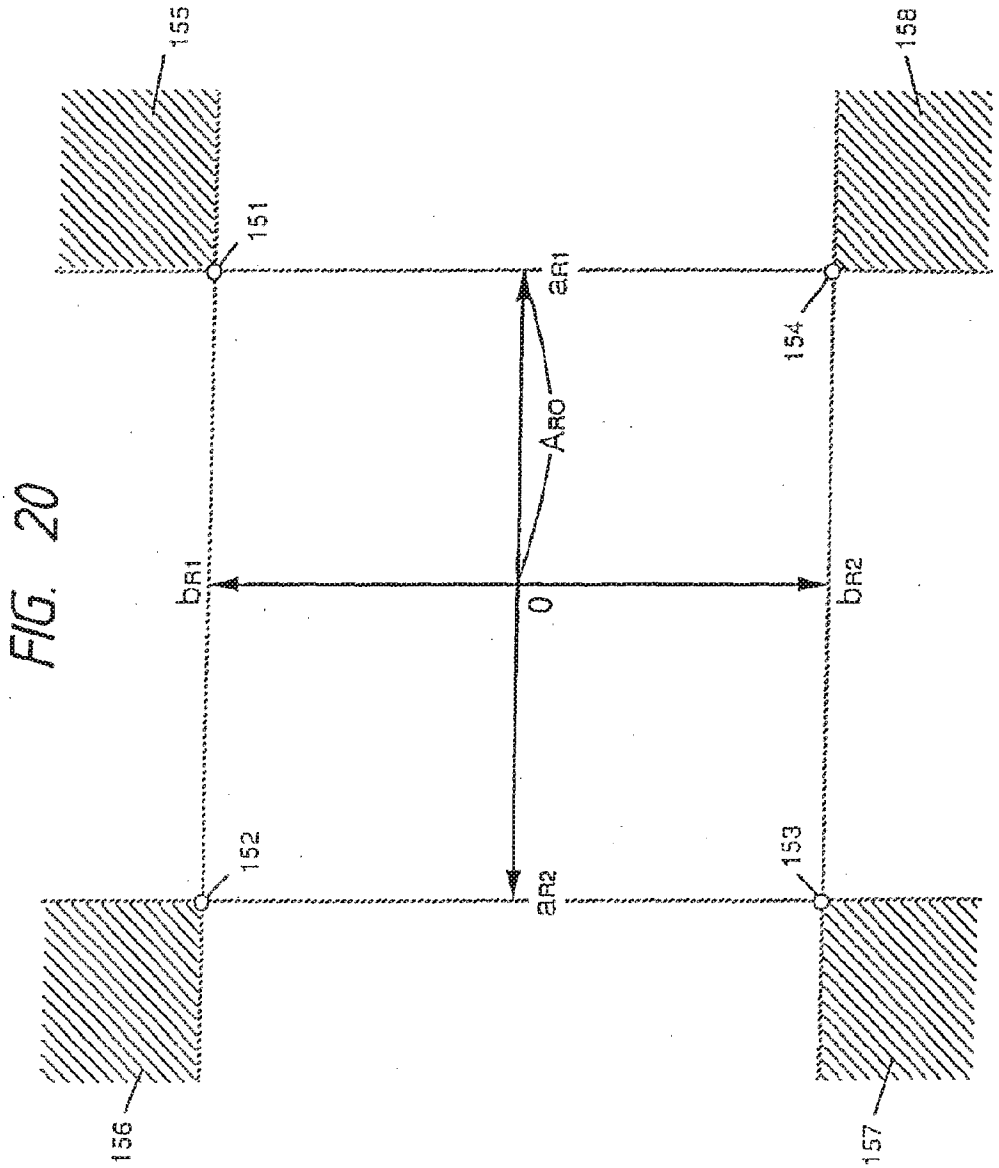


FIG. 21

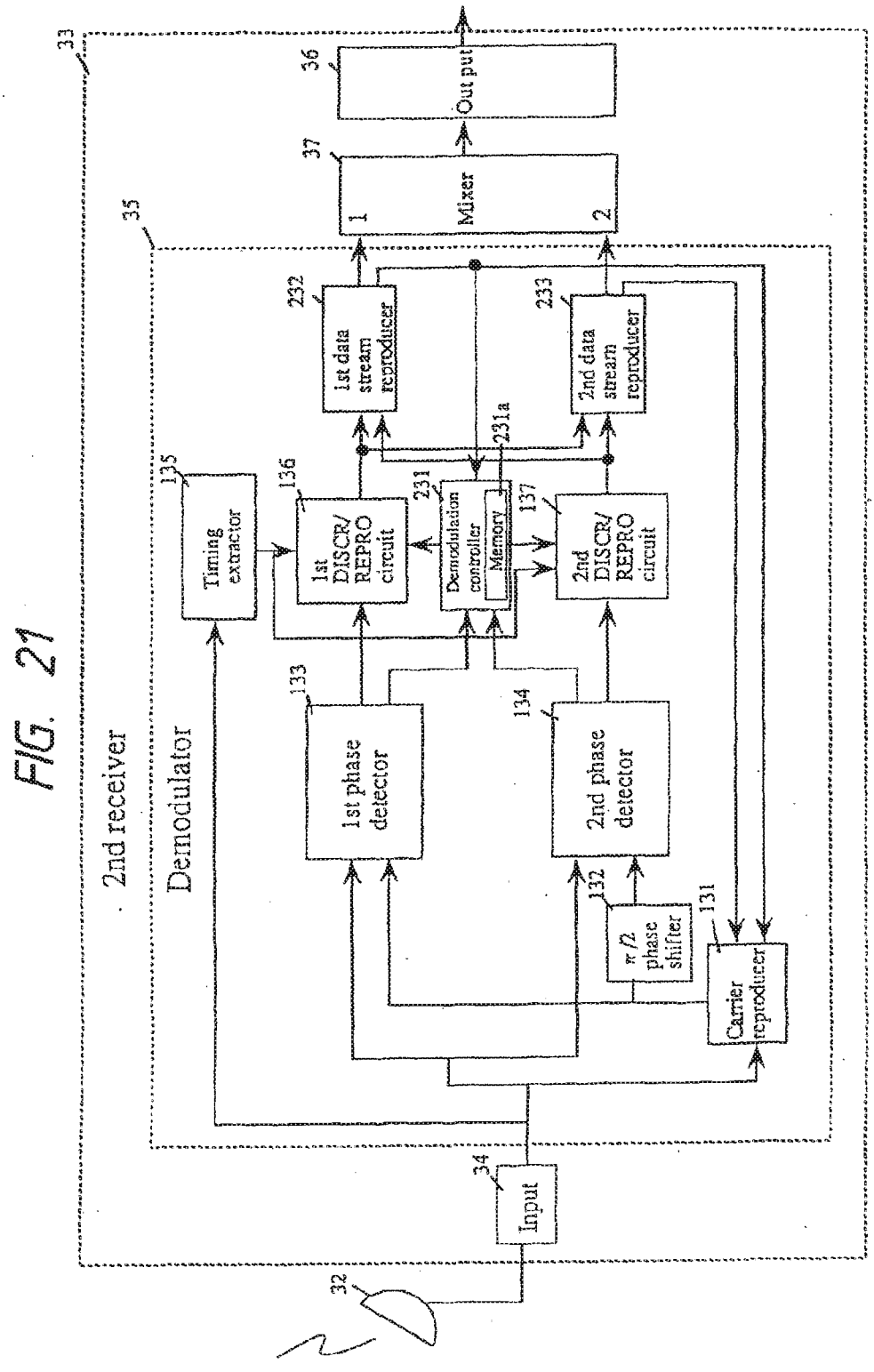
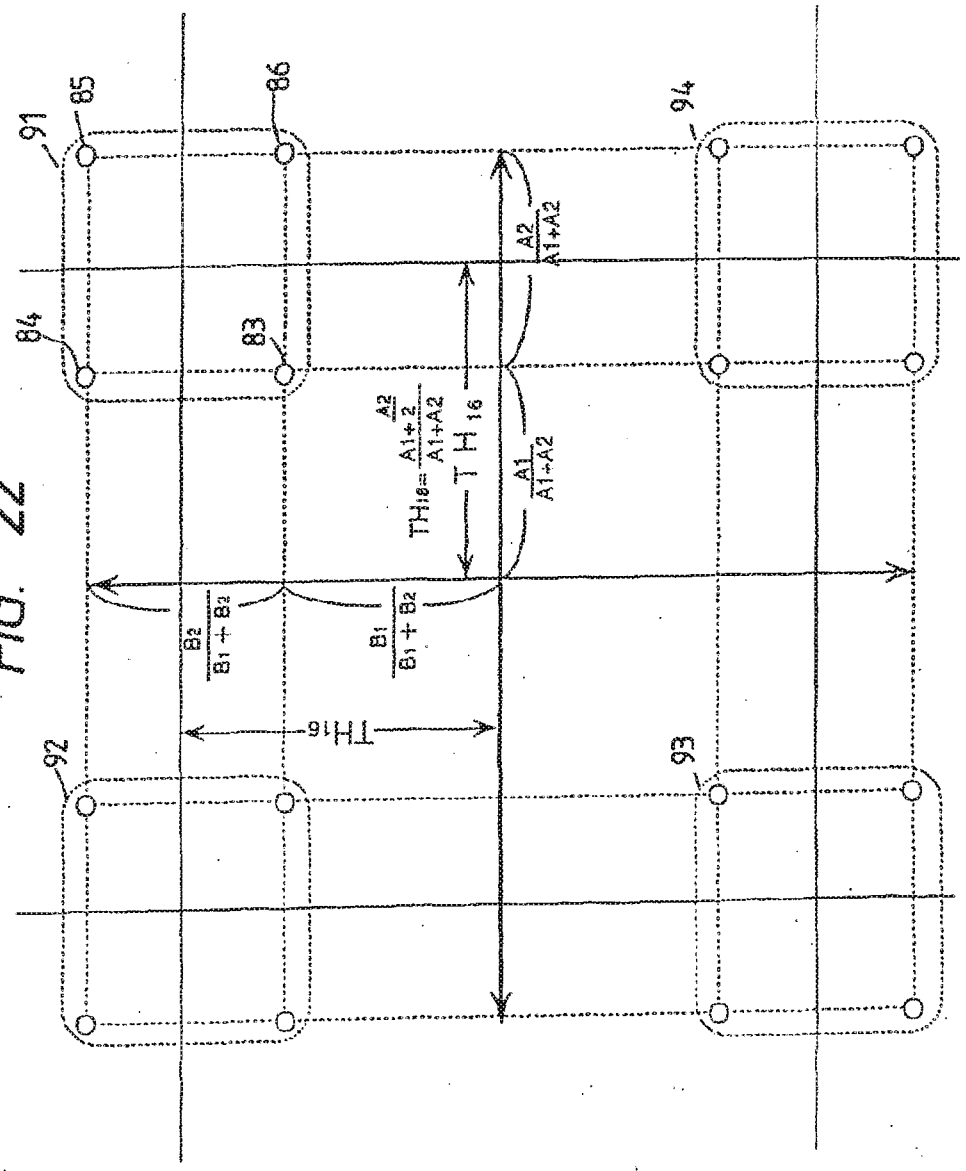


FIG. 22



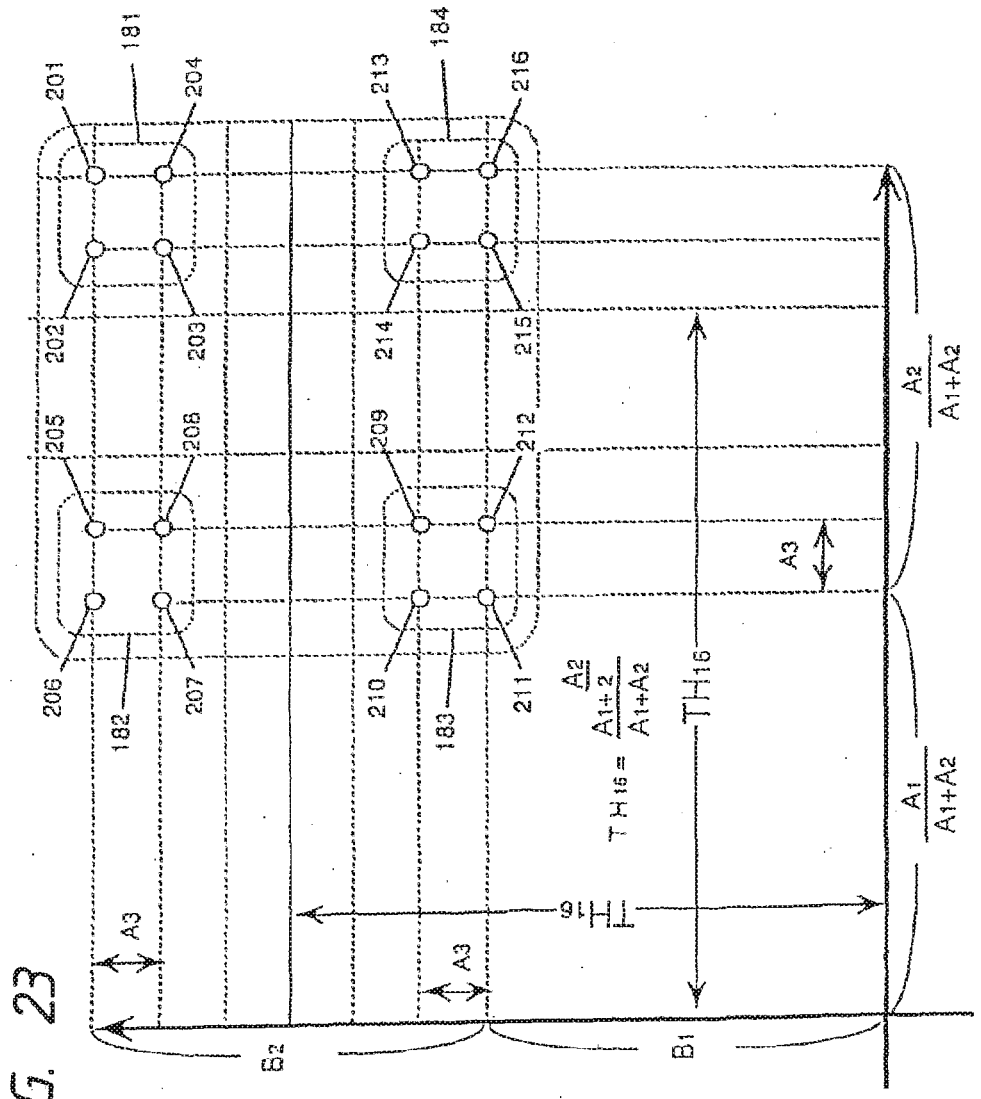


FIG. 23

FIG. 24

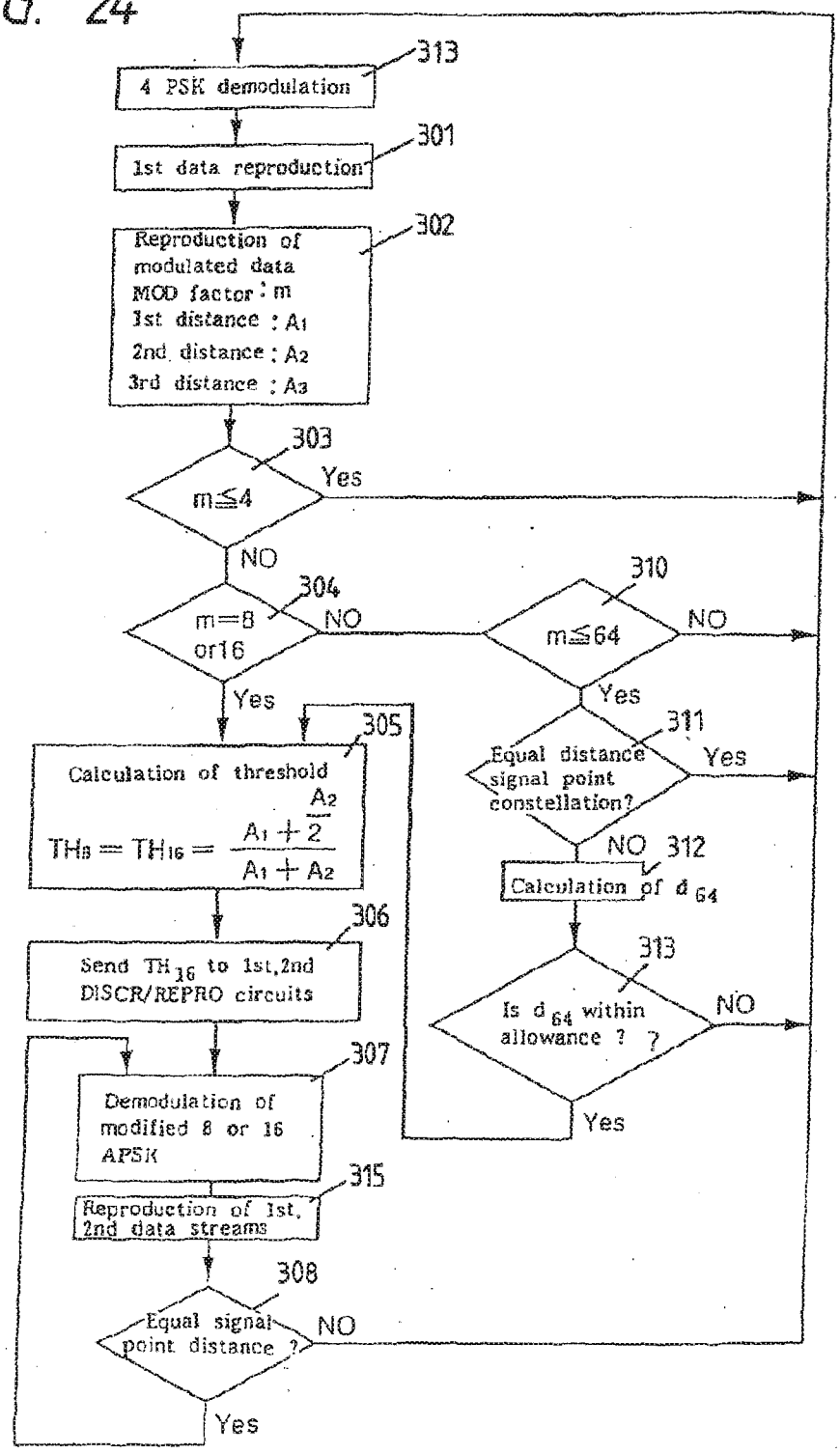
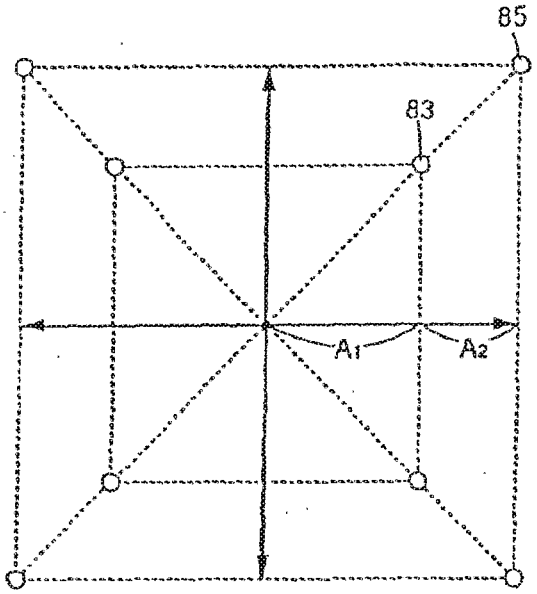


FIG. 25

(a)



(b)

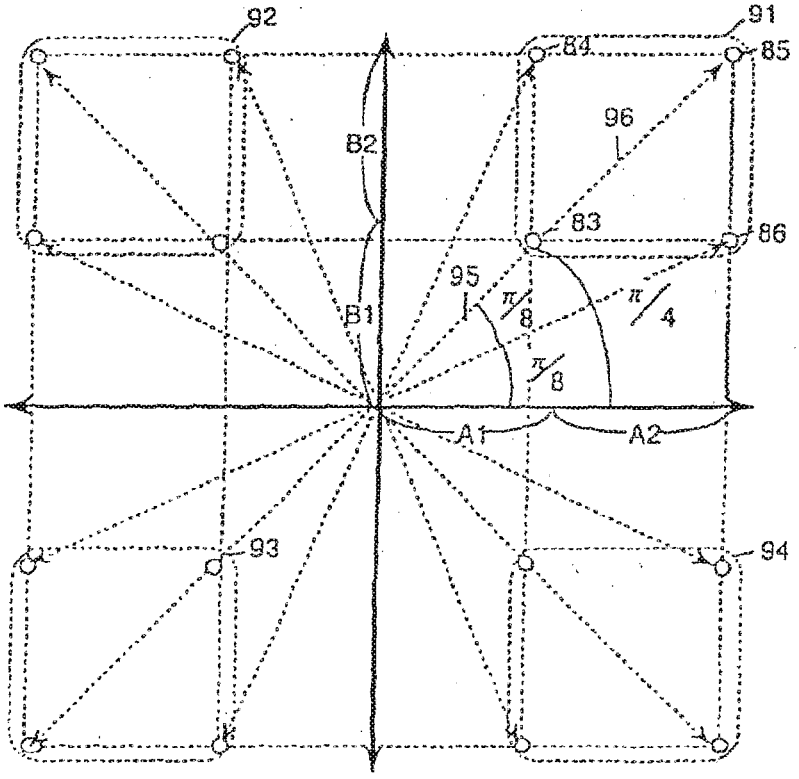
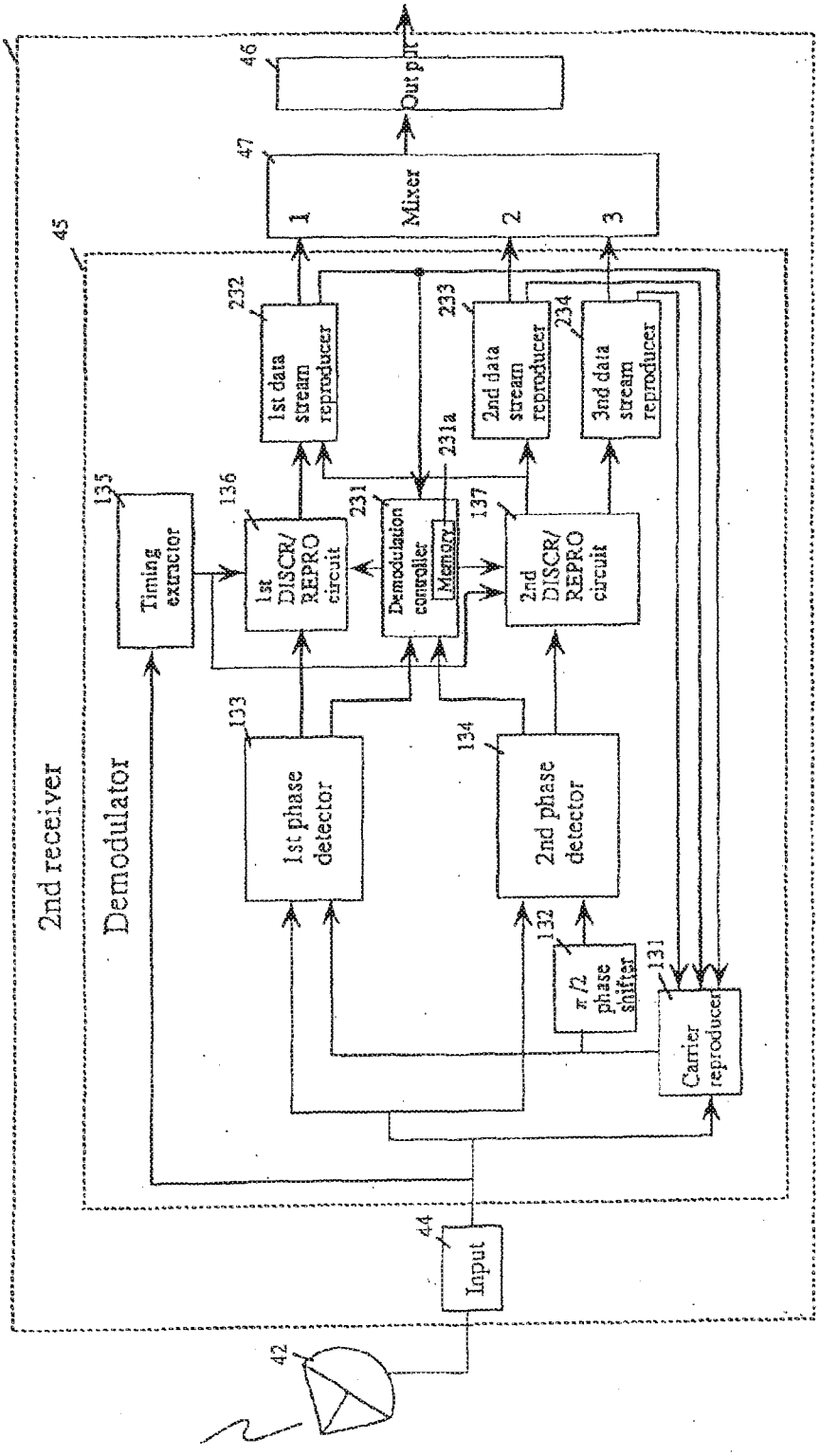


FIG. 26



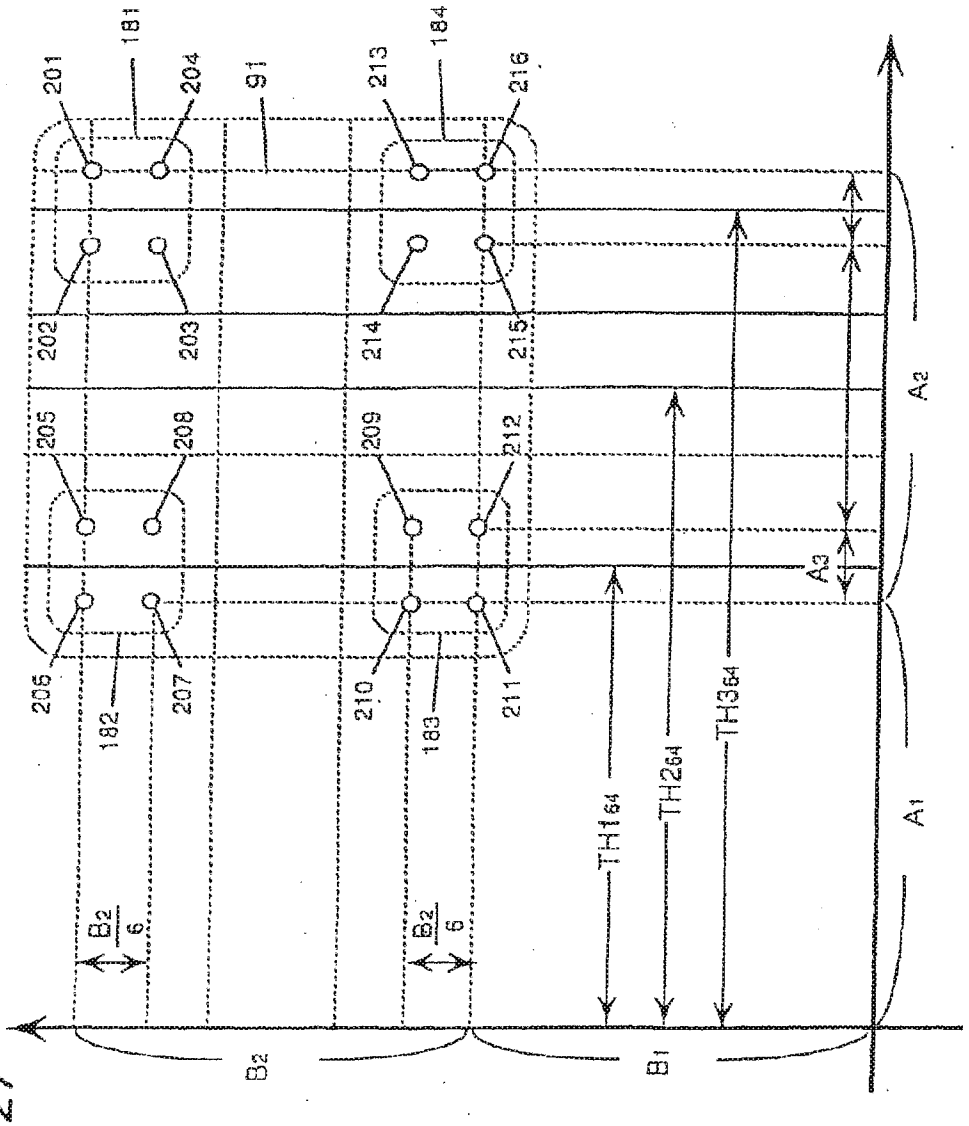


FIG. 27

FIG. 28

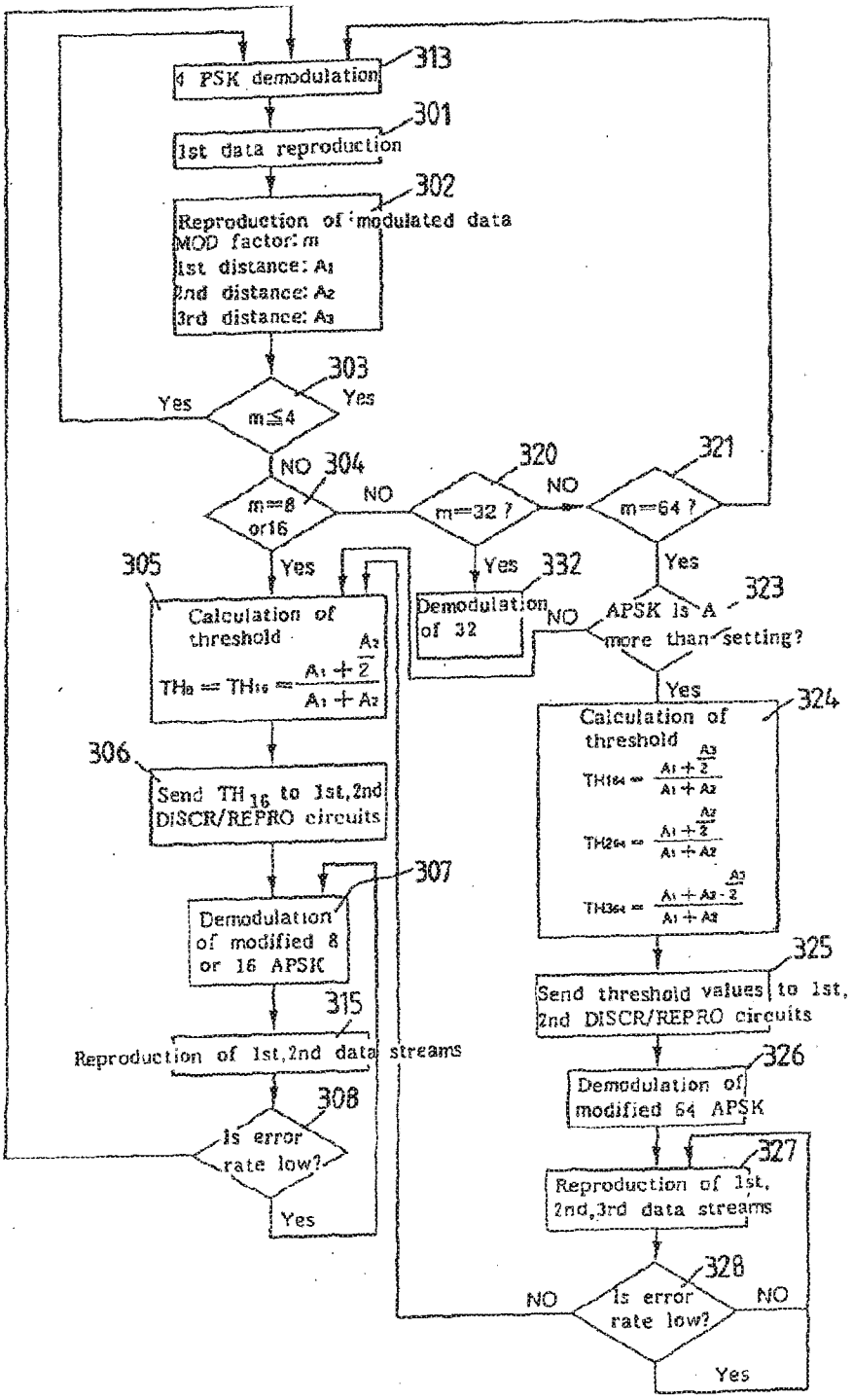


FIG. 29

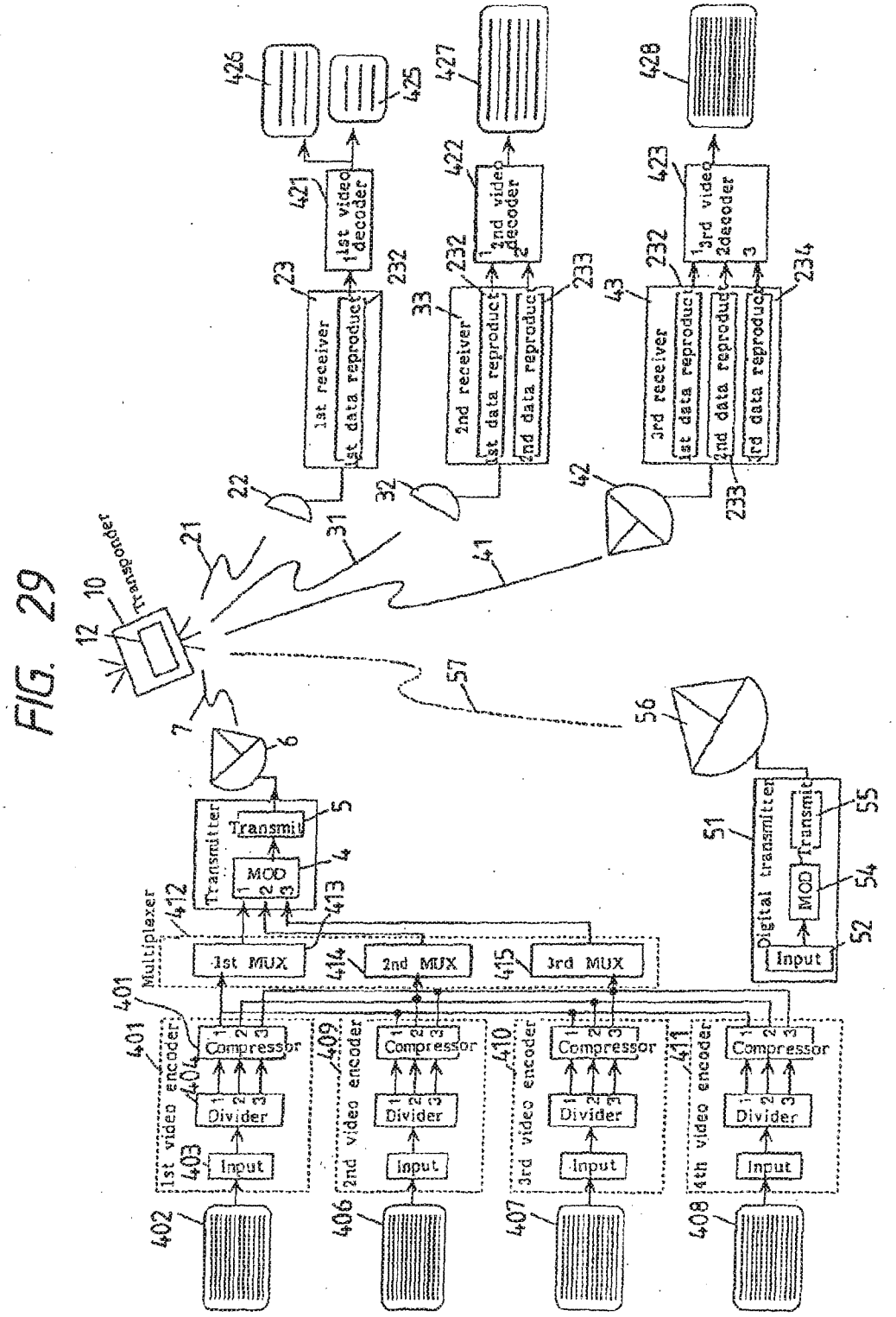


FIG. 30

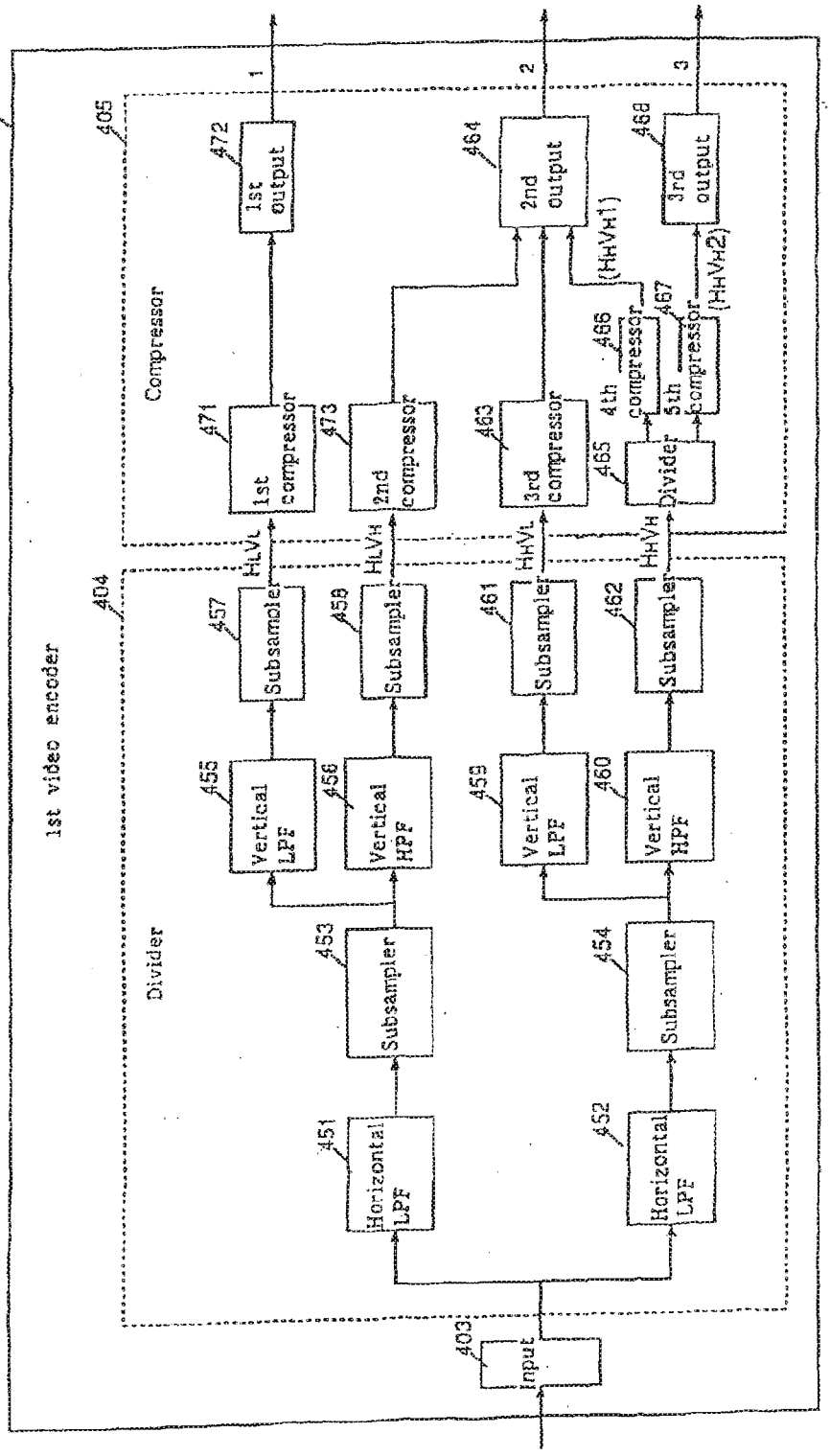


FIG. 31

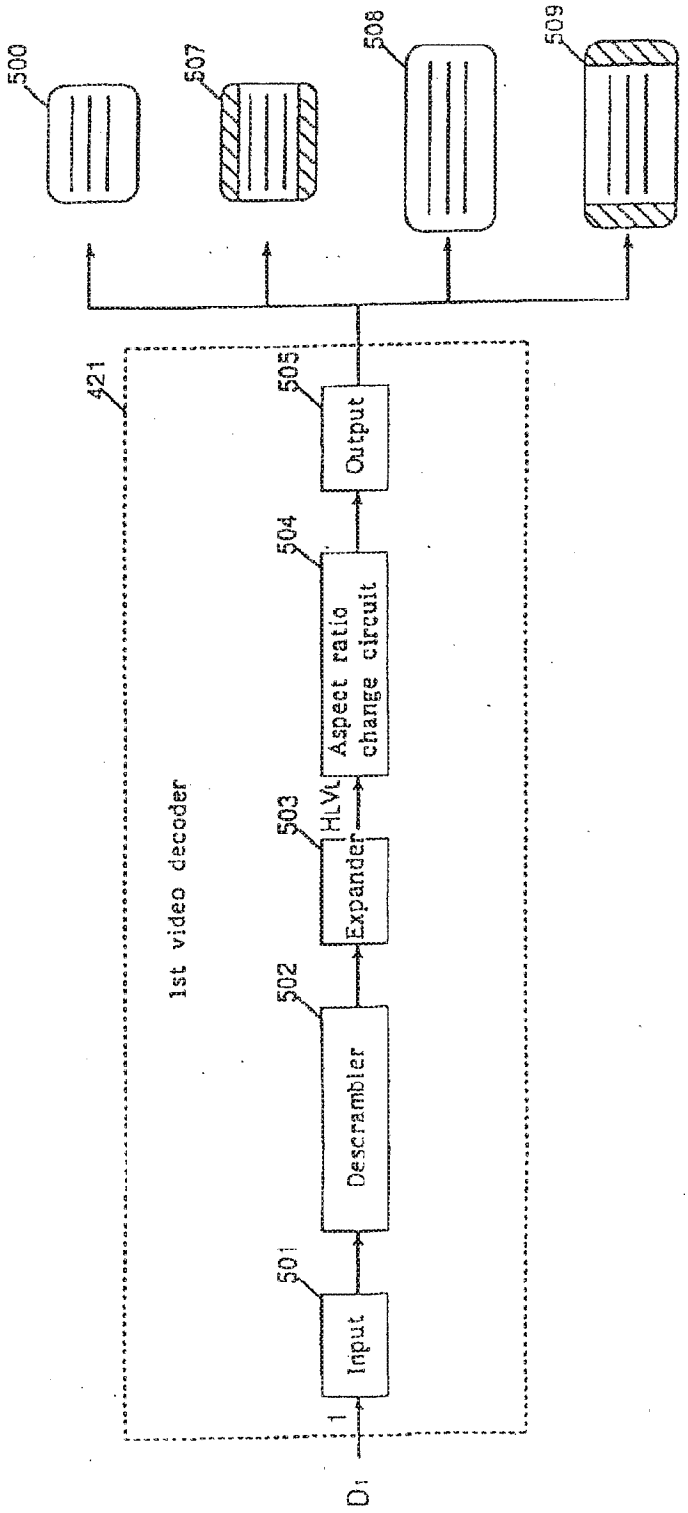


FIG. 32

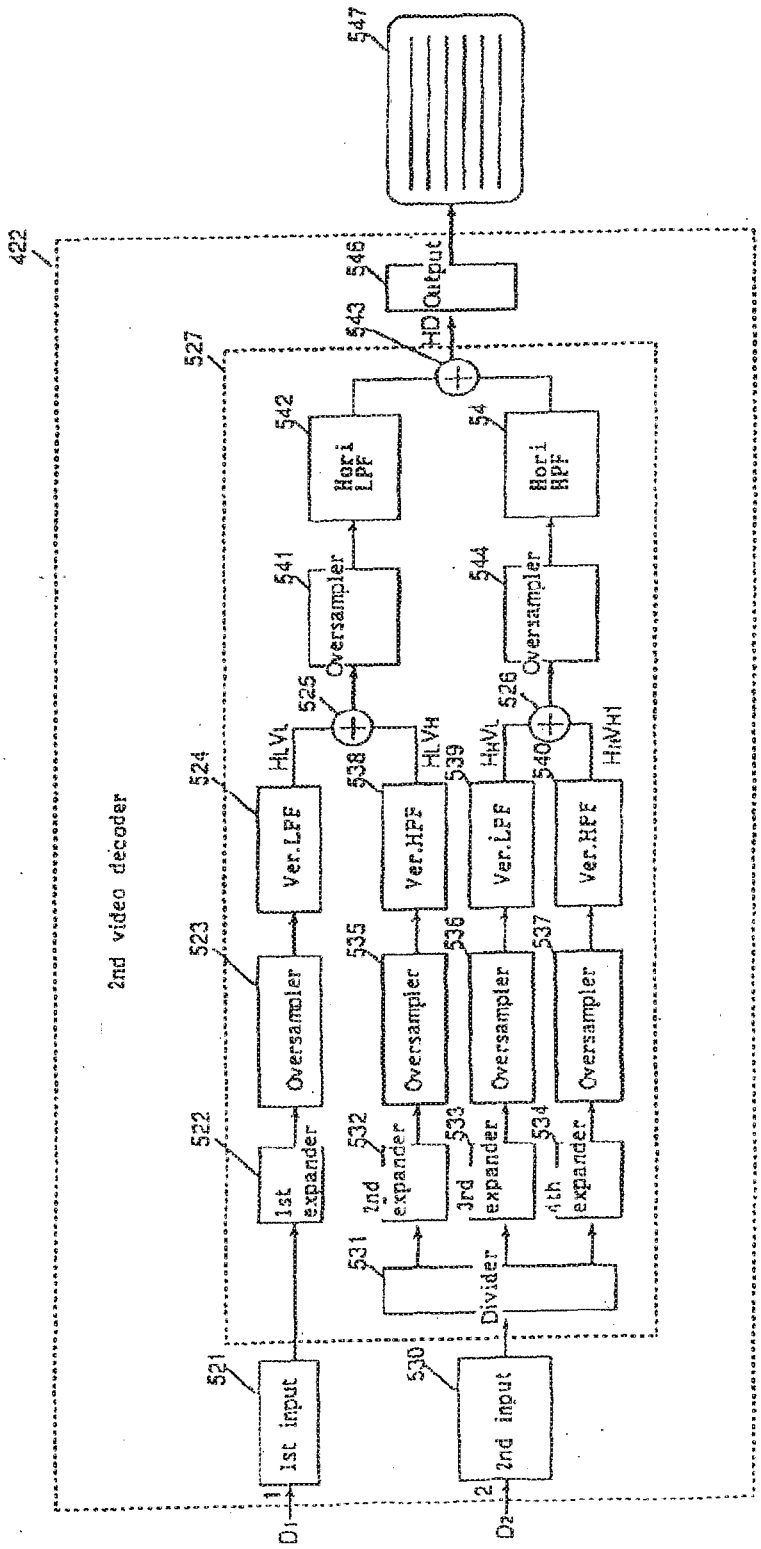


FIG. 33

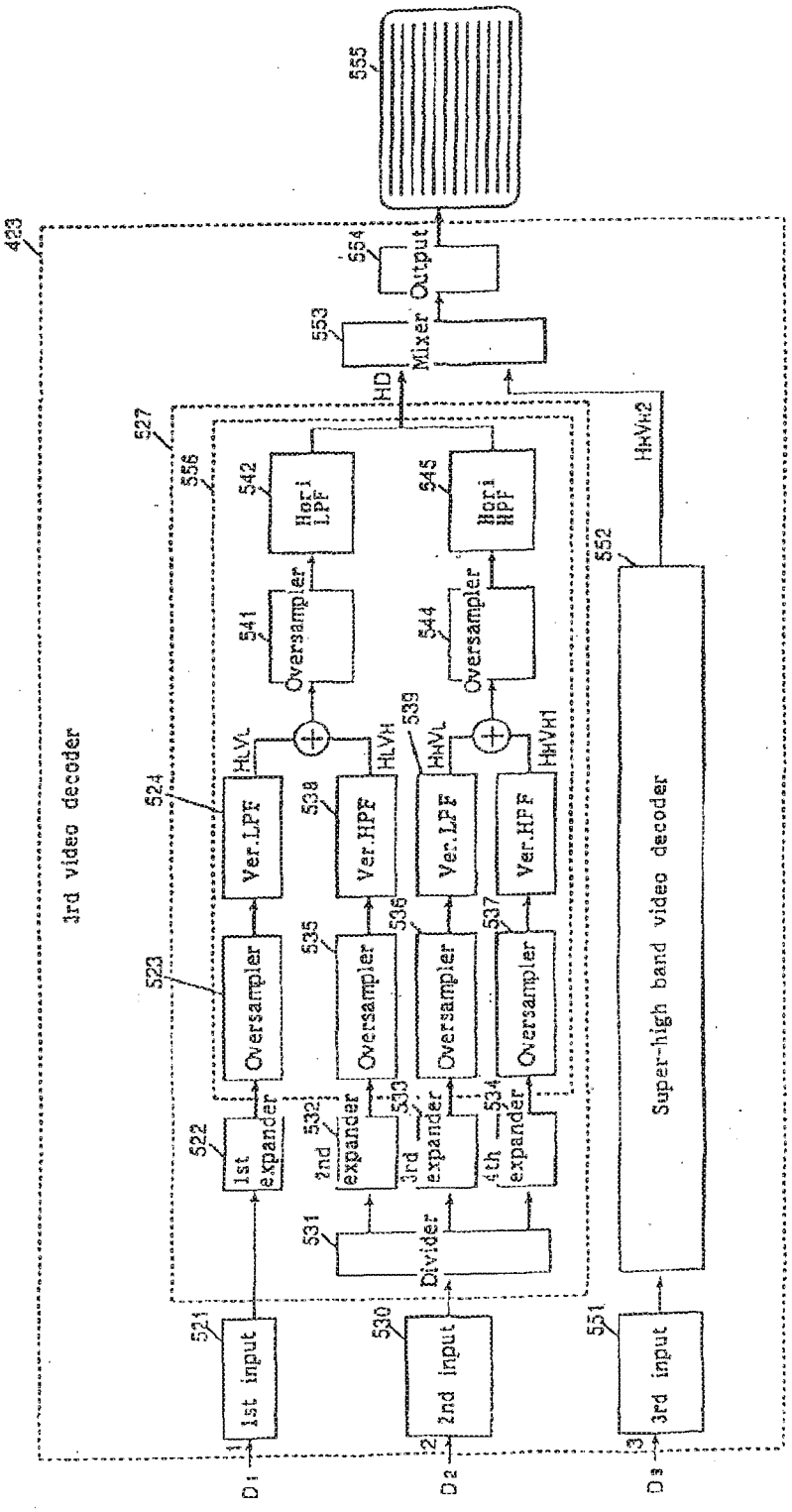

555
423
3rd video decoder
554
Output
553
Mixer
HD
527
556
542
Hori LPF
545
Hori HPF
541
Oversampler
544
Oversampler
HLVL
HLVH
HHVL
HHVH
539
524
Ver.LPF
538
Ver.HPF
Ver.LPF
Ver.HPF
523
535
536
537
Oversampler
Oversampler
Oversampler
Oversampler
522
1st expander
532
2nd expander
533
3rd expander
534
4th expander
531
Divider
521
1st input
530
2nd input
551
3rd input
552
HHVH2
Super-high band video decoder
D1
D2
D3

FIG. 34

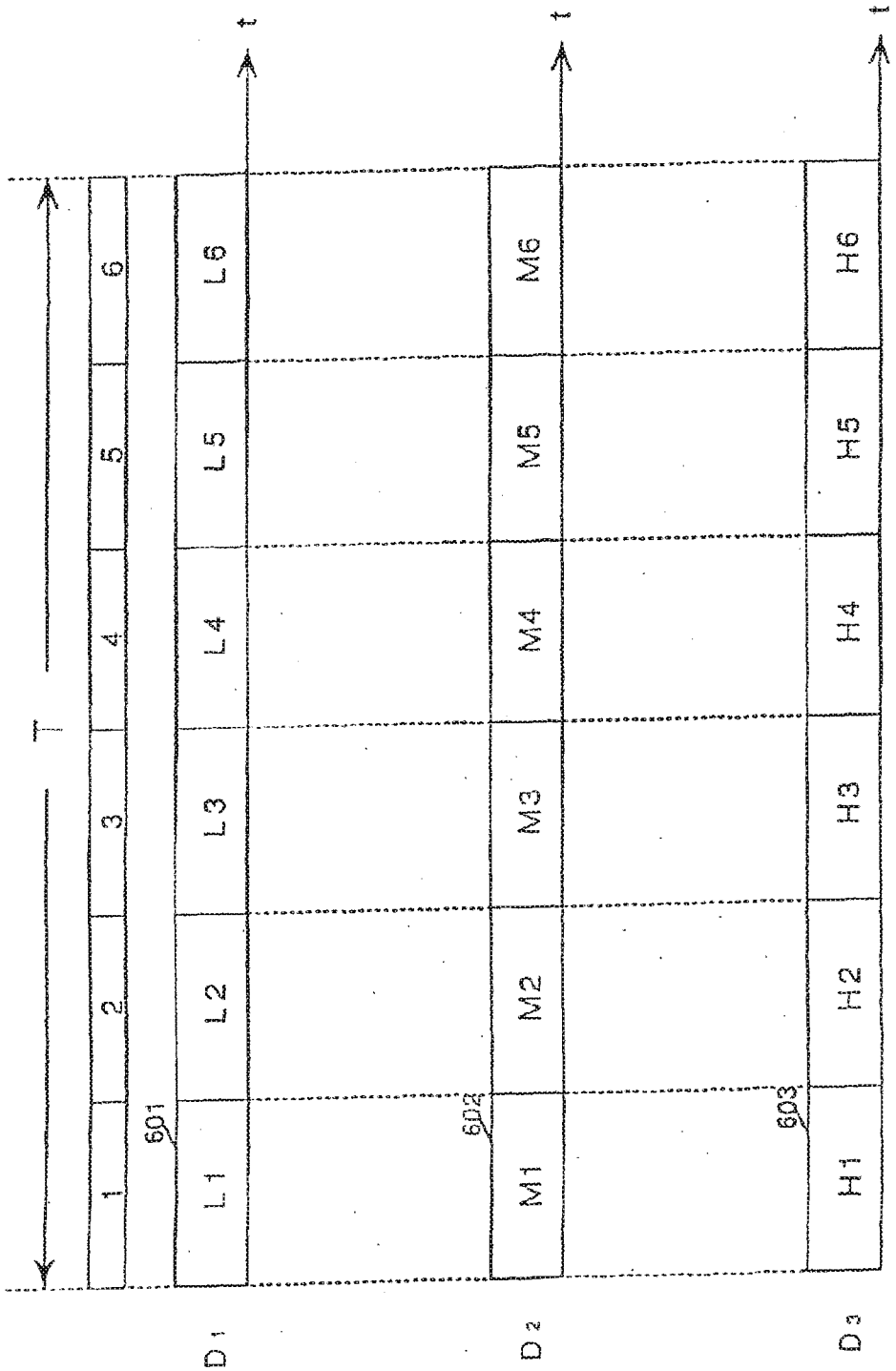


FIG. 35

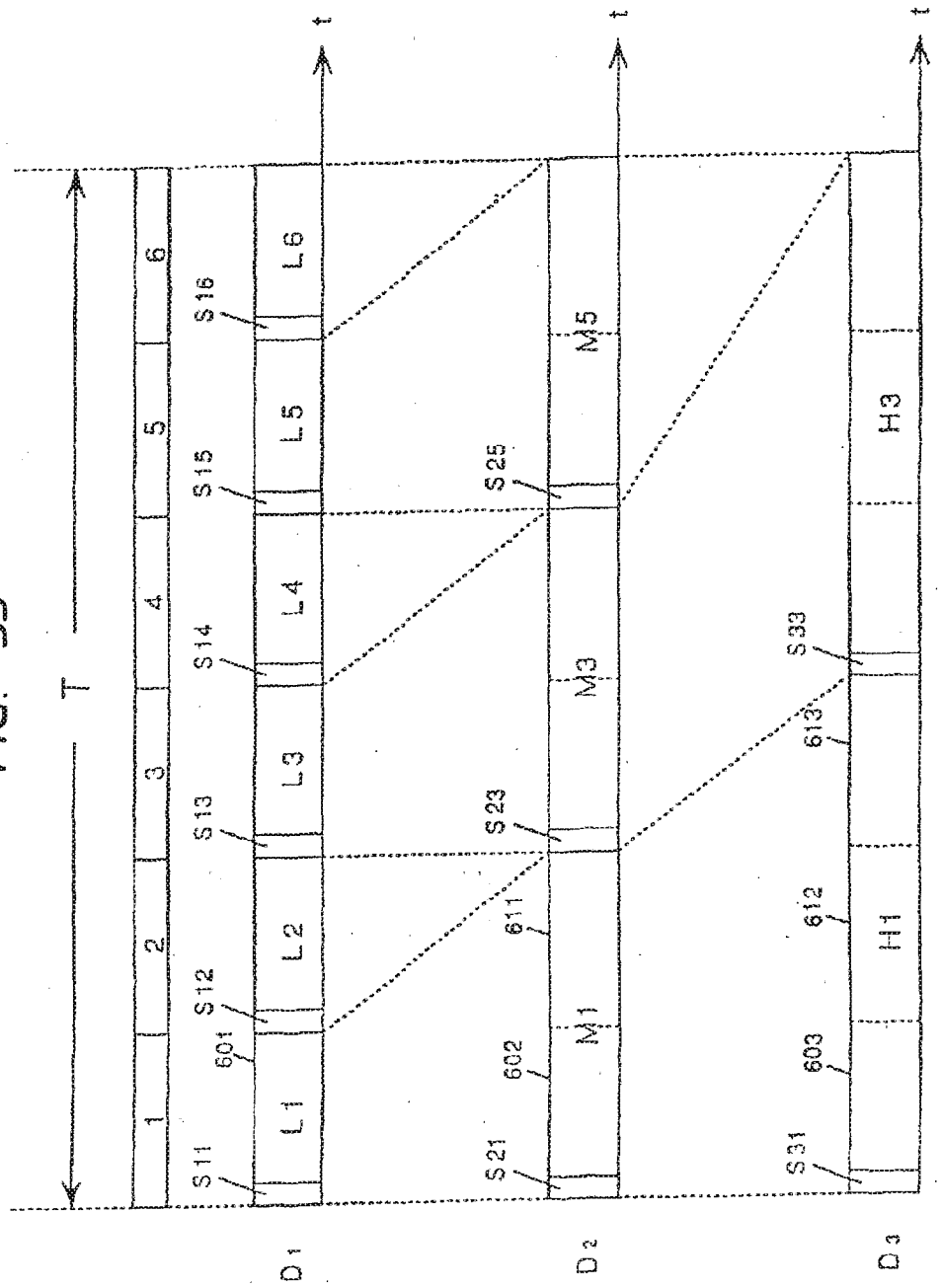


FIG. 36

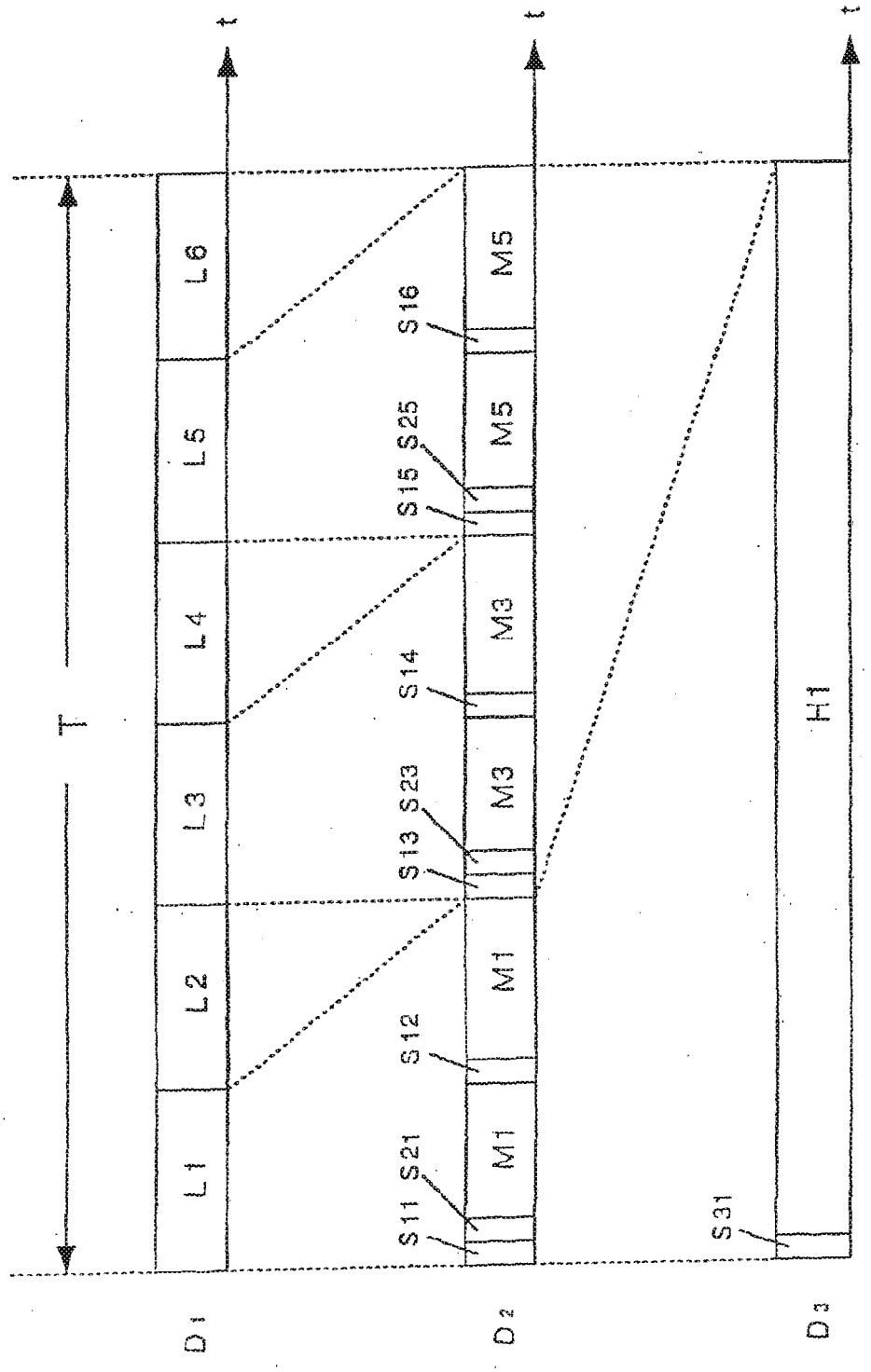
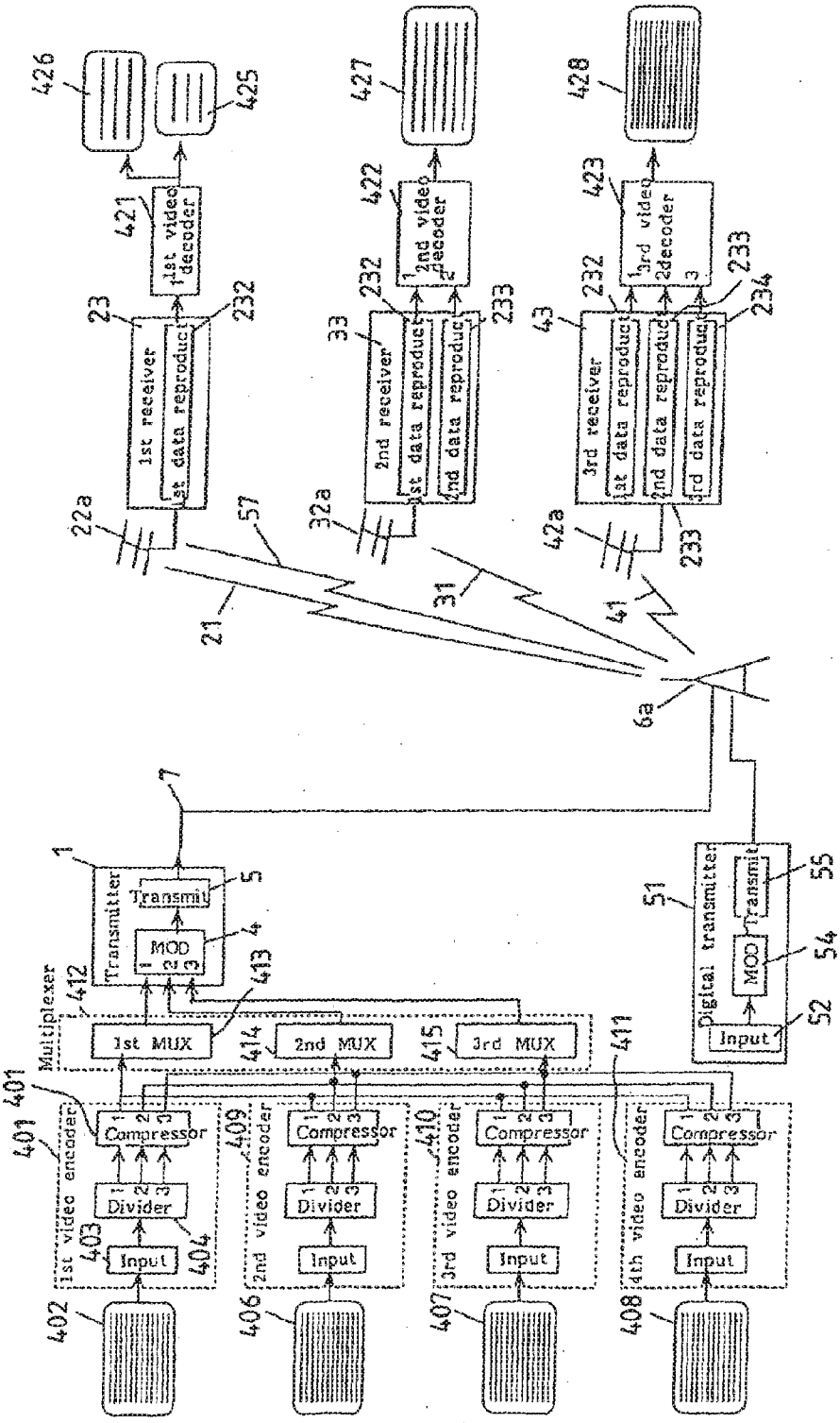


FIG. 37



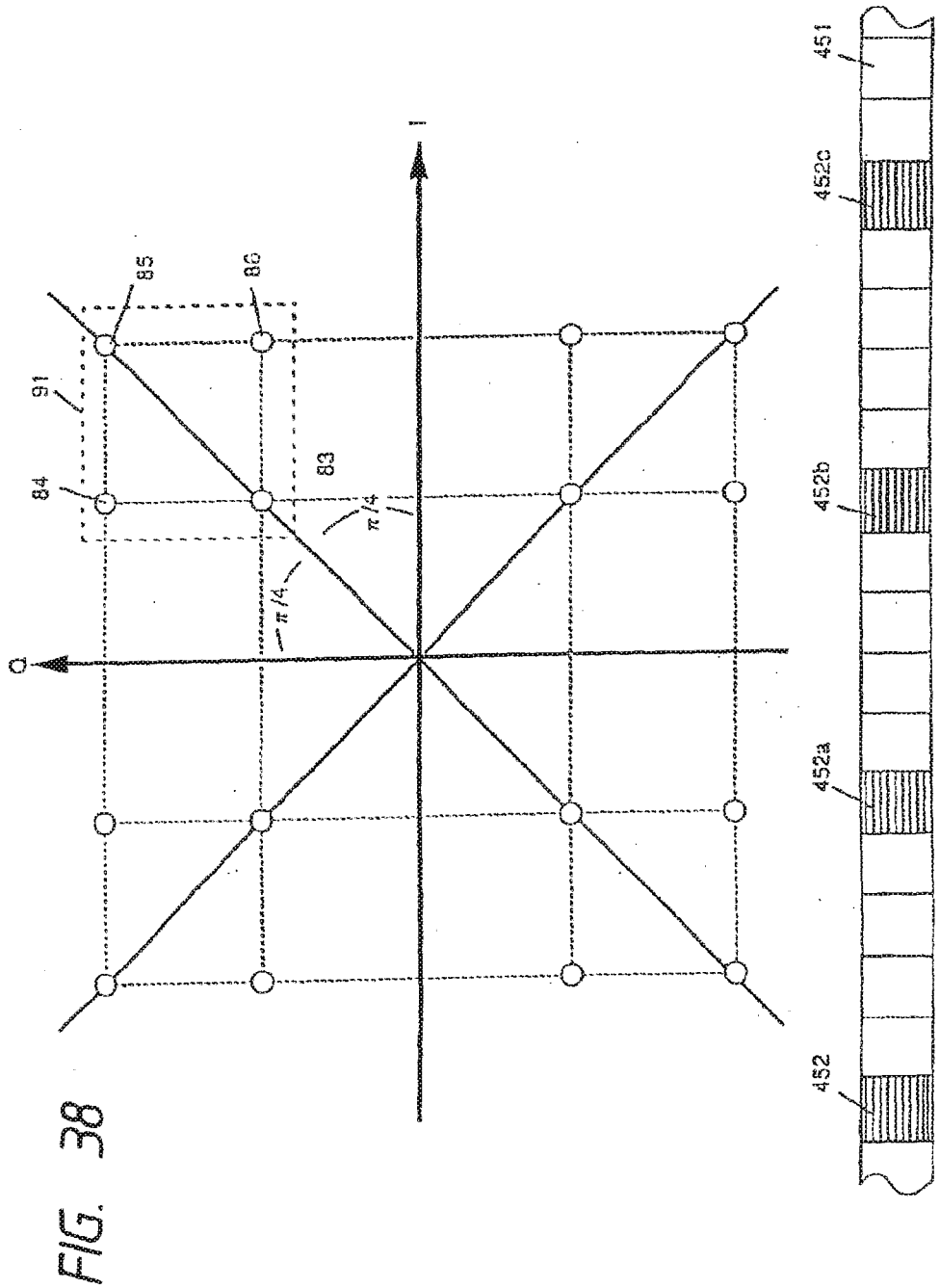


FIG. 38

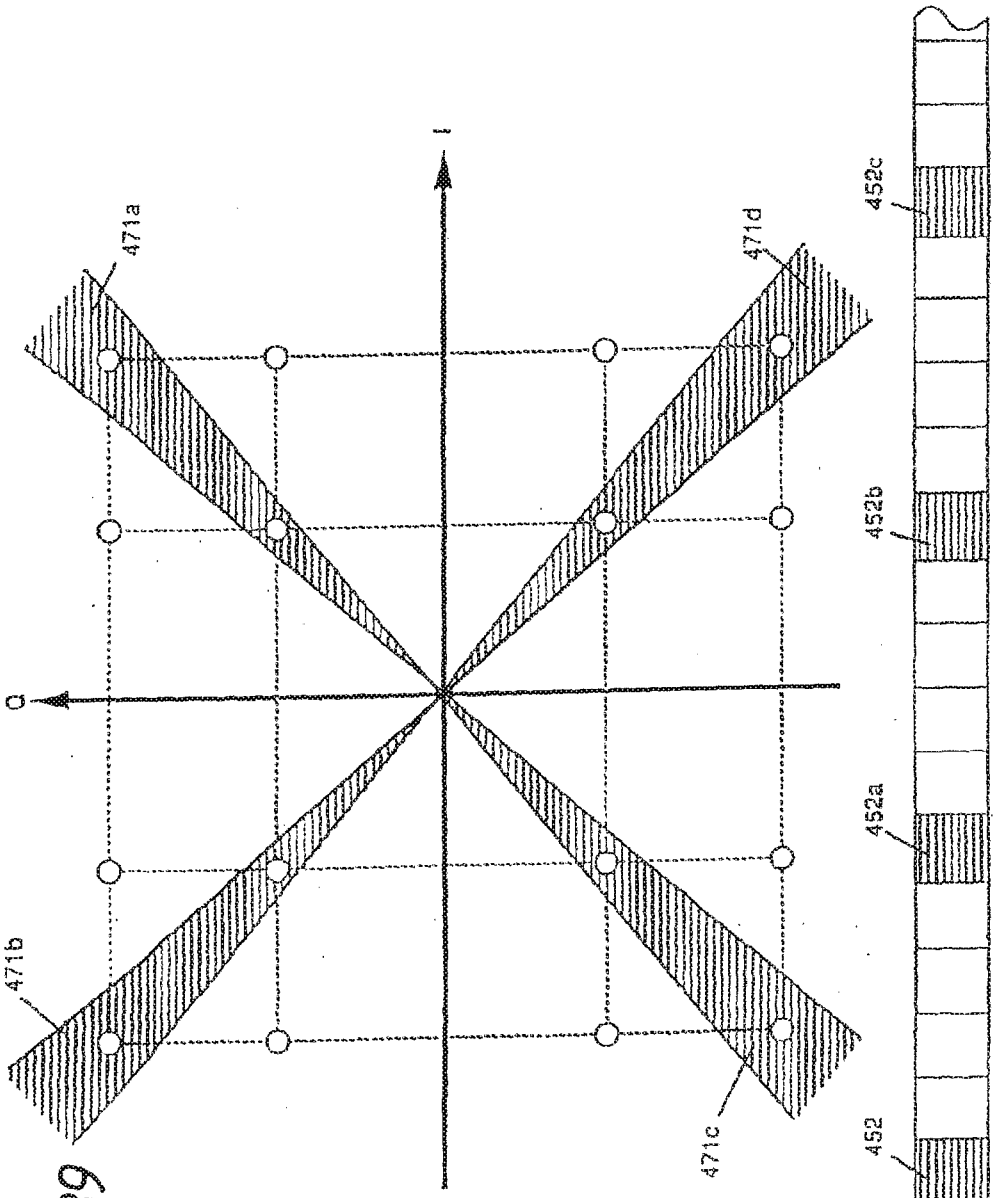


FIG. 39

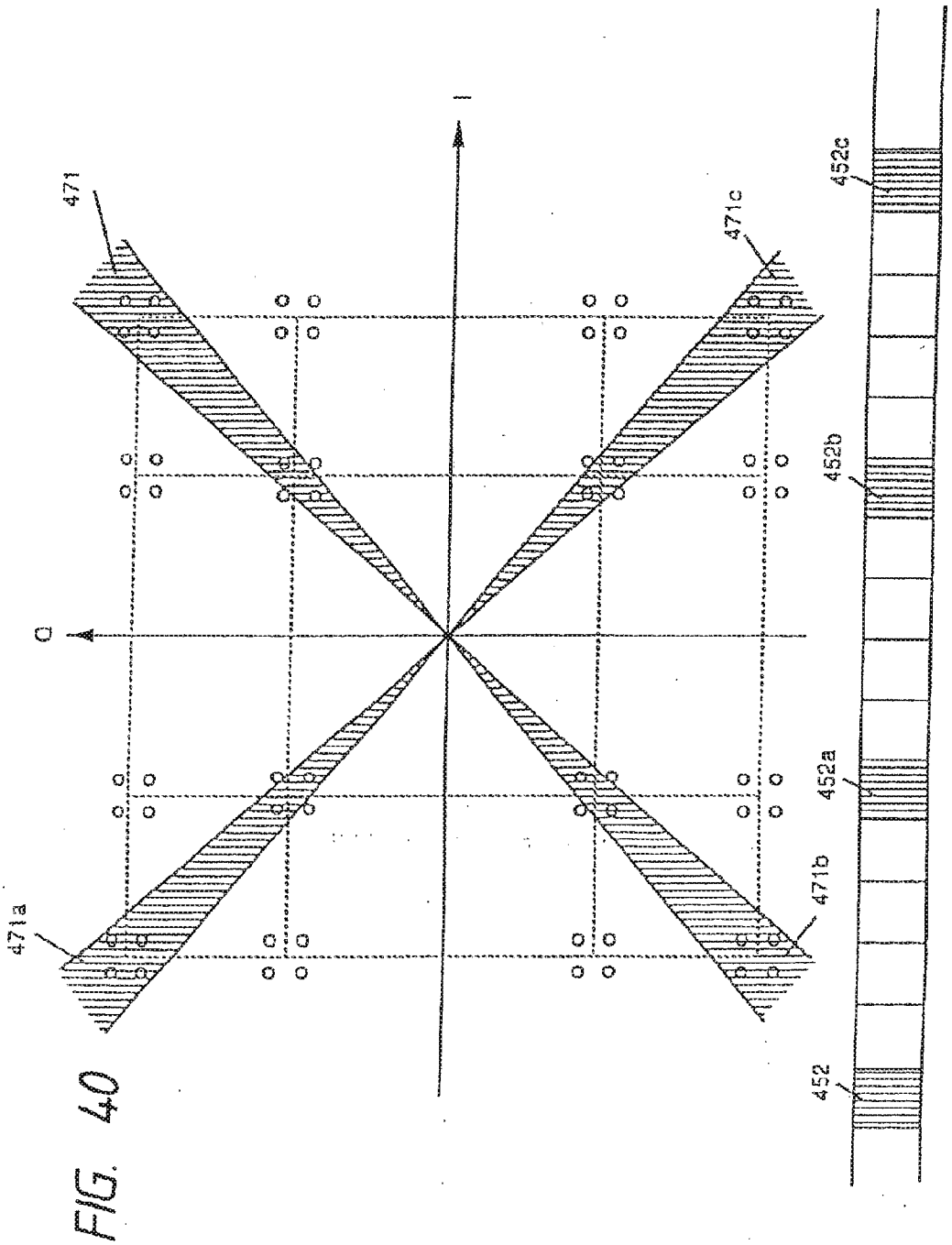


FIG. 40

FIG. 41

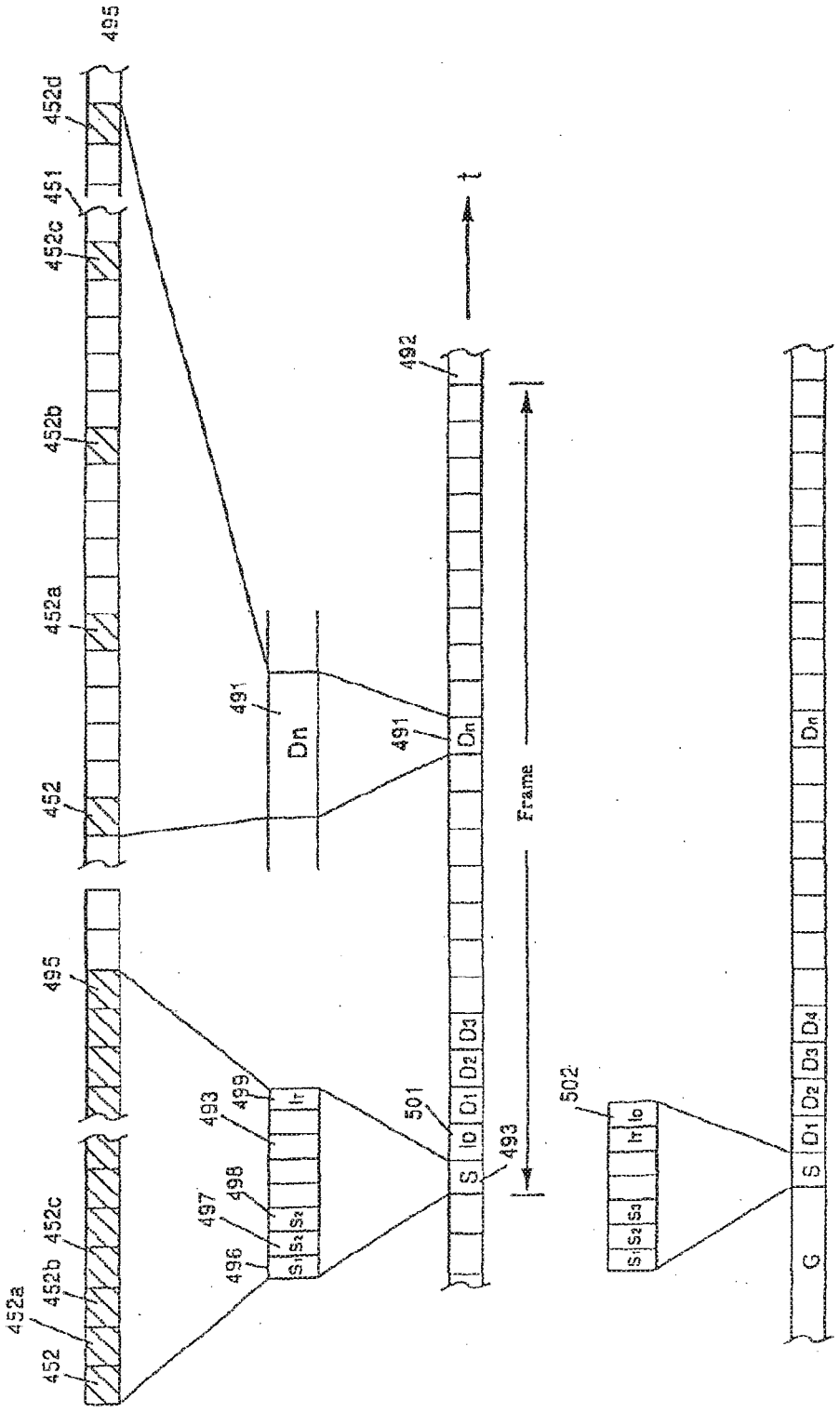


FIG. 42

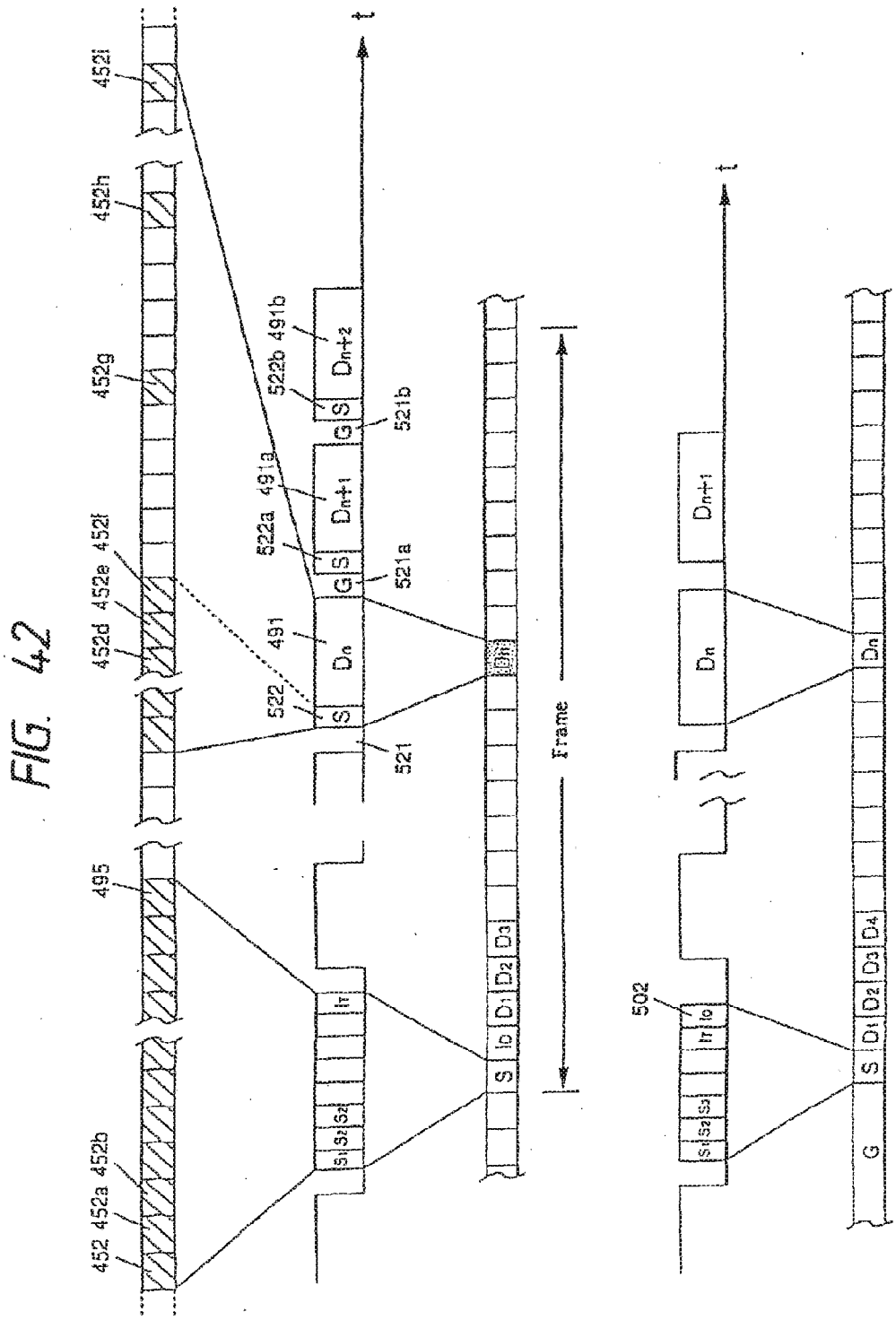


FIG. 43

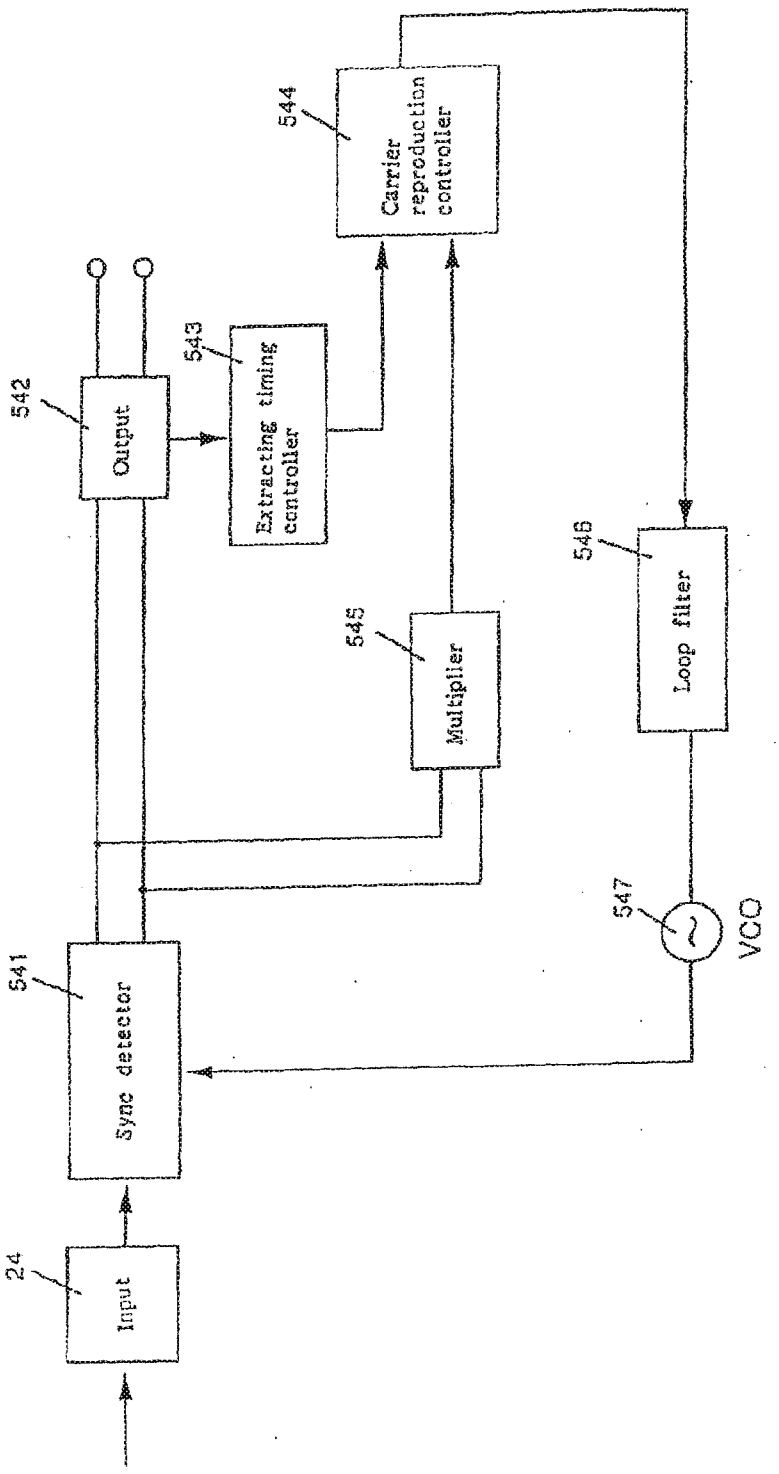
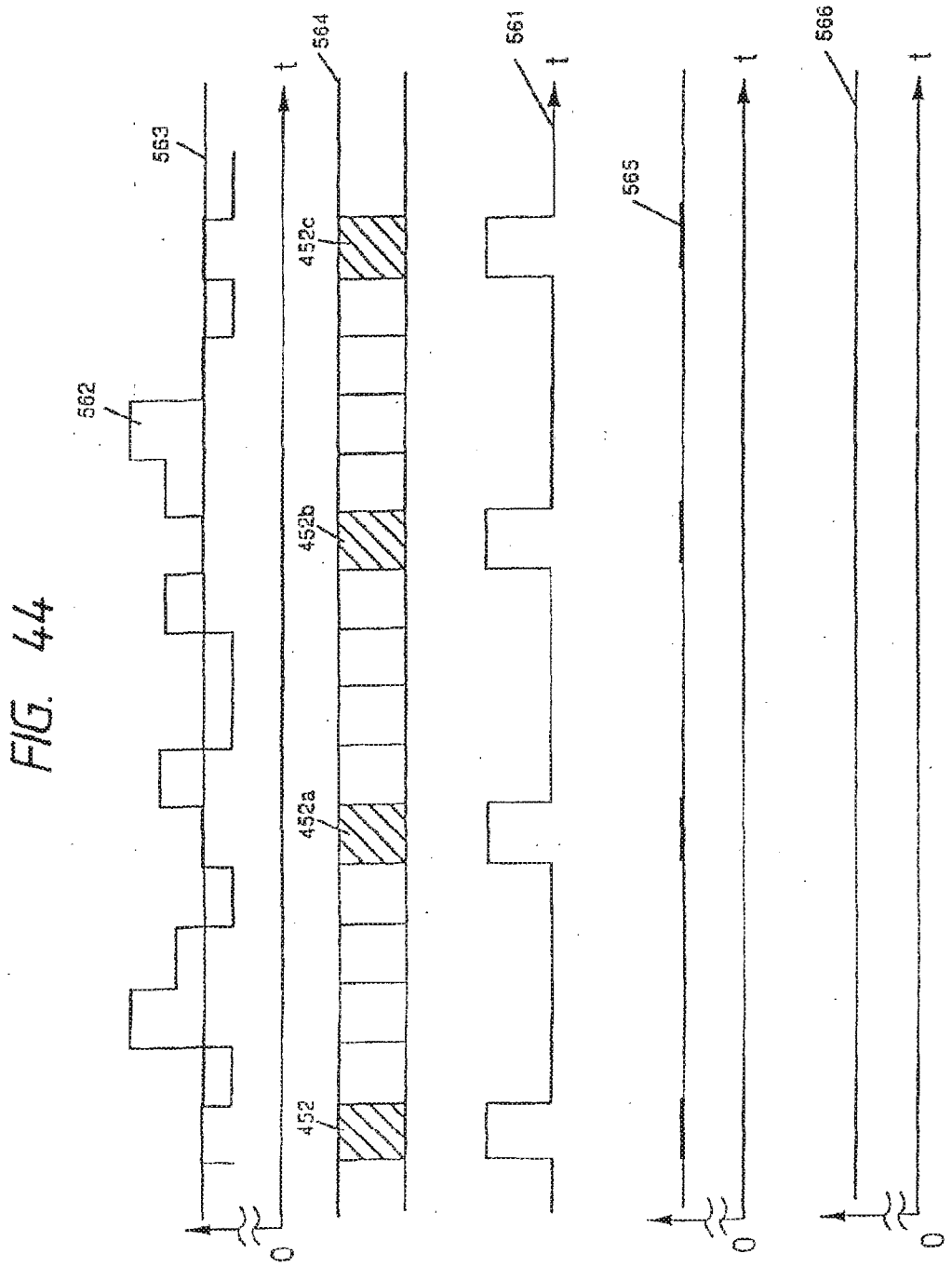


FIG. 44



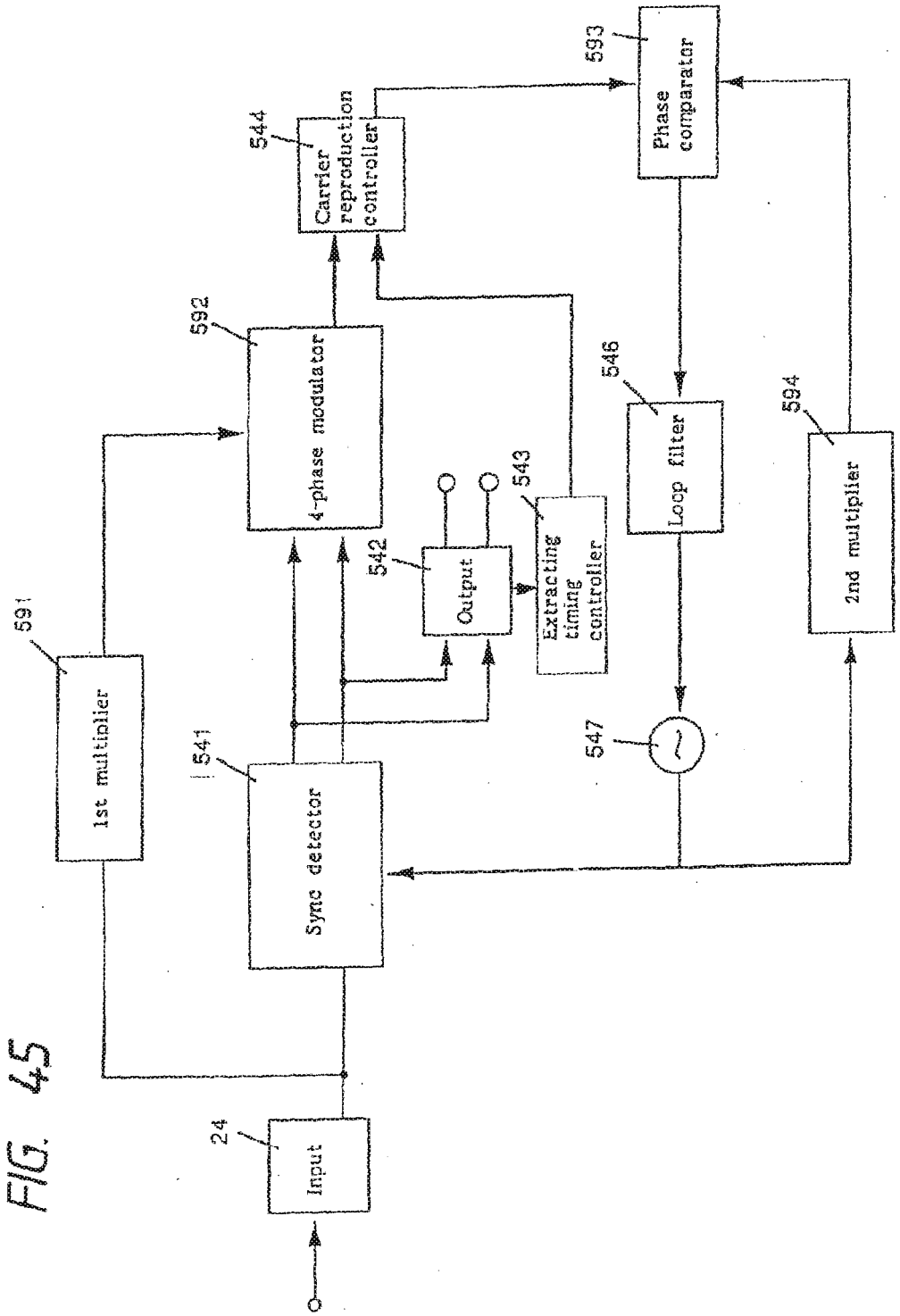
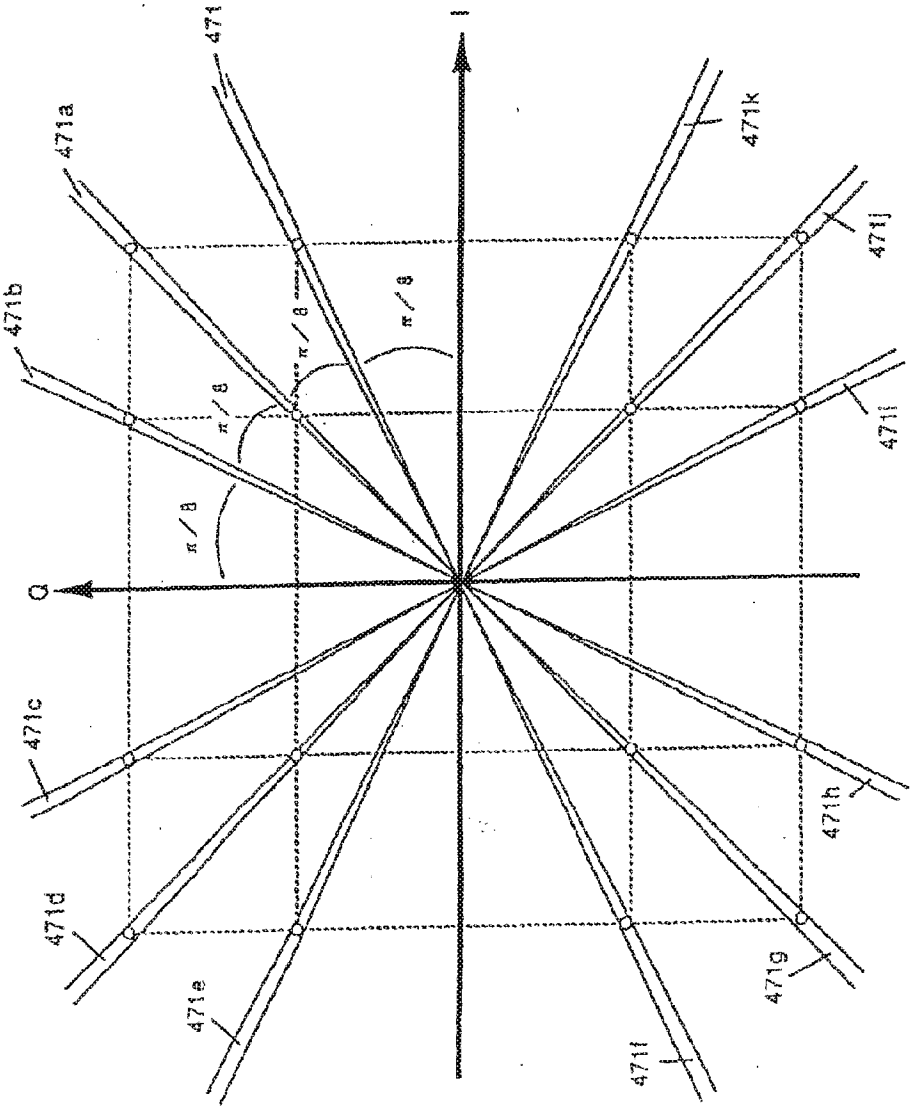


FIG. 45

FIG. 46



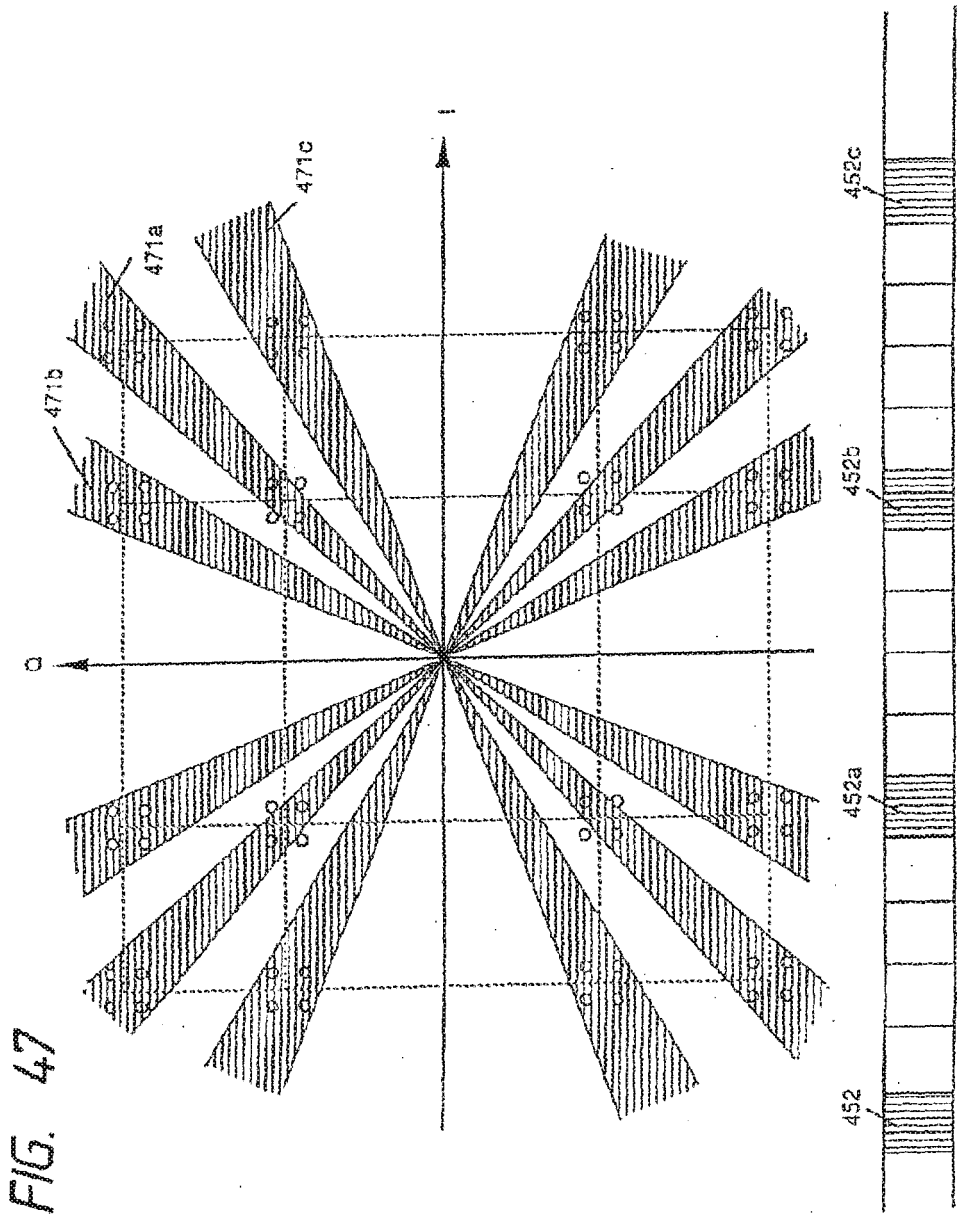
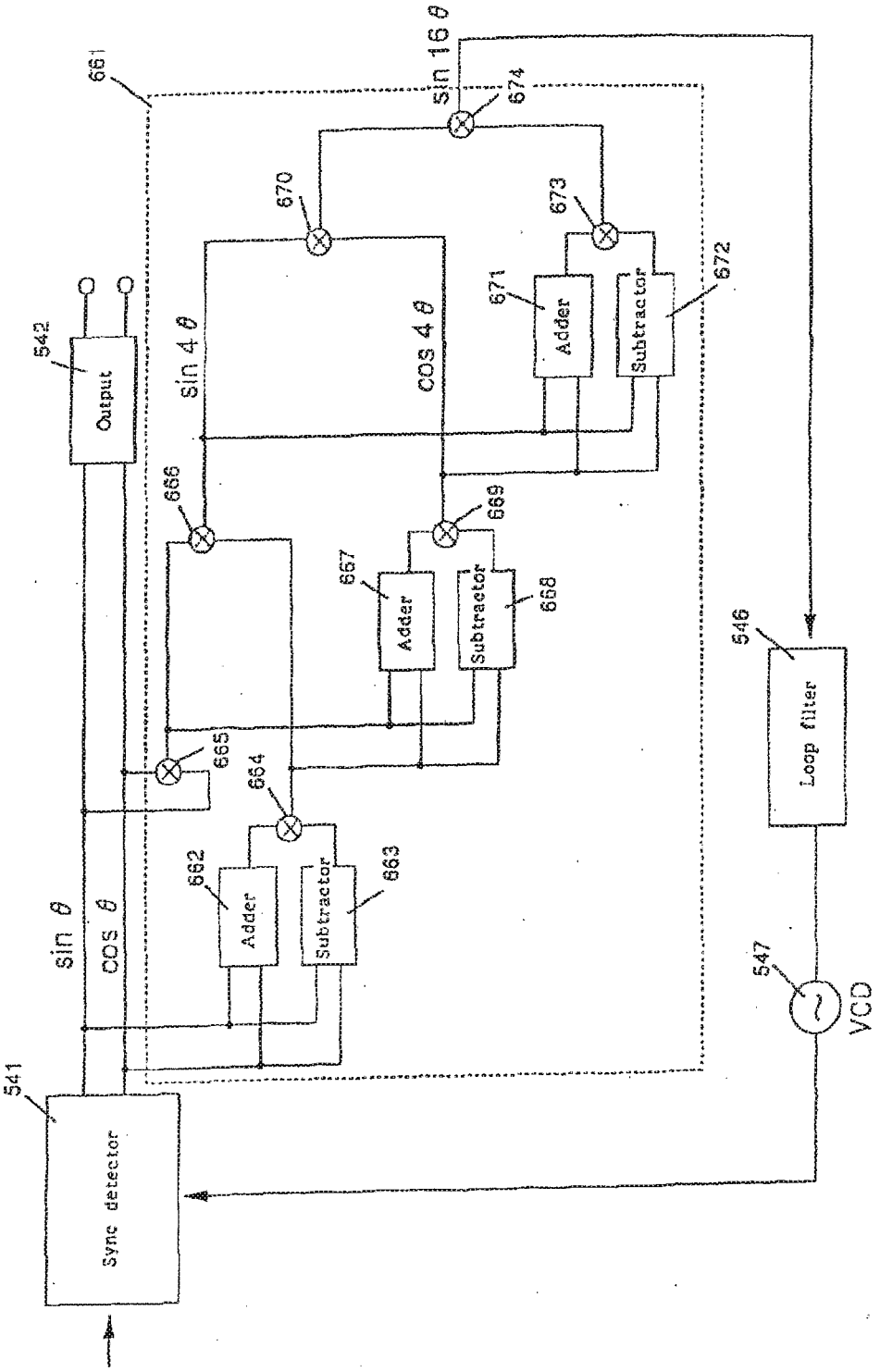


FIG. 47

FIG. 48



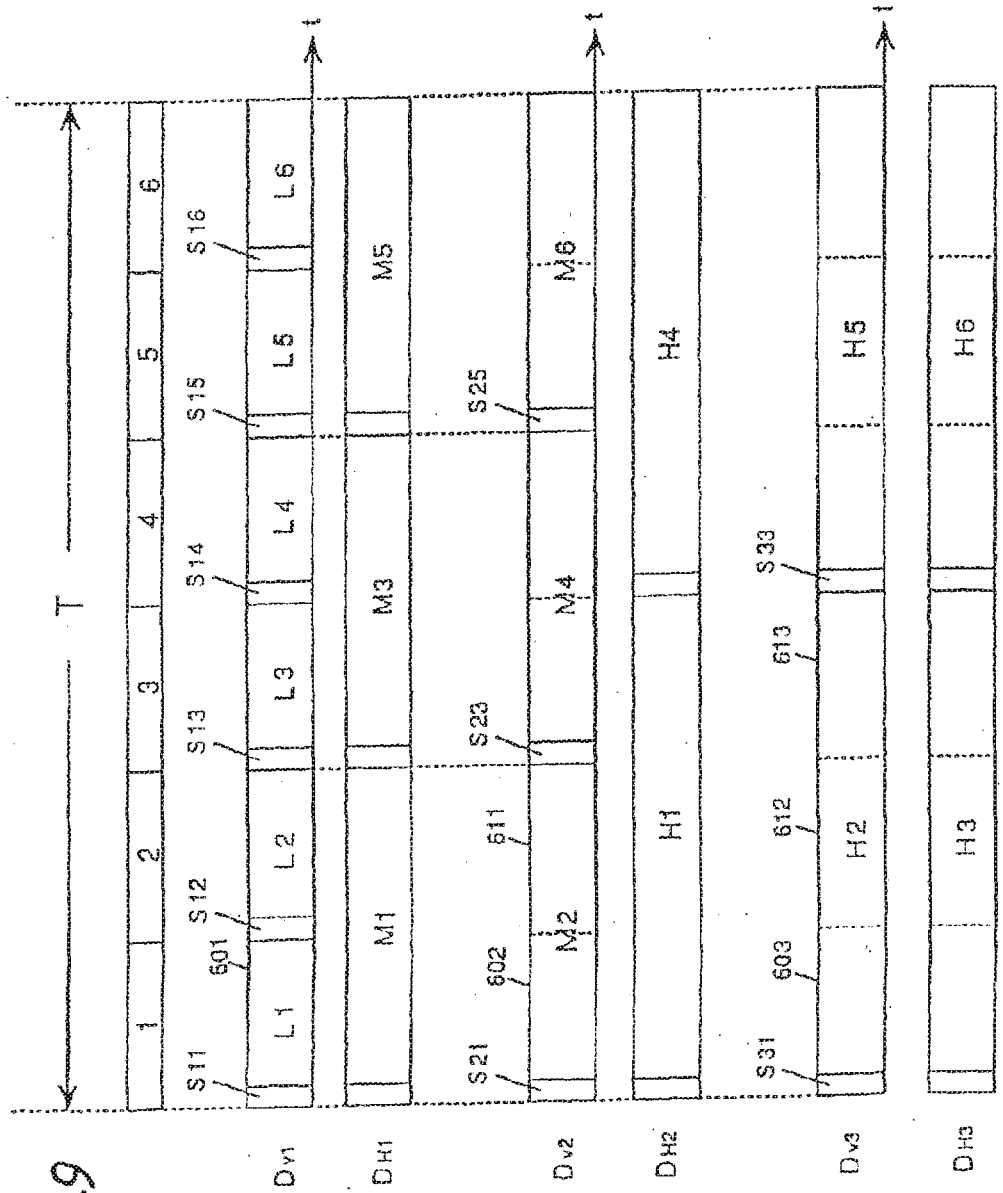


FIG. 49

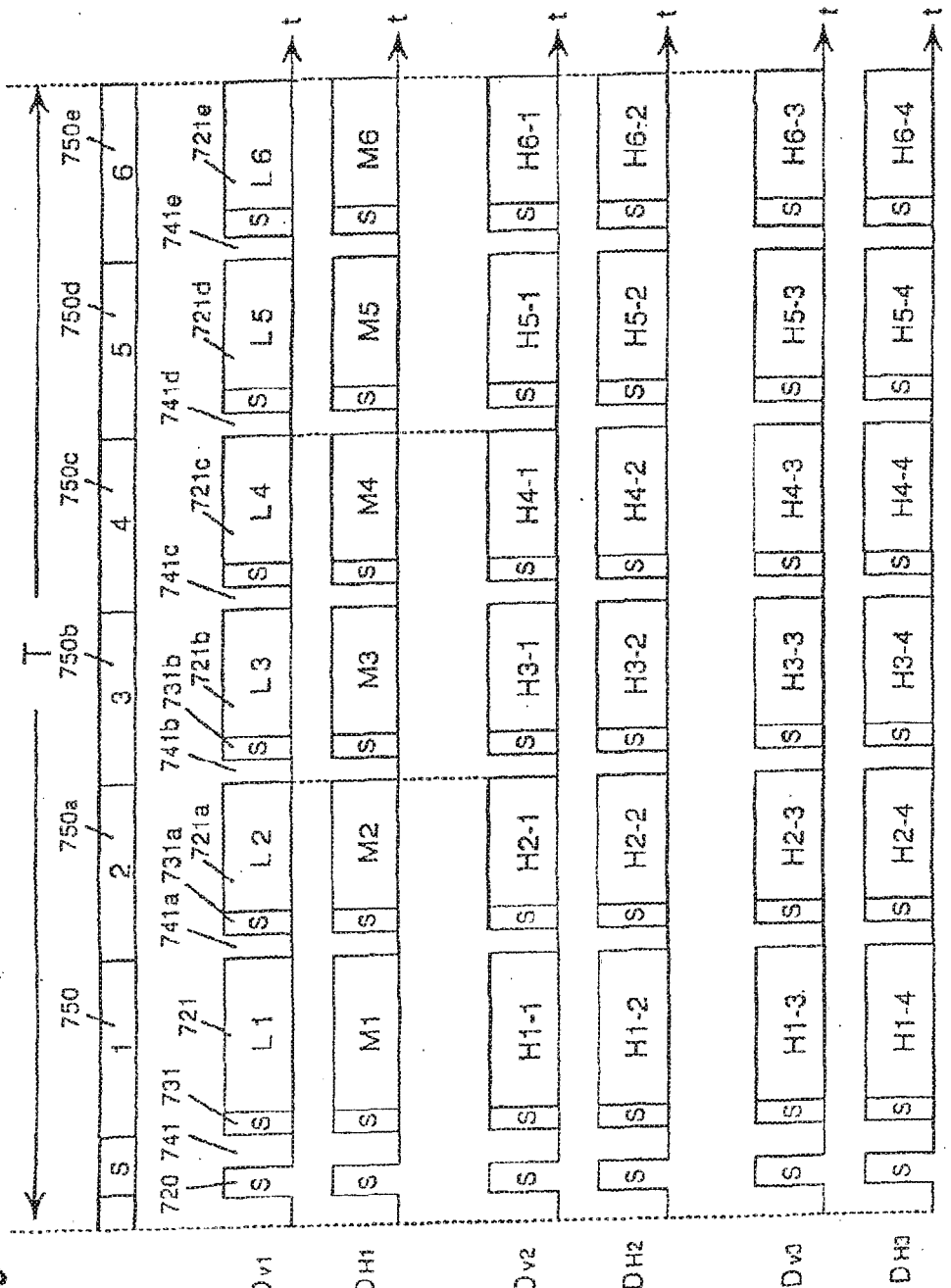


FIG. 50

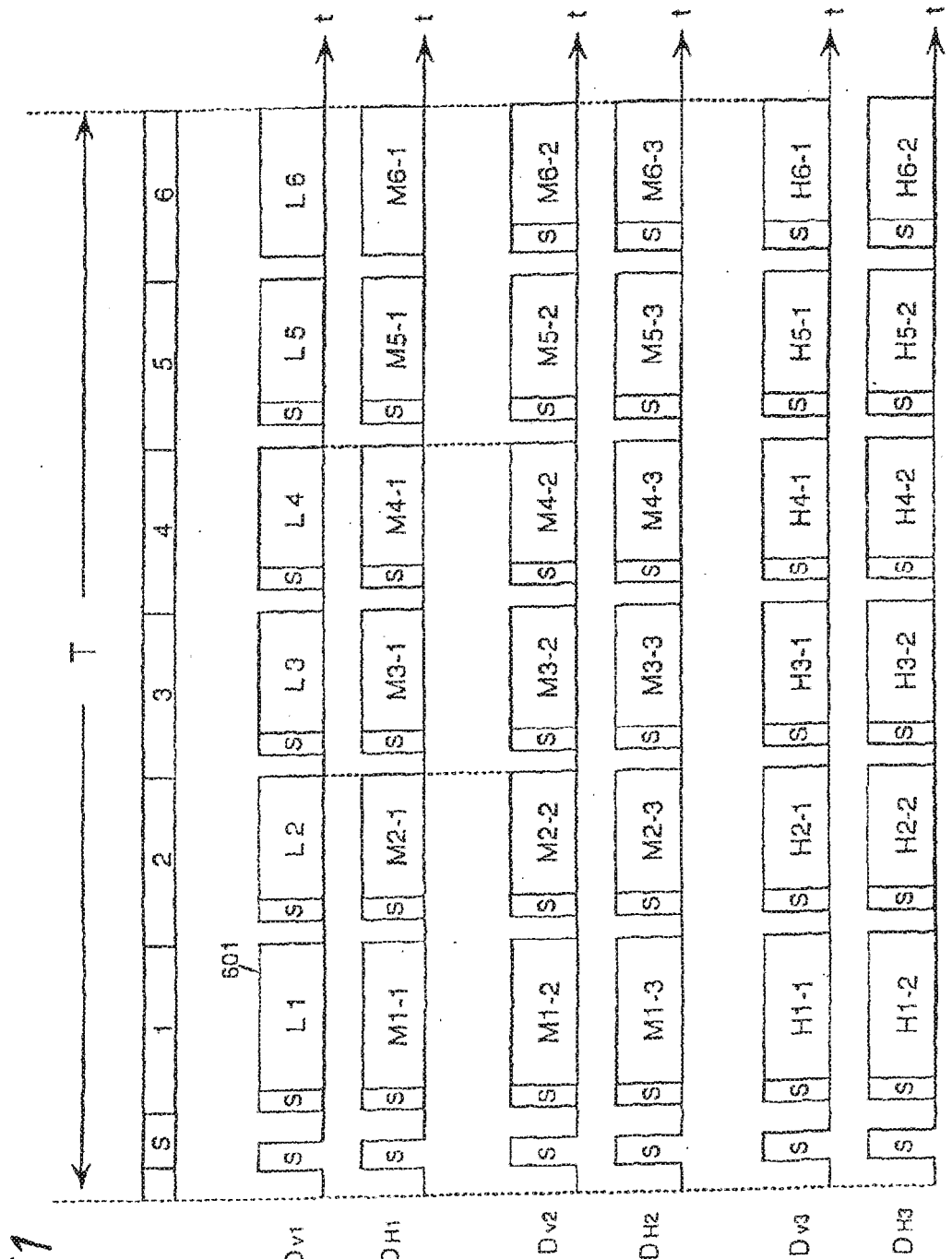


FIG. 51

FIG. 52

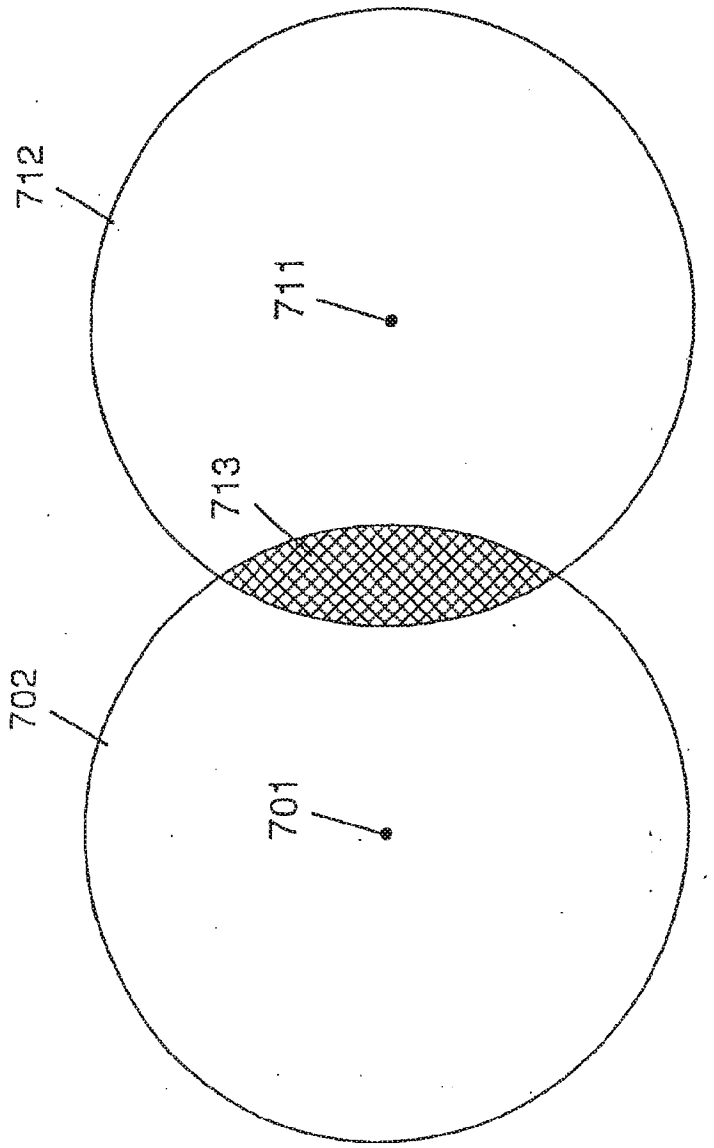


FIG. 53

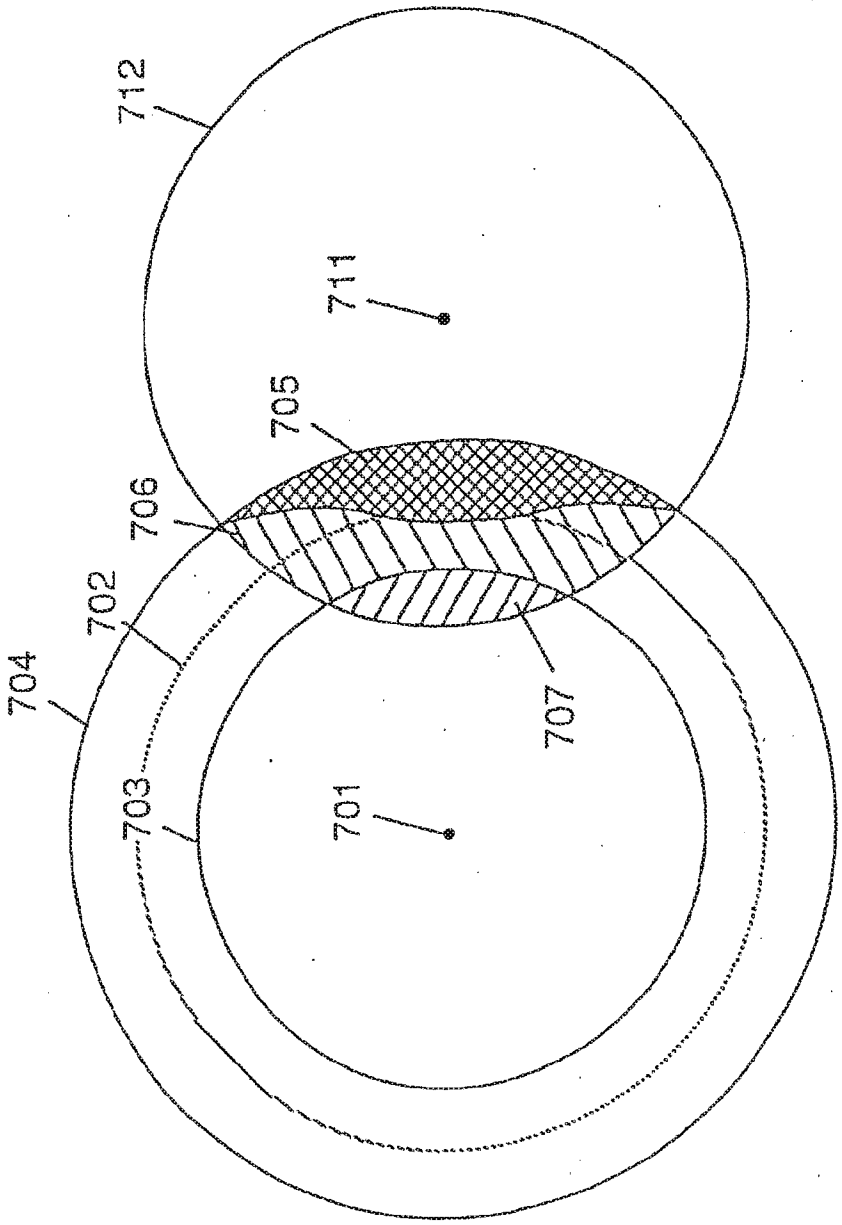


FIG. 54

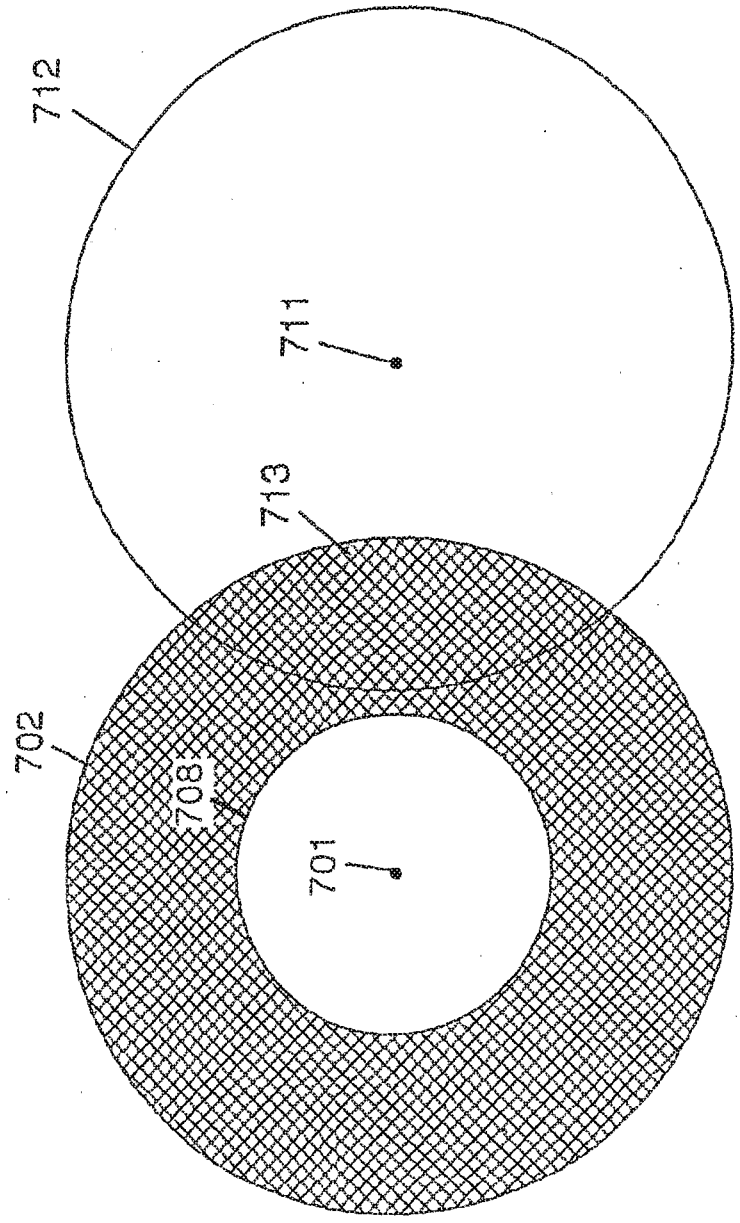


FIG. 55

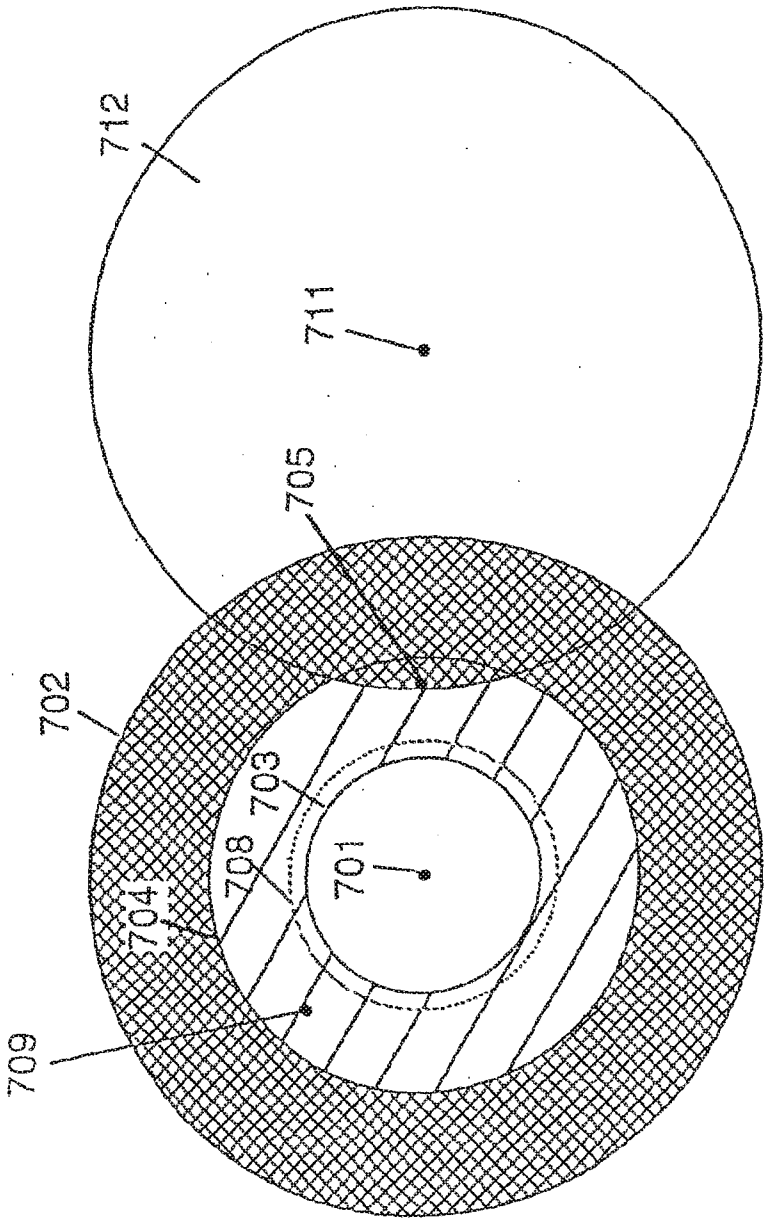
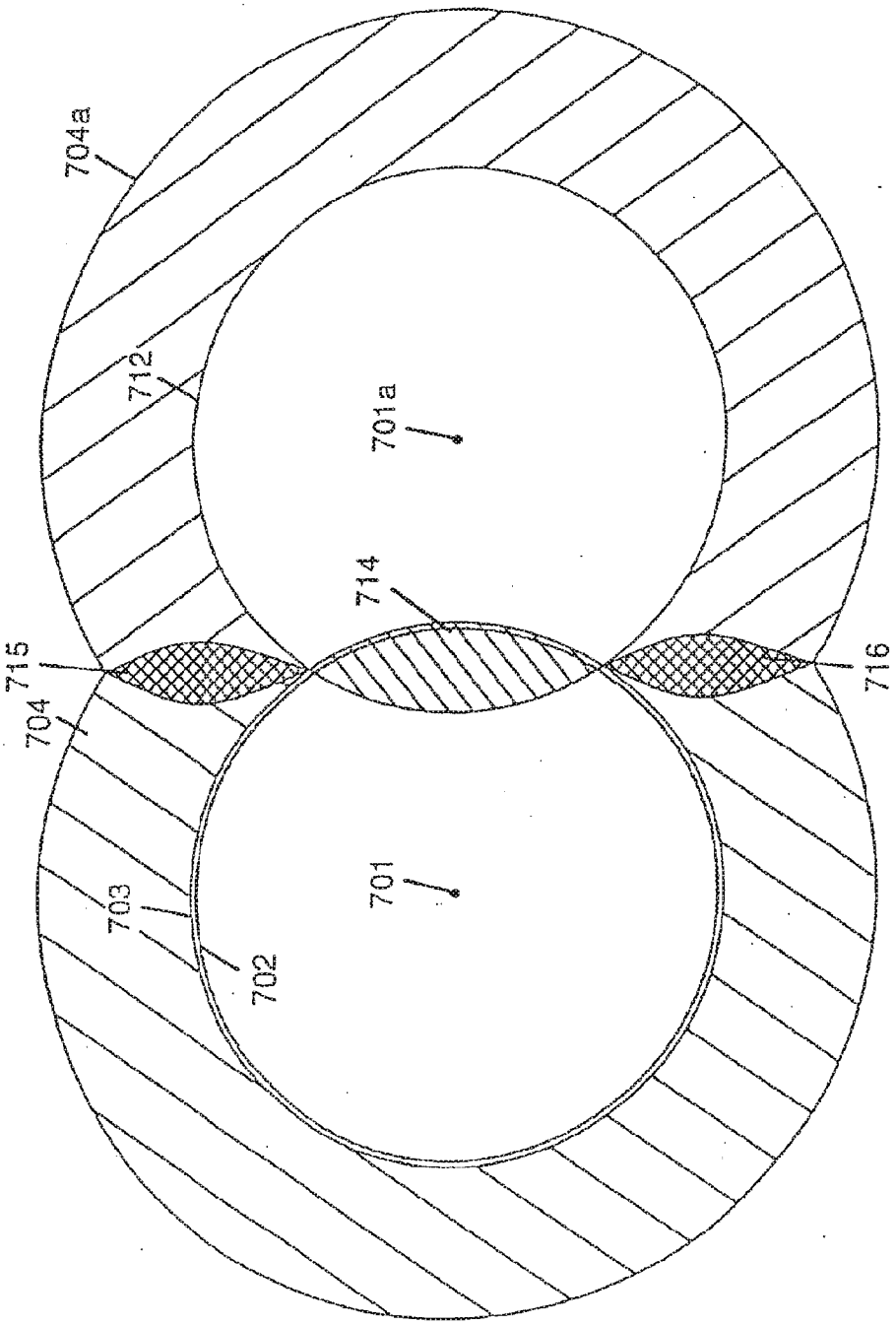


FIG. 56



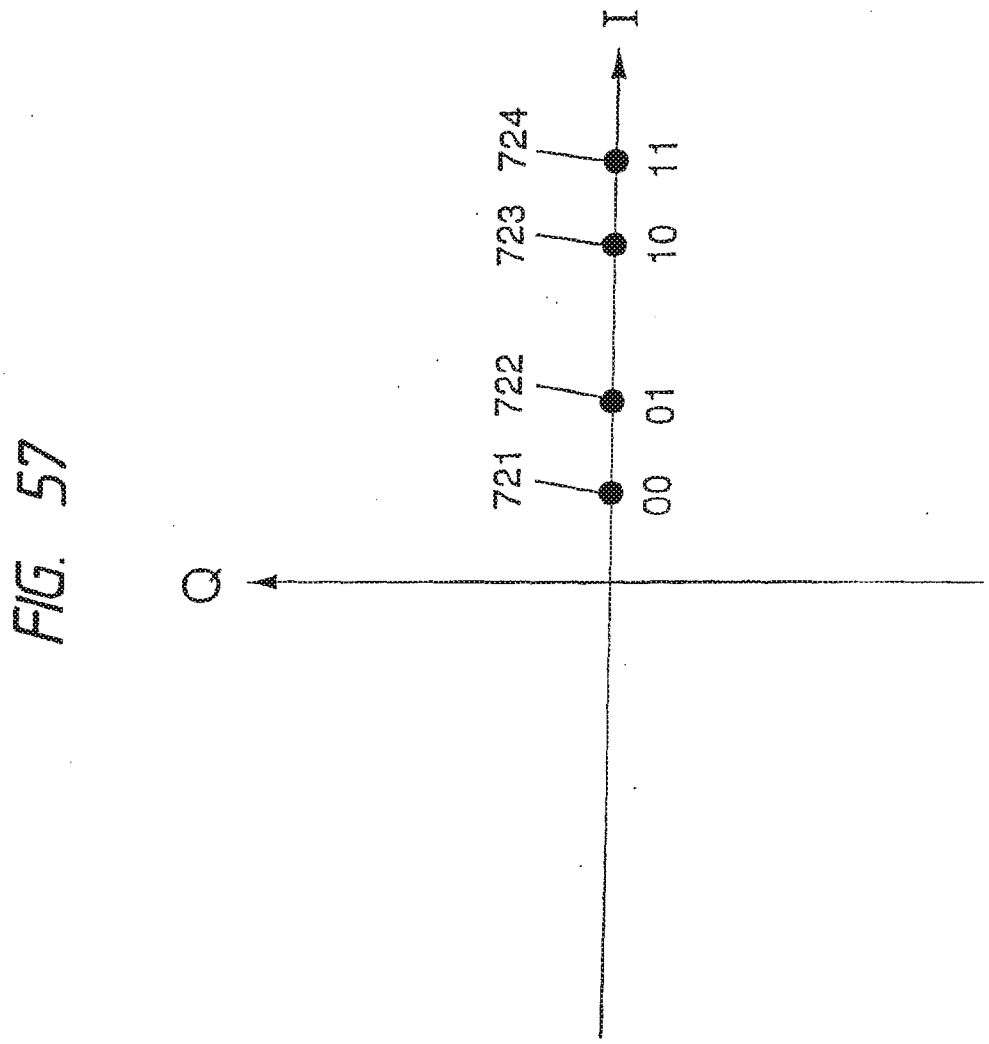


FIG. 57

FIG. 58

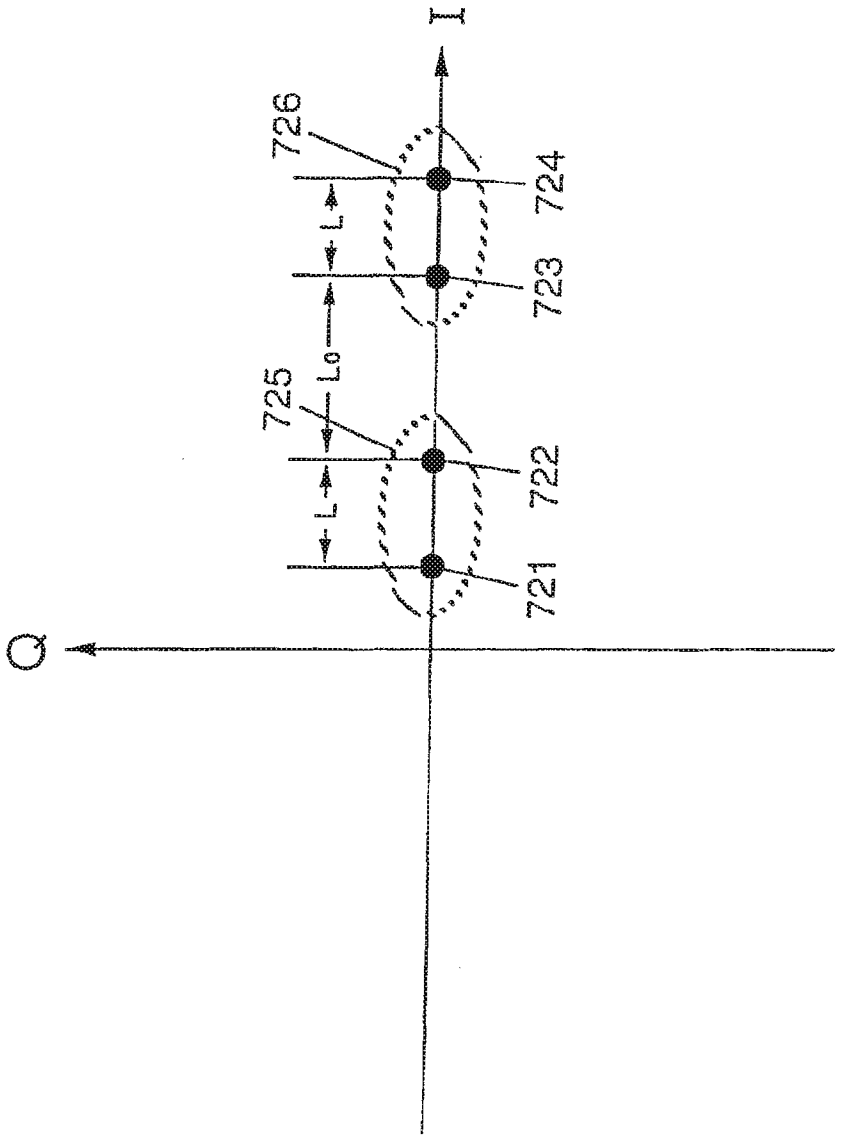


FIG. 59

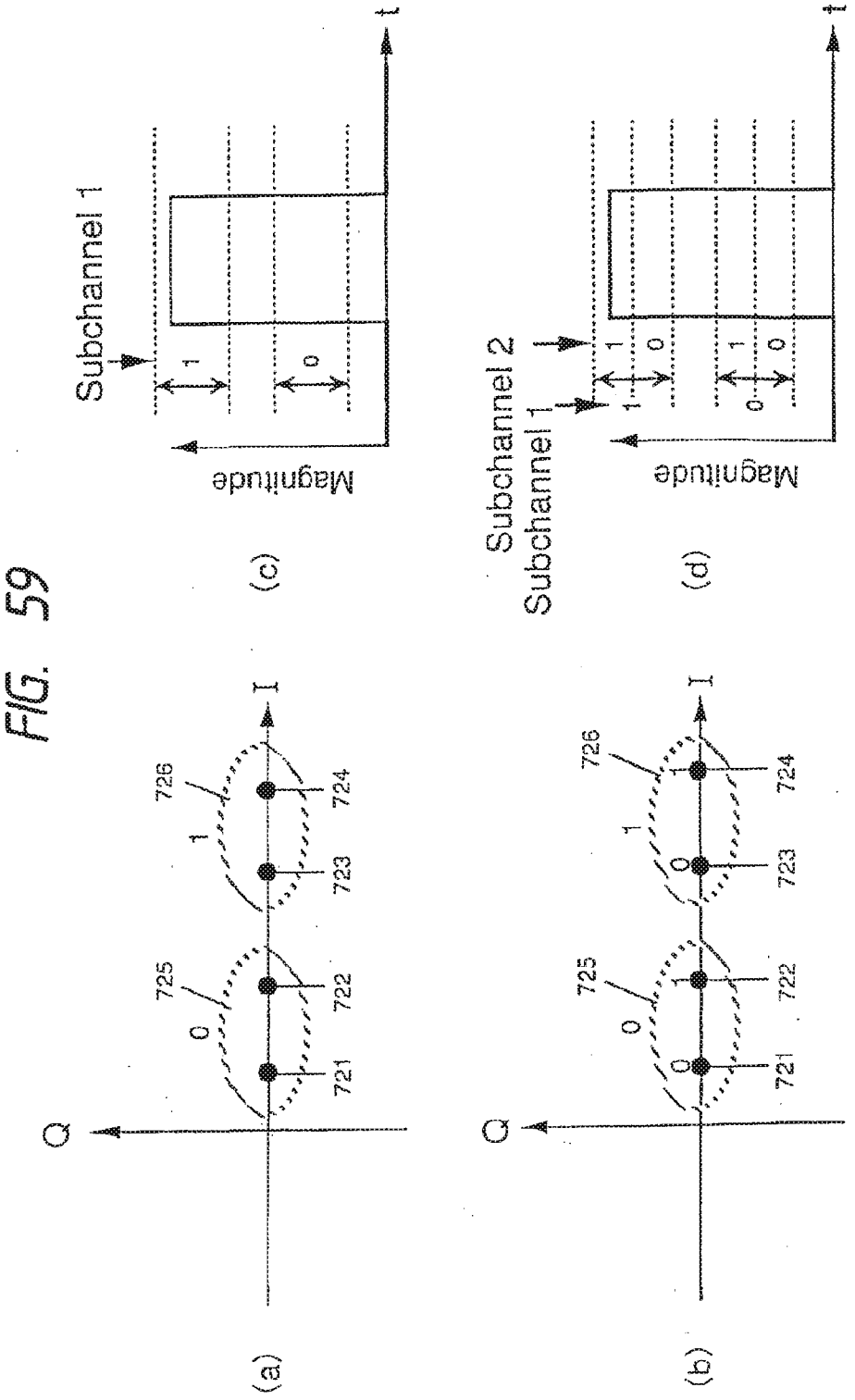


FIG. 60

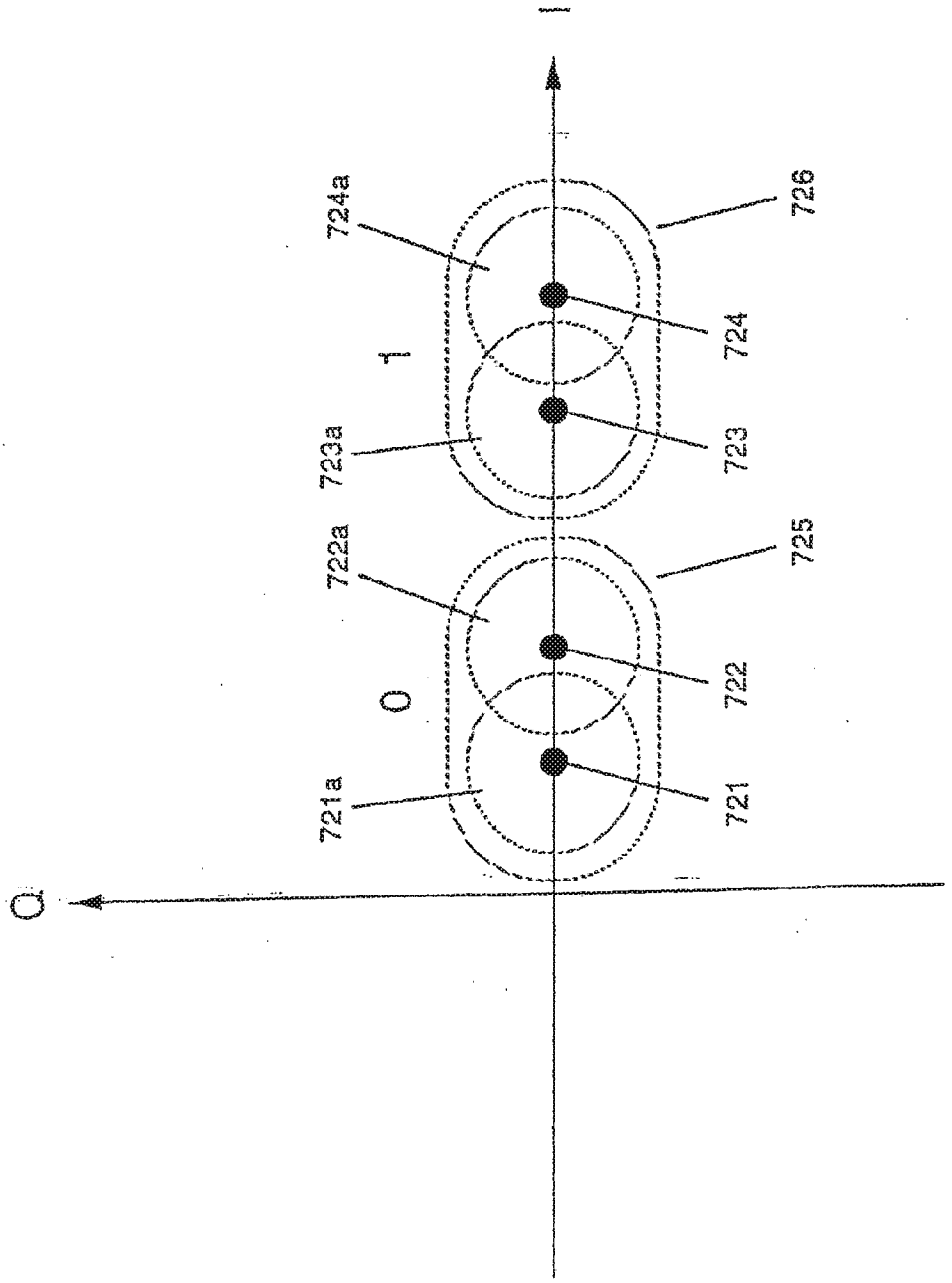
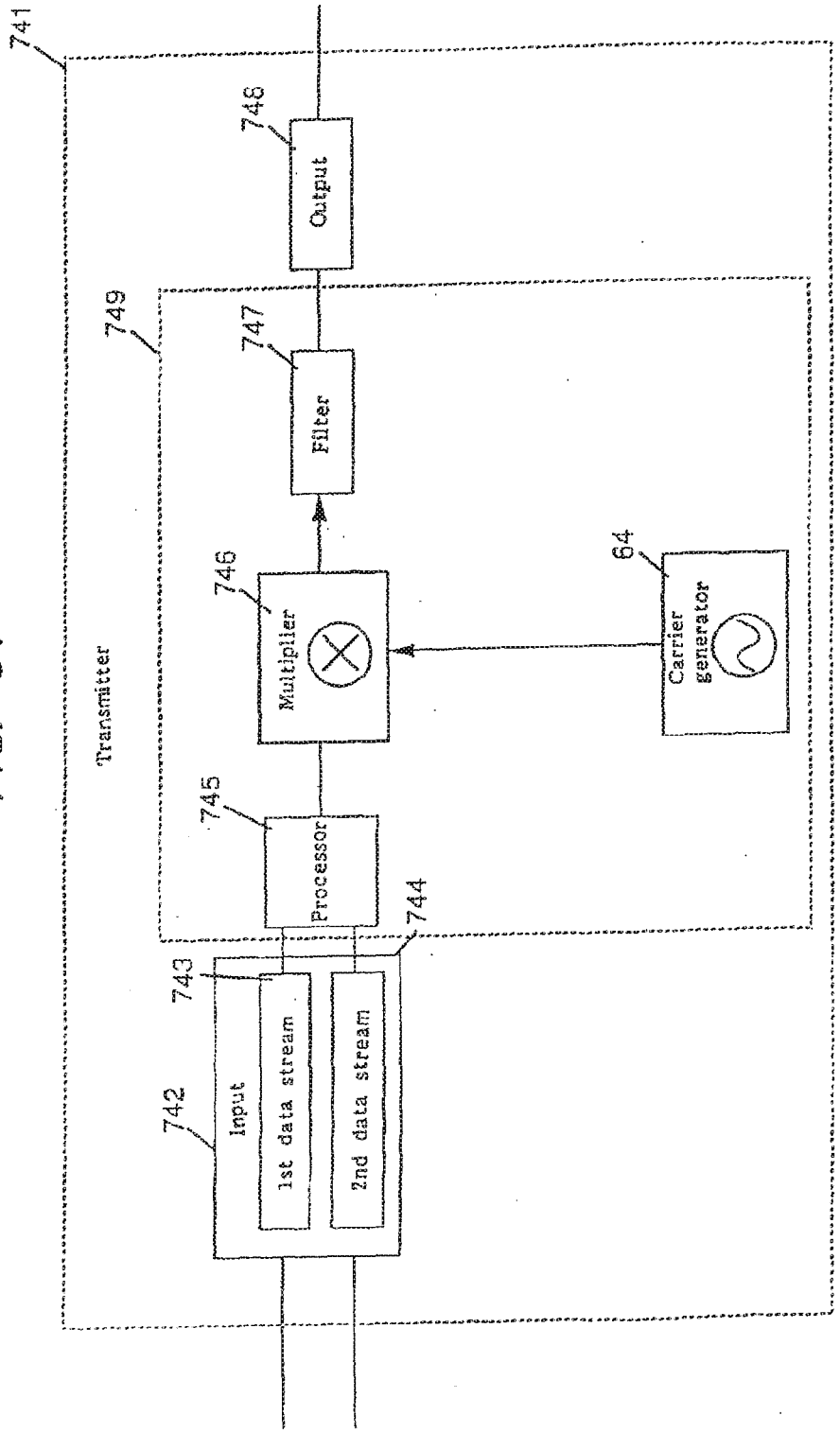


FIG. 61



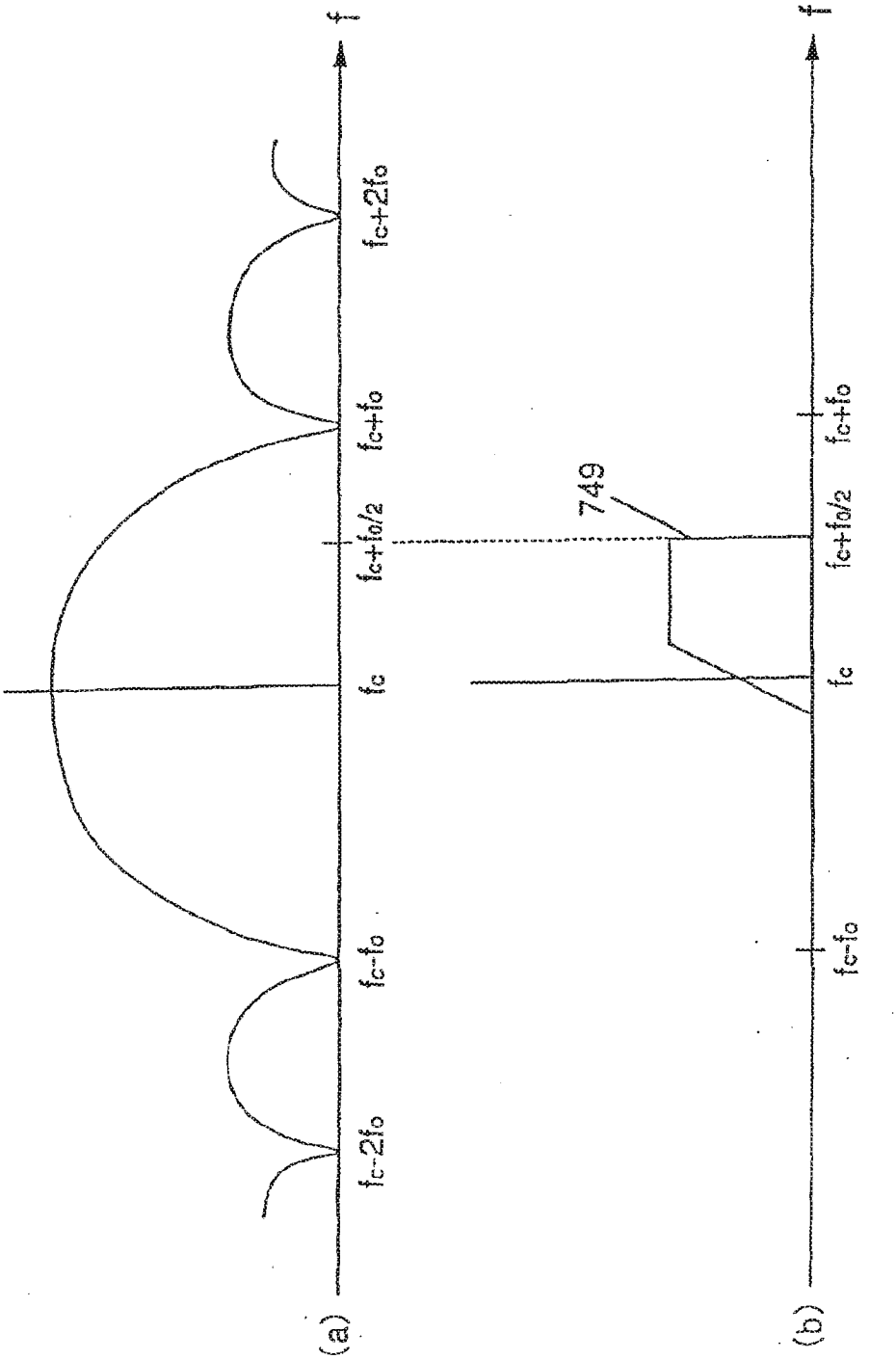


FIG. 62

FIG. 63

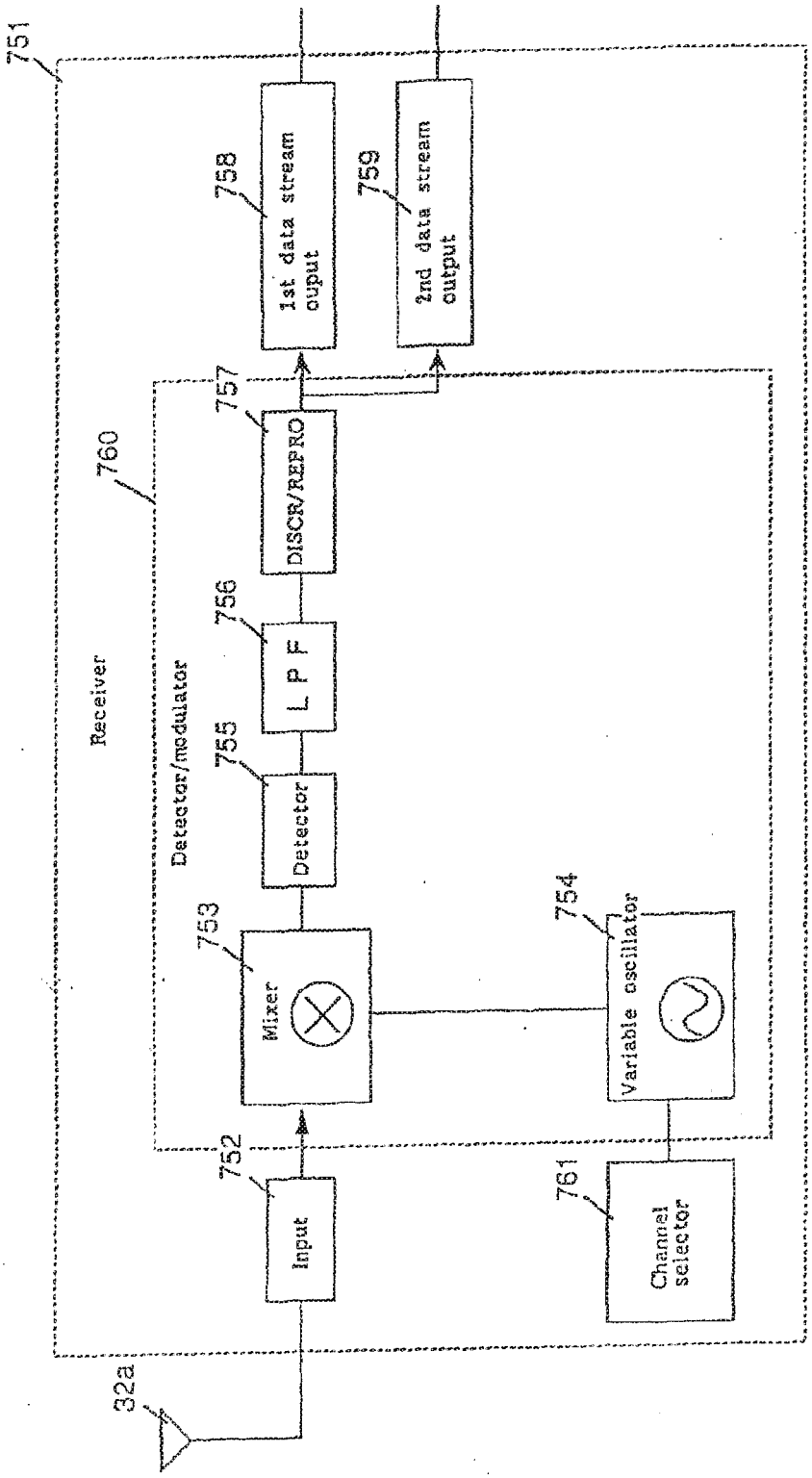

751
758
1st data stream ouput
759
2nd data stream output
757
DISCR/REPRO
760
Receiver
Detector/modulator
756
L P F
755
Detector
753
Mixer
754
Variable oscillator
752
Input
761
Channel selector
32a

FIG. 64

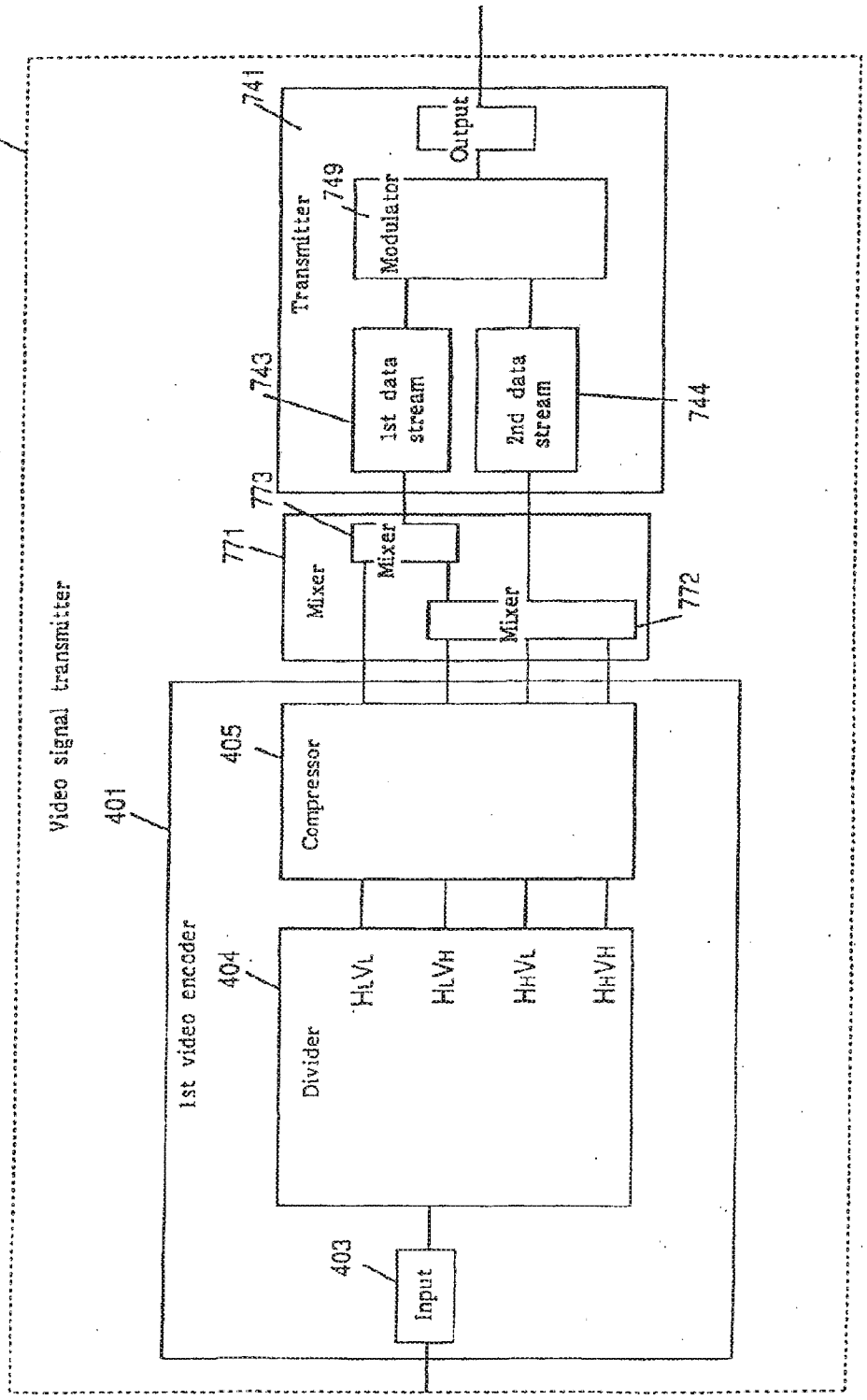


FIG. 65

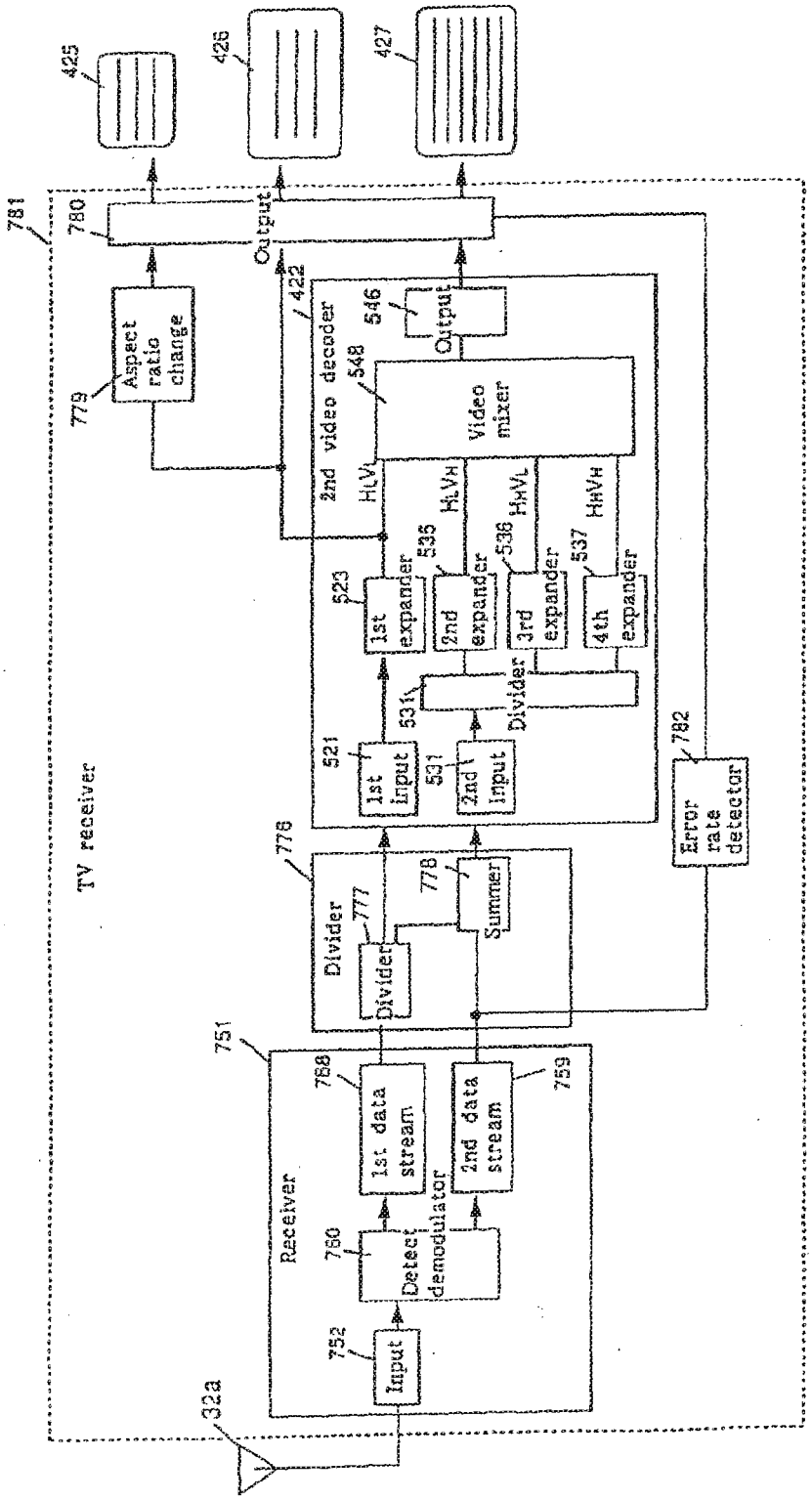

TV receiver
781
780
Output
425
426
427
Aspect ratio change
779
422
2nd video decoder
546
Output
548
Video mixer
HLVL
HLVH
HHVL
HHVH
523
1st expander
535
2nd expander
536
3rd expander
537
4th expander
Divider
531
521
1st input
501
2nd input
782
Error rate detector
778
Divider
777
Divider
778
Summer
751
Receiver
768
1st data stream
759
2nd data stream
760
Detect demodulator
752
Input
32a

FIG. 66

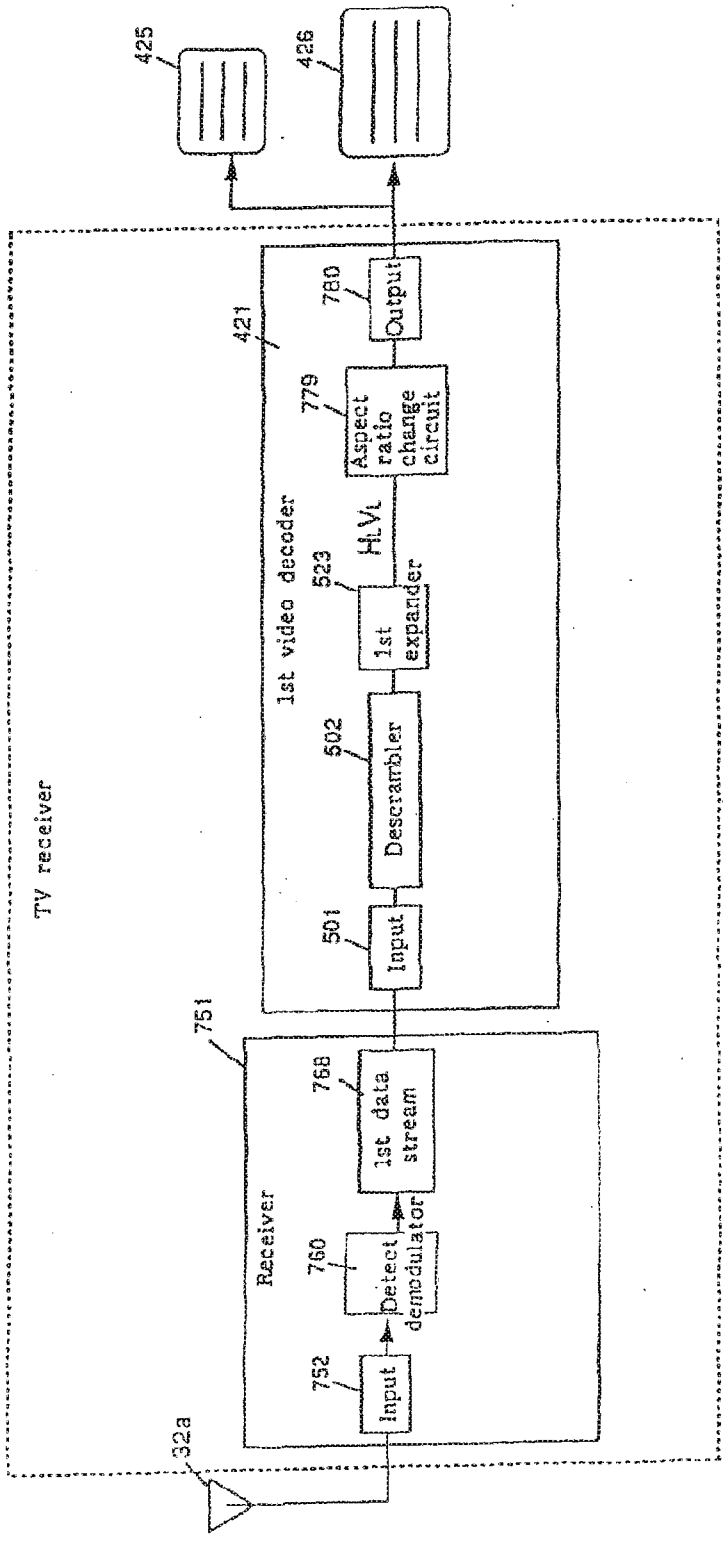


FIG. 67

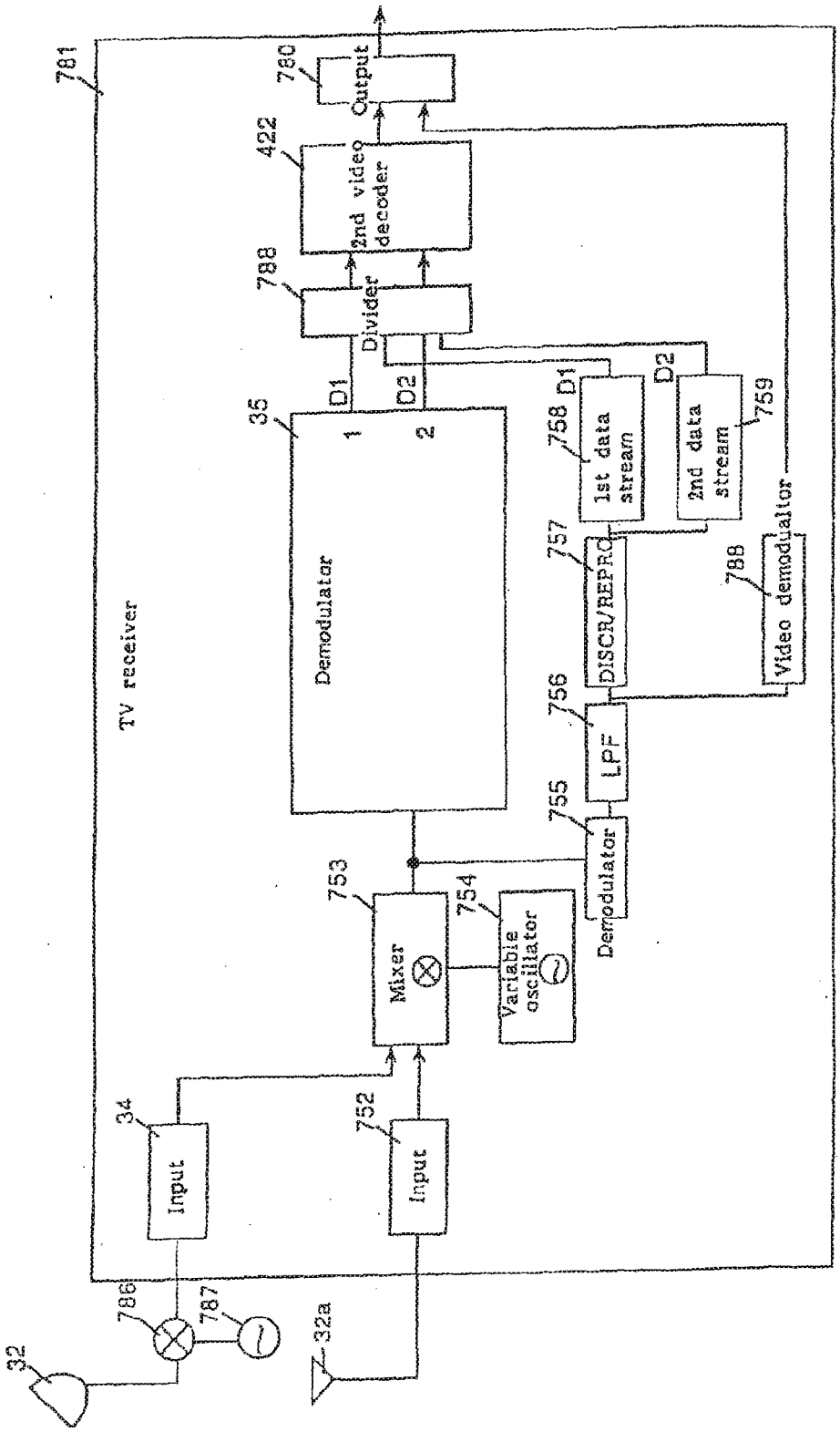


FIG. 68

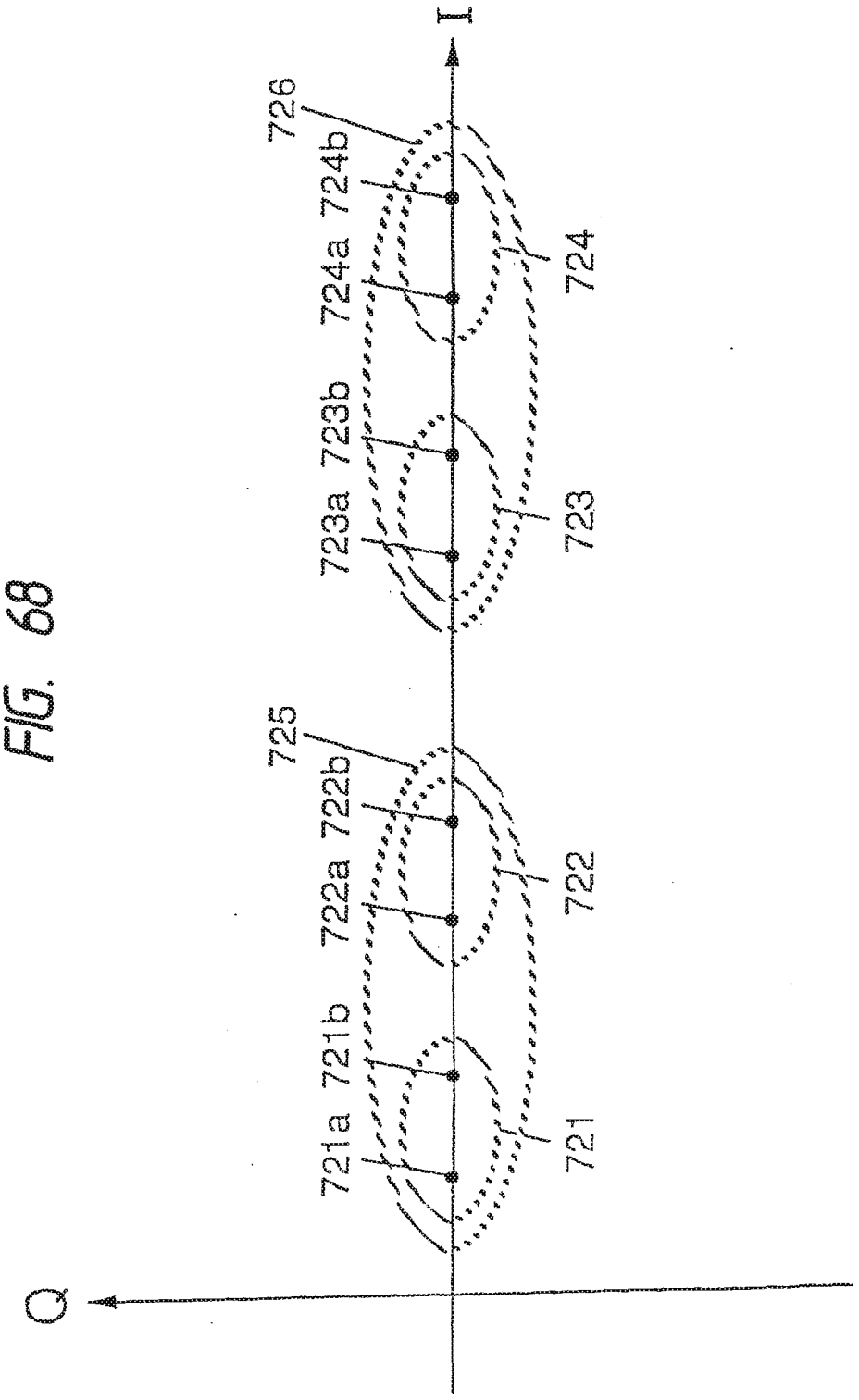
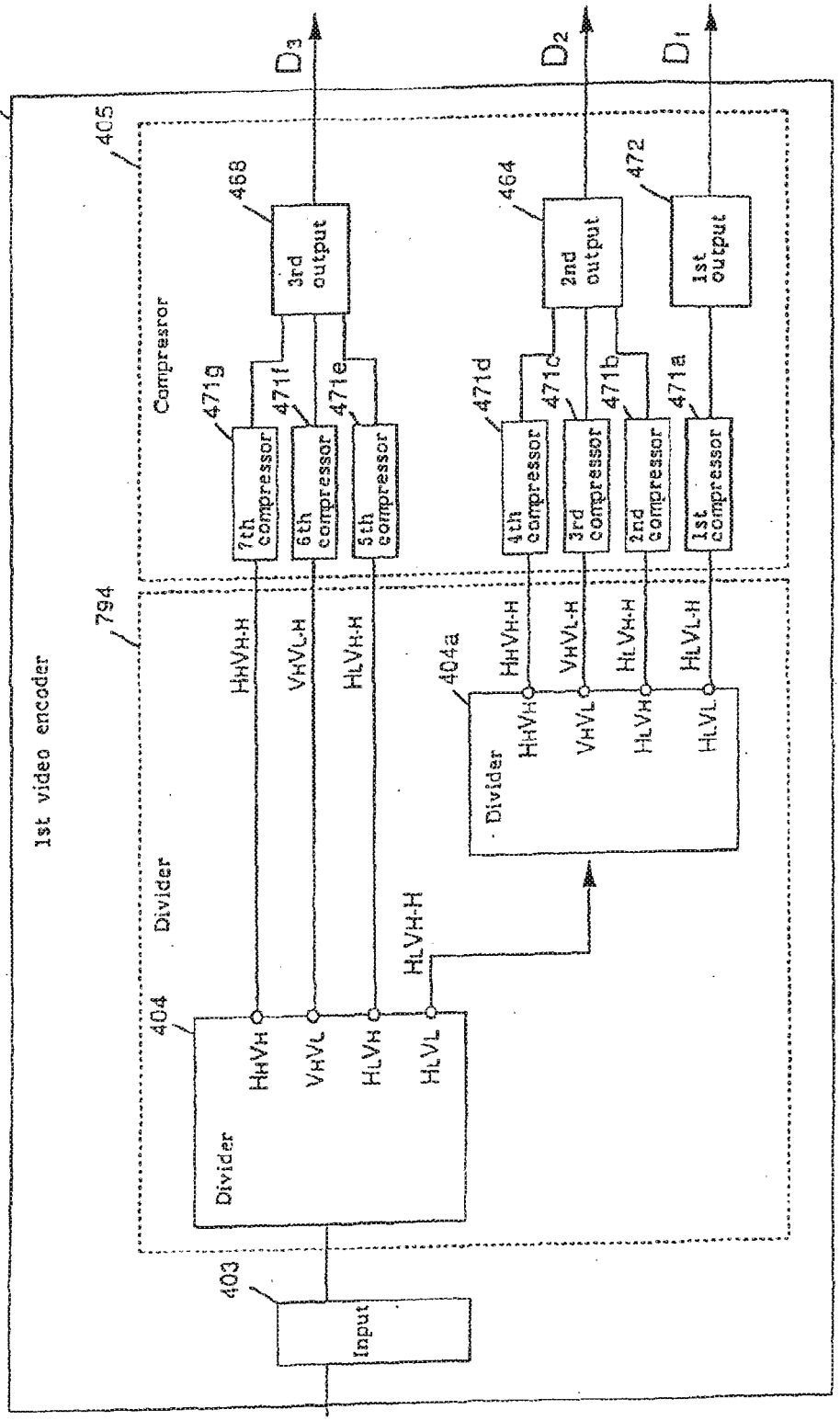


FIG. 69



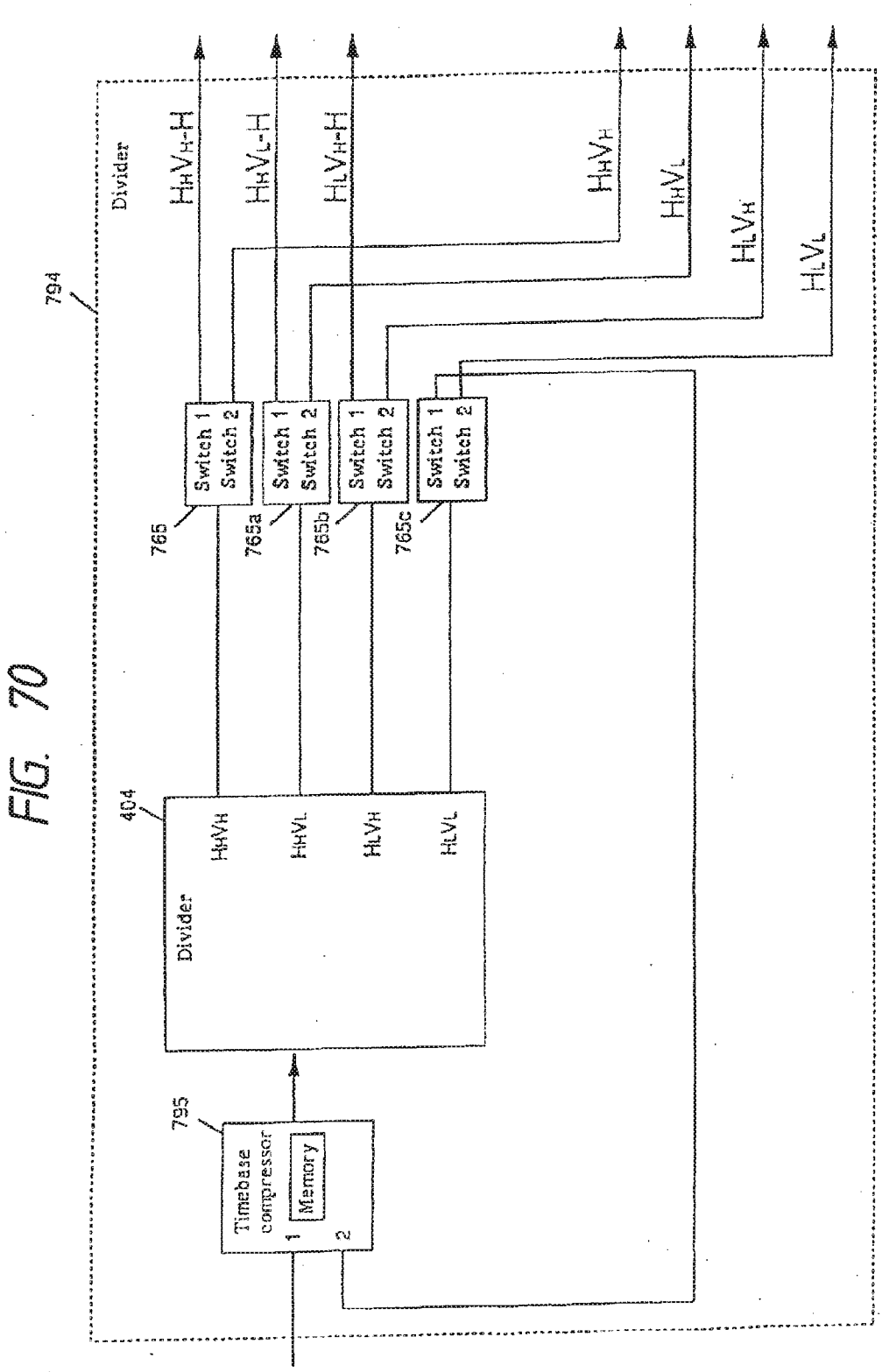

794
Divider
HHVH-H
HHVL-H
HLVH-H
HHVH
HHVL
HLVH
HLVL
Switch 1
Switch 2
765
765a
765b
765c
404
Divider
HHVH
HHVL
HLVH
HLVL
795
Timebase compressor
Memory
1
2

FIG. 70

FIG. 71

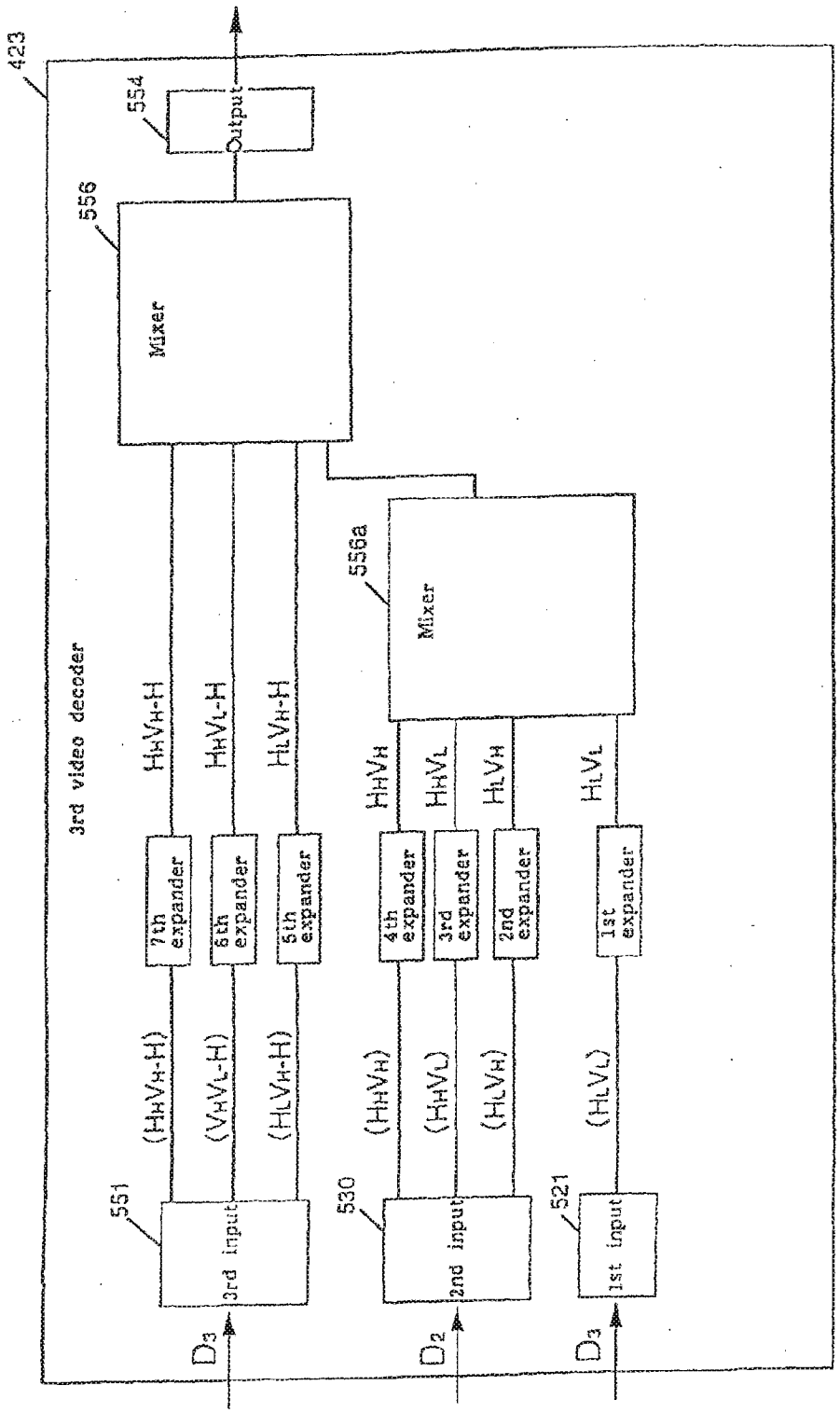


FIG. 72

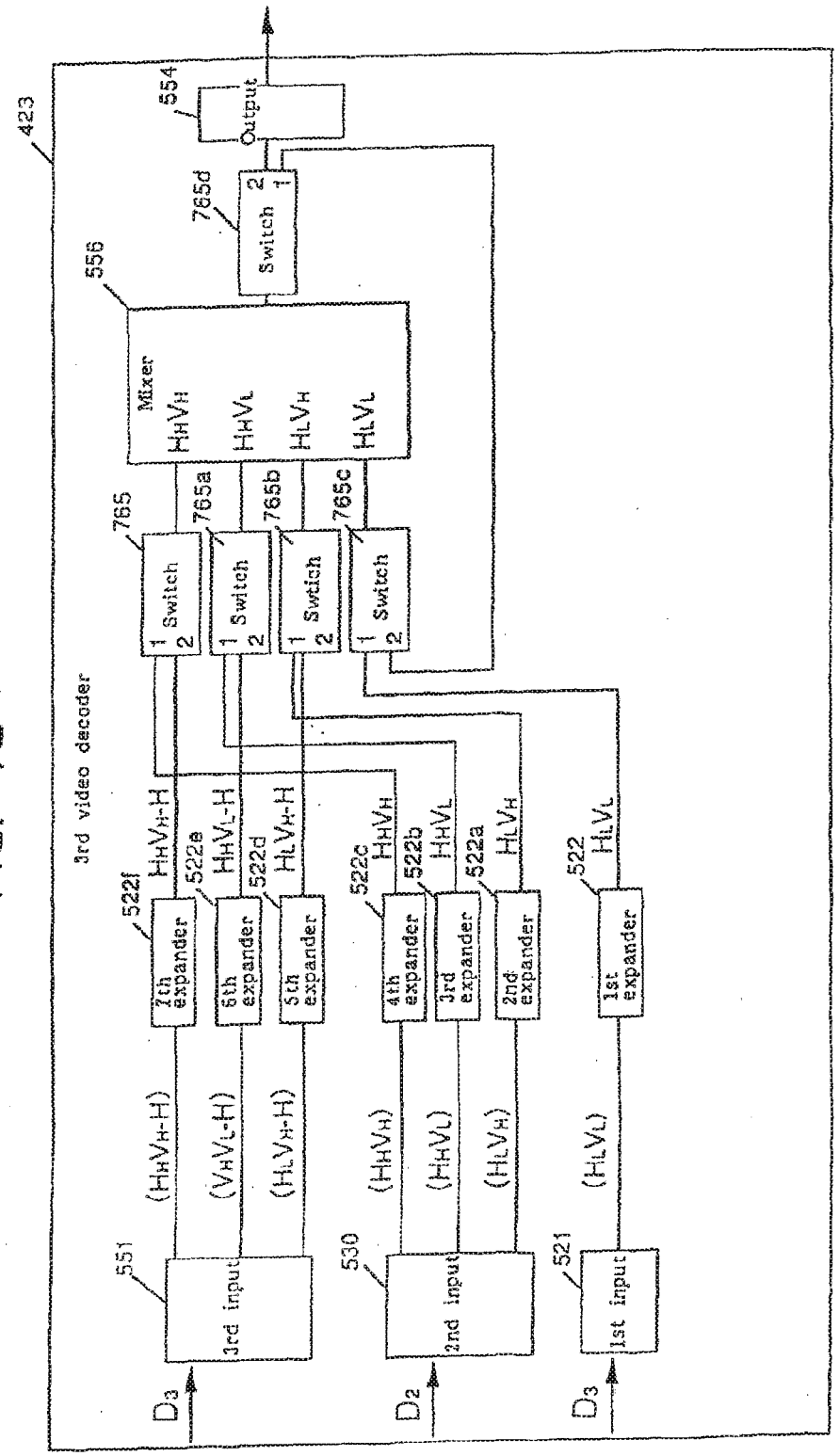


FIG. 73

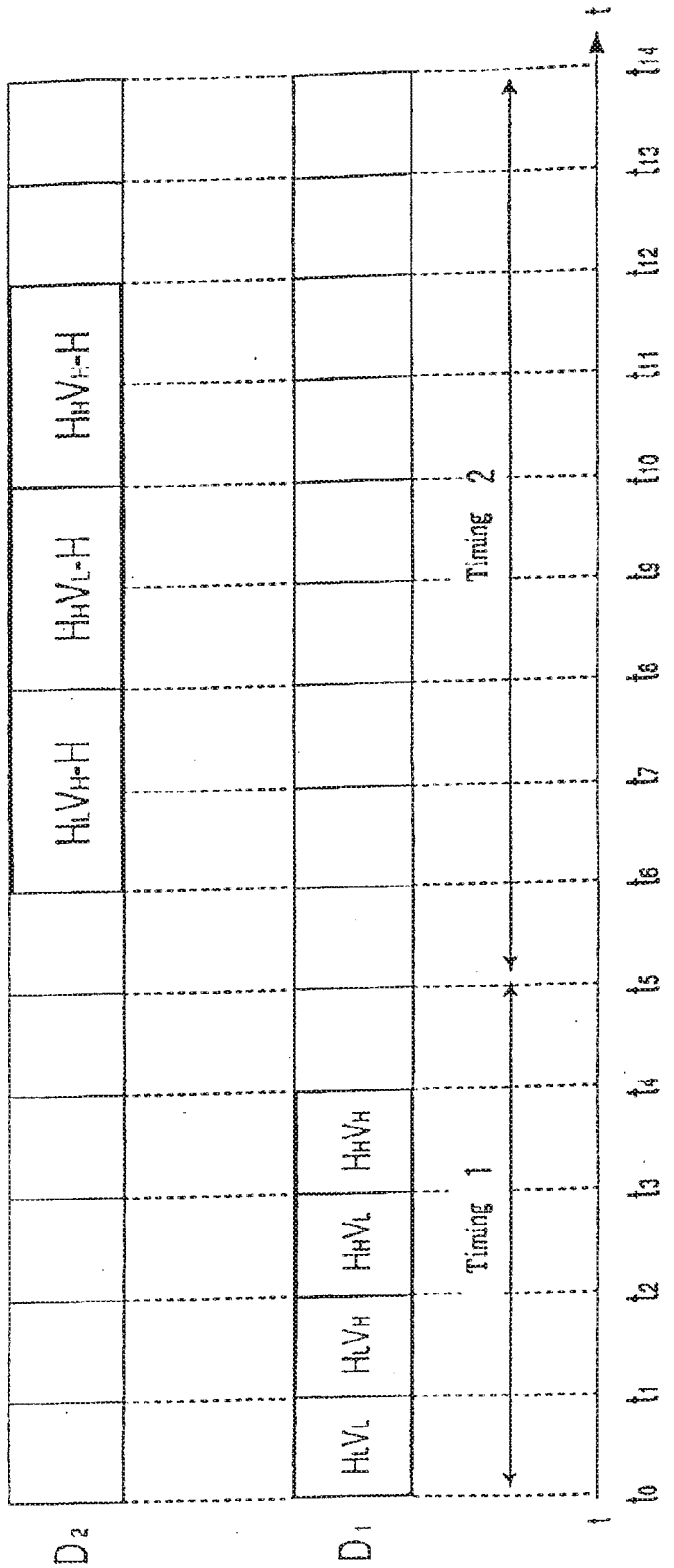


FIG. 74

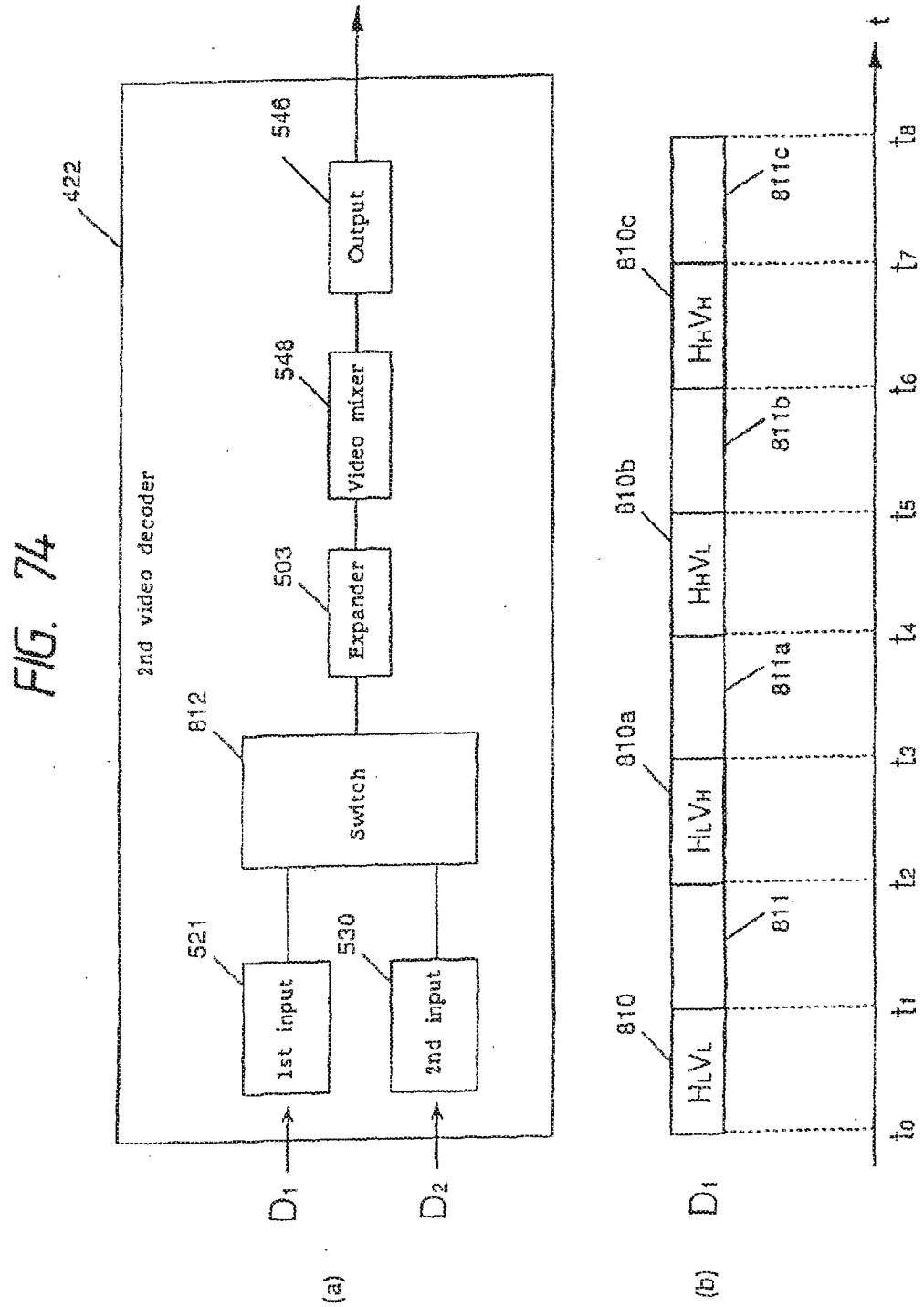


FIG. 75

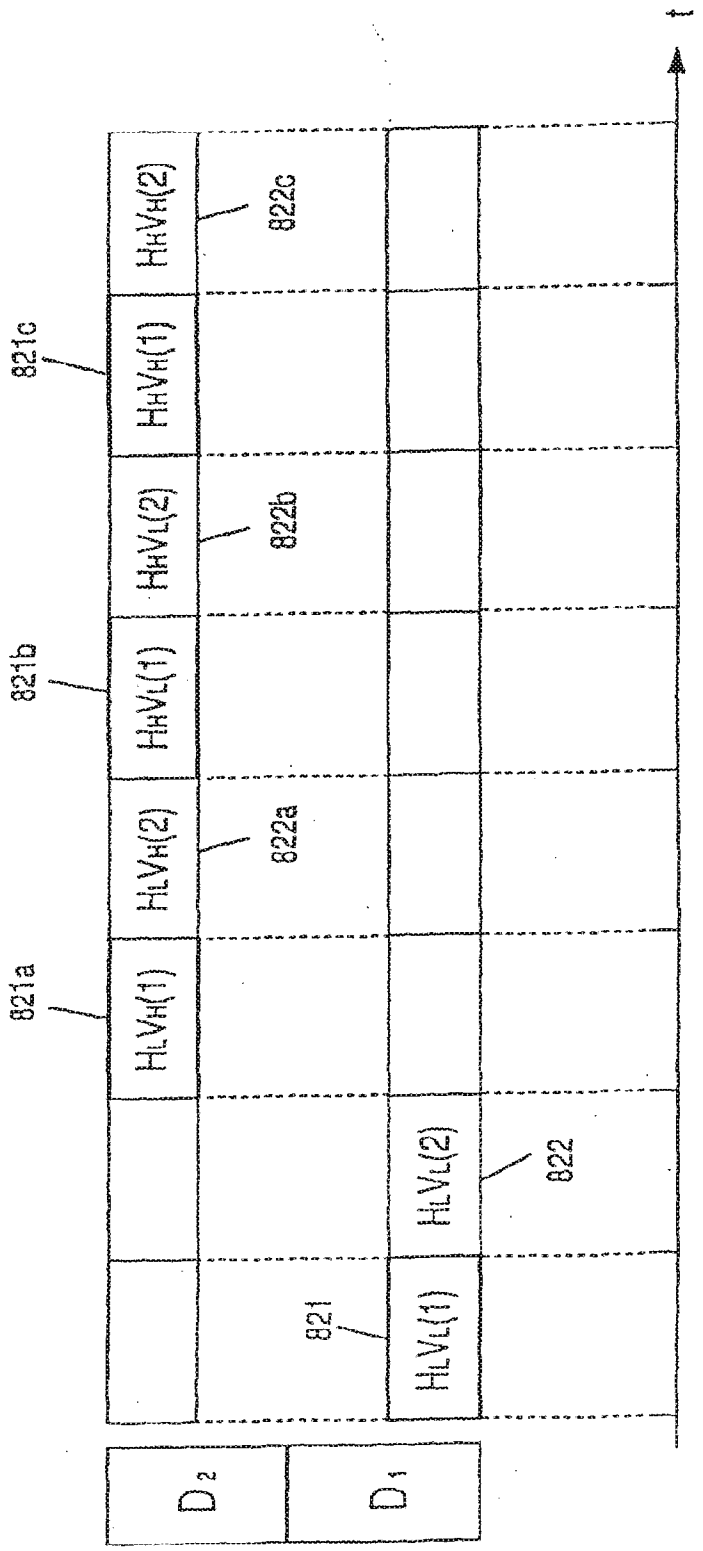


FIG. 76

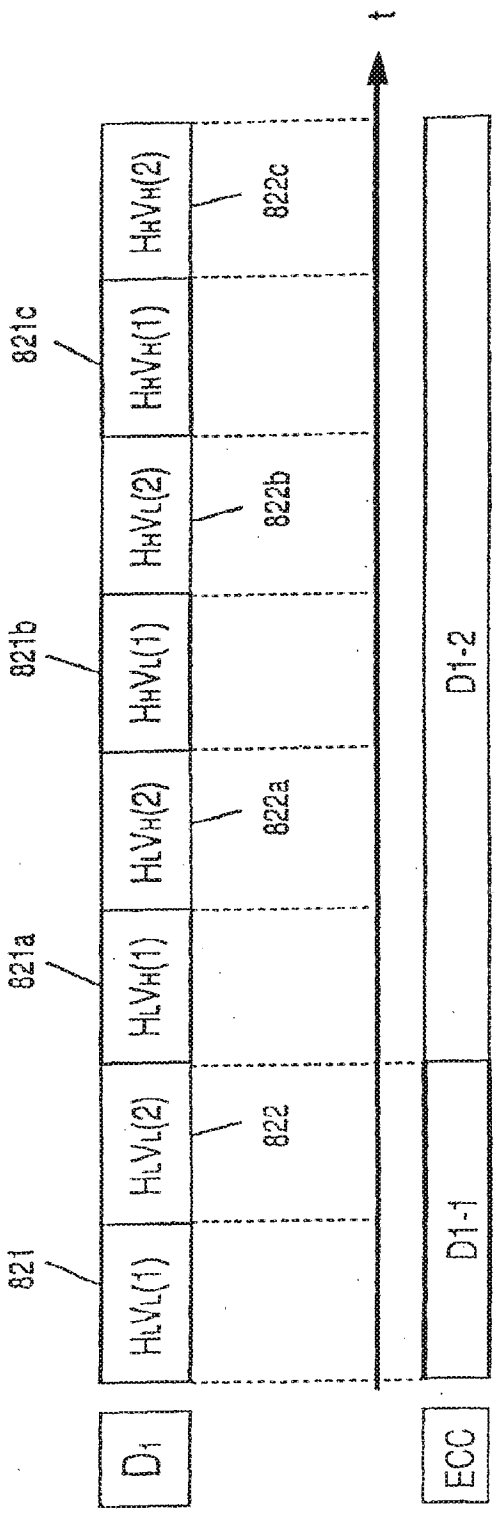


FIG. 77

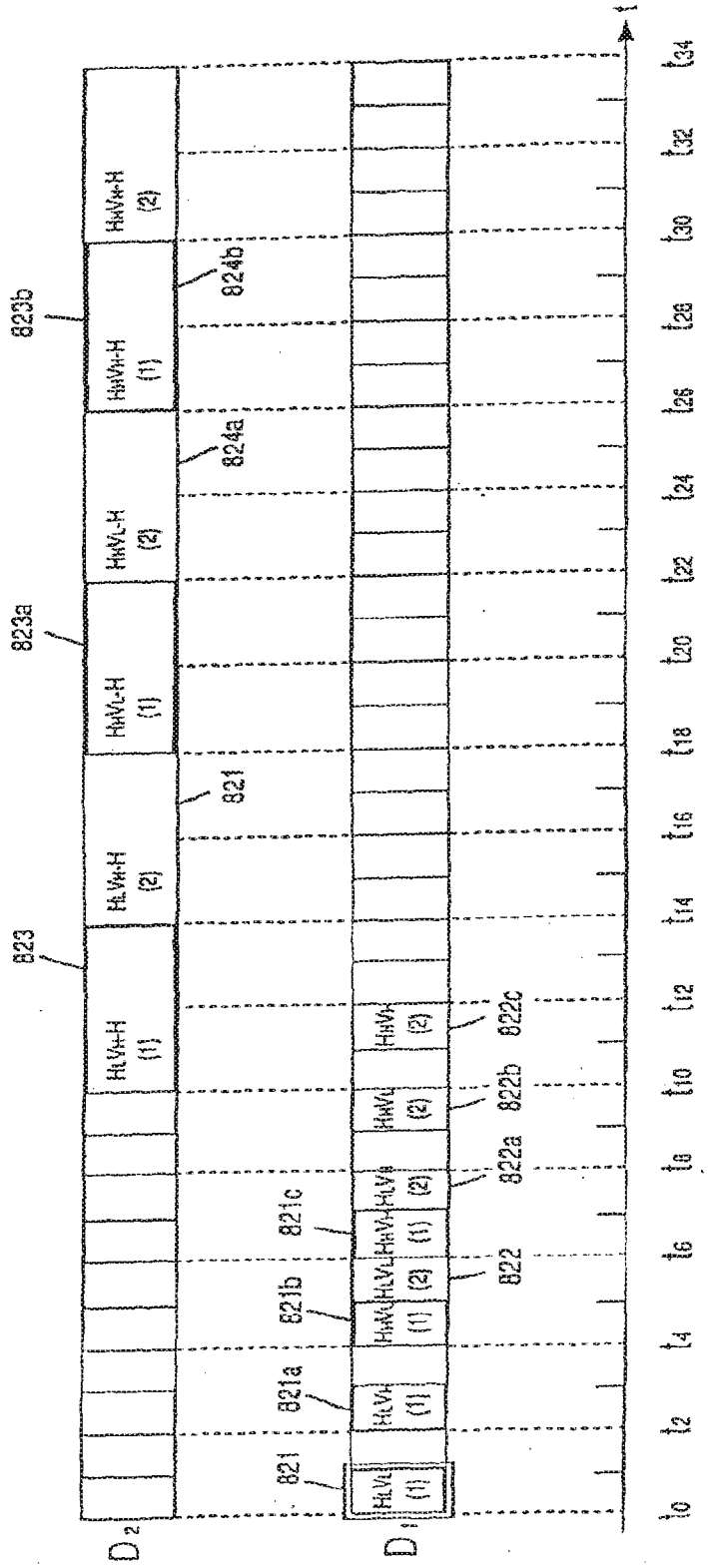


FIG. 78

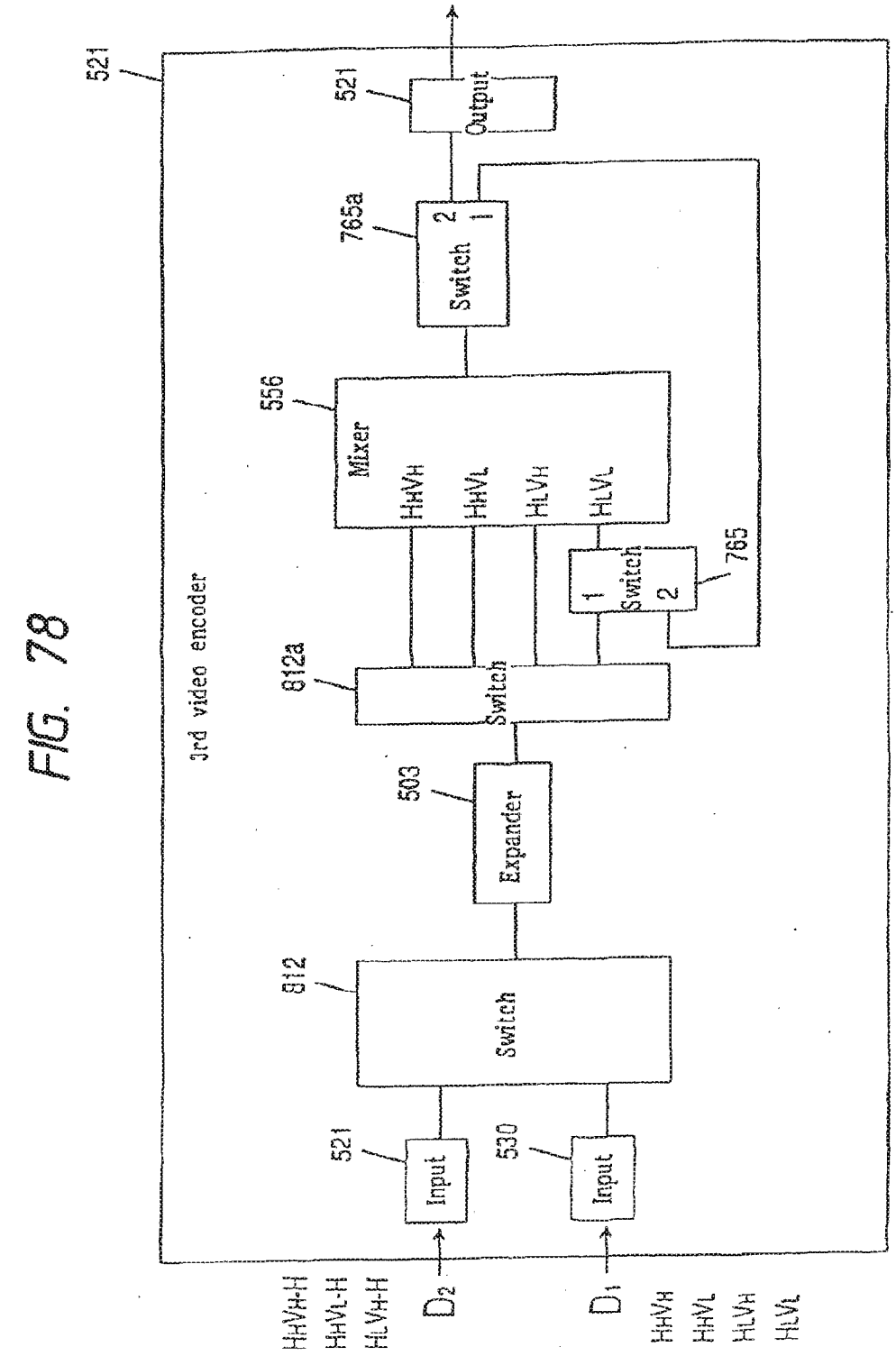


FIG. 79

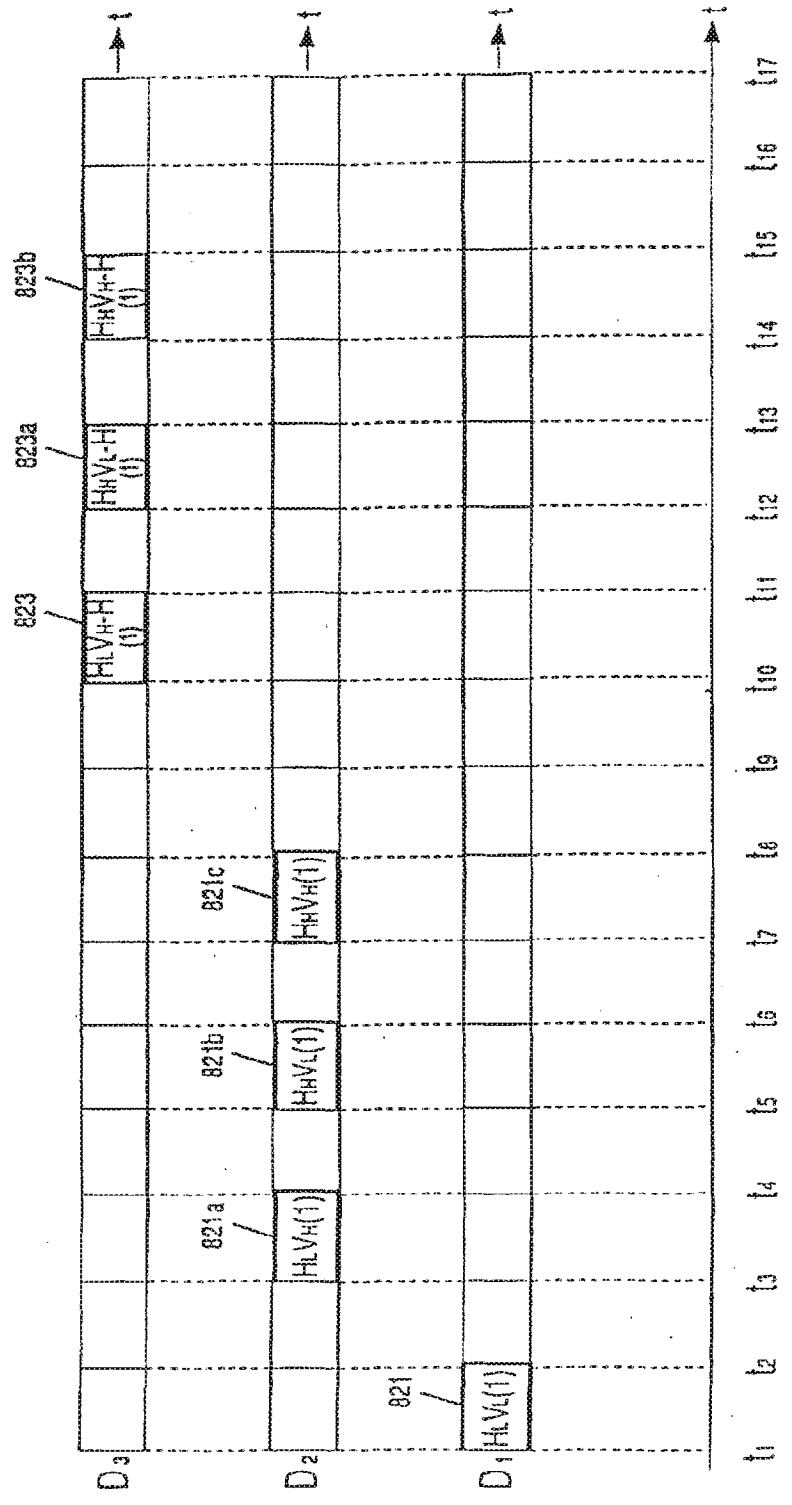


FIG. 80

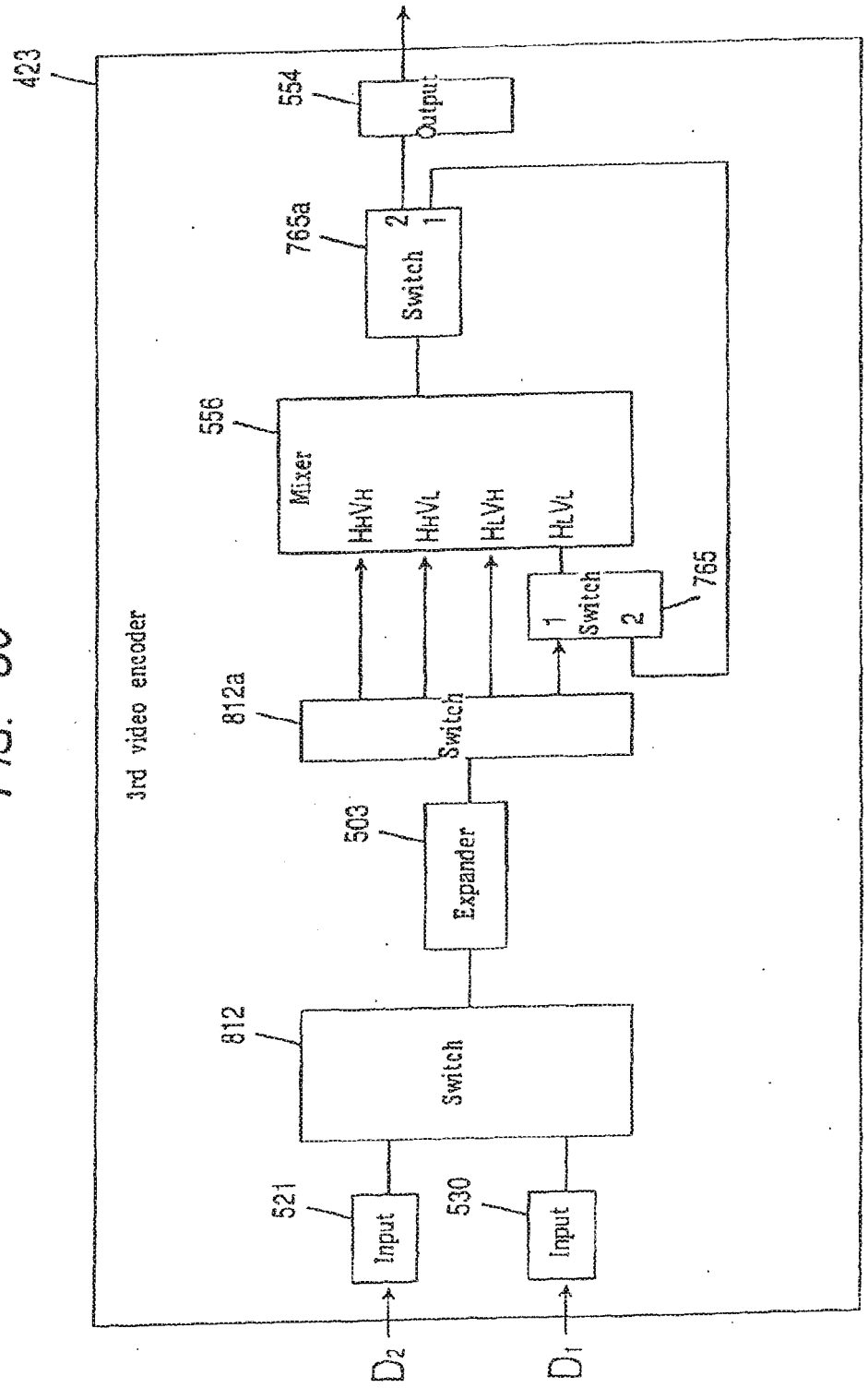

423
3rd video encoder
554
Output
765a
Switch
2
1
556
Mixer
HHVH
HHVL
HLVH
HLVL
765
Switch
1
2
812a
Switch
503
Expander
812
Switch
521
Input
530
Input
D2
D1

FIG. 81

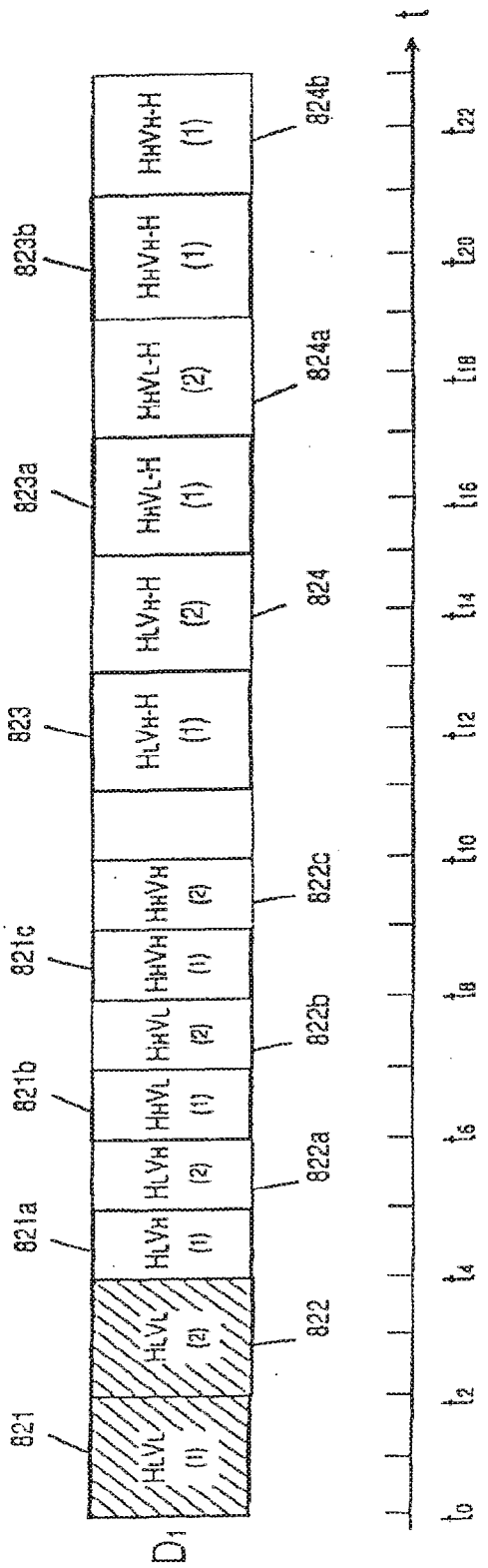


FIG. 82

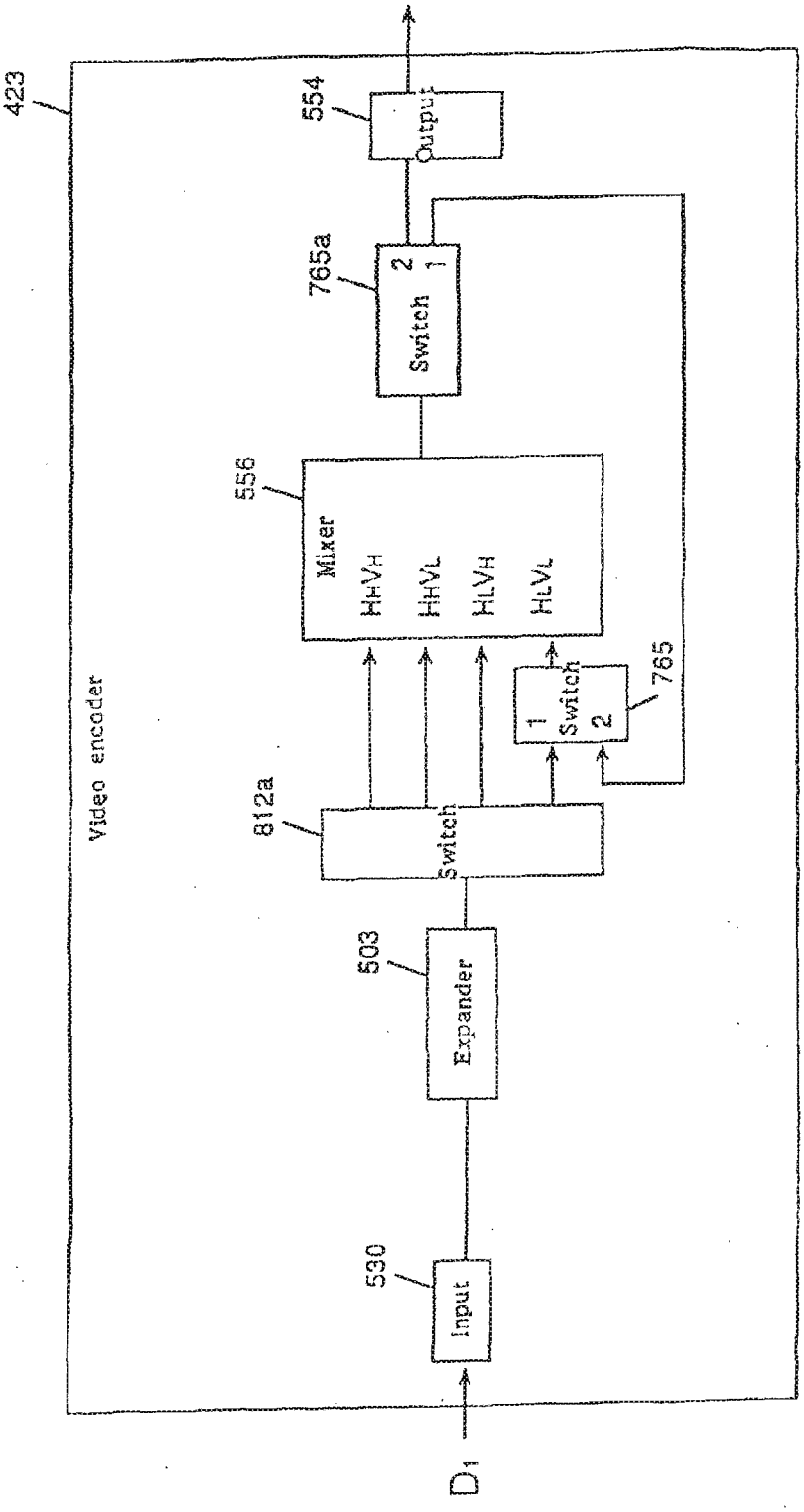


FIG. 83

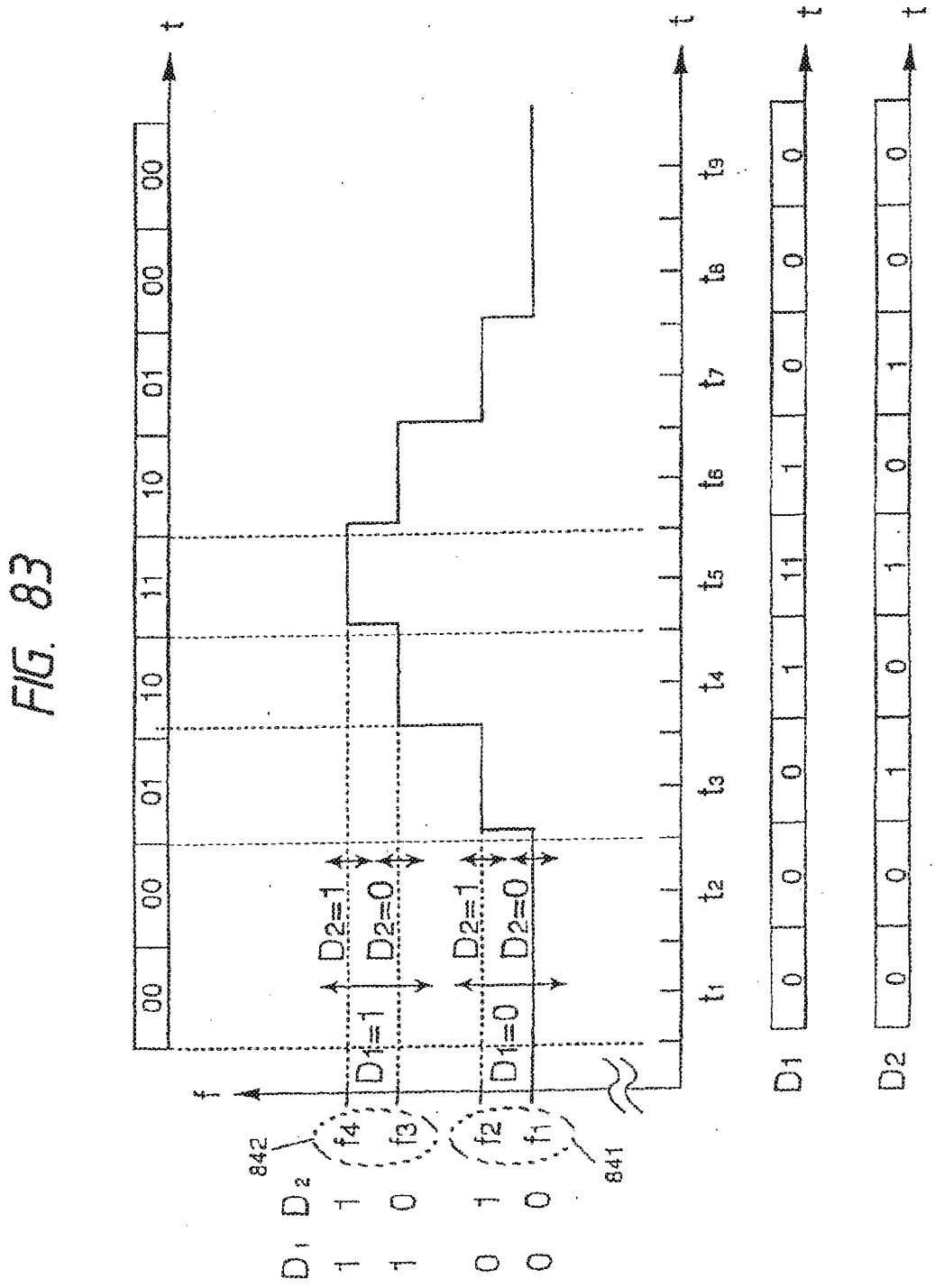

t
00
01
10
11
D2=1
D2=0
D1=1
D1=0
f4
f3
f2
f1
842
841
D2
D1
t1
t2
t3
t4
t5
t6
t7
t8
t9

FIG. 84

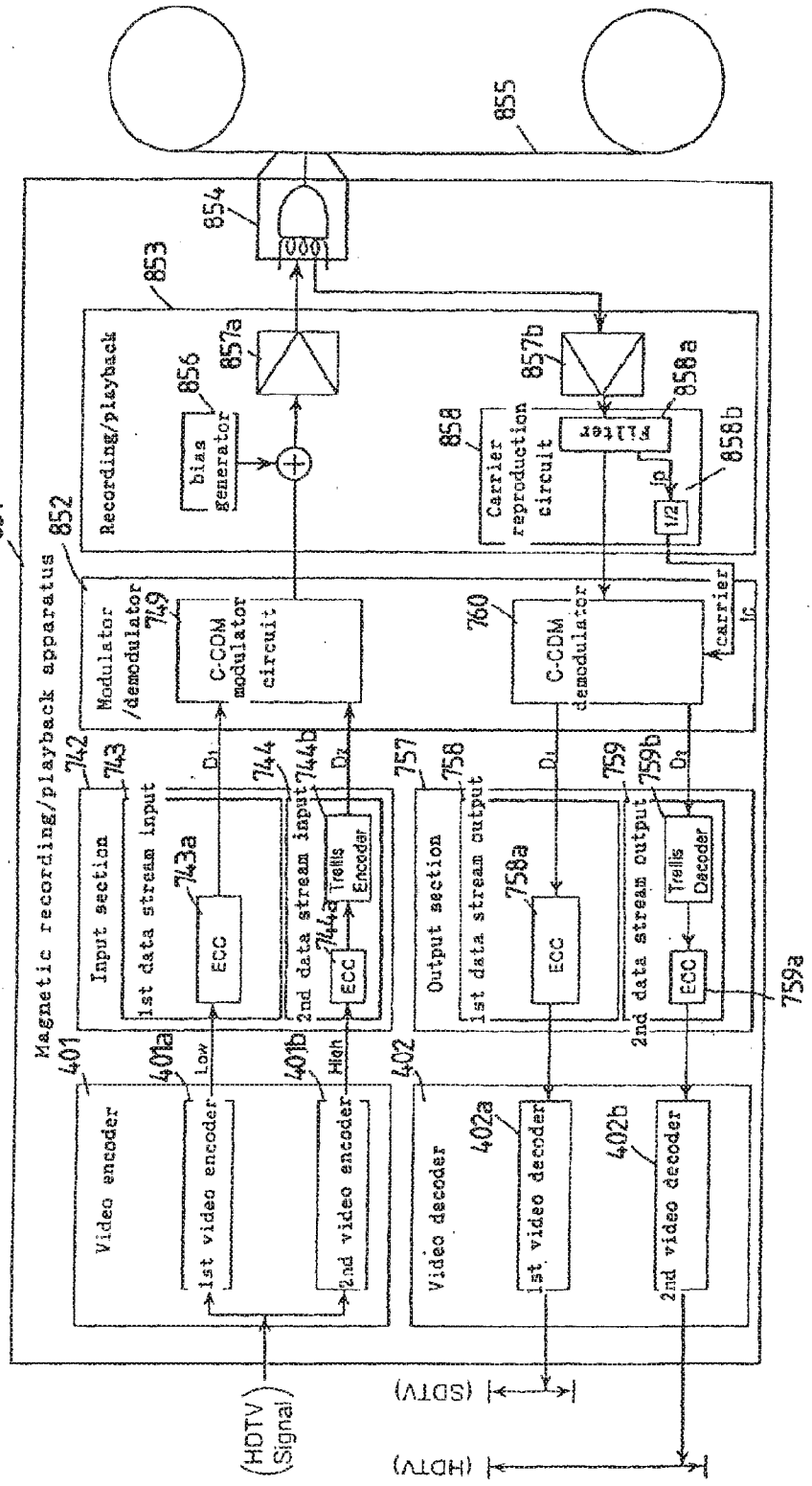


FIG. 85

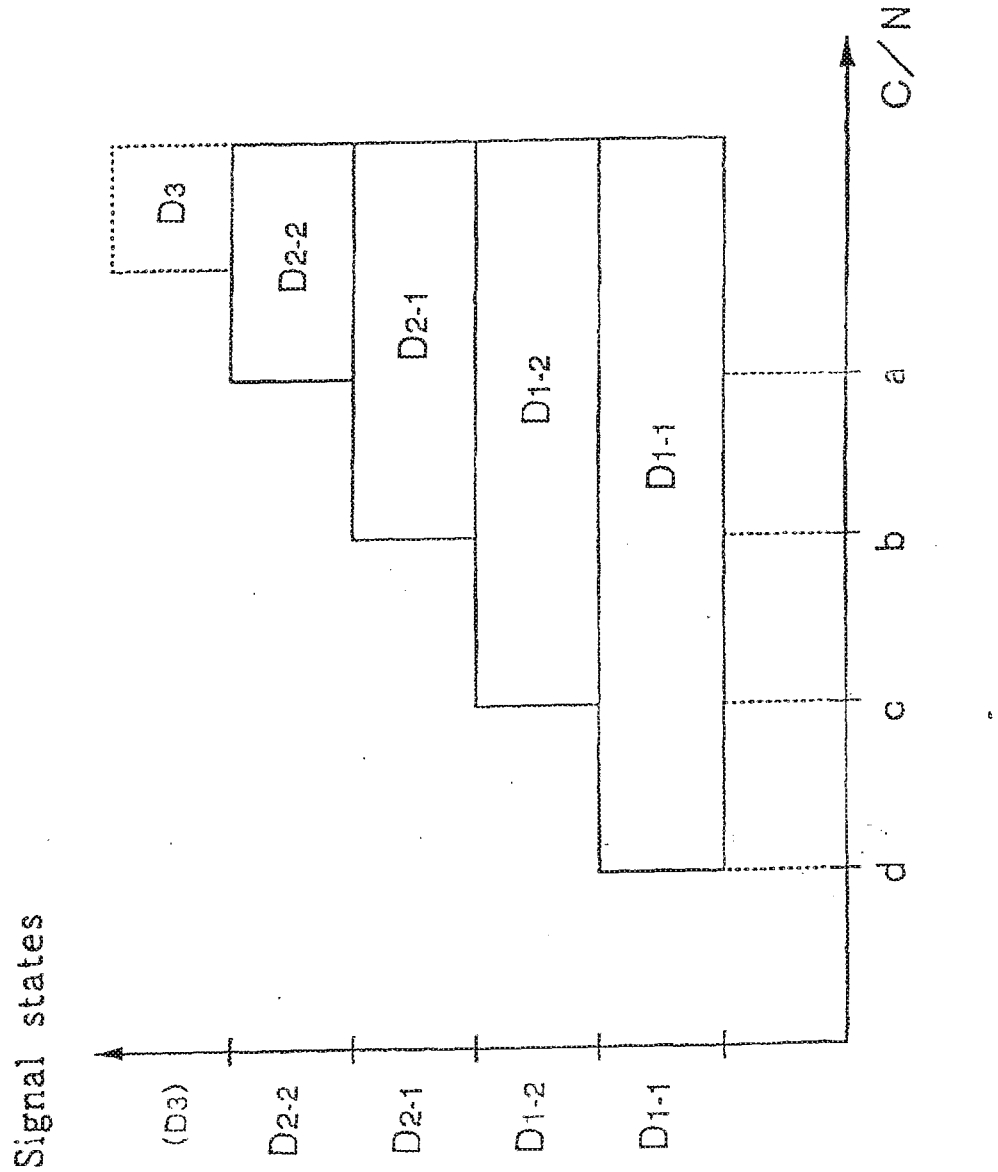


FIG. 86

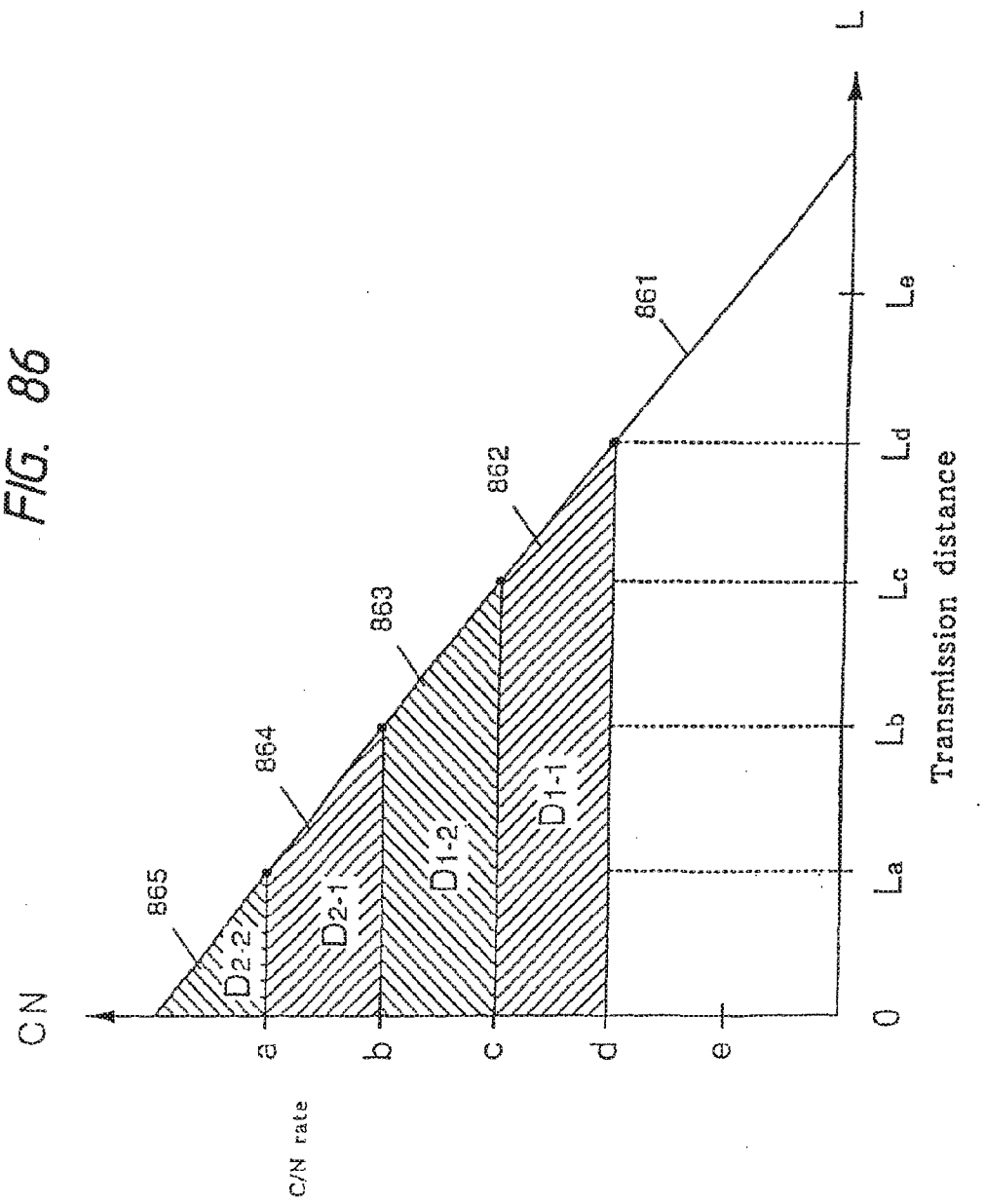


FIG. 87

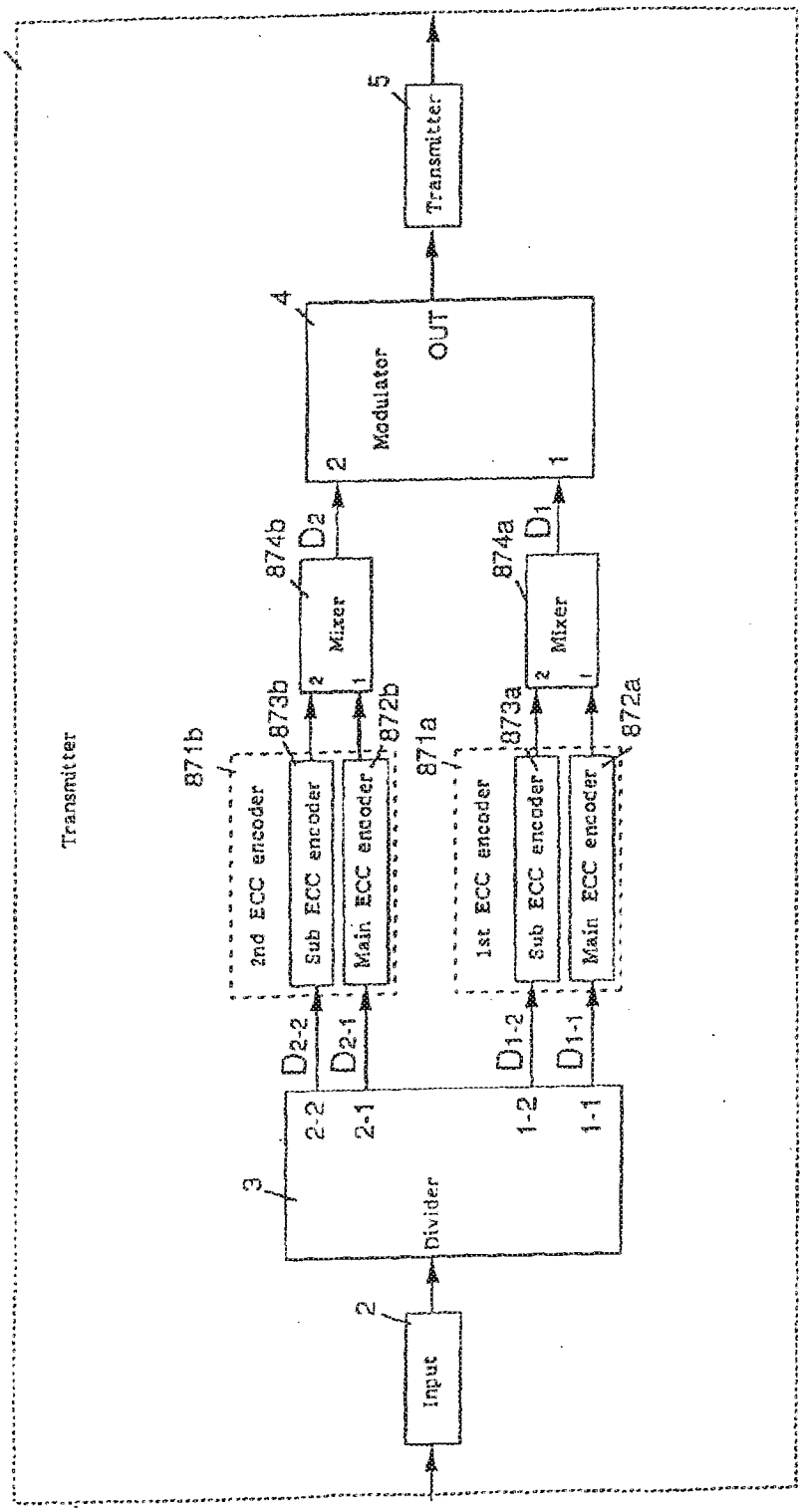


FIG. 88

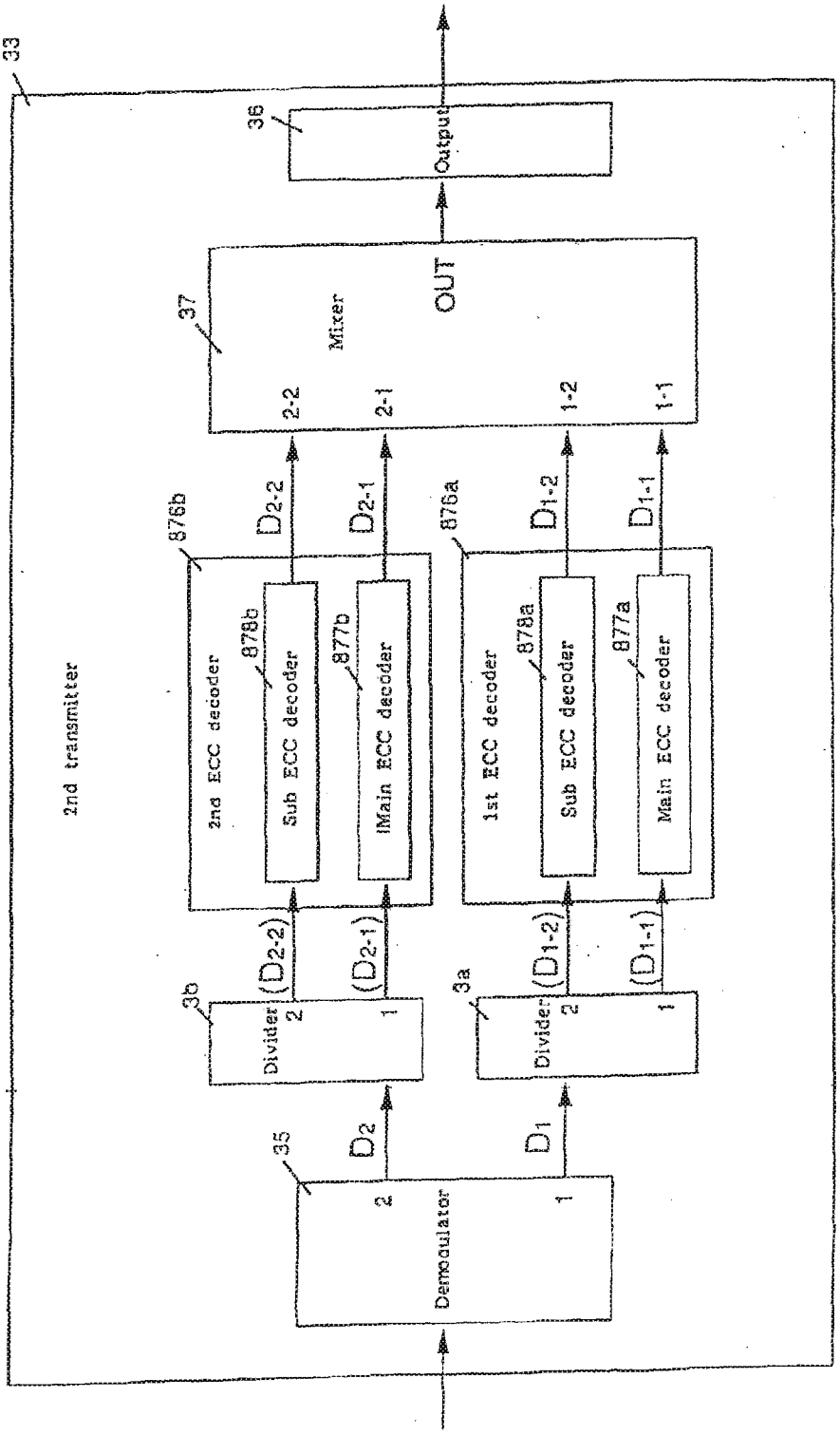
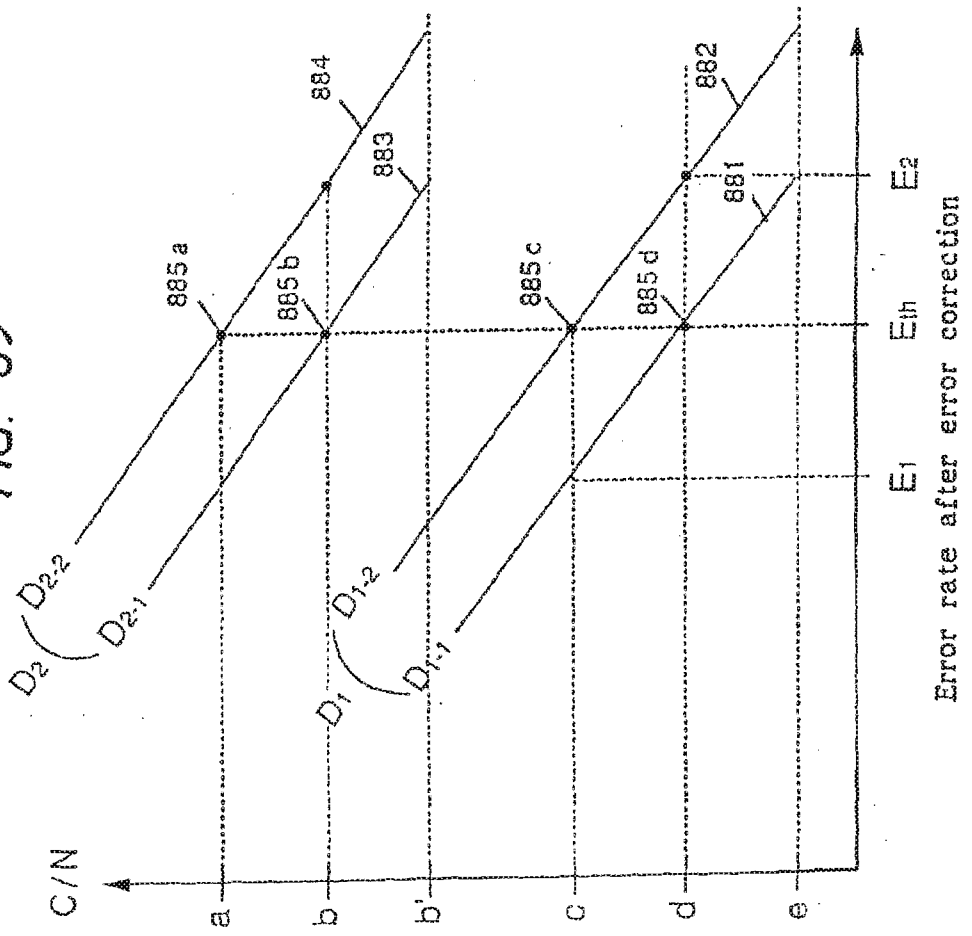


FIG. 89



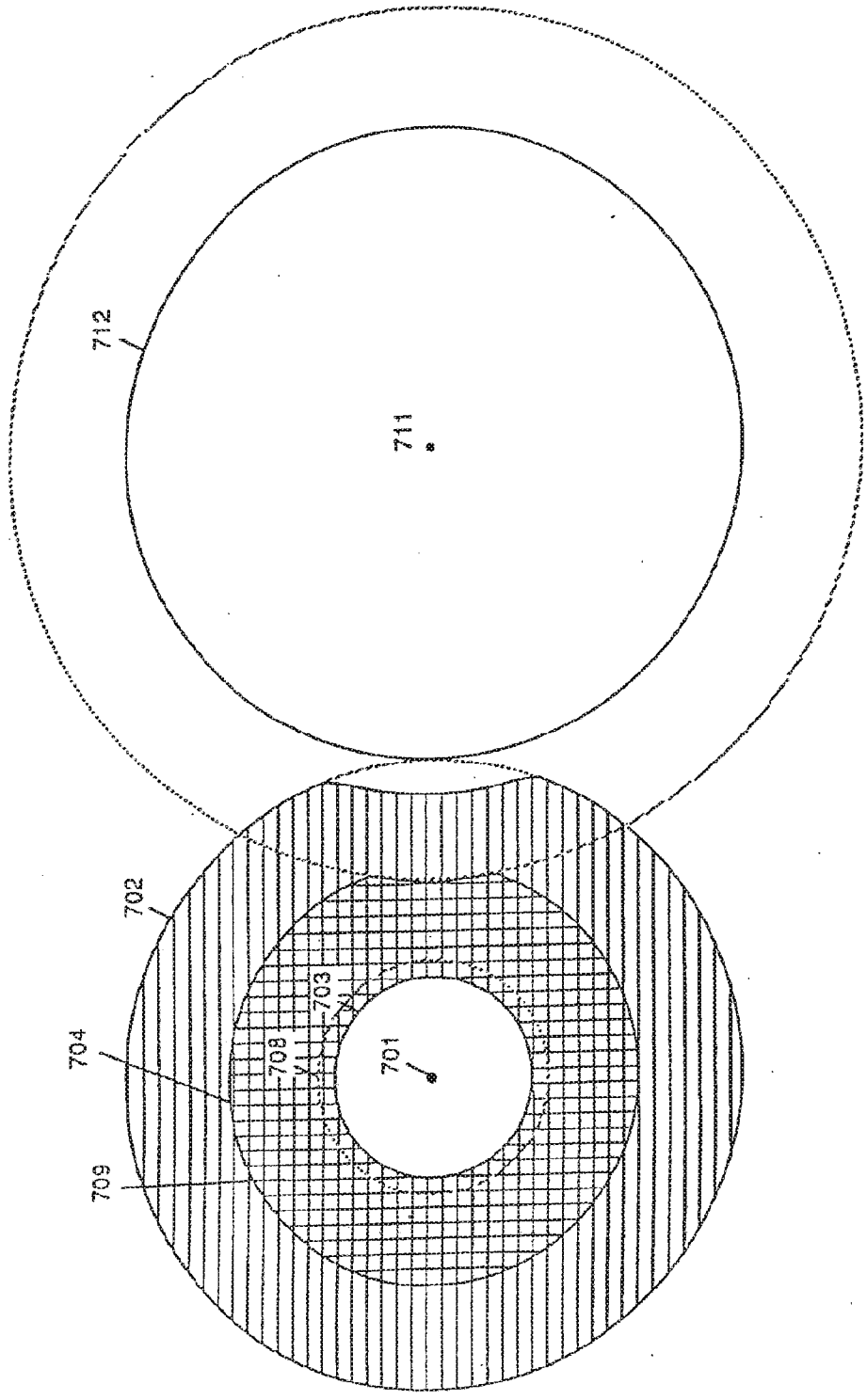


FIG. 90

FIG. 91

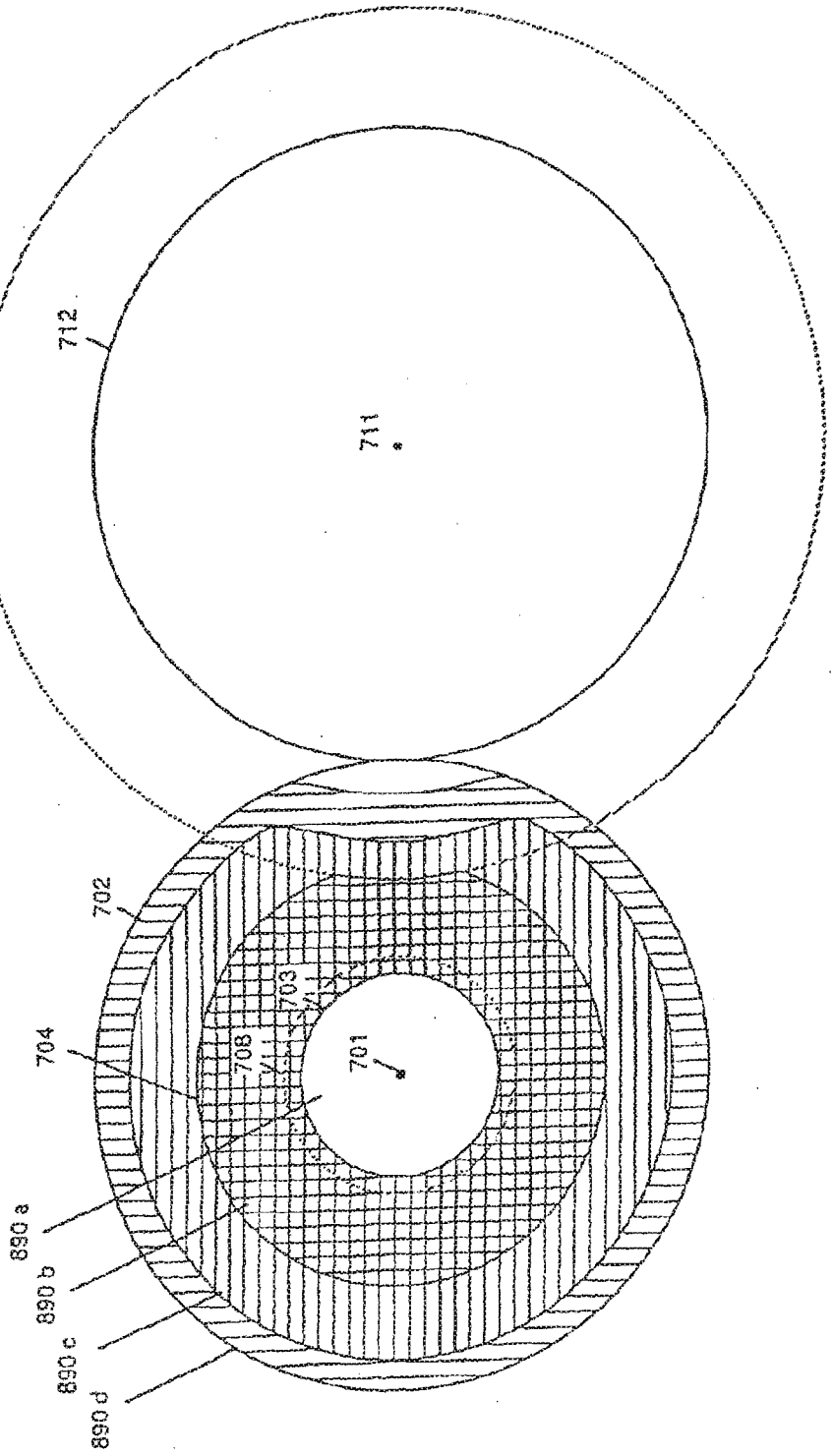


FIG. 92

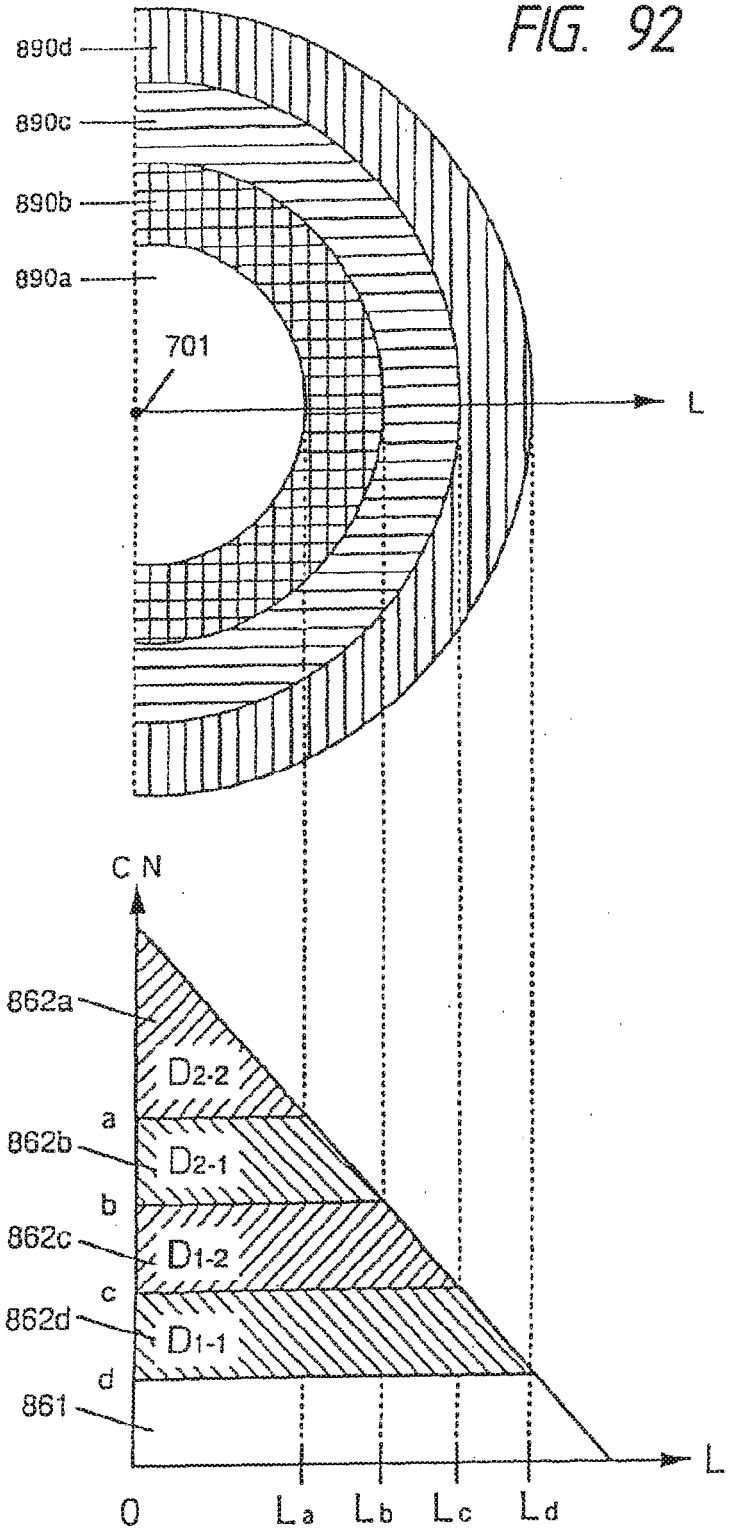


FIG. 93

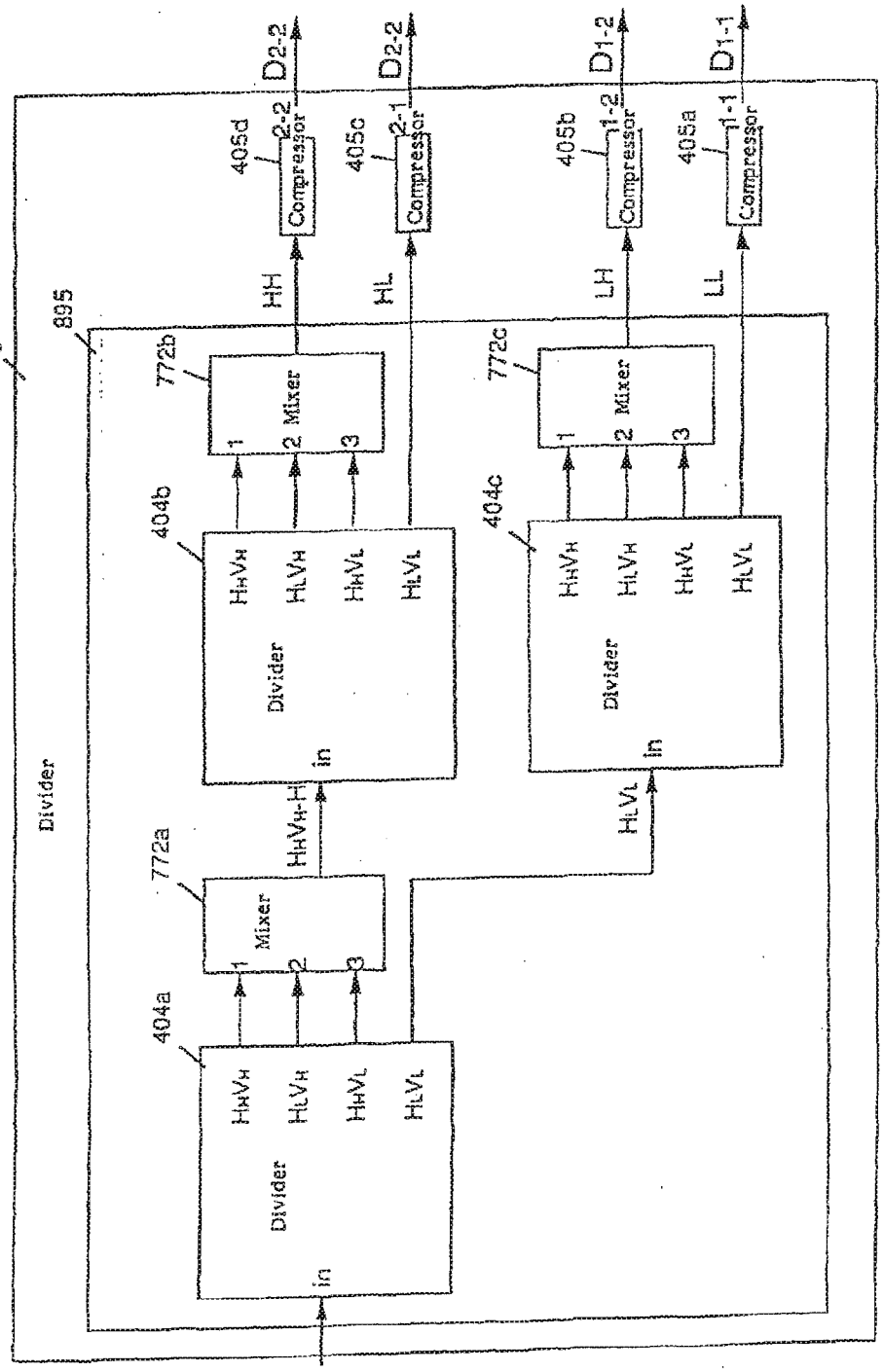

3
Divider
895
D2-2
D2-2
D1-2
D1-1
405d
2-2
Compressor
405c
2-1
Compressor
405b
1-2
Compressor
405a
1-1
Compressor
HH
HL
LH
LL
772b
772c
772a
Mixer
1
2
3
404b
404c
404a
HHVH
HLVH
HHVL
HLVL
Divider
in
HHVH-H
HLVL

FIG. 94

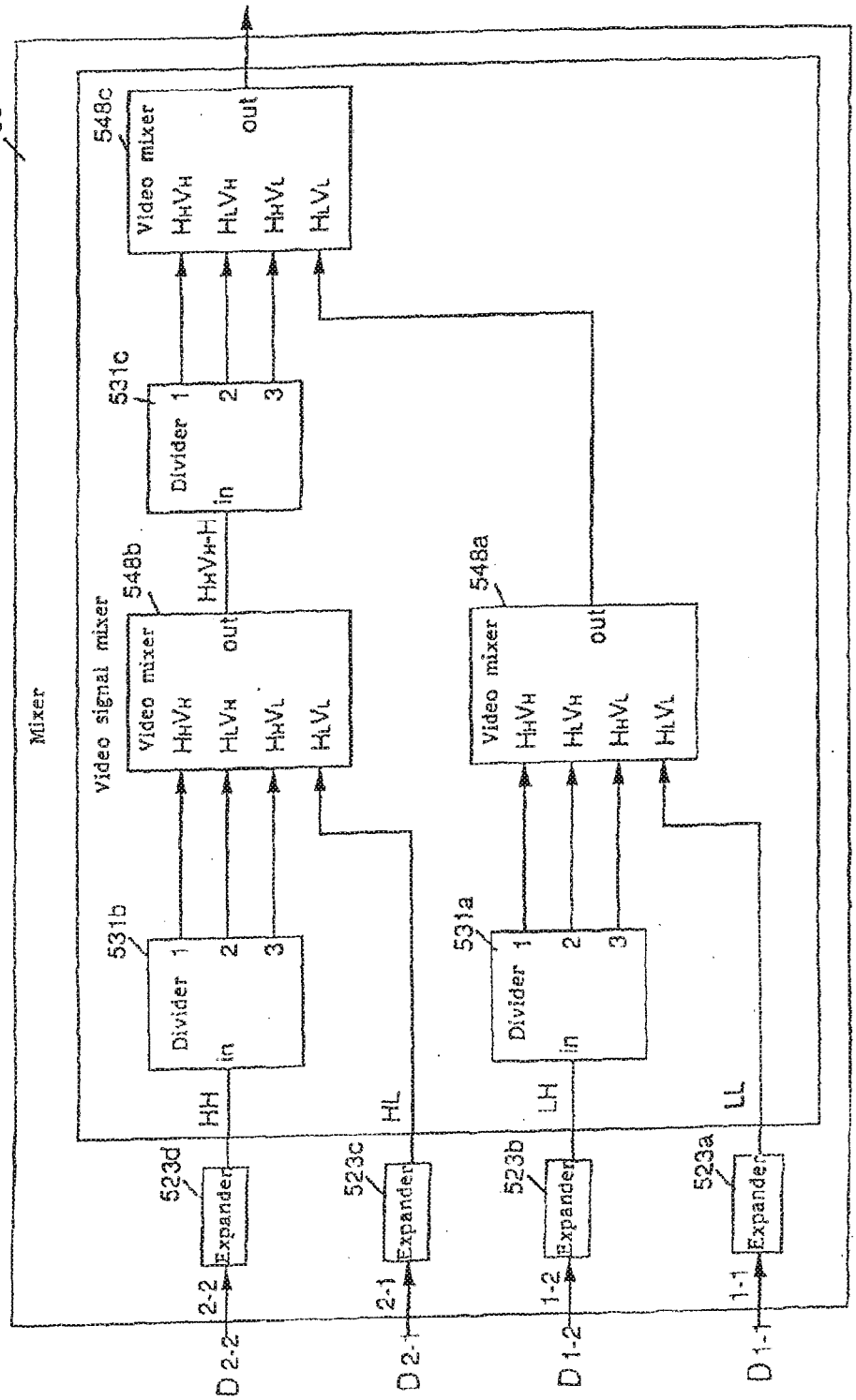
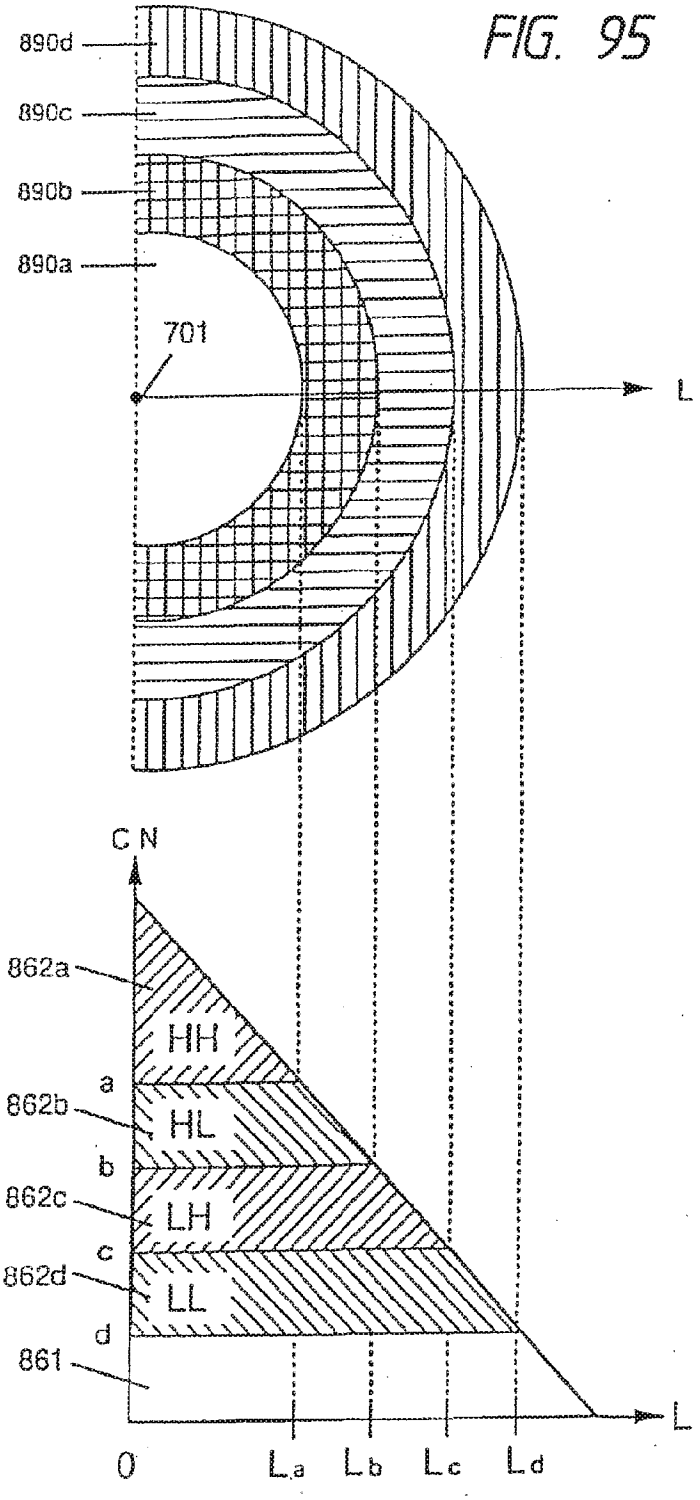

33
Mixer
Video signal mixer
548c
Video mixer
HHVH
HLVH
HHVL
HLVL
out
531c
Divider
1
2
3
in
HHVH-H
548b
548a
531b
531a
HH
HL
LH
LL
523d
523c
523b
523a
Expander
2-2
2-1
1-2
1-1
D 2-2
D 2-1
D 1-2
D 1-1

FIG. 95



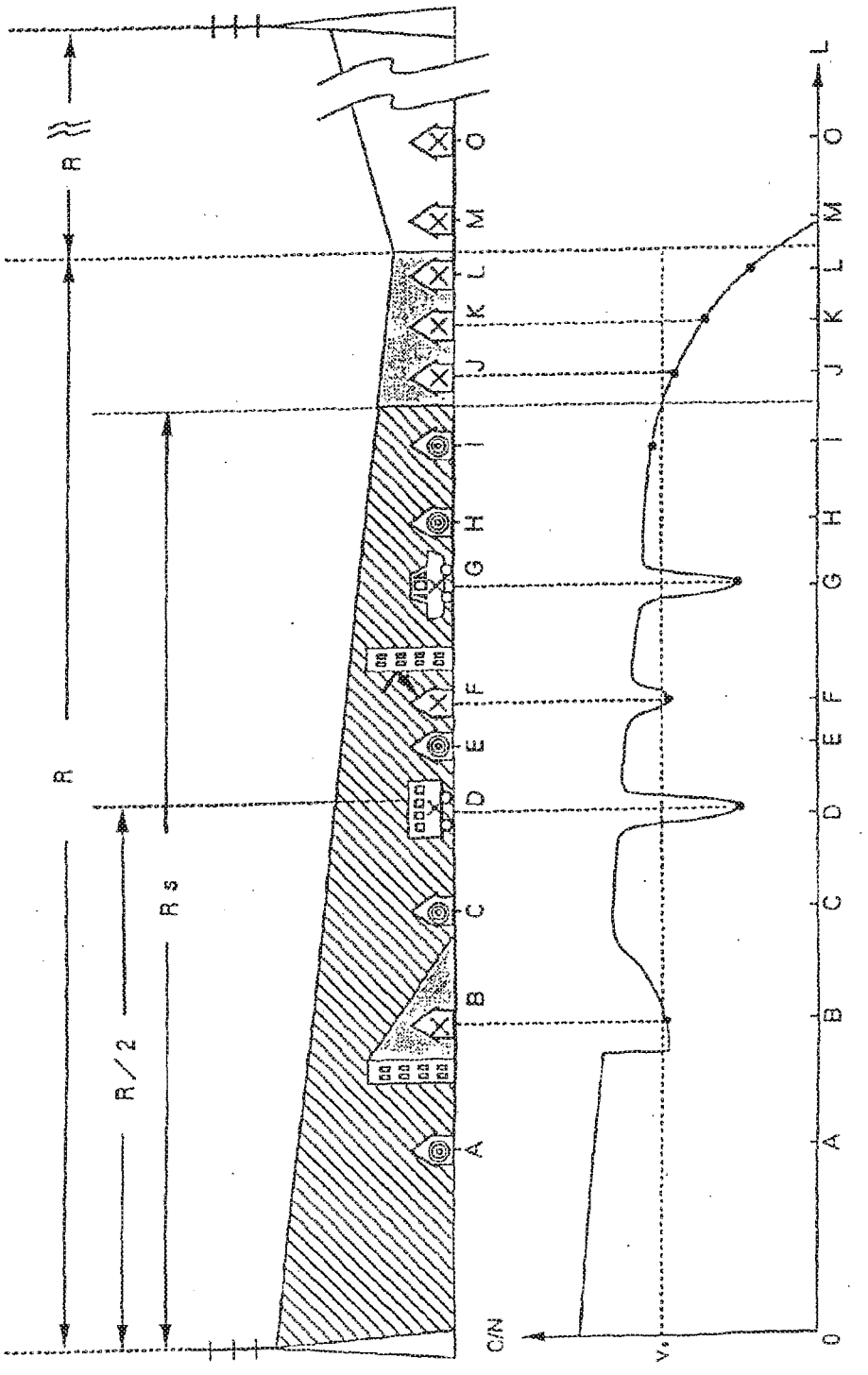


FIG. 96

FIG. 97

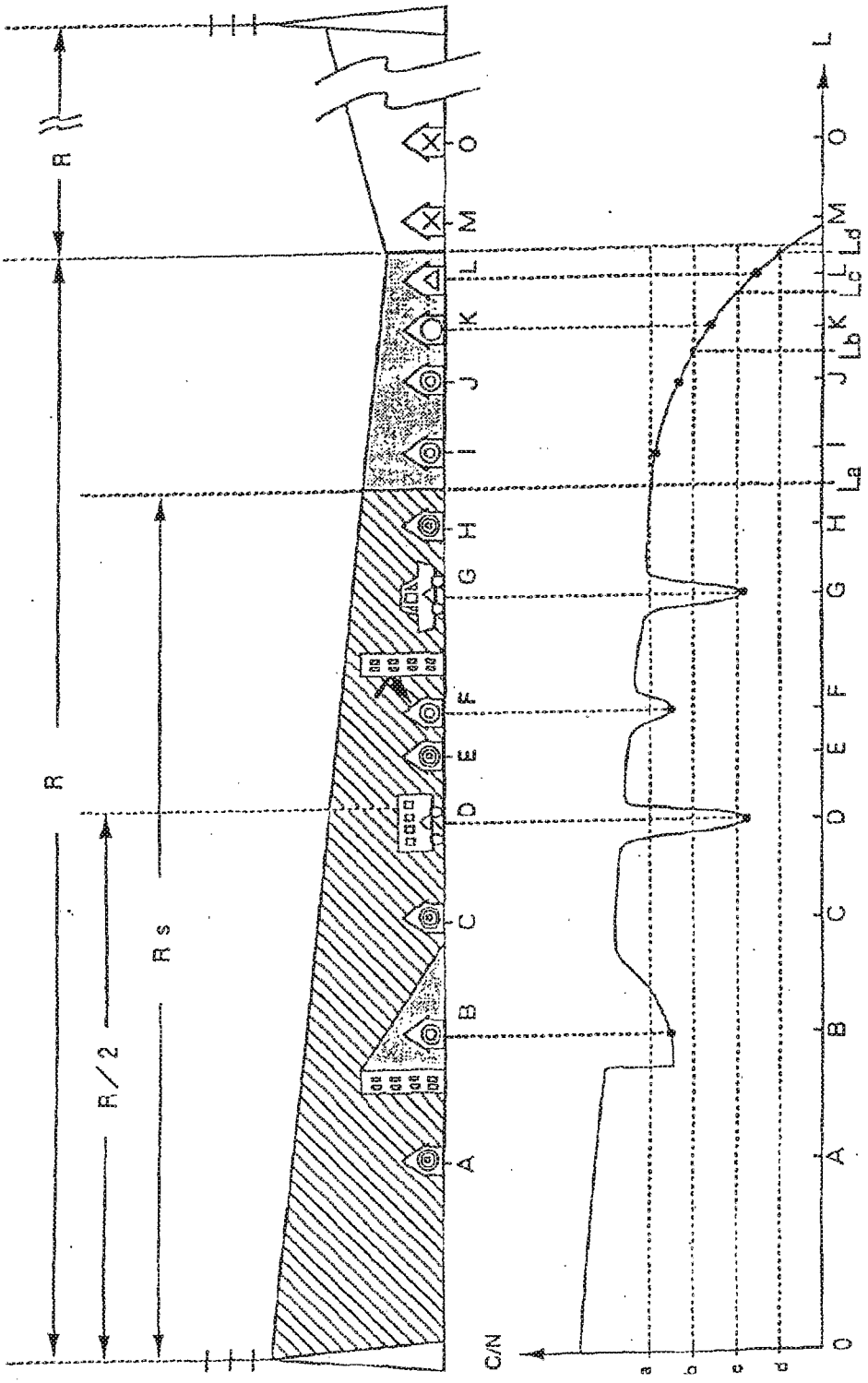
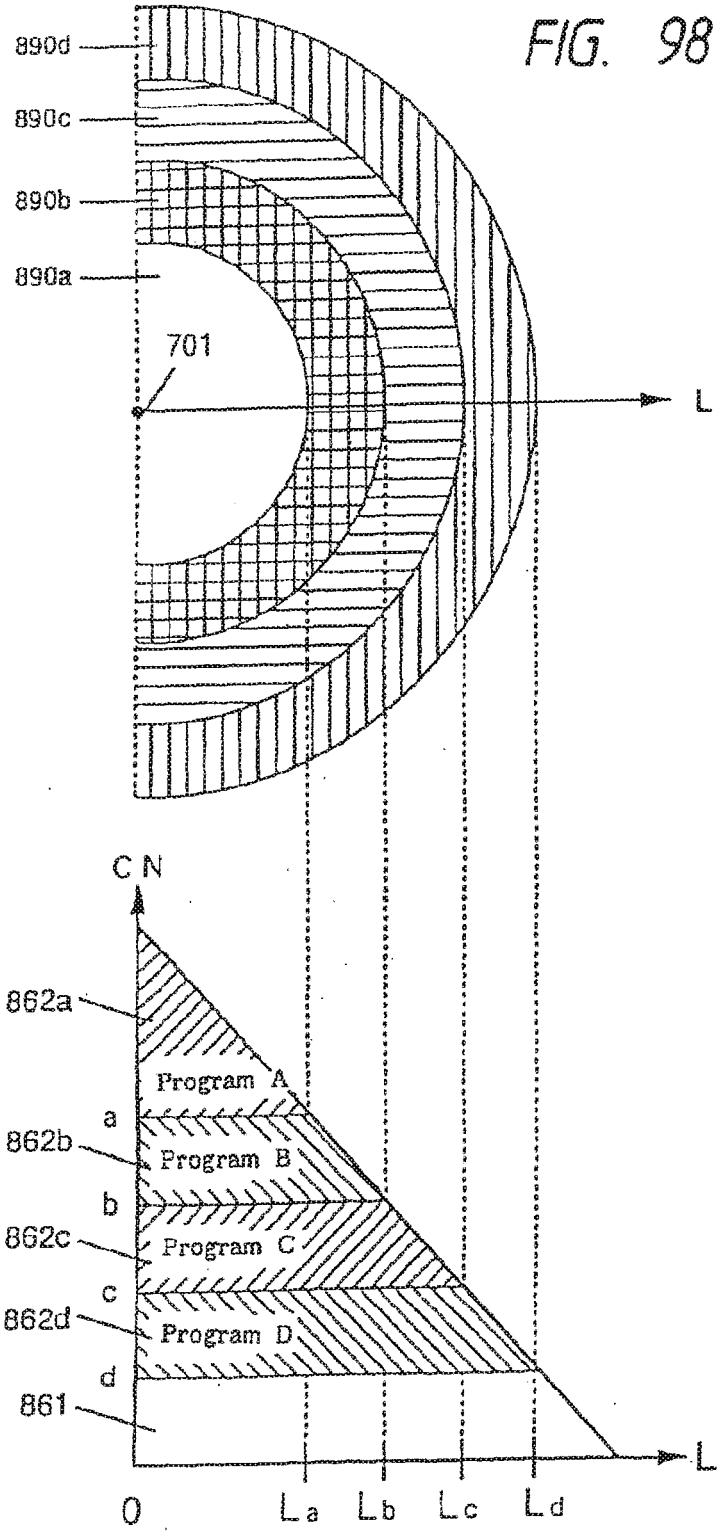


FIG. 98



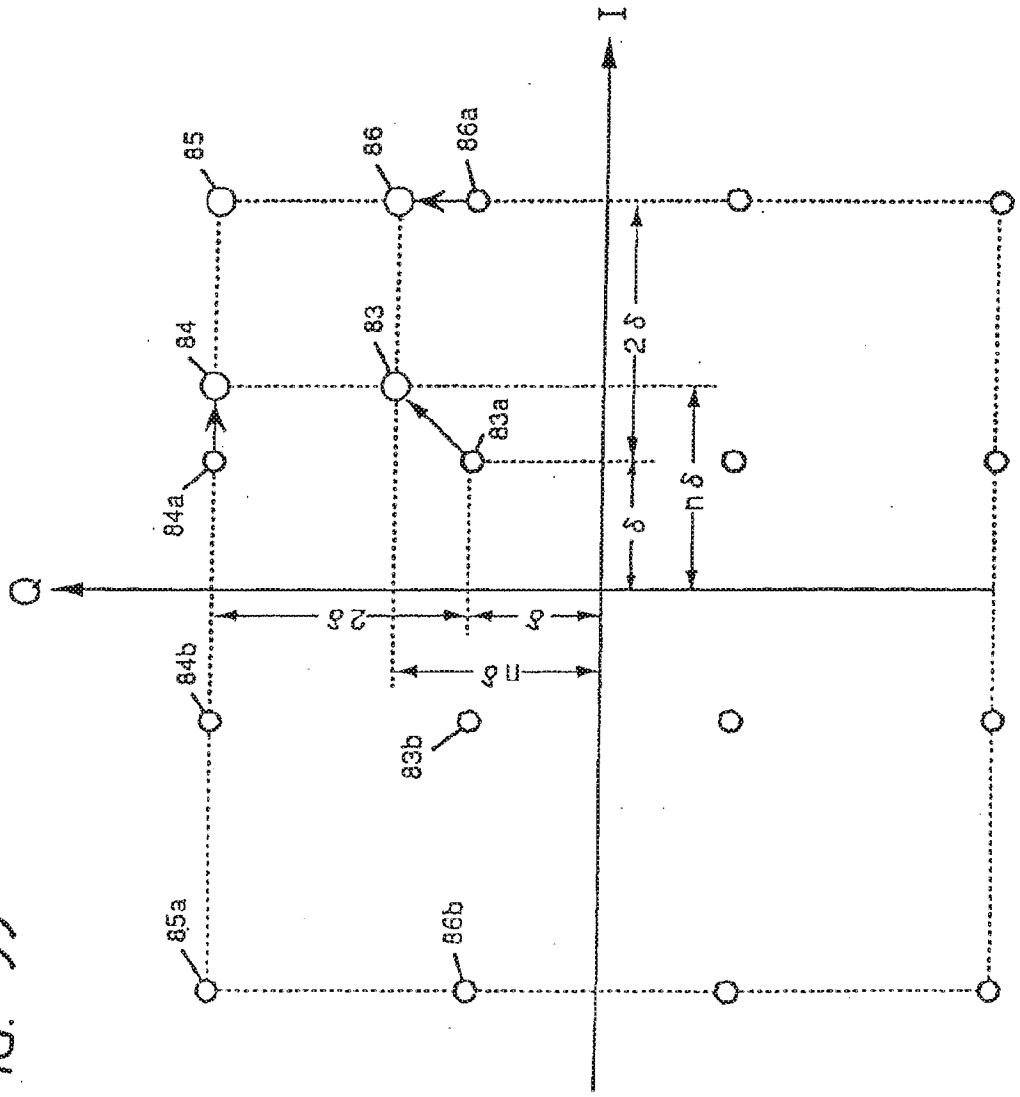


FIG. 99

FIG. 100

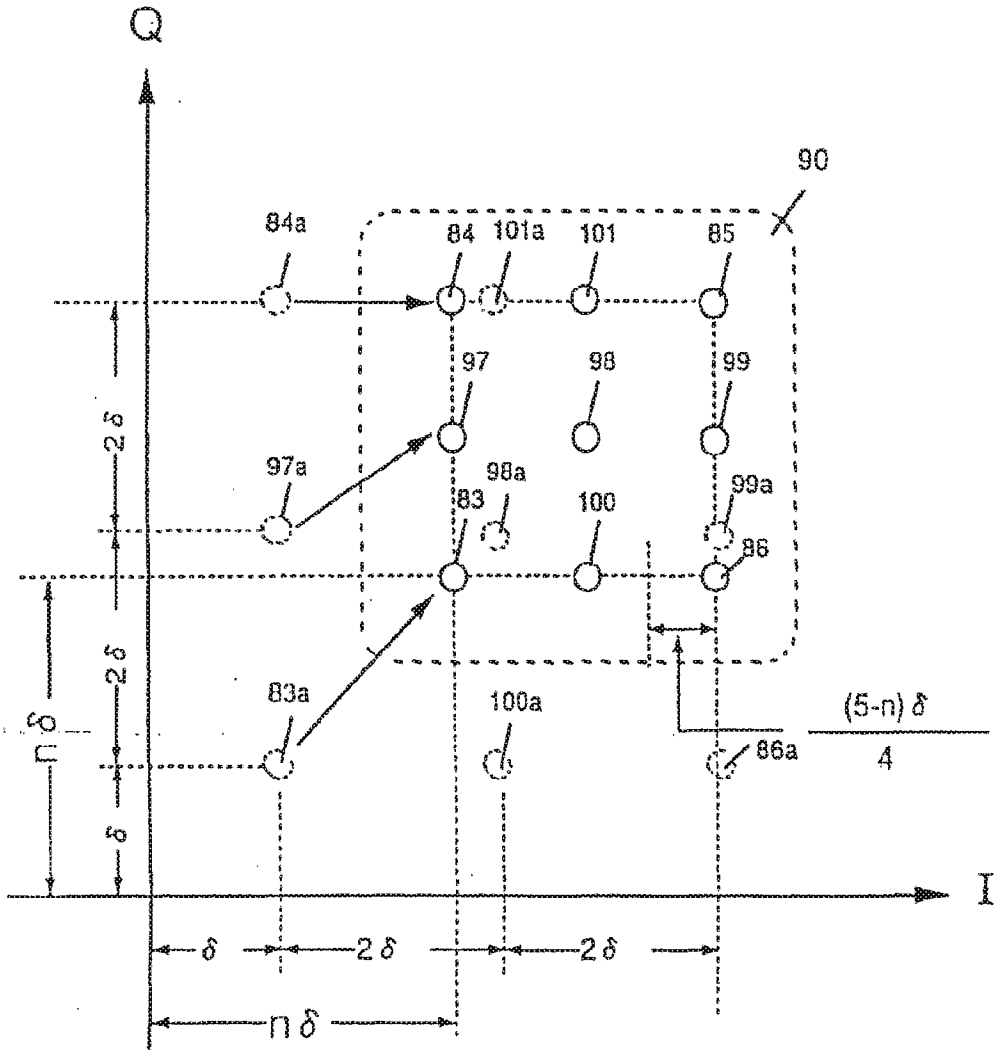


FIG. 101

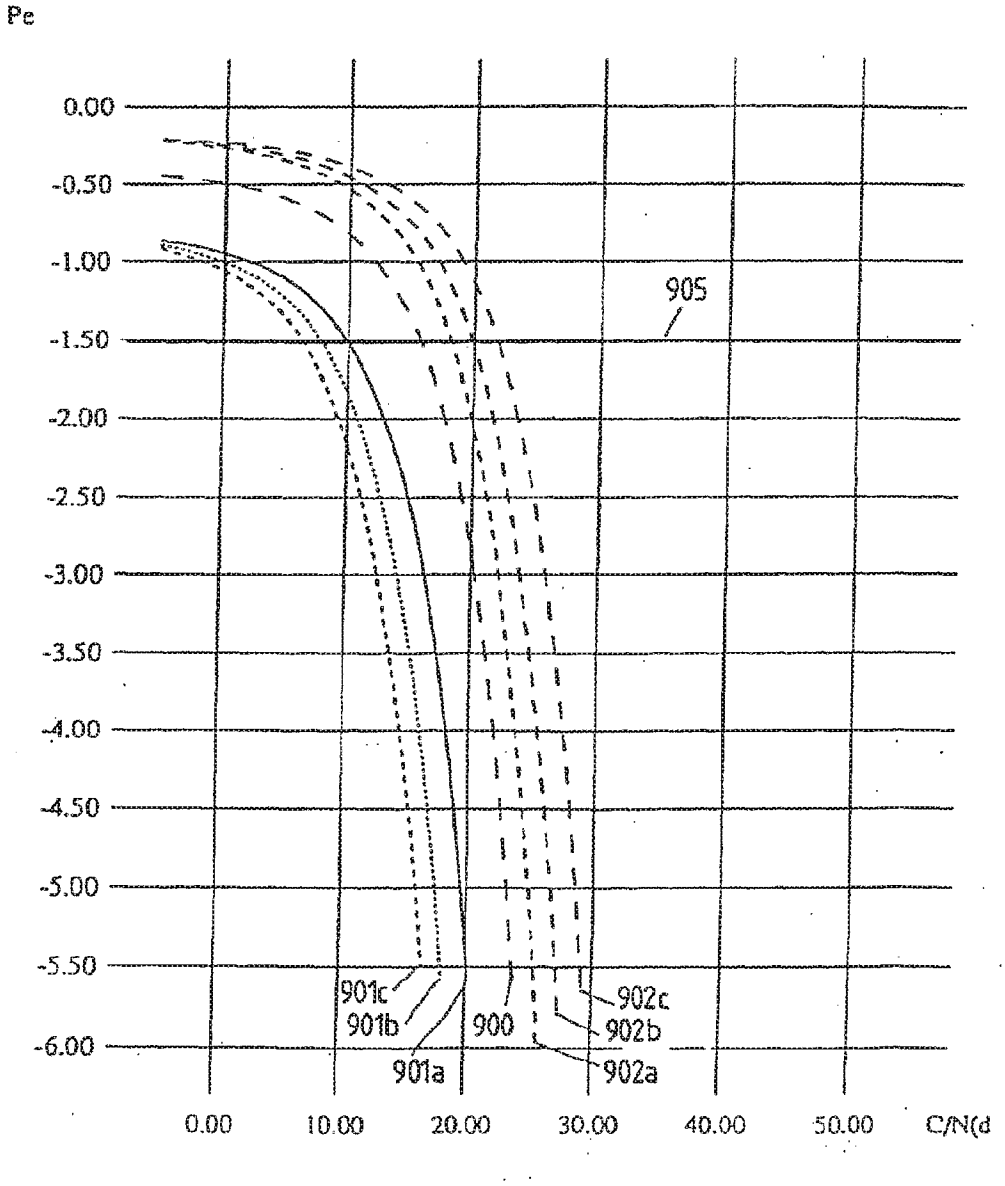


FIG. 102

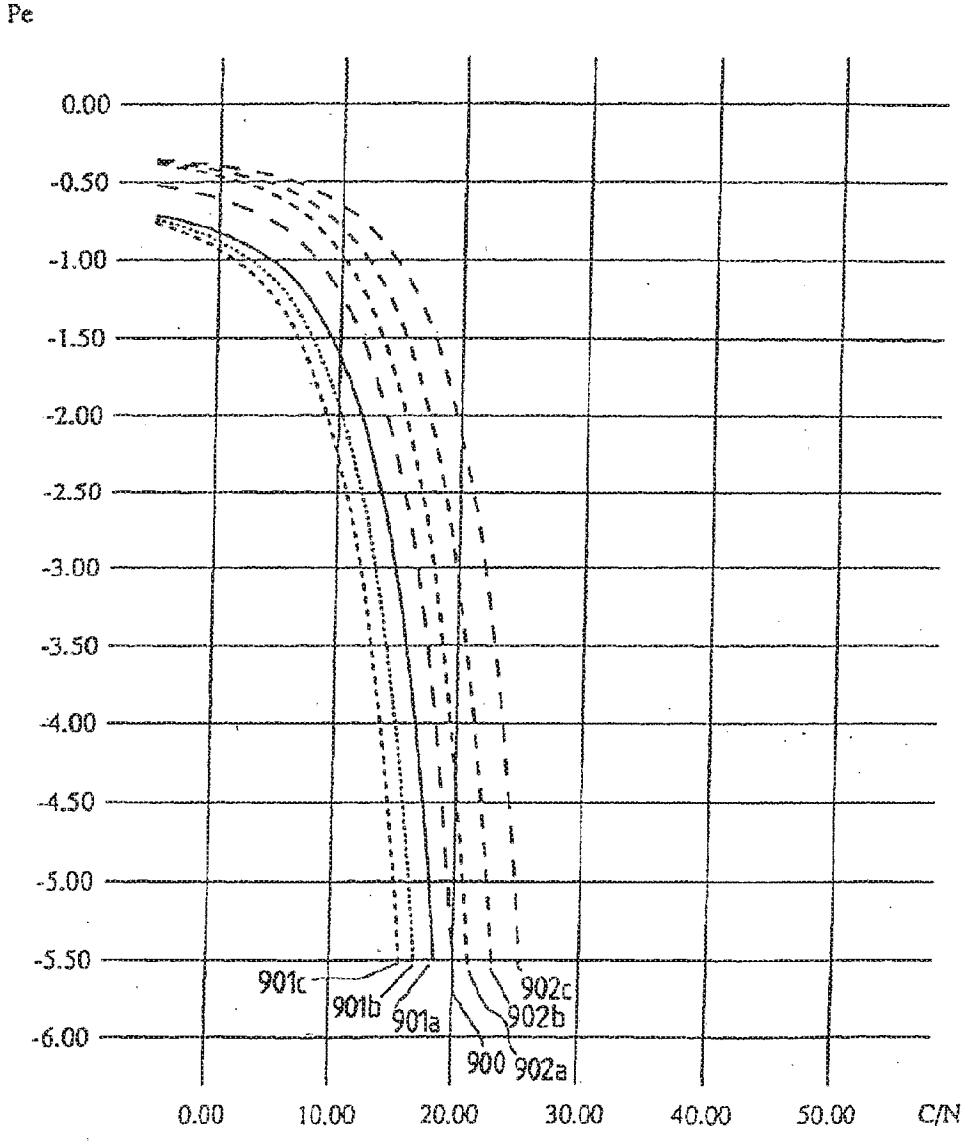


FIG. 103

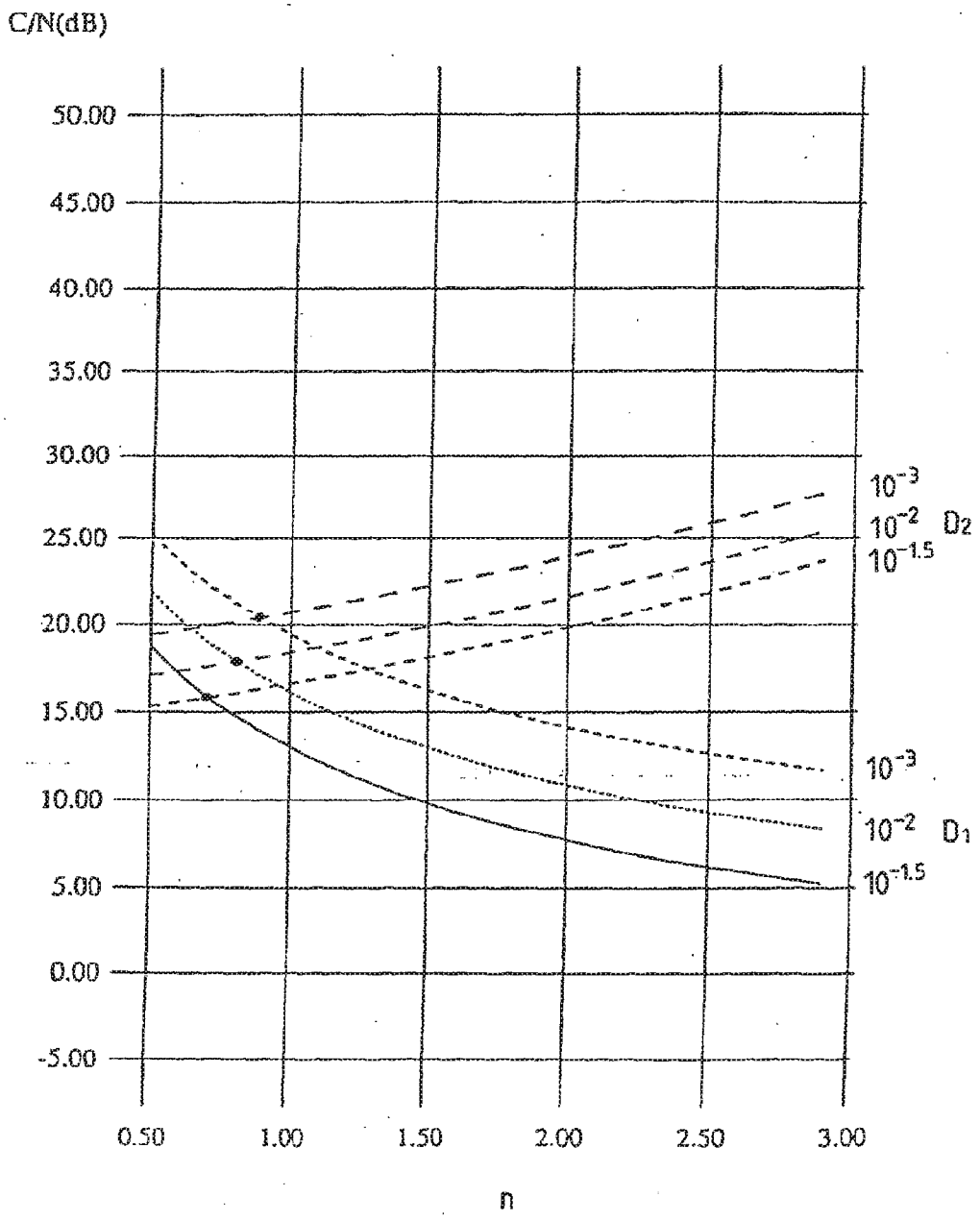


FIG. 104

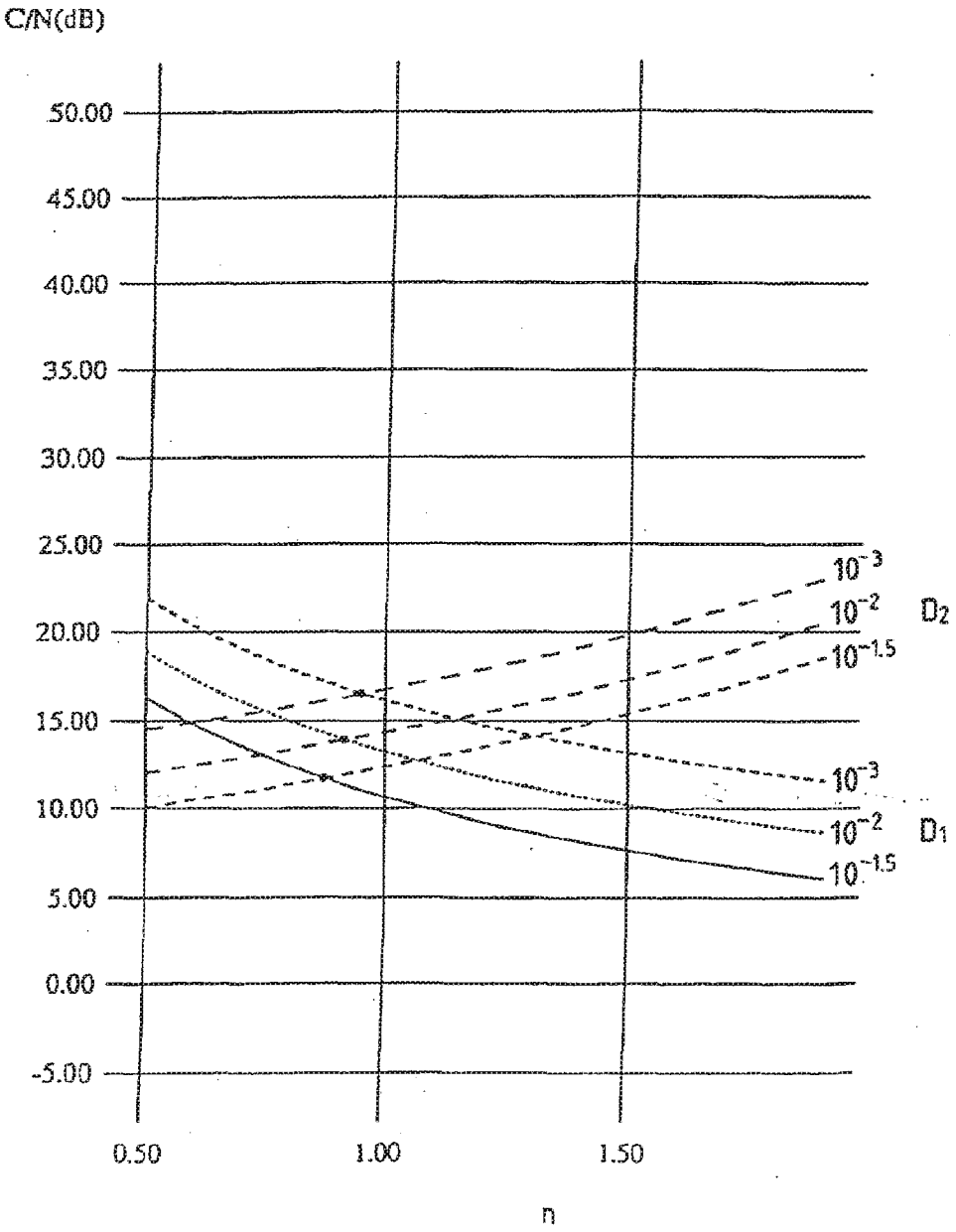


FIG. 105

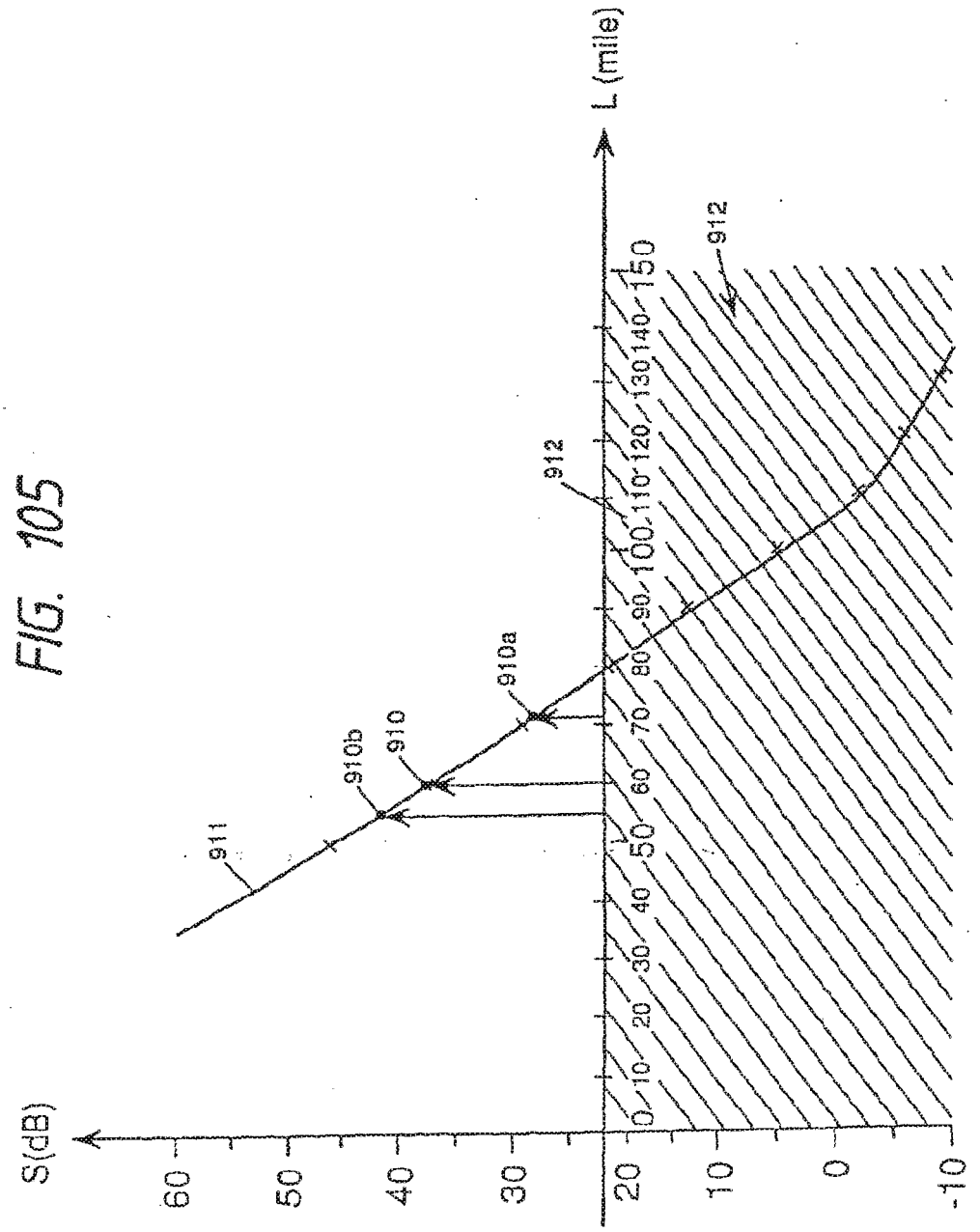


FIG. 106

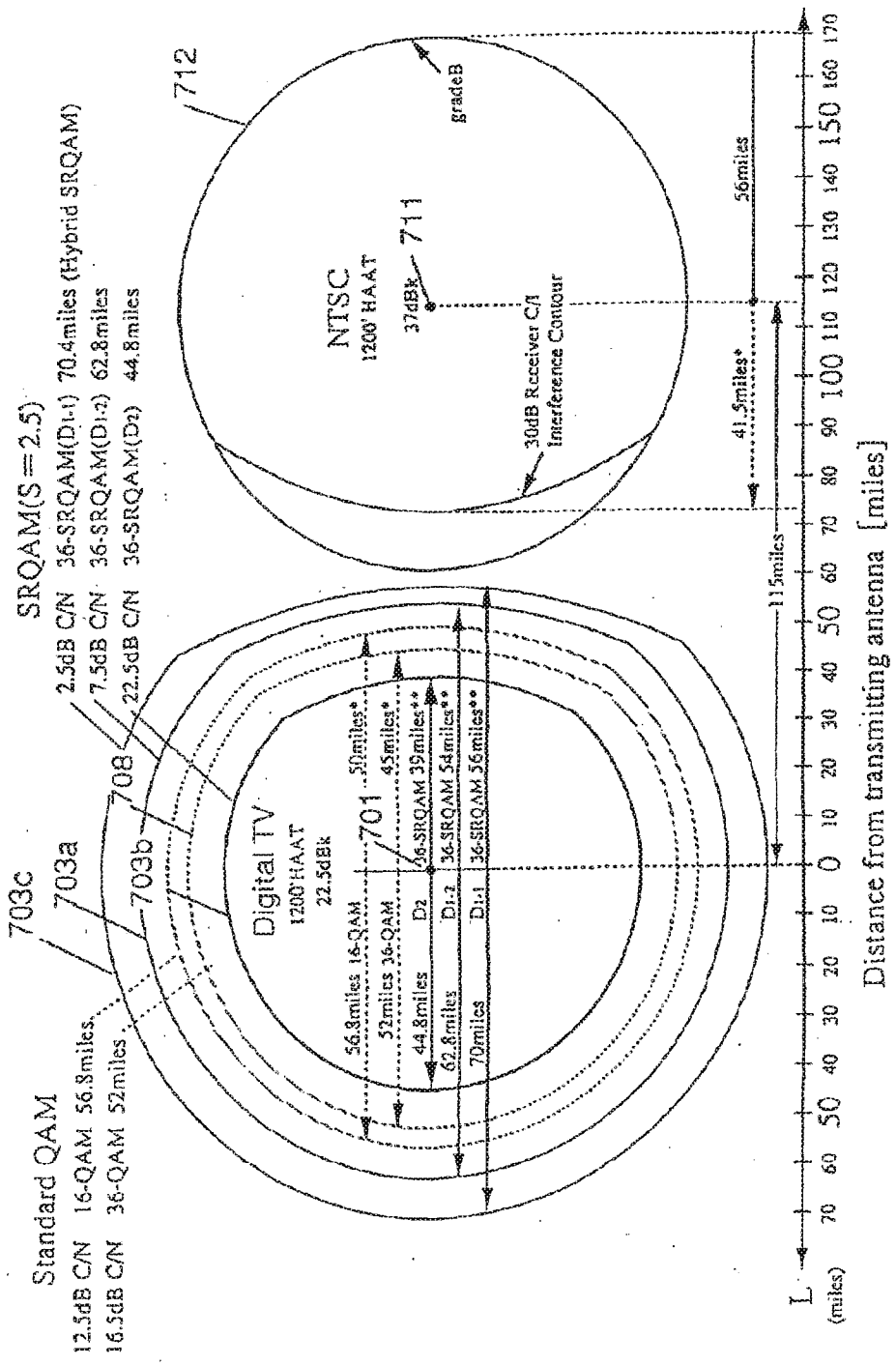


FIG. 107

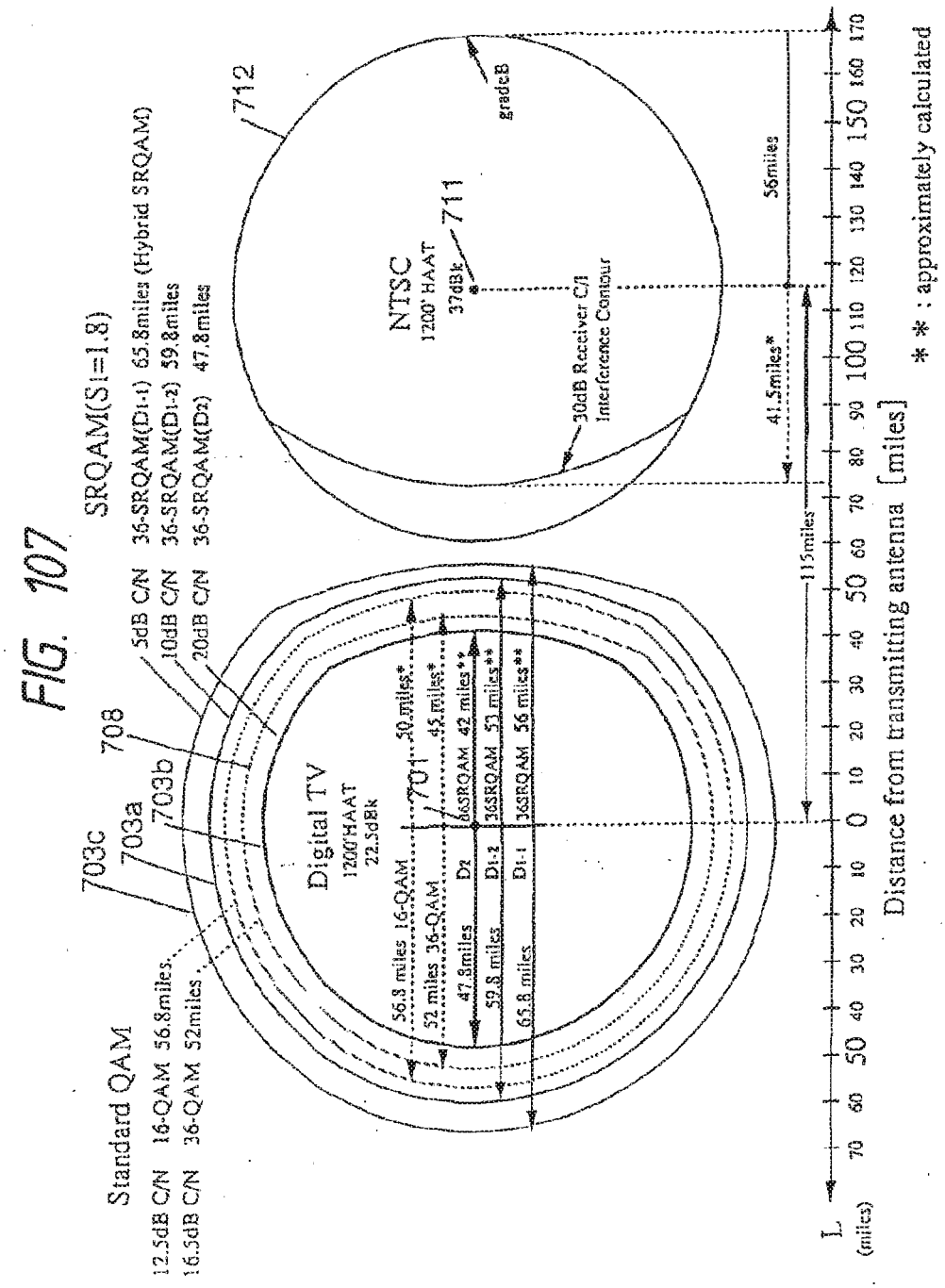


FIG. 108

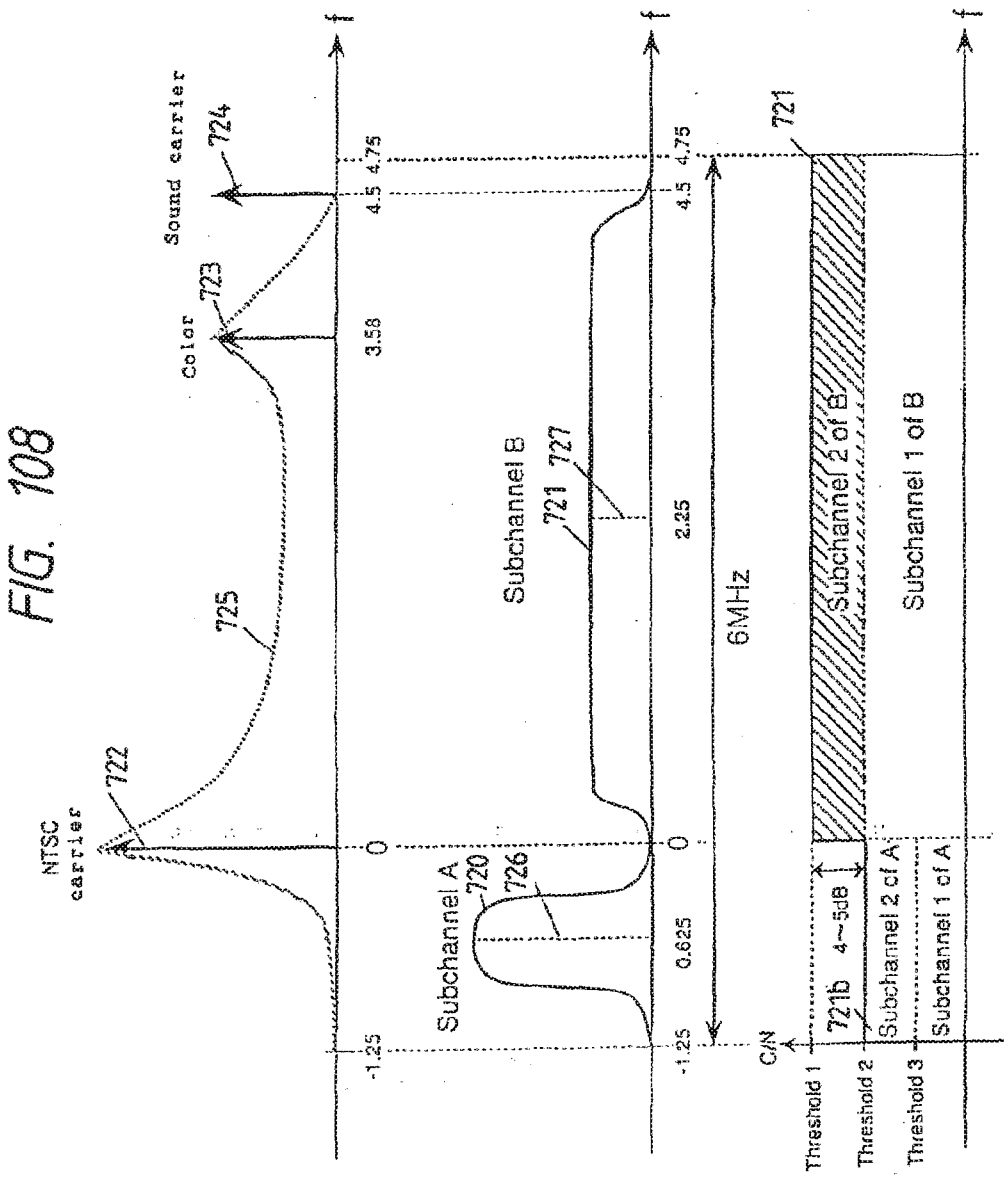
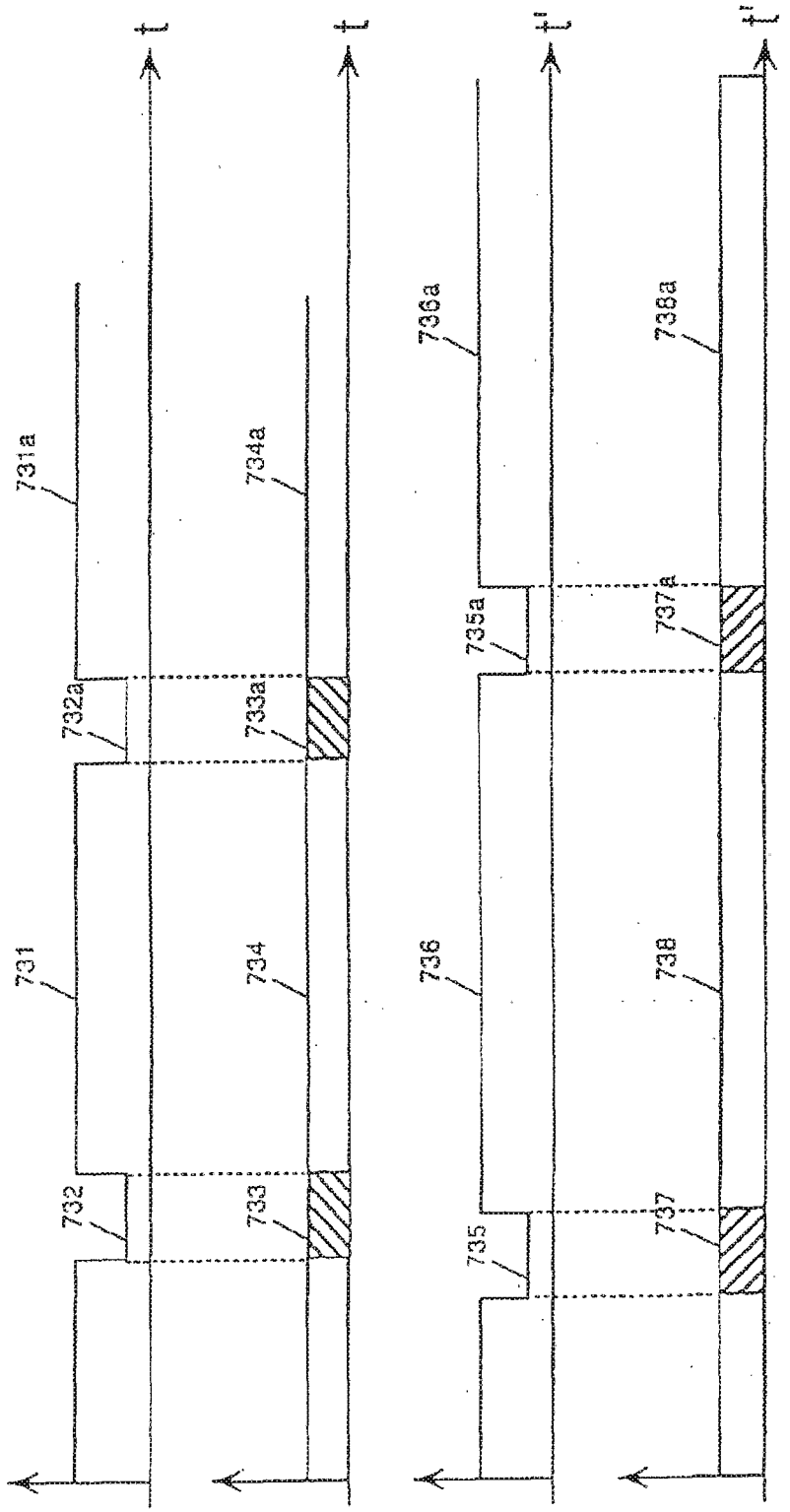


FIG. 109



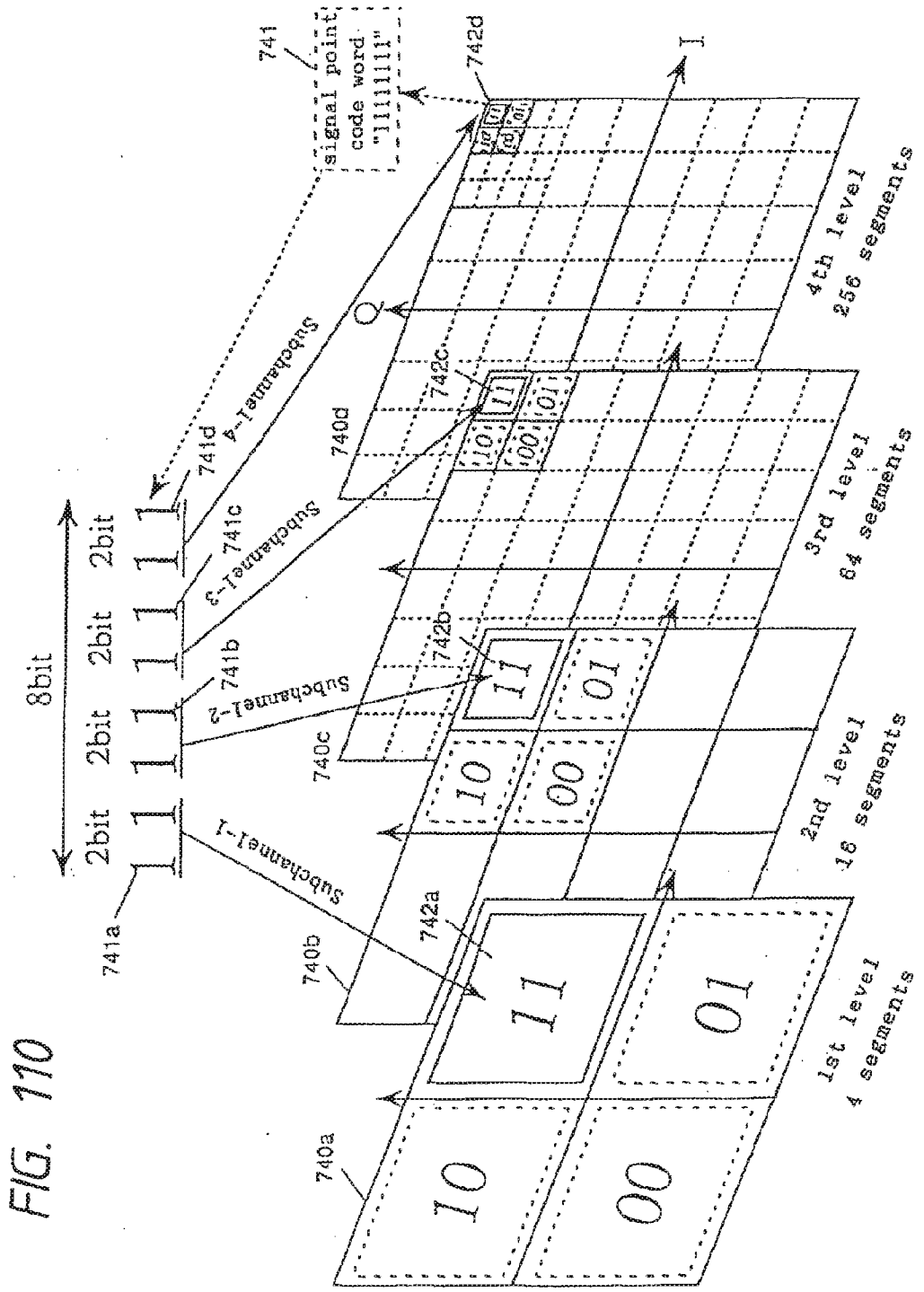


FIG. 110

FIG. 111

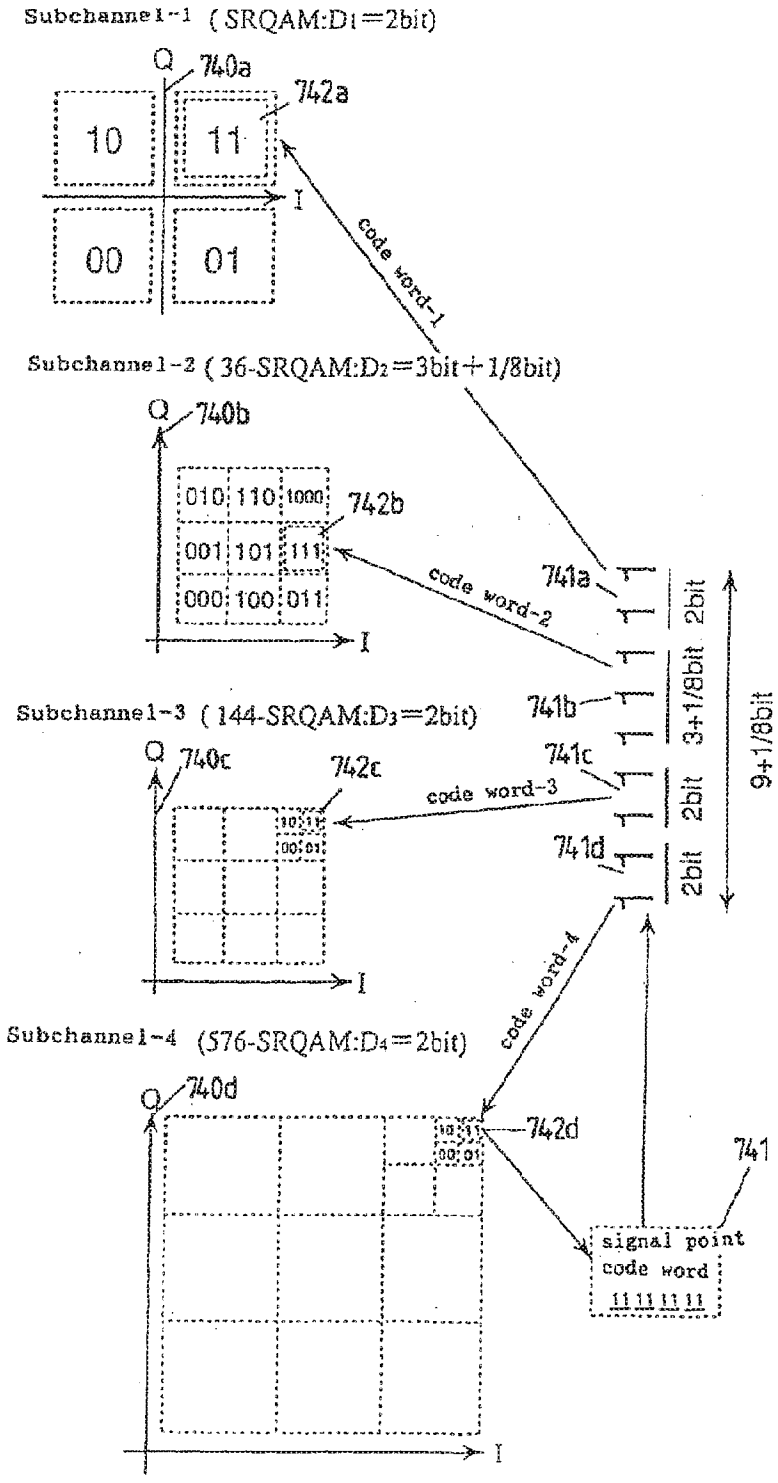


FIG. 112

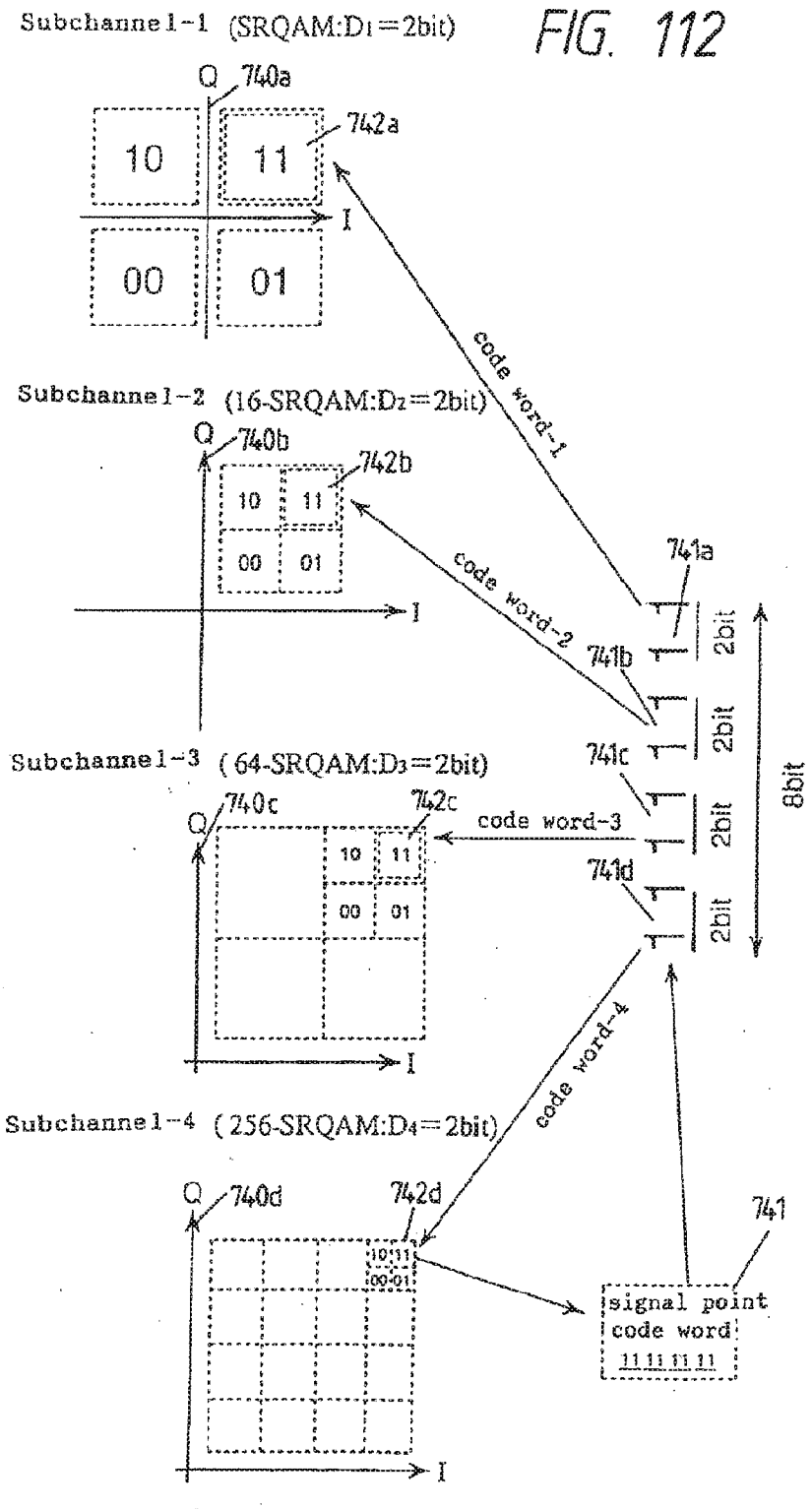


FIG. 113

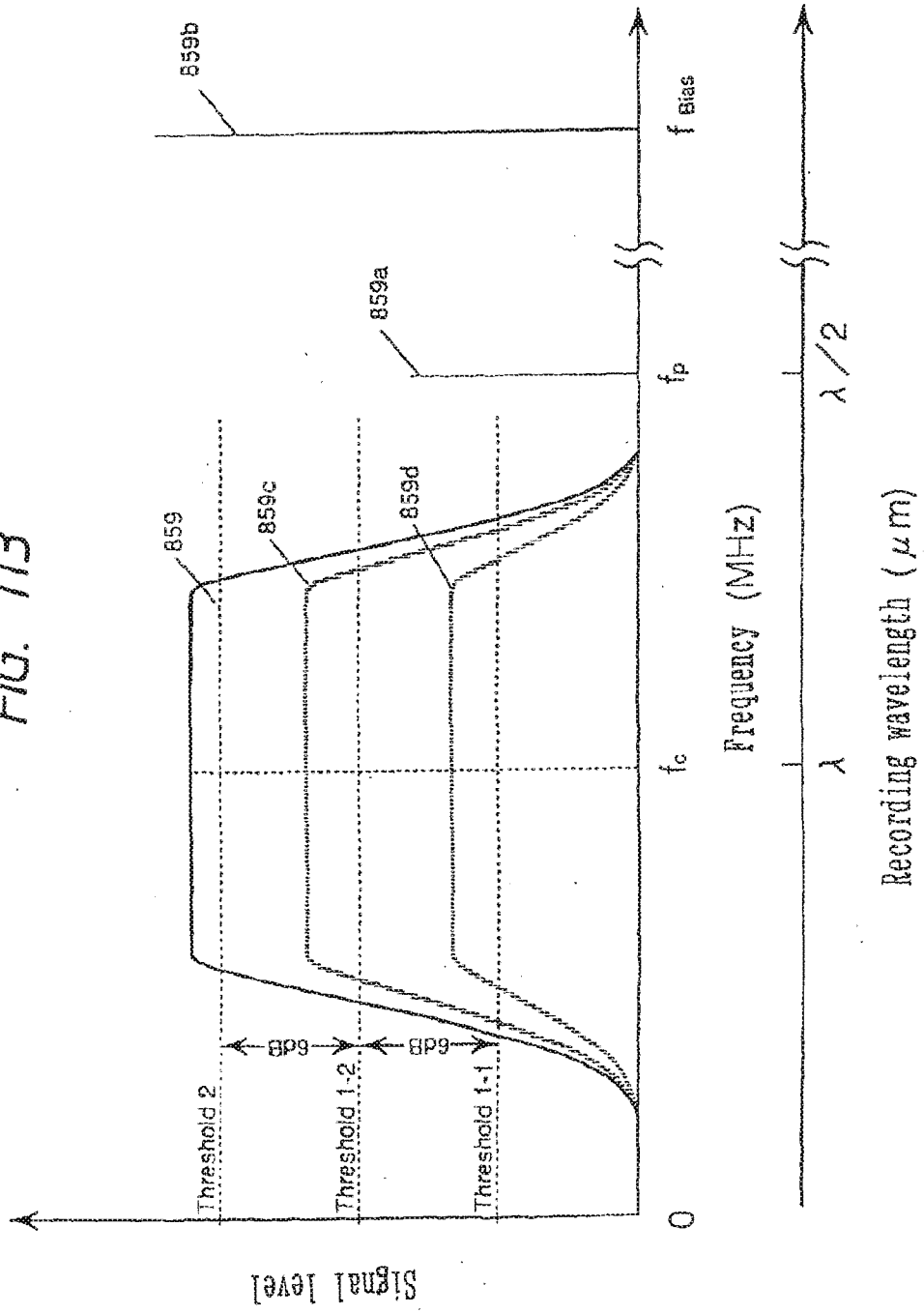


FIG. 114

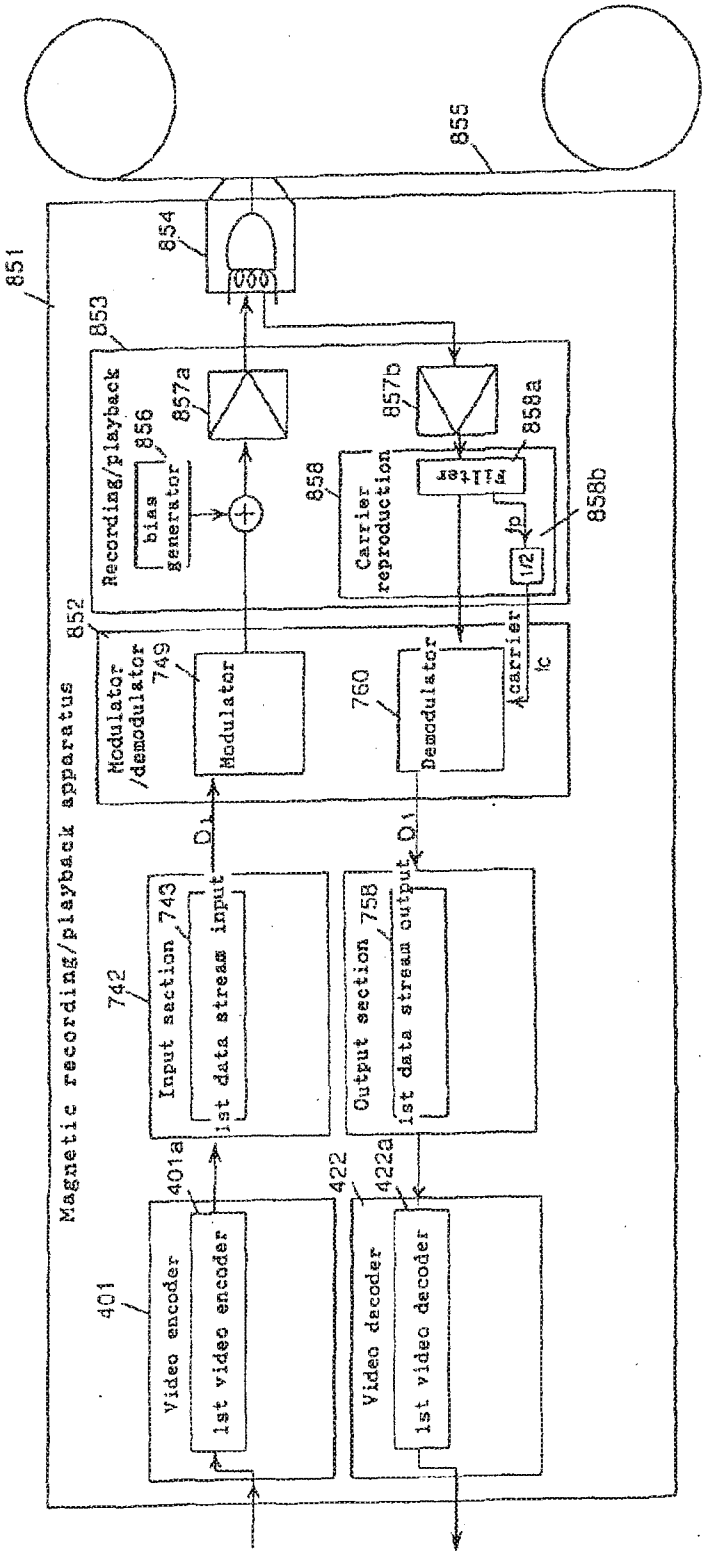
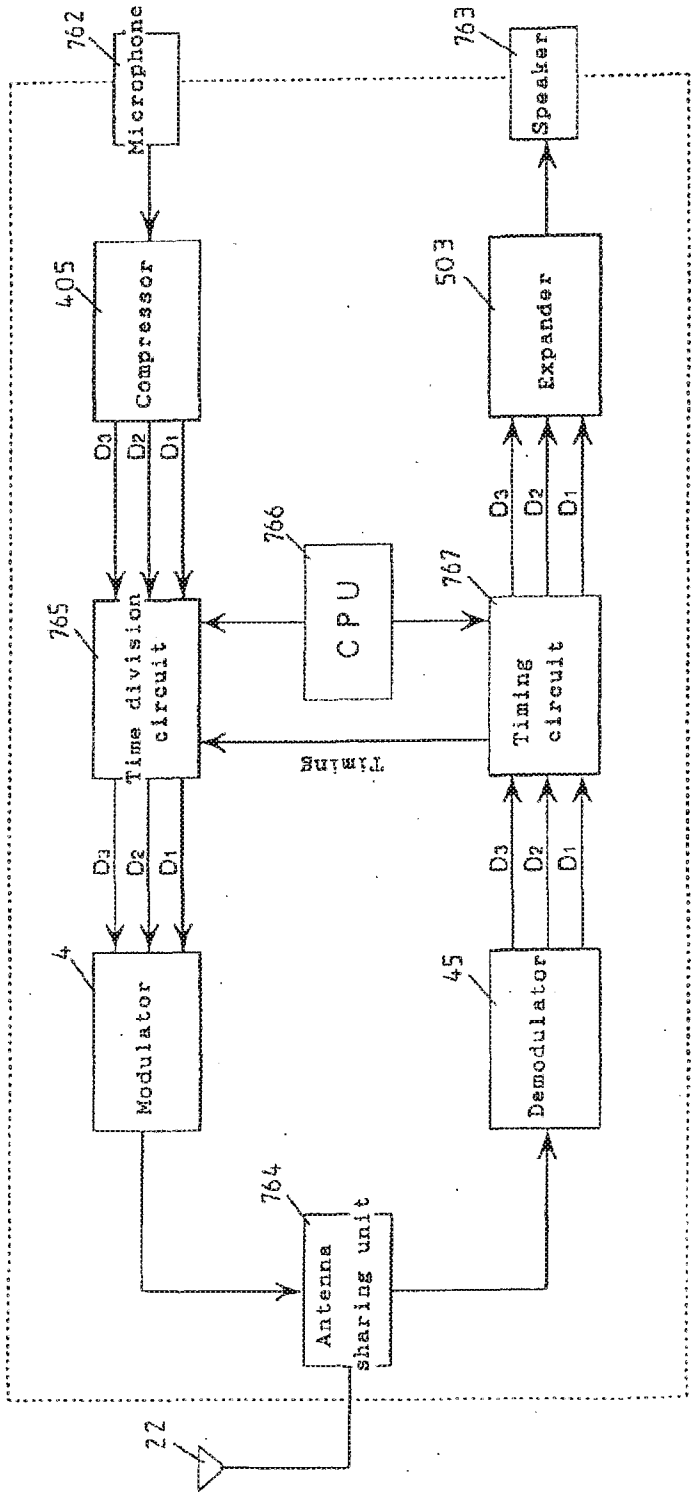


FIG. 115



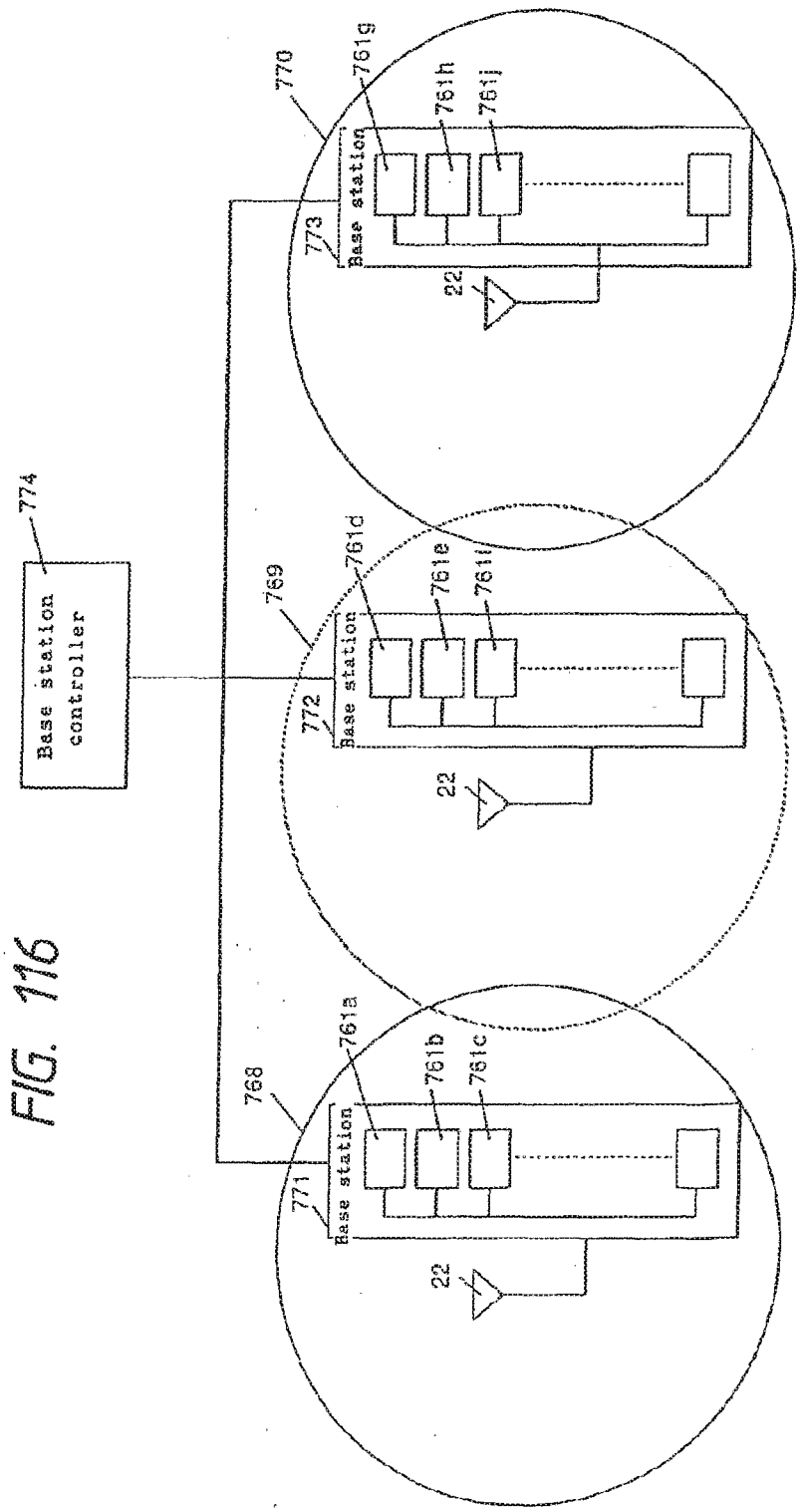


FIG. 116

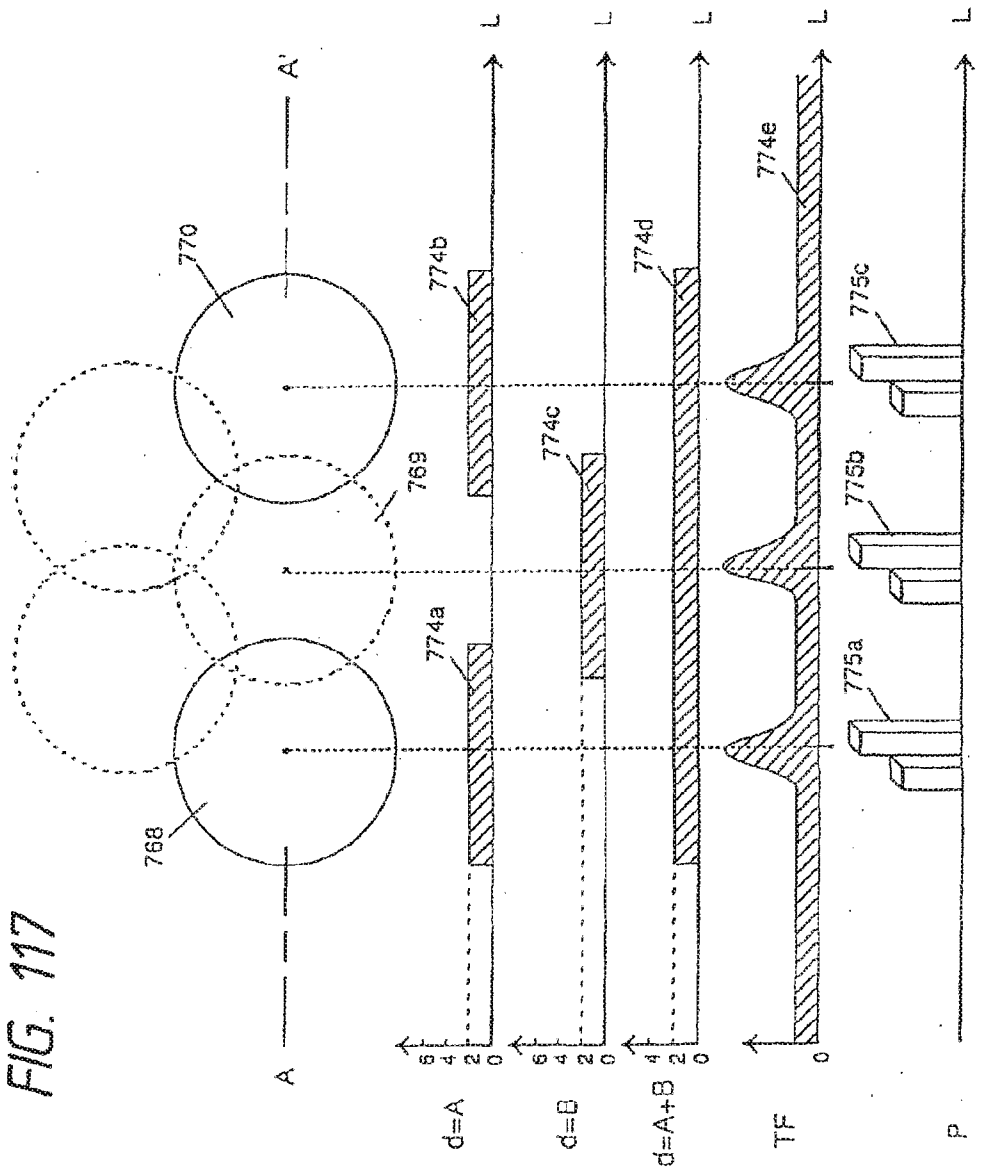


FIG. 117

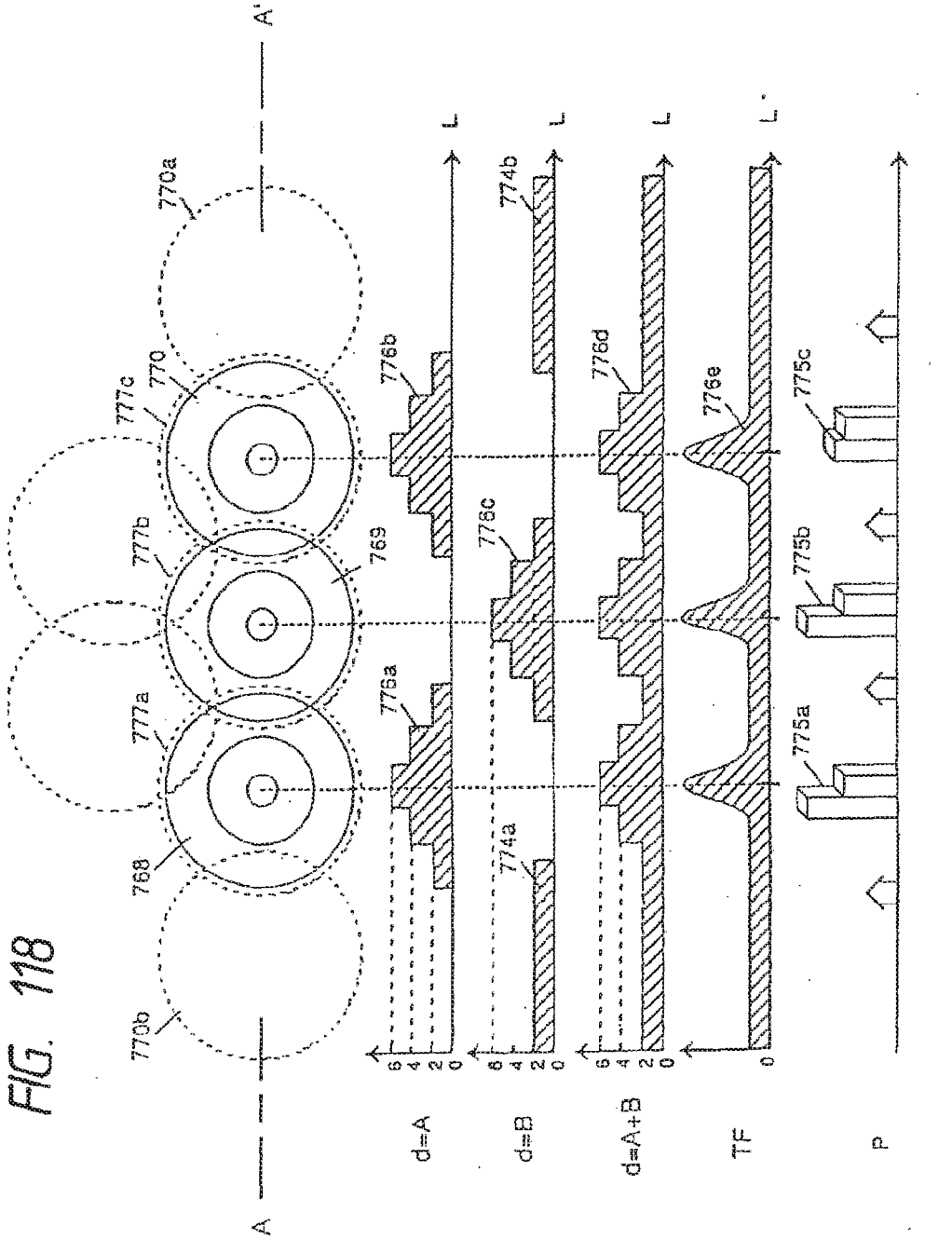


FIG. 118

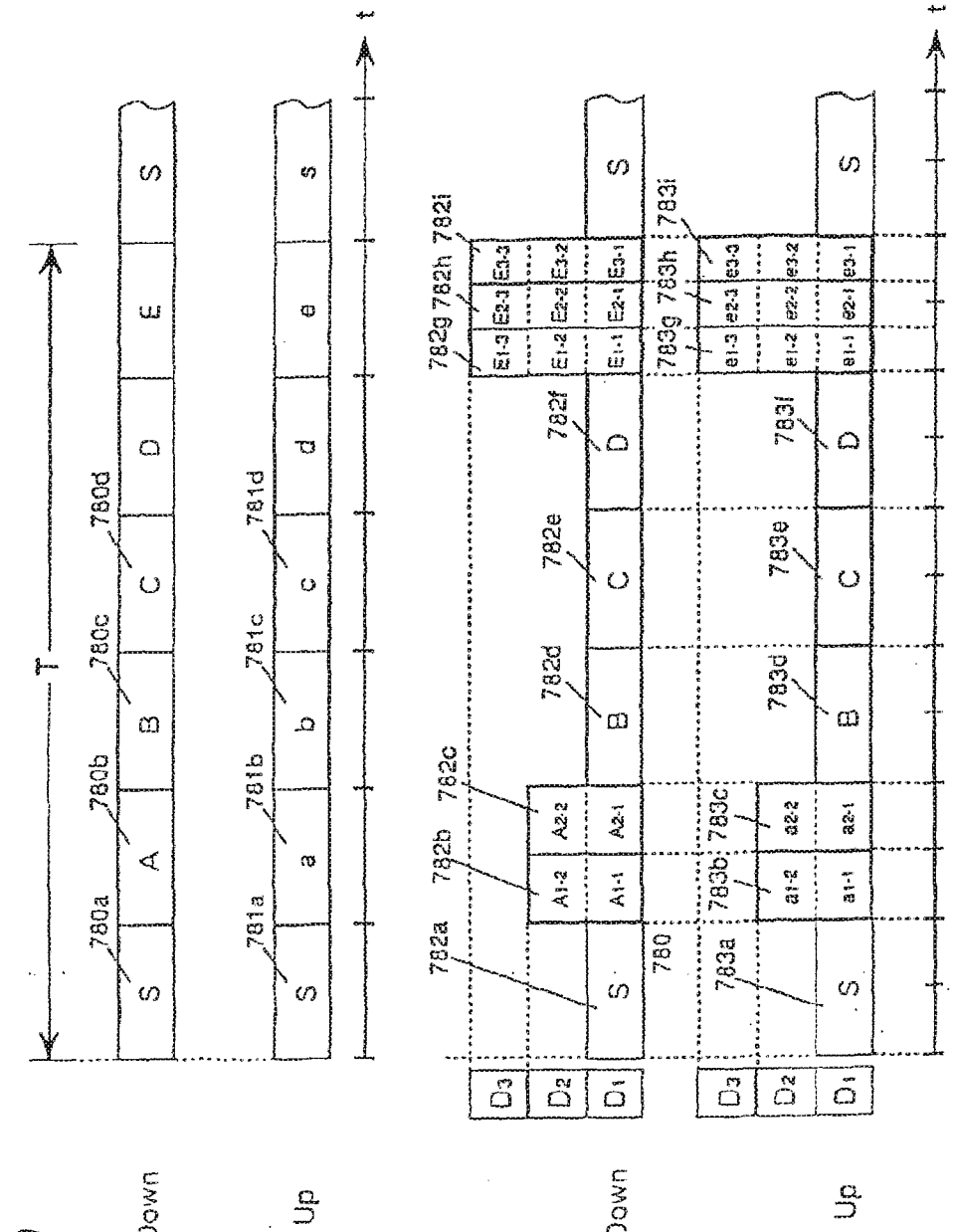


FIG. 119

FIG. 120

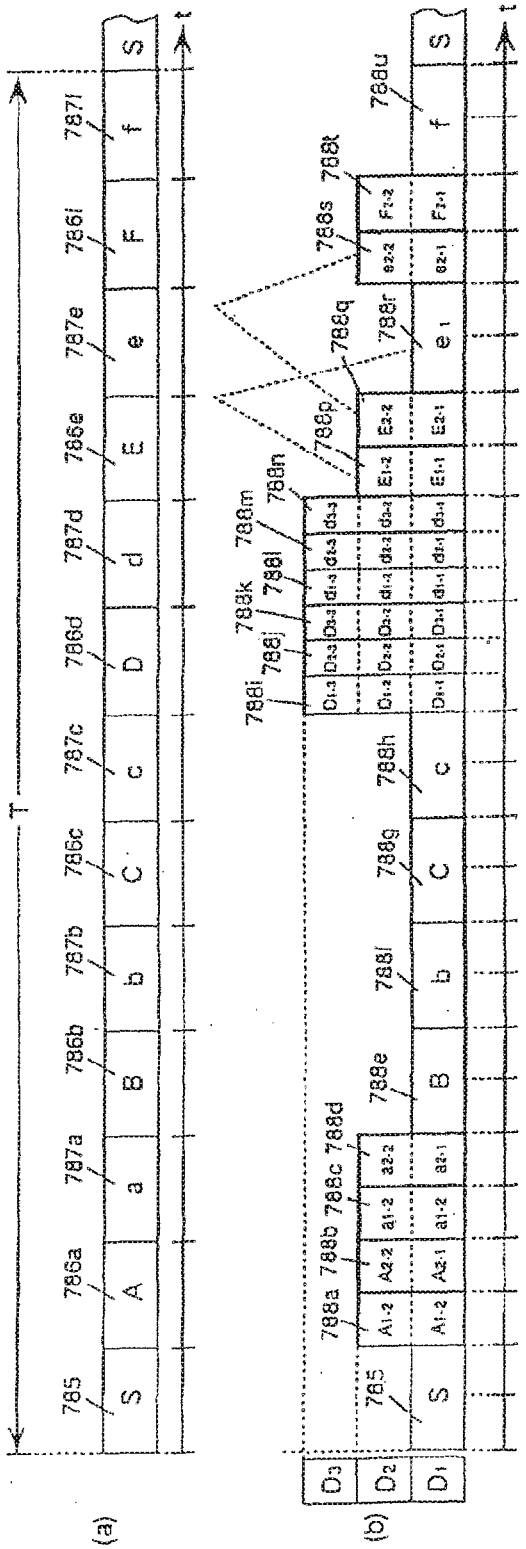


FIG. 121

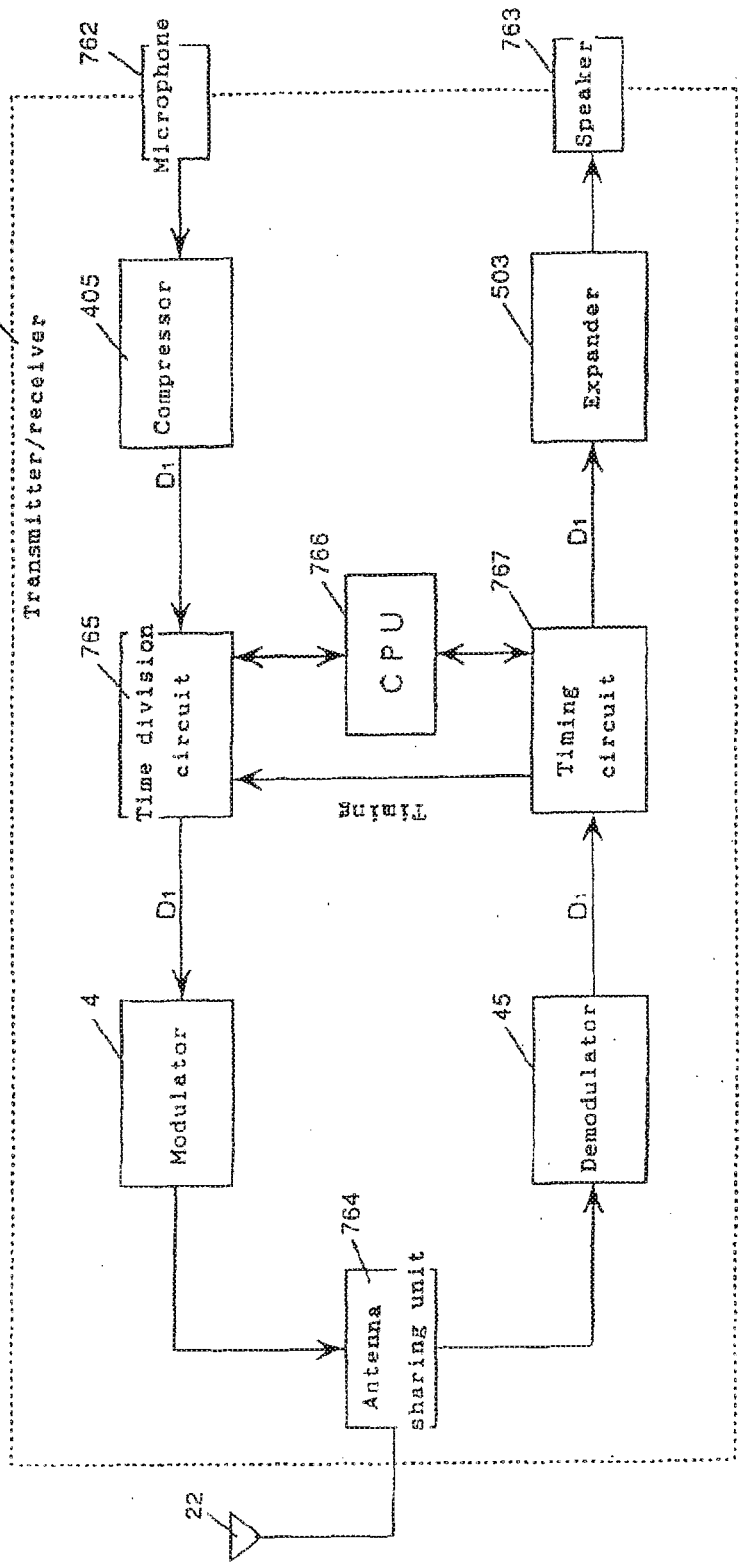


FIG. 122

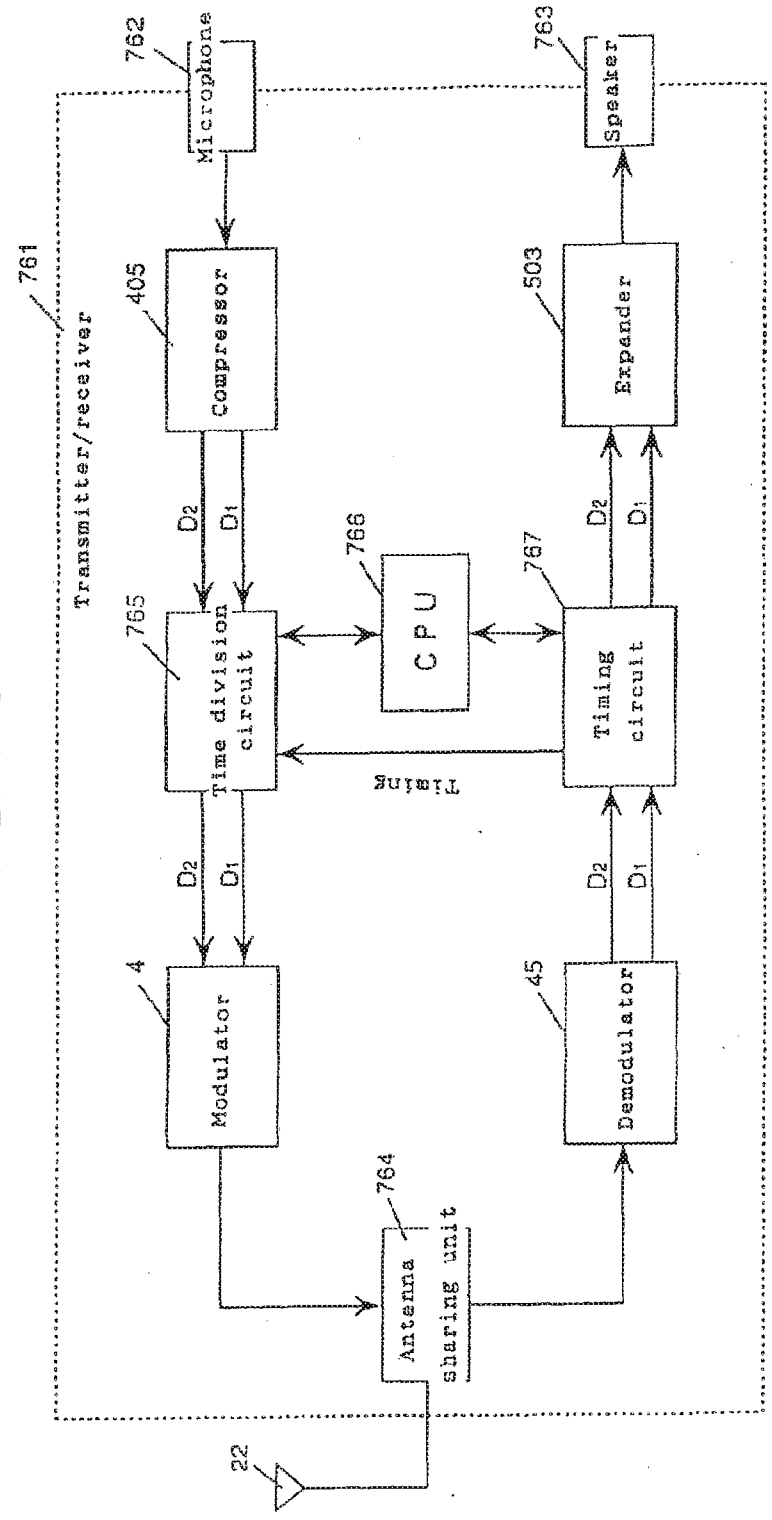
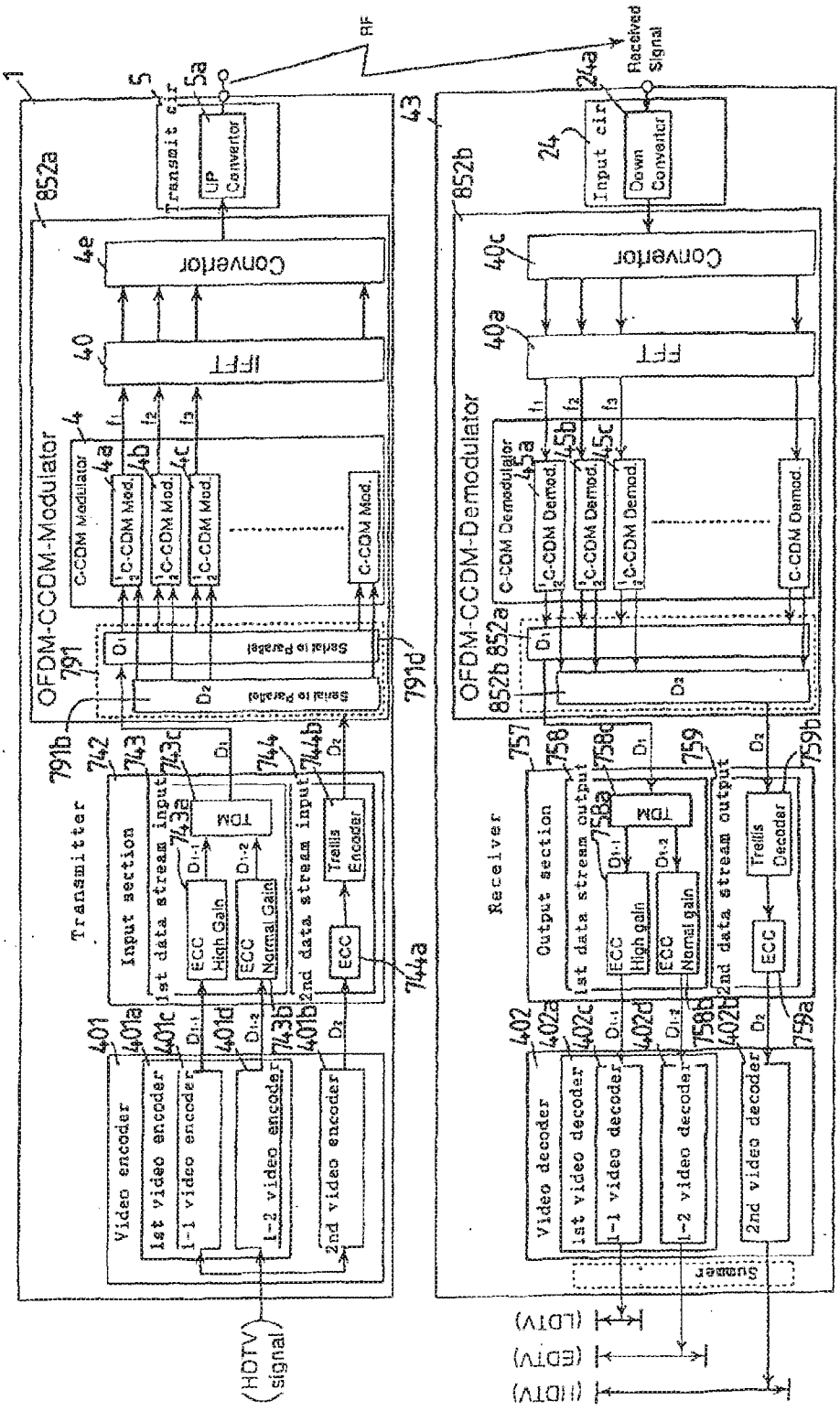


FIG. 123



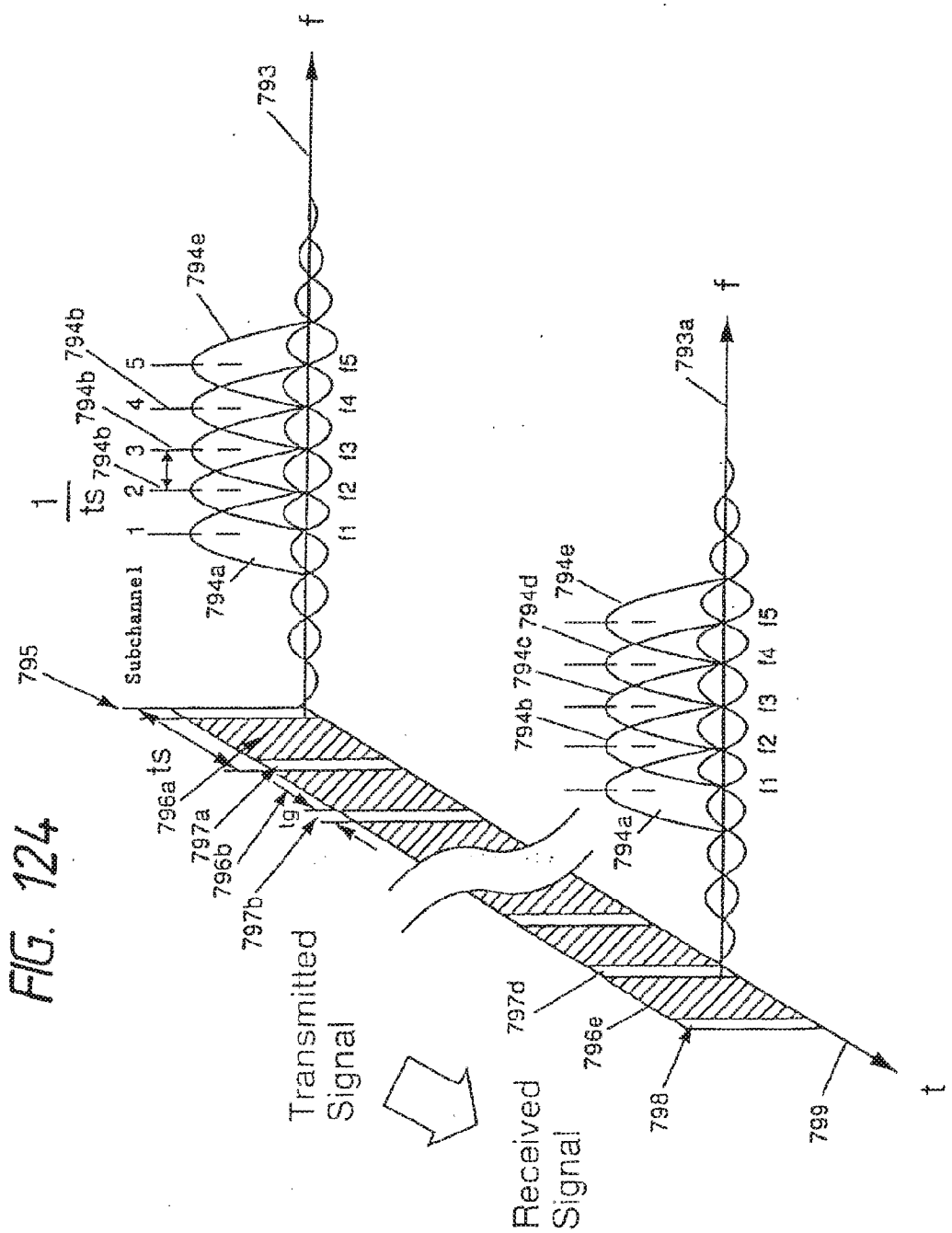

f
793
794e
794b
794b
794b
794a
1
tS
Subchannel
1 2 3 4 5
f1 f2 f3 f4 f5
795
796a tS
797a
796b
tg
797b
Transmitted Signal
793a
f
794e
794d
794c
794b
794a
f1 f2 f3 f4 f5
797d
796e
798
799
Received Signal
t

FIG. 124

FIG. 125

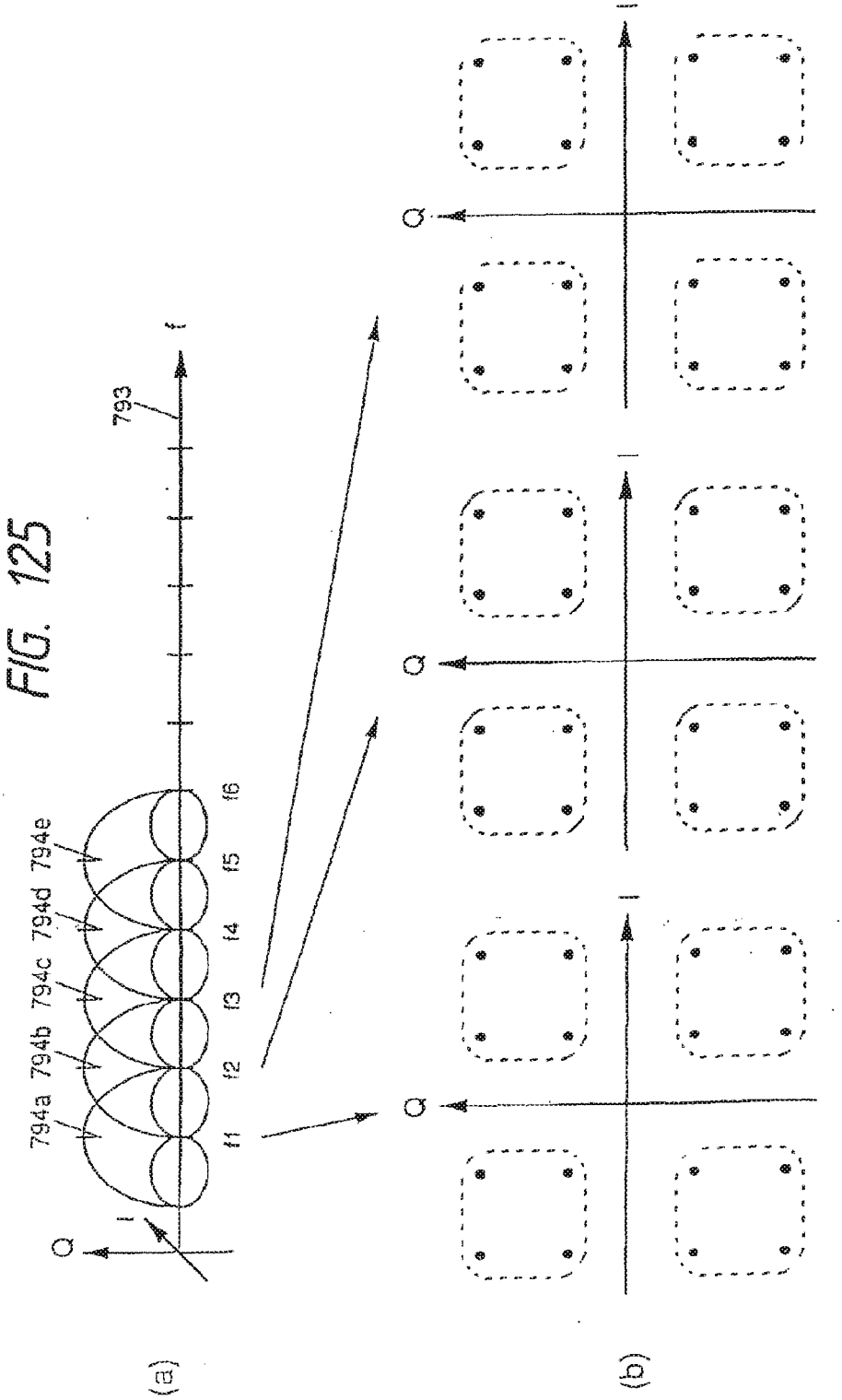


FIG. 126

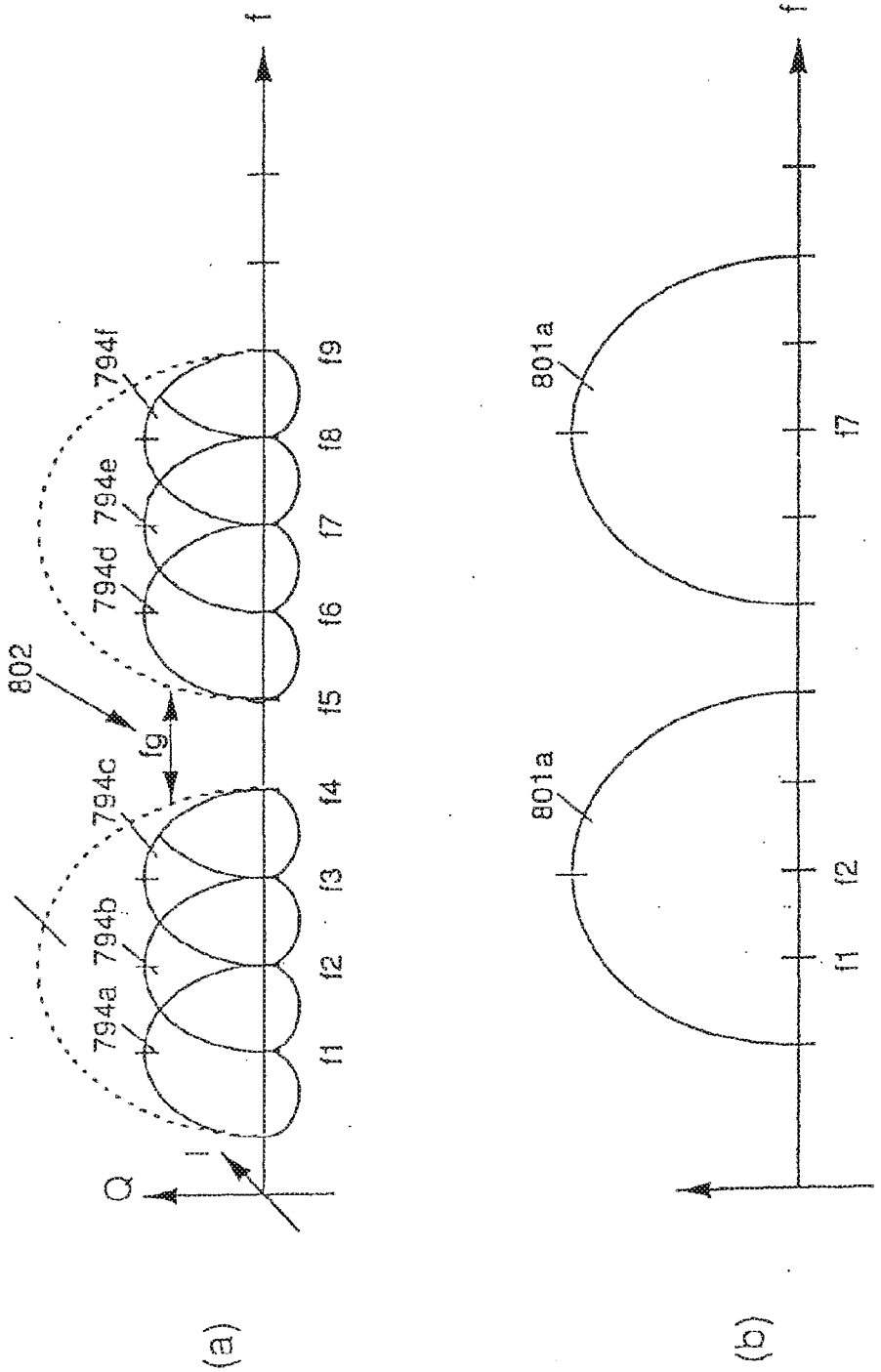
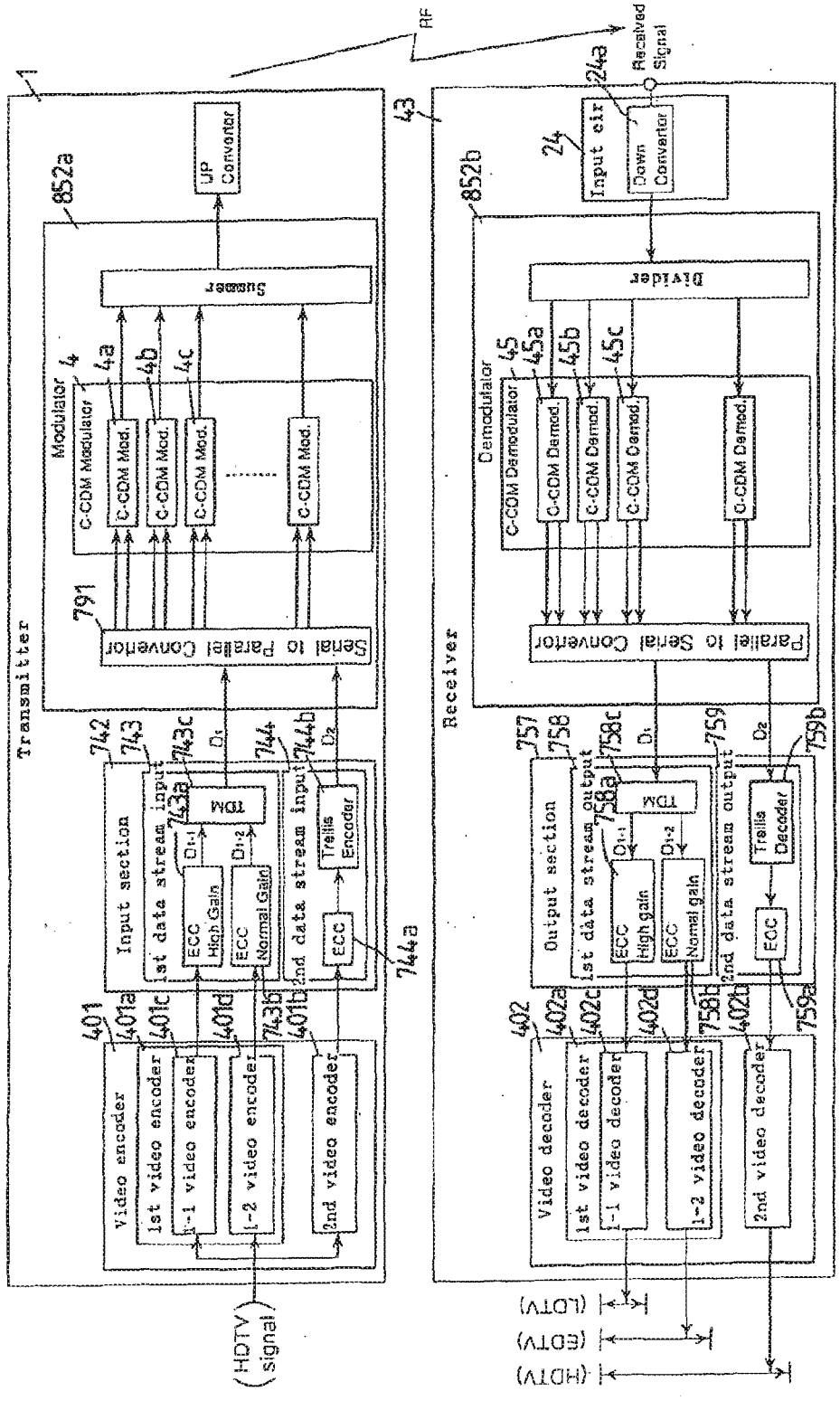


FIG. 127



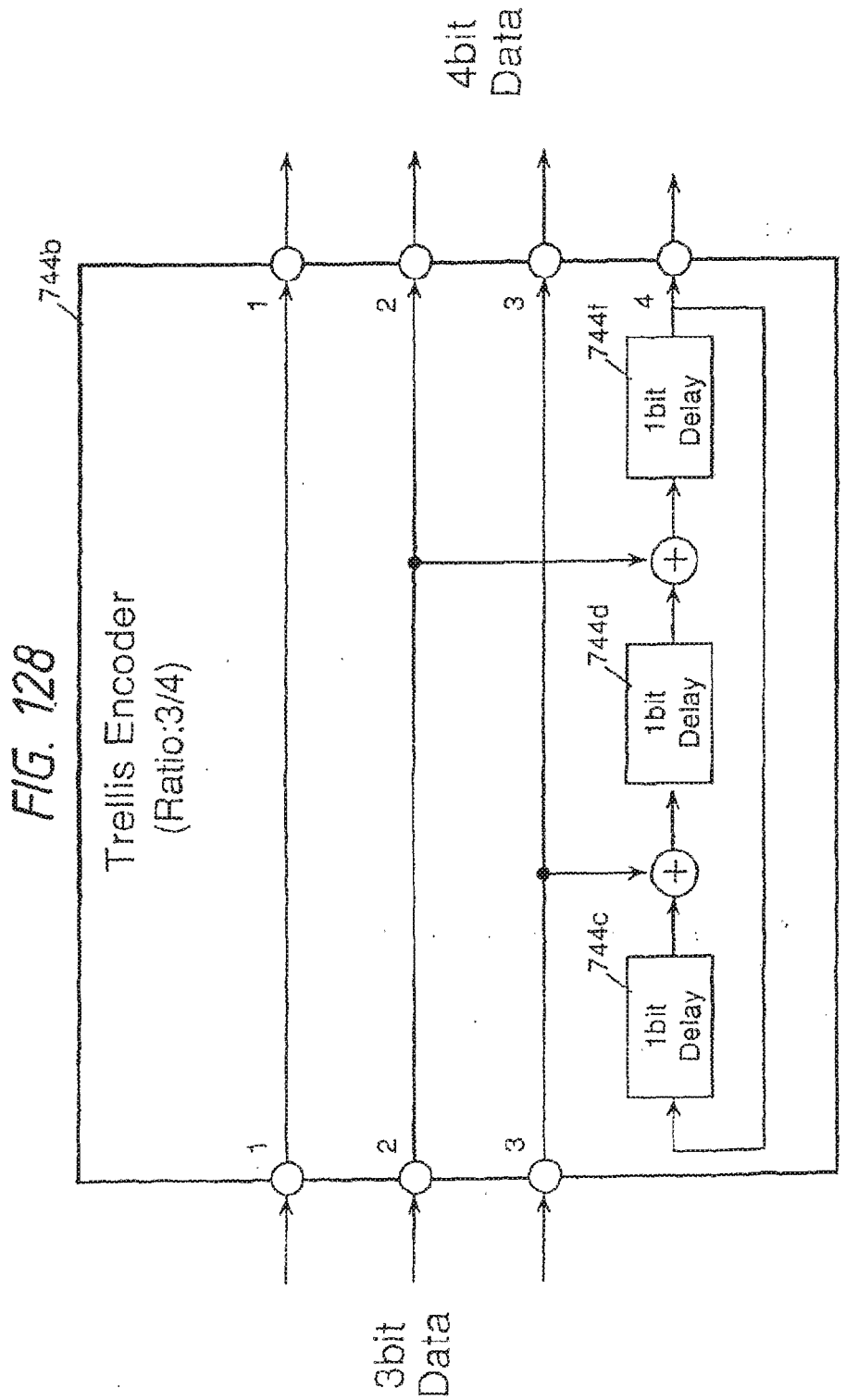


FIG. 128

FIG. 129

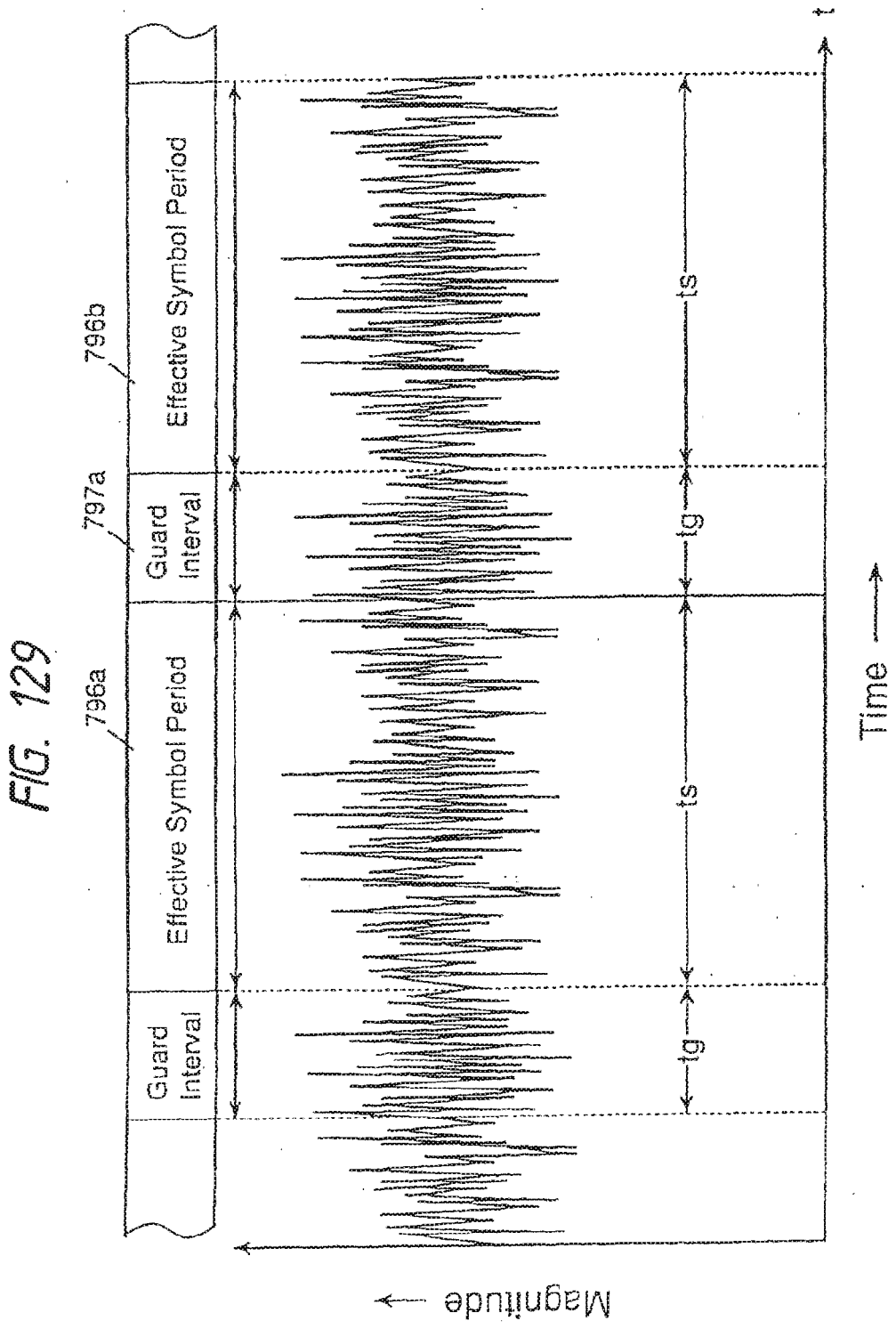

796a
Effective Symbol Period
797a
Guard Interval
796b
Effective Symbol Period
Guard Interval
ts
tg
ts
tg
Time
Magnitude
t

FIG. 13a

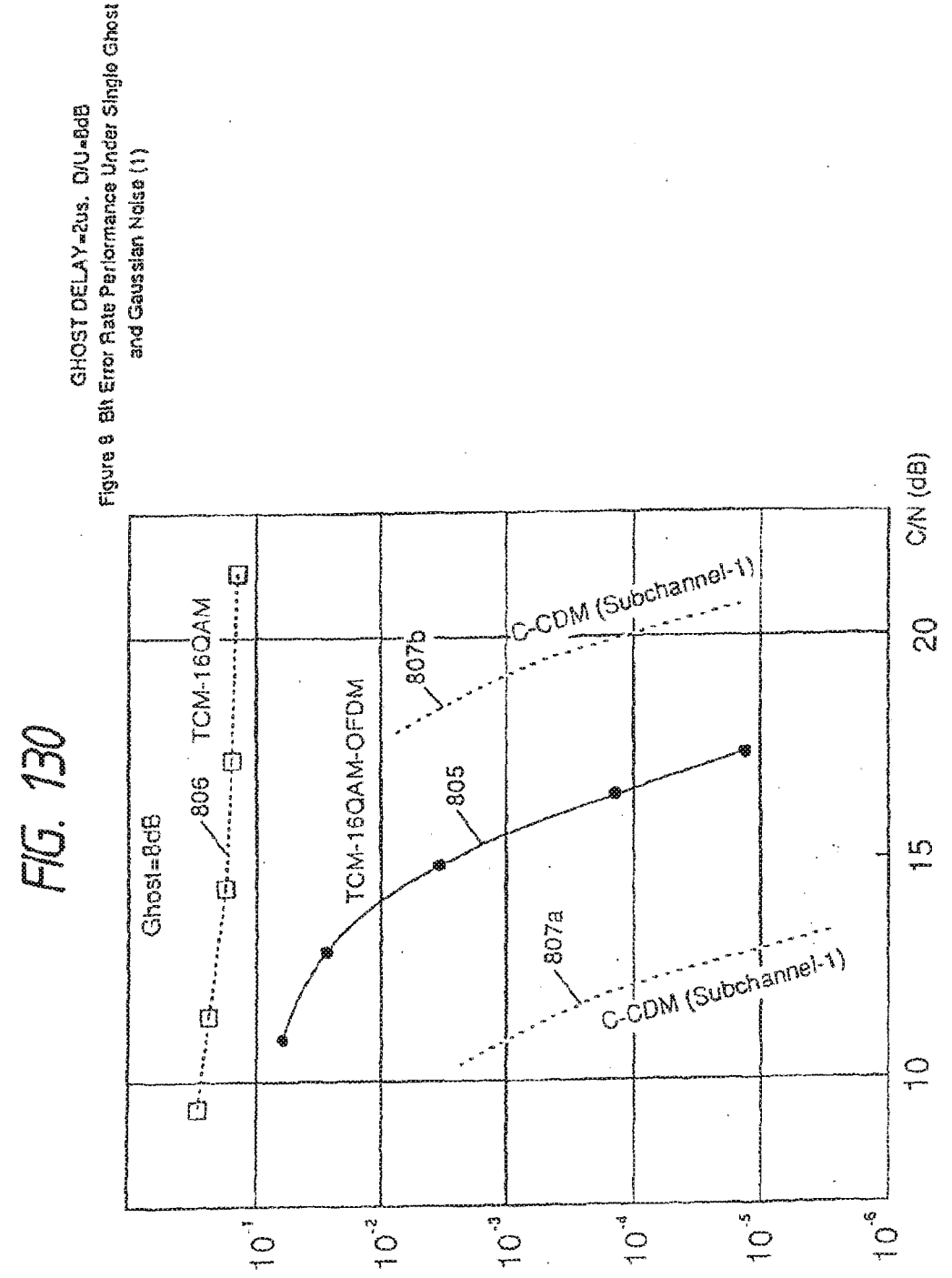
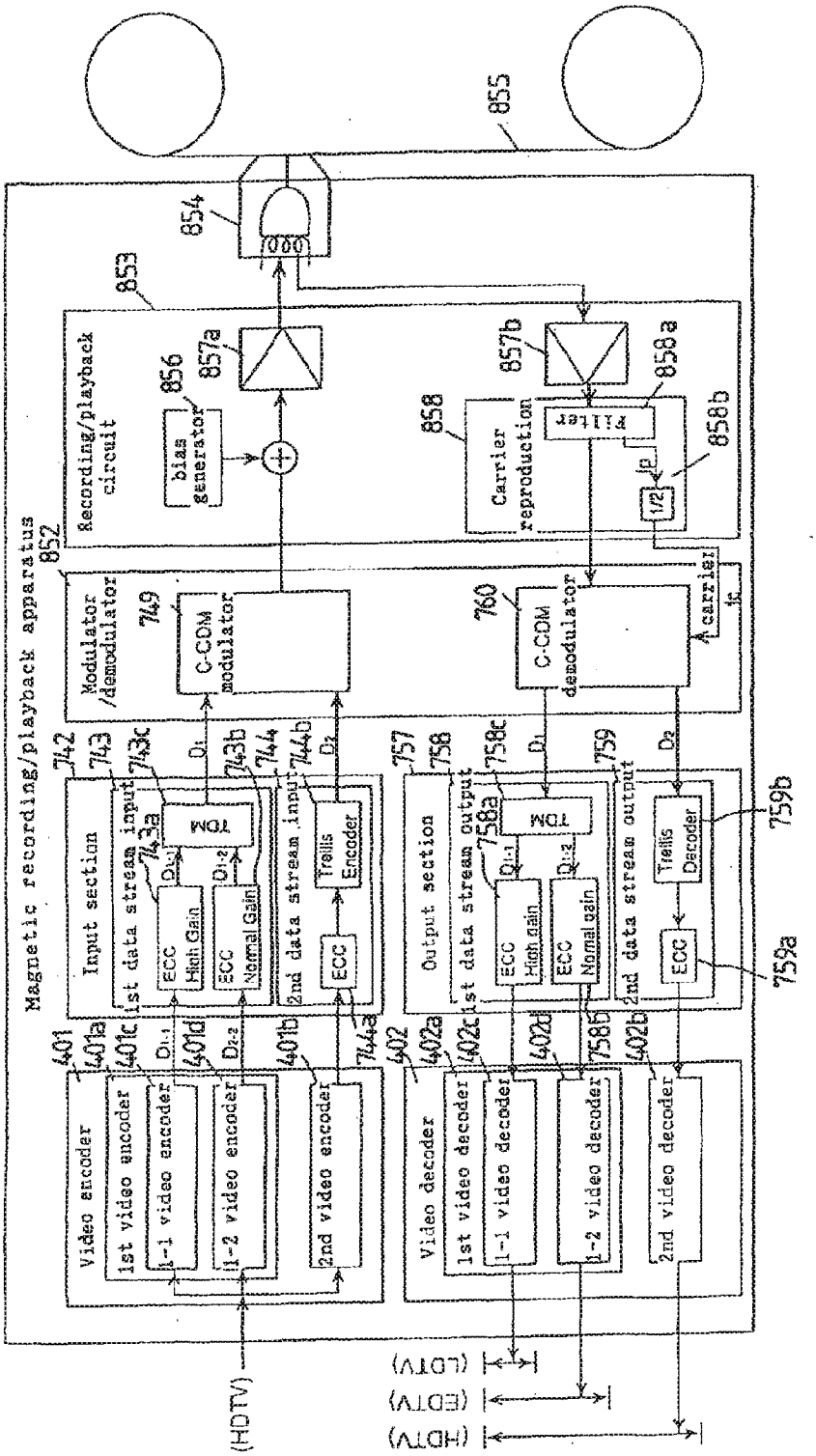


Figure 9 Bit Error Rate Performance Under Single Ghost and Gaussian Noise (1)

FIG. 131



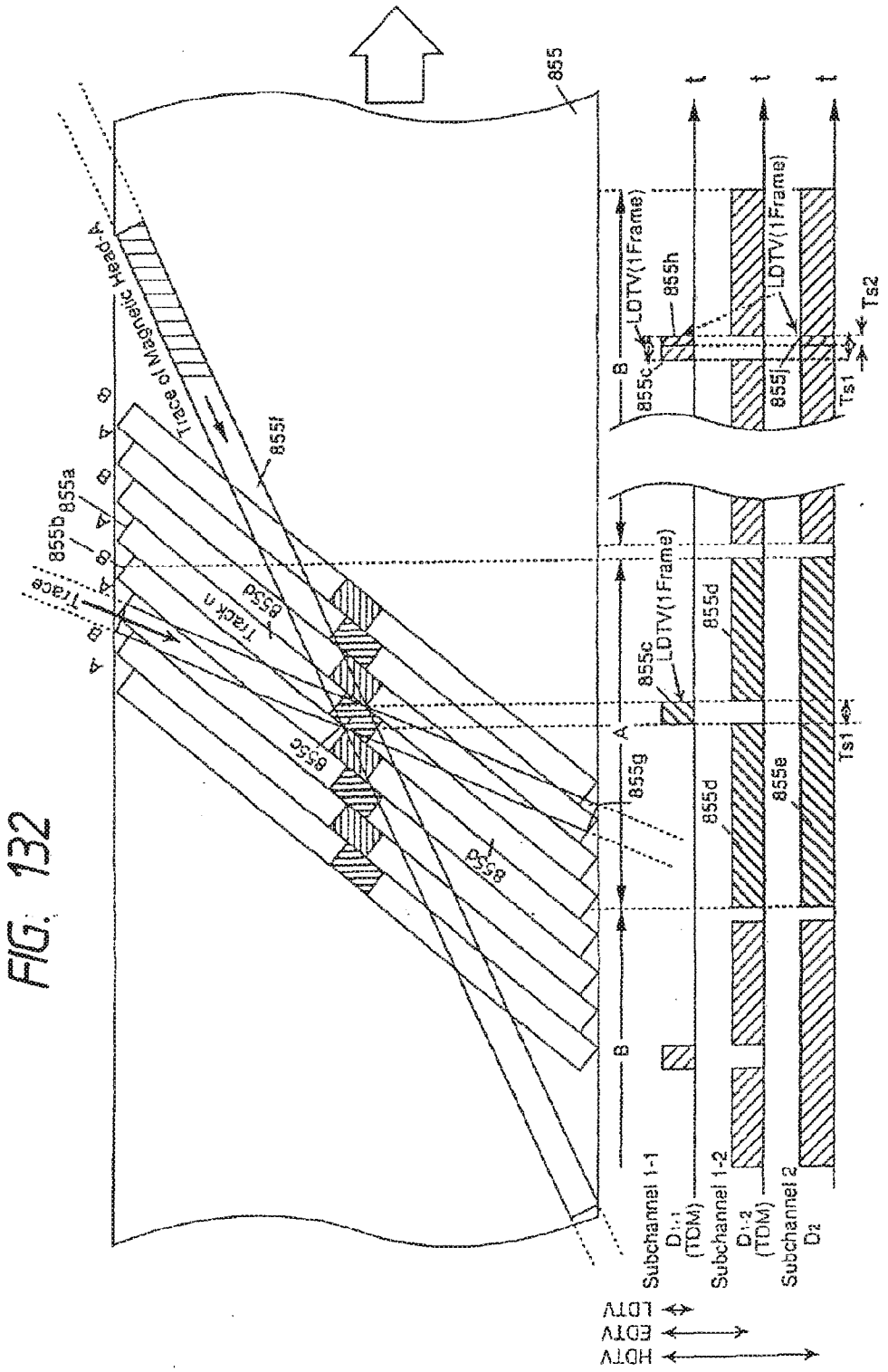
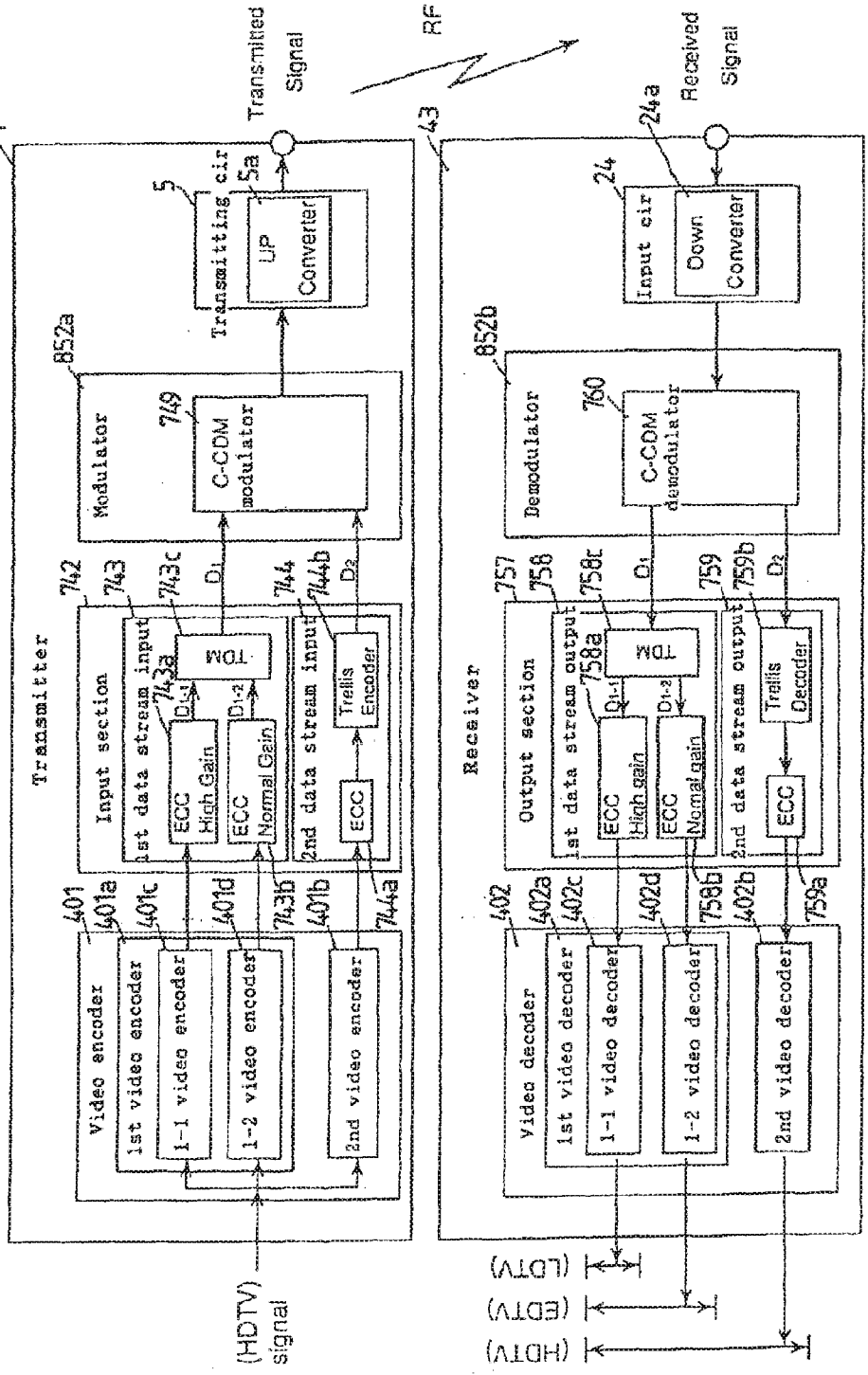


FIG. 132

FIG. 133



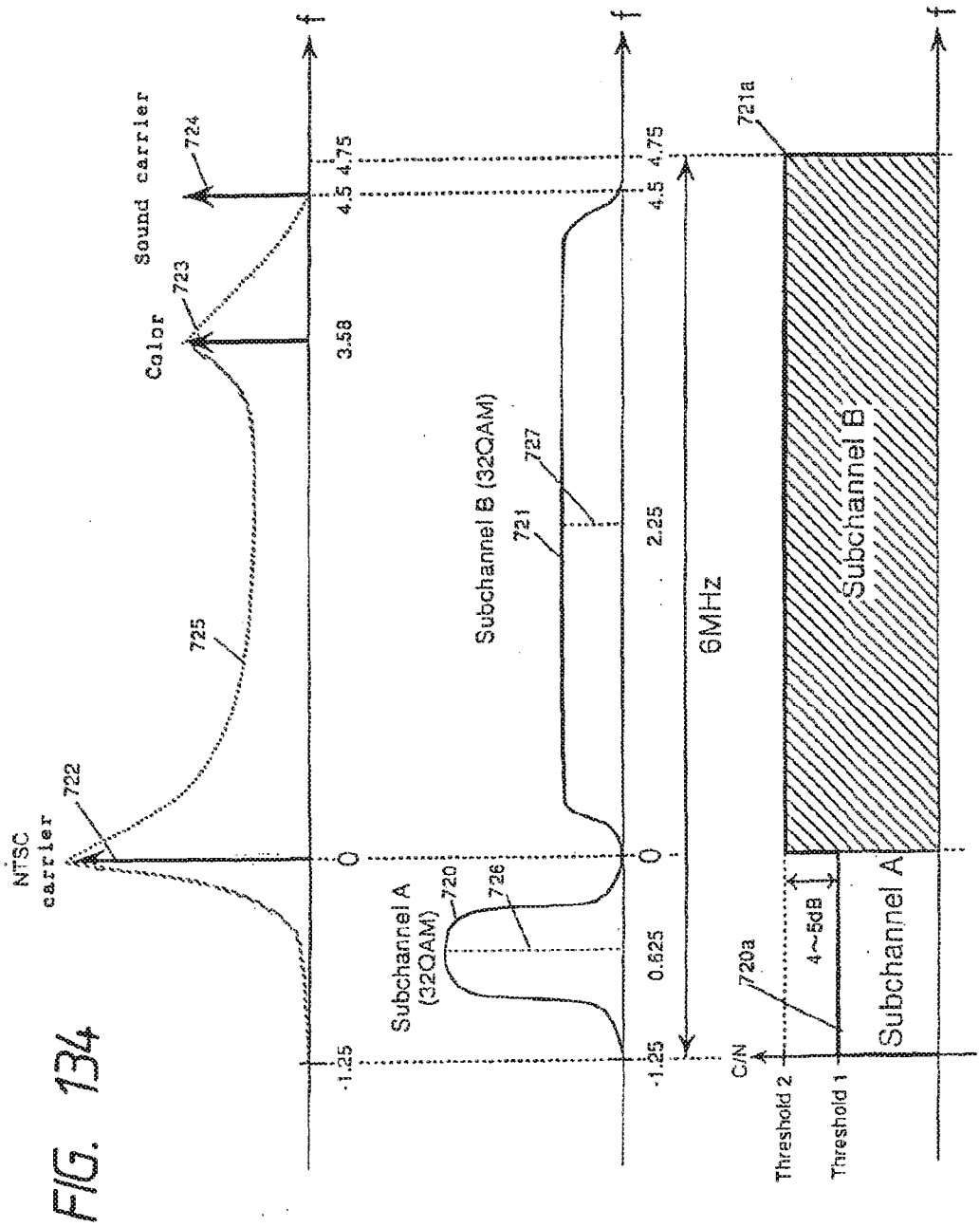


FIG. 13A

FIG. 135

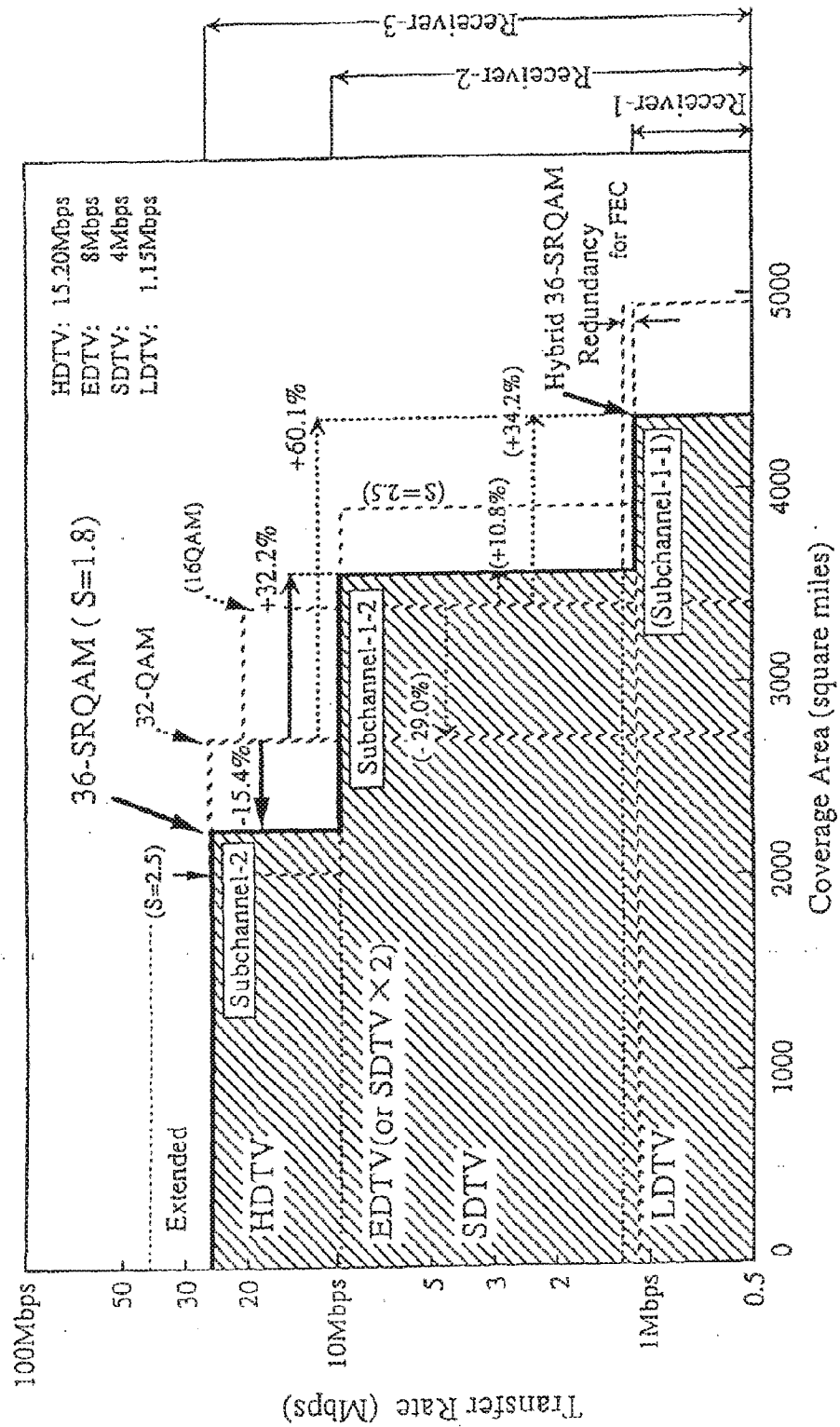


FIG. 136

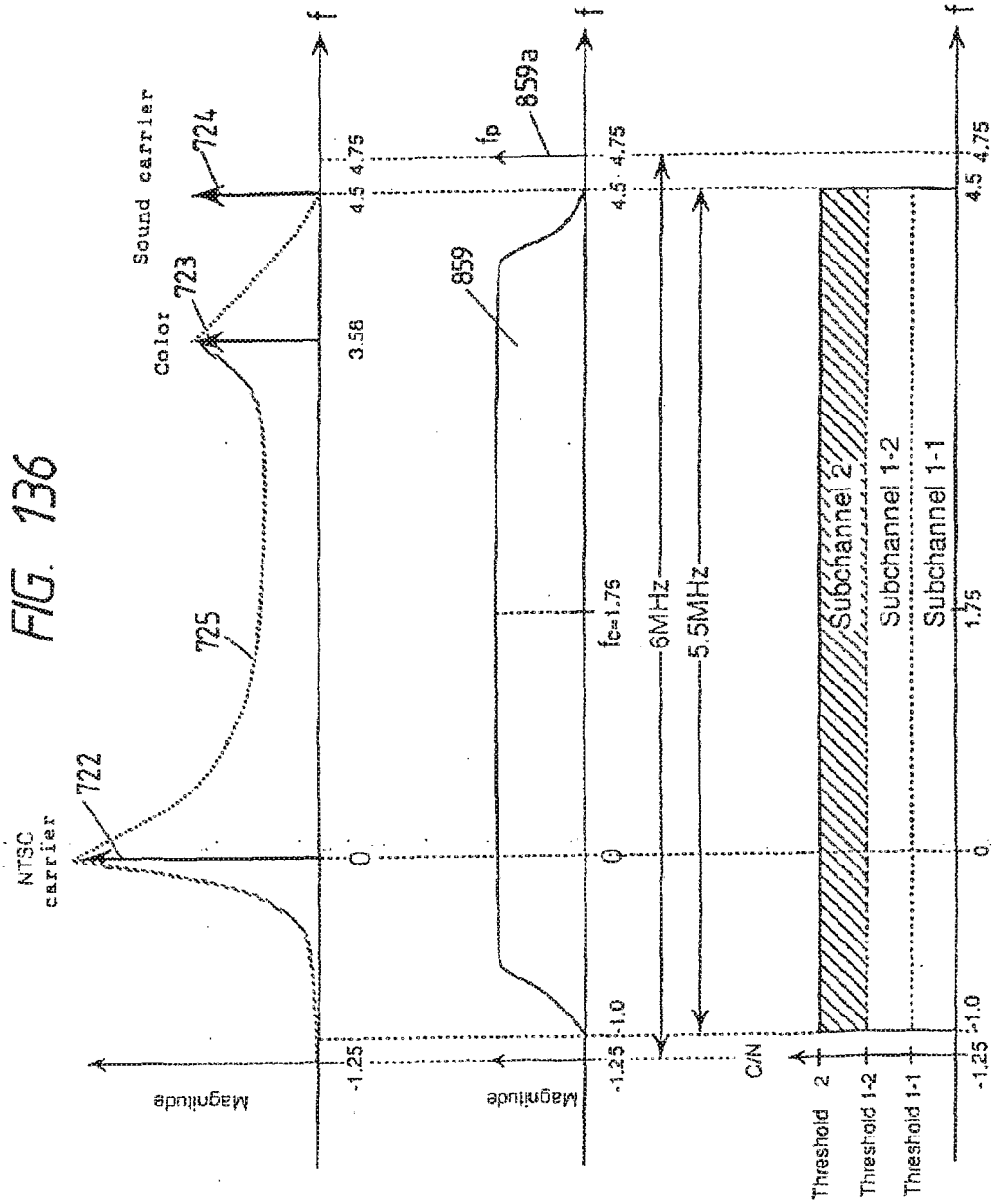


FIG. 137

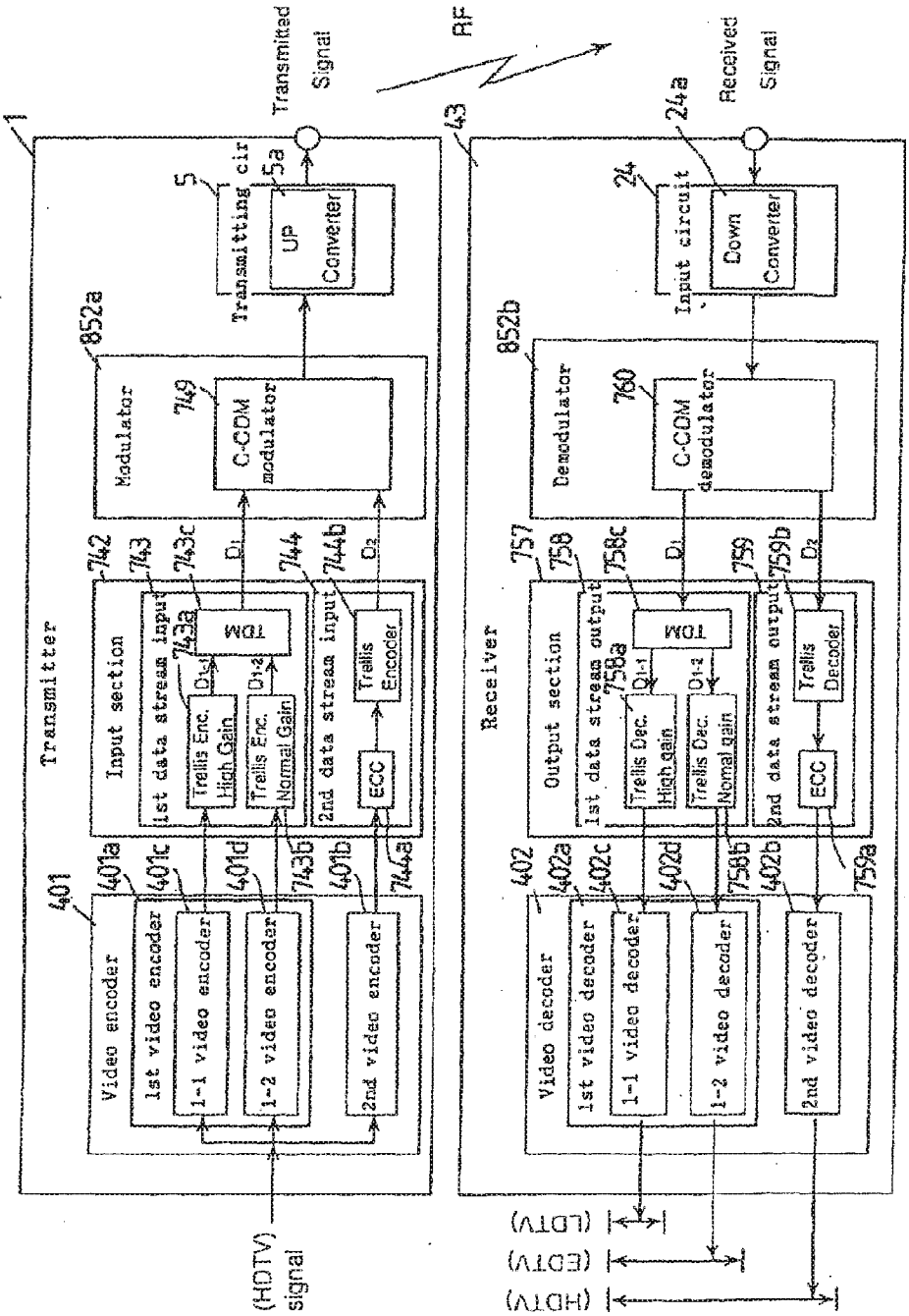
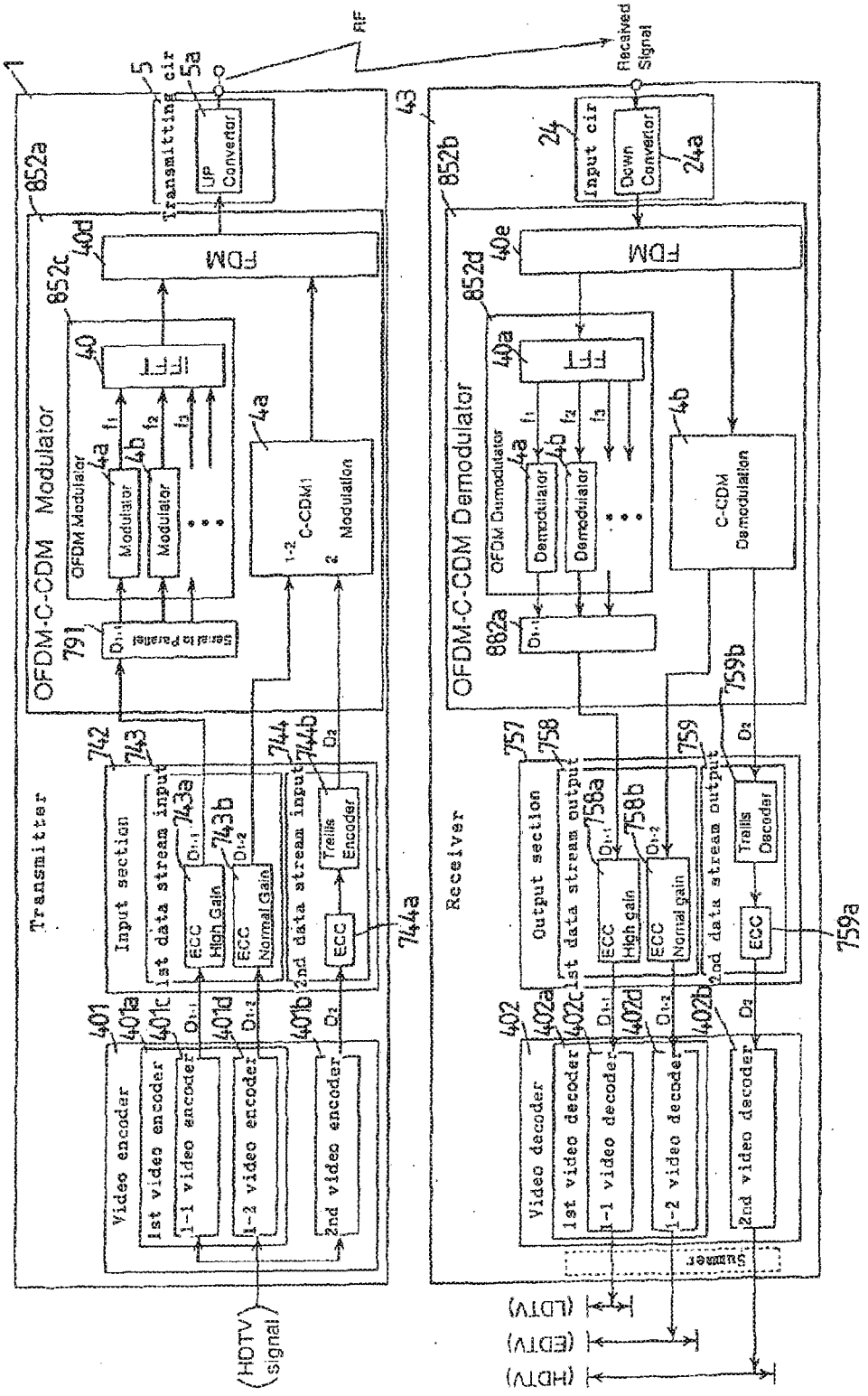


FIG. 138



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(54) Coding for a multilevel transmission system

Kodierung für ein Vielfachpegel-Übertragungssystem

Codage pour un système de transmission à niveaux multiples

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EP-A- 0 282 298
EP-A- 0 490 552
US-A- 4 346 473

- **International Telecommunications Symposium ITS '90, 03.-06.09.1990, Rio de Janeiro, B pages 525-528, IEEE, New York, US; XP245474; J. A. DELGADO-PENIN / A. CORREAS-CORCOBADO: 'Power Spectral Density of a Novel Adaptive Multilevel Line Code.**
- **International Telecommunications Symposium ITS '90, 03.-06.09.1990, Rio de Janeiro, B pages 302-306, IEEE, New York, US; XP245437; E. BIGLIERI / P. MCLANE: 'Multidimensional Signaling for Intersymbol Interference Channels.'**

Description

[0001] The present invention relates to an arrangement for communicating parameter values in a noisy environment.

[0002] Increasing the capacity and robustness to errors of communications and data storage systems have been the object of much research effort. In 'Weighted PCM' by Edward Bedrosian, IRE Transactions on Information Theory, March 1958 a technique is described in which the relative amplitudes of the pulses in a pulse code modulation scheme are adjusted to minimise the noise power of the reconstructed signal due to errors in transmission. In brief, those pulses which have a greater effect on the reconstructed signal are transmitted at a higher amplitude than the others, subject to the constraint that the overall message power transmitted is constant. A performance analysis described in the paper exhibits a significant increase in signal to noise ratio. Such techniques, however, have not been widely used and it has been suggested that this is due to the higher power capability and large number of different quantisation levels required at the transmitter. In addition there has been an increase in emphasis on modulation schemes and error correction coding.

[0003] EP-A-0 490 552 discloses a system for applying unequal error protection to a high definition TV (HDTV) signal. More particularly the system comprises means for dividing the HDTV signal into a plurality of classes of information, separately coding each one of the plurality of classes of information using different coded modulation schemes and multiplexing the plurality of coded outputs for transmission. Each of the coded outputs comprises the sum of the number of bits applied to the modulator plus the number of redundant bits introduced by the encoder. Thus the multiplexer output has a larger overall number of bits compared to those in the original HDTV signal.

[0004] EP-A-0 282 298 discloses a method for combining encoding and modulation of digital information for transmission through an information channel. The method comprises indexing digital signals representative of elementary modulations by indexing vectors to create a decomposition of indexing vectors of an index vector space into a plurality of ordered subspaces, including binary and nonbinary subspaces; associating with each said indexing vector a Euclidean distance in modulation space such that any two modulations whose indexing vectors differ only by a distance vector contained in a first subspace and any preceding (higher significant) subspaces of the series of ordered subspaces are separated in said modulation space by at least said Euclidean distance; and encoding information signals by encoders employing error-correcting codes, each said encoder producing a symbol representative of an indexing vector of the same dimension as a corresponding one of said ordered subspaces for communication of said symbol through said information channel.

[0005] It is an object of the present invention to minimise noise in parameter values which are transmitted to a receiver or stored for later recall.

[0006] According to a first aspect of the present invention there is provided an arrangement for coding a continuous stream of parameter values consisting of a plurality of bits, characterised by means for separating the plurality of bits into at least two sections according to whether they are more or less significant, first means for encoding more robustly a bit in the more significant section as a separate symbol, second means for encoding at least 2 bits in the less significant section as a single symbol, means for combining said symbols produced by said first and second means to produce an output signal in which the duration of the total number of symbols does not exceed the duration of the total number of symbols represented by encoding each bit as a respective symbol.

[0007] The present invention also provides an arrangement for transmitting a continuous stream of parameter values, comprising the arrangement as claimed in Claim 1 together with the additional feature of means for transmitting said output signals.

[0008] The present invention further provides an arrangement for communicating a continuous stream of parameter values, comprising the arrangement as claimed in Claim 1 together with the additional features of means for recovering said output signal, means for separating symbols representative of bits in the more significant section from the remaining symbols in said recovered signal, means for decoding said bits represented by said symbols and means for supplying a plurality of bits in the correct order of significance.

[0009] By generating at least two symbols based upon a digital data word, the more significant bit or bits of the word can be transmitted in a reliable manner using for example bi-level (binary) amplitude modulation or other robust signalling. The less significant bits are considered as one or more sub-sections each representing a larger number of states and these are converted to one or more multi-state symbols for transmission in a shorter time interval than would apply if binary modulation were used. The less significant bits are more prone to error using such a technique but the gain in channel capacity outweighs this disadvantage where parameters or quantised analogue quantities are being transmitted. This gain in channel capacity may be used to improve the channel robustness or to provide extra channels.

[0010] The less significant bits may thus be transmitted using, for example, amplitude modulation, quadrature amplitude modulation (QAM), quadrature phase shift keying (QPSK) or 8-PSK while the more significant bits are transmitted using bi-level or bi-phase modulation, 3-level modulation and so on. Longer words may be separated into a greater number of sub-sections, for example an eight bit digital word may be encoded as four 2-state symbols, a 3-state symbol and an 8-state symbol. A word which is coded in accordance with the present invention may comprise a non-integer

number of bits. The boundaries between bits in the word will not necessarily correspond to the boundaries between symbols.

[0011] The length of time for which a symbol is transmitted also directly affects the likelihood of error. The time saved, compared to a purely bi-level system, by representing the less significant bits of a data word as a multilevel signal having 3 or more levels could be used to increase the duration of the symbol or symbols representing the most significant bit or bits. The duration of such a symbol may conveniently be an integer multiple of the duration of the other symbols used to represent a word but other durations are possible.

[0012] Two symbols may be transmitted simultaneously in different modulation dimensions using, for example, Quadrature Amplitude Modulation or Phase Shift Keying.

[0013] Providing the most robust transmission for the most significant bits of a data word is particularly applicable to a system for communicating digitised analogue signals. For such a purpose, means are provided to digitise the analogue signals at the input to the system and to derive a replica of the digitised signals at the output of the system.

[0014] A four-bit data word may, by use of the present invention, be represented by two 2-state symbols for the two most significant bits and one 4-state symbol for the two least significant bits. The saving in time thus effected may be used to double the length of the symbol representing the most significant bit with a consequent reduction in its susceptibility to error.

[0015] An eight-bit data word may be represented by four 2-state symbols for the four most significant bits and by two further symbols for the remaining bits. For example, the four least significant bits could be represented by two 4-state symbols or by a 3-state symbol and an 8-state symbol. The latter option may be arranged to leave two of the possible states of the 8-state symbol unused which may be used to provide a useful extra clearance between certain adjacent states.

[0016] The allocation of transmission time to particular bits within a word may be made in non-integer subdivision of a clock interval. This may, however, have an effect on successful clock recovery at a receiver.

[0017] The present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block schematic diagram of a data transmission arrangement in accordance with the present invention,

Figure 2 is a block schematic diagram of a data reception arrangement for use with the transmission arrangement of Figure 1,

Figure 3 shows the possible output levels when the transmission arrangement of Figure 1 is used to encode a four bit data word,

Figure 4 is a graph of a comparison of error probability between a standard binary signalling system and an arrangement which uses a four-level symbol,

Figure 5 is a graph of the effect of using a four-level symbol in a multilevel symbol technique on communicated signal to noise ratio at varying channel signal to noise ratios,

Figure 6 is a block schematic diagram of a transmission arrangement in accordance with the invention for transmitting 8-bit data words,

Figure 7 is a block schematic diagram of a reception arrangement for use with the transmission arrangement of Figure 6,

Figure 8 shows the possible output levels of the transmission arrangement of Figure 6,

Figure 9 is a graph of a comparison of error probability between a standard bi-level signalling system and the arrangements of Figures 6 and 7,

Figure 10 is a graph of error probability for a bi-level system and two multilevel techniques coding a 4-bit word using non-integer clock interval multiples, and

Figure 11 is a graph of error probability for a standard bi-level signalling system and a multilevel technique coding an eight-bit word using non-integer clock interval multiples.

[0018] In Figure 1 a four bit digital data word is fed to an input 10 to a splitting device 12 which separates the word into the two most significant bits and the two least significant bits. If the four bit digital word is supplied in a parallel format, the splitting device 12 may be no more elaborate than tracks printed on a circuit board. Where the word is supplied in a serial format the device 12 may comprise a multiplexer. The two most significant bits are fed to a bi-level modulation device 14 which is arranged to provide a signal having a first level if the binary signal is a 'one' and a second level if the binary signal is a 'zero'. Typically these levels will be assigned the arbitrary values of plus one and minus one respectively. The device 14 provides a pair of symbols each of which represents one of the two most significant bits of the data word in a bi-level format and having a length of one clock interval. The two least significant bits are fed to a four-level modulation device 16 which provides an output symbol one clock interval long which represents the two bits as a single symbol which may assume any one of four states. Multilevel modulation is described in greater detail in 'Digital Trans-

mission Systems' by David R. Smith, published by Van Nostrand Reinhold. The modulated symbols are fed to a combining device 18 which places them in an appropriate order for transmission and provides them to a transmitter (Tx) 20 for transmission over a channel. While a transmitter for a radio system is depicted, transmission may be effected over alternative channels, for example a fixed line or an optical fibre link, or the symbols may be stored in an appropriate medium, for example magnetic or optical, for later retrieval.

[0019] Figure 3 shows the possible states of the output of the combining device 18 of Figure 1 during a first clock interval b1, a second clock interval b2 and a third clock interval b3. It is apparent from the drawing that the four-level signal which occupies clock interval b3 has a higher peak amplitude than the two-level signals in the first and second clock intervals. This is so that the symbol transmitted in the third clock interval has the same average power as each of those transmitted in the first two. If it is assumed that the peak amplitude of the multi-level symbol is a, that the levels are equidistant and all equally likely, then $\frac{1}{2}(a^2 + (1/3\ a)^2) = 1$ which gives a = 1.34.

[0020] A more general formula for a is

$$a = \sqrt{3\frac{S-1}{S+1}}$$

where S is the number of states which the symbol may assume. Where the likelihood of occurrence of particular states differs, the average expected power is the sum of the powers of the levels multiplied by their probability of occurrence.

[0021] Figure 2 shows a reception arrangement for use with the arrangement of Figure 1 in which a receiver (Rx) 22 has an output which is coupled to a splitting device 24 having two outputs. A first output is coupled to a demodulator 26 and a second output is coupled to a demodulator 28. The bi-level symbols are demodulated in the demodulator 26 to provide a binary output to a first input of a combining device 30. The four-level symbol is demodulated in the demodulator 28 to provide a binary output to a second input of the combining device 30. The combining device 30 provides a four bit word at an output bus 32. The device 30 may be no more complex than tracks on a printed circuit board if the outputs of the demodulators are in parallel and are active simultaneously.

[0022] Figure 4 shows the error performance of a four level symbol when compared to a pair of bi-level symbols using a root mean square (RMS) error criterion. The horizontal axis S/N is the signal to noise ratio of the channel over which communication is to occur expressed in dB and the vertical axis is the probability of error P expressed in negative powers of ten. The dashed lines 1q, 2q and 3q represent the probabilities of an error of distance 1, (in other words, 1 sent, 2 received, 4 sent, 3 received and so on) distance 2 and distance 3 respectively, using a single four-level symbol. The probability of an error of distance 1 is quite likely but errors of distance 2 or 3 are rather unlikely. The solid lines 1b, 2b and 3b represent the probabilities of an error distance of either 1 or 2 and an error of distance 3, respectively, when using two, 2-level symbols. The probabilities of an error distance of 1 or 2 are virtually equal since these correspond to a single error in the less significant bit and to a single error in the more significant bit respectively. The error probabilities are not quite the same because of the small but finite chance of having an error in both bits, which marginally increases the probability of an error distance of one as a result of the possibility of the corruption from 10b to 01b and vice versa. As can be observed, the likelihood of an error of distance 1 using the two, 2-level symbols is much less likely than when using a single 4-level signal. However, the likelihood of error of distance 2 using the two, 2-level symbols is significantly more likely than when using a 4-level symbol. Where parameters or continuously varying quantities are being transmitted in a digital format, an error in the least significant bit may well go unnoticed but errors in more significant bits may well be intolerable. In such circumstances the performance of the 4-level symbol could well be preferable to that of the two, 2-level symbols.

[0023] Figure 5 shows the communicated (COM) signal to noise (S/N) ratio on the vertical axis against channel (CH) signal to noise ratio on the horizontal axis for a four-bit data word transmitted in four clock intervals as four 2-level symbols (B) and in three clock intervals as two 2-level symbols and a 4-level symbol (M1). At channel S/N ratios of 7 dB or less the communicated S/N ratios are virtually identical but above 7 dB the pure 2-level system has superior performance. Also plotted in the Figure as a broken line is the magnitude of the least significant bit, 6dB x 4 = 24dB. It can be argued that accuracy much greater than that of the least significant value bit is of no practical use when communicating parameter values. Indeed, there will often not have been any greater accuracy in the source signal, which may have been quantised to 4 bits and subject to quantisation noise accordingly. A recovered rms error value that is significantly less than the smallest bit is therefore of little advantage and if it can be traded for another property then it should be. In the case of the multilevel technique here, it has been traded for a reduction in transmission time.

[0024] Figure 5 also shows a curve (M2) which is the communicated S/N ratio against channel S/N ratio for a four-bit data word transmitted as three 2-level symbols and a 4-level symbol, the most significant bit being transmitted as two, 2-level symbols. The performance using this technique is better than that of the three symbol technique at channel S/N ratios of less than approximately 11 dB and better than the four 2-level symbol technique at channel S/N ratios of less than approximately 9 dB. Both of the techniques which use a 4-level symbol are limited in their performance by the pres-

ence of that symbol when a good channel is available.

[0025] Two symbols may be transmitted simultaneously in different modulation dimensions using quadrature channels for example. Consider a three bit word encoded as a 2-level symbol for the most significant bit and a 4-level symbol for the remaining bits. Instead of transmitting the two symbols during different clock intervals, a first quadrature channel can transmit the 2-level symbol and a second quadrature channel can transmit the 4-level symbol. Because of the greater peak amplitude of the 4-level symbol as described previously, the peak amplitude of the signal in the second quadrature channel is greater than that of the first quadrature channel. Thus the two symbols are combined in different modulation dimensions rather than in different clock intervals. Alternatively this symbol combination may be considered as a quadrature amplitude modulated (QAM) signal in which one of the modulation dimensions is weighted differently to the other.

[0026] Using the previous 4 symbol example, one quadrature channel could carry two 2-level symbols representing the most significant bit one symbol after the other while at the same time the other channel could carry the remaining 2-level symbol followed by the 4-level symbol. This is analogous to a QAM arrangement comprising a clock interval containing 4-QAM signal and a clock interval containing an 8-QAM signal with differently weighted modulation dimensions.

[0027] The two symbols representing different respective numbers of states in accordance with the invention may comprise a traditional QAM symbol (having equal interstate separations in the two dimensions) together with a one dimensional multi-level symbol or even a QAM symbol representing fewer states. QAM is described in more detail in the book 'Digital Transmission Systems' identified above. Briefly, in 16-QAM four different levels in each of two different modulation dimensions combine to provide 16 separate states. This modulation may be used for less significant bits of a word while 2-level (or 3-level and so on) modulation is used for the more significant bits. One possible allocation for the values of a digital word applied to a 16-QAM signal is shown as a simple grid, thus:

1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16

[0028] The aim when assigning states to the word values is to arrange for the values of adjacent states of the modulation to provide the minimum RMS error on reception or decoding when adjacent states are mistaken for one another, for example due to noise on a communication channel.

[0029] A 16-QAM signal may be used to represent sixteen states which correspond to four bits of a digital word and so enable longer digital words to be communicated in fewer clock intervals. Alternatively such a signal could be used, for example, to represent ten or twelve different states and error detection or correction coding which is known in the art could be applied to these states to exploit the remaining available states in 16-QAM.

[0030] As a further alternative the 16-QAM symbol may be used to represent fewer than sixteen states without attempting to use all or any of the unused states to provide error coding. The greater distance between certain adjacent states will provide an improvement in performance in its own right. For example, the allocation of 14 of the 16 states as depicted below results in approximately 75% of the RMS error of the allocation of 16 states shown above:

1	2	4	7
3	5		9
6		10	12
8	11	13	14

[0031] Fewer still of the states could be allocated to provide more robust transmission. A coding system in accordance with the invention may thus provide a plurality of 16-QAM signals to encode a word. The more significant bits of the word will be encoded with a less-dense (or sparse) 16-QAM allocation than the less significant bits. Such less-dense QAM allocations can conveniently be considered as one symbol rather than as two symbols in different modulation dimensions since the QAM signal cannot readily be decomposed into symbols representing different numbers of states. Where the smallest interstate separation in the two dimensions differs, this can be considered as two symbols in differ-

ent modulation dimensions even if not every state in those two symbols is allocated.

[0032] The exploitation of multi-dimensional modulation in accordance with the invention may be extended to three dimensions and beyond.

[0033] Figure 6 shows a transmission arrangement in accordance with the present invention for transmitting digitally encoded analogue signals. A source of analogue signals, depicted as a microphone 34 has an output coupled to a code excited linear prediction (CELP) analogue signal coding arrangement 36. Other types of coding arrangement are suitable for use in the transmission arrangement, particularly parameter-based arrangements such as vocoders. The output of the arrangement 36 is a set of digital parameter values comprising up to eight bits each and these are supplied in sequence to a splitting device 38 having three outputs. A first output of the device 38 comprises the four most significant bits of the parameters and this output is fed to a bi-level modulation device 40 which provides four 2-level modulated symbols to a first input of a combining device 46. A second output of the device 38 comprises the fifth and sixth most significant bits of the parameter and is fed to a first multilevel modulation device 42. An output of the device 42 is a three-level symbol which is fed to a second input of the combining device 46. A third output of the device 38 comprises the sixth, seventh and eighth most significant bits of the parameter and is fed to a second multilevel modulation device 44. An output of the device 44 is an 8-level symbol which is fed to a third input of the combining device 46. The device 46 arranges the six symbols into a serial stream and couples them to a transmitter (Tx) 48 for transmission. In this arrangement the four least significant bits, which may represent one of sixteen states are sub-divided into a factor of three represented by a three-level symbol and the factor of six represented by an eight-level symbol. A six-level symbol could be used in place of the eight level symbol. Alternatively, error detection or correction coding could be applied to the least significant bits to provide twenty-four states altogether, thus fully exploiting the states which may be represented by the three-level and the eight-level symbols. More simply the states of the digital word could be applied to the eight-level symbol to maximise the distance of the states from each other and provide more robust coding as described above. Of course certain parameters produced by the arrangements 36 may have no particular weighting towards any of the bits which they comprise and these parameters may be transmitted using a purely 2-level technique or the same multilevel symbols for the whole parameter in the usual manner. The splitting device 38 may thus be arranged to apply the whole of such a parameter to the appropriate modulation device.

[0034] Figure 8 shows the possible states of the output of the combining device 46 (Figure 6) during clock intervals b1 to b6. The 3-level symbol in interval b5 has the effect of decreasing the significance of the following symbol, reducing the level of its error contribution.

[0035] Figure 7 shows a reception arrangement for use with the transmission arrangement of Figure 6. A radio receiver (Rx) 50 has an output which is coupled to a splitting device 52 having three outputs. A first output of the device 52 is fed to a bi-level demodulator 54 and comprises the four 2-level symbols of the received signal. A second output of the device 52 is fed to a 3-level demodulator 56 and comprises the 3-level symbol of the received signal. A third output of the device 52 is fed to an 8-level demodulator 58 and comprises the 8-level symbol of the received signal. Outputs of the three demodulators are fed to respective inputs of a combining device 60 which converts the demodulated signals to a parallel data word. The parallel data word is fed to a CELP analogue signal re-synthesising device 62 whose output is coupled to a transducer, in this case a loudspeaker 64.

[0036] The arrangements of Figures 6 and 7 are applicable to the communication of signals other than analogue signals if the analogue signal encoding and decoding devices are omitted. An eight bit word may thus be transmitted in just six clock intervals. Longer words may also be communicated by selecting appropriate symbols and using more clock intervals.

[0037] Figure 9 shows a graph comparing the performance of the transmission arrangement of Figures 6 and 7 with a system in which all eight bits are encoded as bi-level symbols. The vertical axis (COM) is the communicated S/N ratio of the transmitted signals and the horizontal axis (CH) is the channel S/N ratio. The curve B shows the performance of the bi-level system in 8 clock intervals and the curve M shows the performance of the multilevel technique in 6 clock intervals. As can be seen the performance of the two systems are virtually identical for channel S/N ratios below 11 dB and do not differ to a great extent even at S/N ratios greater than this. As in Figure 5 a broken line is included in the Figure to indicate the limit of useful accuracy, in this case 48dB. As can be seen the multilevel technique produces virtually the same performance up to this limit.

[0038] As an alternative to amplitude modulation, multi-state symbols may be generated by Phase Shift Keying (PSK) where the particular states are modulated at the transmitter as a series of phase or angle variations. Binary PSK is capable of sending one of two possible states per symbol by using one of two signals at relative phase shifts of 0 and π respectively. Quadrature PSK uses relative phase shifts of 0, $\pi/2$, π and $3\pi/2$ radian and 8-PSK uses relative phase shifts of 0, $\pi/4$, $\pi/2$, $3\pi/4$, π, $5\pi/4$, $3\pi/2$ and $7\pi/4$ radian.

[0039] A system in accordance with the invention which uses PSK may comprise the arrangement of Figure 1 in which the modulation devices 14,16 are arranged to provide two binary PSK symbols and a quadrature PSK symbol respectively. The combining device 18 and the Tx 20 are arranged to operate with PSK signals. Similarly the Rx 22, splitting device 24 and demodulation devices 26,28 of Figure 2 are arranged to operate with PSK signals. The use of PSK may

be extended to further multistate symbols such as a combination of binary, quadrature and 8-PSK in a similar manner to that described for multi-level symbols above.

[0040] On reception of PSK signals, when an error is made a signal sent as one state is equally confusable with the two adjacent states as is the case for amplitude modulation. However, there is an additional complication due to the nature of PSK, that of a cyclic error effect, meaning that a phase signal transmitted as 0 radian in 8-PSK may be received as $\pi/4$ radian or $7\pi/4$ radian with equal probability. Thus, if a straightforward allocation were to be made of the eight states represented by the digital word to those of the PSK, there could be an error in transmission of a single phase graduation which would cause a signal transmitted in the first state to be received as a signal in the last state and vice versa. To prevent such a minor error of just one phase graduation from affecting the received value to such an extent the eight states of the word could be allocated to PSK phases as follows:

State	Phase
1	0 rad
3	$\pi/4$
5	$\pi/2$
7	$3\pi/4$
8	π
6	$5\pi/4$
4	$3\pi/2$
2	$7\pi/4$

[0041] Thus a transmission error of one phase graduation, or $\pi/4$, can never result in a perceived error in a digital word having a magnitude of more than two states.

[0042] Different styles of state allocation may be applied to PSK coding using different numbers of states. For example, where a 12-state symbol is used a straightforward allocation would be:

1 2 3 4 5 6 7 8 9 10 11 12

but the RMS error may be reduced by 4dB using the following allocation:

1 2 3 5 6 8 9 11 12 10 7 4.

A further slight improvement can be obtained using:

1 3 5 7 9 11 12 10 8 6 4 2.

[0043] In a similar manner to the above combination of two multi-state symbols in different modulation dimensions, two symbols can be combined in a single PSK signal. For example a 2-state symbol and a 4-state symbol could be combined by allocating 0 radian to one of the states of the 2-state symbol and π radian to the other state. The states of the 4-state symbol could be allocated $-\pi/4$, $-\pi/12$, $+\pi/12$ or $+\pi/4$ respectively. A combination of the two symbols results in an eight state symbol with unequal interstate graduations. There is a minimum angle of $\pi/2$ between the states of the 2-state symbol and a minimum angle of $\pi/6$ between the states of the 4-state signal, thus providing different degrees of protection to the most significant bit and the remaining bits.

[0044] As was observed earlier, with reference to Figure 5, representing the most significant bit by more than one symbol has quite a noticeable effect on the performance of the system when compared with a most significant bit communicated in just one clock interval. This effect can be extended to alteration of the duration of all of the symbols to be transmitted.

[0045] In the case of the four-bit word, the saving of one clock interval by using multiple symbol signalling as opposed to a pure 2-level system, can be used to extend the duration of the three symbols by a factor a 4/3. The channel noise will be reduced by 10 log [4/3] = 1.25 dB with a consequent improvement in the sensitivity of the communication system. However there may be problems with clock recovery at the receiving end of the system.

[0046] Alternatively the duration of the symbols can be made different from each other. One possible allocation of 4 clock intervals to a four-bit word is:

Message bit	Symbol	Symbol Duration
1 (MSB)	bi-level	2.25
2	bi-level	1.25
3	4-level	0.5
4		

[0047] To transmit a four-bit word in three clock intervals, a possible allocation is:

Message bit	Symbol	Symbol Duration
1 (MSB)	bi-level	1.6
2	bi-level	0.9
3	4-level	0.5
4		

[0048] Figure 10 shows the communicated S/N ratio (COM) on the vertical axis against the channel S/N ratio (CH) on the horizontal axis for a pure bi-level symbol scheme (B), the four clock interval (M1) scheme and three clock interval (M2) scheme above. By comparison with Figure 5 the improvement in performance of the non-integer clock interval allocations over a system in which the symbol edges coincide with the clock interval boundaries can be seen. The four clock interval scheme has a sensitivity of 1.7 dB better than the pure bi-level scheme while even the three clock interval scheme can out-perform the pure bi-level system, despite occupying only three quarters of the transmission time. As before, a limit of useful accuracy is shown by a broken line at 24dB communicated S/N.

[0049] Unequal symbol durations can be applied to a system for encoding an 8-bit data word in 8 clock intervals. One possible allocation is as follows:

Message bit	Symbol	Symbol Duration
1 (MSB)	bi-level	1.78
2	bi-level	1.47
3	bi-level	1.21
4	bi-level	0.95
5	3-level	1.64
6		
7	8-level	0.95
8		

[0050] Figure 11 shows a graph of communicated S/N ratio (COM) on the vertical axis against channel S/N ratio (CH) on the horizontal axis for the pure 2-level symbol scheme (B) and the multiple-level symbol scheme (M). The pure 2-level scheme can be seen to provide inferior performance to the multiple-level symbol scheme M at channel S/N ratios below approximately 12.5 dB. In very poor channels the error values are maintained using the multiple-level symbol scheme with channel S/N ratios of up to 2 dB worse than the pure 2-level scheme. As previously, the limit of useful accuracy, 48dB, is shown in a broken line.

[0051] As an alternative to non-coincident symbol durations and clock intervals, the communication time saved by the invention may be used to apply error correction or detection codes to the more significant bits of the digital word. One suitable code would be a convolutional code which provides two output bits for each input bit. Other coding techniques, such as Hamming Codes may be applied. Error detection or correction coding bits for those more significant bits, which are probably communicated as two-state symbols, may be arranged to be communicated with the less significant bits as part of a multi-state symbol.

[0052] From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the design, manufacture and use of systems for communicating digital data words and component parts thereof and which may be used instead of or in addition to features already described herein.

Claims

1. An arrangement for coding a continuous stream of parameter values consisting of a plurality of bits, characterised by means (12,36) for separating the plurality of bits into at least two sections according to whether they are more or less significant, first means (14,40) for encoding more robustly a bit in the more significant section as a separate symbol, second means (16,44) for encoding at least 2 bits in the less significant section as a single symbol, means (18,46) for combining said symbols produced by said first and second means to produce an output signal in which the duration of the total number of symbols does not exceed the duration of the total number of symbols represented by encoding each bit as a respective symbol.

2. An arrangement as claimed in claim 1, characterised in that said second means (16,44) encodes a plurality of bits as a single multi-level symbol.

3. An arrangement as claimed in claims 1 or 2, characterised in that the first and second means (14,16,40,44) produce symbols having a substantially equal average power.

4. An arrangement as claimed in any one of claims 1 to 3, characterised in that each symbol is of substantially equal duration.

5. An arrangement as claimed in any one of claims 1 to 3, characterised in that the first means (14,40) encodes the most significant bit as two symbols.

6. An arrangement as claimed in any one of claims 1 to 3, characterised in that the symbols produced by said first means (14,40) are of a longer duration than the symbols produced by said second means (16,44).

7. An arrangement for transmitting a continuous stream of parameter values consisting of a plurality of bits, comprising an arrangement as claimed in any one of claims 1 to 6 and means (20,48) for transmitting said output signal.

8. An arrangement as claimed in claim 7, characterised in that the transmitting means (20, 48) comprises a phase shift keying transmitting means for transmitting at least one symbol from said first means (14,40) simultaneously with at least one symbol from said second means (16,44).

9. An arrangement for communicating a continuous stream of parameter values consisting of a plurality of bits, comprising an arrangement as claimed in any one of claims 1 to 6, means(22,50) for recovering said output signal, means for separating symbols representative of bits in the more significant section from the remaining symbols in said recovered signal, means (26,28,54,58) for decoding said bits represented by said symbols and means (30,60) for supplying a plurality of bits in the correct order of significance.

10. An arrangement as claimed in Claim 9, characterised in that the combining means (18,46) comprises transmitting means for transmitting at least one symbol from said first means (14,40) simultaneously with at least one symbol from said second means (16,44).

Patentansprüche

1. Anordnung zur Codierung eines kontinuierlichen Stroms von Parameterwerten, die aus einer Vielzahl von Bits bestehen, dadurch gekennzeichnet, dass sie folgendes enthält: Mittel (12, 36) zum Aufteilen der Vielzahl von Bits in mindestens zwei Abschnitte, je nachdem, ob sie eine höhere oder eine geringere Wertigkeit aufweisen; erste Mittel (14, 40) zum zuverlässigeren Codieren eines Bits in dem Abschnitt mit höherer Wertigkeit als ein getrenntes Symbol; zweite Mitte (16, 44) zum Codieren von mindestens 2 Bits in dem Abschnitt mit geringerer Wertigkeit als ein einziges Symbol; Mittel (18, 46) zum Kombinieren der durch die genannten ersten und zweiten Mittel erzeugten Symbole, um ein Ausgangssignal zu erzeugen, wobei die Dauer der Gesamtzahl der Symbole nicht die Dauer der Symbole überschreitet, die durch Codieren jedes Bits als ein entsprechendes Symbol dargestellt werden.

2. Anordnung nach Anspruch 1, dadurch gekennzeichnet, dass die genannten zweiten Mittel (16, 44) eine Vielzahl von Bits als ein einziges Vielfachpegelsymbol codieren.

3. Anordnung nach Anspruch 1 oder 2, dadurch gekennzeichnet, dass die ersten und zweiten Mittel (14, 16, 40, 44) Symbole mit einer im wesentlichen gleichen Durchschnittsleistung erzeugen.

4. Anordnung nach einem der Ansprüche 1 bis 3, dadurch gekennzeichnet, dass jedes Symbol im wesentlichen die gleiche Dauer hat.

5. Anordnung nach einem der Ansprüche 1 bis 3, dadurch gekennzeichnet, dass die ersten Mittel (14, 40) das Bit mit der höchsten Wertigkeit als zwei Symbole codieren.

6. Anordnung nach einem der Ansprüche 1 bis 3, dadurch gekennzeichnet, dass die von den genannten ersten Mitteln (14, 40) erzeugten Symbole eine längere Dauer als die von den genannten zweiten Mitteln (16, 44) erzeugten Symbole haben.

7. Anordnung zum Übertragen eines kontinuierlichen Stroms von aus einer Vielzahl von Bits bestehenden Parameterwerten, die eine Anordnung nach einem der Ansprüche 1 bis 6 und Mittel (20, 48) zum Übertragen des genannten Ausgangssignals enthält.

8. Anordnung nach Anspruch 7, dadurch gekennzeichnet, dass die Übertragungsmittel (20, 48) Übertragungsmittel mit Phasenumtastung enthalten, um mindestens ein Symbol von den genannten ersten Mitteln (14, 40) gleichzeitig mit mindestens einem Symbol von den genannten zweiten Mitteln (16, 44) zu übertragen.

9. Anordnung zum Übertragen eines kontinuierlichen Stroms von aus einer Vielzahl von Bits bestehenden Parameterwerten, die folgendes beinhaltet: eine Anordnung nach einem der Ansprüche 1 bis 6, Mittel (22, 50) zum Wiederherstellen des genannten Ausgangssignals, Mittel zum Trennen der Bits in dem Abschnitt mit höherer Wertigkeit darstellenden Symbole von den übrigen Symbolen in dem genannten wiederhergestellten Signal, Mittel (26, 28, 54, 58) zum Decodieren der genannten durch die genannten Symbole dargestellten Bits und Mittel (30, 60) zum Liefern einer Vielzahl von Bits in der richtigen Reihenfolge der Wertigkeit.

10. Anordnung nach Anspruch 9, dadurch gekennzeichnet, dass die Kombinationsmittel (18, 46) Übertragungsmittel zum gleichzeitigen Übertragen von mindestens einem Symbol von den genannten ersten Mitteln (14, 40) gleichzeitig mit mindestens einem Symbol von den genannten zweiten Mitteln (16, 44) enthalten.

Revendications

1. Montage pour codage d'un train continu de valeurs paramétriques constitué d'une pluralité de bits, caractérisé par un moyen (12,36) pour séparer la pluralité de bits en au moins deux sections selon qu'ils soient plus ou moins significatifs, un premier moyen (14,40) servant à coder plus solidement un bit dans la section la plus significative sous forme de symbole séparé, un deuxième moyen (16,44) servant à coder au moins deux bits dans la section la moins significative en un symbole unique, un moyen (18,46) pour combiner lesdits symboles produits par ledit premier et ledit deuxième moyens pour produire un signal de sortie dans lequel la durée du nombre total de symboles ne dépasse pas la durée du nombre total de symboles représentés en codant chaque bit sous la forme d'un symbole respectif.

2. Montage selon la revendication 1, caractérisé en ce que ledit deuxième moyen (16,44) code une pluralité de bits sous la forme d'un symbole unique à niveaux multiples.

3. Montage selon les revendications 1 ou 2, caractérisé en ce que le premier et le deuxième moyens (14,16,40,44) produisent des symboles ayant une puissance moyenne sensiblement égale.

4. Montage selon l'une quelconque des revendications 1 à 3, caractérisé en ce que chaque symbole est de durée sensiblement égale.

5. Montage selon l'une quelconque des revendications 1 à 3, caractérisé en ce que le premier moyen (14,40) code le bit le plus significatif sous la forme de deux symboles.

6. Montage selon l'une quelconque des revendications 1 à 3, caractérisé en ce que les symboles produits par ledit premier moyen (14,40) ont une durée plus longue que les symboles produits par ledit deuxième moyen (16,44).

7. Montage pour la transmission d'un train continu de valeurs paramétriques comprenant une pluralité de bits, comprenant un montage selon l'une quelconque des revendications 1 à 6 et un moyen (20,48) pour transmettre ledit signal de sortie.

8. Montage selon la revendication 7, caractérisé en ce que le moyen de transmission (20,48) comprend un moyen de transmission à modulation par déplacement de phase pour transmettre au moins un symbole dudit premier moyen (14,40) simultanément avec au moins un symbole dudit deuxième moyen (16,44).

9. Montage pour transmettre un train continu de valeurs paramétriques comportant une pluralité de bits, comprenant un montage selon l'une quelconque des revendications 1 à 6, un moyen (22,50) pour récupérer ledit signal de sortie, un moyen pour séparer des symboles représentatifs de bits de la section la plus significative des symboles restant dans ledit signal récupéré, un moyen (26,28,54,58) pour décoder lesdits bits représentés par lesdits symboles et un moyen (30,60) pour délivrer une pluralité de bits dans l'ordre correct de signification.

10. Montage selon la revendication 9, caractérisé en ce que le moyen de combinaison (18,46) comprend un moyen de transmission pour transmettre au moins un symbole dudit premier moyen (14,40) simultanément avec au moins un symbole dudit deuxième moyen (16,44).

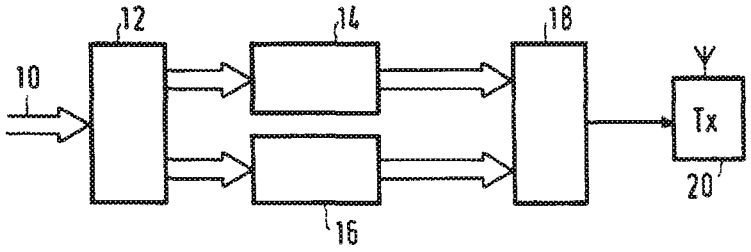

FIG.1

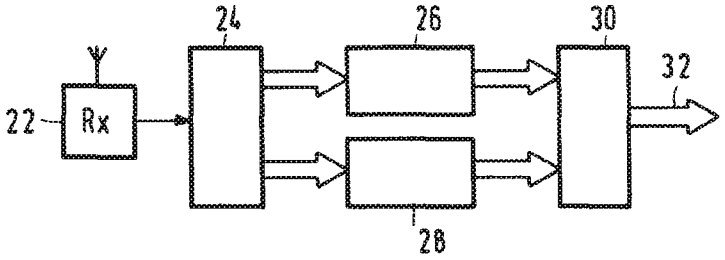

FIG.2

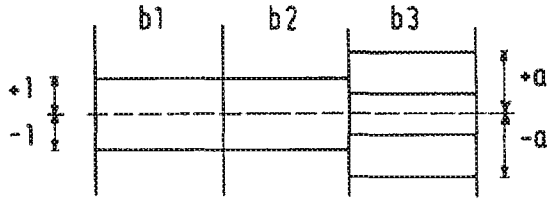

FIG.3

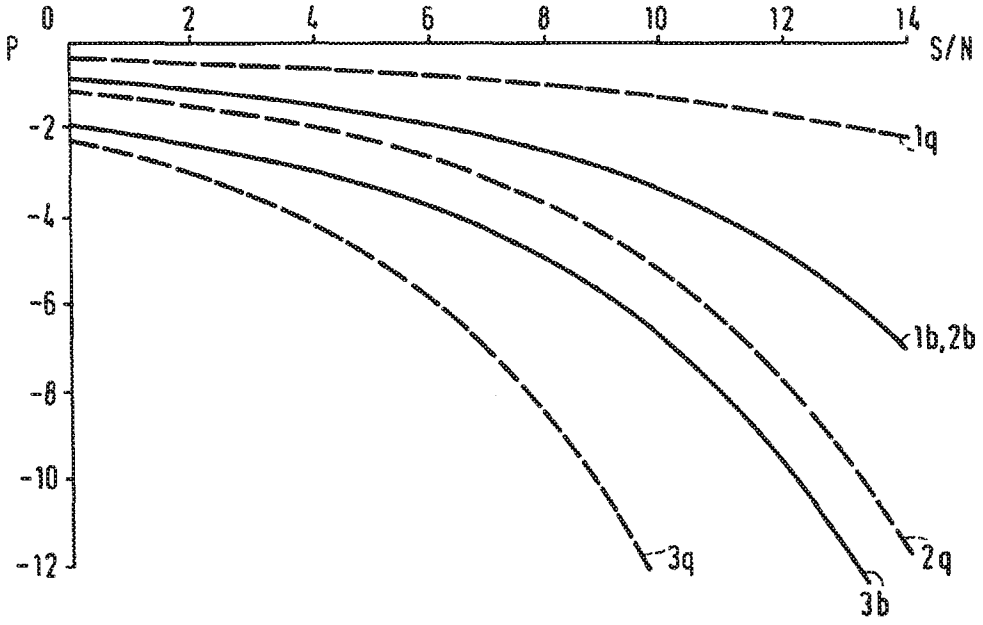

FIG.4

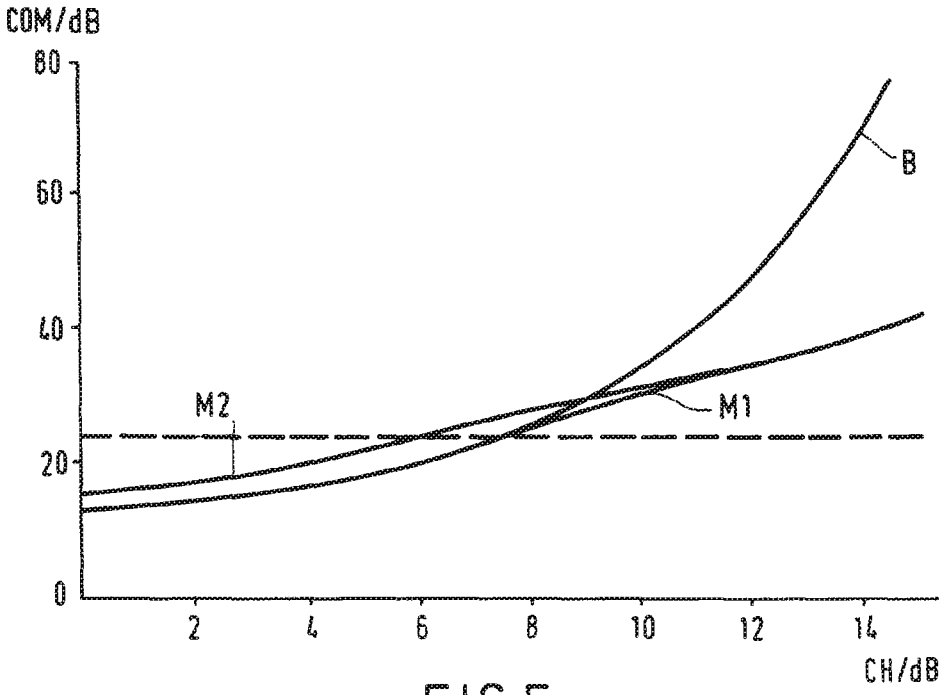

FIG.5

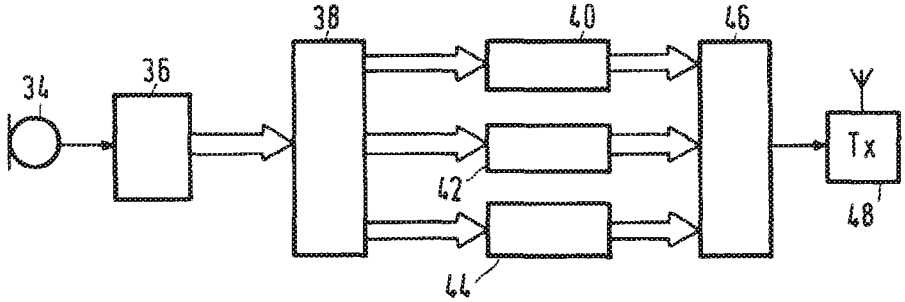

FIG.6

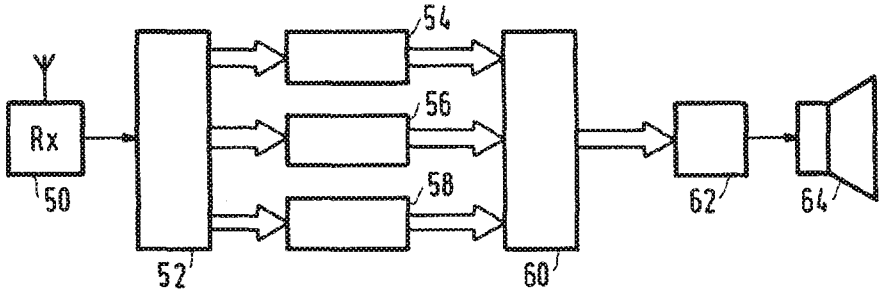

FIG.7

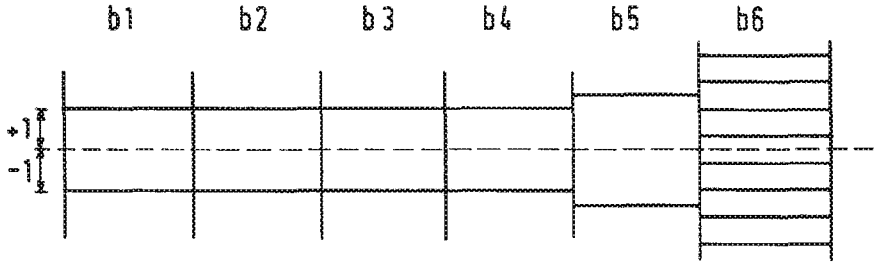

FIG.8

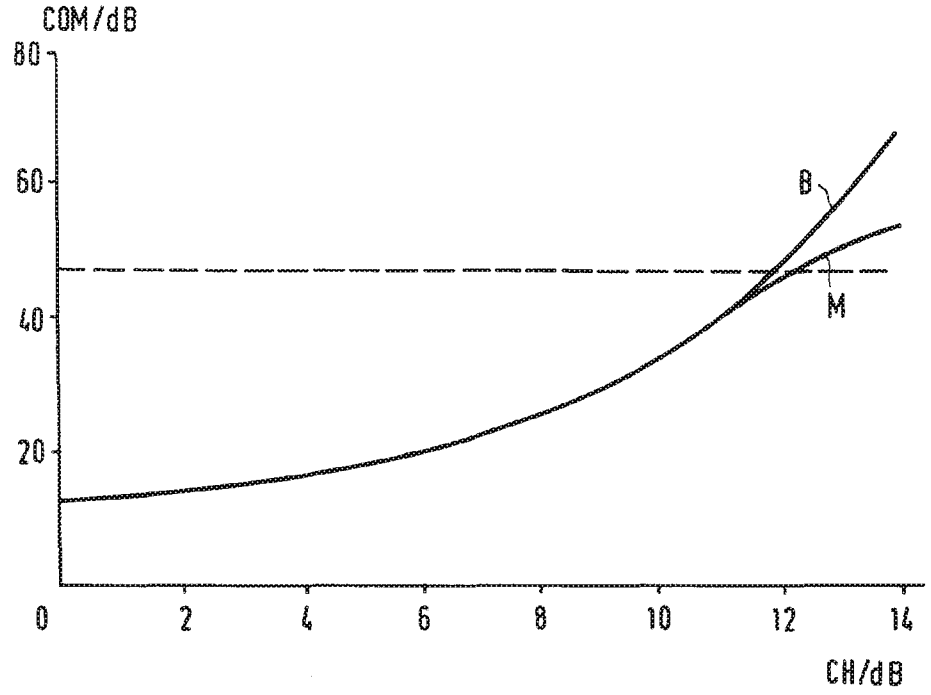

FIG.9

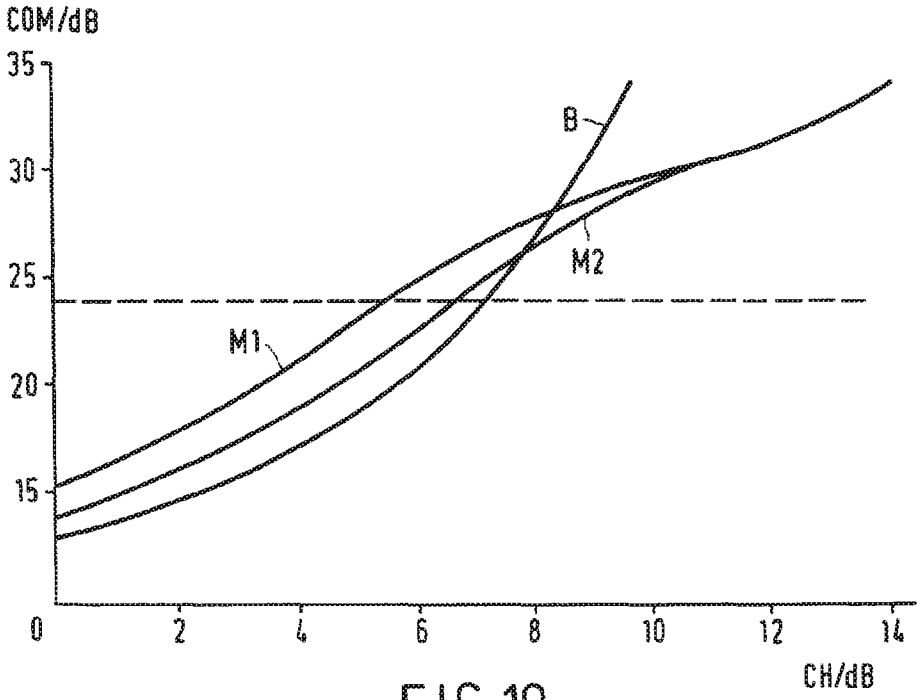

FIG.10

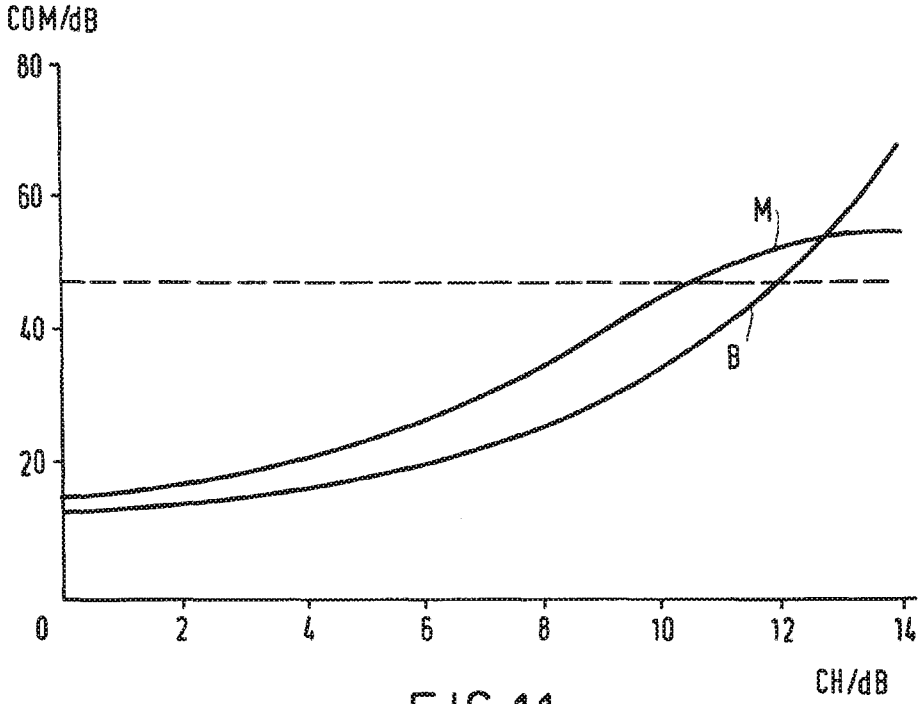

FIG.11

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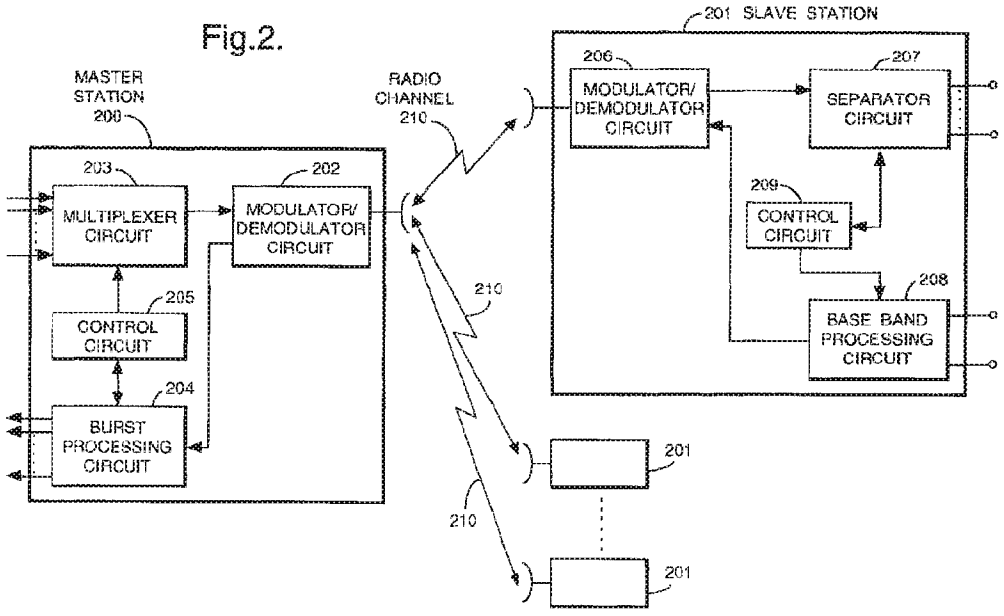
(54) Time-division multidirectional multiplex communication system capable of using message area in radio burst signals divided into a plurality of areas

(57) A master station and at least one slave stations are connected by radio channels, and each slave station transmits data to the master station by time division multiple access. First means equally divides a prescribed area, which is defined in a burst signal for use in transmission from each slave station to the master station and intended for arrangement of message signals sent from at least one terminal connected to the slave station, into at least two sub-areas, and arranges a message signal in each sub-area. Second means generates a burst signal, in which at least a control signal and a channel quality monitoring signal are arranged, in the area peripheral to each sub-area in which a message signal is arranged. Here the prescribed area in the burst signal is an area corresponding to a data quantity of 64 kbps in transmission speed. The data quantity of the message signal arranged in that area corresponds to data of 32 kbps, 16 kbps or 8 kbps in transmission speed.

Fig.2.



EP 0 700 175 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 30 6007

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 444 592 A (NIPPON ELECTRIC CO) 4 September 1991 (1991-09-04) * column 1, line 1 - line 9; claim 3; figures 1,2 * * column 4, line 33 - line 51 * * column 5, line 36 - line 40 * * column 10, line 15 - line 17 * * column 6, line 46 - column 7, line 12 *	1,5,10, 14,17, 20,24	H04B7/26 H04B7/212
Y	* column 5, line 36 - line 40 *	2-4,6-9, 11-13, 15,16, 18,19, 21-23	
Y	EP 0 587 225 A (PHILIPS ELECTRONICS UK LTD ;PHILIPS ELECTRONICS NV (NL)) 16 March 1994 (1994-03-16) * page 3, line 15 - line 42; claim 1; figure 2 * * page 5, line 7 - line 15 * * page 4, line 40 - line 51 *	2-4,6-9, 11-13, 15,16, 18,19, 21-23	
A	US 5 251 217 A (TRAVERS JEAN-FRANCOIS ET AL) 5 October 1993 (1993-10-05) * column 2, line 40 - line 47; figure 1 *	1-24	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
H04B
H04J
H04Q

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	29 February 2000	Felsen, J

CATEGORY OF CITED DOCUMENTS
X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 95 30 6007

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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29-02-2000

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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Office européen des brevets

(11) EP 0 730 251 B1

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(21) Application number: **96102276.1**

(22) Date of filing: **15.02.1996**

(54) **Non-contact type IC card and system therefor**

Kontaktlose IC-Karte und System dafür

Carte à circuit intégré sans contact et système pour une telle carte

(84) Designated Contracting States:
DE FR GB

(30) Priority: **03.03.1995 JP 4431595**

(43) Date of publication of application:
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(60) Divisional application:
01120575.4 / 1 170 696

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Description

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001] The present invention relates to a non-contact type IC card for carrying out the data transmission and reception through a radio wave or the like, and a non-contact type IC card system including the same IC card.

DESCRIPTION OF THE RELATED ART

[0002] Fig. 15 is a block diagram schematically showing an arrangement of a known non-contact type IC card system. In Fig. 15, the system is shown as comprising a non-contact type IC card (which will hereinafter be referred to as a card) 1, a reader writer unit (which will hereinafter be referred to as an R/W) 2 for the data transmission and reception through a radio wave to and from the card 1, and a host computer 3 coupled through a cable C (wire-based signal transmission and reception system) to the R/W 2 for control.

[0003] The card 1 is composed of an antenna 4 for transmission and reception, a modulating circuit 5 for the modulation of the transmission data, a demodulating circuit 6 for the demodulation of the received data, a rectification and voltage control circuit 7 for rectifying an alternating current signal from the transmission and reception antennas 4 and further for regulating the rectified signal to a desired operating voltage which in turn, is supplied to the respective sections, and an E^2PROM 9 for storage of programs and data. Also included in the card 1 is a control section 8 comprising a CPU (not shown), a memory (not shown) for storing programs for operating the CPU, and others.

[0004] Further, the R/W 2 includes a transmission and reception antenna 21, a modulation and demodulation circuit 22 for the modulation of the data being transmitted and the demodulation of the received data, and a control section for controlling the data transmission. An R/W 2 side CPU and a program for the operation of the CPU are provided in the control section 23 or the host computer 3. For this reason, the R/W 2 and the host computer 3 can be considered as one unit, which is sometimes generally called an R/W.

[0005] In operation, the card 1 and the R/W 2 are not in electrically connecting relation to each other through a cable or the like, but the transmission and reception of the data therebetween are accomplished through a radio wave EM. The R/W 2 comes into connection with the host computer 3 through the cable C to be operable under control of the host computer 3.

[0006] Recently, there has been known a product which rectifying a radio wave from the R/W 2 within the card 1 for the generation of an operating voltage. In this instance, the card 1 incorporates the rectifying and voltage control circuit 7, and accepts, through the transmission and reception antenna 4, a radio wave from an external unit such as the R/W 2 so that the rectifying and voltage control circuit 7 produces a desired operating voltage to supply a power to the respective internal circuits (functional blocks), thus operating the card 1.

[0007] In the card 1, the reception of the data from the R/W 2 is conducted with the transmission and reception antenna 4 and the received data is demodulated in the demodulating circuit 6 and then inputted into the control section 8. The control section 8 decodes the data from the R/W 2 and implements an operation in accordance with the decoded results.

[0008] For example, when an ID code is outputted to the external, the ID code stored in advance in the E^2PROM 9 serving as a data memory is modulated in the modulating circuit 5 and transmitted through the transmission and reception antenna 4 to the R/W 2 in the form of the radio wave EM. On the other hand, when the data is written in the card 1, the data is written into the E^2PROM 9 under the control of the control section 8.

[0009] In the R/W 2, under the control of the host computer 3 coupled thereto, the control section 23 controls the modulation and demodulation circuit 22 for the transmission and reception of the data. The modulation and demodulation circuit 22 combines a modulation circuit and a demodulation circuit, and the data transmission is accomplished through the modulation and demodulation circuit 22 from the transmission and reception antenna 21 in both the data transmission and reception.

[0010] In addition, as shown in Fig. 16, as the typical data modulating method, there have been known the following three methods. That is, the first is the ASK (Amplitude Shift Keying) modulation where the data "1/0" are made to correspond with two kinds of amplitudes, the second is the FSK (Frequency Shift Keying) modulation where the data "1/0" are made to correspond with two kinds of frequencies, and the third is the PSK (Phase Shift Keying) modulation where the data "1/0" are made to correspond with the presence and absence of the phase variation of the radio wave.

[0011] Known non-contact type IC cards can generally deal with only one of the aforesaid modulation methods. For instance, a communication unit which performs the data transmission and reception in accordance with the FSK modulation method has been disclosed in the Japanese Published Unexamined Patent Application No. 5-210768, and this prior art can realize the data transmission and reception on the basis of the FSK modulation while not realizing the data transmission and reception on the basis of the other modulations. Further, the Japanese Published Unexamined Patent Application No. 5-143792 discloses a method of transmitting both the data and power through radio waves. However, as well as the first-mentioned prior art, this prior art adopts the ASK modulation method and therefore can not accommodate the other modulation methods.

[0012] As described above, the known non-contact type IC cards can generally accepts only one of the

aforesaid modulation methods, for that the circuit arrangement is different at every modulation method and, for accommodating a plurality of modulation methods, the circuit arrangement becomes complicated and large in size. That is, difficulty is experienced to independently place plural kinds of modulation circuits within the size-limited card, and hence this arrangement has not been realized heretofore. For this reason, the known non-contact type IC card is limited in use to a system having the same modulation method as that of the IC card so that there is a problem that limitation is imposed on the use range.

SUMMARY OF THE INVENTION

[0013] The present invention has been developed in order to eliminate the above-mentioned problems, and it is therefore an object of the present invention to provide a non-contact type IC card which is capable of the data transmission based on a plural kinds of modulation methods and a system including this card.

[0014] Another object of this invention is to provide a data transmission method with a higher reliability for a non-contact IC card system.

[0015] In accordance with a first aspect of this invention, there is provided a non-contact type IC card using a radio wave as a communication medium, comprising antenna means for transmission and reception of data, modulation means for modulating a transmission data in accordance with PSK- and FSK-modulation methods by switching a resonance frequency of the antenna means to suit the transmission data, PSK/FSK switching means for performing a switching operation so that the modulating means conducts one of the PSK- and FSK-modulations, demodulation means for demodulating data received by the antenna means, and control means for controlling the aforesaid means.

[0016] According to the first aspect of this invention, the non-contact type IC card is equipped with a simple circuit comprising a resonance frequency switching section for switching the resonance frequency of the antenna means and a modulation circuit for driving the switching section, and a PFSEL switch of the modulation circuit is only coupled to the VDD or GND. Thus, one card can select one of the PSK modulation and the FSK modulation and further is applicable in a wide range.

[0017] In accordance with a second aspect of this invention, in the first aspect the modulation means further comprises a first modulating section for performing the PSK- and FSK-modulations at a first modulating timing, a second modulating section for performing the PSK- and FSK-modulations at a second modulating timing, and modulation timing switching means for changing the modulation timing by switching a circuit between the first and second modulating sections.

[0018] In the non-contact type IC card according to the second aspect of this invention, the modulation method is selectable (can be selected) between the PSK modulation and the FSK modulation, and the modulation timing for the data being transmitted is switchable (can be switched) between a modulation timing at which the modulation is accomplished in response to the inversion of the transmission data "0/1" and a modulation timing at which the modulation is always accomplished, for example, when the data being transmitted is "0", thus permitting the card to deal with more data communication specifications.

[0019] In accordance with a third aspect of this invention, a non-contact type IC card system comprises a non-contact type IC card having the aforementioned first and second aspects and a reader writer including antenna means for performing transmission and reception of data to and from the IC card, modulation and demodulation means for carrying out modulation and demodulation of data transmitted and received through the antenna means, and control means for controlling the aforesaid means.

[0020] In the non-contact IC card system according to the third aspect of this invention, the modulation method in the card is selectable from the PSK modulation method and the FSK modulation method, besides the modulation timing of the data being transmitted is arranged to be switchable in some type of the card, with the result that the relationship between the R/W and the card becomes more flexible to realize a system more expandable in the card application range.

[0021] In accordance with a fourth aspect of this invention, in the reader writer of the third aspect, the antenna means comprises an antenna for data transmission and an antenna for data reception which are separately provided.

[0022] In the non-contact IC card system according to the fourth aspect of this invention, the antenna means is divided into the transmission antenna and the reception antenna to offer two kinds of antenna characteristics for the transmission and the reception, by which arrangement the transmission antenna can retain the antenna characteristic developing a transmission power while the reception antenna can have an antenna sensitivity subject to a weak or faint radio wave, which can realize a non-contact type IC card system capable of the data transmission and reception accomplishing a long communication distance.

[0023] In accordance with a fifth aspect of this invention, in the third or fourth aspect the reader writer employs the PSK modulation at data transmission and the non-contact type IC card employs the FSK modulation at data transmission.

[0024] In the non-contact type IC card system according to the fifth aspect of this invention, the data transmission from the R/W to the card is implemented on the basis of the PSK modulation, whereas the data transmission from the card to the R/W is achieved on the basis of the FSK modulation. With this arrangement, since there is no need for a complicated demodulating circuit for the FSK modulation to be incorporated in the card,

the demodulating circuit within the card is designed to correspond with the PSK modulation, with the result that the size reduction and price reduction of the card becomes possible. In addition, since the R/W side carries out the demodulation for the FSK modulation, a non-contact type IC card system can be realized so that even a radio wave with a higher frequency is receivable.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] The object and features of the present invention will become more readily apparent from the following detailed description of the preferred embodiments taken in conjunction with the accompanying drawings in which:

Fig. 1 is a block diagram showing an arrangement of a non-contact type IC card according to an embodiment of this invention;
Fig. 2 is an illustration of arrangements of a transmission and reception antenna, a resonance frequency switching section and a modulation circuit of the Fig. 1 card;
Fig. 3 is an illustration of one example of the modulation circuit in Fig. 1;
Figs. 4A and 4B are time charts available for description of an operation of the Fig.3 modulation circuit;
Fig. 5 is a block diagram showing an arrangement of a non-contact type IC card according another embodiment of this invention;
Fig. 6 is an illustration of one example of the Fig. 5 modulation circuit;
Fig. 7 is a time chart useful for explanation of an operation of the Fig. 6 modulation circuit;
Fig. 8 is a block diagram showing an arrangement of a non-contact type IC card system according to a further embodiment of this invention;
Fig. 9 is a block diagram showing an arrangement of a non-contact type IC card system according to a still further embodiment of this invention;
Fig. 10 is a block diagram showing an arrangement of a non-contact type IC card system according to a still further embodiment of this invention;
Fig. 11 is a block diagram showing one example of a system which carries out a data transmission method;
Fig. 12 is an illustration of waveforms useful for explaining an operation of the Fig. 11 system;
Fig. 13 is a block diagram showing one example of a system which carries out a different data transmission method;
Fig. 14 is an illustration of waveforms available for description of an operation of the Fig. 13 system;
Fig. 15 is a block diagram showing an arrangement of a known non-contact type IC card system; and
Fig. 16 is an illustration of waveforms useful for description of a modulation method for a non-contact type IC card.

DETAILED DESCRIPTION OF THE INVENTION

[0026] Referring now to the drawings, a description will be made hereinbelow of embodiments of the present invention.

First Embodiment

[0027] Fig. 1 is a block diagram showing an arrangement of a non-contact type IC card according to an embodiment of this invention. In this non-contact type IC card (which will hereinafter be referred to as a card) 10, the modulation method at data transmission is selectable from two kinds of modulations: the PSK modulation and FSK modulation with a simple circuit arrangement.

[0028] In Fig. 1, the card 10 is shown as comprising a transmission and reception antenna 4, a resonance frequency switching section 40 for switching the resonance frequency of the transmission and reception antenna 4, a modulation circuit 50 for driving the resonance frequency switching section 40 to switch the resonance frequency to match a data being transmitted so that the transmission data is selectively subjected to one of the PSK modulation and the FSK modulation, a PFSEL switch 11 for switching between the PSK modulation and the FSK modulation for the modulation circuit 50, a demodulation circuit 6, a rectifying and voltage control circuit 7, a control section 8 and an E^2PROM 9.

[0029] The PFSEL switch 11 has a PFSEL terminal-coupled to the VDD or the GND to realize the switching to the PSK modulation or the FSK modulation. For example, it is provided as a terminal within the card 10, and its terminal is connected with the VDD or the GND at the manufacturing stage to be provided as a set terminal, or is constructed as a mechanical change-over switch placed on a surface of the card 10 or as a switch comprising a transistor turning on and off in accordance with a command signal from the R/W.

[0030] Fig. 2 shows arrangements of the transmission and reception antenna 4, the resonance frequency switching section 40 and the modulation circuit 50 in Fig. 1. The resonance frequency f of the transmission and reception antenna 4 depends upon the value of a coil L and a value of a capacitor C1 and is obtainable as $f = 1 / \{2(\sqrt{LC1})\}$. In the ordinary transmission and reception antenna, the resonance frequency has conventionally been determined by a set of LC for the data transmission and reception to and from the external. In this invention, for realizing the PSK modulation and FSK modulation, the resonance frequency switching section comprising a capacitor C2 and switching device Tr1 is provided in order to halve the resonance frequency of the transmission and reception antenna 4.

[0031] When the switching device Tr1 made up of a transistor is in the "ON" condition, C = C1 + C2, and when the switching device Tr1 is in the "OFF" condition,

C = C1. For instance, in a case where the resonance frequency is set to f = 400 KHz in a state that the switching device Tr1 is in the "OFF" condition, L = 350 μH and C1 = 452.3 pF. In the case that the resonance frequency f is set to 200 KHz being 1/2 of 400 KHz, if the switching device Tr1 gets into the "ON" state, the C value of the resonance circuit becomes C = C1 + C2, and f = 200 KHz signifies L = 350 μH and C = 1.81 nF so that C2 = 1.358 nF.

[0032] In this embodiment, the transmission and reception antenna 4 makes up the antenna means, the resonance frequency switching section 40 and the modulation circuit 50 constitute the modulation means, the PFSEL switch 11 composes the PSK/FSK switching means, the demodulation circuit 6 organizes the demodulation means, and the control section 8 forms the control means.

[0033] Fig. 3 concretely shows one example of the modulation circuit 50 operative to control the switching device Tr1 of the resonance frequency switching section 40, and Figs. 4A and 4B illustrate time charts associated with this circuit. In Fig. 3, a carrier signal CAR and a transmission data TXD come from the control circuit 8, and the modulation is accomplished at the timing depending upon the carrier signal CAR. An output signal A indicated in Fig. 3 is coupled to a gate input terminal of the switching device Tr1 shown in Fig. 2.

[0034] In Fig. 3, reference numeral 501 represents a D-type flip-flop for accepting the transmission data TXD in a state with using the carrier signal CAR as a clock signal, numeral 502 designates a D-type flip-flop for accepting the output of the D-type flip-flop 501 in a state with using the carrier signal CAR as a clock signal, numeral 503 depicts a NAND gate for accepting the output of the D-type flip-flop 502 and a PFSEL signal, numeral 504 denotes a NOR gate for receiving the output of the D-type flip-flop 501 and the output of the NAND gate 503, numeral 505 stands for a circuit comprising an AND gate 507 and a NOR gate 508, and numeral 506 signifies a circuit comprising an AND gate 509 and a NOR gate 510.

[0035] Secondly, a description will be made hereinbelow of an operation of this circuit. The description will begins, referring to Fig. 4A, with the PSK modulation taken when the PFSEL switch 11 placed in the modulation circuit 50 is connected with the VDD (power supply side). When the transmission data TXD from the control section 8 varies from "L" → "H" or "H" → "L", the output of the modulation circuit 50 represents a signal waveform indicated by A, and when the signal waveform A comes into the "H" state, the switching device Tr1 gets into the "ON" state.

[0036] As described before, when the switching device Tr1 takes the "ON" state, the resonance frequency of the transmission and reception antenna 4 is set to half of the resonance frequency for when being in the "OFF" state, and hence the output waveform of the transmission and reception antenna 4 takes an output waveform at both ends of the L as shown in Fig. 4A. That is, in the output waveform across the L in Fig. 4A, if the switching device Tr1 does not come into the "ON" condition, the signal waveform becomes as indicated by a dotted line. On the other hand, if the switching device Tr1 gets into the "ON" condition, the resonance frequency comes to 1/2 during one period with respect to the original frequency, and thereafter returns to the original resonance frequency, thus accomplishing the phase modulation.

[0037] A secondly, a description will be made hereinbelow of the FSK modulation taken when the PFSEL switch 11 is connected with the GND (grounded side). Fig. 4B shows signal waveforms for the connection of the PFSEL switch 11 with the GND. With the connection of the PFSEL switch 11 with the GND, the output signal A keeps its signal condition until the state of the signal from the transmission data TXD inverts, and hence the ON time of the switching device Tr1 is controlled so that the output waveform from the resonance circuit of the transmission and reception antenna 4 becomes the output waveform across the L as shown in Fig. 4B, thus realizing the frequency modulation.

[0038] As described above, in the non-contact type IC card according to this embodiment, only a simple circuit is provided which comprises the resonance frequency switching section for switching over the resonance frequency of the transmission and reception antenna and the modulation circuit for actuating the switching section and the PFSEL switch of this modulation circuit is connected with the VDD or the GND, with the result that one card can deal with both the PSK and FSK modulation methods, which results in realizing a non-contact type IC card applicable in a wide application range.

Second Embodiment

[0039] Fig. 5 is a block diagram showing an arrangement of a non-contact type IC card according to another embodiment of this invention. This card, designated at numeral 10a, can perform the switching between the PSK and FSK modulations as well as the aforesaid first embodiment and further can alter the timing of the transmission data modulation.

[0040] The different points of the card 10a shown in Fig. 5 from the Fig. 1 card 10 relate to the arrangement of a modulation circuit 51, which will be mentioned later, and the provision of a TXSEL switch 12 for changing the timing of the modulation of the transmission data. Although in the above-described first embodiment the transmission data modulation is accomplished at the time that the "0/1" of the transmission data inverts, the card 10a according to this invention permits the modulation to be implemented when the "0/1" of the transmission data inverts and further the modulation to be always conducted when the transmission data is "0/1". The switching therebetween is achieved through the TXSEL switch 12.

[0041] One concrete example of the modulation cir-

cuit 51 in this embodiment is shown in Fig. 6. In Fig. 6, a section indicated by character a denotes a circuit which carries out the modulation when the "0/1" of the transmission data inverts, its arrangement and operation being basically similar to those described with reference to Fig. 3. A section indicated by character b signifies a circuit which always performs the modulation when the transmission data is "0", and a section indicated by character c is a circuit which serves to selectively supply one of the output C of the section a and the output D of the section b to the resonance frequency switching section 40.

[0042] In the section b of Fig. 6, the arrangement composed of components 501a to 510a is basically the same as that of the section a. Further, in Fig. 6, reference numeral 511 represents a NOR gate, numeral 512 designates a circuit comprising an AND gate 513 and a NOR gate 514, and numeral 515 denotes a D-type flip-flop. The NOT gate 511 accepts as inputs the transmission data TXD and the output of the D-type flip-flop 515. The circuit 512 receives as inputs the transmission data TXD, the output of the NOR gate 511 and the output of the D-type flip-flop 515. Moreover, the D-type flip flop 515 accepts as a clock a division signal BPS attained by dividing (demultiplying) the carrier signal CAR and further accepts as an input the output of the NOR gate 514, with its output B being supplied to the D-type flip-flop 501a.

[0043] Furthermore, in the section c, components 516 to 518 and a component 519 at the output side are inverters, respectively. In the section c, when the TXSEL switch 12 is connected with the VDD (power supply side), the output C of the section a is outputted from an output terminal indicated by character A, while the output D of the section b is taken out from the output terminal A when being connected with the GND (grounded side).

[0044] In this embodiment, in Fig. 6, the section a composes the first modulation section, the section b constitutes the second modulation section, and the section coupled with the TXSEL switch 12 organize the modulation timing switching means.

[0045] Furthermore, particularly the circuit operation of the section b will be described hereinbelow with reference to a time chart of Fig. 7. The description will be made in terms of the condition that the TXSEL switch 12 is connected with the GND and the PFSEL switch 11 is connected with the VDD. A TXEN signal is a data transmission allowing signal from the control circuit 8 and is coupled to a reset input of the D-type flip-flop 515. While the TXEN signal gives "0", the output B of the D-type flip-flop 515 is fixed to "1", and if the TXEN signal turns into "1", it starts to accept the transmission data TXD. The division signal BPS is obtainable by dividing the carrier signal CAR, and serves as a reference clock used in the case of varying the transmission data TXD signal.

[0046] After the reset release of the D-type flip-flop 515 due to the TXEN signal, when this division signal BPS rises, the D-type flip-flow 515 operates so that, in correspondence with the variation of the transmission data TXD signal, the output B of the D-type flip-flop 515 becomes as indicated by character B in Fig. 7. That is, when the transmission data TXD is "0", a signal that the "0/1" of the signal B inverts is obtainable. This signal is inputted into the same circuit as the section a. Further, since at this time the TXSEL switch 12 is connected with the GND, when the transmission data TXD is "0", a modulating signal as indicated by character A in Fig. 7 is obtainable from the output terminal A.

[0047] Although this embodiment has been described of the case that the PSK modulation is always conducted when the transmission data is "0", it is also possible that the modulation method (PSK modulation/FSK modulation) and modulation timing are respectively switched by changing over the PFSEL switch 11 and the TXSEL switch 12.

[0048] As described above, the non-contact type IC card according to this embodiment can select either the PSK modulation or the FSK modulation, and further can switch over the modulation timing for the transmission data. Accordingly, it is possible to realize one non-contact type IC card capable of suiting a number of data communication specifications.

Third Embodiment

[0049] Fig. 8 is a block diagram showing an arrangement of a non-contact type IC card system according to an embodiment of this invention. The non-contact type IC card system according to this embodiment employs either the card 10 or 10a described in the first or second embodiment.

[0050] The description will be made of the case of using the card 10a according to the second embodiment. The card 10a is arranged such that the PFSEL switch 11 and the TXSEL switch 12 of the modulation circuit 51 are switched to the VDD or the GND in accordance with the modulation method taken in the system including the card and the modulation timing. Thus, the setting is selectively made to the PSK modulation or to the FSK modulation, and further selectively made to the method that the modulation is conducted at the time that the "0/1" of the transmission data inverts or to the method that the modulation is always carried out when the transmission data is "0".

[0051] When the card 10a matching with the system specification comes into the communication-allowable distance range for the R/W 2, the transmission and reception antenna 4 of the card 10a receives a radio wave from the R/W 2 and the rectifying and voltage control circuit 7 develops an operating voltage so that the transmission and reception of the data starts. In the data transmission and reception methods, after the card 10a gets the operating voltage, the data transmission is performed from the R/W 2 to the card 10a and the card 10a

decodes and processes the received data and transmits the processed result to the R/W 2.

[0052] Although the description of this embodiment has been taken in terms of the case of using the card 10a according to the second embodiment, even if using the card 10 according to the first embodiment, the data transmission and reception is possible with the similar procedure. The card 10 according to the first embodiment performs only the setting of the modulation method, i.e., the selection of one of the PSK modulation and the FSK modulation.

[0053] As described above, the non-contact type IC card system according to this embodiment can be designed to select as a modulation method one of the PSK modulation and the FSK modulation and also adopted to change over the modulation timing for the transmission data depending upon the kind of card, and hence the relationship between the R/W and the card is more flexible, which can realize a non-contact type IC card system expanded in its application range.

Fourth Embodiment

[0054] Fig. 9 is a block diagram showing an arrangement of a non-contact type IC card system according to another embodiment of this invention. In the system according to this embodiment, the antenna means of the R/W 2a is divided into an antenna 24 for transmission and an antenna 25 for reception so that at the data transmission to the card 10 or 10a the transmission data is modulated in a modulation and demodulation circuit 22 and transmitted as a radio wave from the transmission antenna 24 while at the data reception a radio wave transmitted is received through the reception antenna 25 and then demodulated in the modulation and demodulation circuit 22.

[0055] In the procedure of the data transmission and reception, according to the modulation method of the system, the PFSEL switch 11 of the modulation circuit 50 or 51 of the card 10 or 10a is brought to be connected with the VDD or the GND (if the system is also equipped with the TXSEL switch 12 for switching over the modulation timing, this switch is also operated), and when the card 10 or 10a enters the communication-allowable distance range of the R/W 2a, the transmission and reception antenna 4 of the card 10 or 10a gets a radio wave from the R/W 2a so that the rectifying and voltage control circuit 7 produces a VDD voltage (operating voltage) to start the transmission and reception of the data.

[0056] In the data transmission and reception, after the operating voltage actuates the card 10 or 10a, the data transmission from the R/W 2a to the card 10 or 10a starts to cause the decode and process of the received data to be implemented within the card 10 or 10a, with the processed result being transmitted from the card 10 or 10a to the R/W 2a.

[0057] In the non-contact type IC card system according to this embodiment, the antenna means is divided into the transmission antenna and the reception antenna, and consequently two kinds of antenna characteristics are obtainable for the transmission and reception, respectively. The transmission antenna is made to have an antenna characteristic which can provide a transmission power, while the reception antenna is designed to have an antenna sensitivity accepting a weak radio wave, with the result that a non-contact type IC card system can realized which is capable of the data transmission and reception conquering a longer communication distance.

Fifth Embodiment

[0058] Fig. 10 is a block diagram showing an arrangement of a non-contact type IC card system according to a further embodiment of this invention. In the system according to this embodiment, the data transmission from the R/W 2 to the card 10 or 10a is accomplished on the basis of the PSK modulation, whereas the data transmission from the card 10 or 10a to the R/W 2 is achieved on the basis of the FSK modulation in a state that the PFSEL switch 11 of the modulation circuit 50 or 51 is connected with the GND.

[0059] In the procedure for the data transmission and reception, the PFSEL switch 11 of the modulation circuit 50 or 51 is connected with the GND (if the system is also provided with the TXSEL switch 12, the switch 12 is switched over to match with the system), and if the card 10 or 10a comes in the communication-allowable distance range of the R/W 2, a radio wave from the R/W 2 is received through the transmission and reception antenna 4 of the card 10 or 10a so that the rectifying and voltage control circuit 7 creates an operating voltage to start the data transmission and reception.

[0060] After the card 10 or 10a attains the operating voltage, the data transmission from the R/W 2 to the card 10 or 10a is done on the basis of the PSK modulation and the card 10 or 10a demodulates, decodes and processes the received data, before the processed result is transmitted from the card 10, 10a to the R/W 2 on the basis of the FSK modulation.

[0061] In the non-contact type IC card system according to this embodiment, the data transmission from the R/W to the card is conducted in accordance with the PSK modulation, while the data transmission from the card to the R/W is made in accordance with the FSK modulation, with the result that there is no need for a complicated circuit for the FSK modulation to be incorporated in the card, and when the demodulation circuit within the card is designed to agree with the PSK modulation, the size-reduction and cost-reduction of the card are possible, besides even a radio wave with a higher frequency is receivable because the R/W side carries out the demodulation with respect to the FSK modulation.

Sixth Embodiment

[0062] Fig. 11 is a block diagram showing an arrangement of a non-contact type IC card system which executes a data transmission method, and Fig. 12 is an illustration of waveforms of signals taken at the data transmission and reception by the R/W and the card of this system. In this embodiment, after the data transmission from the R/W 2 to the card 10 or 10a, the supply of a radio wave from the R/W 2 is continued even at the data transmission from the card 10 or 10a to the R/W 2 so that the operating voltage (VDD) within the card 10 or 10a is always stable.

[0063] The particular difference of the Fig. 11 system from the aforementioned embodiments is that a program stored in a control section 23a of the R/W 2 or in a host computer 3a executes the operations to be described later.

[0064] In operation, the PFSEL switch 11 of the modulation circuit 50 or 51 of the card 10 or 10a is connected with, for example, the VDD side (if the system is also equipped with the TXSEL switch 12, at the same time the switch is operated in accordance with the system) , so that the data transmission and reception is accomplished on the PSK modulation. For the data transmission and reception between the R/W 2 and the card 10 or 10a, first the transmission and reception antenna 21 of the R/W 2 begins to transmit a radio wave. The card 10 or 10a receives the radio wave through its transmission and reception antenna 4, which radio wave is rectified in the rectifying and voltage control circuit 7. The rectifying and voltage control circuit 7 also develops the operating voltage VDD. This term constitutes the VDD rise time period in Fig. 12.

[0065] When the operating voltage VDD comes up to 5V, the card 10 or 10a and the R/W 2 get into the data transmission and reception allowable conditions, and hence the data transmission period from the R/W 2 to the card 10 or 10a starts. In accordance with the instruction from the host computer 3a, in the R/W 2 the control section 23a modulates the data using the modulation and demodulation circuit 22 and further transmits the data using the transmission and reception antenna 21. This data is received by the transmission and reception antenna 4 within the card 10 or 10a.

[0066] In Fig. 12, at the points A and B for the modulation in the R/W 2, the resonance circuit of the transmission and reception antenna 4 of the card 10 or 10a side also has deformed or distorted waveforms at points C and D. That data undergoes the demodulation in the demodulation circuit 6 and further the process in the control section 8, whereby the data transmission from the R/W 2 to the card 10 or 10a takes place.

[0067] Subsequently, the data transmission period from the card 10 or 10a to the R/W 2 starts. In this embodiment, even after the completion of the data transmission from the R/W 2 to the card 10 or 10a, the data transmission from the card 10 or 10a to the R/W 2 is conducted while the supply of the signal (radio wave) to the card 10 or 10a continues, and hence the control section 23a of the R/W 2 continues to emit the radio wave from the transmission and reception antenna 21.

[0068] In this state, the control section 8 of the card 10 or 10a sends the transmission data to the modulation circuit 50 or 51 in accordance with the processed result of the received data from the R/W 2 in order to implement the PSK modulation in the modulation circuit 50 or 51. This is shown at the points E and F in Fig. 12. Since the resonance circuit of the transmission and reception antenna 21 of the R/W 2 continuously issues the signal, when the card 10 or 10a side modulates the data, the waveform is expanded as shown at the points G And H in Fig. 12, which allows the judgment on the fact that the data has been subjected to the modulation.

[0069] Subsequently, the modulation and demodulation circuit 22 demodulates this waveform and supplies the control section 23a with the demodulated waveform which in turn, is fed to the host computer 3a. Thereafter, the data transmission and reception is completed with the repeated data transmission from the R/W 2 to the card 10 or 10a and data transmission from the card 10 or 10a to the R/W 2.

[0070] Although the description of the above embodiment has been made of the PSK modulation, the data transmission on the FSK modulation is similarly workable.

[0071] In the data transmission method, after the data transmission from the R/W to the card, even during the data transmission from the card to the R/W, the supply of the radio wave continuously occurs, and therefore, the operating voltage VDD is always stable and the continuous data transmission and reception is possible, thus realizing a data transmission method capable of a high-speed data communication with a high reliability.

Seventh Embodiment

[0072] Fig. 13 is a block diagram showing an arrangement of a non-contact type IC card system for carrying out a different data transmission method, and Fig. 14 is an illustration of waveforms of signals at data transmission and reception between the R/W and the card in this system. In this embodiment, in the R/W 2, the resonance of the resonance circuit continues at the data transmission from the R/W 2 to the card 10 or 10a, while the supply of the radio wave stops at the data transmission from the card 10 or 10a to the R/W 2, with the result that even a weak radio wave from the card 10 or 10a to the R/W 2 becomes easily receivable in the R/W 2 side.

[0073] If a weak radio wave is tried to be received from the card 10 or 10a in a state that a strong transmission power from the R/W 2 is in supply, the weak radio wave is subject to be absorbed into the strong radio wave for the transmission from the R/W 2 to the card 10 or 10a so that difficulty is encountered to discriminate or distinguish the weak radio wave.

[0074] The difference of the Fig. 13 system from the above-described embodiments is that a program built in the control section 23b of the R/W 2 or a host computer 3a implements the operation which will be described below.

[0075] In operation, the PFSEL switch 11 of the modulation circuit 50 or 51 of the card 10 or 10a is coupled to, for example, the VDD side (if the system is also provided with the TXSEL switch 12, at the same time the switch is changed over in accordance with the system), so that the data transmission and reception is implemented on the basis of the PSK modulation. The data transmission and reception between the R/W 2 and the card 10 or 10a starts with the transmission of a radio wave from the transmission and reception antenna 21 of the R/W 2. In the card 10 or 10a, the transmission and reception antenna 4 receives that radio wave and the rectifying and voltage control circuit 7 rectifies it to produce the operating voltage VDD. This is accomplished during the VDD rise period in Fig. 14.

[0076] When the operating voltage VDD reaches 5V, the card 10 or 10a and the R/W 2 gent into the data transmission allowable condition, and the data transmission period from the R/W 2 to the card 10 or 10a starts. In accordance with the instruction from the host computer 3b, in the R/W 2 the control section 23b modulates the data in the modulation and demodulation circuit 22 and sends the modulated data through the transmission and reception antenna 21. This data is received through the transmission and reception antenna 4 of the card 10 or 10a.

[0077] In Fig. 14, at the points A and B for the modulation in the R/W 2, the resonance circuit of the transmission and reception antenna 4 of the card 10 or 10a side also has deformed or distorted waveforms at points C and D. That data is subjected to the demodulation in the demodulation circuit 6 and further subjected to the process in the control section 8, whereby the data transmission from the R/W 2 to the card 10 or 10a takes place.

[0078] Subsequently, the data transmission period from the card 10 or 10a to the R/W 2 starts. In this embodiment, after the completion of the data transmission from the R/W 2 to the card 10 or 10a, the supply of the signal (radio wave) to the card 10 or 10a stops, while the data transmission from the card 10 or 10a to the R/W 2 is carried out. Accordingly, the operating voltage VDD in the card 10 or 10a starts to decrease from 5V. In addition, the resonance attenuation of the resonance circuit of the card 10 or 10a begins.

[0079] In this embodiment, in this attenuation state the data transmission is conducted from the card 10 or 10a to the R/W 2. For example, until the operating voltage VDD attenuates from 5V up to 2.5V, the data transmission from the card 10 or 10a to the R/W 2 completes. In this attenuation term, the control section 8 of the card 10 or 10a supplies the transmission data to the modulation circuit 50 or 51 to carry out the PSK modulation therein. This is shown at the points I and J in Fig. 14. The resonance circuit of the transmission and reception antenna 21 of the R/W 2 also stops the signal supply and receives the modulated data during the attenuating oscillation, whereby the waveform is distorted as shown at the points K and L in Fig. 14. From this, the R/W 2 determines the fact that the data has undergone the modulation.

[0080] Furthermore, this waveform is demodulated in the modulation and demodulation circuit 22 and then inputted into the control section 23b, before being supplied to the host computer 3b. In this system, in a case where, after the completion of one data transmission and reception, the data transmission and reception is again carried out, the operation restarts from the VDD rise period due to the supply from the R/W 2 to the card 10 or 10a, and the data transmission and reception is re-performed after the operating voltage VDD in the card 10 or 10a is set to 5V.

[0081] Although the description of this embodiment has been made in terms of the PSK modulation, the data transmission on the FSK modulation is possible in the same manner.

[0082] The data transmission is particularly effective in the case that, since the distance between the card and the R/W is long, the data transmission power from the R/W needs to be strong, and the transmission power from the card is weak because of the long distance. The transmission power from the R/W is stopped at the time of the transmission from the card to the R/W conducted after the completion of the transmission from the R/W to the card, by which a data transmission method can be realized which is capable of facilitating the reception of a weak radio wave from the card side in the R/W side.

Claims

1. A non-contact type IC card (10) using a radio wave as a communication medium, comprising:

   antenna means (4) for transmission and reception of data;
   modulation means (40, 50) for performing PSK- and FSK-modulation of a data being transmitted, by switching over a resonance frequency of the antenna means to suit the transmission data;
   PSK/FSK switching means (11) for performing a switching operation so that said modulation means conducts one of the PSK- and FSK-modulations;
   demodulation means (6) for demodulating data received by said antenna means; and
   control means (8) for controlling the respective means.

2. The non-contact type IC card according to claim 1,

wherein said modulation means includes:

a first modulating section for performing the PSK- and FSK-modulations at a first modulating timing;
a second modulating section for performing the PSK- and FSK-modulations at a second modulating timing; and
modulation timing switching means for changing the modulation timing by switching a circuit between said first and second modulating sections.

3. A non-contact type IC card system comprising:

a non-contact type IC card (10, 10a) using a radio wave as a communication medium, including:

antenna means (4) for transmission and reception of data;
modulation means (40, 50, 51) for performing PSK- and FSK-modulation of a data being transmitted, by switching over a resonance frequency of the antenna means to suit the transmission data;
PSK/FSK switching means (11) for performing a switching operation so that said modulation means conducts one of the PSK- and FSK-modulations;
demodulation means (6) for demodulating data received by said antenna means; and
control means (8) for controlling the respective means of said IC card; and
a reader writer (2; 2a) including:

antenna means (21; 24, 25) for performing transmission and reception of data to and from said IC card;
modulation and demodulation means (22) for carrying out modulation and demodulation of data transmitted and received through said second-mentioned antenna means; and
control means (23) for controlling said means of said reader writer.

4. The non-contact type IC card system according to claim 3, wherein said modulation means of said non-contact type IC card includes:

a first modulating section for performing the PSK- and FSK-modulations at a first modulating timing;
a second modulating section for performing the PSK- and FSK-modulations at a second modulating timing; and
modulation timing switching means for changing the modulation timing by switching a circuit between said first and second modulating sections.

5. The non-contact type IC card system according to claim 3, wherein said antenna means of said reader writer comprises an antenna (24) for data transmission and an antenna (25) for data reception, said transmission antenna being provided separately from said reception antenna.

6. The non-contact type IC card system according to claim 3, wherein said reader writer employs the PSK modulation at data transmission and said non-contact type IC card employs the FSK modulation at data transmission.

7. The non-contact type IC card system according to claim 4, wherein said reader writer employs the PSK modulation at data transmission and said non-contact type IC card employs the FSK-modulation at data transmission.

8. The non-contact type IC card system according to claim 5, wherein said reader writer employs the PSK modulation at data transmission and said non-contact type IC card employs the FSK modulation at data transmission.

Patentansprüche

1. Kontaktlose IC-Karte (10), die eine Radiowelle als Kommunikationsmedium verwendet, mit:

einem Antennenmittel (4) zum Senden und Empfangen von Daten;
einem Modulationsmittel (40, 50) zum Ausführen einer PSKund FSK-Modulation von gesendeten Daten durch Umschalten einer Resonanzfrequenz des Antennenmittels zur Anpassung an die Sendedaten;
einem PSK/FSK-Schaltmittel (11) zum Ausführen einer Umschaltoperation, so daß das Modulationsmittel entweder die PSK- oder die FSK-Modulation durchführt;
einem Demodulationsmittel (6) zum Demodulieren von über das Antennenmittel empfangene Daten; und mit
einem Steuermittel (8) zum Steuern des jeweiligen Mittels.

2. Kontaktlose IC-Karte nach Anspruch 1, bei der das Modulationsmittel ausgestattet ist mit:

einem ersten Modulationsabschnitt zum Ausführen der PSK- und FSK-Modulation zu einer ersten Modulationszeitvorgabe;

einem zweiten Modulationsabschnitt zum Ausführen der PSKund FSK-Modulation bei einer zweiten Modulationszeitvorgabe; und mit
einem Modulationszeitvorgabe-Umschaltmittel zum-Ändern der Modulationszeitvorgabe durch Umschalten einer Schaltung zwischen dem ersten und dem zweiten Modulationsabschnitt.

3. Kontaktloses IC-Kartensystem, mit:

einer kontaktlosen IC-Karte (10, 10a), die eine Radiowelle als Kommunikationsmedium verwendet, mit:

einem Antennenmittel (4) zum Senden und Empfangen von Daten;
einem Modulationsmittel (40, 50, 51) zum Ausführen einer PSK- und FSK-Modulation von gesendeten Daten durch Umschalten einer Resonanzfrequenz des Antennenmittels zur Anpassung an die Sendedaten;
einem PSK/FSK-Umschaltmittel (11) zum Ausführen einer Umschaltoperation, so daß das Modulationsmittel entweder die PSK- oder FSK-Modulation durchführt;
einem Demodulationsmittel (6) zum Demodulieren von über das Antennenmittel empfangene Daten; und
einem Steuermittel (8) zum Steuern des jeweiligen Mittels der IC-Karte; und mit
einer Lese/Schreibeinrichtung (2; 2a), mit:

einem Antennenmittel (21; 24, 25) zum Ausführen von Senden und Empfangen von Daten zu oder von der IC-Karte;
einem Modulations- und Demodulationsmittel (22) zum Ausführen einer Modulation und einer Demodulation von gesendeten und empfangenen Daten durch das zweitgenannte Antennenmittel; und mit
einem Steuermittel (23) zum Steuern der Mittel der Lese/Schreibeinrichtung.

4. Kontaktloses IC-Kartensystem nach Anspruch 3, dessen Modulationsmittel der kontaktlosen IC-Karte ausgestattet ist mit:

einem ersten Modulationsabschnitt zum Ausführen der PSK- und FSK-Modulation zu einer ersten Modulationszeitvorgabe;
einem zweiten Modulationsabschnitt zum Ausführen der PSKund FSK-Modulation zu einer zweiten Modulationszeitvergabe; und mit
einem Modulationszeitvorgabe-Umschaltmittel zum Ändern der Modulationszeitvorgabe durch Umschalten einer Schaltung zwischen dem ersten und dem zweiten Modulationsabschnitt.

5. Kontaktloses IC-Kartensystem nach Anspruch 3, dessen Antennenmittel von der Lese/Schreibeinrichtung über eine Antenne (24) zur Datensendung und eine Antenne (25) zum Datenempfang verfügt, wobei die Sendeantenne separat von der Empfangsantenne vorgesehen ist.

6. Kontaktloses IC-Kartensystem nach Anspruch 3, dessen Lese/Schreibeinrichtung die PSK-Modulation bei der Datensendung verwendet, wobei die kontaktlose IC-Karte die FSK-Modulation bei Datensendung verwendet.

7. Kontaktloses IC-Kartensystem nach Anspruch 4, dessen Lese/Schreibeinrichtung die PSK-Modulation bei der Datensendung verwendet, wobei die kontaktlose IC-Karte die FSK-Modulation bei Datensendung verwendet.

8. Kontaktloses IC-Kartensystem nach Anspruch 5, dessen Lese/Schreibeinrichtung die PSK-Modulation bei der Datensendung verwendet, wobei die kontaktlose IC-Karte die FSK-Modulation bei Datensendung verwendet.

Revendications

1. Une carte à circuit intégré (10) du type sans contact utilisant une onde de radio à titre de support de communication, comprenant :

une structure d'antenne (4) pour l'émission et la réception de données;
des moyens de modulation (40, 50) pour effectuer une modulation PSK et une modulation FSK de données qui sont émises, en commutant une fréquence de résonance de la structure d'antenne pour l'adapter aux données émises;
des moyens de commutation PSK/FSK (11) pour effectuer une opération de commutation de façon que les moyens de modulation accomplissent l'une des modulations PSK et FSK;
des moyens de démodulation (6) pour démoduler des données reçues par la structure d'antenne; et
des moyens de commande (8) pour commander les moyens respectifs.

2. La carte de circuit intégré du type sans contact selon la revendication 1, dans laquelle les moyens de

modulation comprennent :

une première section de modulation pour effectuer les modulations PSK et FSK dans une première condition temporelle de modulation;
une seconde section de modulation pour effectuer les modulations PSK et FSK dans une seconde condition temporelle de modulation; et
des moyens de commutation de conditions temporelles de modulation, pour changer la condition temporelle de modulation en commutant un circuit entre les première et seconde sections de modulation.

3. Un système de carte à circuit intégré du type sans contact comprenant :

une carte à circuit intégré (10, 10a) du type sans contact utilisant une onde de radio à titre de support de communication, comprenant:

une structure d'antenne (4) pour l'émission et la réception de données;
des moyens de modulation (40, 50, 51) pour effectuer une modulation PSK et une modulation FSK de données qui sont émises, en commutant une fréquence de résonance de la structure d'antenne pour l'adapter aux données émises;
des moyens de commutation PSK/FSK (11) pour effectuer une opération de commutation, de façon que les moyens de modulation accomplissent l'une des modulations PSK et FSK;
des moyens de démodulation (6) pour démoduler des données reçues par la structure d'antenne; et
des moyens de commande (8) pour commander les moyens respectifs de la carte à circuit intégré; et
un dispositif de lecture/écriture (2; 2a) comprenant :

une structure d'antenne (21; 24, 25) pour effectuer l'émission de données vers la carte à circuit intégré et la réception de données à partir de cette dernière;
des moyens de modulation et de démodulation (22) pour accomplir une modulation et une démodulation de données émises et reçues par l'intermédiaire de la structure d'antenne mentionnée en second; et
des moyens de commande (23) pour commander les moyens du dispositif de lecture/écriture.

4. Le système de carte à circuit intégré du type sans contact selon la revendication 3, dans lequel les moyens de modulation de la carte à circuit intégré du type sans contact comprennent :

une première section de modulation pour effectuer les modulations PSK et FSK dans une première condition temporelle de modulation;
une seconde section de modulation pour effectuer les modulations PSK et FSK dans une seconde condition temporelle de modulation; et
des moyens de commutation de condition temporelle de modulation, pour changer la condition temporelle de modulation en commutant un circuit entre les première et seconde sections de modulation.

5. Le système de carte à circuit intégré du type sans contact selon la revendication 3, dans lequel la structure d'antenne du dispositif de lecture/écriture comprend une antenne (24) pour l'émission de données et une antenne (25) pour la réception de données, l'antenne d'émission étant établie séparément de l'antenne de réception.

6. Le système de carte à circuit intégré du type sans contact selon la revendication 3, dans lequel le dispositif de lecture/écriture utilise la modulation PSK pour l'émission de données, et la carte à circuit intégré du type sans contact utilise la modulation FSK pour l'émission de données.

7. Le système de carte à circuit intégré du type sans contact selon la revendication 4, dans lequel le dispositif de lecture/écriture utilise la modulation PSK pour l'émission de données et la carte à circuit intégré du type sans contact utilise la modulation FSK pour l'émission de données.

8. Le système de carte à circuit intégré du type sans contact selon la revendication 5, dans lequel le dispositif de lecture/écriture utilise la modulation PSK pour l'émission de données et la carte à circuit intégré du type sans contact utilise la modulation FSK pour l'émission de données.

FIG. 1

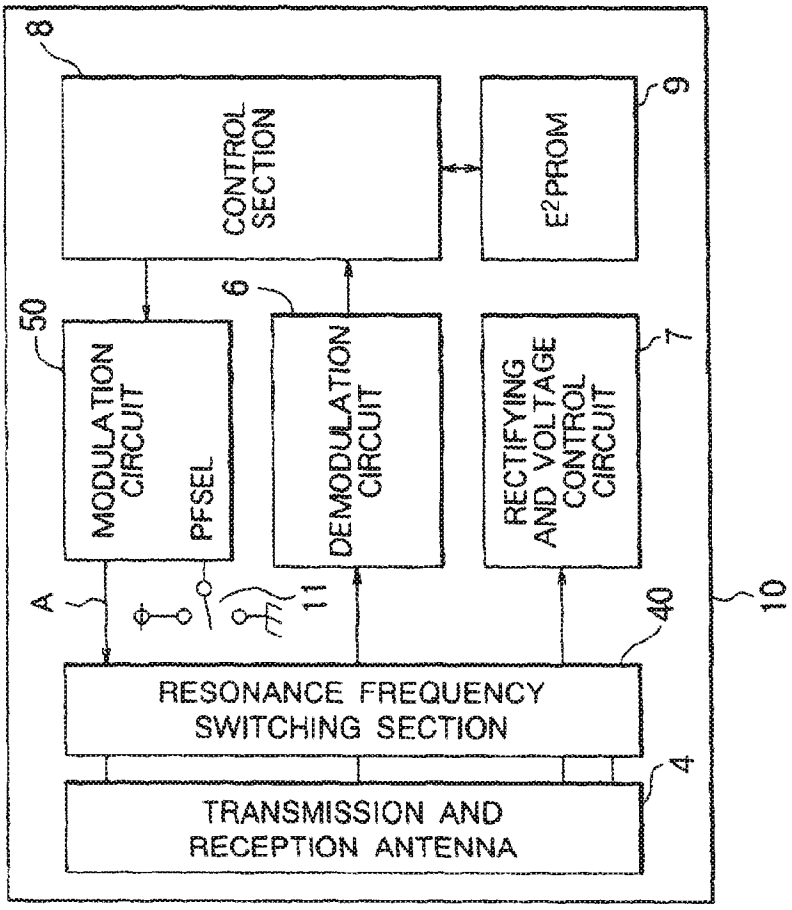

8
CONTROL SECTION
E²PROM
9
6
50
MODULATION CIRCUIT
PFSEL
DEMODULATION CIRCUIT
RECTIFYING AND VOLTAGE CONTROL CIRCUIT
7
A
11
40
10
RESONANCE FREQUENCY SWITCHING SECTION
4
TRANSMISSION AND RECEPTION ANTENNA

FIG. 2

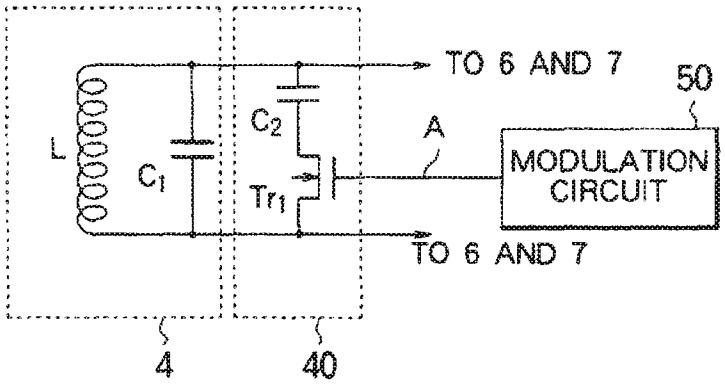

TO 6 AND 7
50
L
C1
C2
Tr1
A
MODULATION CIRCUIT
TO 6 AND 7
4
40

FIG. 3

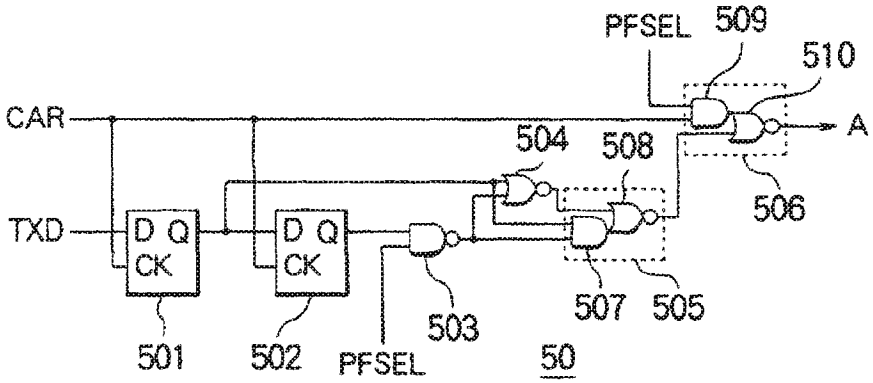

PFSEL
509
510
CAR
A
504
508
506
TXD
D Q
CK
D Q
CK
507
505
503
501
502
PFSEL
50

FIG. 4A

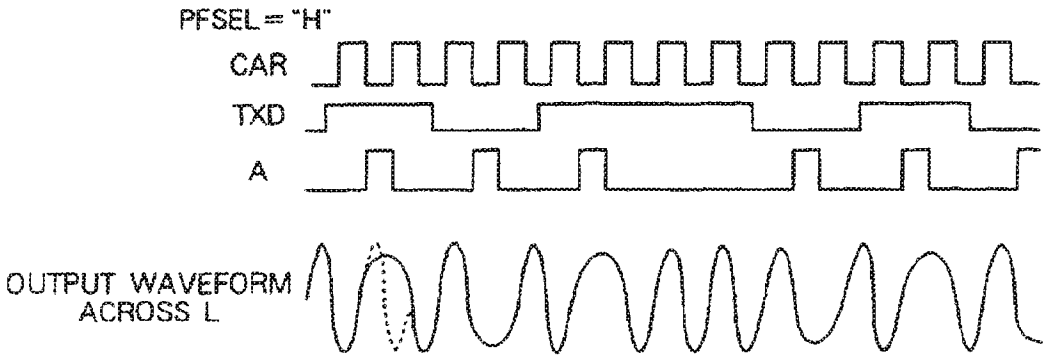


FIG. 4B

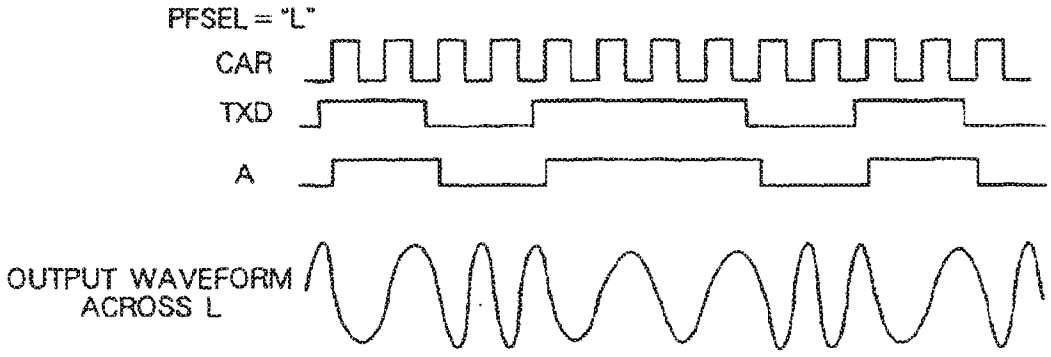


FIG. 5

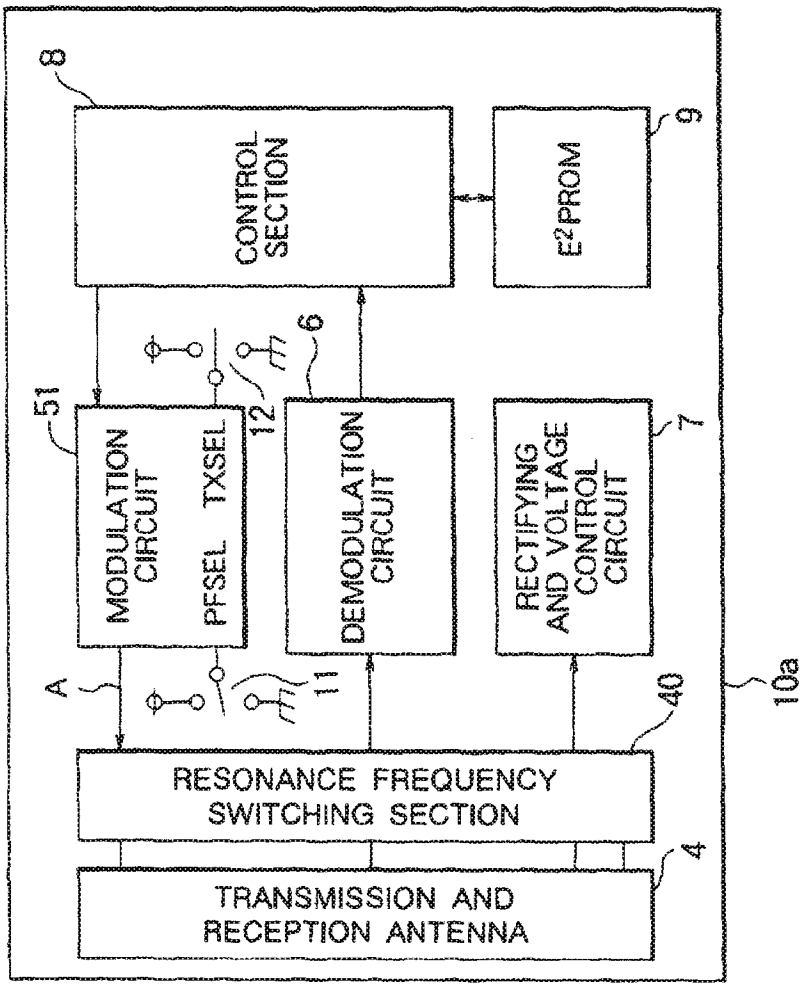


FIG. 6

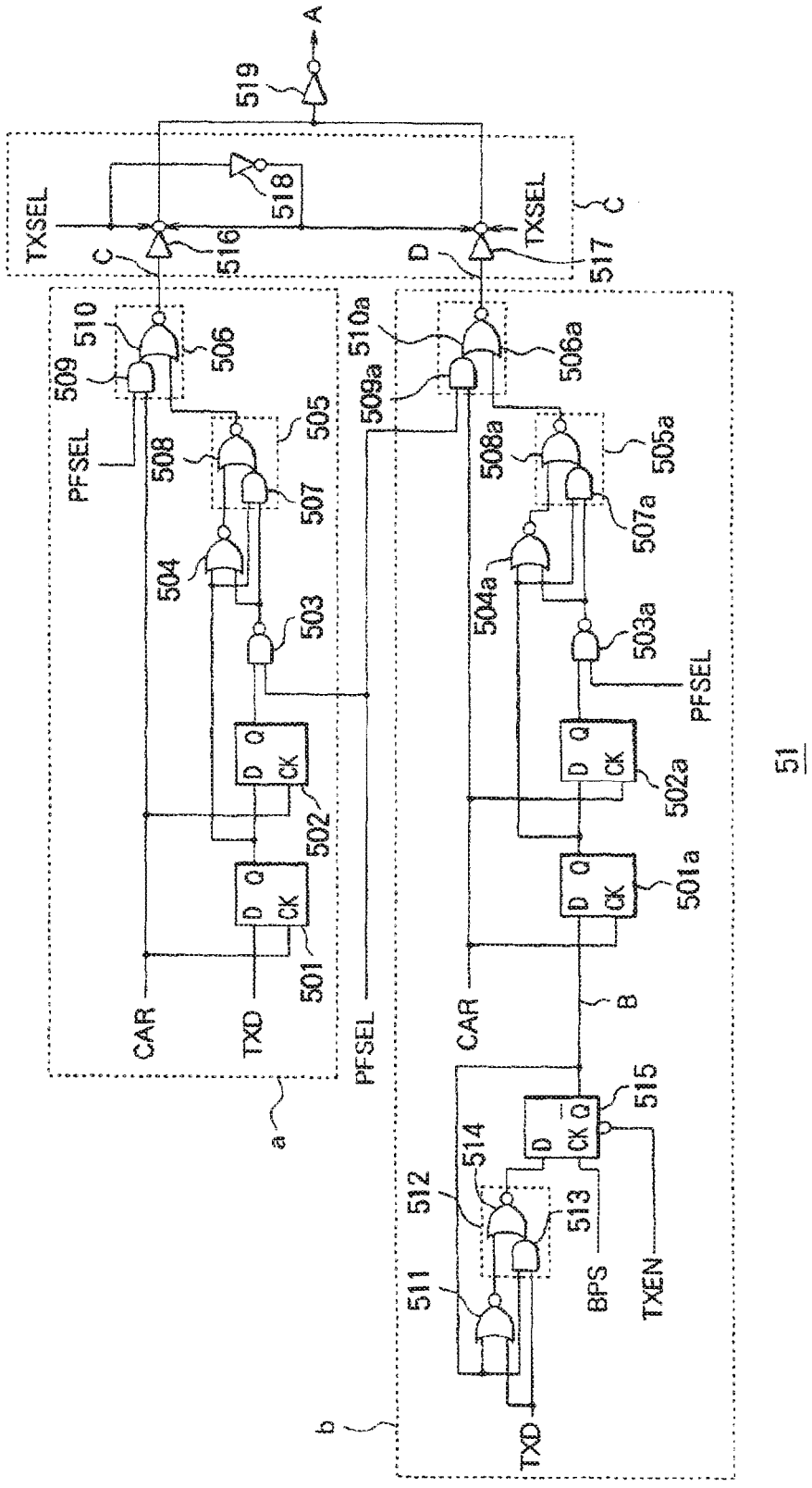

A
519
518
TXSEL
C
516
D
517
TXSEL
C
510
509
506
PFSEL
508
505
507
504
503
D Q
CK
502
501
CAR
TXD
a
PFSEL
510a
509a
506a
508a
505a
507a
504a
503a
PFSEL
502a
501a
B
CAR
515
514
512
513
511
BPS
TXEN
TXD
b
51

FIG. 7

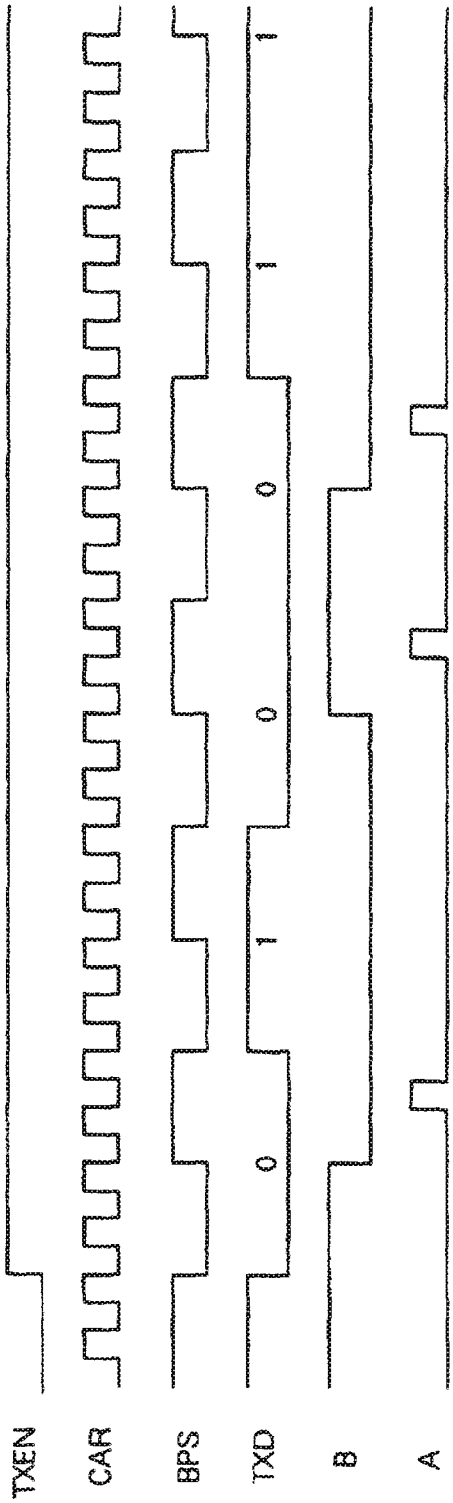


FIG. 8

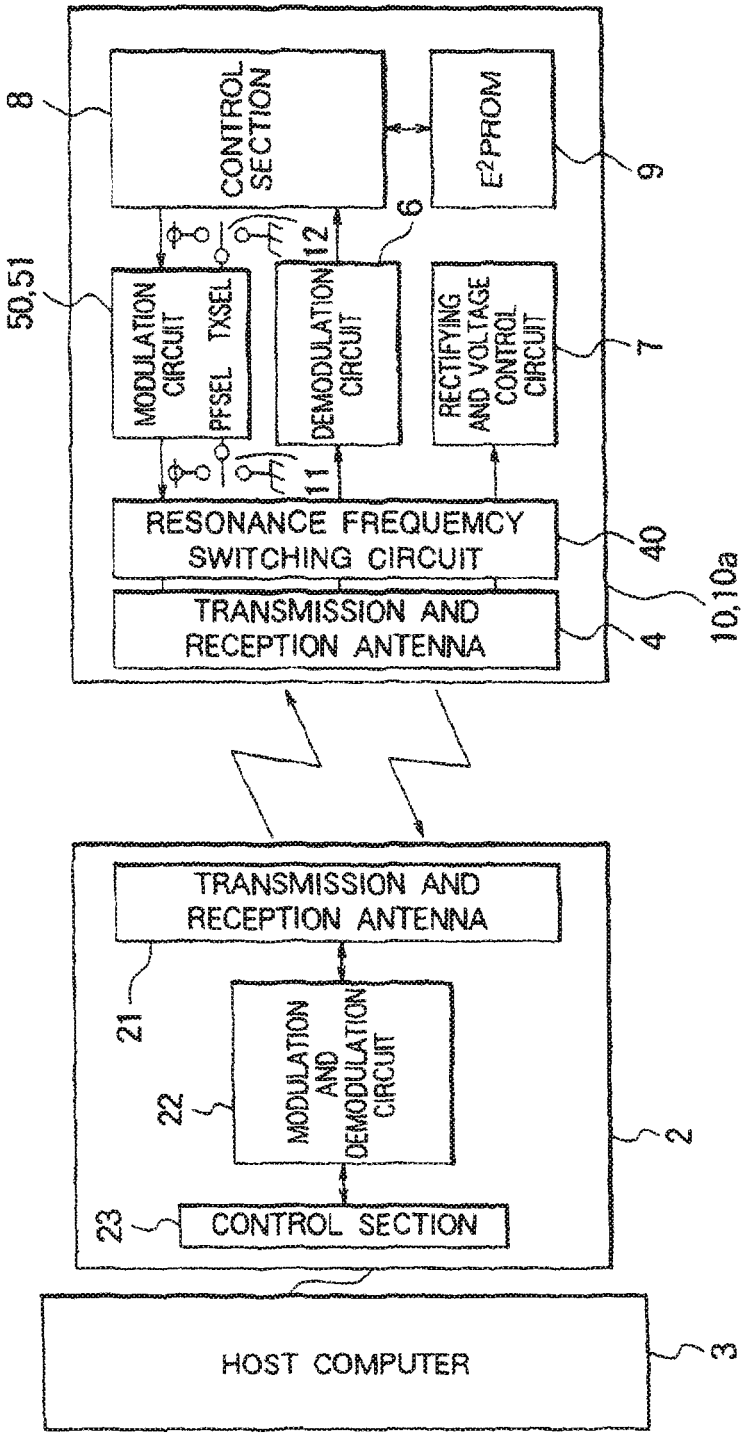

8
CONTROL SECTION
E²PROM
9
6
12
50,51
MODULATION CIRCUIT
PFSEL TXSEL
DEMODULATION CIRCUIT
RECTIFYING AND VOLTAGE CONTROL CIRCUIT
7
11
RESONANCE FREQUEMCY SWITCHING CIRCUIT
40
TRANSMISSION AND RECEPTION ANTENNA
4
10,10a
TRANSMISSION AND RECEPTION ANTENNA
21
22
MODULATION AND DEMODULATION CIRCUIT
2
23
CONTROL SECTION
HOST COMPUTER
3

FIG. 9

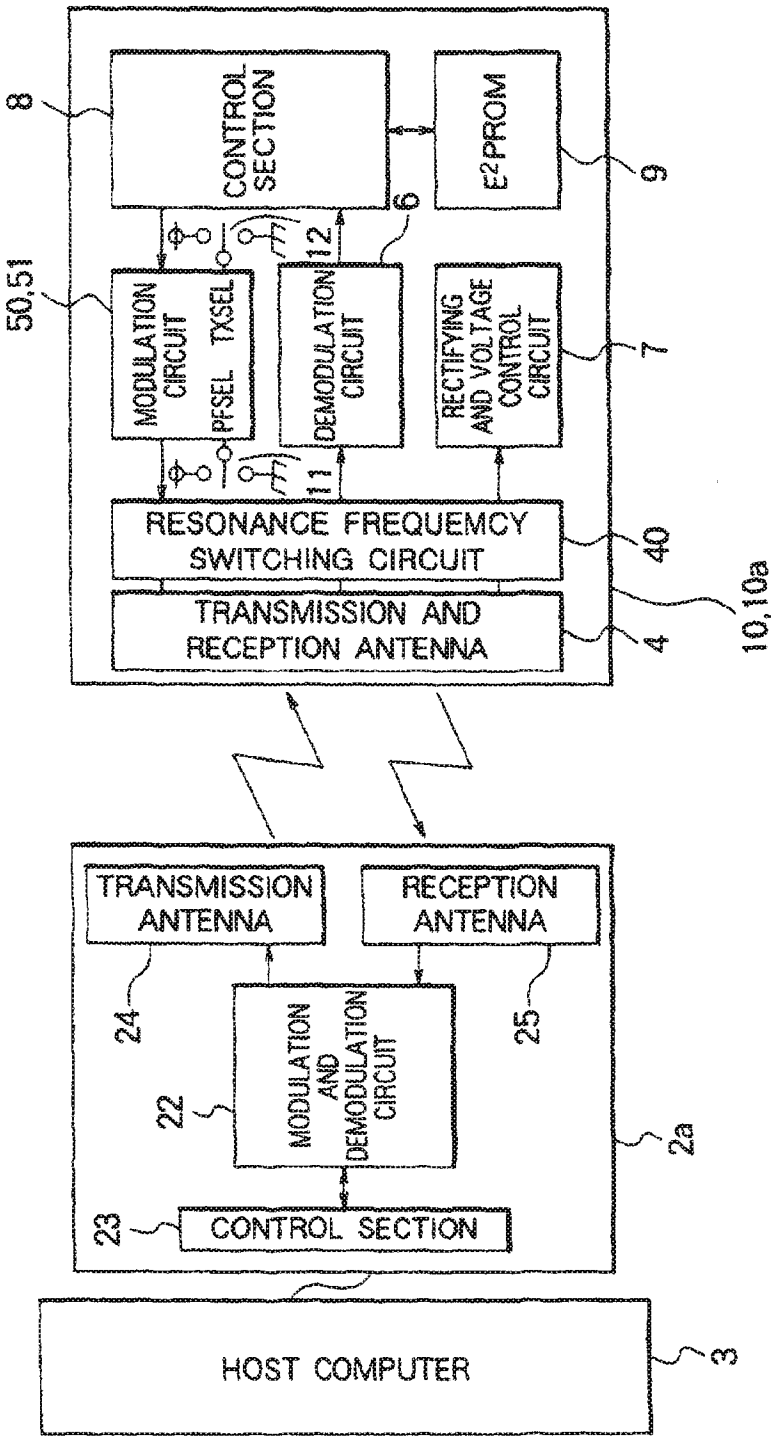

8
CONTROL SECTION
E²PROM
9
6
12
50,51
MODULATION CIRCUIT
PFSEL
TXSEL
DEMODULATION CIRCUIT
RECTIFYING AND VOLTAGE CONTROL CIRCUIT
7
11
RESONANCE FREQUEMCY SWITCHING CIRCUIT
40
TRANSMISSION AND RECEPTION ANTENNA
4
10,10a
TRANSMISSION ANTENNA
RECEPTION ANTENNA
24
25
22
MODULATION AND DEMODULATION CIRCUIT
2a
23
CONTROL SECTION
HOST COMPUTER
3

FIG. 10

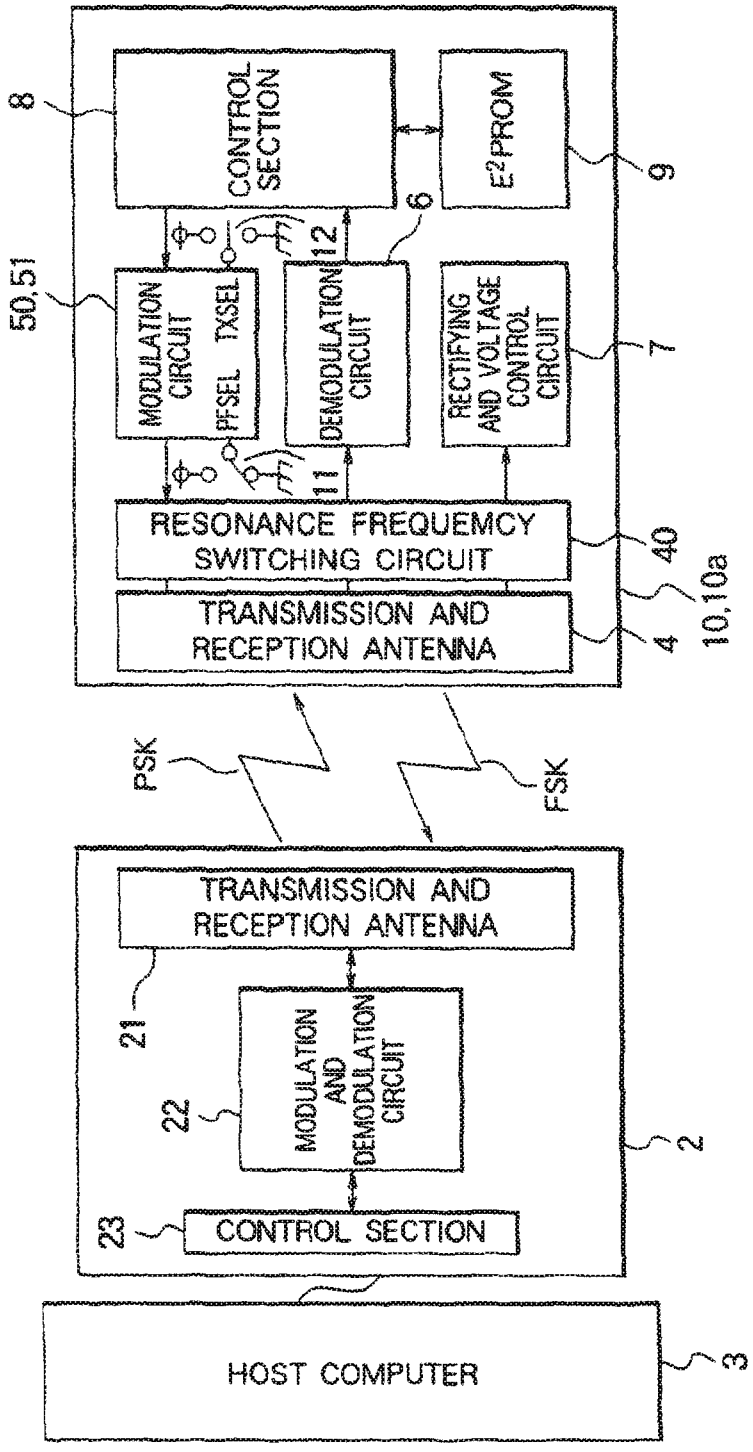
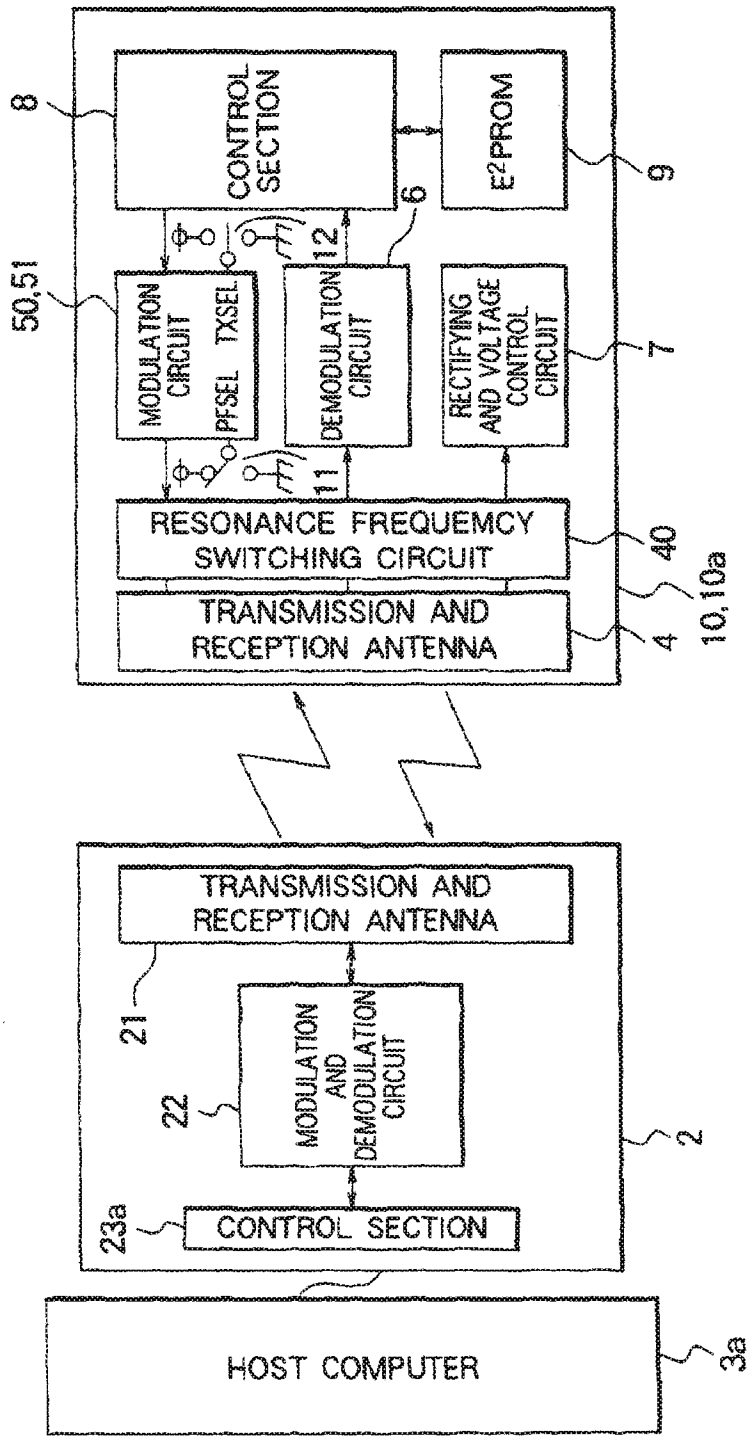

8
CONTROL SECTION
E²PROM
9
6
12
50,51
MODULATION CIRCUIT
PFSEL
TXSEL
DEMODULATION CIRCUIT
RECTIFYING AND VOLTAGE CONTROL CIRCUIT
7
11
RESONANCE FREQUEMCY SWITCHING CIRCUIT
40
TRANSMISSION AND RECEPTION ANTENNA
4
10,10a
PSK
FSK
TRANSMISSION AND RECEPTION ANTENNA
21
22
MODULATION AND DEMODULATION CIRCUIT
2
23
CONTROL SECTION
HOST COMPUTER
3

FIG. 11


8
CONTROL SECTION
E²PROM
9
6
12
50,51
MODULATION CIRCUIT
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TXSEL
DEMODULATION CIRCUIT
RECTIFYING AND VOLTAGE CONTROL CIRCUIT
7
11
RESONANCE FREQUEMCY SWITCHING CIRCUIT
40
TRANSMISSION AND RECEPTION ANTENNA
4
10,10a
TRANSMISSION AND RECEPTION ANTENNA
21
22
MODULATION AND DEMODULATION CIRCUIT
2
23a
CONTROL SECTION
HOST COMPUTER
3a

FIG. 12

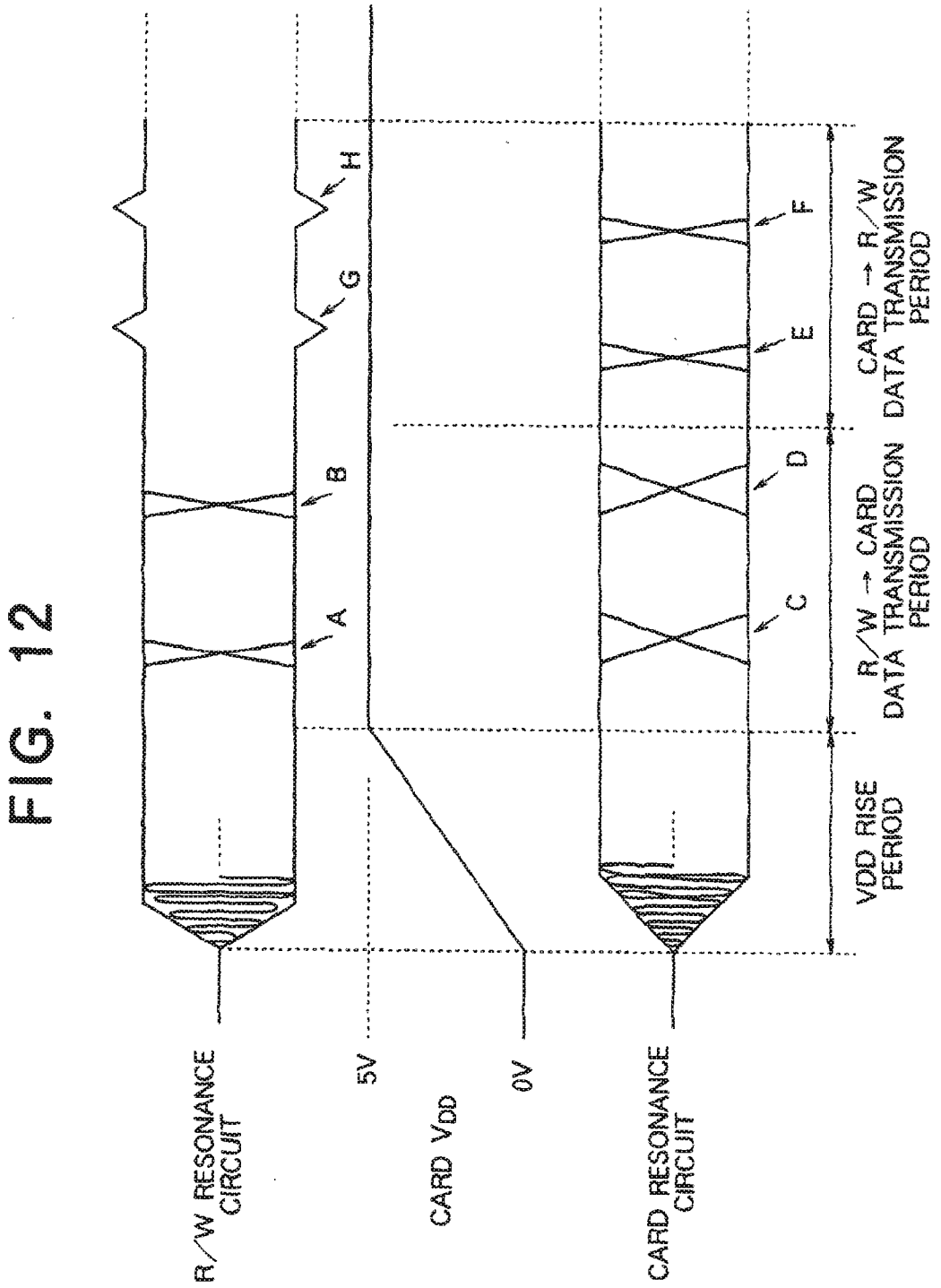


FIG. 13

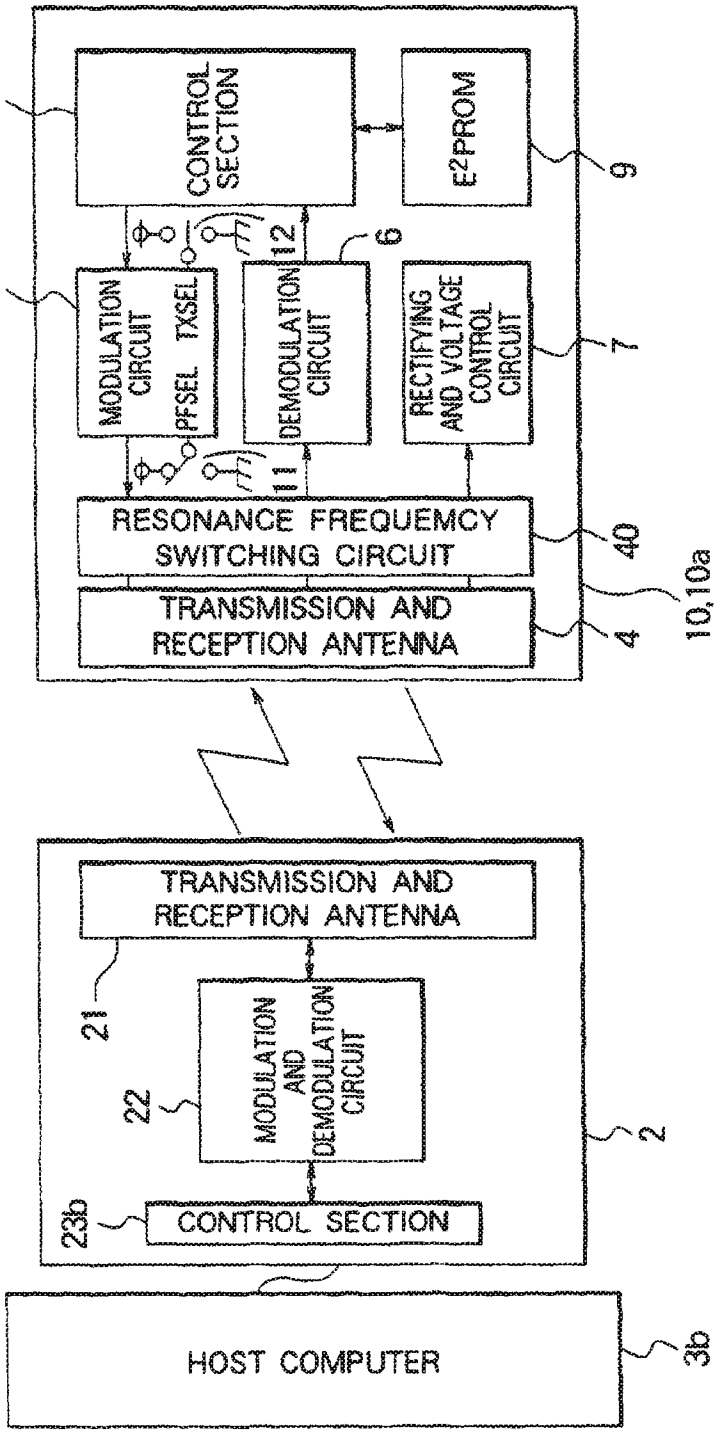

8
CONTROL SECTION
E²PROM
9
50,51
MODULATION CIRCUIT
PFSEL TXSEL
12
6
DEMODULATION CIRCUIT
RECTIFYING AND VOLTAGE CONTROL CIRCUIT
7
11
RESONANCE FREQUEMCY SWITCHING CIRCUIT
40
TRANSMISSION AND RECEPTION ANTENNA
4
10,10a
TRANSMISSION AND RECEPTION ANTENNA
21
22
MODULATION AND DEMODULATION CIRCUIT
2
23b
CONTROL SECTION
HOST COMPUTER
3b

FIG. 14

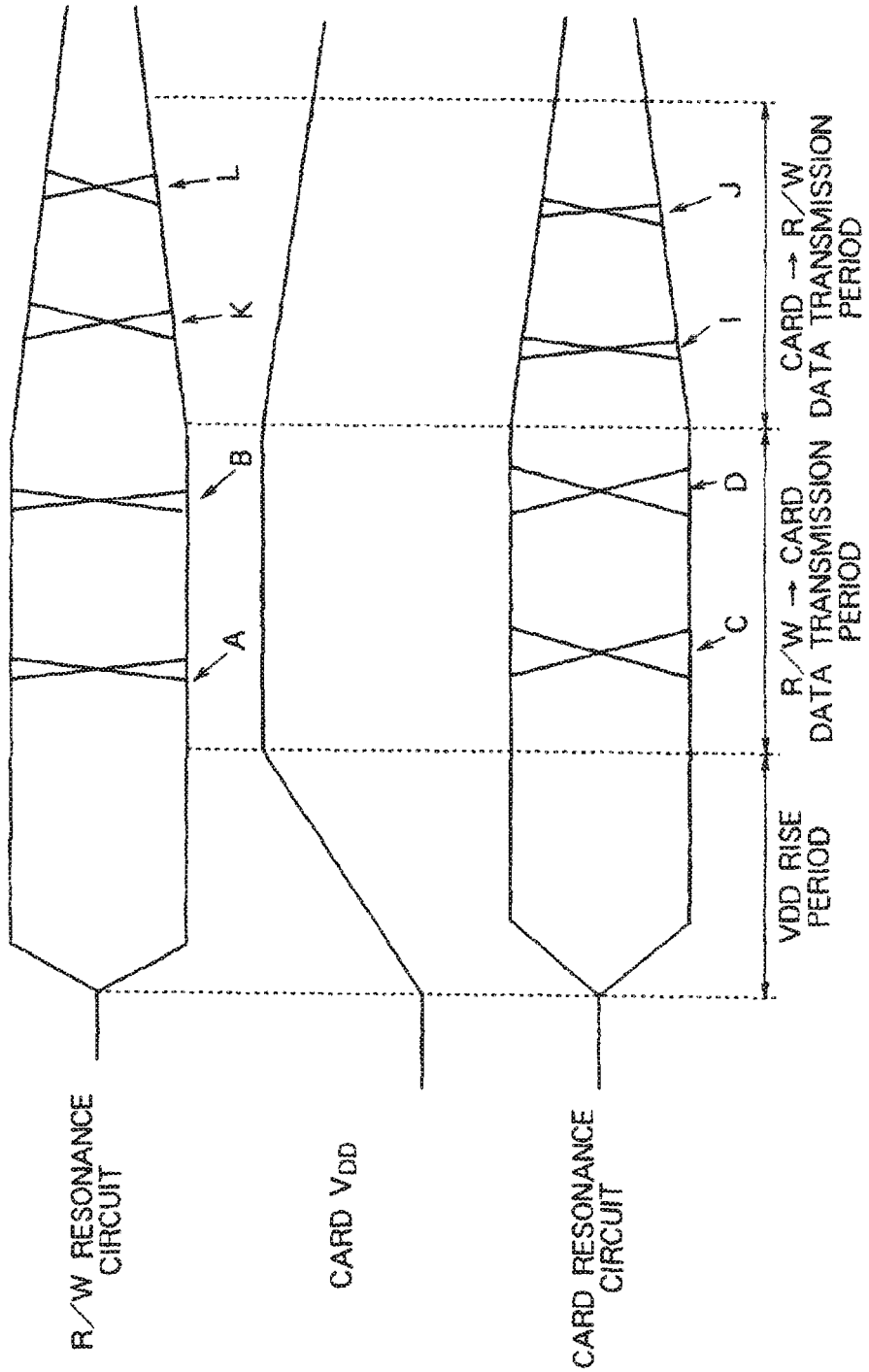


FIG. 15

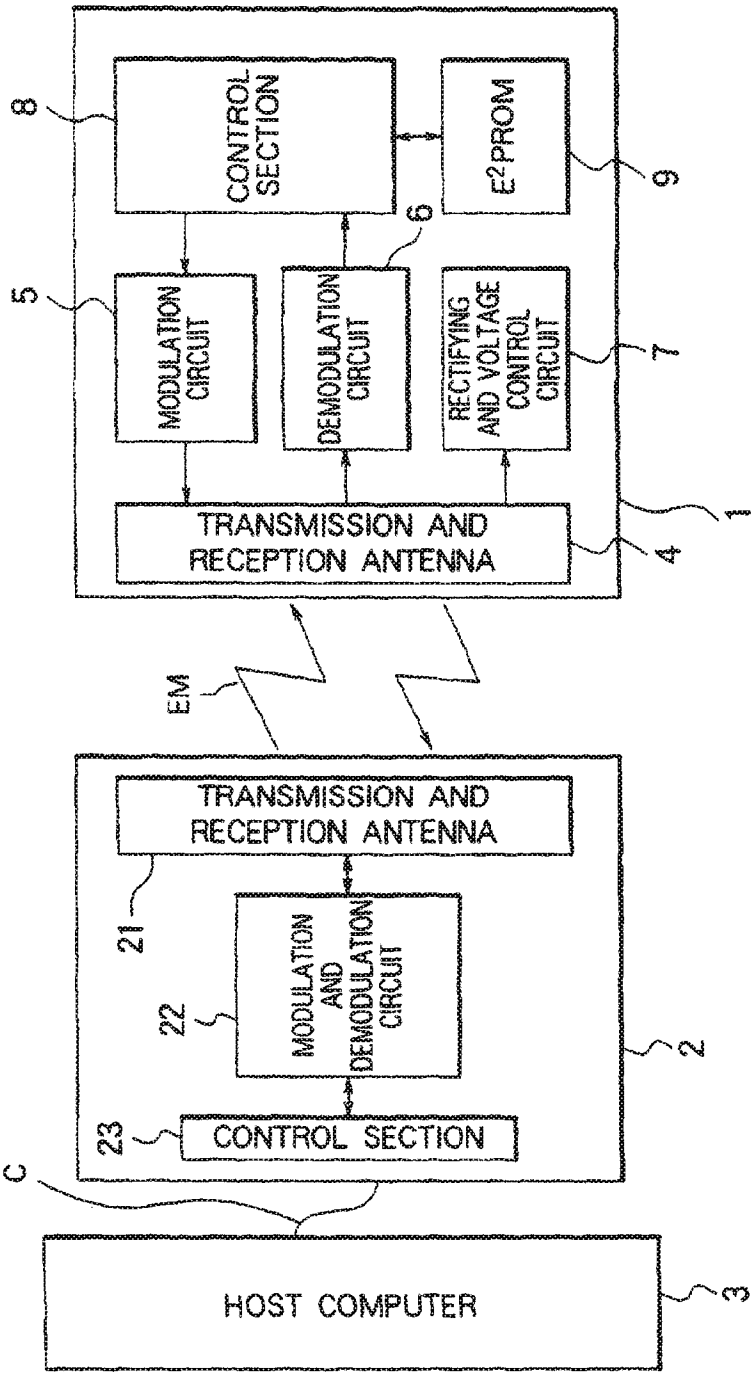
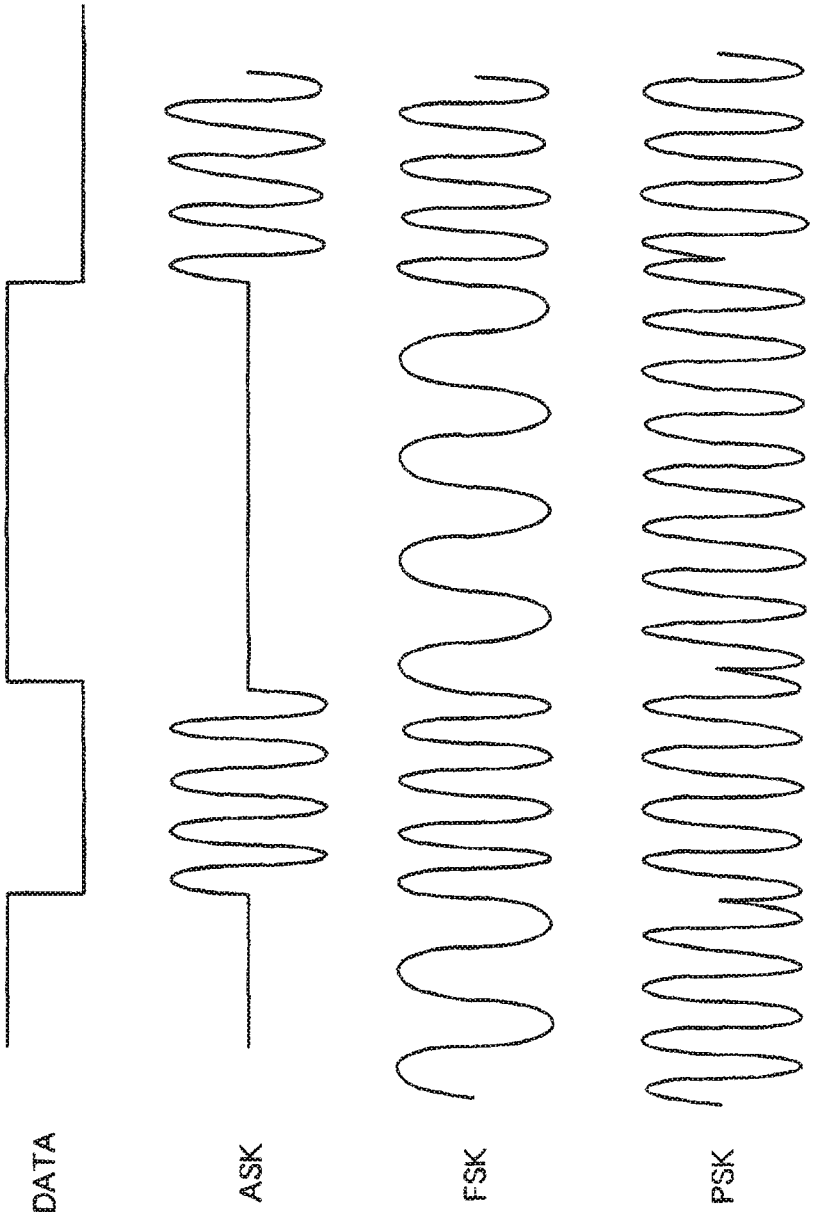

8
CONTROL SECTION
E²PROM
9
6
5
MODULATION CIRCUIT
DEMODULATION CIRCUIT
RECTIFYING AND VOLTAGE CONTROL CIRCUIT
7
TRANSMISSION AND RECEPTION ANTENNA
4
1
EM
TRANSMISSION AND RECEPTION ANTENNA
21
22
MODULATION AND DEMODULATION CIRCUIT
2
23
CONTROL SECTION
C
HOST COMPUTER
3

FIG. 16



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(54) **RICHTFUNKSYSTEM FÜR PUNKT-ZU-MEHRPUNKT VERBINDUNGEN**

RADIO LINK SYSTEM FOR POINT TO MULTI-POINT COMMUNICATION

SYSTEME DE RADIODIFFUSION PAR FAISCEAU DIRIGE, POUR COMMUNICATIONS ENTRE UN POINT ET PLUSIEURS POINTS

(84) Benannte Vertragsstaaten:
CH DE ES FR GB IT LI SE

(30) Priorität: **23.07.1994 DE 4426183**

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(56) Entgegenhaltungen:
EP-A- 0 169 713
EP-A- 0 568 291
WO-A-92/15164
WO-A-93/00751

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Beschreibung

Die vorliegende Erfindung betrifft ein Richtfunksystem für Punkt-zu-Mehrpunkt-Verbindungen, bei dem die für die Kommunikation zwischen einer Zentralstation und mehreren Teilnehmern zur Verfügung stehenden Frequenzkanäle bedarfsweise zuteilbar sind.

Ein solches Richtfunksystem ist im Mikrokwellen-Magazin, Vol. 10, No. 6, 1984, S. 629, 630 erwähnt. Bei Punkt-zu-Mehrpunkt-Richtfunkverbindungen läßt sich demnach die Frequenzbandausnutzung durch eine nur bedarfsweise Belegung des erforderlichen Freqenzbandes verbessern. Die Kommunikation zwischen der Zentralstation und den einzelnen Teilnehmern erfolgt entweder durch Vielfachzugriff im Frequenzmultiplex (FDMA) oder durch Vielfachzugriff im Zeitmultiplex (TDMA), wobei die Frequenzkanäle oder Zeitschlitze je nach Bedarf der Teilnehmer zugeteilt werden.

Aus EP 0 169 713 A3 ist ein Duplex-Übertragungssystem bekannt. Dabei erfolgt lediglich zwischen zwei Sende/Empfangs-Stationen eine Sprachübertragung entweder nur in eine Richtung (Simplex-Übertragung) oder in beide Richtungen (Duplex-Übertragung) gleichzeitig. Für eine Simplex-Übertragung wird ein Übertragungskanal zur Verfügung gestellt, der eine größere Bandbreite aufweist als jeder der zwei für eine Duplex-Übertragung bereitgestellten Übertragungskanäle. Dazu werden die Datenraten der übertragenen Signale an die Bandbreite der ihnen jeweils zugeordneten Übertragungskanäle angepaßt.

Bei einem aus der WO-A-93/00751 bekannten Datenübertragungssystem werden die Sendesignalpegel so geregelt, daß sich eine optimale Übertragungsqualität einstellt.

Der Erfindung liegt die Aufgabe zugrunde, ein Richtfunksystem der eingangs genannten Art anzugeben, dessen Übertragungskapazität möglichst flexibel an den Bedarf der Teilnehmer angepaßt werden kann.

Erfindungsgemäß wird diese Aufgabe durch die Merkmale des Anspruchs 1 gelöst. Vorteilhafte Weiterbildungen der Erfindung gehen aus den Unteransprüchen hervor.

Punkt-zu-Mehrpunkt Richtfunksysteme stellen eine kostengünstige und mit geringem Aufwand realisierbare Alternative zu leitergebundenen Übertragungssystemen dar. Dies gilt in besonderem Maße für neue Netzbetreiber im Rahmen des Aufbaus eigener Telekommunikationsinfrastruktur.

Ein nach der Erfindung ausgeführtes Punkt-zu-Mehrpunkt Richtfunksystem kann seine Übertragungsbandbreitenkapazität an verschiedene von den einzelnen Teilnehmern geforderte Datenübertragungsraten anpassen. Damit stellt ein solches System ein frequenzökonomisches, am Bedarf der einzelnen Teilnehmer orientiertes Übertragungsmedium dar.

Anhand eines in der Zeichnung dargestellten Ausführungsbeispiels wird nun die Erfindung näher erläutert.

Die Figur zeigt ein Frequenzkanalraster.

Ein Punkt-zu-Mehrpunkt Richtfunksystem besteht aus einer Zentralstation mit einer in Azimutrichtung rundstrahlenden oder sektorisiert strahlenden Antenne und mehreren Teilnehmern, welche mit Richtantennen ausgestattet sind. Prinzipiell weisen die Zentralstation und die einzelnen Teilnehmer in bekannter Weise Hochfrequenz-Sende/Empfangs-Baugruppen, Umsetzer von der Hochfrequenz- in die Zwischenfrequenzebene und im Zwischenfrequenzbereich arbeitende Modulatoren und Demodulatoren auf.

Die Modulatoren und Demodulatoren in der Zentralstation sind so ausgelegt, daß ein Zwischenfrequenzträger mit einer variablen Datenrate, z.B. im Bereich von 64 KBit/s bis maximal 8 MBit/s, modulierbar bzw. demodulierbar ist. D.h. die Zentralstation kann - z.B. softwaregesteuert - jedem Teilnehmer einen Frequenzkanal zur Verfügung stellen, dessen Bandbreite an die vom jeweiligen Teilnehmer geforderte Datenübertragungsrate angepaßt ist. Das in der Zeichnung dargestellte Frequenzkanalraster enthält beispielhaft zwei Frequenzkanäle 1 und 5 für eine Datenrate von 2 MBit/s, zwei weitere Frequenzkanäle 2 und 4 für eine Datenrate von 64 KBit/s und einen Frequenzkanal 3 für eine Datenrate von 1 MBit/s. Die Lage der einzelnen Kanäle relativ zu der Mittenfrequenz f_m des Übertragungsbandes wird zweckmäßigerweise so organisiert, daß die Kanäle symmetrisch um die Mittenfrequenz f_m herum verteilt sind (vgl. Figur). Die maximal mögliche Anzahl der den Teilnehmern zugeordneten Kanäle ist durch die Kanalrasterung, den zulässigen spektralen Abstand und die kanalindividuelle Datenrate bestimmt.

In der Zentralstation können die von den Teilnehmern geforderten Kanalbandbreiten registriert werden, damit für jeden Teilnehmer eine von der Übertragungsbandbreite abhängige Tarifierung möglich ist.

Modulatoren und Demodulatoren können auch für verschiedene Modulationsarten (z.B. n - PSK, n - QPSK mit n = 1 ... 8 oder M - QAM mit M = 4 ... 256) ausgelegt werden, so daß Datenübertragungen mit teilnehmerindividuell unterschiedlichen Modulationen möglich sind.

Um entfernungsabhängige Empfangspegelunterschiede ausgleichen zu können, ist in der Zentralstation eine entsprechende Verstärkungsregelung für die Sendesignale vorgesehen.

Patentansprüche

1. Richtfunksystem für Punkt-zu-Mehrpunkt Verbindungen, bei dem die für die Kommunikation zwischen einer Zentralstation und mehreren Teilnehmern zur Verfügung stehenden Frequenzkanäle bedarfsweise zuteilbar sind, dadurch gekennzeichnet, daß die Bandbreite der einzelnen Frequenzkanäle (1 ... 5) auf die von den einzelnen Teilnehmern jeweils geforderte Datenübertragungsrate einstellbar ist.

2. Richtfunksystem nach Anspruch 1, dadurch gekennzeichnet, daß die Verstärkung der Sendesignale regelbar ist, so daß entfernungsabhängige Unterschiede der Empfangssignalpegel ausgeglichen werden können.

3. Richtfunksystem nach Anspruch 1, dadurch gekennzeichnet, daß Modulatoren und Demodulatoren auf verschiedene Modulationsarten einstellbar sind.

4. Richtfunksystem nach Anspruch 1, dadurch gekennzeichnet, daß die Zentralstation für die einzelnen Teilnehmer eine von der Übertragungsbandbreite abhängige Tarifierung vornimmt.

Claims

1. Microwave system for point-to-multipoint links, in which the frequency channels which are available for communication between a central station and a plurality of subscribers can be assigned according to requirements, characterized in that the bandwidth of the individual frequency channels (1 ... 5) can be adjusted to the data transmission rate respectively required by the individual subscribers.

2. Microwave system according to Claim 1, characterized in that the amplification of the transmission signals can be regulated, so that distance-dependent differences in the reception signal levels can be compensated.

3. Microwave system according to Claim 1, characterized in that modulators and demodulators can be adjusted to different types of modulation.

4. Microwave system according to Claim 1, characterized in that the central station performs tariff metering for the individual subscribers as a function of the transmission bandwidth.

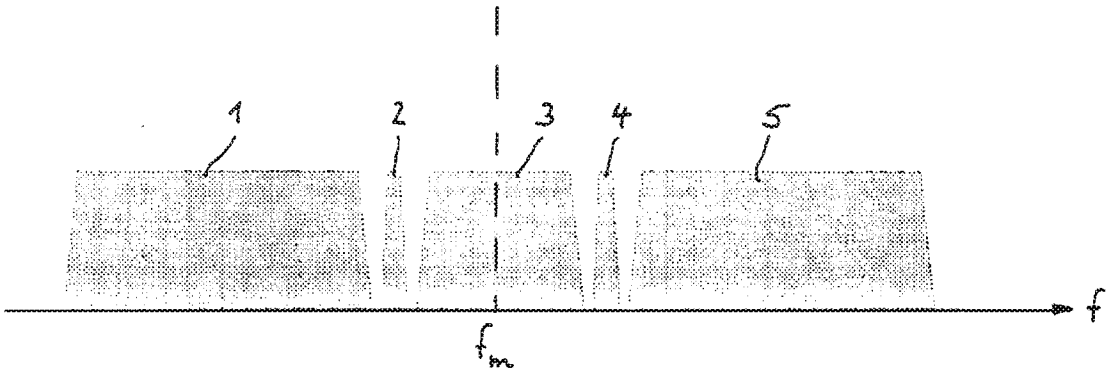
Revendications

1. Système de radiodiffusion par faisceau dirigé entre un point et plusieurs points, selon lequel les canaux de fréquence disponibles pour la communication entre une station centrale et plusieurs abonnés peuvent être attribués à la demande,
caractérisé en ce que
la largeur de bande des différents canaux de fréquence (1 ... 5) se règle sur le débit de données de transmission demandé par chacun des abonnés.

2. Système de radiodiffusion par faisceau dirigé selon la revendication 1,
caractérisé en ce que
l'amplification des signaux d'émission est réglable pour permettre de compenser des différences de niveau de signal de réception dépendant de l'éloignement.

3. Système de radiodiffusion par faisceau dirigé selon la revendication 1,
caractérisé en ce que
les modulateurs et démodulateurs peuvent être réglés sur différents types de modulation.

4. Système de radiodiffusion par faisceau dirigé selon la revendication 1,
caractérisé en ce que
la station centrale réalise une tarification dépendant de la largeur de la bande de transmission de chaque abonné.



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27.10.2004 Bulletin 2004/44

(51) Int Cl.7: **H04L 27/38**, H04Q 7/38

(21) Application number: **96118227.6**

(22) Date of filing: **13.11.1996**

(54) **Digital signal detecting method and detector**

Verfahren zum Erfassen eines digitalen Signals und Detektor

Procédé de détection d'un signal numérique et détecteur

(84) Designated Contracting States:
DE GB SE

(30) Priority: **16.11.1995 JP 29870795**

(43) Date of publication of application:
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(56) References cited:
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- **FINES P ET AL: "FULLY DIGITAL M-ARY PSK AND M-ARY QAM DEMODULATORS FOR LAND MOBILE SATELLITE COMMUNICATIONS" ELECTRONICS AND COMMUNICATION ENGINEERING JOURNAL, vol. 3, no. 6, 1 December 1991, pages 291-298, XP000277949**
- **AGHAMOHAMMADI A ET AL: "A NEW METHOD FOR PHASE SYNCHRONIZATION AND AUTOMATIC GAIN CONTROL OF LINEARLY MODULATED SIGNALS ON FREQUENCY-FLAT FADING CHANNELS" IEEE TRANSACTIONS ON COMMUNICATIONS, vol. 39, no. 1, 1 January 1991, pages 25-29, XP000220443**
- **SAMUELI H ET AL: "VLSI architectures for a high-speed tunable digital modulator/ demodulator/bandpass-filter chip set" 1992 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS (CAT. NO.92CH3139-3), SAN DIEGO, CA, USA, 10-13 MAY 1992, ISBN 0-7803-0593-0, 1992, NEW YORK, NY, USA , pages 1065-1068 vol.3, XP002069780**
- **DATABASE WPI Section EI, Week 9349 Derwent Publications Ltd., London, GB; Class U22, AN 93-390790 XP002069781 & JP 05 291 859 A (HITACHI LTD)**

Printed by Jouve, 75001 PARIS (FR)

Description

[0001] The present invention relates to a digital signal detecting method which permits the reception of signals modulated by different modulation schemes and send signals of various symbol transmission rates and a detector therefor.

[0002] To realize future multimedia communications, there is a demand for techniques of transmitting data, speech and images over the same digital radio channel. One possible means for effectively transmitting data, speech and images by digital radio communication is to use symbol transmission rates and modulation/demodulation schemes optimum for the objects to be transmitted. In the field of mobile communication, for instance, it is to be wished that the base station offer a service of providing still pictures of television, data bank or the like, whereas the mobile station be capable of receiving such still pictures from the base station by simple operation with simple equipment as well as conducting usual voice communications. In this instance, a QPSK modulation scheme is usually employed for the voice communication but a QAM or similar multilevel modulation scheme is needed for the transmission of still pictures because of the necessity for transmitting a larger amount of information than that required for the voice communication. This requirement could be met by providing independent transmitters and receivers each corresponding to a particular modulation/demodulation scheme as shown in Fig. 1A, in which the transmitting station is provided with a transmitter group 10 consisting of, for example, QAM, PSK and FSK modulating transmitters 11, 12 and 13 and the receiving station is provided with a receiver group 20 consisting of QAM, PSK and FSK receivers. Another method is common to the above in the provision of the independent transmitters 11, 12 and 13 at the transmitting side but differs therefrom in that the receiving station is equipped with a single receiver 21 with QAM, PSK and FSK detectors 22, 23 and 24 built therein as shown in Fig. 1B. One possible method for providing a plurality of detectors in the same radio as shown in Fig. 1B is to build therein independent detectors each designed specifically for one modulation/demodulation scheme.

[0003] At present, mobile communication services are allocated 800 and 1500 MHz bands but cannot be switched back and forth between them. If the bands can be switched by a simple operation with a simple structure, however, cochannel interference can be reduced by using the 800 MHz band outdoors and the 1500 MHz band indoors and in closed spaces through utilization of a property that the linearity of electric waves in the 1500 MHz band is higher than in the 800 MHz band.

[0004] The device configuration depicted in Fig. 1B has a plurality of independent detectors built-in, and hence it is inevitably bulky and complex. Furthermore, in the digital radio communication for transmitting data, speech and images, it is hard to instantaneously switch the independent detectors by dynamically changing the demodulating scheme and the carrier frequency. The receiver 21 quadrature-demodulates the received signal, for which it is necessary to generate a local oscillation signal synchronized with the carrier of the input received signal. In this instance, if the carrier frequency of the received signal varies from f_1 to f_2, f_3, and f_4 with the lapse of time as shown in Fig. 2A, the frequency of the local oscillation signal also needs to vary correspondingly. To meet this requirement, it is general practice in the prior art to employ such a method as shown in Fig. 2B, in which the oscillation frequency of a PLL local oscillator 25 is switched by switching means 17 to f_1, f_2, f_3 and f_4 one after another as indicated by local oscillators 25_1, 25_2, 25_3 and 25_4, then the output from the switched local oscillator and the input modulated signal are multiplied by an multiplier 18 and the multiplied output is applied to a filter 19 to obtain a base band signal. The frequency switching speed in the PLL local oscillator 25 is several milliseconds at the highest even by the use of a digital loop preset type frequency synthesizer. With such a low response speed, it is impossible to fully respond to the frequency switching during communication.

[0005] For example, when the symbol transmission rate of the received signal varies from B_1 to B_2, B_3, and B_4 with the lapse of time as shown in Fig. 2C, it is conventional that filters 261, 262, 263 and 264 for filtering the output from a quadrature demodulator are switched one after another by switching means 27 and 28 in response to the variation in the transmission rate of the received signal as depicted in Fig. 2D. Since the filters are formed by hardware, the filter switching speed cannot be increased because of transient characteristics of the filters.

[0006] US-A-5,259,000 discloses a modulator-demodulator constructed of digital circuits that is intended to provide a simple, economical modulator-demodulator apparatus, wherein two MODEMs are provided for G3 facsimile and G2/G1 facsimile which are selectively used by controlling a switch in accordance with the received signal. The functions of the respective facsimile modes are implemented by a digital signal processor, but it is assumed that different algorithms are used for different facsimile modes and the characteristics of each function that implements a corresponding facsimile mode are not changed. The document also shows the use of interpolation; however, the interpolation is performed to increase Signal-to-Noise Power Ratio to thereby avoid degradation in detection when the eye-pattern is closed by change in transmission rate or increase the in number of values of multi-value modulation (M-ary modulation scheme).

[0007] The document *Fines P et al: "Fully Digital M-ary PSK and M-ary QAM demodulators for land mobile satellite communications" Electronics and Communication Engineering Journal, Vol.3, No. 6, 1 December* 1991, *pages* 291-298, *XP000277949* discloses the use of an adaptive filter, and sets of coefficients of the adaptive filter are predetermined and stored in a memory. The document also teaches the use of interpolation, but the purpose is the same as that in

US-A-5,259,000.

[0008] US-A-3,497,625 relates to digital modulation and demodulation, wherein a desired one of plural types of modulation scheme (and demodulation scheme) is selectively operated.

[0009] The document D4 *SAMUELI H ET AL: "VLSI architectures* for a *high-speed tunable digital modulator/demodulator/bandpass filter chip set", 1992 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS (CAT. No. 92CH3139-3), SAN DIEGO, CA, USA, 10-13 MAY 1992, ISBN 0-7803-0593-0, 1992, NEW YORK, NY, USA, pages 1065-1068 vol.3, XP002069780* relates to an all-digital multirate modulator/demodulator of a 3-chip set, wherein in the first chip a double-sideband IF signal is subjected to a Hilbert transform to obtain a complex single-sideband signal, in the second chip the single-sideband signal is quadrature-demodulated to produce a baseband signal and in the third chip the baseband signal is decimated to effect lowpass-filtering of a selected bandwidth. The document D4 does not teach the use of interpolation and decimation for enhancing time-resolution of quadrature-demodulation.

[0010] It is therefore an object of the present invention to provide a digital signal detecting method and a detector therefor which enable digital communication equipment having a plurality of detecting means built-in to be used in common to pluralities of modulation/demodulation schemes, local oscillation frequencies and symbol transmission rates.

[0011] Another object of the present invention is to provide a digital signal detecting method and a detector therefor which are capable of responding fast to the switching of the modulation schemes and a change in the symbol transmission rate.

SUMMARY OF THE INVENTION

[0012] These objects are achieved by a method as claimed in claim 1 and a detector as claimed in claim 20. Preferred embodiments of the invention are subject-matter of the dpendent claims.

[0013] A feature of the present invention is to obtain a base band signal by subjecting an AD converted received signal to digital signal processing implemented by software.

[0014] The digital signal detecting method according to the present invention comprises: a quadrature-demodulating step of performing a quadrature-demodulating operation of an AD converted received modulated signal; a filtering step of performing a filtering operation of the quadrature-demodulated signal to obtain a base band signal; and a control step of changing at least one process variable in at least one of the quadrature-demodulating step and the filtering step in response to a request for changing the process variable.

[0015] The quadrature-demodulating step comprises: an interpolating step of performing an n-point interpolation of the input modulated digital signal to interpolate therein samples at n points (n being a real number equal to or greater than 1); a multiplying step of complex-multiplying the interpolation result by a local oscillation signal; and a decimating step of performing an n-point decimation of the multiplication result to decimate therefrom samples at n points. The process variables that can be changed in the quadrature demodulation step are the frequency, amplitude and phase of the local oscillation signal and the value of the above-mentioned n.

[0016] The filtering step comprises a smoothing step of smoothing the result of the quadrature-demodulating operation to reduce the number of samples; and a digital filtering step of performing a band-limiting operation of the result of the smoothing operation. The process variables in the band-limiting step are the number of smoothing points and the characteristic of the digital filter used.

[0017] Further, the input modulated signal is gain controlled by an automatic gain controller for input into an AD converter as a signal of a predetermined level range.

[0018] The above-mentioned various processes are performed by a microprocessor which decodes and executes programs.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019]

Fig. 1A is a block diagram schematically showing an example of a digital mobile radio communication system employing a plurality of different modulation/demodulation schemes;

Fig. 1B is a block diagram schematically showing an example of a digital mobile radio communication system employing a receiver which contains a plurality of detectors each corresponding to one of the modulation/demodulation schemes in Fig. 1A;

Fig. 2A is a graph showing variations in the carrier frequency of a received signal with the lapse of time;

Fig. 2B is a diagram showing a conventional method for changing the local oscillation frequency of a detector in response to the variations in the carrier frequency shown in Fig. 2A;

Fig. 2C is a graph showing variations in the symbol transmission rate of the received signal with the lapse of time;

Fig. 2D is a diagram showing a conventional method for switching band-limiting filters of a detector in response to the variations in the symbol transmission rate shown in Fig. 2C;
Fig. 3 is a block diagram illustrating the functional configuration of the detector according to the present invention;
Fig. 4A is a block diagram illustrating a concrete example of the functional construction of quadrature demodulating means 33 in Fig. 3;
Fig. 4B is a flowchart showing an example of a procedure for automatic synchronization of the local oscillation signal with the input received signal;
Fig. 5A is a diagram explanatory of n-point interpolation processing by an FFT technique;
Fig. 5B is a diagram explanatory of a method for performing the n-point interpolation processing by an interpolation algorithm using an m-order function;
Fig. 5C is a diagram explanatory of a method for performing the n-point interpolation processing by a method of estimating samples to be interpolated by an interpolation algorithm;
Fig. 6A is a diagram explanatory of n-point decimation processing by a simple decimation method;
Fig. 6B is a diagram explanatory of n-point decimation processing by a weighted substitution method;
Fig. 7 is a block diagram illustrating a concrete example of the functional configuration of filter means 43 in Fig. 3;
Fig. 8A is a diagram explanatory of smoothing processing by a simple extraction method;
Fig. 8B is a block diagram showing an example of the functional configuration for another smoothing scheme;
Fig. 8C is a diagram for explaining the operation of the Fig. 8B configuration;
Fig. 9A through 9H are diagrams showing the states of signals occurring at respective parts of the digital detector according to the present invention;
Fig. 10A is a block diagram illustrating an example of the functional configuration for switching the oscillation frequency in the quadrature demodulating means 33 in Fig. 3;
Fig. 10B is a block diagram showing an example of the functional configuration for switching the local oscillation frequency in the filter means 34 in Fig. 3;
Fig. 11 is a block diagram illustrating an example of the functional configuration for carrying out this invention method;
Fig. 12 is a flowchart showing an example of the procedure of the detecting method according to the present invention;
Fig. 13 is a flowchart showing an example of the digital detecting procedure;
Fig. 14 is a diagram showing an example of the frame structure of the received signal;
Fig. 15 is a block diagram illustrating an example of the functional configuration in which a microprocessor for use in the present invention is utilized for other processing;
Fig. 16 is a block diagram illustrating the functional configuration of a transceiver embodying the present invention;
Fig. 17A is a table showing, by way of example, stored contents of a process variable storage part;
Fig. 17B is a table showing, by way of example, some of other stored contents of the process variable storage part; and
Fig. 17C is a table showing, by way of example, stored contents in other areas of the storage part of Fig. 17B.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0020] Referring now to Fig. 3, an embodiment of the present invention will be described below. An analog signal received at an input terminal 30 is provided via a band pass filter (not shown) to an automatic gain controller 31, which controls, with its amplification gain, the received signal so that its amplitude varies within a fixed range. The output analog signal from the automatic gain controller 31 is converted by an AD converter 32 to a digital signal. The received signal thus converted into digital form is subjected to demodulating operation by quadrature demodulating means 33 and is spectrum shaped by filtering operation by digital filter means 34, from which a demodulated digital base band signal is provided at an output terminal 40. The base band signal is provided to decision means 39, wherein its in-phase component and quadrature component are each decided in terms of the symbol period, and based on these decision results, it is determined which signal point on the IQ-diagram the base band signal corresponds to. For example, in the case of a QPSK signal, it is decided whether its in-phase component and quadrature component are +1 or -1, and based on the decision results, it is determined which of four signal points on the IQ-diagram the baseband signal corresponds to.

[0021] In Fig. 3, the arithmetic processing for the digital signal by the quadrature demodulating means 33 and the digital filter means 34 is implemented by software which uses the sampling frequency, the symbol transmission rate, the modulation scheme and the local oscillation frequency as arguments (variables). Control means 35 has software for controlling the automatic gain controller 31, the quadrature demodulating means 33 and the digital filter means 34. The control means 35 controls the automatic gain controller 31 to vary its amplification gain to limit the amplitude variation of the base band signal to a fixed range. The control means 35 controls arguments set in the quadrature

demodulating means 33 and the digital filter means 34 in response to changes in the sampling frequency, the symbol transmission rate and the modulation scheme of the digitized modulated signal and the local oscillation frequency. A keyboard or similar set/input means 36 is connected to the control means 35. The set/input means 36 has pluralities of keys indicating several sampling frequencies, several symbol transmission rates and several local oscillation frequencies, respectively, and a desired parameter is input by pressing the corresponding one of the keys indicating several parameters of each category. Alternatively, the input means 36 is provided with keys each indicating the sampling frequency, the symbol transmission rate and the local oscillation frequency and has a construction in which a desired parameter can be input by pressing the corresponding key and its numerical value can be set and input by manipulating ten keys. Further, the set/input means 36 has a plurality of keys respectively indicating modulation schemes so that the modulation scheme of the received signal can be input.

[0022] As described above, the digital signal processing by the quadrature demodulating means 33 and the digital filter means 34, which uses the sampling frequency, the symbol transmission rate, the modulation scheme and the local oscillation frequency as variables, can be implemented by software. By controlling the gain of the automatic gain controller 31 and the variables with the software of the control means 35, it is possible to construct a digital signal detector which performs an operation corresponding to a parameter specified in one of the groups of modulation schemes, local oscillation frequencies and symbol transmission rates.

[0023] Fig. 4A shows a preferred configuration of the quadrature demodulating means 33 in Fig. 3. The output digital signal from the AD converter 32 is subjected to an n-point interpolation by n-point interpolation means 41_I and 41_Q, whereby samples are interpolated in the digital signal at n points on the time base. The interpolated signals are fed to multiplying means 42_I and 42_Q, wherein they are multiplied by 90°-out-of-phase signals $f_{LI}(k)$ and $f_{LQ}(k)$from local oscillation means 45. The outputs from the multiplying means 42_I and 42_Q are subjected to an n-point decimation by n-point decimation means 43_I and 43_Q, whereby samples are decimated from the multiplied outputs at n points on the time base. By this decimation processing, the samples interpolated by the n-point interpolation means 41_I and 41_Q are decimated from the multiplied outputs, whereby the in-phase and quadrature components of the demodulated signal from the quadrature demodulation means 33 can be obtained. The time resolution for the multiplication processing can be scaled up by the n-point interpolation means 41_I and 41_Q. The scaled-up time resolution permits the establishment of synchronization between the digitized modulated signals and the local oscillation signals with high accuracy, and the time resolution of the multiplied outputs is scaled down by the n-point decimation means 43_I and 43_Q, lessening the load of subsequent digital signal processing. The multiplying means 42_I and 42_Q constitute a complex multiplying means 42.

[0024] A description will be given of the arithmetic operation by the quadrature demodulating means 33. The input analog signal (an IF signal) y(t) to the AD converter 32 can be expressed by the following equation.

$$y(t) = A(t)\cos\{\omega t+\varphi(t)\} \tag{1}$$

where t is time, ω is $2\pi f$ (where f is the carrier frequency), A(t) is the envelope and $\varphi(t)$ is the phase. The analog signal y(t) is sampled by the AD converter 32 every sampling time T_s and each sample value is converted to a digital signal. Letting m denote an integer, the time t and the sampling time T_s bear the following relationship.

$$t= mT_s \tag{2}$$

The digital signal $y_s(mT_s)$ converted from the analog signal y(t) can be expressed as follows:

$$y_s(mT_s) = A_s(mT_s)\cos\{\omega mT_s+\varphi_s(mT_s)\} \tag{3}$$

where $A_s(mT_s)$ is a sampled value of the envelope at time mT_s and $\varphi_s(mT_s)$ is a sampled phase value of the phase φ (t) at time mT_s.

[0025] Normalizing the time in Eq. (3) with the sampling time T_s gives

$$y_s(m) = A_s(m)\cos\{\omega m+\varphi_s(m)\} \tag{4}$$

[0026] Next, the time sequence of digital signals given by Eq. (4) is subjected to an n-point interpolation operation to insert therein samples at n points, thereby interpolating the digitized received signals. The n-point interpolation result

y_u is given as follows:

$$y_u(k) = y_s(k/n) \tag{5}$$

$$= A_s(k/n)\cos\{\omega(k/n)+\varphi_s(k/n)\} \tag{6}$$

This interpolation value is calculated by the interpolation algorithm described later on. As the result of this, the amount of data of the interpolation result $y_u(k)$ on the time base becomes n times larger than the amount of data of the digital-signal time sequence $y_s(m)$.

[0027] The local oscillation means 45 outputs the local oscillation signal $f_L(k)$ synchronized with an angular velocity ω.

$$f_L(k) = B_L \exp\{j\omega(k/n)\} \tag{7}$$

where B_L is the amplitude of the local oscillation signal $f_L(k)$ and exp(•) is an exponential function, $f_L(k)$ being a complex number. The digital multiplying means 42 multiplies the n-point interpolation result $y_u(k)$ by the local oscillation signal $f_L(k)$.

$$z_u(k) = y_u(k) \cdot f_L(k) \tag{8}$$

[0028] The multiplication result $z_u(k)$ is the output from the multiplying means 42, which is a complex number. The multiplication result $z_u(k)$ is subjected to an n-point decimation operation by n-point decimation means 43 to decimate samples in the time sequence every n points. The decimation result z_d is as follows:

$$z_d(p) = z_u(pn) \tag{9}$$

$$= y_u(pn) \cdot f_L(pn) \tag{10}$$

$$= y_s(pn/n) \cdot f_L(pn) \tag{11}$$

$$= y_s(p) \cdot f_L(pn) \tag{12}$$

The number of samples of the interpolation result z_u on the time base becomes n/1 the number of samples of the multiplication result $z_u(k)$. As long as the n-point interpolation means 41 and the n-point decimation means 43 are used, the $z_d(p)$ sampling interval in the AD converter 32 always equals the sampling time T_s.

[0029] At the start of demodulation processing, the local oscillation signal $f_L(m'T_s)$ from the local oscillation means 45 is synchronized with the received signal, i.e. the input signal $y_s(mT_s)$ to the quadrature demodulation means 33 for accurate synchronous detection processing in order that the operation result by the quadrature demodulation means 33 may be processed as a demodulation result by the filter means 34,. This synchronization processing is carried out following the procedure shown in Fig. 4B, for instance. In the first place, the output which is obtained from each of the n-point interpolation means 41_I and 41_Q when n is set to zero, that is, the uninterpolated digital signal $y_s(mT_s)$, is multiplied by the local oscillation signal $f_L(m'T_s)$ (S1).

$$z_s(m) = y_s(mT_s) f_L(m'T_s) \tag{13}$$

$$z_s(m) = A_s(m)\cos(2\pi f m T_s + \theta) B_L \cos(2\pi f' m' T_s) \tag{14}$$

$$z_s(m) = (1/2)A_s(m)B_L[\cos(2\pi(fm-f'm')T_s+\theta) + \cos(2\pi(fm+f'm')T_s+q\theta)] \quad (15)$$

This zs(m) is subjected to low-pass filtering to extract a difference frequency component $\hat{z}_s(m)$ which is given by the following equation.

$$\hat{z}_s(m) = (1/2)A_s(m)B_L\cos[2\pi(fm-f'm')T_s+\theta] \quad (16)$$

Normalizing the amplitude and the initial phase in Eq. (16) gives

$$z'_s(m) = \cos(fm-f'm') \quad (17)$$

$2\pi f=\omega$ and $2\pi f'=\omega'$. The $z_s'(m)$ by Eq. (17) is called an evaluation function, and the local oscillation frequency f' is so controlled as to maximize the evaluation function $z_s'(m)$. That is, a check is made to see if the evaluation function has become maximum (S3), and if not, the frequency f' of the local oscillation signal $f_L(m'Ts)$ is adjusted so that the evaluation function $z_s'(m)$ becomes maximum, followed by a return to step S1 (S4). When the evaluation function $z_s'(m)$ becomes maximum, the input signals $y_s(mT_s)$ and the local oscillation signal $f_L(m'T_s)$ are subjected to n-point interpolation processing (S5), and the resulting interpolated signals $y_u(k\Delta)$ and $f_L(k'\Delta)$ (where $n\Delta=Ts$) are multiplied (S6). The multiplication result is subjected to low-pass filter processing to obtain the difference frequency component (S7). A check is made to see if an evaluation function $z_s'(k)=\cos(fk-fk')$ similar to that in step S3 is maximum (S8), and if not, it is determined whether the interpolation number n needs to be changed (S9); if not, the k' in the local oscillation signal $f_L(k'\Delta)$ is so adjusted as to maximize the evaluation function $z_s'(k)$, followed by a return to step S6 (S10). A check is made to see whether the interpolation number n needs to be changed, that is, whether the evaluation function $z_s'(k)$ is larger than a threshold value. If the evaluation function $z_s'(k)$ is larger than the threshold value and will hardly change even if the interpolation number n is increased, the interpolation number n is increased by 1 or so, followed by a return to step S5 (S11). When the evaluation value $z_s'(k)$ is maximum, it is decided that the received signal and the local oscillation signal are synchronized with each other, and synchronization control comes to an end.

[0030] When the evaluation function $z_s'(k)$ hardly increases even if the interpolation number n is increased, the interpolation number n of the smaller value is used in the subsequent processing, that is, the evaluation function $z_s'(k)$ is made maximum and the interpolation number n minimum for synchronization with high accuracy and for minimum computational complexity. In the above, since the adjustable minimum value of the local oscillation signal $z_s(k'\Delta)$ in step S10 is k'=1, i.e. the sample interval Δ after interpolation, the accuracy of synchronization of the local oscillation signal $f_L(m'T_s)$ with the input signal $y_s(mT_s)$ increases with an increase in the interpolation number n. Incidentally, low-pass filter means 101 in Fig. 4A is means for carrying out the processing of steps S2 and S7 in Fig. 4B.

[0031] Next, a description will be given of a concrete interpolation processing method for the interpolation means 41_I and 41_Q. As shown in Fig. 5A, the time sequence signal $y_s(m)$ of the sampling period T_s is transformed by fast-Fourier-transform (FFT) processing into a frequency domain signal y(f) for each period Ta, and a zero point is inserted into the signal y(f) on the frequency axis to obtain a signal y'(f), which is transformed by inverse fast-Fourier-transform (IFFT) processing into a time sequence signal $y_u(k)$ which has an increased number of samples per time Ta. This interpolation method by FFT ensures high reliability of signals interpolated when the number of interpolated samples is large. This method is described in, for example, Toshinori Yoshikawa et al., "Numerical Calculation in Engineering," pp. 183, Nihon Rikoh Kai, 1984.

[0032] Another method is shown in Fig. 5B, in which sample values which are determined by a linear function at+b or quadratic function at^2+bt+c are interpolated between adjacent actual sample values of the time sequence signal $y_s(m)$ for each period Ta as indicated by the broken line to obtain the time sequence signal $y_u(k)$ which has an increased number of samples per time Ta. Such a method of interpolating samples estimated by a linear m-order function is simple and easy. With this method, the computational complexity is low and reliability is relatively high when the number of interpolated samples is small.

[0033] It is also possible to use such a method as shown in Fig. 5C, in which Q previous samples of the time sequence signal $y_u(k)$ derived by interpolation from the time sequence signal $y_s(m)$ are used to estimate, by an adaptive algorithm, the samples to be interpolated next and the estimated samples are interpolated into the next time sequence signal $y_s(m)$ to obtain the time sequence signal $y_u(k)$. The adaptive algorithm for the estimation of samples needs only to have been optimized for or with respect to Gaussian noise; a Kalman Filter algorithm, least means squares algorithm, re-

cursive least square algorithm, Newton method, or steepest descent method can be used. With this method, it is possible to interpolate samples into the time sequence signal while compensating for the degradation of the signal by the transmission line to some extent.

[0034] Next, a concrete example of the decimation processing method by the decimation means 43_I and 43_Q in Fig. 4A will be described. For example, as shown in Fig. 6A, samples of the same number as those interpolated by each of the interpolating means 41_I and 41_Q are simply decimated from the time sequence signal $z_u(k)$ for each period Ta to obtain a time sequence signal $z_d(p)$ which has a decreased number of samples per time Ta. The processing by this method is very simple and easy.

[0035] Alternatively, as shown in Fig. 6B, an evaluation function is used to perform operation processing of a plurality Q (three in Fig. 6B) of samples in the time sequence signal $z_u(k)$ to obtain one sample, thus decimating samples in the time sequence signal $z_u(k)$ to obtain the time sequence signal $z_d(p)$. The evaluation function may be a function for calculating a mean value or centroids of a plurality of samples. With this method, information about the samples to be decimated can be reflected by the evaluation function on the samples left undecimated.

[0036] The digital filter means 34 in Fig. 3 performs a filtering operation and a smoothing operation. As shown in Fig. 7, the in-phase and quadrature component outputs from the quadrature demodulating means 33, that is, the outputs from the n-point decimation means 43_I and 43_Q in Fig. 4A, are smoothed by smoothing means 51_I and 51_Q, respectively, by which the number of samples on the time base is reduced within the range that meets the Nyquist sampling theorem. In other words, a plurality of samples is reduced by the averaging down to one. This enables decimation processing on the time base. Based on the processing results by the smoothing means 51_I and 51_Q, the orders of filter coefficients can be lowered by digital filter means 52_I and 52_Q, respectively. The smoothing of samples is expressed by the following equation.

$$z_{ds}(p_s) = g(...,z_d((k-1)p), z_d(kp),...) \tag{18}$$

where $g(\cdot)$ is a function indicating the smoothing processing, p_s a normalization variable of the output by the smoothing processing and z_{ds} a complex signal which is the output from the smoothing means 51. The smoothing processing averages signals at m points, for example, to reduce the number of samples down to 1/m. The signal $z_{ds}(p_s)$ is band-limited by the filter means 52. This is expressed by the following equation.

$$\hat{z}(p_s) = h(z_{ds}(p_s)) \tag{19}$$

where $h(\cdot)$ is a signal processing function of the filter means 52, $\hat{z}$ the filter processing output signal and $\hat{z}(\cdot)$ a complex number. The quadrature demodulating operation, the smoothing operation and the filtering operation may be carried out as a complex operation for each of the in-phase and the quadrature component as shown in Figs. 4 and 7; alternatively, such a complex operation as indicated by the above equations may directly be conducted.

[0037] A concrete method for the processing by the smoothing means 51 in Fig. 7 will be described. Fig. 8A shows the simplest method according to which N samples are decimated from the time sequence signal $z_d(p)$ from the quadrature demodulating means 33 every N+1 samples to obtain the smoothed time sequence signal $z_{ds}(p_s)$. Smoothing processing by a linearly weighting scheme is shown in Fig. 8B, in which the time sequence signal $z_{ds}(p)$ is fed directly to multiplying means M_0 (Fig. 8C) and, at the same time, it is applied to delay means D_1, ..., D_L, from which signals delayed by sampling periods T_s, $2T_s$, ..., Lt_s of the time sequence signal $z_d(p)$, respectively, are provided to multiplying means M_1, ..., M_L. The inputs into the multiplying means M_0, M_1, ..., M_L are multiplied by weights f_0, f_1, ..., f_L, respectively, then the multiplication results are added together by adder means S_u, and the addition result is output therefrom as the time sequence signal $z_{ds}(p_s)$ smoothed every L+1 samples. That is, the signal $z_{ds}(p)$ is assigned the weights f_0, ..., f_L every L samples, then added together to form one sample of the smoothed signal $z_{ds}(p_s)$.

$$z_{ds}(p_s) = f_0 \cdot z_d(p) + f_1 \cdot z_d(p-1) + ... + f_L \cdot Zd(p-L)$$

When L=3, four samples $z_d(p-s)$ to $z_d(p)$ are linearly weighted and output as one sample $z_{ds}(p_s)$ as shown in Fig. 8C.

[0038] To perform the smoothing processing by the adaptive filtering scheme, the weighting coefficients f_0, ..., f_L are changed by adaptive algorithm processing means 50 through the use of an adaptive algorithm so as to optimize the decision result from the received data decision means as indicated by the broken lines in Fig. 8C. The weighting coefficients are determined first, for example, in a pilot signal (training signal) period in which received data is already known. The adaptive algorithm for use in this case may be a Kalman Filter algorithm or those derived therefrom.

[0039] Next, a description will be given, with reference to Fig. 9, of a specific operative example of a method for detecting signals of different modulation schemes according to the present invention. A received analog signal shown in Fig. 9A, whose amplitude component is limited to a certain range by the automatic gain controller 31 (Fig. 3), is converted by the AD converter 32 to a digital signal shown in Fig. 9B. The local oscillation means 45, placed under software control, generates local oscillation signals of in-phase and quadrature components depicted in Figs. 9C and D. The digital signal of Fig. 9B and the local oscillation signals of Figs. 9C and D are multiplied by the multiplying means 42I and 42_Q, respectively. As a result, the in-phase and the quadrature component of the output from the quadrature demodulation means 33 become such as depicted in Figs. 9E and 9F. The thus multiplied in-phase and quadrature components are spectrum shaped by the independent digital filter means 34 placed under software control. In consequence, the spectrum-shaped baseband signal has such in-phase and quadrature components as shown in Figs. 9G and 9H. In this way, even if the modulation scheme or mode of the send signal changes from QPSK to 16QAM and BPSK one after another at time intervals as short as 4 milliseconds during transmission, the signal can accurately be reproduced by the digital signal detector of the present invention. This modulated signal is transmitted and received at rates of 2 bits by QPSK, 4 bits by 16QAM and 1 bit by BPSK per symbol. Thus, the digital signal detector of the present invention implements the detection of signals in the variable-bit transmission. In this example, it is preknown that the QPSK, 16QAM and BPSK modulated signals are sequentially received every 4 milliseconds, and the control means 35 switches variables for respective means in synchronization with the received signals.

[0040] To switch the local oscillation frequency in response to the change in the modulation scheme, the control means 35 sends a frequency switching command to the local oscillation means 45 as shown in Fig. 10A. The local oscillation means 45 is implemented basically by software, and for the designated frequency f, an operation $f_{L1}B_L\exp(j2\pi fmT_s)$ is performed. In the case of switching the frequency as shown in Fig. 2A, the control means 35 instructs the local oscillation means 45 to switch the oscillation frequency in order f_1-f_2-f_3-f_4. This instruction is executed in an instruction execution cycle of a microprocessor which executes software in principle. Hence, the local oscillation frequency can be switched fast in as short a time as several nanoseconds. As will be seen from the above, according to the present invention, the frequency of the local oscillation means 45 can be switched faster than in the past and the frequency switching during communication can be fully dealt with, besides the invention is also applicable to fast frequency hopping for dynamic switching of the carrier frequency.

[0041] In response to a change in the symbol transmission rate, too, the present invention similarly changes the characteristic of the filter means 34 through a program of software; the instruction to change the transmission rate is provided by the control means 35. That is, the filter means 34 and the control means 35 implement digital signal processing by software. For example, when the transmission rate varies as shown in Fig. 2C, the symbol transmission rates B1, B2, B3 and B4 are sequentially indicated from the control means 35 to the filter means 34 as depicted in Fig. 10B. Accordingly, the transmission rate is varied in an instruction execution cycle of a microprocessor which executes software in principle. Thus, according to the present invention, the characteristic of the filter means 34 can be changed by the control means 35 at high speed. The characteristic control of the filter means 34 is effected according to the modulation mode of the received signal as well. For example, when the modulation mode changes as shown in Fig. 9G, the roll-off of the filter characteristic is changed to 0.5 for QPSK, 0.3 for 16QAM and 0.5 for BPSK.

[0042] As described above, various processes involved in the present invention are performed by software operations. That is, as shown in Fig. 11, a microprocessor 37 in the control means 35 decodes and executes a program 38 in the control means 35 to control the automatic gain controller 31, the quadrature demodulation means 33 and the digital filter means 34. The automatic gain controller 31 is controlled as follows. The output level of the automatic gain controller 31 is detected by a level detector (not shown), the detected level is converted to a digital value, which is compared with a reference value in the microprocessor 37, and the amplification gain is controlled step by step to bring the output of the automatic gain controller 31 into a predetermined range of amplitude variations. The control of the quadrature demodulation means 33 is effected by controlling the local oscillation means 45, the n-point interpolation means 41 and the n-point decimation means 43. As regards the local oscillation means 45, the frequency f, phase φ and amplitude B_L of the local oscillation signal are designated by the microprocessor 37. For the n-point interpolation means 41 and the n-point decimation means, the sampling frequency $1/T_s$ and the numbers n of interpolation and decimation points are designated. The digital filter means 34 is controlled through the smoothing means 51 and the digital filter means 52. For the smoothing means 51, the sampling frequency $1/T_s$, the number of smoothing points and the smoothing method are designated. For the digital filter means 52, the sampling frequency $1/T_s$, the filter coefficient and the number of symbols necessary for filtering are designated. That is, once the carrier frequency of the input modulated signal of the AD converter 32 is set and input, the minimum value of its sampling frequency $1/T_s$ is automatically determined in accordance with the input carrier frequency. For example, when the carrier frequency of the input modulated signal is 130 MHz, the minimum value of the sampling frequency of the AD converter 32 is set at 260 MHz. For accurate synchronization with the carrier of the input modulated signal, the local oscillation signal needs to be a digital signal of a sampling frequency at least four times higher than the carrier frequency of the input modulated signal; therefore, the numbers n of interpolation points and decimation points are automatically determined. Where the

conversion rate of the AD converter 32 is high, it is also possible to sample the input modulated signal above the minimum sampling frequency to reduce the number n of samples to be interpolated and decimated correspondingly.

[0043] When the frequency of the demodulated baseband signal is, for example, 20 KHz, the sampling frequency necessary for this signal processing may be 40 RHz; since the quadrature demodulation means 33 outputs an unnecessarily large number of signals, these signals are effectively used to perform processing by the smoothing means 51 to produce a base band signal as faithful to them as possible and decrease its sampling frequency. The number of smoothing points in this case is automatically determined by the set carrier frequency of the input modulated signal and the set symbol transmission rate. As described previously with reference to Figs. 2D and 10B, an appropriate filter characteristic is needed in accordance with the symbol transmission rate, and hence the filter coefficient and the number of symbols necessary for filtering are automatically determined by the set symbol transmission rate. Further, the filter coefficient is automatically determined, depending on the set modulation mode as mentioned previously. Thus, programs are prepared so that various parameters (variables) for the filter means 34, the local oscillation means 45, the interpolation means 41 and the decimation means 43 are automatically designated in accordance with the carrier frequency, the symbol transmission rate and the modulation mode which are set on the basis of the above-mentioned relations.

[0044] In the present invention, it is possible to employ what is called distributed processing system in which microprocessor are provided for the quadrature demodulation means 33 and the digital filter means 34, these microprocessors supplied with the above-mentioned various parameters (variables) designated by the microprocessor 37 and use them as arguments to execute programs for interpolation, quadrature demodulation and decimation and programs for smoothing and filter processing, respectively. Of course, such distributed processing system may be substituted with a centralized processing system in which the microprocessor 37 itself designates first the parameters for the respective means and executes the interpolation, quadrature demodulation, decimation, smoothing and filtering programs on a time-sharing basis, thereby performing virtually parallel processing.

[0045] Fig. 12 is a flowchart showing the procedure of the digital detector. The procedure begins with making a check to see if a request is made for a variable change (S1). Such a variable change request is made when a change in the carrier frequency or symbol transmission rate is newly set and input via set/input means 36, or when the time of changing the modulation mode arrives which is preknown as described previously with reference to Fig. 9, or when switching between the 800 Mhz and 1500 MHz or between audio and still picture information is input via the set/input means as referred to previously in the section "BACKGROUND OF THE INVENTION." Fig. 14 is explanatory of the case where the received signal is a 3-channel time division multiplex signal. The frame for each channel is composed of a preamble 71 and data 72 as shown in Fig. 14B. The preamble 71 is composed of a synchronization word 73 and a base station number 74 together with modulation system information 75 such as the modulation scheme of the data used in the data frame 72 and the symbol transmission rate as shown in Fig. 14C. For example, in the case where the modulation scheme of the data in the data frame 72 is newly designated, the variable change request is considered to be made when the data indicating the modulation scheme is demodulated.

[0046] When such a variable change request is made, the variables to be changed and their values are determined to comply with the request (52). For example, when the request is made for changing the variables for quadrature demodulation, the newly determined variables such as the number n of interpolation points, the local carrier frequency and its amplitude and phase are set as arguments in the processor which executes the quadrature demodulation program (S3). This is followed by the execution of the digital detection program (S4).

[0047] Fig. 13 shows the procedure for digital detection. In the first place, the received signal is subjected to automatic gain control by the automatic gain controller 31 in Fig. 11 so that the level of the received signal falls within a predetermined range (S1). The thus gain-controlled received signal is converted by the AD converter 32 to a digital signal (S2), which is subjected to an n-point interpolation (S3), and the thus interpolated digital signal is subjected to the quadrature demodulation operation (S4). The demodulation result is subjected to n-point decimation processing (S5) and then smoothing processing (S6), and the smoothing result is subjected to low-pass filter processing (S7). This is followed by a signal point decision to decide which signal point on the IQ plane corresponds to the result of the low-pass filter processing (S8).

[0048] As depicted in Fig. 15, the digital detector 53 of the present invention built in a radio, a radio channel controller 54 and an audio encoding/decoding processor 55 may be placed under the time sharing control of the microprocessor 37. Control programs 38, 56 and 57 are prepared which are exclusive to the digital detector 53, the radio channel controller 54 and the audio encoding/decoding processor 55, respectively. The microprocessor 37 switches each of the digital detector 53, the radio channel controller 54, the audio encoding/decoding processor 55 and its control program at proper time intervals on a time sharing basis. Accordingly, a plurality of objects of control can be processed by the single microprocessor 37. Incidentally, this radio is a mobile station of a mobile communication system, for instance, and the radio channel controller 54 performs switching between control and communication channels.

[0049] Fig. 16 illustrates a digital radio communication transceiver which has the digital detector of the present invention built-in, the parts corresponding to those in Fig. 3 being identified by the same reference numerals. The received

modulated signal from an antenna 60 is amplified by a low-noise amplifier 61, then converted by frequency converting means 62 to an intermediate-frequency (IF) signal, which is band limited by a filter 63, thereafter being fed to the automatic gain controller 31. That is, the received signal is applied to the digital detector of the present invention, shown in Fig. 3, and the detected output, i.e. the output from the filter means 34 is applied to the radio channel controller 54, from which it is fed to an exchange of a network (not shown), for instance. A signal from the exchange is fed via the radio channel controller 54 to filter means 64, wherein it is band limited. The band-limited signal is applied to quadrature modulating means 65, wherein its IF carrier is quadrature-modulated. The modulated output, i.e. the modulated signal is converted by a DA converter 66 to an analog signal, which is further converted by a frequency converter 67 to a high-frequency signal. The high-frequency modulated signal is power amplified by a transmitting power amplifier 68 for transmission from an antenna 69.

[0050] Next, concrete examples of the present invention will be described.

(i) Mobile Multimedia:

[0051] Here, the control operation of the present invention will be described with respect to the cases where the mode setting is (1) manually changed by the user of a mobile station, (2) automatically changed by a command from a base station, and (3) automatically changed according to an autonomous decision by the mobile station. Now, let it be assumed that the audio service is of a conventional PDC (Personal Digital Cellular) system whereas multimedia service (service of receiving broadcast still pictures, for instance) is of a multilevel modulation system (160QAM, for instance). The transmission bandwidth is supposed not to change with the services. Further, assume that the service is switched from a speech to a still picture mode and that the media service is being broadcast in a predetermined frequency band.

[0052] (1) When switching the reception of the audio service to the media service such as still picture, the user of the mobile station changes the service mode of the mobile station. This change is made by a dial key or mode switch provided in the set/input means 36 (Fig. 11). When supplied with a request signal for mode switching from the audio to the media service mode, for instance, the control means 35 of the mobile station changes the process variables of a synthesizer (not shown) for channel selection, the gain controller 31, the quadrature demodulation means 33 and the filter means 34. In the synthesizer, its frequency is set in a predetermined frequency band. In the gain controller 31, the setting of the maximum amplitude of its input signal is changed. That is, since the modulation mode is switched from QPSK to QAM, the maximum set value of the input signal is made larger than in that for QPSK. For the quadrature demodulation means 33 the setting of the numbers n of interpolation points and decimation points is changed. The value n is made larger than that for QPSK. The process variable of the filter means 34 that are changed are the smoothing method, the filter coefficient and the filter order. In this instance, a plurality of smoothing methods optimum for the modulation schemes used are prepared and algorithms of these optimum smoothing methods are prestored in a ROM. Based on the service mode switching signal applied thereto, the control means 35 reads out of the ROM the smoothing method optimum for the specified mode and performs smoothing processing accordingly. The roll-off rate of the filter means 52 (Fig. 7) is made lower than in the case of QPSK and, at the same time, its coefficient and order are also changed.

[0053] With a view to changing various process variables according to the mode being set, control means 35 includes process variable storage part 102 and a smoothing method storage part 103 as shown in Fig. 11. In the process variable storage part 102, for example, as shown in Fig. 17A, there are stored for each of the audio and the picture mode, the maximum amplitude value of the automatic gain controller, the number n of interpolation points, the number of the ROM having stored therein an algorithm for smoothing processing, the roll-off rate and filter coefficient of the filter means. In accordance with the mode set and input, the control means 35 reads out these variables and uses them for respective particular purposes. In the smoothing method storage part 103 there are stored the numbers of the ROMS which have stored therein algorithms or procedures necessary for the execution of various smoothing processes. In order to receive services other than the audio and picture or visual services, process variables for such service modes may be stored in the process variable storage part 102.

[0054] (2) The user of the mobile station changes the service mode setting of the mobile station by the set/input means 36 as in the case (1). Upon receipt of the service mode change request, the control means 35 of the mobile station transmits it, together with a flag indicating the mode change, over a transmission channel for communication with the base station. To set a flag is to make a predetermined bit 0 or 1 on the transmission frame a 1 or 0. When receiving the service change request flag from the mobile station (a request for media service in this example), the base station sends transmission information on the media service via a down-link channel to the mobile station. The mobile station detects the transmission information from the base station by the radio channel controller 54 (Fig. 16). In the thus detected transmission information there are contained the modulation scheme and the transmission rate to be used in the data frame of the radio channel, the time slot in the TDMA frame to be used, and so forth. The mobile station and the base station exchanges signals over the radio channel several times concerning the new service mode,

as required. The detected transmission information is input as a variable change request signal into the control means 35. The control means 35 changes the variables for the synthesizer, the gain controller, the quadrature demodulation means and the filter means. The contents to be changes are the same as those in the case (1).

[0055] In this instance, the process variable storage part 102 is designed so that the maximum amplitude value, the interpolation point number n and the ROM number of the smoothing method are read out in accordance with the modulation mode specified by the base station as shown in Fig. 17B and the roll-off rate and the filter coefficient are read out in accordance with the symbol transmission rate specified by the base station as shown in Fig. 17C.

[0056] (3) The user of the mobile station changes the setting of the service mode of the mobile station as in the case (1). In this case, several combinations of modulation schemes and symbol transmission rates are predetermined for each of the audio and media services and are assigned different mode numbers, and the respective process variables are stored in the process number storage part 102 in correspondence with the mode numbers as shown in Fig. 17A. The relationships of the mode numbers to the modulation schemes and the symbol transmission rates are also held in the base station. When a service mode change is set and input, the control means 35 transmits a code indicating the number of the set mode to the base station over the transmission channel for communication therewith. Further, the control means 35 reads out of the storage part 102 the process variables corresponding to the set and input mode and uses the read-out process variables to perform detection processing.

[0057] The base station receives and responds to the mode number indicating the newly set service mode to change the setting of the modulation scheme, the transmission rate and the time slot of the TDMA frame which are used in the radio channel for the transmission of information to the mobile station. As required, the mobile station and the base station exchange signals over the radio channel several times concerning the service mode to be newly changed.

(ii) Compatible Mobile Station

[0058] Here, the control operation of the present invention will be described with respect to the cases where the mode setting is (1) manually changed by the user of a mobile station, (2) automatically changed by a command from a base station, and (3) automatically changed according to an autonomous decision by the mobile station. Assume that the mobile station has gone indoors (a closed space like an underground shopping center). Suppose that the mobile station receives the PDC audio service outdoors and 16QAM media service indoors and that the transmission band remains unchanged.

(1) The user changes the communication mode setting of the mobile station when he goes indoors. This is done using a dial key or dedicated mode change switch of the set/input means 36. Upon receipt of a communication mode change request, the control means 35 changes the setting of the oscillation frequency of the synthesizer. For example, when the 800 MHz band is used outdoors and 1500 MHz band indoors, the local oscillation frequency to be supplied to the frequency converter for conversion to an IF signal is changed for use in the 1500 MHz band. Since the modulation scheme is switched from QPSK to 16QAM as is the case with the mobile multimedia (i), the control means 35 makes the maximum amplitude value of the gain controller large, sets the number n of interpolation and decimation points in the quadrature demodulation to a value larger than in the case of QPSK, uses a ROM having stored the optimum smoothing method, makes the roll-off rates of the filter means 64 at the sending side (Fig. 16) and the filter means 34 at the receiving side (Fig. 16) small, and changes their filter coefficients.

(2) The user of the mobile station changes the communication mode setting of the mobile station by the set/input means 36 when he goes indoors. The mobile station flags a communication mode change signal on the transmission frame of the radio channel to the base station. The base station receives the service change request flag from the mobile station and supplies it with transmission information about the communication mode over the downlink channel. The mobile station detects the transmission information from the base station by the radio channel controller 54. In the detected transmission information there are contained the carrier frequency, the modulation scheme, the transmission rate and the time slot of the TDMA frame which are used in the radio channel. Based on the transmission information, the mobile station changes the process variables which are used in the synthesizer, the quadrature modulation means, the gain controller, quadrature demodulation means and the filter means. The contents of the changes are the same as in the case (1).

(3) As in the cases (1) and (2), the user of the mobile station changes the setting of the communication mode of the mobile station when he goes indoors. In this instance, there are predetermined a plurality of modes corresponding to several combinations of modulation schemes and symbol transmission rates, and the mobile station informs the base station of changing the communication mode setting through the radio channel. The base station responds to the signal from the mobile station to set a predetermined communication mode. At this time, the settings are the carrier frequency, modulation scheme, transmission rate and the time slot of the TDMA frame which are used in the radio channel. The base station and the mobile station exchange signals several times over the radio channel and then communicate with each other in the newly set communication mode. Based on the

newly set communication mode, the mobile station reads the process variable storage part 102 and changes the variables which are used in the synthesizer, the quadrature demodulation means, the gain controller,the quadrature demodulation means and the filter means. The contents of these changes are the same as in the cases (1) and (2).

[0059] In the above, the variables to be used in the gain controller 31, the quadrature demodulation means 33 and the digital filter means 34 are all changed according to every mode switching. This is a preferred example. For example, when the modulation scheme is changed to QAM, at least the maximum amplitude value of the gain controller 31 is changed to ensure accurate detection of the amplitude value of the received signal and the other variables need not be changed. In the case of switching to the QPSK modulation scheme, the change of the maximum value of the gain controller 31 need not be given priority because the amplitude information is not used. The change of the roll-off rate in the filter means 34 and the corresponding changes of the filter coefficient and filter order are relatively important. Next in the order of importance comes the number of interpolation points, followed by the choice of the smoothing method. The necessity of changing the variables decreases in descending order of their importance.

[0060] While in the above the present invention has been described as being applied to the reception of radio signals, the invention is also applicable to the reception of signals in a wired communication system in which the modulation scheme and the symbol transmission rate are switched to those optimum for each information. In such an instance, the automatic gain controller 31 can be dispensed with.

[0061] As will be appreciated from the above, the present invention is advantageous over the prior art as listed below.

(i) A plurality of modulation schemes can be dealt with;
(ii) A plurality of local oscillation frequencies can be dealt with:
(iii) A plurality of symbol transmission rates can be dealt with;
(iv) Variable bit transmission and variable symbol rate transmission can be implemented with one receiver;
(v) A completely quadrature demodulated wave can be generated; and
(vi) The invention is applicable to fast frequency hopping.

Claims

1. A method of digitally detecting a signal, comprising:

an AD conversion step of converting a received modulated analog signal to a digital signal;
a quadrature demodulation step of performing a digital quadrature-demodulating operation on said digital signal using a local oscillation frequency of a local oscillation signal as a process variable;
a filtering step of performing a digital low-pass filtering operation on said quadrature-demodulated digital signal using filter characteristics as process variables; and
a control step of changing, in response to a process variable change request, at least one process variable in at least one of said quadrature demodulation step, for changing the local oscillation frequency in accordance with a carrier frequency, and said filtering step, for changing the filter characteristics according to the modulation scheme and transmission rate of the modulated signal;

characterized by

an interpolation step of performing n-point interpolation processing on said digital signal resulting from said AD conversion step to interpolate therein samples at n points to produce an n-point interpolated digital signal to be quadrature-demodulated in said quadrature demodulation step, said n being a real number equal to or greater than 1;
a multiplication step of complex-multiplying the n-point interpolated digital signal by said local oscillation signal; and
a decimation step of performing n-point decimation processing on a digital signal resulting from the complex-multiplication to decimate therefrom samples at n points.

2. The method of claim 1, wherein said filtering step comprises:

a smoothing step of performing smoothing processing on the result of said quadrature demodulation to reduce the number of samples on the time base; and
a digital filter step of performing band-limiting operation on the result of said smoothing processing using said filter characteristics.

3. The method of claim 1, wherein said interpolation step is a step of performing discrete Fourier transform processing on said digital signal and performing inverse discrete Fourier transform on the result of said Fourier transform processing after adding thereto a zero coefficient to obtain said result of said interpolation processing.

4. The method of claim 1, wherein said interpolation step is a step of performing a linear interpolation which approximates an m-th order function to said digital signal and interpolates therein samples which fit said m-th order function.

5. The method of claim 1, wherein said interpolation step is a step of interpolating samples estimated by an adaptive algorithm used for those preceding them in said digital signal every predetermined number of samples.

6. The method of claim 1, wherein said decimation step is a step of decimating from said multiplication result said samples interpolated at said n points in said interpolation step.

7. The method of claim 1, wherein said decimation step is a step of calculating a mean value or centroid of a plurality of samples in a sequence of samples of said multiplication result to obtain one sample.

8. The method of claim 1, further comprising a step of synchronizing said local oscillation signal with said digital signal.

9. The method of claim 8, wherein said synchronizing step comprises the steps of:

synchronizing the local oscillation frequency of said local oscillation signal with said digital signal; and
time-synchronizing said frequency-synchronized local oscillation signal with said n-point interpolated digital signal.

10. The method of claim 1, wherein said at least one process variable in said quadrature demodulation step is the number n of interpolation points.

11. The method of claim 1, wherein said at least one process variable in said quadrature demodulation step is the local oscillation frequency of said local oscillation signal.

12. The method of claim 21, wherein said at least one process variable in said filter step is the number of smoothing points used to reduce said number of samples.

13. The method of claim 2, wherein said at least one process variable in said filter step is a filter characteristic in said digital filter step.

14. The method of any one of claims 2 and 8 to 13, further comprising a gain control step of controlling the maximum amplitude of said received modulated signal to be a set value which is said at least one process variable.

15. The method of claim 14, further comprising:

a process variable change request detecting step of detecting a process variable change request;
a process variable determining step of responding to said process variable change request to determine which process variable is to be changed and its value; and
a step of changing said process variable to said determined variable.

16. The method of claim 15, wherein each of said steps is executed by decoding and executing a program.

17. The method of claim 16, wherein said process variable determining step is a step of reading out a prestored process variable in response to said variable change request.

18. The method of claim 17, wherein said variable change request is input by manipulating set/input means.

19. The method of claim 17, wherein said process variable change request detecting step is a step of detecting said process variable change request from a received signal.

20. A digital signal detector comprising:

an AD converter (32) for converting a received modulated analog signal to a digital signal;
quadrature demodulation means (33) for performing a digital quadrature demodulating operation on said digital signal using a digital local oscillation signal of a local oscillation frequency as a process variable;
filter means (34) for performing a digital low-pass filter operation on the quadrature demodulated digital signal using filter characteristics as process variables;
input means (36) for inputting a process variable change request for changing a process variable; and
control means (35) responsive to said process variable change request to change at least one process variable in at least one of said quadrature demodulation means, for changing the local oscillation frequency in accordance with a carrier frequency, and said filter means (34) for changing the filter characteristics according to the modulation scheme and transmission rate;

characterized by

interpolating means (41I, 41Q) for performing n-point interpolation processing on said digital signal from said AD converter (32) to interpolate therein samples at n points to produce an n-point interpolated digital signal to be quadrature-demodulated by said quadrature demodulation means (33), said n being a real number equal to or greater than 1;
local oscillation means (45) for generating said digital local oscillation signal through digital operation;
multiplying means (42) for complex-multiplying the n-point interpolated digital signal by said digital local oscillation signal; and
decimating means (43I, 43Q) for performing n-point decimation processing on a digital signal resulting from said complex-multiplication to decimate therefrom samples at said n points.

21. The detector of claim 20, wherein said filter means (34) comprises:

smoothing means (51) for smoothing the output from said quadrature demodulation means (33) and for performing an operation for reducing the number of samples of said output; and
digital filter means (52) for performing a band-limiting operation on the result of said operation by said smoothing means (51) using said filter characteristics.

22. The detector of claim 21, further comprising an automatic gain controller (31) provided at a stage preceding said AD converter (32), for controlling the gain of said received modulated signal so that its maximum amplitude becomes a set value which is one of said process variables that can be changed by said control means (35).

23. The detector of claim 22, further comprising a storage part (102) having prestored therein a comparative table of variable change requests and process variables, and wherein said control means (35) is means responsive to said process variable change request to read out said storage part and to change the process variable corresponding to said read-out one.

24. The detector of claim 23, wherein said input means (36) is set/input means for inputting said process variable change request by a manual operation.

25. The detector of claim 23, wherein said input means is means (36) for detecting said process variable change request from a received signal.

26. The detector of any one of claims 20 to 25, wherein said control means (35) comprises a program and a microprocessor for decoding and executing said program.

27. The detector of claim 26, wherein said control means (35) serves also as control means of a digital radio transceiver.

Patentansprüche

1. Verfahren zum digitalen Erfassen eines Signals, das Folgendes umfasst:

einen AD-Wandlungsschritt des Wandelns eines empfangenen modulierten Analogsignals in ein Digitalsignal;
einen Quadratur-Demodulationsschritt des Ausführens einer digitalen Quadratur-Demodulationsoperation an dem Digitalsignal unter Verwendung eines lokalen Oszillationssignals einer lokalen Oszillationsfrequenz als

einer Prozessvariablen;
einen Filterschritt des Ausführens einer digitalen Tiefpass-Filteroperation an dem quadratur-demodulierten Digitalsignal unter Verwendung von Filtercharakteristika als Prozessvariablen; und
einen Steuerschritt des Änderns, als Antwort auf eine Prozessvariablenänderungsanfrage, wenigstens einer Prozessvariablen in dem Quadratur-Demodulationsschritt, um die lokale Oszillationsfrequenz in Übereinstimmung mit einer Trägerfrequenz zu ändern, und/oder dem Filterschritt, um die Filtercharakteristika in Übereinstimmung mit dem Modulationsschema und der Übertragungsrate des modulierten Signals zu ändern;

gekennzeichnet durch

einen Interpolationsschritt des Ausführens einer n-Punkt Interpolationsverarbeitung an dem Digitalsignal, das aus dem AD-Wandlungsschritt resultiert, um darin Abtastwerte an n Punkten zu interpolieren, um ein n-Punkt-interpoliertes Digitalsignal zu erzeugen, das in dem Quadratur-Demodulationsschritt quadraturdemoduliert wird, wobei n eine reelle Zahl ist, die gleich oder größer ist als 1;
einen Multiplikationsschritt des komplexen Multiplizierens des n-Punkt-interpolierten Digitalsignals mit dem lokalen Oszillationssignal; und
einen Dezimierungsschritt des Ausführens einer n-Punkt Dezimierungsverarbeitung an einem Digitalsignal, das aus der komplexen Multiplikation resultiert, um daraus Abtastwerte an n Punkten zu dezimieren.

2. Verfahren nach Anspruch 1, bei dem der Filterschritt folgendes umfasst:

einen Glättungsschritt des Ausführens einer Glättungsverarbeitung an dem Ergebnis der Quadraturdemodulation, um die Anzahl der Abtastwerte auf der Zeitachse zu reduzieren; und
einen digitalen Filterschritt des Ausführens einer bandbegrenzenden Operation an dem Ergebnis der Glättungsverarbeitung unter Verwendung der Filtercharakteristika.

3. Verfahren nach Anspruch 1, bei dem der Interpolationsschritt ein Schritt des Ausführens einer diskreten Fouriertransformationsverarbeitung an dem Digitalsignal und einer inversen diskreten Fouriertransformation an dem Ergebnis der Fouriertransformationsverarbeitung nach Hinzuaddieren eines Nullkoeffizienten ist, um das Ergebnis der Interpolationsverarbeitung zu erhalten.

4. Verfahren nach Anspruch 1, bei dem der Interpolationsschritt ein Schritt des Ausführens einer linearen Interpolation ist, welche eine Funktion m-ter Ordnung an das Digitalsignal annähert und darin Abtastwerte interpoliert, welche zu der Funktion m-ter Ordnung passen.

5. Verfahren nach Anspruch 1, bei dem der Interpolationsschritt ein Schritt des Interpolierens von Abtastwerten, die von einem adaptiven Algorithmus geschätzt werden, der auf die ihnen in dem Digitalsignal vorangegangenen angewendet wird, nach jeder vorbestimmten Zahl von Abtastwerten ist.

6. Verfahren nach Anspruch 1, bei dem der Dezimierungsschritt ein Schritt des Dezimierens der in dem Interpolationsschritt an den n Punkten interpolierten Abtastwerte von dem Multiplikationsergebnis ist.

7. Verfahren nach Anspruch 1, bei dem der Dezimierungsschritt ein Schritt des Berechnens eines Mittelwertes oder Schwerpunktes einer Mehrzahl von Abtastwerten in einer Folge von Abtastwerten des Multiplikationsergebnisses zum Erhalten eines Abtastwerts ist.

8. Verfahren nach Anspruch 1, das weiter einen Schritt des Synchronisierens des lokalen Oszillationssignals mit dem Digitalsignal enthält.

9. Verfahren nach Anspruch 8, bei dem der Synchronisationsschritt die folgenden Schritte umfasst:

Synchronisieren der lokalen Oszillationsfrequenz des lokalen Oszillationssignals mit dem Digitalsignal; und
Zeitsynchronisieren des frequenzsynchronisierten lokalen Oszillationssignals mit dem n-Punkt-interpolierten Digitalsignal.

10. Verfahren nach Anspruch 1, bei dem wenigstens eine Prozessvariable in dem Quadratur-Demodulationsschritt die Anzahl n der Interpolationspunkte ist.

11. Verfahren nach Anspruch 1, bei dem wenigstens eine Prozessvariable in dem Quadratur-Demodulationsschritt die lokale Oszillationsfrequenz des lokalen Oszillationssignals ist.

12. Verfahren nach Anspruch 21, bei dem wenigstens eine Prozessvariable in dem Filterschritt die Anzahl der Glättungspunkte ist, an denen die Anzahl der Abtastwerte reduziert werden soll.

13. Verfahren nach Anspruch 2, bei dem wenigstens eine Prozessvariable in dem Filterschritt eine Filtercharakteristik in dem digitalen Filterschritt ist.

14. Verfahren nach einem der Ansprüche 2 und 8 bis 13, das weiter einen Verstärkungssteuerungsschritt des Steuerns der maximalen Amplitude des empfangenen modulierten Signals auf einen Sollwert umfasst, der die wenigstens eine Prozessvariable ist.

15. Verfahren nach Anspruch 14, das weiter umfasst:

einen Prozessvariablenänderungsanfrage-Erfassungsschritt des Erfassens einer Prozessvariablenänderungsanfrage;
einen Prozessvariablenbestimmungsschritt des Antwortens auf die Prozessvariablenänderungsanfrage, um die zu ändernde Prozessvariable und deren Wert zu bestimmen; und
einen Schritt des Änderns der Prozessvariablen zu der bestimmten Variable.

16. Verfahren nach Anspruch 15, bei dem jeder der Schritte durch Dekodieren und Ausführen eines Programms ausgeführt wird.

17. Verfahren nach Anspruch 16, bei dem der Prozessvariablenbestimmungsschritt ein Schritt des Auslesens einer vorab gespeicherten Prozessvariablen als Antwort auf die Variablenänderungsanfrage ist.

18. Verfahren nach Anspruch 17, bei dem die Variablenänderungsanfrage durch Handhaben eines Setz-/Eingabemittels eingegeben wird.

19. Verfahren nach Anspruch 17, bei dem der Prozessvariablenänderungsanfrage-Erfassungsschritt ein Schritt zum Erfassen der Prozessvariablenänderungsanfrage von einem empfangenen Signal ist.

20. Digitaler Signaldetektor, der Folgendes umfasst:

einen AD-Wandler (32) zum Wandeln eines empfangenen modulierten Analogsignals in ein Digitalsignal;
ein Quadratur-Demodulationsmittel (33) zum Ausführen einer digitalen Quadratur-Demodulationsoperation an dem Digitalsignal unter Verwendung eines digitalen lokalen Oszillationssignals mit einer lokalen Oszillationsfrequenz als einer Prozessvariablen;
ein Filtermittel (34) zum Ausführen einer digitalen Tiefpass-Fitteroperation an dem quadratur-demodulierten Digitalsignal unter Verwendung von Filtercharakteristika als Prozessvariablen;
ein Eingabemittel (36) zum Eingeben einer Prozessvariablenänderungsanfrage zum Ändern einer Prozessvariablen; und
Steuermittel (35), die auf die Prozessvariablenänderungsanfrage zum Ändern wenigstens einer Prozessvariablen in dem Quadratur-Demodulationsmittel, um die lokale Oszillationsfrequenz in Übereinstimmung mit einer Trägerfrequenz zu ändern, und/oder dem Filtermittel (34), um die Filtercharakteristika in Übereinstimmung mit dem Modulationsschema und der Übertragungsrate zu ändern, ansprechen;

gekennzeichnet durch

ein Interpolationsmittel (411, 41Q) zum Ausführen einer n-Punkt-Interpolationsverarbeitung an dem Digitalsignal von dem AD-Wandler (32), um darin Abtastwerte an n Punkten zu interpolieren, um ein n-Punkt-interpoliertes Digitalsignal für die Quadratur-Demodulation **durch** das Quadratur-Demodulationsmittel (33) zu erzeugen, wobei n eine reelle Zahl ist, die gleich oder größer ist als 1;
ein lokales Oszillationsmittel (45) zum Erzeugen des digitalen lokalen Oszillationssignals **durch** digitale Operation;
ein Multiplikationsmittel (42) zur komplexen Multiplikation des n-Punkt-interpolierten Digitalsignals mit dem digitalen lokalen Oszillationssignal; und

ein Dezimierungsmittel (431, 43Q) zum Ausführen einer n-Punkt-Dezimierungsverarbeitung an dem Digitalsignal, das aus der komplexen Multiplikation resultiert, um daraus Abtastwerte an den n Punkten zu dezimieren.

21. Detektor nach Anspruch 20, wobei das Filtermittel (34) folgendes umfasst:

ein Glättungsmittel (51) zum Glätten der Ausgabe von dem Quadratur-Demodulationsmittel (33) und zum Ausführen einer Operation zum Reduzieren der Anzahl der Abtastwerte der Ausgabe; und
ein digitales Filtermittel (52) zum Ausführen einer bandbegrenzenden Operation an dem Ergebnis der Operation des Glättungsmittels (51) unter Verwendung der Filtercharakteristika.

22. Detektor nach Anspruch 21, der ferner einen automatischen Verstärkungsregler (31) umfasst, der in einer dem AD-Wandler (32) vorangehenden Stufe vorgesehen ist, zum Regeln der Verstärkung des empfangenen modulierten Signals, so dass dessen maximale Amplitude zu einem Sollwert wird, der eine der Prozessvariablen ist, die durch das Steuermittel (35) geändert werden kann.

23. Detektor nach Anspruch 22, der ferner ein Speicherteil (102) umfasst, in dem eine Vergleichstabelle von Variablenänderungsanfragen und Prozessvariablen vorab gespeichert ist, und bei dem das Steuermittel (35) ein Mittel ist, das auf die Prozessvariablenänderungsanfrage anspricht, um aus dem Speicherteil auszulesen, und um die Prozessvariable entsprechend der ausgelesenen zu ändern.

24. Detektor nach Anspruch 23, bei dem das Eingabemittel (36) ein Setz-/Eingabemittel zum Eingeben der Prozessvariablenänderungsanfrage durch eine manuelle Operation ist.

25. Detektor nach Anspruch 23, bei dem das Eingabemittel ein Mittel (36) zum Erfassen der Prozessvariablenänderungsanfrage von einem empfangenen Signal ist.

26. Detektor nach einem der Ansprüche 20 bis 25, bei dem das Steuermittel (35) ein Programm und einen Mikroprozessor zum Entschlüsseln und Ausführen dieses Programms umfasst.

27. Detektor nach Anspruch 26, bei dem das Steuermittel (35) auch als Steuermittel eines digitalen Funk-Sender-Empfängers dient.

Revendications

1. Procédé pour détecter un signal de façon numérique, comprenant :

une étape de conversion A/N consistant à convertir en un signal numérique un signal analogique modulé reçu;
une étape de démodulation en quadrature consistant à effectuer une opération de démodulation en quadrature numérique sur le signal numérique en utilisant une fréquence d'oscillation locale d'un signal d'oscillation locale en tant que variable de processus;
une étape de filtrage consistant à effectuer une opération de filtrage passe-bas numérique sur le signal numérique démodulé en quadrature, en utilisant des caractéristiques de filtre en tant que variables de processus; et
une étape de commande consistant à changer, en réponse à une demande de changement de variable de processus, au moins une variable de processus dans l'une au moins de l'étape de démodulation en quadrature, pour changer la fréquence d'oscillation locale conformément à une fréquence porteuse, et de l'étape de filtrage, pour changer les caractéristiques de filtre conformément à la technique de modulation et au débit de transmission du signal modulé;

caractérisé par

une étape d'interpolation consistant à effectuer un traitement d'interpolation à n points sur le signal numérique résultant de l'étape de conversion A-N, pour interpoler dans celui-ci des échantillons à n points, pour produire un signal numérique interpolé à n points devant être démodulé en quadrature dans l'étape de démodulation en quadrature, n étant un nombre réel égal ou supérieur à 1;
une étape de multiplication consistant à effectuer une multiplication complexe du signal numérique interpolé

à n points par le signal d'oscillation locale; et
une étape de décimation consistant à effectuer un traitement de décimation à n points sur un signal numérique résultant de la multiplication complexe, pour décimer à partir de celui-ci des échantillons à n points.

2. Procédé selon la revendication 1, dans lequel l'étape de filtrage comprend :

une étape de lissage consistant à effectuer un traitement de lissage sur le résultat de la démodulation en quadrature pour réduire le nombre d'échantillons sur la base de temps; et
une étape de filtrage numérique consistant à effectuer une opération de limitation de bande sur le résultat du traitement de lissage, en utilisant les caractéristiques de filtre.

3. Procédé selon la revendication 1, dans lequel l'étape d'interpolation est une étape consistant à effectuer un traitement de transformation de Fourier discrète sur le signal numérique et à effectuer une transformation de Fourier discrète inverse sur le résultat du traitement de transformation de Fourier, après lui avoir ajouté un coefficient zéro pour obtenir le résultat du traitement d'interpolation.

4. Procédé selon la revendication 1, dans lequel l'étape d'interpolation est une étape consistant à effectuer une interpolation linéaire qui forme une approximation du signal numérique avec une fonction du m-ième ordre, et interpole dans celui-ci des échantillons qui sont ajustés à la fonction du m-ième ordre.

5. Procédé selon la revendication 1, dans lequel l'étape d'interpolation est une étape consistant à interpoler des échantillons estimés par un algorithme adaptatif utilisé pour ceux qui les précèdent dans le signal numérique, à chaque nombre prédéterminé d'échantillons.

6. Procédé selon la revendication 1, dans lequel l'étape de décimation est une étape consistant à décimer à partir du résultat de multiplication les échantillons interpolés auxdits n points dans l'étape d'interpolation.

7. Procédé selon la revendication 1, dans lequel l'étape de décimation est une étape consistant à calculer une valeur moyenne ou un centroïde d'une multiplicité d'échantillons dans une séquence d'échantillons du résultat de multiplication, pour obtenir un échantillon.

8. Procédé selon la revendication 1, comprenant en outre une étape consistant à synchroniser le signal d'oscillation locale avec le signal numérique.

9. Procédé selon la revendication 8, dans lequel l'étape de synchronisation comprend les étapes suivantes :

on synchronise la fréquence d'oscillation du signal d'oscillation locale avec le signal numérique; et
on effectue une synchronisation temporelle du signal d'oscillation locale synchronisé en fréquence avec le signal numérique interpolé à n points.

10. Procédé selon la revendication 1, dans lequel l'au moins une variable de processus dans l'étape de démodulation en quadrature est le nombre n de points d'interpolation.

11. Procédé selon la revendication 1, dans lequel l'au moins une variable de processus dans l'étape de démodulation en quadrature est la fréquence d'oscillation locale du signal d'oscillation locale.

12. Procédé selon la revendication 21, dans lequel l'au moins une variable de processus dans l'étape de filtrage est le nombre de points de lissage utilisés pour réduire le nombre d'échantillons.

13. Procédé selon la revendication 2, dans lequel l'au moins une variable de processus dans l'étape de filtrage est une caractéristique de filtre dans l'étape de filtrage numérique.

14. Procédé selon l'une quelconque des revendications 2 et 8 à 13, comprenant en outre une étape de commande de gain consistant à commander l'amplitude maximale du signal modulé reçu de façon qu'elle soit une valeur fixée qui est l'au moins une variable de processus.

15. Procédé selon la revendication 14, comprenant en outre :

une étape de détection de demande de changement de variable de processus consistant à détecter une demande de changement de variable de processus;
une étape de détermination de variable de processus consistant à réagir à la demande de changement de variable de processus en déterminant quelle variable de processus doit être changée, et sa valeur; et
une étape de changement de la variable de processus pour qu'elle devienne la variable déterminée.

16. Procédé selon la revendication 15, dans lequel chacune des étapes est exécutée en décodant et en exécutant un programme.

17. Procédé selon la revendication 16, dans lequel l'étape de détermination de variable de processus est une étape consistant à lire une variable de processus préenregistrée, en réponse à la demande de changement de variable.

18. Procédé selon la revendication 18, dans lequel la demande de changement de variable est introduite en manipulant un moyen de fixation / d'entrée.

19. Procédé selon la revendication 17, dans lequel l'étape de détection de demande de changement de variable de processus est une étape consistant à détecter la demande de changement de variable de processus à partir d'un signal reçu.

20. Détecteur de signal numérique, comprenant :

un convertisseur A/N (32) pour convertir en un signal numérique un signal analogique modulé reçu;
un moyen de démodulation en quadrature (33) pour effectuer une opération de démodulation en quadrature numérique sur le signal numérique en utilisant un signal d'oscillation locale numérique d'une fréquence d'oscillation locale, en tant que variable de processus;
un moyen de filtrage (34) pour effectuer une opération de filtrage passe-bas numérique sur le signal numérique démodulé en quadrature, en utilisant des caractéristiques de filtre en tant que variables de processus;
un moyen d'entrée (36) pour introduire une demande de changement de variable de processus pour changer une variable de processus; et
un moyen de commande (35) réagissant à la demande de changement de variable de processus en changeant au moins une variable de processus dans l'un au moins du moyen de démodulation en quadrature, pour changer la fréquence d'oscillation locale conformément à une fréquence porteuse, et du moyen de filtrage (34) pour changer les caractéristiques de filtre conformément à la technique de modulation et au débit de transmission;

caractérisé par

un moyen d'interpolation (41I, 41Q) pour effectuer un traitement d'interpolation à n points sur le signal numérique provenant du convertisseur A/N (32), pour interpoler à l'intérieur des échantillons à n points, pour produire un signal numérique interpolé à n points devant être démodulé en quadrature par le moyen de démodulation en quadrature (33), le nombre n étant un nombre réel égal ou supérieur à 1;
un moyen d'oscillation locale (45) pour générer le signal d'oscillation locale numérique par l'intermédiaire d'une opération numérique;
un moyen de multiplication (42) pour effectuer une multiplication complexe du signal numérique interpolé à n points, par le signal d'oscillation locale numérique; et
un moyen de décimation (43I, 43Q) pour effectuer un traitement de décimation à n points sur un signal numérique résultant de la multiplication complexe, pour décimer à partir de celui-ci des échantillons auxdits n points.

21. Détecteur selon la revendication 20, dans lequel le moyen de filtrage (34) comprend :

un moyen de lissage (51) pour lisser le signal de sortie du moyen de démodulation en quadrature (33) et pour effectuer une opération pour réduire le nombre d'échantillons du signal de sortie; et
un moyen de filtrage numérique (52) pour effectuer une opération de limitation de bande sur le résultat de l'opération effectuée par le moyen de lissage (51), en utilisant lesdites caractéristiques de filtre.

22. Détecteur selon la revendication 21, comprenant en outre une unité de commande automatique de gain (31) placée à un étage qui précède le convertisseur A/N (32), pour commander le gain du signal modulé reçu, de façon que

son amplitude maximale devienne une valeur fixée qui est l'une des variables de processus qui peuvent être changées par le moyen de commande (35).

23. Détecteur selon la revendication 22, comprenant en outre un élément de stockage (102) dans lequel est préenregistrée une table comparative de demandes de changement de variable et de variables de processus, et dans lequel le moyen de commande (35) est un moyen qui réagit à la demande de changement de variable de processus en lisant l'élément de stockage et en changeant la variable de processus correspondant à celle qui est lue.

24. Détecteur selon la revendication 23, dans lequel le moyen d'entrée (36) est un moyen de fixation / d'entrée pour introduire la demande de changement de variable de processus, par une opération manuelle.

25. Détecteur selon la revendication 23, dans lequel le moyen d'entrée est un moyen (36) pour détecter la demande de changement de variable de processus à partir d'un signal reçu.

26. Détecteur selon l'une quelconque des revendications 20 à 25, dans lequel le moyen de commande (35) comprend un programme et un microprocesseur pour décoder et exécuter le programme.

27. Détecteur selon la revendication 26, dans lequel le moyen de commande (35) remplit également la fonction d'un moyen de commande d'un émetteur-récepteur de radio numérique.

FIG. 1A PRIOR ART

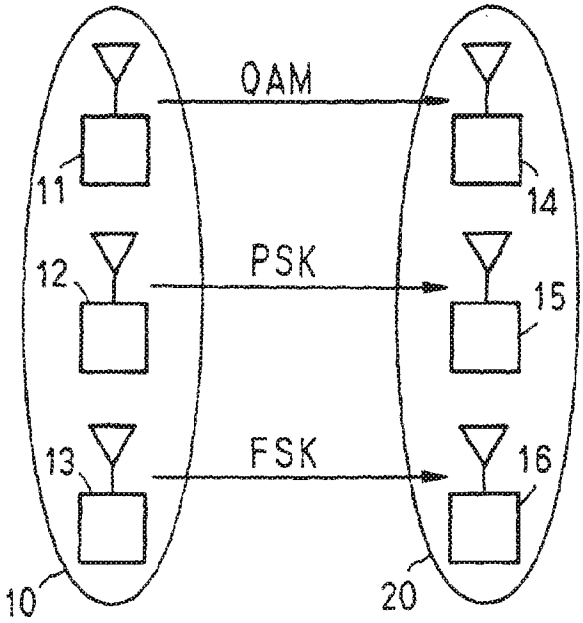


FIG. 1B PRIOR ART

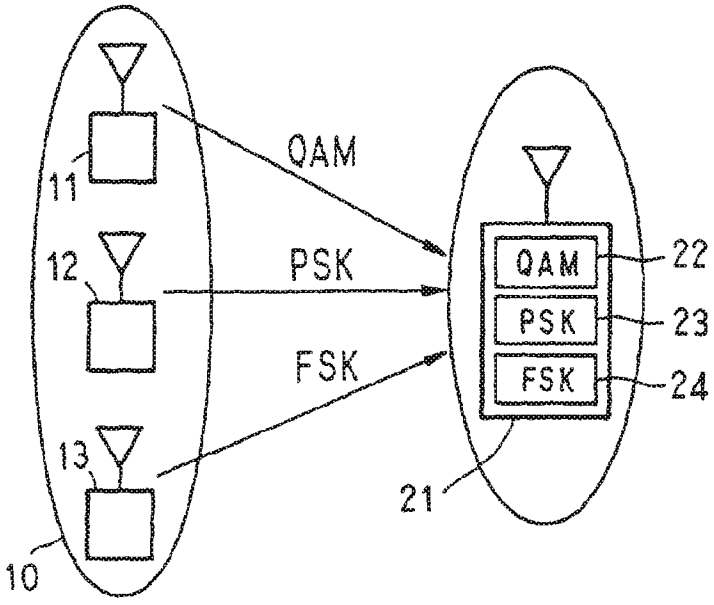


FIG. 2A PRIOR ART

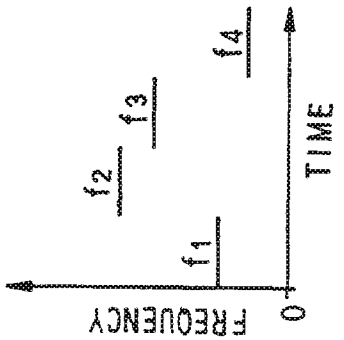


FIG. 2B PRIOR ART

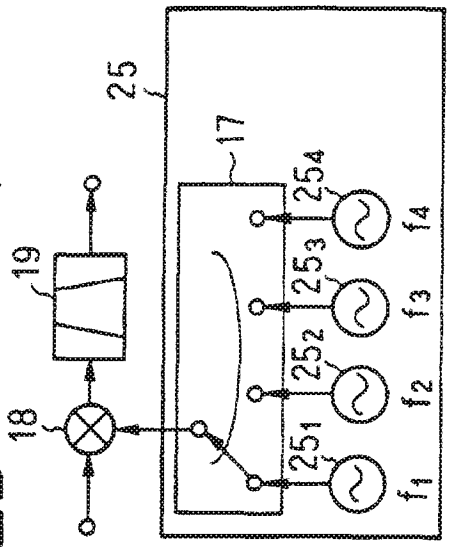


FIG. 2C PRIOR ART

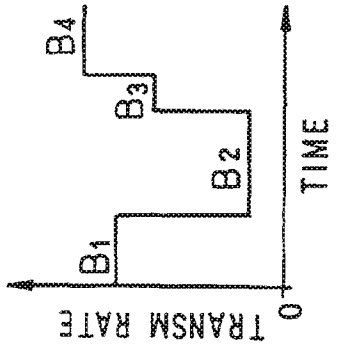
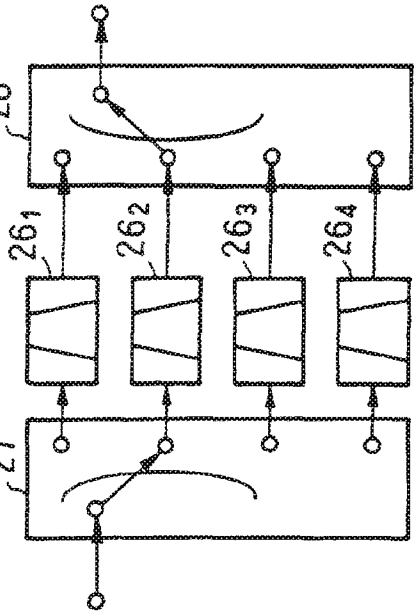


FIG. 2D PRIOR ART



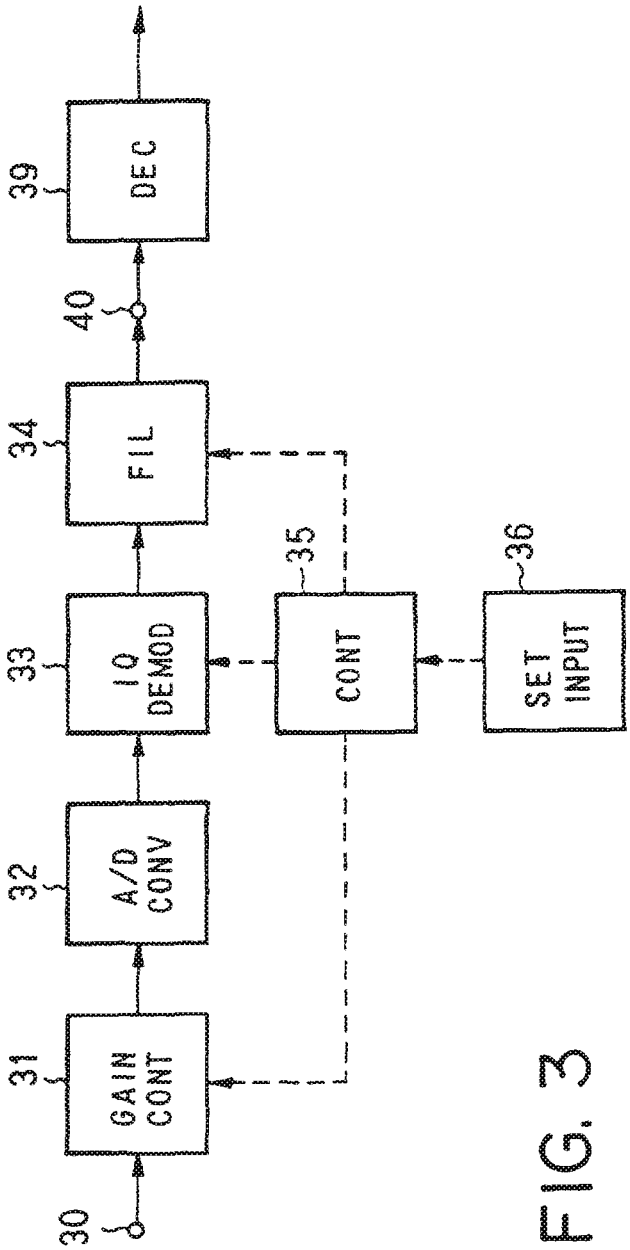

30
GAIN CONT
31
A/D CONV
32
IQ DEMOD
33
FIL
34
40
DEC
39
CONT
35
SET INPUT
36

FIG. 3

FIG.4A

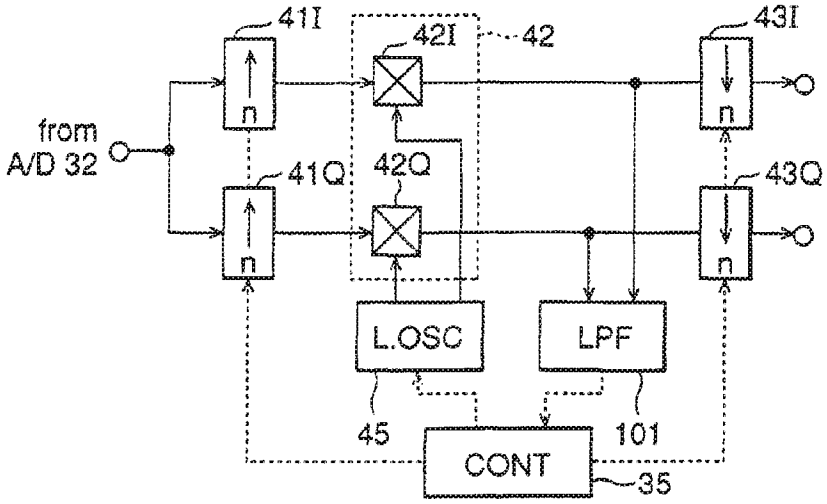
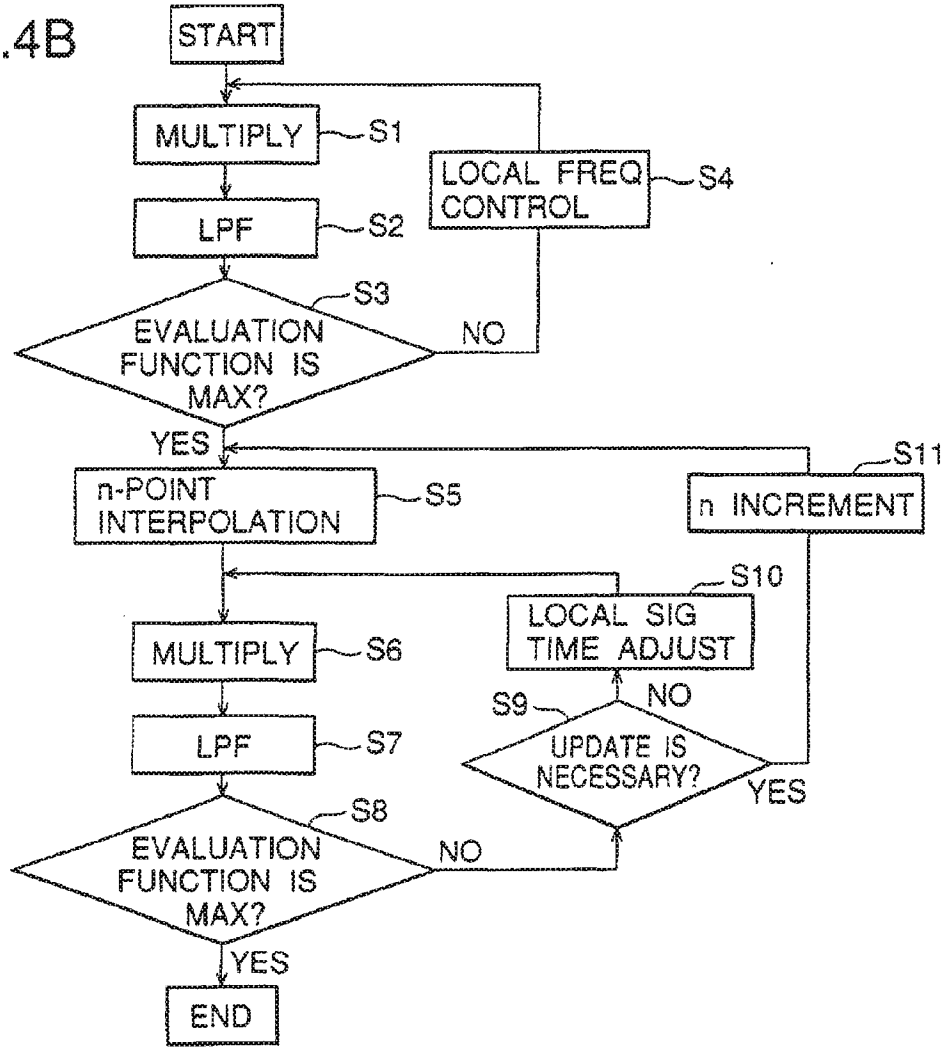


FIG.4B



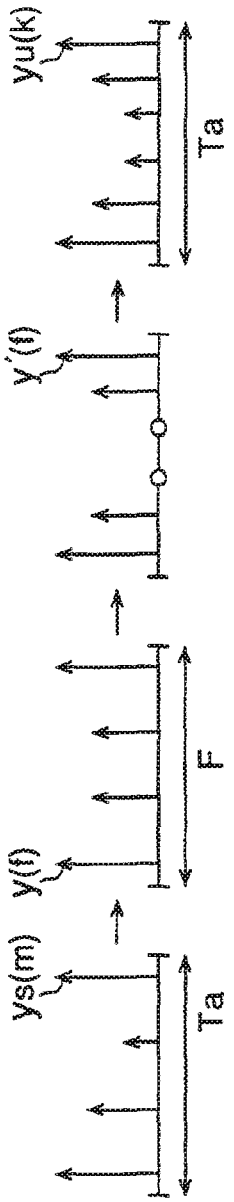


FIG.5A

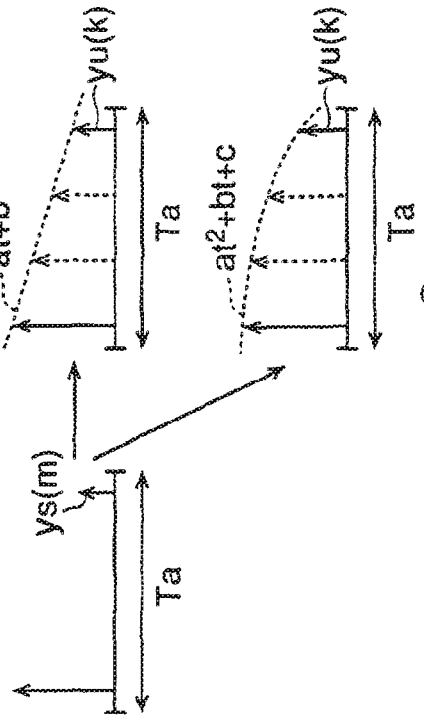


FIG.5B

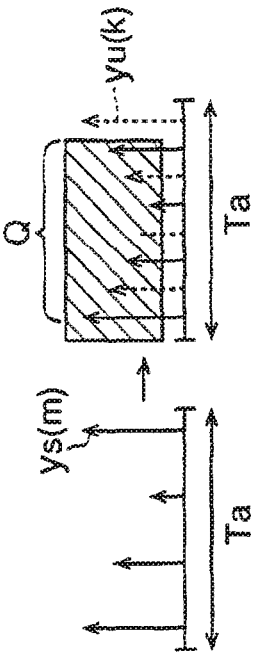


FIG.5C

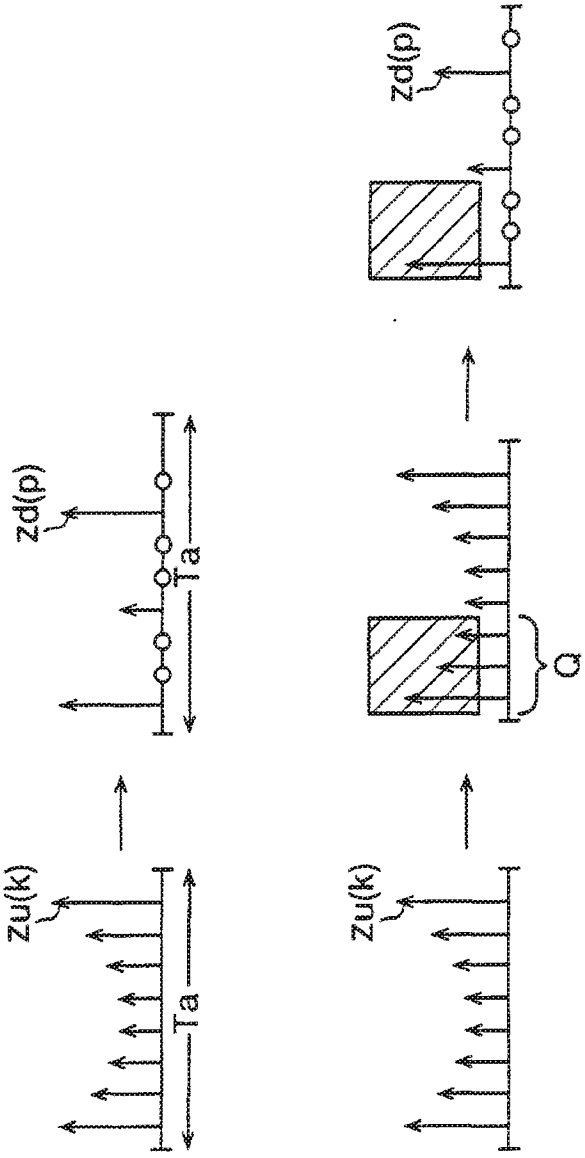


FIG.6A

FIG.6B

FIG.7

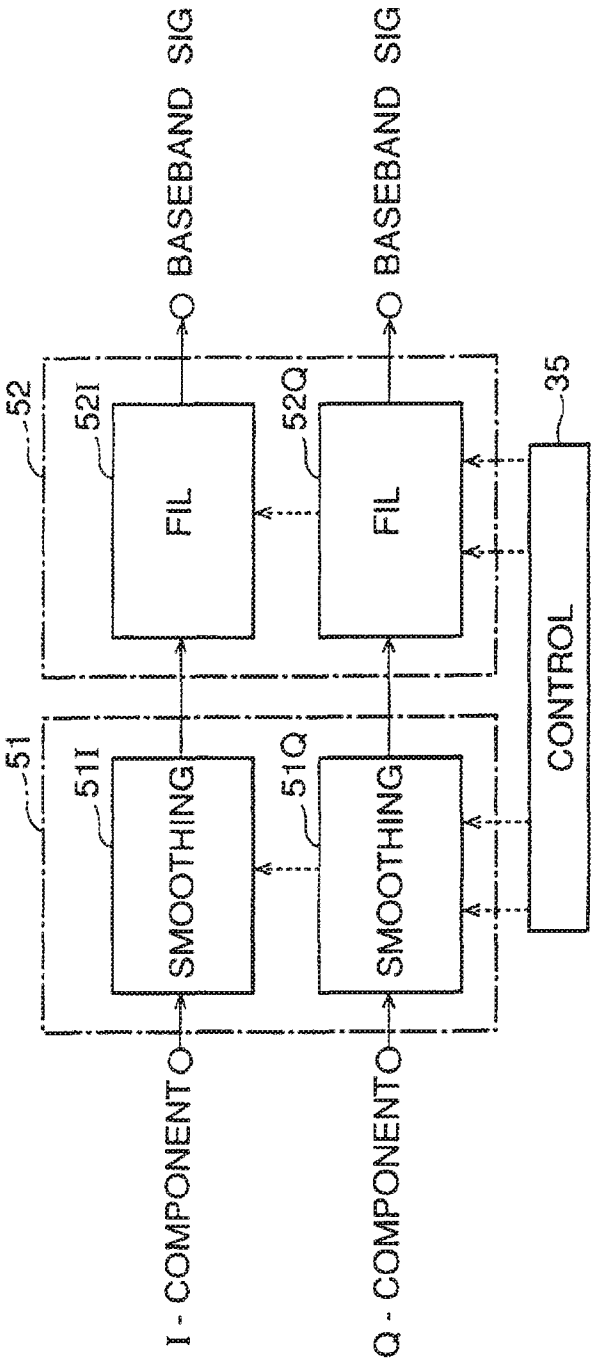


FIG.8A

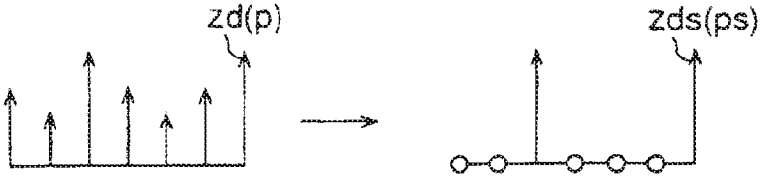


FIG.8B

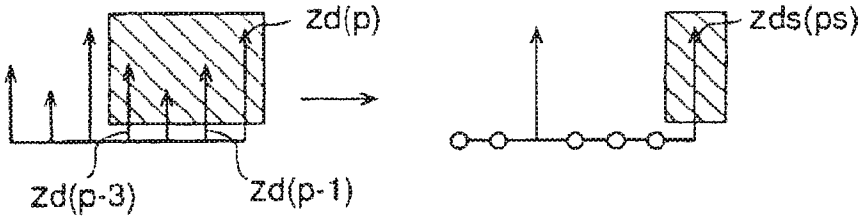
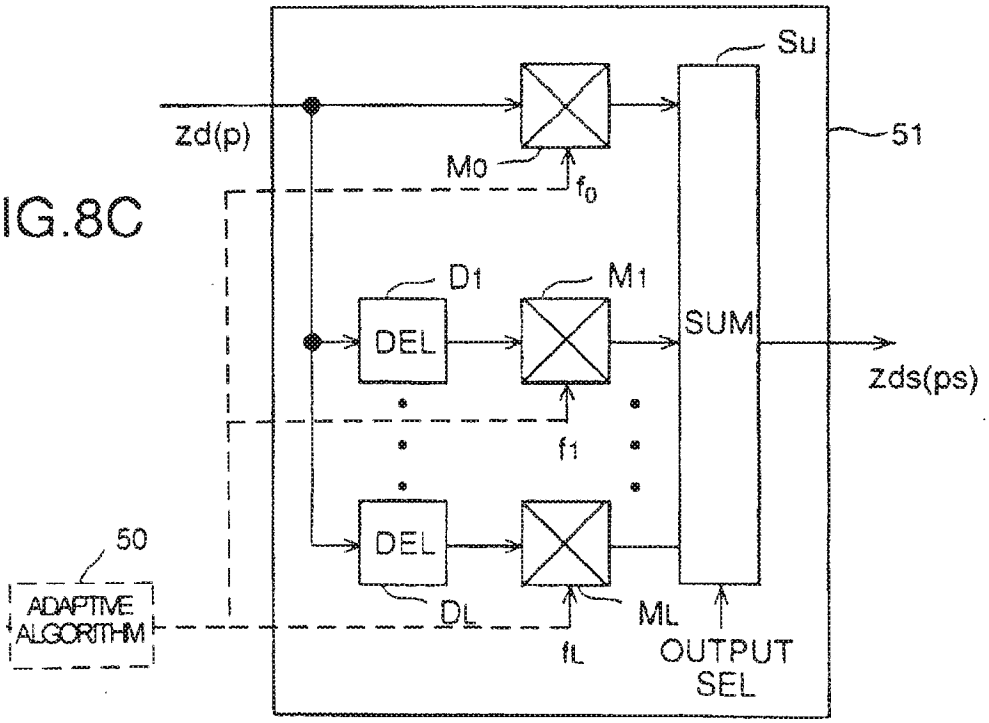


FIG.8C



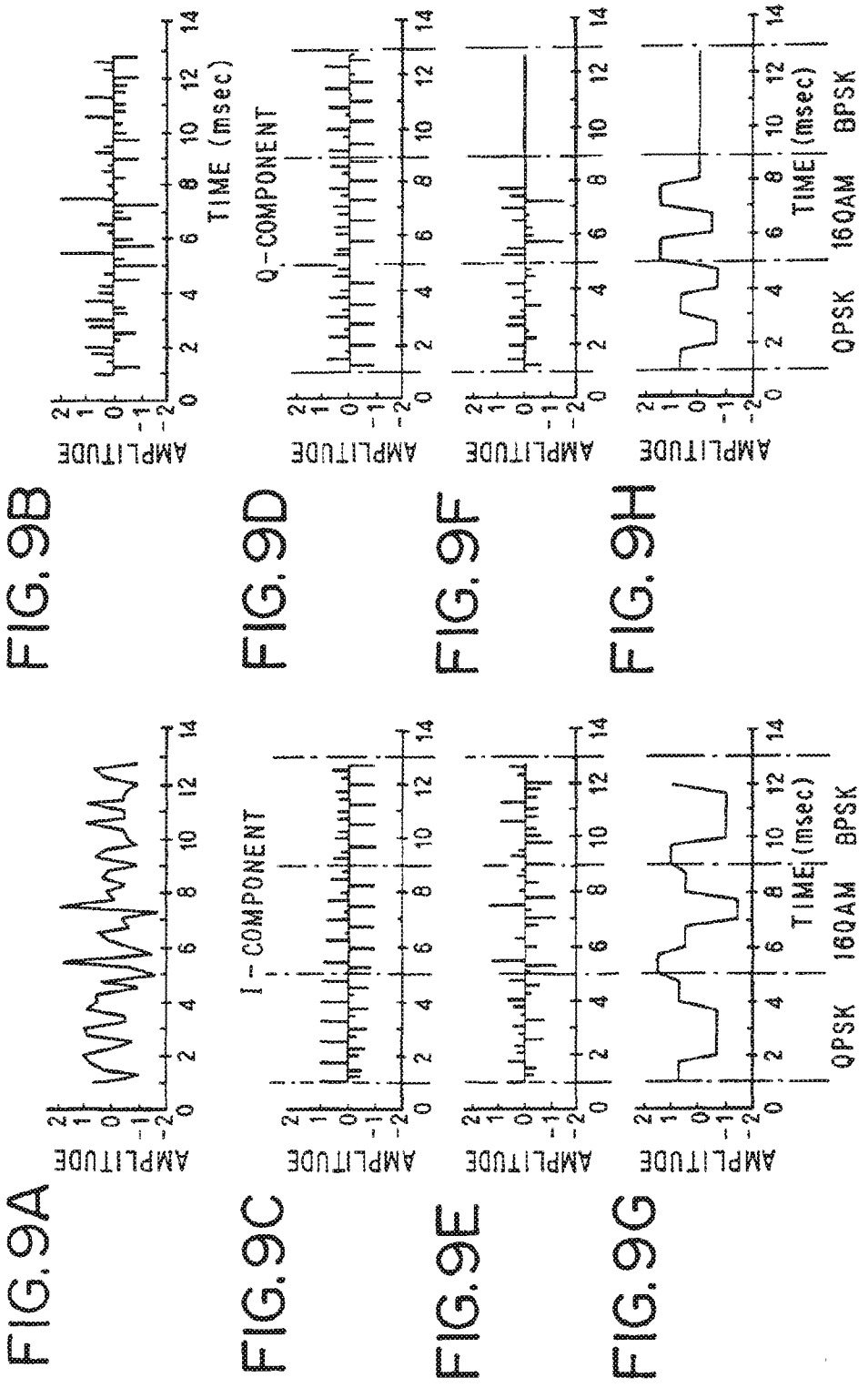


FIG.9A FIG.9B FIG.9C FIG.9D FIG.9E FIG.9F FIG.9G FIG.9H

FIG. 10A

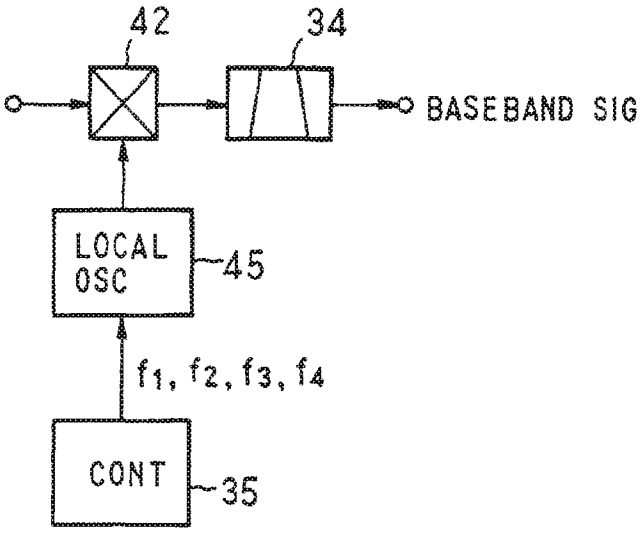


FIG. 10B

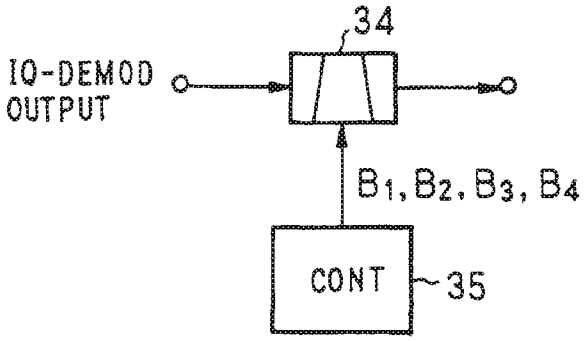


FIG.11

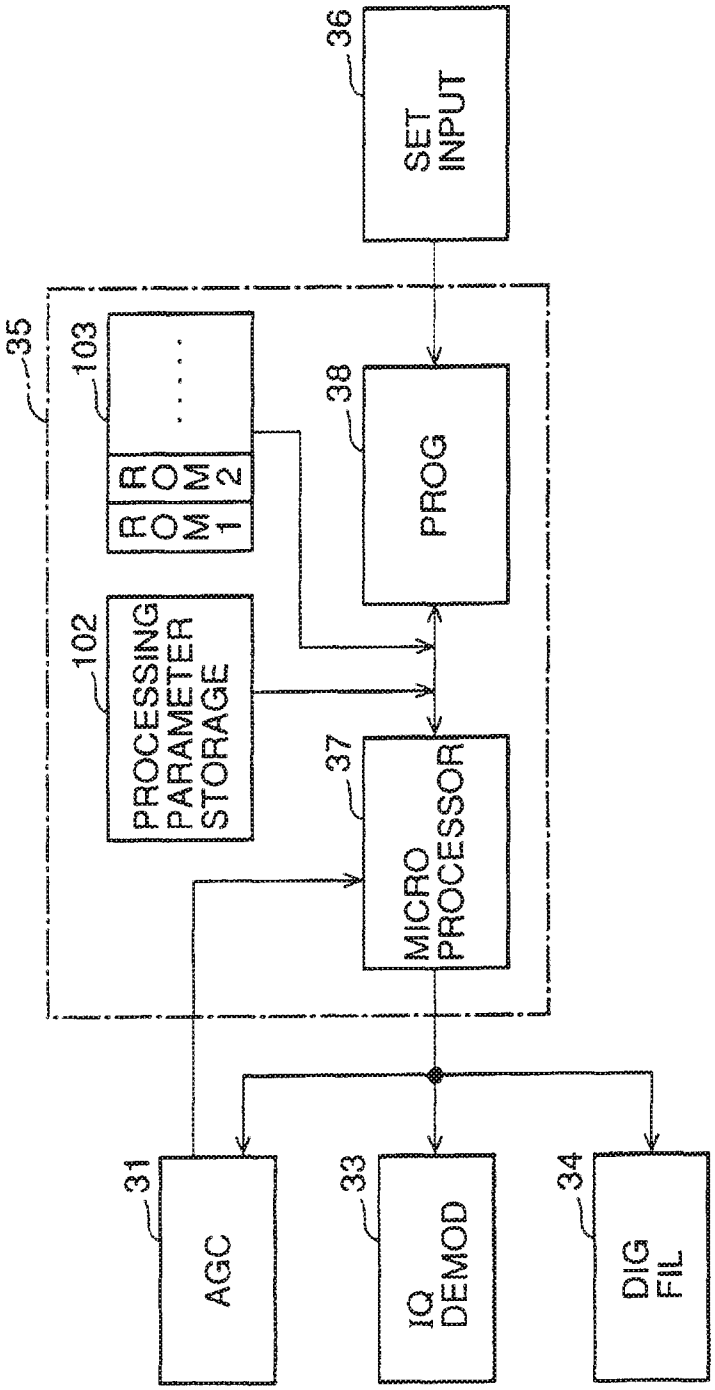


FIG.12

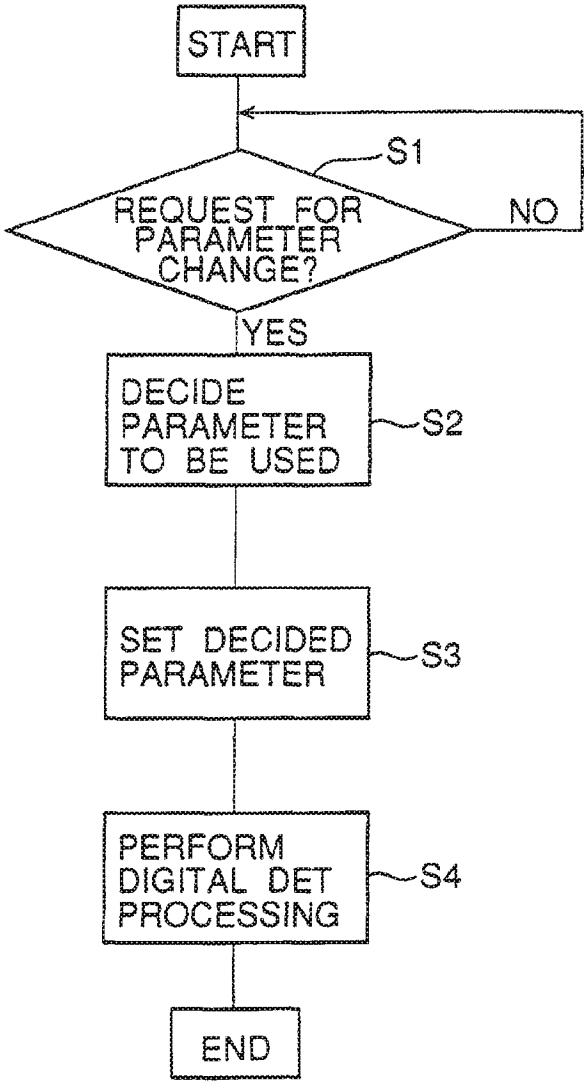


FIG.13

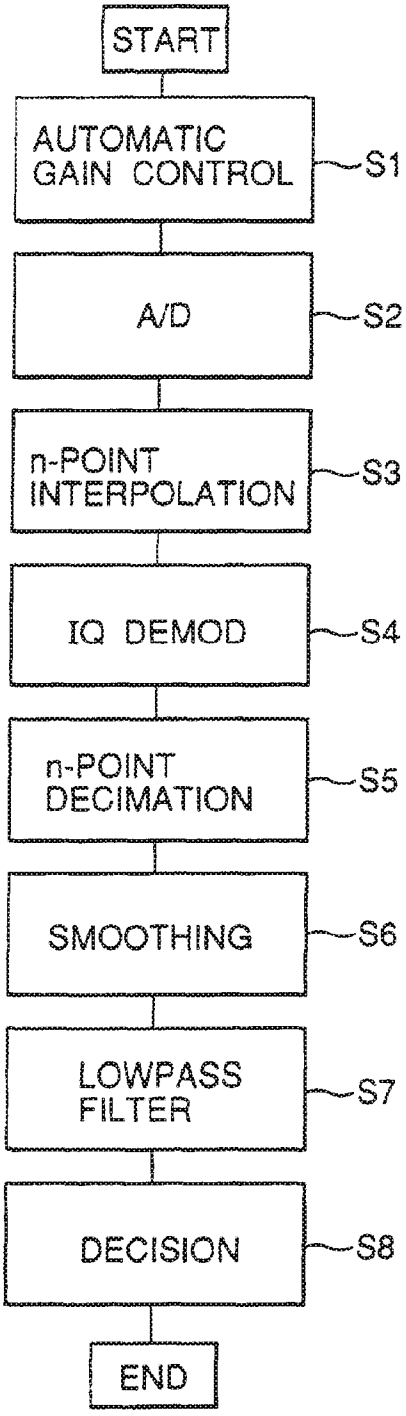


FIG.14

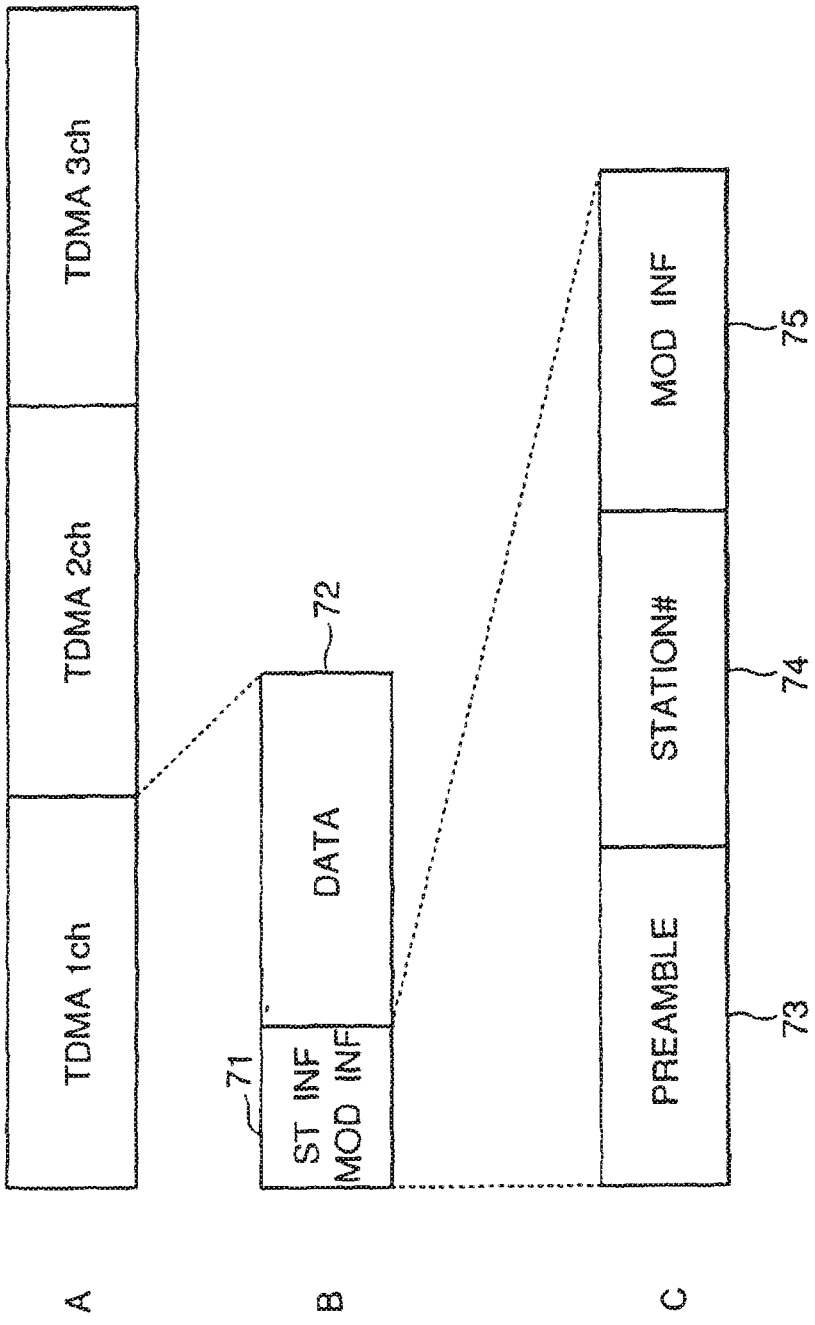
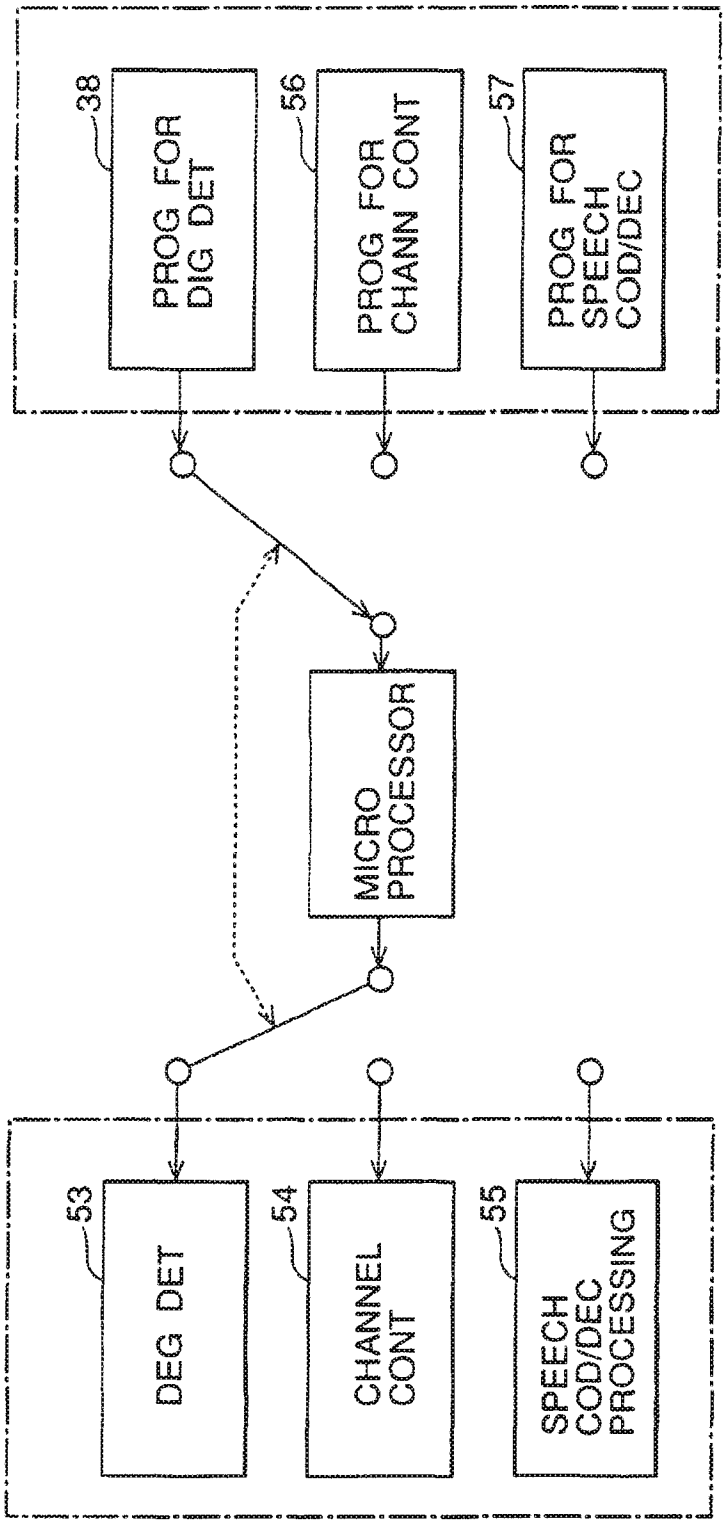


FIG.15



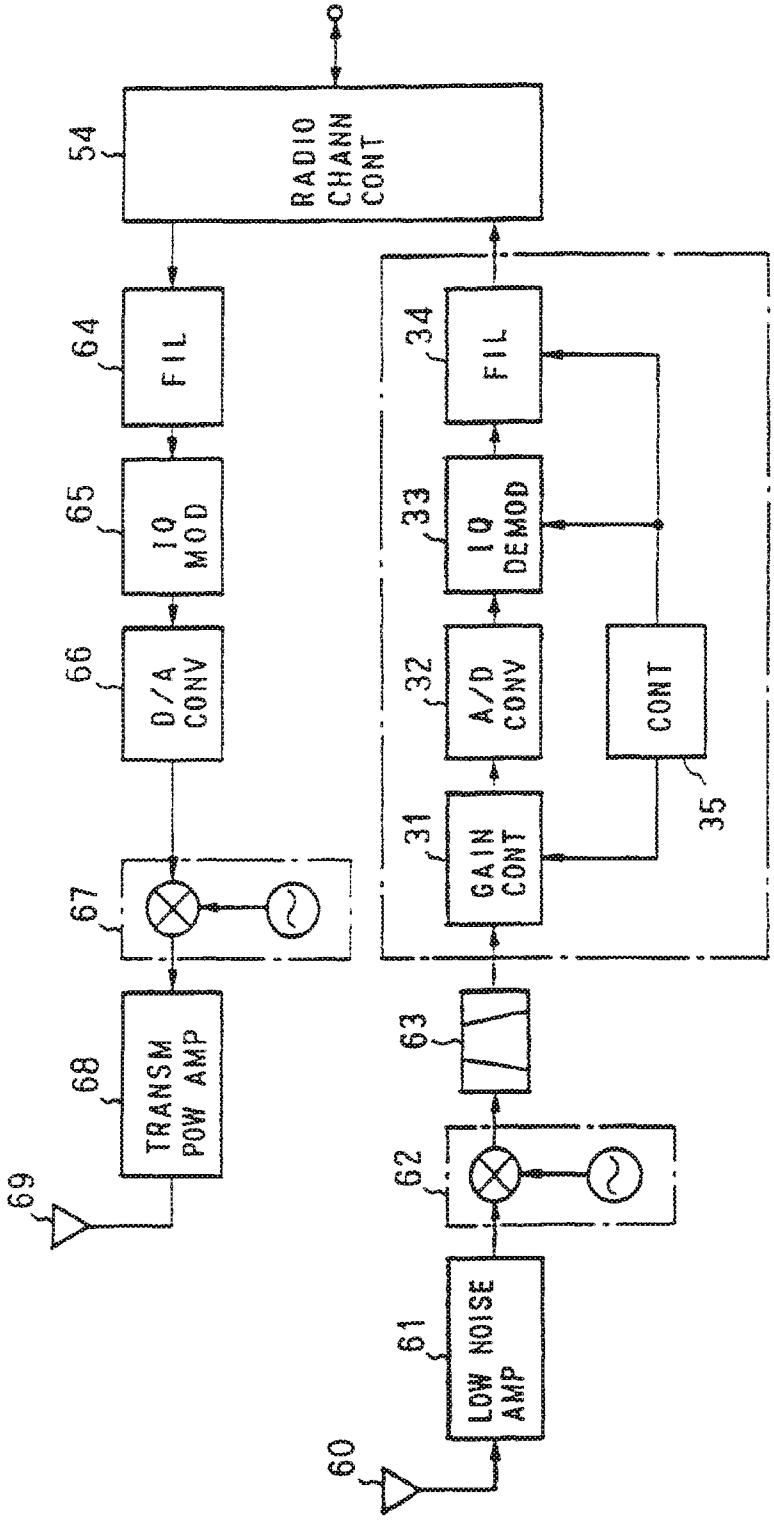


FIG. 16

FIG.17A

	MAX AMPLITUDE	n	SMOOTHING	ROLL-OFF RATIO	FIL COEFF
AUDIO	AM1	n1	ROM1	RO1	h1,h2,··· ,hn
IMAGE	AM2	n2	ROM2	RO2	h1,h2,··· ,hm

FIG.17B

MOD TYPE	MAX AMPLITUDE	n	SMOOTHING
QPSK	AM1	n1	ROM1
16QAM	AM2	n2	ROM2

FIG.17C

CODE RATE	ROLL-OFF RATIO	FIL COEFF
B1	RO1	h1,h2,··· ,hn
B2	RO2	h1,h2,··· ,hm

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 845 916 B1

(12) EUROPEAN PATENT SPECIFICATION

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02.03.2005 Bulletin 2005/09

(51) Int Cl.7: **H04Q 7/38**

(21) Application number: **97850165.8**

(22) Date of filing: **02.12.1997**

(54) **Point to multipoint radio access system**

Punkt zu multipunkt Funksystem

Système radio point à multipoint

(84) Designated Contracting States:
DE FR GB SE

(30) Priority: **02.12.1996 US 31536 P**
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(43) Date of publication of application:
03.06.1998 Bulletin 1998/23

(73) Proprietor: **Telefonaktiebolaget LM Ericsson (publ)**
164 83 Stockholm (SE)

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171 42 Solna (SE)

(74) Representative: **Sjöberg, Mats Hakan et al**
Ericsson AB,
Patent Unit Radio Networks
164 80 Stockholm (SE)

(56) References cited:
WO-A-95/25409

- **SAMPEI S ET AL: "ADAPTIVE MODULATION/TDMA SCHEME FOR PERSONAL MULTI-MEDIA COMMUNICATION SYSTEMS" PROCEEDINGS OF THE GLOBAL TELECOMMUNICATIONS CONFERENCE (GLOBECOM), SAN FRANCISCO, NOV. 28 - DEC. 2, 1994, vol. VOL. 2, 28 November 1994, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 989-993, XP000488685**
- **VADGAMA S K: "ADAPTIVE BIT RATE TRANSMISSION FOR PERSONAL COMMUNICATIONS" PROCEEDINGS OF THE NORDIC SEMINAR ON DIGITAL LAND MOBILE RADIO COMMUNICATIONS (DMR), OSLO, JUNE 26 - 28, 1990, no. SEMINAR 4, 26 June 1990, GENERAL DIRECTORATE OF POSTS AND TELECOMMUNICATIONS;FINLAND, pages 1-9, XP000515571**

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Description

BACKGROUND

1. Field of Invention

[0001] This invention pertains to a point to multipoint radio access system. The invention particularly pertains to the configuration of such system which utilizes a number of different modulation methods, the modulation methods being distinguishable with regard to the bandwidth efficiency but also with regard to the coverage range and the interference immunity.

2. Related Art and Other Considerations

[0002] Radio access methods have become frequently used to enable the rapid and economic implementation of the access network in modern telecommunication networks. Most known solutions up to date are based on conventional mobile cellular techniques, where the subscribers are fixed instead of mobile. One disadvantage of using cellular techniques for the access network is that the radio spectrum is limited and the implication of this is that these systems normally have a too limited capacity, especially in cities.

[0003] Recently a new point to multi point system has been suggested that uses microwave links between a central base station and subscriber terminals. The central base station uses normally 45 or 90 degree sector antennas and the terminals directive antennas pointing towards the base station.

[0004] In the suggested system, frequency reuse can be very effective by the use of alternating vertical and horizontal polarizations for the links in adjacent sectors.

[0005] Also, the line of sight radio links lends themselves to high quality connections, the capacity of which can be adapted individually to different capacities (bitrates).

[0006] To further improve on the frequency economy of this system, it has been suggested to use a number of different modulation types for the links. The highest order of modulation requires minimum bandwidth for a given bitrate but has also the minimum range and is most sensitive for interferences from other links. The lowest order of modulation is the most robust. It has the longest coverage range and is also the least sensitive to interferences from other links.

[0007] The problem in this kind of system is then to select for each link the most suitable modulation, considering bandwidth economy, coverage range and the foreseen interference situation.

[0008] A system of this kind is described in a paper entitled Link Capacity and Cellular Planning Aspects of a Point to Point Fixed Radio Access System, by A Bollmann, D. Chicon, and M Glauner, European conference on Radio Relay Systems 1996, Bologna, Italy. However heretofore there has not been a clear cut procedure for arriving to a suitable strategy to allocate suitable modulation types and bandwidth to each terminal in the system.

[0009] In an article by Sunil K. Vadgama titled "Adaptive Bit Rate Transmission for Personal Communications", Proc. of the Nordic seminar on digital land mobile radio communications (DMR), Oslo, June 26 - 28, 1990, the idea of trading off transmission bit rate for either lower transmission power or extra communication range is discussed. It is noted that in multilevel modulation the bit rate is varied by changing the order of modulation, i.e. the number of bits per modulation symbol, whereby the nominal bandwidth remains constant, making frequency planning simpler. Three system implementations are suggested for a personal communication system: a) using a fixed modulation in a given type of cell, b) creating a number of concentric zones using respective modulation orders, and c) varying the modulation order dynamically across each cell. However, it is noted that the latter implementation would require rather complex signaling, call setup protocols and frame formats. This document forms the preamble of claim 1.

[0010] What is needed, therefore, is a system, which enables a proper choice of a modulation type considering bandwidth efficiency, coverage range and the interference situation.

SUMMARY

[0011] A method is provided for allocating radio link characteristics in a point to multipoint radio access system. The point to multipoint radio access system comprising a number of base stations including a selected base station connected by a plurality of radio links to a corresponding plurality of subscriber terminals located within respective coverage areas of the selected base station. At least some of the plurality of radio links are within a same frequency band.

[0012] In accordance with the method, a base station power density is selected for the selected base station. The base station power density, for each of a plurality of modulation types, is constant for all bitrates. Similarly, for each of the plurality of subscriber terminals located within the coverage area of the selected base station, a terminal power density is selected. The terminal power density, for each of the plurality of modulation types, is constant for all bitrates. A maximum range is then determined for each of the plurality of modulation types. Then, for each of the plurality of

subscriber terminals, a modulation type is allocated to the corresponding radio link dependent upon range from the selected base station. A determination is then made, for each of the plurality of subscriber terminals, whether at the subscriber terminal there is an acceptable signal quality. If not, a next lower modulation type is allocated to the radio link corresponding to the subscriber terminal which does not have the acceptable signal quality.

[0013] After the foregoing has occurred with respect to the subscriber terminals, a determination is made at the selected base station whether there is an acceptable signal quality with respect to each of the plurality of subscriber terminals. If not, the radio link corresponding to the subscriber terminal having unacceptable signal quality is allocated a next lower modulation type. Thereafter, frequencies and bandwidth are allocated to each of the plurality of radio links.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The foregoing and other objects, features, and advantages of the invention will be apparent from the following more particular description of preferred embodiments as illustrated in the accompanying drawings in which reference characters refer to the same parts throughout the various views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

Fig. 1 is schematic view of a microwave coverage network according to an embodiment of the invention.

Fig. 1A is an enlarged schematic view of a portion of a coverage area served by a base station site of the network of Fig. 1.

Fig. 2 is a schematic view of a base station according to an embodiment of the invention.

Fig. 3 is a schematic view of a base station network according to an embodiment of the invention.

Fig. 4 is a schematic view depicting the relationship of Fig. 4A and Fig. 4B.

Fig. 4A and Fig. 4B are flowcharts showing steps executed by a network planning processor according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[0015] In the following description, for purposes of explanation and not limitation, specific details are set forth such as particular architectures, interfaces, techniques, etc. in order to provide a thorough understanding of the present invention. However, it will be apparent to those skilled in the art that the present invention may be practiced in other embodiments that depart from these specific details. In other instances, detailed descriptions of well known devices, circuits, and methods are omitted so as not to obscure the description of the present invention with unnecessary detail.

[0016] Fig. 1 shows a microwave coverage network 20. Network 20 includes a regular pattern of base station sites and the corresponding cell or coverage area for each base station site. In Fig. 1, the cell or coverage area for each base station site is shown as a square, with a base station site being located at the center of the square (i.e., the center of the cell). For example, base station site B1 is centrally located in its cell C1 and base station site B2 is centrally located in its cell C2.

[0017] In the illustrated embodiment, each cell C comprises four triangular sectors. For example, cell C1 comprises sectors $S1_{C1}$, $S2_{C1}$, $S3_{c1}$, and $S4_{C1}$ and cell C2 comprises sectors $S1_{C2}$, $S2_{C2}$, $S3_{C2}$, and $S4_{C2}$.

[0018] Fig. 1A shows an enlargement of the center of cell C1 served by base station site B1. As seen in Fig. 1A, each base station site, such as base station site B1, includes four base stations (base stations B1-1, B1-2, B1-3, and B1-4 being shown as included in base station site B1 in Fig. 1A).

[0019] As shown both in Fig. 1 and Fig. 1A, alternating sectors S of a cell C have differing polarizations. That is, directly adjacent sectors receive transmissions in orthogonal polarizations to obtain decoupling in the overlap regions of the antenna patterns. For example, in cell C1 sectors $S1_{C1}$ and $S3_{C1}$ have horizontal polarization (as indicated by the letter "H") while sectors $S2_{C1}$ and $S4_{C1}$ have vertical polarization (as indicated by the letter "V").

[0020] In Fig. 1, two terminals T1 and T2 are shown. Terminal T1 is located in sector $S4_{C1}$ which is served by base station B1-4; T2 is located in sector $S4_{C2}$ which is served by base station B2-4. Terminals T1 and T2 are thus served by base stations which use the same polarizations.

[0021] In the particular configuration shown in Fig. 1, base stations B1, B2 have approximately 90 degree wide antennas. Terminals T1 and T2, on the other hand, have much smaller antenna beamwidths, typically 4-8 degrees. Although only two terminals T1 and T2 are illustrated in Fig. 1, it should be understood that many terminals typically reside in each sector S. Terminals are located at premises of customers, with each terminal being connected by lines

(e.g., POTS or ISDN lines) to many telephone subscribers. Each terminal is dedicated and adjusted to one base station (e.g., terminal T1 is dedicated to base station B1-4).

[0022] Although there are several terminals within each sector, for a given sector each terminal T is allocated its individual frequency from a range of frequencies available in that sector. It can occur that the same frequency is being utilized both in sector $S4_{C1}$ and $S4_{C2}$. Thus, if terminals T1 and T2 were assigned the same frequency, a potential interference problem would arise. In this regard, a signal transmitted on a frequency f1 to terminal T1 from base station B1-4 at site B1 would, due to the wide antenna angle of base station B1-4, also hit the terminal T2 as indicated by line 30. If terminal T2 is also using frequency f1, interference would result. Thus, base station B1-4 could cause interference at terminal T2.

[0023] Likewise, terminal T2 could cause interference in base station B1-4. In this regard, terminal T2 has a narrow antenna beam which is directed towards its own base station B2-4. Normally the signal directed from terminal T2 to base station B2-4 would not hit the base station B1. However, if terminal T2 is more or less in line with both base station B2-4 as well as with base station B1-4 in the manner shown in Fig. 1, interference may arise. In this situation, the antenna of terminal T2 cannot discriminate between base station B2-4 and base station B1-4, and interference results.

[0024] It should be understood the use of four sectors S per cell as illustrated in Fig. 1 is merely to serve as an example. Whereas Fig. 1 illustrates each cell C sector at ninety degrees in view of the particular antennae employed, the cells can be sectored at other angles (e.g., forty five degree or fifteen degree angles) in accordance with the angles of the antennae chosen for the base stations.

[0025] The person skilled in the art will appreciate that the wide angle sectored base station antennae have a lower gain than the highly directive terminal antennae (which have a smaller beam). For example, an antenna at a terminal T may have an eight degree main beam with high antenna gain (e.g., 22 dB at 10 Ghz).

[0026] Fig. 2 shows a block diagram of a base station 40 (base station 40 being representative, for example, of base stations B1-4 and B2-4 discussed above). Base station 40 includes in its transmitter part a plurality of transmission channels 41, one such channel 41A being fully shown in Fig. 2. Each channel 41 has a modulator 42 and an upconverter 44 to convert the signals to RF-frequency. All transmission channels 41 are connected to power amplifier 46 as indicated by lines 47. Base station 40 also has a receiver part or receiver side having receiver channels 51, only channel 51A being fully illustrated in Fig. 2. All receiver channels 51 share a common RF-amplifier 52. Amplifier 52 is connected by lines 53 to each receiver channel 51. Each receiver channel 51 includes a down converter 54 and a demodulator 56. Duplexer 60 of base station 40 combines the transmitter and the receiver to a common antenna 62. The modulator 42 and demodulator 56 of each channel (commonly known as a modem) are controlled by a control unit 70. Control unit 70 connects to all transmission and receive channels. Control unit 70 sets the basic link parameters for the modem, i. e. modulation type, transmit power density, and bitrate. In a DBA (Dynamic Bandwidth Allocation) mode, control unit 70 also makes bandwidth allocations to the individual terminals on a momentary basis.

[0027] Fig. 3 shows an overview of a base station network 100. A number of base stations 40_0, 40_1, 40_2, etc. are connected to a Network Management System (NMS) 102. In particular, control units 70 of the plurality of base stations 40 are connected to Network Management System (NMS) 102.

[0028] Network Management System (NMS) 102 is, in turn, connected to a network planning processor (NPP) 110. Network planning processor (NPP) 110 can take various forms, such as a stand alone personal computer (PC). Operations and calculations performed by NPP 110 are described in more detail below. Results and outputs from Network planning processor 110 are transmitted to Network management system 102. The output operations from Network planning processor 110 to Network management system 102 can take the form of a simple file transfer. Inputs to Network management system 102 include the allowed modulation types for each terminal T. Thus, when control unit 70 of a base station 40 allocates a channel to a particular terminal T, control unit 70 knows beforehand which modulation types are allowed due to the interference situation.

[0029] The inputs to Network planning processor 110 include the locations of the base stations B and the terminals T; the particular antenna patterns employed; basic link parameters such as power densities available; and modulation sensitivities such as C/N and C/I requirements. In addition, in an FBA (Fixed Bandwidth Allocation) mode, the inputs include the capacities (bitrates) needed per terminal.

[0030] As the notion of modes has been broached above, it should be mentioned that the invention can operate in either of two modes of operation. In the FBA (Fixed Bandwidth Allocation) mode, each specific terminal is allocated a specific capacity (bitrate), modulation type, bandwidth and frequency once and for all. In the Dynamic Bandwidth Allocation (DBA) mode, each terminal is allocated a capacity, modulation type and bandwidth by controller 70 according to the actual need at every moment. In the DBA mode any terminal can change allocated frequency with time as the system tries to move the users to make optimum usage of the total bandwidth.

[0031] Mention is also often made herein to "modulation types". Five different examples of modulation types and corresponding characteristics are shown in Table I.

TABLE I

Example Modulation Types and Corresponding Characteristics				
Modulation Type	C/N	C/I	Efficiency	Relative range
QPSK ½	6.5	9.5	0.85	1
QPSK 3/4	9	12	1.30	0.75
QPSK 7/8	11	14	1.50	0.60
8 TCM 2/3	11.5	14.5	1.70	0.55
16 TCM 3/4	18	21	2.50	0.26

In Table I, the C/I ratio are the values for 3 dB degradation of the noise threshold. This difference is necessary in C/N and C/I is 11.5 dB for the two extremes. The bandwidth requirements are differing by a factor of 3 and the range by a factor of almost 4 between the most robust and the most bandwidth efficient modulation.

[0032] Fig. 4A and Fig. 4B show selected general operations or steps performed by Network planning processor 110 in accordance with the present invention. Prior to performance of the steps shown in Fig. 4A and Fig. 4B, it is assumed four preliminary steps have occurred.

[0033] As a first preliminary, the sites and the needed capacities in number of 64 kb/s lines per site are defined. As a second preliminary, the base station sites B are found by overall considerations of capacity and coverage. For selection of appropriate sites, use is made of line of sight (LOS) coverage diagrams in Network planning processor 110. The base station sites are sectorized and the different sectors are allocated different polarizations. As a third preliminary, terminal sites are allocated to the different base stations. As a fourth preliminary, rain zone and the requirements on unavailable time (UAT) and link quality are defined. Typical other link quality requirements are defined in ITU-T:s Rec G 821. For radio link calculations different rain zones are used, as also defined by ITU.

[0034] Assuming that the foregoing preliminaries have been performed, Network planning processor 110 executes the general steps shown in Fig. 4A and Fig. 4B. Execution begins with selection of a power strategy, as depicted by steps 400 and 402.

[0035] At step 400 a base station's transmit power density (i.e. power transmitted per Hz bandwidth) is selected to be constant for all bitrates and modulation types. This implies that all bitrates transmitted with one specific modulation type have the same range. However a more bandwidth effective modulation type will have a shorter range since it will be less robust [require a higher signal to noise ratio C/N or signal to noise and interference ratio C/(N+I)].

[0036] At step 402 the transmit power density of a terminal is selected to be constant for all bitrates and for all modulation types measured at the range limit of the respective moculation type. With decreasing distance from the terminal to its base station, the power density is decreased so that the power density received at the base is constant for all distances. The power density transmitted from the terminals and also received at the base will differ for the various modulation types with the difference in the C/(N+I) required for the respective modulation types.

[0037] In considering the power selection steps 400 and 402, a typical power density for a base station could be e. g., -60 dBm/Hz bandwidth for all modulation types. For a terminal, power density will vary depending on its distance to the base station, e.g., for a QPSK ½ modulated link the power density could be -70 dBm/Hz at the range limit and would then decrease with distance to result in a constant received power density at the base (the power density would typically decrease with 6 dB for half the distance). For a 16 TCM 3/4 link, the power density would be 11.5 dB higher corresponding to the difference in C/I requirements for a 16 TCM terminal at the same range as a terminal using QPSK $^1/_2$ This implies that the power density received at the base station would be 11.5 dB higher for the 16 TCM terminal.

[0038] At step 404, a maximum range is calculated for each of the various modulation types. At this calculation a 3 dB degradation of the noise threshold is allowed for interference from other links (this means in the C/(N+1) ratio that I=N). The coverage calculations of step 404 are straight forward calculations in microwave link technology which are understood by the person skilled in the art, and accordingly are not described here in further detail. Typical coverage ranges vary with frequency band. In 10.5 GHz, which is a typical band allocated by ITU for point to multipoint services, distances are around 10 km for modulation type QPSK ½ and shorter for the more sensitive modulation types, e.g., 2-3 km for 16 TCM 3/4. In higher frequency bands, e.g. 18 and 26 GHz, ranges are shorter due to the attenuation effect of rain (which is higher with higher frequency). A special case could be that the cell radius is selected so small that all modulation types have enough range.

[0039] At step 406 the minimum bandwidth modulation type is allocated to each terminal in dependence on its range from the base station. Thus, depending on the range of the terminal sites, the different links are allocated a modulation scheme which complies with the maximum range for that modulation and which uses minimum bandwidth.

[0040] At step 408, for each terminal a calculation is performed of the C/I ratio, where C represents the desired signal

from the own base station sector and I the interference from each other base station sector. The interference from all other (sector) base stations is calculated taking the polarizations, antenna patterns (these have diagrams for both copolar and cross polarizations) and assigned power density into account. These interferences are added together to obtain the "I" of the C/I ratio.

[0041] At step 410, for each terminal the calculated C/I is checked to determine if it is greater than the minimum required C/I. Here the C/I values that represent a 3 dB degradation of the noise threshold should be used to comply with the coverage calculation of step 404. If the required C/I is not satisfied when checked at step 410, for any terminal failing the check the next lower (more robust modulation type) is selected for that terminal (step 412). If a further check (step 414) whether the C/I ratio is greater than the minimum, it is determined that no modulation type will satisfy the condition and the terminal is designated at step 416 as a problem terminal to be handled separated (e.g., such a problem terminal could be denied service or allocated a separate frequency from the total available bandwidth).

[0042] As an example of the foregoing, suppose that at step 410 the C/I is calculated to be 13. Such C/I ratio is permissible if the selected modulation type is QPSK ½, which requires 9.5 dB. On the other hand, if the selected modulation type were 16 TCM 3/4, which requires 21 dB, the nearest most robust modulation type compatible with C/I – 13 dB would be QPSK 3/4. Thus QPSK 3/4 would be selected instead of 16 TCM 3/4. In connection with step 412, it should be noted that a change from one modulation type to another will not affect the C/I calculations just performed as all modulation types are transmitted with the same power density.

[0043] At step 418 (see Fig. 4B) the C/I ratios at the base stations are calculated (i.e., C/I calculations are made from each terminal to its base). For each terminal, the desired signal C is compared to the received interference signals I from other terminals. Note here that within each sector only one terminal will work on a specific frequency. Thus one link at the base station will only be interfered by a maximum of one terminal in each sector. With normal cell plans it is not likely that more than two terminals will contribute significantly to the interference. Thus it will be sufficient as a worst case to add a 3 dB margin to the interference level from the worst terminal.

[0044] At step 420 a check is made at the base station whether the received interference power density is below this maximum for each terminal. If not, at step 422 the terminal is allocated the next more robust modulation type, which will mean that the terminal will decrease its transmit power density. After a further check for such terminal at step 424, any terminal that can not be made to satisfy the condition on maximum interference power is marked as a problem terminal (step 426) and is treated separately as described above.

[0045] The present invention does not lead to a large number of calculations. By observing that (1) the received desired signal C from each terminal is constant for a specific modulation type (see step 402), and (2) that the difference in received signal level for the various modulation types correspond to the difference in required ratio C/I, it can be derived that the maximum allowed interference level is constant for all modulation types.

[0046] In connection with even numbered steps 418 through 426, it is to be noted that the wanted signal at a base station is always received with the same level for each specific modulation type. For a 16 TCM 3/4 modulated link, however, the received level is 11.5 dB higher than for a QPSK ½ modulated link. As the allowed carrier to interference ratio C/I for the 16 TCM 3/4 link is 11.5 dB higher than for the QPSK link, it can be concluded that the maximum allowed interference level is the same for all modulation types. Thus, in order to check the C/I for the uplink from the terminals to the base stations, it is sufficient to calculate the received interference signal at the base station. For example, if the nominal wanted signal C at the base is -140 dBm/Hz for a QPSK ½ link, the maximum interference signal level would be -140-9.5 = - 149.5 dBm/Hz for all modulation types. Thus, if the calculated interference signal level from terminal T2 were -145 dBm/Hz, it would have to be reduced. If the modulation type for terminal T2 were e.g., 16 TCM 3/4, the interference level could be reduced by selecting a more robust modulation type, which would have a lower power density at the same range. To be not higher that the maximum -149.5 dBm/Hz the interference signal level must be reduced by 4.5 dB. This could be done by selecting the modulation 8 TCM 2/3, which would reduce the interference level by 6.5 dB (decoupling by modulation type). If it would not be possible to find a more robust modulation that reduces the interference level enough, the terminal would be marked as a problem terminal (step 426) and could, e.g., be allocated a special frequency band, not used in the interfering sector (decoupling by frequency).

[0047] A special problem for the uplink (terminal to base) is that terminals from different sectors may add interference signals and it is difficult to know which terminals contribute (work on the same frequencies). This is typical for the DBA mode. However, it is not likely that more than two terminals will contribute simultaneously. Thus by using a 3 dB margin in the maximum allowed interference level the problem will be taken into account. Moreover, instead of using the figure -149.5 dBm/Hz as the maximum allowed interference signal level, the figure -152.5 dBm/Hz should be used.

[0048] Upon completion of either steps 420 or 424, the bitrate and modulation type for each terminal is be clear. Then, at step 428, when in the FBA mode, a specific frequency and bandwidth is allocated to each link, allowing for appropriate guardbands between the links. The links should basically be packed from narrow to broader channels. It should be understood that step 428 is executed only for the FBA mode. For the DBA mode the allocation of bitrate, modulation type and bandwidth is done momentarily by the control unit 70 in the sector.

[0049] At step 430 it is determined whether a new terminal is to be added to the system. When adding a new terminal

to the system, steps 432, 434, and 436 are executed. These steps are similar to operations discussed above, in that for the new terminal: (1) a modulation type is determined with regard to range [step 432], (2) the C/I is checked from all base station sectors and the modulation type adjusted if necessary [step 434], and, (3) the interference level is checked in each base station sector from the new terminal and the modulation type is adjusted if necessary to comply with the maximum allowed interference density at the base [step 436]. Network planning processor 210 can continue to operate in a loop awaiting additions of other terminals as shown in Fig. 4B.

[0050] The above-described operations and calculations of Fig. 4A and Fig. 4B are performed by Network planning processor 110 and the results thereof passed to control units 70 of the various base stations. In the DBA mode, for each terminal the highest possible modulation type is specified. It is then up to the control units 70 to decide the actual modulation, bandwidth and frequency to use. The suggested highest possible modulation types are preferably inputted to control units 70 via the network management system 102.

[0051] Thus, the invention concerns a point to multipoint radio access system, comprising a number of sectorized base station sites and a number of subscriber terminals located within the coverage area of the base station sites. The radio links between subscriber terminals and base stations all work within the same frequency band. From sector to sector the base station antennas alternate between vertical and horizontal polarization in a systematic way to minimize the potential interference areas. In accordance with the invention, the links connecting a base station site to the subscriber terminals can be allocated differing capacities and differing modulation schemes selected from a number of choices. Of the modulation schemes, the most robust scheme corresponds to the widest bandwidth needed for a specific bitrate and also to the largest range possible. The least robust modulation scheme corresponds to the most narrow bandwidth needed for a specific bitrate and also the minimum possible range.

[0052] Characteristics of the system and method thus include the following:

(1) the base stations transmit with constant power density for all specific modulation types.

(2) the terminals transmit with constant power density for all bitrates and for all modulation types measured at the range limit of the respective modulation type and decrease the power density with decreasing range to the base station so that the power density received at the base station is constant for all distances for a specific modulation type;

(3) at a given range the transmitted power density from a terminal will differ for different modulation types corresponding to the differences in C/(N+I); and

(4) the individual links to the terminals are designated a modulation type that is consistent with its range to the base station, the C/(N+I) from the various base stations and a maximum allowed interference level received at the base stations which is consistent with the required C/(N+I) and which occupies the least bandwidth.

[0053] Thus, the present invention advantageously provides a simple method to allocate modulation type, power strategy and bandwidth to each radio link in a point to multipoint system including the feature of allowing for various modulation types, considering the required coverage range, the minimum bandwidth requirement and the foreseen interference situation. The operation and allocation of the present invention is without undue consideration of other links, which could easily lead into countless iterations back and force before a satisfactory solution is achieved. The present invention also facilitates a system with dynamic channel allocation.

[0054] While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood, for example, that the polarization scheme for the antennas need not necessarily systematically alternate by sector between vertical and horizontal polarization. Moreover, the radio links can operate in more than one frequency band, e.g., two frequency bands.

Claims

1. A method of allocating radio link characteristics in a point to multipoint radio access system, the point to multipoint radio access system comprising a number of base stations including a selected base station connected by a plurality of radio links to a corresponding plurality of subscriber terminals located within respective coverage areas of the selected base station, at least some of the plurality of radio links being within a same frequency band, **characterized in that** the method comprising:

   for the selected base station (40, B1, B2), selecting a base station transmit power density which, for each of a plurality of modulation types, is constant for all bitrates (400);

for each of the plurality of subscriber terminals (T1, T2) located within the coverage area of the selected base station, selecting a terminal transmit power density which, for each of the plurality of modulation types, is constant for all bitrates (402);

determining a maximum range for each of the plurality of modulation types (404);

for each of the plurality of subscriber terminals, allocating a modulation type to the corresponding radio link dependent upon range from the selected base station (406);

determining, for each of the plurality of subscriber terminals (T1, T2), whether at the subscriber terminal there is an acceptable signal quality and, if not, allocating a next lower order modulation type to the radio link corresponding to the subscriber terminal which does not have the acceptable signal quality (408, 410, 412); and

determining at the selected base station (40, B1, B2) whether there is an acceptable signal quality with respect to each of the plurality of subscriber terminals and, if not, allocating a next lower order modulation type to the radio link corresponding to the subscriber terminal with respect to which there is not the acceptable signal quality (418, 420, 422).

2. The method of claim 1, further comprising allocating frequencies within the same frequency band and bandwidth to each of the plurality of radio links.

3. The method of claim 1, wherein the acceptable signal quality is indicated by a signal to noise and interference ratio [C/(N+I)].

4. The method of claim 1, wherein for all modulation types there is constant power density for all bitrates measured at range limits of the respective modulation types, wherein the power density decreases with decreasing range to the selected base station (40, B1, B2) whereby the power density received at the selected base station is constant for all distances for a specific modulation type, at a given range the transmitted power density from the selected subscriber terminal (T1, T2) differing for different modulation types in accordance with corresponding differences in the signal quality.

5. The method of claim 1, wherein a most robust modulation type corresponds to a widest bandwidth needed for a specific bitrate and also to a largest range possible, and a least robust modulation type corresponds to a most narrow bandwidth needed for a specific bitrate and also a minimum possible range.

6. The method of claim 1, wherein the base stations are provided with antennas, which systematically alternate by sector between vertical (V) and horizontal (H) polarization to minimize potential interference.

Patentansprüche

1. Verfahren zur Zuweisung von Funkverbindungseigenschaften in einem Punkt-zu-Mehrpunkt-Funkzugangssystem, wobei das Punkt-zu-Mehrpunkt-Funkzugangssystem eine Anzahl von Basisstationen, einschließlich einer gewählten Basisstation, umfaßt, die durch eine Vielzahl von Funkverbindungen mit einer entsprechenden Vielzahl von Teilnehmerendgeräten verbunden sind, die sich in jeweiligen Versorgungsbereichen der gewählten Basisstation befinden, wobei zumindest einige aus der Vielzahl von Funkverbindungen in einem gleichen Frequenzband sind, **dadurch gekennzeichnet, daß** das Verfahren umfaßt:

für die gewählte Basisstation (40, B1, B2), Wählen einer Basisstations-Sendeleistungsdichte, die für jeden aus einer Vielzahl von Modulationstypen bei allen Bitraten (400) konstant ist;
für jedes aus der Vielzahl von Teilnehmerendgeräten (T1, T2), die sich im Versorgungsbereich der gewählten Basisstation befinden, Wählen einer Endgerät-Sendeleistungsdichte, die für jeden aus der Vielzahl von Modulationstypen bei allen Bitraten (402) konstant ist;
Bestimmen einer maximalen Reichweite für jeden aus der Vielzahl von Modulationstypen (404);
für jedes aus der Vielzahl von Teilnehmerendgeräten, Zuweisen eines Modulationstyps der entsprechenden Funkverbindung in Abhängigkeit von der Reichweite der gewählten Basisstation (406);
Bestimmen für jedes aus der Vielzahl von Teilnehmerendgeräten (T1, T2), ob am Teilnehmerendgerät eine annehmbare Signalqualität vorhanden ist, und wenn nicht, Zuweisen eines Modulationstyps der nächstnied-

rigeren Ordnung an die Funkverbindung entsprechend dem Teilnehmerendgerät, das keine annehmbare Signalqualität hat (408, 410, 412); und
Bestimmen an der gewählten Basisstation (40, B1, B2), ob eine annehmbare Signalqualität vorhanden ist in bezug auf jedes aus der Vielzahl von Teilnehmerendgeräten, und wenn nicht, Zuweisen eines Modulationstyps der nächstniedrigeren Ordnung an die Funkverbindung entsprechend dem Teilnehmerendgerät, bei dem die annehmbare Signalqualität nicht vorhanden ist (418, 420, 422).

2. Verfahren nach Anspruch 1, ferner mit dem folgenden Schritt: Zuweisen von Frequenzen im gleichen Frequenzband und in der gleichen Frequenzbandbreite an jede aus der Vielzahl von Funkverbindungen.

3. Verfahren nach Anspruch 1, wobei die annehmbare Signalqualität durch ein Signal-Rausch und Stör-Verhältnis [C/(N + I)] angegeben wird.

4. Verfahren nach Anspruch 1, wobei für alle Modulationstypen eine konstante Leistungsdichte bei allen Bitraten vorhanden ist, die in den Reichweitegrenzen der jeweiligen Modulationstypen gemessen werden, wobei die Leistungsdichte mit abnehmender Reichweite bis zur gewählten Basisstation (40, B1, B2) abnimmt, wobei die Leistungsdichte, die an der gewählten Basisstation empfangen wird, für alle Entfernungen für einen spezifischen Modulationstyp konstant ist, wobei bei einer gegebenen Reichweite die Sendeleistungsdichte vom gewählten Teilnehmerendgerät (T1, T2) für verschiedene Modulationstypen gemäß entsprechenden Unterschieden der Signalqualität unterschiedlich ist.

5. Verfahren nach Anspruch 1, wobei ein robustester Modulationstyp einer für eine spezifische Bitrate benötigten breitesten Bandbreite und auch einer möglichst größten Reichweite entspricht, und ein am wenigsten robuster Modulationstyp einer für eine spezifische Bitrate benötigten schmalsten Bandbreite und auch einer möglichst geringen Reichweite entspricht.

6. Verfahren nach Anspruch 1, wobei die Basisstationen mit Antennen versehen sind, die systematisch um einen Sektor zwischen einer vertikalen (V) und einer horizontalen (H) Polarisation alternieren, um die potentielle Interferenz zu minimieren.

Revendications

1. Procédé d'allocation de caractéristiques de liaison radio dans un système d'accès radio point à multipoint, le système d'accès radio point à multipoint comprenant un certain nombre de stations de base incluant une station de base sélectionnée qui est connectée au moyen d'une pluralité de liaisons radio à une pluralité correspondante de terminaux d'abonnés qui sont localisés à l'intérieur de zones de couverture respectives de la station de base sélectionnée, au moins certaines de la pluralité de liaisons radio étant à l'intérieur d'une même bande de fréquences, **caractérisé en ce que** le procédé comprend:

pour la station de base sélectionnée (40, B1, B2), la sélection d'une densité de puissance d'émission de station de base qui, pour chacun d'une pluralité de types de modulation, est constante pour tous les débits de bits (400);
pour chacun de la pluralité de terminaux d'abonnés (T1, T2) qui sont localisés à l'intérieur de la zone de couverture de la station de base sélectionnée, la sélection d'une densité de puissance d'émission de terminal qui, pour chacun de la pluralité de types de modulation, est constante pour tous les débits de bits (402);
la détermination d'une plage maximum pour chacun de la pluralité de types de modulation (404);
pour chacun de la pluralité de terminaux d'abonnés, l'allocation d'un type de modulation à la liaison radio correspondante en fonction d'une plage par rapport à la station de base sélectionnée (406);
la détermination, pour chacun de la pluralité de terminaux d'abonnés (T1, T2), de si oui ou non, au niveau du terminal d'abonné, il y a une qualité de signal acceptable et si ce n'est pas le cas, l'allocation d'un type de modulation d'ordre plus faible suivant à la liaison radio correspondant au terminal d'abonné qui ne dispose pas de la qualité de signal acceptable (406, 410, 412); et
la détermination, au niveau de la station de base sélectionnée (40, B1; B2), de si oui ou non il y a une qualité de signal acceptable par rapport à chacun de la pluralité de terminaux d'abonnés et si ce n'est pas le cas, l'allocation d'un type de modulation d'ordre plus faible suivant à la liaison radio correspondant au terminal d'abonné en relation avec lequel il n'y a pas la qualité de signal acceptable (418, 420, 422).

2. Procédé selon la revendication 1, comprenant en outre l'allocation de fréquences, à l'intérieur de la même bande de fréquences et de la même largeur de bande, à chacune de la pluralité de liaisons radio.

3. Procédé selon la revendication 1, dans lequel la qualité de signal acceptable est indiquée au moyen d'un rapport signal sur bruit et interférence [C/(N + I)].

4. Procédé selon la revendication 1, dans lequel, pour tous les types de modulation, il y a une densité de puissance constante pour tous les débits de bits mesurés pour des limites de plage des types de modulation respectifs, dans lequel la densité de puissance diminue avec une plage décroissante sur la station de base sélectionnée (40, B1, B2) et ainsi, la densité de puissance qui est reçue au niveau de la station de base sélectionnée est constante pour toutes les distances pour un type de modulation spécifique, et pour une plage donnée, la densité de puissance émise depuis le terminal d'abonné sélectionné (T1, T2) différant pour différents types de modulation conformément à des différences correspondantes au niveau de la qualité de signal.

5. Procédé selon la revendication 1, dans lequel un type de modulation le plus robuste correspond à une largeur de bande la plus large nécessaire pour un débit de bits spécifique et également à une plage possible la plus grande et un type de modulation le moins robuste correspond à une largeur de bande la plus étroite nécessaire pour un débit de bits spécifique et également une plage possible minimum.

6. Procédé selon la revendication 1, dans lequel les stations de base sont munies d'antennes qui sont en alternance de façon systématique, au moyen d'un secteur entre les polarisations verticale (V) et horizontale (H) afin de minimiser une interférence potentielle.

Fig. 1 Microwave coverage network

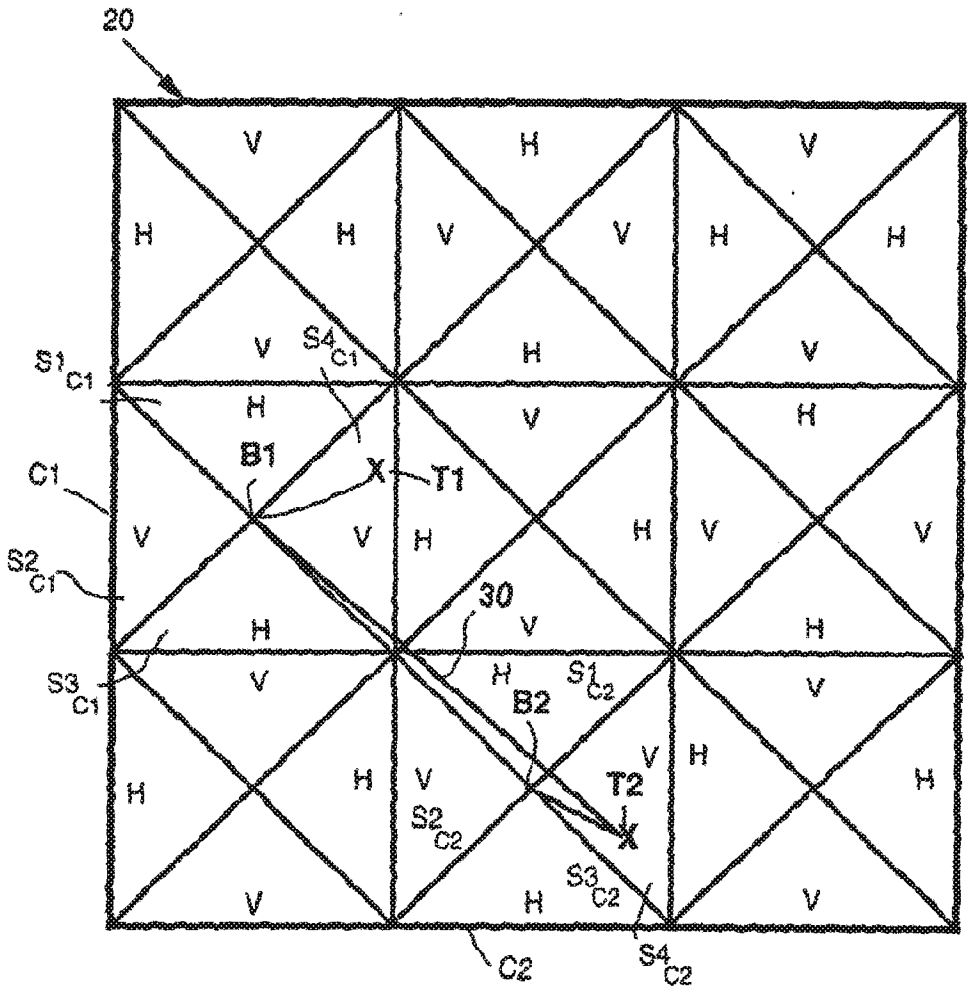
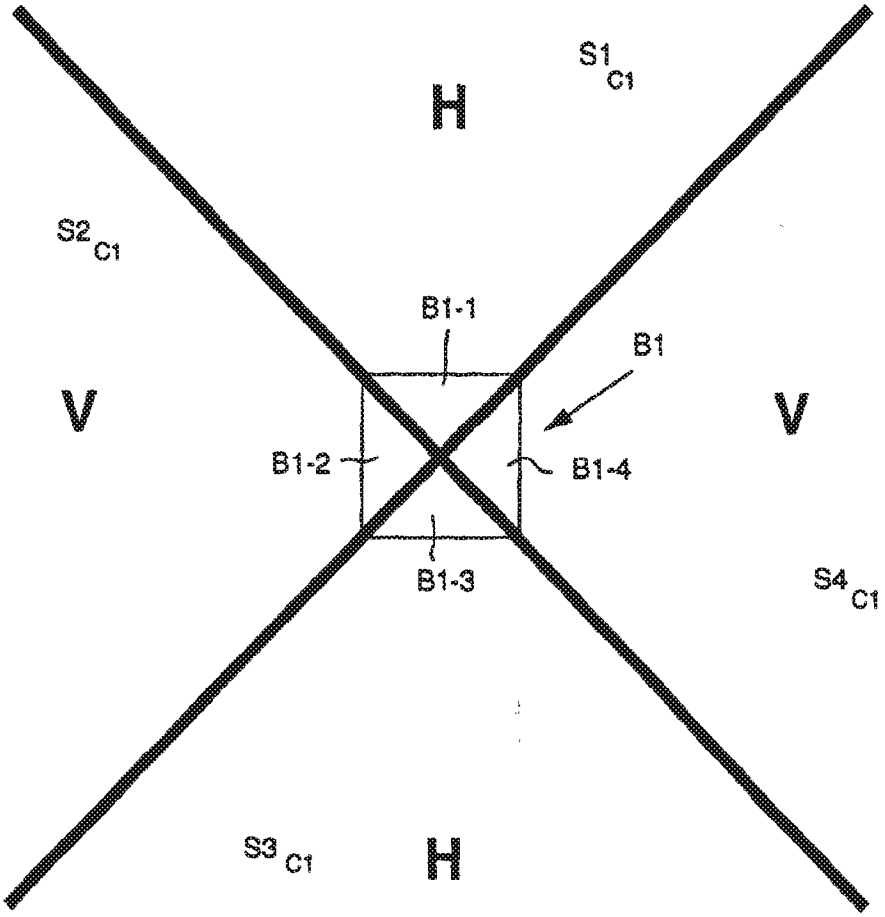


FIG. 4A

FIG. 4B

Fig. 4

Fig. 1A



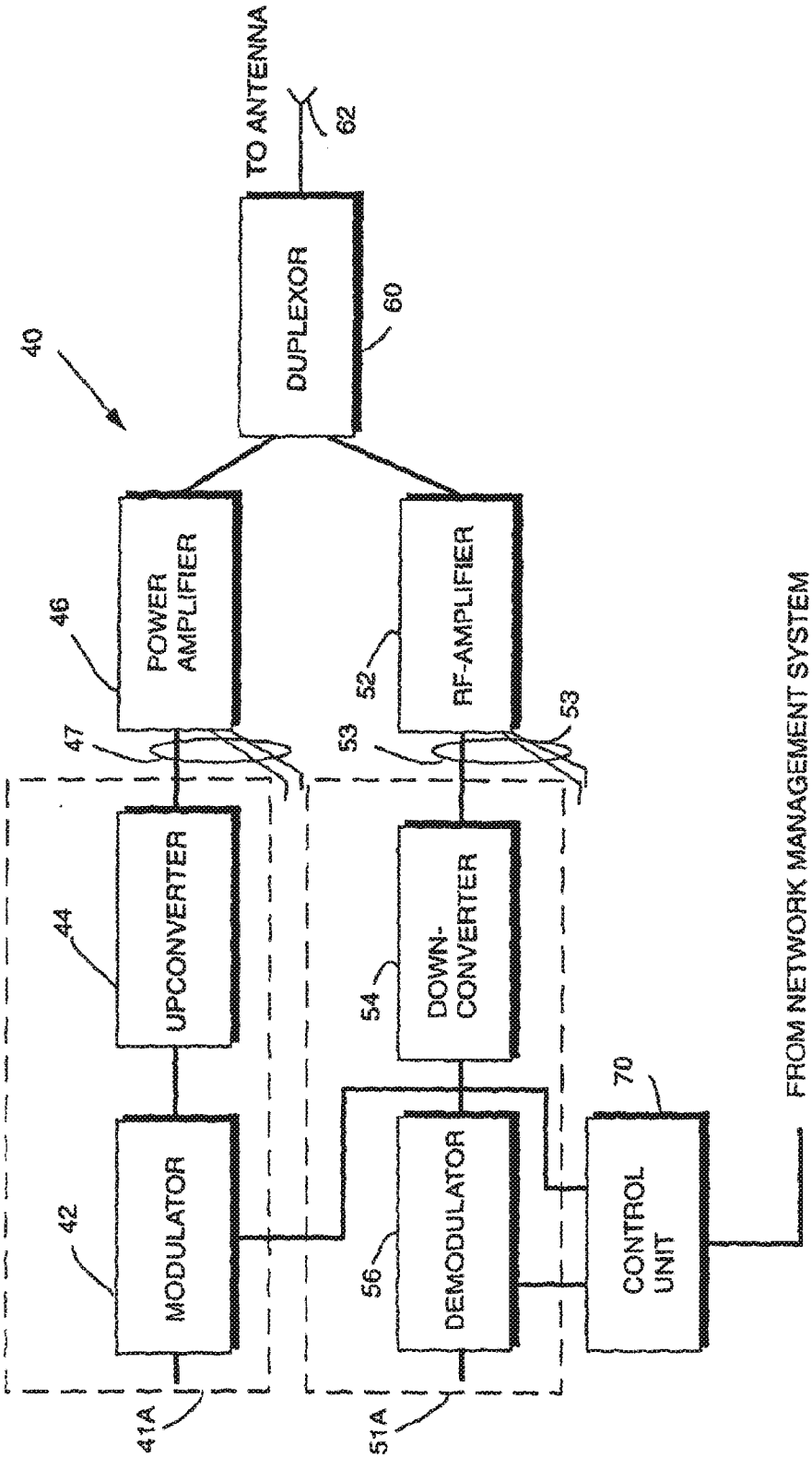


Fig. 2 Basic base station block diagram

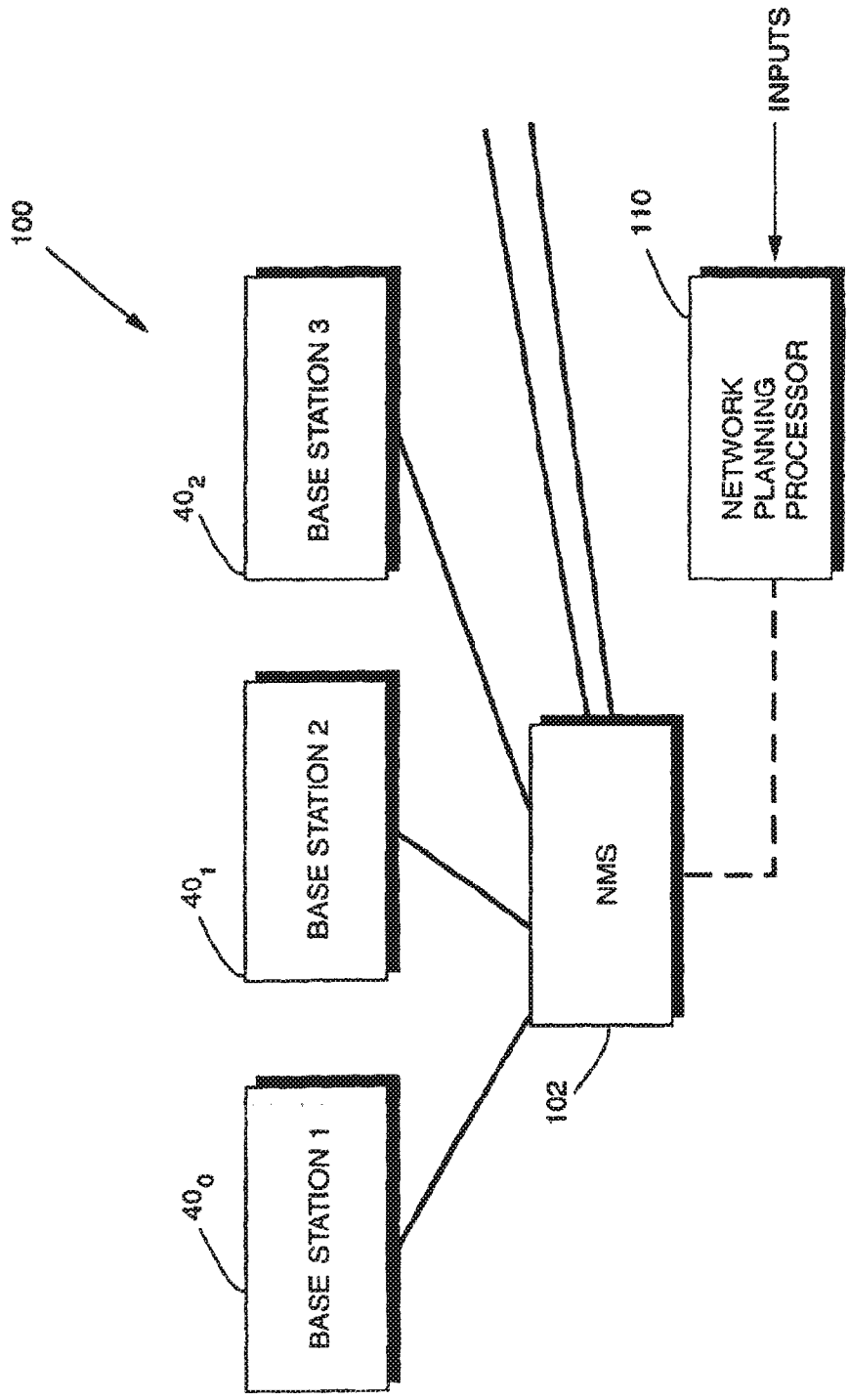


Fig. 3 Basic base station network

Fig. 4A

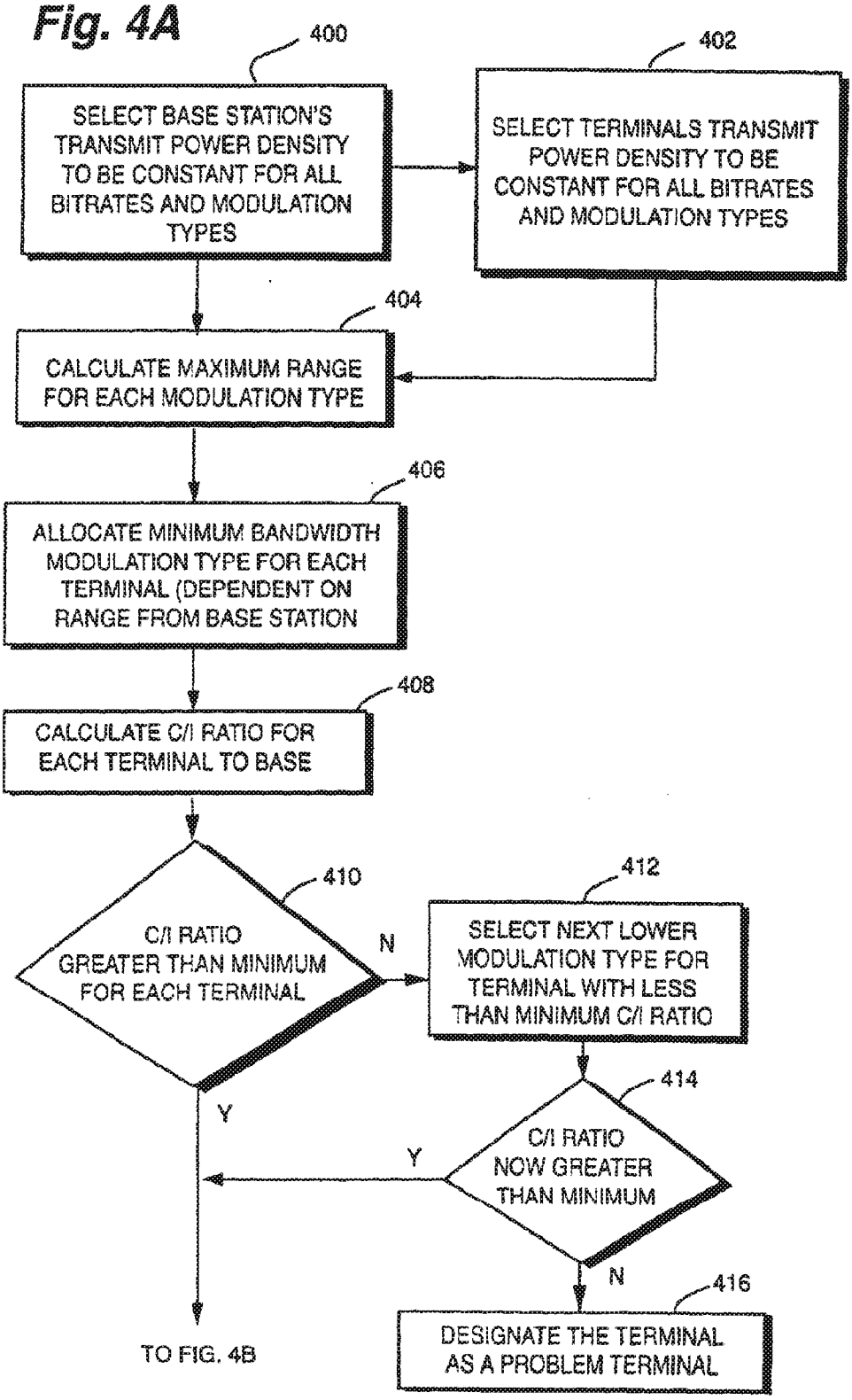
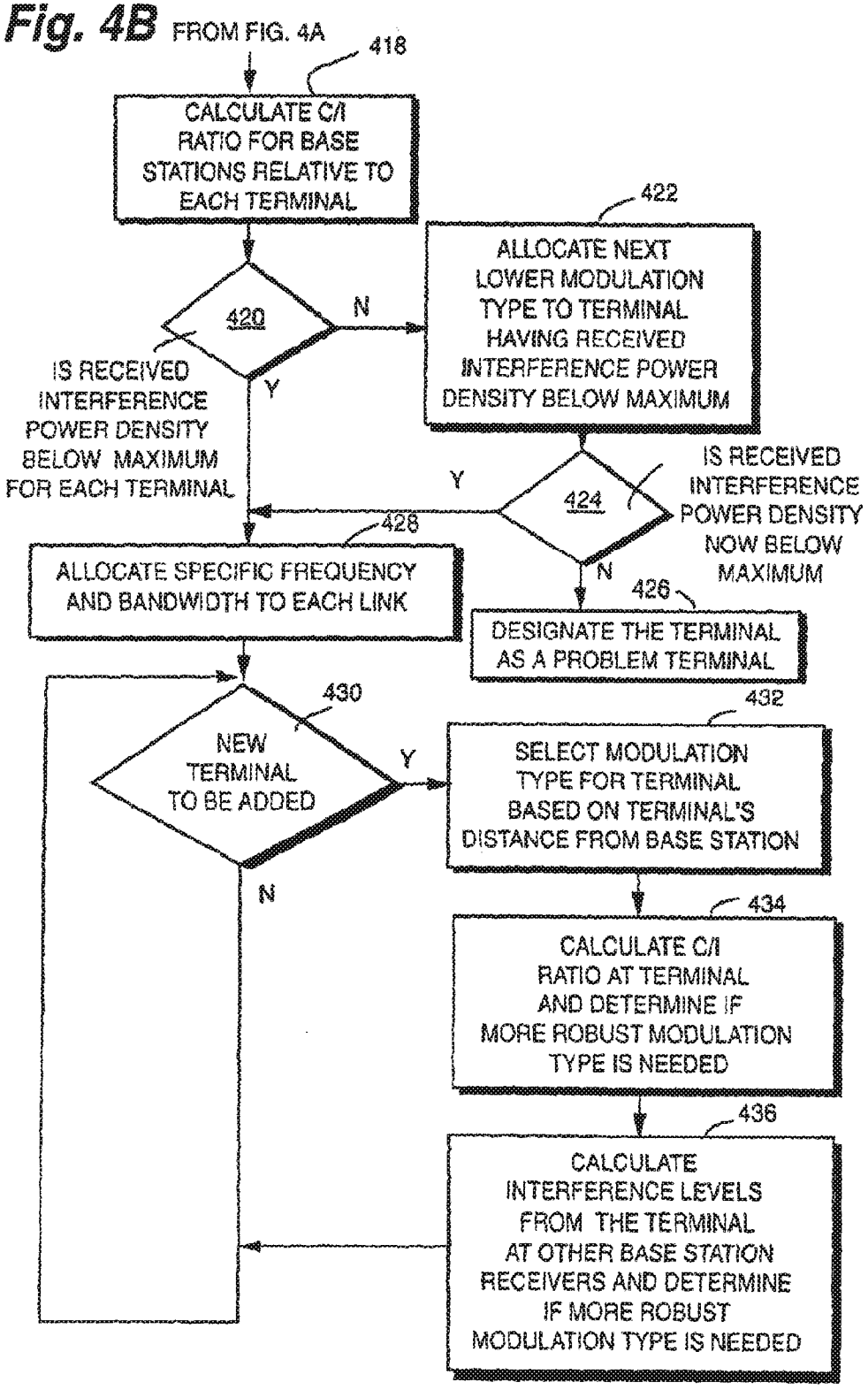


Fig. 4B



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- **KANNAN RAMCHANDRAN: "MULTIRESOLUTION BROADCAST FOR DIGITAL HDTV USING JOINT SOURCE/ CHANNEL CODING", IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS, IEEE INC. NEW YORK, US, VOL. 11, NR. 1, PAGE(S) 6-22 XP000377993 ISSN: 0733-8716 * Seite 1, rechte Spalte, Zeile 12 - Zeile 26 * * Seite 5, rechte Spalte, Zeile 11 - Seite 6, linke Spalte, Zeile 23 * * Abbildungen 6-8,17 ***
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Beschreibung

Stand der Technik

[0001] Die Erfindung geht aus von einem Verfahren zur Vergrößerung der mit einem Multiträger-Übertragungsverfahren über Rundfunk übertragenen Datenrate, sowie einem Sender und einem Empfänger, insbesondere stationäre Geräte, nach der Gattung der unabhängigen Ansprüche.

Aus dem Stand der Technik ist die Übertragung von digitalen Daten nach dem ETS 300 401 bekannt, der entwickelt wurde um den mobilen Multimediaempfang über terrestrische, digitale Rundfunksysteme zu standardisieren. Dieser zunächst für den Hörfunk konzipierte Standard DAB (Digital Audio Broadcasting) eignet sich auch für die mobile Fernsehübertragung. Beim DAB-Verfahren bietet sich die Möglichkeit, die gesamte Bandbreite von 1,5 MHz für die Datenübertragung von Videodaten zur Verfügung zu stellen. So können Daten mit einer maximalen Datenrate von ungefähr 1,8 Mbit/s zum mobilen Empfänger übertragen werden. Diese Datenrate erlaubt unter Einsatz bisheriger Kompressionsverfahren (MPEG) eine gute Qualität auf Bildschirmen, wie sie bei mobilen Geräten eingesetzt werden. Da ein über DAB ausgestrahltes Fernsehprogramm auch stationär empfangen werden kann, können bei den wesentlich größeren Bildschirmdiagonalen, Kodierungseffekte, Unschärfe oder Blockbildung sichtbar werden. Für eine Darstellung auf größeren Bildschirmen ist eine größere Datenübertragungsrate notwendig. Aus "X-DAB - Eine abwärtskompatible Erweiterung des DAB-Standards für Multimediaanwendungen", Kleinheubacher Berichte, 1996, G. Zimmermann u. H. Schulze, ist eine Erweiterung des DAB-Verfahrens bekannt, wobei ein kodiertes 8-PSK-(Phase Shift Keying) Verfahren als Modulationsverfahren angewendet wird. Diese Erweiterung das sogenannte X-DAB bietet die Möglichkeit, die mobil zu empfangenden Datenraten um 20 % zu erhöhen. Das Modulationsverfahren macht es allerdings für bisher konventionelle DAB-Empfänger unmöglich, die Signale zu empfangen.

[0002] Aus EP 616 454 A1 ist ein digitales Übertragungsverfahren bekannt, das eine sogenannte Multi-Resolution-Modulation ermöglicht. Dabei können Daten mit unterschiedlichen Modulationsverfahren moduliert werden. Aus K. Ramchandran et al.: Multiresolution Broadcast for Digital HDTV Using Joint Source/Channel Coding, IEEE Journal on Selected Areas in Communications, New York, US, Vol. 11 Nr. 1, Seiten 6 bis 22 ist ebenfalls die Verwendung der Multi-Resolution-Modulation für die Übertragung von digitalen HDTV-Signalen bekannt. Auch R. Kays: Kanalcodierung und Modulation für die digitale Fernsehübertragung, Fernseh- und Kinotechnik, VDE Verlag, Berlin, Vol. 48, Nr. 3, Seiten 109 bis 114 zeigt die Verwendung einer hierarchischen Übertragung eines HDTV-Programms in einem 8 MHz-Kanal. Dabei wird eine Multi-Resolution-QAM verwendet. Aus K. Pazel et al.: A Concept of Digital Tewestrial Television Broadcasting, Wireless Personal Communications Kluwer, Vol. 2, Nr. 1 bis 2, Seiten 9 bis 27 ist es bekannt, HDTV-Signale in drei Stufen mit unterschiedlichen Codierungen bereitzustellen, um eine "graceful degradation" empfängerseitig zu ermöglichen. Damit liegt das gleiche Signal verschieden aufgelöst vor. Es können dabei Modulationsverfahren wie QPSK und QAM verwendet werden. Dies ermöglicht insbesondere Empfang durch stationäre und mobile Empfänger mit angepassten Empfangsqualitäten.

Vorteile der Erfindung

[0003] Das erfindungsgemäße Verfahren mit den kennzeichnenden Merkmalen des Hauptanspruchs 1 hat demgegenüber den Vorteil, die übertragene Datenrate zu erhöhen, indem zwei Datenströme getrennt voneinander moduliert und anschließend vor der Übertragung kombiniert werden. Mit der zusätzlichen Modulation lassen sich die Datenraten stark steigern. Durch das erfindungsgemäße Verfahren ist es möglich, daß ein Empfänger, der nur Daten, die mit einem ersten Modulationsverfahren moduliert werden, empfangen kann, die Daten problemlos empfängt, während ein weiterer, z. B. stationärer Empfänger die Daten, die mit dem zweiten Modulationsverfahren moduliert werden, zusätzlich verarbeiten kann. Dadurch wird das Übertragungsverfahren an die im Augenblick gegebenen Modulationsverfahren angepaßt, während es gleichzeitig zusätzliche Informationen für verbesserten Empfang liefert.

[0004] Durch die in den Unteransprüchen aufgeführten Maßnahmen ist eine vorteilhafte Weiterbildung und Verbesserung des im unabhängigen Anspruch angegebenen Verfahrens möglich. Besonders vorteilhaft ist es, wenn die Daten des zweiten Teildatenstroms mit einer Amplituden-Modulation oder anderen alternativen Modulationsverfahren moduliert werden.

[0005] Vorteilhaft ist es weiterhin, daß die Daten des ersten Teildatenstroms einer DQPSK-Modulation (Differential Quadrature Phase Shift Keying) unterzogen werden. Dadurch ist es für konventionelle Empfänger des DAB-Verfahrens möglich die Daten des ersten Teildatenstroms zu empfangen.

[0006] Vorteilhafter Weise enthalten die Daten des ersten Teildatenstroms alle notwendigen Informationen, um z. B. ein Fernsehbild in einem mobilen Empfänger darzustellen. Der zweite Teildatenstrom enthält zusätzliche Informationen, die zu einer besseren Bildqualität in einem stationären Empfänger verarbeitet werden können.

[0007] Der erfindungsgemäße Sender zur Vergrößerung der übertragenen Datenrate mit den kennzeichnenden Merkmalen des unabhängigen Anspruchs 6 hat den Vorteil, daß er zusätzlich zu den Bauteilen, die ein Sender für das DAB-Verfahren aufweisen muß, einen weiteren Modulator für den zweiten Teildatenstrom enthält. Zusätzlich ist ein Kombinierer für die mit den un-

terschiedlichen Modulationsverfahren modulierten Teildatenströme vorhanden.

[0008] Vorteilhafter Weise ist der zweite Modulator ein Amplitudenmodulator oder ein äquivalenter Modulator.

[0009] Der erfindungsgemäße Empfänger zum Empfang von digitalen Daten mit den kennzeichnenden Merkmalen des unabhängigen Anspruchs 8 hat den Vorteil, daß er einen Abzweig für einen zweiten Teildatenstrom aufweist, in dem ein zweiter Demodulator vorhanden ist. Vorteilhafter Weise enthält der Empfänger einen Decoder, der die Teildatenströme zusammenführen kann.

Zeichnung

[0010] Ein Ausführungsbeispiel der Erfindung ist in der Zeichnung dargestellt und in der nachfolgenden Beschreibung näher erläutert. Es zeigt Figur 1 einen erfindungsgemäßen Sender, Figur 2 einen erfindungsgemäßen Empfänger und Figur 3 eine Darstellung des erfindungsgemäßen Modulationsverfahrens.

Beschreibung des Ausführungsbeispiels

[0011] Figur 1 zeigt das Schaltungsschema für einen erfindungsgemäßen Sender. Auf der linken Seite erkennt man die verschiedenen Datenquellen bestehend aus den Videodaten 1, den Audiodaten 2, allgemeinen Daten 3 und Paketdaten 4. Video-, Audio- und sonstige Daten werden in einen MPEG-Enkoder 5 eingespeist, der die Daten in zwei Teilströme kodiert. Der erste Teilstrom 7 durchläuft einen DVB-Enkoder 8 und einen DAB-Enkoder 9. Der zweite Datenstrom 6 wird ebenfalls über den DVB-Enkoder 8 und den DAB-Enkoder geführt. Weitere Audiodaten 2 werden über einen Audioenkoder 10, den DAB-Enkoder 9 zu einem DAB-Multiplexer 12 geführt. Die Paketdaten 4 durchlaufen einen Paketmultiplexer 11, den DAB-Enkoder 9 und den DAB-Multiplexer 12. Alle Daten des ersten Teildatenstroms 40 durchlaufen eine DQPSK-Modulation 13. Der zweite Datenstrom 41 durchläuft einen Amplitudenmodulator 14 und wird in einem Kombinierer 15 mit dem Datenstrom 40 zusammengeführt. Die resultierenden Daten 42 durchlaufen einen OFDM-Generator 16 und werden über eine Antenne 17 abgestrahlt.

[0012] Das analoge Fernsehsignal liegt zunächst als Kombination aus Videodaten 1, Audiodaten 2, sowie anderen Daten 3 vor. Dieses Signal wird im MPEG-Enkoder 5 komprimiert. Das komprimierte Videosignal besteht dabei aus zwei Teildatenströmen: Dem Low-Definition-Teildatenstrom 7 für eine Basis-Bildqualität, sowie den Standarddefinition-Teildatenstrom 6, der zusammen mit dem Low-Definition-Datenstrom 7 eine verbesserte Bildqualität für einen stationären Empfänger ermöglicht. Die Datenrate der Teildatenströme richtet sich nach der möglichen Übertragungskapazität der Teilkanäle. Der Teildatenstrom 40, der für den mobilen Empfang gedacht ist, hat eine maximale Nutzdatenrate von etwa 1,8 MBit/s. Der zweite Teildatenstrom 6 für den stationären Empfänger, der zusammen mit dem für mobile Teilnehmer gesendeten Teildatenstrom 7 eine verbesserte Bildqualität auf einem großen Bildschirm ermöglicht, beträgt je nach verwendeter Kanalcodierung ebenfalls ca. 1,8 MBit/s. Beide Übertragungskanäle haben eine maximale Kapazität von ca. 2,3 MBit/s. Der für den mobilen Empfänger bestimmten Teildatenstrom 7, sowie der zusätzliche Teildatenstrom 6 werden wie bisher im DAB-Sender mit einem äußeren Fehlerschutz versehen. Dazu durchlaufen die Daten den DVB-Enkoder 8, der in mehreren Schritten den Fehlerschutz beaufschlagt, durch DVB-Energy-Dispersal, äußeren Reed-Solomon-Code und äußeren Faltungsinterleaver. Es folgen für beide Teildatenströme die im DAB-Verfahren vorgesehenen Schritte für die Übertragung im Stream-Mode. Die Daten durchlaufen den DAB-Enkoder 9 der die Schritte DAB-Energy-Dispersal, DAB-Faltungscoding und DAB-Faltungsinterleaver enthält. Im folgenden DAB-Multiplexer 12 werden die Daten des Teildatenstroms 7 mit evtl. vorhandenen zusätzlichen Audiodaten 2 oder Paketdaten 4 gemischt, und aus der Gesamtheit der Daten der DAB-Übertragungsrahmen gebildet. Der erste Datenstrom 40 durchläuft einen DQPSK (Differential Quadrature Phase Shift Keying) -Modulator mit vorgeschaltetem Frequenzinterleaving. Der für den stationären Empfänger bestimmte Datenstrom 6 durchläuft den gleichen äußeren Fehlerschutz wie der erste Datenstrom 7 sowie die DAB-Kodierung. Im folgenden Amplitudenmodulator 14 werden die eingehenden Bits mit einem bestimmten Modulationsverfahren kodiert. Der darauffolgende Kombinierer 15 kombiniert die Datenströme 41 und 40 mit den unterschiedlichen Modulationsverfahren zu einem resultierenden Datenstrom 42, der nach der OFDM-Modulation über die Antenne 17 gesendet wird.

Figur 3 zeigt die Darstellung des Modulationsverfahrens an drei Beispielen. Aufgetragen ist in Figur 3a bis 3c der komplexe Phasenraum. Im komplexen Phasenraum sind die DQPSK-Symbole 34 dargestellt. Im Beispiel Figur 3a wird dem zweiten Datenstrom 41 durch eine Amplitudenmodulation eines von vier möglichen Symbolen, die als Punkte ausgeführt sind, zugeordnet. Die Zuordnung entspricht in diesem Beispiel einer Gray-Kodierung, d. h. um Doppelfehler bei falscher Detektion zu vermeiden wird so durchnumeriert, daß wenn man bei der Detektion um ein Symbol danebenliegt, in jedem Fall ein Bit korrekt empfangen wird. Im Kombinierer 15 werden die DQPSK-Symbole 34 mit den entsprechend zugewiesenen Amplituden des Modulators 14 beaufschlagt. Die daraus resultierenden Signalpunkte sind in Figur 3a dargestellt. Der relative Abstand der Signalpunkte zueinander, der durch die Amplitude des Signals bestimmt ist, beeinflußt die Empfangseigenschaften sowohl vom mobilen als auch stationären Empfänger. So bedeutet eine enge Lage der vier amplitudenmodulierten Signalpunkte zueinander keine oder eine sehr ge-

ringe Verschlechterung der mobilen Empfangseigenschaften auf Kosten der stationären Empfangseigenschaften, da ein größerer Signal-Störungsabstand benötigt wird. Dagegen lassen sich bei zunehmendem Abstand der Signalpunkte zueinander, d. h. bei größeren Amplituden, die Empfangseigenschaften vom mobilen und stationären Empfänger gegeneinander abwägen. Dies ermöglicht eine große Flexibilität des Übertragungsverfahrens in Bezug auf gewünschte oder vorgegebene Empfangseigenschaften. Alternativ zu der Amplitudenmodulation aus Figur 3a ist in Figur 3b eine Quadratureamplitudenmodulation in Verbindung mit der DQPSK-Modulation dargestellt. In Figur 3 c wird die Möglichkeit einer Phasenshiftmodulation in Kombination mit der DQPSK-Modulation gezeigt. Alle Modulationskombinationen haben die Eigenschaft, daß die Signalpunkte innerhalb der DQPSK-Symbole liegen. Das bedeutet, daß ein Standard DAB-Empfänger die Signale, innerhalb der von den Symbolen vorgegebenen Rahmen empfangen kann. Das bedeutet auch daß ein normaler DAB-Empänger von der zusätzlichen Modulation nicht beeinflußt wird.

[0013] Figur 2 stellt das Schaltschema eines erfindungsgemäßen Empfängers dar. Eingangsseitig ist die Antenne 17 mit dem A/D-Wandler 18 und der Synchronisierung 19 verbunden. Anschließend ist ein schneller Fouriertransformator 20, und ein DQPSK-Demodulator 21 einem DAB-Multiplexer 22 vorgeschaltet. Der DAB-Demultiplexer 22 ist über einen DAB-Decoder 24 sowie einem Audio-Decoder 27 mit der Audiosenke 30 und über einen Paketdemultiplexer 28 mit der Paketdatensenke 29 verbunden. Videodaten werden in einem DVB-Decoder 25 in einem MPEG-Decoder 26 eingespeist, von wo aus sie mit den Audiosenken 30, mobilen Videosenken 32, stationären Videosenken 33, sowie weiteren Datensenken 31 verbunden sind. Nach dem DQPSK-Demodulator 21 zweigt ein Signalzweig zu einem Amplituden-Demodulator 23 ab. Dieser ist über einen DAB-Decoder 24 mit einem DVB-Decoder 25 und dem MPEG-Decoder 26 verbunden.

[0014] Über die Antenne 17 wird das OFDM-Symbol empfangen und im A/D-Wandler 18 einer Analog-Digitalwandlung unterzogen. Anschließend erfolgt die Zeit-, Frequenz- und Phasensynchronisation im Synchronisierer 19. Das Datensignal wird von der schnellen Fourier-Transformation 20 zerlegt und im DQPSK-Demodulator 21 demoduliert. Nach dem Demodulator 21 folgen für den mobilen Empfänger die Verarbeitungsschritte wie bei einer konventionellen Videoübertragung. Der stationäre Empfänger verwendet für den Demodulator 23 eine Amplitudenschätzung aus dem Phasenreferenzsymbol nach der Synchronisierung 19, um die Amplitudendemodulation durchzuführen. Hier werden aus der Amplitude des komplexen DQPSK-Symbols die zwei fehlenden Codebits gewonnen. Es folgt die DAB-konforme Kanalkodierung im Decoder 24 und die DVB-konforme äußere Kanaldecodierung. Der Quelldecoder der MPEG-Decoder 26 stellt dem mobilen Empfänger den Low-Definition Teilstrom 7 für das Videosignal zur Verfügung. Zudem erhält er die zugehörigen Audioinformationen und evtl. gesendete Daten. Ein stationärer Empfänger kann mit Hilfe des zusätzlichen Datenstroms 6, Zusatzanteil für Standarddefinition, und eines hierarchischen MPEG-Decoders ein verbessertes Fernsehbild darstellen.

[0015] Bei dem erfindungsgemäßen Verfahren wird die volle Kompatibilität mit der bisherigen mobilen Fernsehübertragung über das DAB-Verfahren möglich. Das heißt DAB-Geräte für den mobilen Fernsehempfang können sowohl eine einstufige Standarddefinition als auch die erste Stufe eines hierarchischen Low-Definition/Standarddefinition-Fernsehsignals empfangen und wiedergeben. Es ist wesentlich einfacher mobile Endgeräte zur Videoübertragung für die Bandbreite von 1,5 MHz zu realisieren, als Systeme, die eine größere Bandbreite erforderlich machen. Durch die große Flexibilität der Wahl der Lage der amplitudenmodulierten Signalpunkte im Hinblick auf gewünschte bzw. geforderte Empfangseigenschaften der mobilen und der stationären Empfänger sind bessere Realisierungen möglich.

Patentansprüche

1. Verfahren zur Vergrößerung der mit einem Multiträgerübertragungsverfahren über Rundfunk übertragenen Datenrate, insbesondere für stationären Empfang, wobei digitale Daten in zwei Datenströme geteilt werden und ein erster Teildatenstrom (40) mit einem ersten Modulationsverfahren (13) moduliert wird, wobei ein zweiter Teildatenstrom (41) mit einem zweiten Modulationsverfahren (14) moduliert wird und wobei beide Teildatenströme vor der Übertragung kombiniert werden, **dadurch gekennzeichnet, dass** beide Teildatenströme (6, 7) zuerst einen DVB-Encoder (8) und dann einen DAB-Encoder (9) zur Bildung eines DAB-Übertragungsrahmens durchlaufen.

2. Verfahren zur Vergrößerung der übertragenen Datenrate über Rundfunk nach Anspruch 1, **dadurch gekennzeichnet, dass** die Daten des zweiten Teildatenstroms (41) einer Amplitudenmodulation oder einer Quadraturamplitudenmodulation oder einer Phase Shift Keying-Modulation unterzogen werden.

3. Verfahren zur Vergrößerung der übertragenen Datenrate über Rundfunk nach Anspruch 1 oder 2, **dadurch gekennzeichnet, dass** die Daten des ersten Teildatenstroms (40) einer DQPSK-Modulation unterzogen werden.

4. Verfahren zur Vergrößerung der übertragenen Datenrate über Rundfunk nach Anspruch 1 bis 3, **dadurch gekennzeichnet, dass** der zweite Teildaten-

strom (41) zusätzliche Informationen zum ersten Teildatenstrom (40) enthält.

5. Verfahren zur Vergrößerung der übertragenen Datenrate über Rundfunk nach Anspruch 1 bis 4, **dadurch gekennzeichnet, dass** die digitalen Daten Fernsehbilder enthalten und im ersten Teildatenstrom (40) Daten für das Basisbild und im zweiten Teildatenstrom (41) Daten für ein Standardbild übertragen werden.

6. Sender zur Vergrößerung der übertragenen Datenrate über Rundfunk, wobei der Sender zur Verarbeitung der Audio- (2), Video- (1) und sonstigen Daten (3, 4), Encoder (5, 8, 9, 10), einen Multiplexer (12) sowie einen ersten Modulator (13) aufweist, wobei ein erster Encoder (5) einen ersten und zweiten Teildatenstrom erzeugt und ein zweiter Modulator (14) für den zweiten Teildatenstrom (41) und ein Kombinierer (15) für den ersten und zweiten Teildatenstrom vorhanden ist, **dadurch gekennzeichnet, dass** für beide Teildatenströme (6, 7) für die Codierung zuerst ein DVB-Encoder (8) und dann ein DAB-Encoder (9) vorhanden sind, wobei der Sender derart konfiguriert ist, dass er einen DAB-Übertragungsrahmen bildet.

7. Sender zur Vergrößerung der übertragenen Datenrate über Rundfunk nach Anspruch 6, **dadurch gekennzeichnet, dass** der zweite Modulator ein Amplitudenmodulator oder ein Quadraturamplitudenmodulator oder ein Phase Shift Keying-Modulator ist.

8. Empfänger zum Empfang von digitalen Daten über Rundfunk, wobei der Empfänger einen A/D-Wandler (18), ein Synchronisationsbauteil (19), eine FFT (20), einen ersten Demodulator (21), sowie Demultiplexer (22), Decoder (25, 24, 26, 27, 28) mit Anschlüssen zu den jeweiligen Datensenken (29, 30, 31, 32, 33) aufweist, wobei nach dem ersten Demodulator (21) ein Abzweig für einen zweiten Teildatenstrom (41) in einen zweiten Demodulator (23) vorhanden ist und wobei ein Decoder (26) die Teildatenströme zusammenführt, **dadurch gekennzeichnet, dass** für beide Teildatenströme ein DAB- und ein DVB-Decoder (24, 25) vorgesehen sind, wobei die Teildatenströme zuerst den DAB- und dann den DVB-Decoder (24, 25) durchlaufen.

9. Empfänger von digitalen Daten über Rundfunk nach Anspruch 8, **dadurch gekennzeichnet, dass** der zweite Demodulator (23) ein Amplitudendemodulator oder ein Quadraturamplitudendemodulator oder ein Phase Shift Keying-Demodulator ist.

Claims

1. Method for increasing the data rate transmitted by broadcast radio using a multicarrier transmission method, particularly for stationary reception, where digital data are divided into two datastreams, and a first subsidiary datastream (40) is modulated using a first modulation method (13), with a second subsidiary datastream (41) being modulated with a second modulating method (14), and where the two subsidiary datastreams are combined before transmission, **characterized in that** the two subsidiary datastreams (6, 7) first pass through a DVB encoder (8) and then through a DAB encoder (9) in order to form a DAB transmission frame.

2. Method for increasing the transmitted data rate by broadcast radio according to Claim 1, **characterized in that** the data in the second subsidiary datastream (41) are subjected to amplitude modulation or to quadrature amplitude modulation or to phase shift keying modulation.

3. Method for increasing the transmitted data rate by broadcast radio according to Claim 1 or 2, **characterized in that** the data in the first subsidiary datastream (40) are subjected to DQPSK modulation.

4. Method for increasing the transmitted data rate by broadcast radio according to Claim 1 to 3, **characterized in that** the second subsidiary datastream (41) contains additional information relating to the first subsidiary datastream (40).

5. Method for increasing the transmitted data rate by broadcast radio according to Claim 1 to 4, **characterized in that** the digital data contain television pictures, and the first subsidiary datastream (40) is used to transmit data for the base picture, and the second subsidiary datastream (41) is used to transmit data for a standard picture.

6. Transmitter for increasing the transmitted data rate by broadcast radio, where the transmitter has encoders (5, 8, 9, 10), a multiplexer (12) and a first modulator (13) in order to process the audio (2), video (1) and other data (3, 4), where a first encoder (5) produces a first and a second subsidiary datastream, and a second modulator (14) for the second subsidiary datastream (41) and a combiner (15) for the first and the second subsidiary datastream are provided, **characterized in that** first a DVB encoder (8) and then a DAB encoder (9) are provided for the coding for the two datastreams (6, 7), with the transmitter being configured such that it forms a DAB transmission frame.

7. Transmitter for increasing the transmitted data rate

by broadcast radio according to Claim 6, **characterized in that** the second modulator is an amplitude modulator or a quadrature amplitude modulator or a phase shift keying modulator.

8. Receiver for receiving digital data by broadcast radio, where the receiver has an A/D converter (18), a synchronization component (19), an FFT (20), a first demodulator (21), and also a demultiplexer (22), decoders (25, 24, 26, 27, 28) with connections to the respective data sinks (29, 30, 31, 32, 33), where a branch for a second subsidiary datastream (41) into a second demodulator (23) is provided downstream of the first demodulator (21), and where a decoder (26) combines the subsidiary datastreams, **characterized in that** a DAB decoder and a DVB decoder (24, 25) are provided for the two subsidiary datastreams, with the subsidiary datastreams first passing through the DAB decoder and then through the DVB decoder (24, 25).

9. Receiver for digital data by broadcast radio according to Claim 8, **characterized in that** the second demodulator (23) is an amplitude demodulator or a quadrature amplitude demodulator or a phase shift keying demodulator.

Revendications

1. Procédé pour augmenter le débit de données transmises par radiodiffusion avec un procédé de transmission multiporteuse, en particulier pour la réception fixe, selon lequel des données numériques sont divisées en deux flux de données, un premier flux de données (40) est modulé avec un premier procédé de modulation (13), un deuxième flux de données (41) est modulé avec un deuxième procédé de modulation (14), les deux flux de données étant combinés avant la transmission,
caractérisé en ce que
les deux flux de données (6, 7) traversent tout d'abord un encodeur DVB (8) puis un encodeur DAB (9) pour former un cadre de transmission DAB.

2. Procédé pour augmenter le débit de données transmises par radiodiffusion selon la revendication 1,
caractérisé en ce que
les données du deuxième flux partiel de données (41) sont soumises à une modulation d'amplitude ou une modulation d'amplitude en quadrature ou à une modulation Phase Shift Keying.

3. Procédé pour augmenter le débit de données transmises par radiodiffusion selon la revendication 1 ou 2,
caractérisé en ce que
les données du premier flux partiel de données (40) sont soumises à une modulation DQPSK.

4. Procédé pour augmenter le débit de données transmises par radiodiffusion selon la revendication 1 à 3,
caractérisé en ce que
le deuxième flux partiel de données (41) contient des informations en supplément du premier flux partiel de données (40).

5. Procédé pour augmenter le débit de données transmises par radiodiffusion selon la revendication 1 à 4,
caractérisé en ce que
les données numériques contiennent des images de télévision et des données pour l'image de base sont transmises dans le premier flux partiel de données (40) et des données pour une image standard sont transmises dans le deuxième flux partiel de données (41).

6. Emetteur destiné à augmenter le débit de données transmises par radiodiffusion, dans lequel l'émetteur présente, pour le traitement des données audio (2), vidéo (1) et autres (3, 4), des encodeurs (5, 8, 9, 10), un multiplexeur (12) ainsi qu'un premier modulateur (13), avec un premier encodeur (5) produisant un premier et un deuxième flux partiels de données, un deuxième modulateur (14) pour le deuxième flux partiel de données (41) et un combinateur (15) pour le premier et le deuxième flux partiel de données,
caractérisé en ce que
pour les deux flux partiels de données (6, 7), tout d'abord un encodeur DVB (8) et ensuite un encodeur DAB (9) sont présents pour le codage, l'émetteur étant configuré de manière qu'il forme un cadre de transmission DAB.

7. Emetteur destiné à augmenter le débit de données transmises par radiodiffusion selon la revendication 6,
caractérisé en ce que
le deuxième modulateur est un modulateur d'amplitude ou un modulateur d'amplitude en quadrature ou un Phase Shift Keying Modulator.

8. Récepteur destiné à recevoir des données numériques par radiodiffusion, dans lequel le récepteur présente un convertisseur A/N (18), un composant de synchronisation (19), un FFT (20), un premier démodulateur (21), ainsi que des multiplexeurs (22), des décodeurs (25, 24, 26, 27, 28) munis de connexions qui aboutissent aux drains de données correspondants (29, 30, 31, 32, 33), dans lequel, en aval du premier démodulateur (21) une branche dérivée pour un deuxième flux partiel de données (41) est présente dans un deuxième démodulateur (23),

et dans lequel un décodeur (26) réunit les flux partiels de données,
caractérisé en ce que
pour les deux flux partiels de données, sont prévus un décodeur DAB et un décodeur DVB (24, 25), les flux partiels de données traversant tout d'abord le décodeur DAB puis le décodeur DVB (24, 25).

9. Récepteur de données numériques par radiodiffusion selon la revendication 8,
caractérisé en ce que
le deuxième démodulateur (23) est un démodulateur d'amplitude ou un démodulateur d'amplitude en quadrature ou un Phase Shift Keying Demodulator.

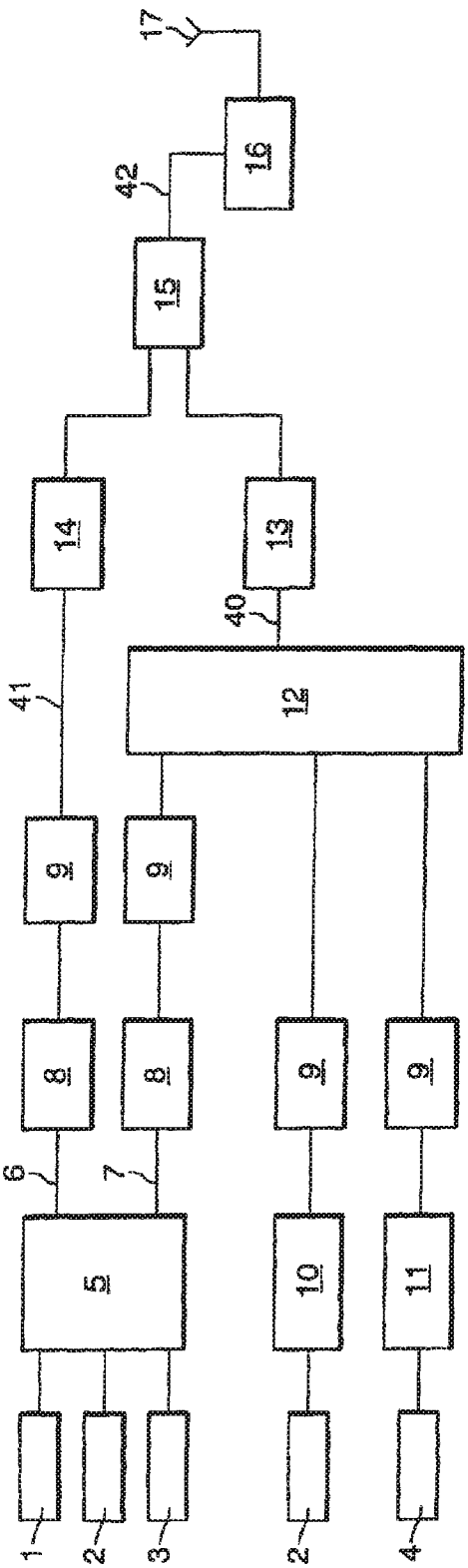


Fig. 1

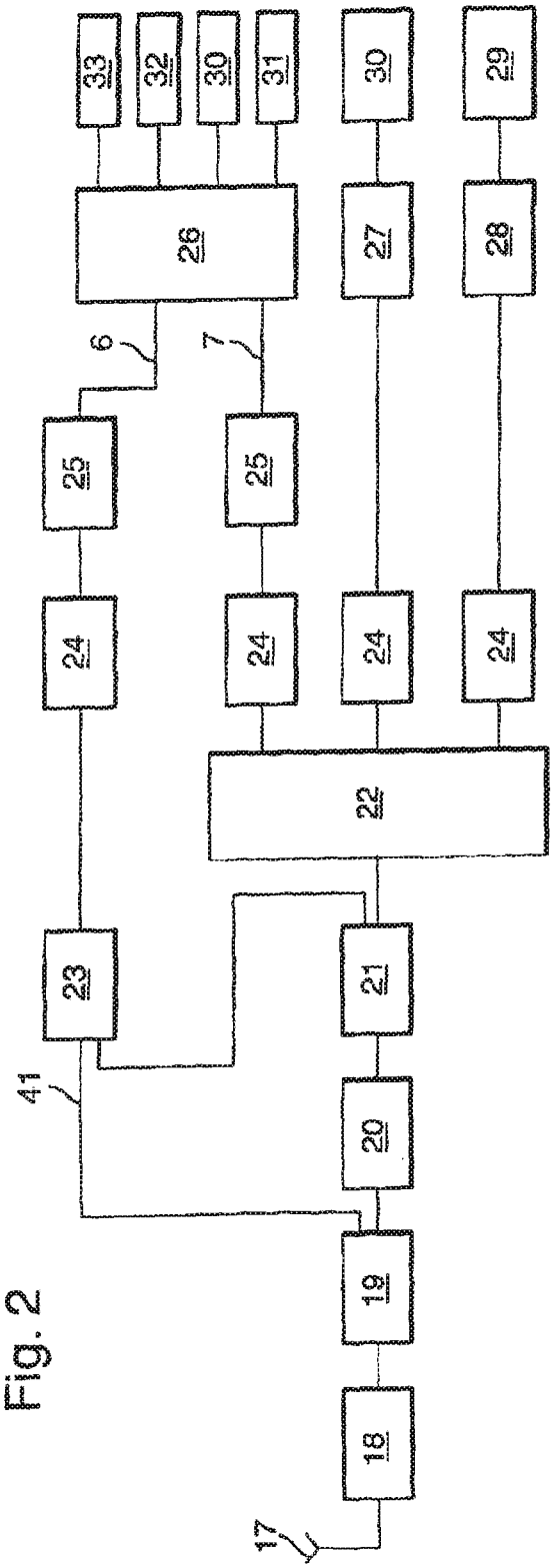


Fig. 2

Fig. 3a

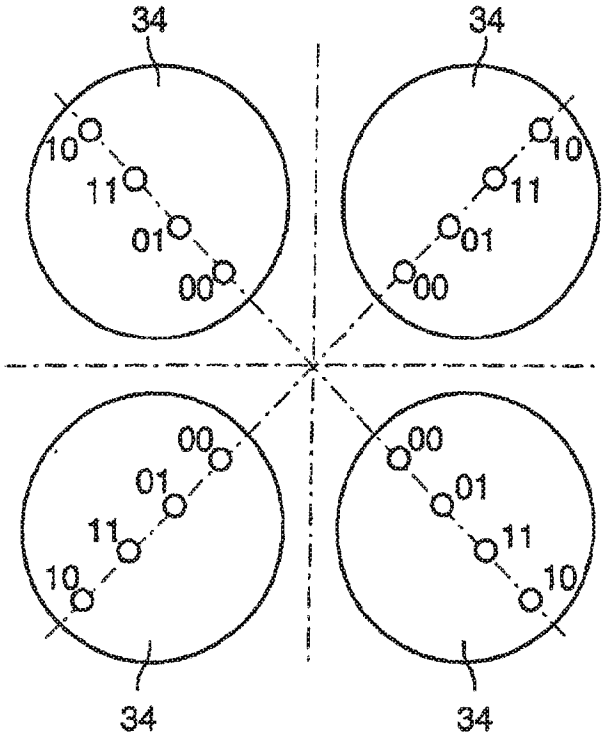


Fig. 3b

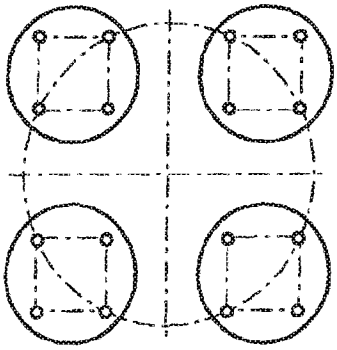
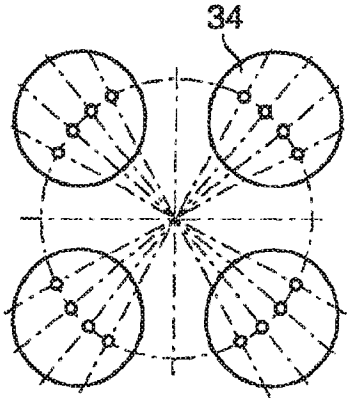


Fig. 3c



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⑭デイジタルデータ記録方法

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明　　細　　書

1、発明の名称

ディジタルデータ記録方法

2、特許請求の範囲

第一のディジタルデータを第一の変調方法により記録した後、第一のディジタルデータを復調し、該ディジタルデータを基準に第二のディジタルデータを第一のディジタルデータに続いて、第二の変調方法により記録し、第一の変調方法による変調信号のレベル反転間隔を第二の変調方法による変調信号に現われるレベル反転間隔の中に存在するものとすることを特徴とするディジタルデータ記録方法。

3、発明の詳細な説明

産業上の利用分野

本発明はディジタルデータを記録媒体に記録再生するに際してのディジタルデータの記録方法に関するものである。

従来例の構成とその問題点

近年、磁気ディスク装置によるディジタルデータの記録が計算機との整合性が良く広く使用されている。特に大容量のディジタルデータ記録再生が可能なものとして光メモリディスクがある。

この光ディスク装置において、ディジタルデータの読み出しに際して、光ディスク上に書かれたアドレスを検出し、このアドレスに続くディジタルデータを読み出すという検索を行なっている。また、ディジタルデータの書込みに際しては、既に書込まれているアドレスを検出し、このアドレスに続く空白部にディジタルデータを書込むことが行なわれている。アドレスデータ及びディジタルデータは記録に際して変調、例えばＦＭ，MFM，４－５変換，３ＰＭ変調等の変調を受けて記録される。第１図(ア)，(イ)にディジタルデータの記録される前の状態Ａと、記録された後Ｂの状態を示す。さらに第２図に再生側の構成を示す。従来、アドレス部１の記録の変調方式としては変復調アルゴリズムが簡易なもの、及び可変速再生の簡易なもの、例えばＦＭ変調が用いられ、データ部２の記録の変調方式としては高密度記録可能なもの、例

えば4－5変換、3PM変調等が用いられている。アドレス部1とデータ部2の変調方法が異なるので、復調回路6，7はそれぞれに対応したものが必要となる。また復調に際してのクロック再生が必要であるが、アドレス部1のクロック周波数とデータ部2の周波数が異なっているために、クロック再生回路4，5もまたそれぞれ異なるものが必要となる。また、クロック再生回路4，5に位相制御発振回路（以下PLL回路と呼ぶ）を用いた場合、アドレス部1ではデータ部2のクロック再生回路のクロックが、データ部2ではアドレス部1のクロック再生回路のクロックが所定の周波数よりずれるので、アドレス部1でのアドレス部クロック再生回路4のPLL回路の引き込み、データ部2でのデータ部クロック再生回路5のPLL回路の引き込みに時間がかかり、アドレス，データの前部に引き込みに必要にアンプル部を長くとる必要があるという問題点を有していた。

発明の目的

本発明は上記従来の問題点を解消するもので、アドレス部とデータ部のクロック周波数が同一になるようにし、アドレス部，データ部のクロック再生回路を一つにし、クロック再生回路にPLL回路を用いた場合に引き込み時間を短くし、アンプル部の期間を短くするディジタルデータの記録再生方法を提供することを目的とする。

発明の構成

本発明はアドレス部にアドレスを記録するに用いる第一の変調方法による変調信号のレベル反転間隔をデータ部にデータを記録するに用いる第二の変調方法による変調信号に現われるレベル反転間隔より選択したものとすることにより、アドレス部とデータ部のクロック周波数を同一にし、クロック再生回路を一つとし、クロック再生時の引き込み時間を短くすることを目的とする。

実施例の説明

本発明の一実施例として、アドレス部の変調方法としてFM変調，データ部の変調方法として4－5変換変調を用いた場合を示す。FM変調は、データが"1"のときデータのビットセルの中央でレベル反転，データが"0"のときはレベル反転なし、データのビットセルの境界は常にレベル反転する変調方法であり、第3図にその例を示す。4－5変換変調は、データを4ビット単位に分割し，該4ビットのデータ語に対して第4図に示す変換テーブルに従って5ビットの符号語に変換し該符号語のビット"1"のビットセルの中央でレベル反転させる変調方法であり、第5図にその例を示す。FM変調のレベル反転間隔はT_1とT_2の2種類のみであり、4－5変換変調ではT_3，T_4，T_5の3種類である。T_1とT_2の関係は

$$T_2 = 2T_1 \quad \cdots\cdots\cdots\cdots(1)$$

であり、T_3，T_4，T_5の関係は

$$\left.\begin{aligned} T_5 &= 3T_3 \\ T_4 &= 2T_1 \end{aligned}\right\} \quad \cdots\cdots\cdots\cdots(2)$$

である。以上の関係から、T_1をT_3と等しくし、T_4をT_2と等しくすることにより、FM変調のレベル反転間隔は、4－5変換変調のレベル反転間隔に存在するものとなる。その結果、各変調信号に対する再生クロック信号を第6図に示すように同一とすることができる。

次に第7図により再生クロック信号を用いたFM変調信号の復調について説明する。得られた再生クロック信号Dより検出窓Fを作る。この検出窓Fのハイレベル内にあるFM信号Cのエッヂパルスを抜き取りパルスGを得る。パルスGをDフリップフロップのクロック入力に入力し、データ入力に検出窓Fを入力し、エッヂパルスEの検出窓Fのローレベル内にあるパルスをリセット入力に入力することにより、データが"1"を示す信号Hを得る。この信号Hを検出窓Fの立下り時にDフリップフロップに読み込むようにすることにより再生データIが得られることになる。

再生クロック信号を用いた4－5変換変調信号の復調を以下に示す。得られた再生クロックDを用いて4－5変換変調信号を1クロック分遅延させた信号Kを作り、JとKとを排他的論理和をとることにより再生符号語データ系列Lを得る。この再生符号語データ系列を再生クロックDにより5ビットシフトレジスタに入力し、この5ビット

ごとに変換テーブルに従って４ビットのデータ語に変換すれば、もとのデータが得られる。

以上のように４－５変換変調のレベル反転間隔の内２種類を用いたＦＭ変調とすることにより、アドレス部の再生クロックとデータ部の再生クロックとが同一となるので、クロック再生回路を一つにすることができ、アドレス部でクロックが引き込まれておればアドレス部とデータ部の境界で若干のクロックの乱れがあるが、クロック周波数は大きくはずれないので次のデータ部のクロック引き込みが容易となる。それゆえデータ部の前のクロック引き込みのアンプル期間を短くすることができるので、データ部の有効データ量を多く確保することができる。

以上は、第一の変調をＦＭ変調とし、第二の変調を４－５変換変調としたものであるが、その他の変調方法でも同様に考えることができる。例えば第一の変調をＭＦＭ変調で、第二の変調がＳＰＭ変調の場合を次に説明する。ＳＰＭ変調の場合、レベル反転間隔は、データのビット周期をＴとすれば、１.５Ｔ，２Ｔ，２.５Ｔ，３Ｔ，３.５Ｔ，４Ｔ，４.５Ｔ，５Ｔ，５.５Ｔ，６Ｔの１０種類がある。ＭＦＭ変調では最短のレベル反転間隔をT_Mとすれば、T_M，$1.5T_M$，$2T_M$の３種類である。T_Mを２Ｔとすることにより、$1.5T_M$は３Ｔ，$2T_M$は４Ｔとなり、ＳＰＭ変調のレベル反転間隔を用いて変調信号を構成することができる。それゆえ、第一の実施例で述べたように再生クロックが同一となり、同様の効果が得られる。

発明の効果

本発明のディジタルデータ記録再生方法は、第一の変調方法による変調信号のレベル反転間隔を第二の変調方法による変調信号に現われるレベル反転間隔の中より選択したものとすることにより、第一の変調方法による記録及び第二の変調方法による記録が共に存在する記録再生装置において、クロック再生回路を第一の変調の復調回路、第二の変調の復調回路とで共用することができ、第一の変調から第二の変調へ変化する部分において、再生クロックの乱れを最小限にすることができ、第二の変調の記録部分の前部に存在するアンプル部分を短くすることができ、第二の変調の記録部の有効データ量を多く確保することができる。

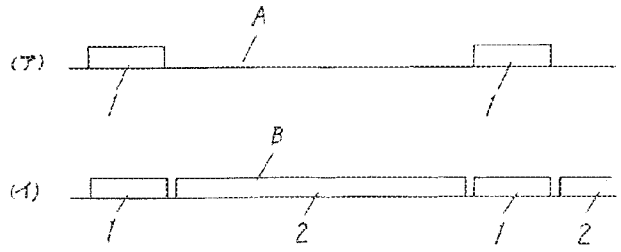
４．図面の簡単な説明

第１図は従来の光ディスクディジタル記録再生装置の記録信号構成を示す図、第２図は前記装置の再生側のブロック図、第３図は本発明の第一の実施例で用いるＦＭ変調を説明する波形図、第４図は第一の実施例で用いる４－５変換変調の対応関係を説明する図、第５図は４－５変換の波形図、第６図は本発明を実施した場合の波形図、第７図はＦＭ変調の復調を説明するための波形図、第８図は４－５変換変調の復調を説明するための波形図である。

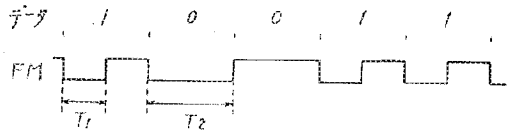
Ｄ……再生クロック信号、Ｆ……検出窓、Ｅ……パルス、Ｈ……“１”を示す信号、Ｉ……再生データ。

代理人の氏名　弁理士　中　尾　敏　男　ほか１名

第 1 図



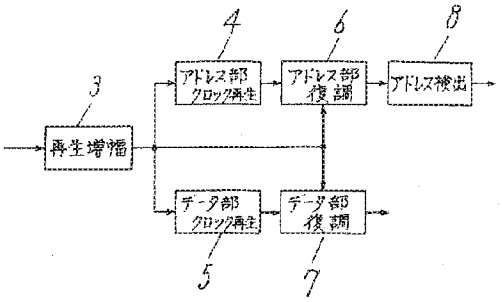
第 3 図



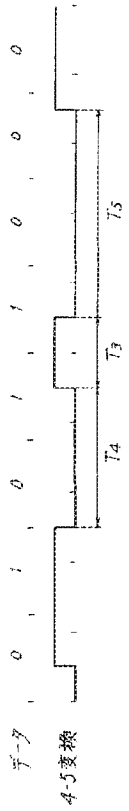
第 4 図

データ語	符号語
0 0 0 0	1 1 0 0 1
0 0 0 1	1 1 0 1 1
0 0 1 0	1 0 0 1 0
0 0 1 1	1 0 0 1 1
0 1 0 0	1 1 1 0 1
0 1 0 1	1 0 1 0 1
0 1 1 0	1 0 1 1 0
0 1 1 1	1 0 1 1 1
1 0 0 0	1 0 0 1 0
1 0 0 1	0 1 0 0 1
1 0 1 0	0 1 0 1 0
1 0 1 1	0 1 0 1 1
1 1 0 0	1 1 1 1 0
1 1 0 1	0 1 1 0 1
1 1 1 0	0 1 1 1 0
1 1 1 1	0 1 1 1 1

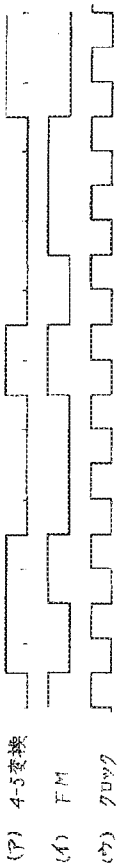
第 2 図



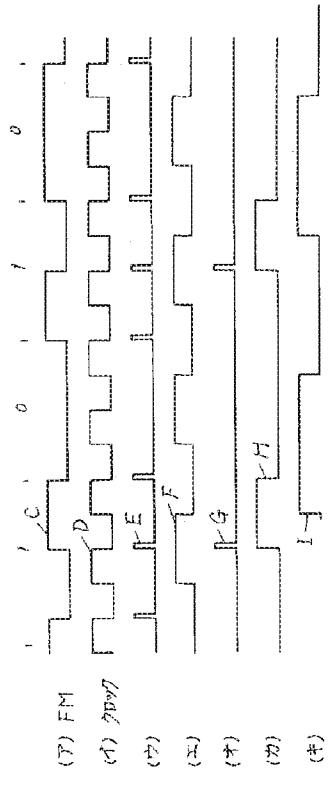
第 5 図



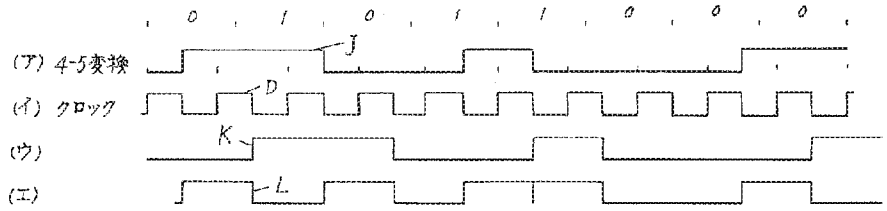
第 6 図



第 7 図



第 8 図



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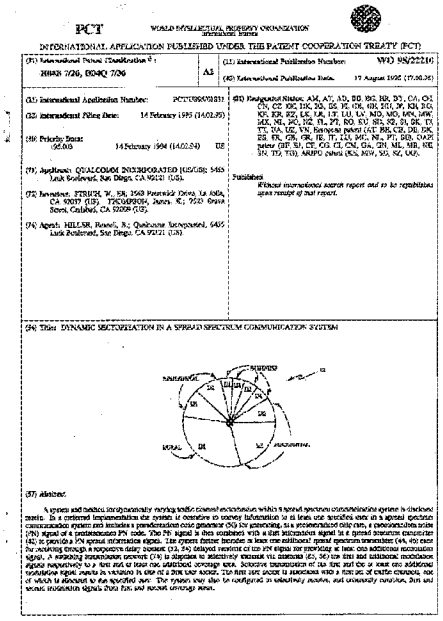
(54) Title: DYNAMIC SECTORIZATION IN A SPREAD SPECTRUM COMMUNICATION SYSTEM.

Un sistema para transportar informaci¢n a por lo menos un usuario en un sistema de comunicaci¢n de espectro disperso, que comprende: un medio para generar, a una velocidad de chip predeterminada, una primera se¤al de ruido pseudoaleatorio (PN) de un primer c¢digo PN predeterminado; un primer medio para combinar la primera se¤al Pn y una primera se¤al de informaci¢n y para proporcionar una primera se¤al de modulaci¢n resultante; un medio para proporcionar una segunda se¤al de modulaci¢n haciendo retardar la primera se¤al de modulaci¢n en un primer retardo predeterminado que se relaciona inversamente a la velocidad de chip; un medio para transmitir selectivamente la primer y la segunda se¤ales de modulaci¢n respectivamente a la primera y la segunda reas de cobertura; mediante lo cual la transmisi¢n selectiva de la primera y la segunda se¤ales de modulaci¢n da por resultado la variaci¢n en tama¤o de un primer sector de usuario en donde se incluye el por lo menos un usuario.



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(54) Title: DYNAMIC SECTORIZATION IN A SPREAD SPECTRUM COMMUNICATION SYSTEM

(57) Abstract

A system and method for dynamically varying traffic channel sectorization within a spread spectrum communication system is disclosed herein. In a preferred implementation the system is operative to convey information to at least one specified user in a spread spectrum communication system and includes a pseudorandom code generator (50) for generating, at a predetermined chip rate, a pseudorandom noise (PN) signal of a predetermined PN code. The PN signal is then combined with a first information signal in a spread spectrum transmitter (42) to provide a PN spread information signal. The system further includes at least one additional spread spectrum transmitter (44, 46) each for receiving through a respective delay element (52, 54) delayed versions of the PN signal for providing at least one additional modulation signal. A switching transmission network (74) is disposed to selectively transmit via antennas (85, 86) the first and additional modulation signals respectively to a first and at least one additional coverage area. Selective transmission of the first and the at least one additional modulation signal results in variation in size of a first user sector. The first user sector is associated with a first set of traffic channels, one of which is allocated to the specified user. The system may also be configured to selectively receive, and coherently combine, first and second modulation signals from first and second coverage areas.

A system and method for dynamically varying traffic channel sectorization within a spread spectrum communication system is disclosed herein. In a preferred implementation the system is operative to convey information to at least one specified user in a spread spectrum communication system and includes a pseudorandom code generator (50) for generating, at a predetermined chip rate, a pseudorandom noise (PN) signal of a predetermined PN code. The PN signal is then combined with a first information signal in a spread spectrum transmitter (42) to provide a PN spread information signal. The system further includes at least one additional spread spectrum transmitter (44, 46) each for receiving through a respective delay element (52, 54) delayed versions of the PN signal for providing at least one additional modulation signal. A switching transmission network (74) is disposed to selectively transmit via antennas (85, 86) the first and additional modulation signals respectively to a first and at least one additional coverage area. Selective transmission of the first and the at least one additional modulation signal results in variation in size of a first user sector. The first user sector is associated with a first set of traffic channels, one of which is allocated to the specified user. The system may also be configured to selectively receive, and coherently combine, first and second modulation signals from first and second coverage areas.

SECTORIZACIÓN DINAMICA EN UN SISTEMA DE COMUNICACIÓN DE ESPECTRO DE DISPERSIÓN

Antecedentes de la Invención

I. Campo de la Invención

La presente invención se relaciona con sistemas de comunicación que utilizan señales de espectro disperso, y en forma más particular se relaciona con un método y un aparato novedosos para la sectorización dinámica de canal dentro de un sistema de comunicación de espectro disperso.

II. Descripción de la Técnica Relacionada

Se han desarrollado sistemas de comunicación que permiten la transmisión de señales de información a partir de una ubicación fuente hacia un destino de usuario físicamente distinto. Los dos métodos, analógico y digital, se han utilizado para transmitir estas señales de información sobre canales de comunicación que se eslabonan con la fuente y las ubicaciones de usuario. Los métodos digitales tienden a proporcionar varias ventajas con relación a las técnicas analógicas, entre ellas se incluyen, por ejemplo, la inmunidad mejorada al ruido e interferencia de canal, la capacidad aumentada, y la mejor seguridad de las comunicaciones a través del uso del cifrado.

Al transmitir una señal de información desde una ubicación fuente sobre un canal de comunicación, la señal de información se convierte primero en una forma adecuada para la eficiente transmisión sobre el canal. La conversión, o modulación, de la señal de información involucra variar un parámetro de una onda portadora con base en la señal de información, de tal forma que el espectro de la portadora modulada resultante queda confinado dentro de la anchura de banda del canal. En la ubicación del usuario la señal de mensaje original se replica de una versión de la portadora modulada recibida subsecuentemente para la propagación sobre el canal. Esta replicación en general se logra utilizando un inverso del proceso de modulación empleado por el transmisor fuente.

La modulación facilita también el multiplexado, es decir, la transmisión simultánea de varias señales sobre un canal común. Los sistemas de comunicación multiplexados en general incluirán una pluralidad de unidades de suscriptor remotas que requieren del servicio intermitente de una duración relativamente corta en lugar del acceso continuo hacia el canal de comunicación. Los sistemas diseñados para permitir la comunicación en breves períodos de tiempo con un juego de unidades de suscriptor, se han denominado: sistemas de comunicación de acceso múltiple.

Un tipo particular de sistemas de comunicación de

acceso múltiple es el conocido como sistema de espectro disperso. En los sistemas de espectro disperso la técnica de modulación utilizada da por resultado una dispersión de la señal transmitida sobre una banda de frecuencia amplia dentro del canal de comunicación. Un tipo de sistema de espectro disperso de acceso múltiple es un sistema de modulación de acceso múltiple por división de código (CDMA). Otras técnicas de sistema de comunicación de acceso múltiple como por ejemplo los esquemas de acceso múltiple por división de tiempo (TDMA), acceso múltiple por división de frecuencia (FDMA) y modulación AM, tales como los esquemas de banda lateral simple de amplitud compuesta, ya se conocen en la técnica. Sin embargo, la técnica de modulación de espectro disperso de CDMA tiene ventajas considerables sobre estas técnicas de modulación para los sistemas de comunicación de acceso múltiple. El uso de las técnicas CDMA en un sistema de comunicación de acceso múltiple se revela en la Patente de los Estados Unidos No 4,901,307, otorgada el 13 de febrero de 1990 y titulada *"Spread Spectrum Multiple Access Communication System Using Satellite or Terrestrial Repeaters"*, cedida a la cesionaria de esta invención.

En la Patente de los Estados Unidos No. 4,901,307 antes mencionada, se revela una técnica de acceso múltiple en donde un gran número de usuarios del sistema móvil,

tienen cada uno un transceptor que se comunica a través de repetidores vía satélite o de estaciones base terrestres utilizando señales de comunicación de espectro disperso CDMA. Al utilizar comunicaciones CDMA, el espectro de frecuencia puede reutilizarse varias veces permitiendo así un aumento en la capacidad de usuario del sistema. El uso del CDMA da por resultado una eficiencia espectral mucho mayor que aquella lograda utilizando otras técnicas de acceso múltiple.

En particular, la comunicación de los sistemas CDMA entre una estación base y las unidades de suscriptor dentro de la región celular circundante se logra mediante la dispersión de cada señal transmitida sobre la anchura de banda de canal disponible utilizando un código de dispersión usuario único. En estos sistemas CDMA, las secuencias de código utilizadas para dispersar el espectro se construyen a partir de dos tipos diferentes de secuencias, cada una con diferentes propiedades para proporcionar diferentes funciones. Existe un código externo que se comparte por todas las señales en una célula o sector que se utiliza para discriminar entre señales de trayectoria múltiple. Además, al ajustar la fase del código externo permite que ésta se utilice para discriminar entre juegos de usuarios agrupados en "sectores" dentro de una célula dada. Por ejemplo, los usuarios dentro de una

célula dada pueden dividirse en tres sectores disponiendo tres fases del código externo. También existe un código interno que se utiliza para discriminar entre señales de usuario transmitidas sobre una pluralidad de "canales de tráfico" asociados con cada sector usuario. Las señales transmitidas específicas se extraen de los canales de comunicación mediante la desdispersión de la energía de señal compuesta en el canal de comunicación con el código interno asociado con la señal transmitida que va a extraerse.

Haciendo referencia a la Figura 1A, se muestra una primera célula 10 ejemplaria en la que están dispuestas una pluralidad de unidades de suscriptor 12 y una estación base 14. Como se indica en la Figura 1A, la célula 10 está dividida en seis áreas de cobertura C1-C6. La estación base 14 puede incluir un juego de seis antenas de haz fijo (no mostradas) dedicadas a facilitar la comunicación con las unidades de suscriptor en las áreas de cobertura C1-C6, respectivamente. Las unidades de suscriptor 12 se agrupan en una pluralidad de sectores de usuario, cada uno de los cuales soporta un número equivalente de canales de tráfico. Como se indica por la Figura 1A, un primer sector de usuario residencial abarca las áreas de cobertura C1 y C6, mientras que un segundo sector de usuario residencial expande el área de cobertura C4. En forma similar, el

sector de usuario que incluye las áreas principalmente rurales está asociado con las áreas de cobertura C2 y C3, mientras que los usuarios comerciales se concentran dentro del área de cobertura C5.

Como se indica en la Figura 1A, es necesario que ciertos sectores de usuarios sean relativamente angostos con objeto de ajustarse a las demandas durante los períodos pico de la utilización del sistema. Por ejemplo, la región neutral relativamente angosta del sector de usuarios comerciales es necesaria debido a la alta concentración de usuarios comerciales dentro del área de cobertura C5 que desean comunicarse durante horas de trabajo, es decir entre las 8 a.m. y las 5 p.m. Esto es, si el alcance del sector de los usuarios comerciales se expandiera para incluir otras regiones diferentes al área de cobertura C5, sería posible que un número insuficiente de los canales de tráficos estuvieran disponibles durante las horas comerciales para ajustarse a todos aquellos que desean hacer llamadas. En contraste, la concentración difusa de las unidades de suscriptor 12 entre las áreas rurales permite que los canales de tráfico asociados con el sector del usuario rural sean asignados entre usuarios distribuidos en dos áreas de cobertura C2-C3.

Desafortunadamente, durante las horas inhábiles, un número de canales de tráfico dedicados al sector de los

usuarios comerciales muy probablemente quedaría sin utilizarse, ya que en esos momentos existen considerablemente menos interesados comerciales en hacer llamadas y un número correspondientemente mayor de personas que desean hacer llamadas residenciales. Consecuentemente, sería deseable poder proporcionar una alta concentración de canales de tráfico a los usuarios comerciales dentro del área de cobertura CS durante las horas hábiles y proporcionar una concentración relativamente menor de canal de tráfico durante las horas inhábiles.

Aunque existen arreglos de antena capaces de conformar de manera adaptable un haz proyectado en respuesta al cambio de la demanda del usuario, la implementación de este tipo de arreglos de antena dentro del sistema de la Figura 1A requeriría de una modificación correspondiente en la arquitectura del haz fijo de la estación base 14. Además, la circuitería relativamente sofisticada de RF/microondas que se emplea típicamente en las redes formadoras de haz adaptable dan por resultado un costo y complejidad mayores en el sistema. En consecuencia, es el objeto de la presente invención el proporcionar una técnica redituable para variar la concentración de los canales de tráfico en respuesta a los cambios en la distribución de usuarios dentro de un sistema de comunicación celular de espectro disperso.

En el ejemplo específico de un sistema de comunicación CDMA, cada sector de usuario es capaz de soportar un nivel dado de demanda de tráfico. En consecuencia, es un objeto adicional de la invención el diseñar el tamaño de los sectores de usuarios específicos dentro de una comunicación CDMA a la demanda de los canales de tráfico dentro del sector. Esta asignación de canal de tráfico eficiente permitiría la utilización óptima de las fuentes de sistemas de comunicación, disminuyendo así el costo por usuario.

Además de dirigirse a la necesidad de la asignación de canales de tráfico flexibles como consecuencia de los cambios a corto término en la demanda de usuario que se describe antes, también es un objeto de la invención el ajustarse a cambios a largo término en la demanda de los usuarios. Estas variaciones a largo término en la demanda podrían surgir, por ejemplo, de desplazamientos en la distribución de la población y de los patrones de construcción dentro de un área geográfica dada.

Una ventaja adicional de los sistemas de haz fijo convencionales, como por ejemplo el sistema de la figura 1A, es que los estimados relativamente precisos de las demandas de los usuarios deberán típicamente estar disponibles antes de la instalación del sistema. Es decir, los diseñadores del sistema generalmente deben contar con

la información detallada que se relaciona con los patrones de demanda esperados con objeto de configurar la estación base de haz fijo para proporcionar la capacidad de canal de tráfico requerida para cada sector de usuarios. Los cambios en los patrones de uso que ocurran en forma próxima al período de instalación tienden por lo tanto a evitar la utilización óptima de los canales de tráfico disponibles. Por lo tanto es todavía otro objeto de la presente invención el proporcionar un sistema de comunicación capaz de ser diseñado, durante la instalación, de acuerdo con los patrones existentes de la demanda de canales de tráfico.

SUMARIO DE LA INVENCIÓN

La invención proporciona un sistema y un método para variar en forma dinámica la sectorización de los canales de tráfico dentro de un sistema de comunicación de espectro de dispersión.

En una modalidad preferida, el sistema de la invención funciona para transportar información hacia por lo menos un usuario específico en un sistema de comunicación de espectro disperso. El sistema incluye una primer red para generar, a una velocidad de chip predeterminada, una primera señal de ruido pseudoaleatorio (PN) de un primer código PN predeterminado. La primera señal PN se combina entonces con una primera señal de

información con objeto de proporcionar una primara señal de modulación resultante. El sistema incluye además una segunda red para proporcionar una segunda señal de modulación retardando la primera señal de modulación en un retardo predeterminado, inversamente relacionado con la velocidad de chip PN. Una red de transmisión de conmutación está colocada para transmitir selectivamente la primera y segunda señales de modulación respectivamente la primera y segunda áreas de cobertura. En esta forma puede utilizarse la transmisión selectiva de la primera y segunda señales de modulación para variar el tamaño del primer sector de usuario durante diferentes períodos de operación del sistema. El primer sector de usuario se asocia con un primer juego de canales de tráfico, uno de los cuales se asigna al usuario específico.

BREVE DESCRIPCIÓN DE LOS DIBUJOS

Los objetos y particularidades adicionales de la invención se podrán comprender con mayor facilidad a partir de la siguiente descripción detallada y de las reivindicaciones anexas, cuando se tomen con relación a los dibujos que se acompañan en donde:

La Figura 1A muestra una célula ejemplo, incluida dentro de un sistema de comunicación celular, en donde se colocan una pluralidad de unidades de suscriptor y una

estación base.

La Figura 1B muestra una segunda célula ejemplo en la forma sectorizada de acuerdo a la invención durante horas hábiles típicas.

La Figura 1C ilustra la segunda célula ejemplo tal como se sectoriza durante horas nocturnas de acuerdo a la invención.

La Figura 1D muestra un diagrama de bloques que representa un transceptor de comunicaciones de estación base ejemplario, en donde el sistema de sectorización dinámica de la invención está incorporado.

La Figura 2 proporciona una representación en diagrama de bloques de una red del transmisor de estación base configurada para proporcionar la sectorización dinámica de usuarios de acuerdo a la invención.

La Figura 3 ilustra una matriz de conmutador, colocada dentro del transmisor de estación base, para proporcionar una conexión conmutable entre la señal de información asociada con cada sector de usuario y un juego de seis manipuladores de antena.

La Figura 4 ilustra un diagrama de bloques de una red del transmisor de estación base capaz de proporcionar la sectorización dinámica de usuarios incrementada, utilizando tanto haces de antena polarizados horizontal y verticalmente.

Las Figuras 5A y 5B proporcionan respectivamente vista superior y lateral de la antena provisional resonante de modo dual incorporada dentro de una implementación requerida de las antenas de estación base.

La Figura 6 muestra una representación en diagrama de bloques de una red receptora de estación base configurada para configurar la sectorización dinámica de usuarios de acuerdo con la invención.

La Figura 7 proporciona una representación en diagrama de bloques de un transmisor de espectro disperso ejemplario.

La Figura 8 ilustra una red de generación piloto para proporcionar las secuencias piloto de canal I y Q.

La Figura 9 muestra una implementación ejemplo de un transmisor de estación base RF.

La Figura 10 es un diagrama de bloques de un receptor de diversidad ejemplo colocado dentro de una unidad de suscriptor.

La Figura 11A representa en forma ilustrativa el patrón de azimuth de un haz fijo de 40 grados, que se asume va a proyectarse por una primera antena de estación base asociada con una de las áreas de cobertura C1-C6 (Figura 1A).

La Figura 11B representa en forma ilustrativa el patrón de azimuth producido cuando par adyacente de antenas

de estación base de haz fijo son manipulados en fase.

La Figura 12 muestra una representación en diagrama de bloques de una red de transmisor de estación base configurada para proporcionar la sectorización dinámica de los usuarios al proyectar un juego de haces en faz a cada sector de usuario.

La Figura 13 ilustra una configuración de estación base alterna para proporcionar la sectorización dinámica de los usuarios al proyectar un juego de haces en fase.

La Figura 14 muestra un arreglo triangular de los paneles de antena del arreglo de primera, segunda y tercera fase, que operan colectivamente para proporcionar un juego de nueve haces de antena.

La Figura 15 ilustra una implementación preferida de los paneles de antena de la Figura 14, cada uno de los cuales incluye un arreglo 4x4 de elementos provisionales.

La figura 16 es un diagrama de bloques de una red formadora de haz que se utiliza para manipular un panel de antena de arreglo en fase.

Descripción de la Modalidad Preferida

I. Introducción

Volviendo ahora a la figura 1B, se muestra una segunda célula 18 ejemplo, sectorizada de acuerdo con la

invención, durante horas hábiles normales. Como se indica en la Figura 1B, la segunda célula 18 está sectorizada en un juego de nueve sectores de usuario U1-U9. La segunda célula 18 está dividida durante las horas hábiles de manera que un juego de cuatro sectores U1-U4, cada uno expandiéndose en un ángulo de, por ejemplo, 20 grados, se asignan a un centro de alta densidad de población. Durante las horas hábiles las áreas rurales y residenciales menos pobladas de la celda reciben servicio mediante un juego de sectores de usuario relativamente amplio U5 y U6-U9, respectivamente. En una modalidad ejemplo la anchura angular del sector de usuario rural U5 es un juego de 100 grados, los sectores usuario residenciales U6, U8 y U9 son cada uno de 40 grados, y el sector usuario residencial U7 es de 60 grados. El respiro angosto de los sectores de usuario U1-U4 se necesitan por la alta concentración de usuarios dentro del centro comercial que desean comunicarse durante horas hábiles. En esta forma el alcance confinado de los sectores de usuario U1-U4 asegura que un número suficiente de los canales de tráfico estén disponibles durante horas hábiles para ajustarse a un número deseado de usuarios que están en el centro comercial.

La Figura 1C ilustra la segunda célula 18 ejemplo sectorizada durante la noche (es decir las horas no hábiles) en una pluralidad de nueve sectores de usuario

U1'-U9' de acuerdo con la invención. Como se indica en la Figura 1C, durante las horas inhábiles un solo sector de usuario U1' de 80 grados, en lugar de cuatro sectores U1-U4 de 20 grados se requieren durante las horas hábiles, y se emplean para dar servicio a las demandas dentro del centro comercial. En forma similar, el desplazamiento de población hacia las áreas residenciales durante las horas de la tarde y noche requieren la sectorización aumentada proporcionada por siete sectores de usuario U2'-U6', y U7'-U9', en relación a los cuatro sectores U6-U9 que se requieren durante el día. En la modalidad ejemplo, la anchura angular de los sectores de usuario residencial U2'-U4' y U8'-U9', se ajusta a 20 grados, y la anchura de los sectores de usuario residencial U6' y U7' se ajusta a 40 grados. Los sectores de usuario rural U5' permanecen en 100 grados durante tanto las horas del día como de la noche como consecuencia de la variación temporal mínima típica en la demanda de los usuarios en las regiones rurales. El cambio en la sectorización ilustrado por las Figuras 1B-1C puede lograrse utilizando el sistema de sectorización dinámica de la invención, la operación del cual se describe a continuación con relación al diagrama de bloques de la Figura 1D.

La Figura 1D muestra una representación en diagrama de bloques de un transceptor de comunicaciones 25

de estación base ejemplo, en donde el sistema de sectorización dinámico de la invención está incorporado. Como se discute abajo, el transceptor 25 funciona para proporcionar servicio mejorado a los usuarios colocados dentro de una primera célula de un sistema de comunicación celular al variar dinámicamente la asignación de los canales de tráfico entre varios sectores de usuario dentro de la célula. El transceptor 25 se observa que incluye un controlador 27, un sistema de antena 29 y bancos de canal de transmisión/recepción 31. El controlador 27 se programa típicamente para proporcionar bancos 31 de ajuste de canal/asignación de transmisión/canal de recepción. Los bancos de canal de transmisión/recepción 31 se acoplan electromagnéticamente al sistema de antena 29 mediante una línea 32 de transmisión de onda guía 32 o semejante. Cada banco de canal individual puede comprender, por ejemplo, una pluralidad de unidades de canal capaces de facilitar la comunicación con un usuario particular. En la modalidad de la Figura 1D, los bancos de canal de transmisión/recepción 31 suministran señales formadoras de haz al sistema de antena 29 a fin de sectorizar la primer célula en una pluralidad de sectores de usuario, cada uno de los cuales tiene asociado con el mismo una pluralidad de canales de tráfico de usuario. Las señales de información se relevan entre los bancos de canal 31 y una red de comunicaciones

externo, por ejemplo una red de teléfono público conmutada (PSTN) sobre un bus de datos 33.

Una primera modalidad preferida de la invención, un número fijo de los canales de tráfico está asociado con cada uno de los sectores de usuario. Bajo esta restricción, la presente invención contempla la variación de ajuste en la demanda de usuarios dentro de las diversas regiones de la célula, ajustando el tamaño relativo de cada sector de usuario. Por ejemplo, podrían emplearse un número de sectores de usuario relativamente angostos para dar servicio a los usuarios que están dentro de un área particular de la célula durante períodos de alta demanda del usuario. Esto aumenta al máximo la probabilidad de que un canal de tráfico esté disponible a todos aquellos que deseen establecer comunicación durante esos períodos de demanda superior. Inversamente, durante los períodos de mínima demanda podría utilizarse un número relativamente menor de sectores de usuario de anchura más amplia para proporcionar la capacidad requerida en el canal de tráfico. Esta ampliación de los sectores de usuario asociado con un área celular particular durante períodos de demanda reducida permite el uso eficiente de un número fijo de canales de tráfico asignados a cada sector de usuario. Es decir, al aumentar la extensión geográfica de los sectores de usuario durante el período de demanda mínima el número

de usuarios probables del sistema incluidos dentro de cada sector de usuario, puede mantenerse relativamente constante. Esto evita que una capacidad en exceso del canal de tráfico se desarrolle en los sectores de usuario dirigidos a un área geográfica dada en caso de que disminuya la concentración de usuarios es decir la demanda dentro del área dada.

Debe entenderse sin embargo, que en modalidades alternativas de la presente invención el número de canales de tráfico asignados a un sector de usuario particular puede variar en respuesta al cambio de las condiciones de demanda. Además, la presente invención puede permitir todavía una mejora en la utilización del canal de tráfico permitiendo que se tengan alteraciones tanto en el tamaño geográfico como en el número de canales de tráfico asociados con un sector de usuario dado

En una modalidad actualmente preferida de la invención se supervisan las estadísticas que se relacionan con el uso del canal dentro de cada sector de usuarios mediante los bancos asociados de los bancos de canal 31 y se transfieren al controlador 27 mediante un primer bus de control 34. La información de control proveniente del controlador 27, recibida respectivamente por los bancos de canal 31 y el sistema de antena 29 sobre el primer bus de control 34, y el segundo bus de control 35, permite que los

canales de tráfico sean asignados a los sectores de usuario con base en las estadísticas de uso suministradas por los bancos de canal 31. Es decir, el patrón de haz proyectado por el sistema de antena 29 se ajusta con objeto de que un juego seleccionado de los canales de tráfico se proporcionen a cada sector de usuario. En la modalidad actualmente preferida, el uso de canal monitoreado se despliega a un operador (no mostrado) mediante el controlador 27, permitiendo así la especificación de la sectorización celular deseada. En un modo automático, el control 27 se programa para asignar canales y/o tamaños de sector con base en las estadísticas de uso de canal.

En otras modalidades de la invención el controlador 27 puede configurarse para monitorear el uso del canal en virtud de la información recibida de los bancos de canal 31 sobre el primer bus control 34. La información de uso de canal pertinente podría de nuevo desplegarse a un operador con objeto de permitirle hacer los ajustes adecuados en el tamaño de cada sector de usuario. Alternativamente el controlador 27 podría programarse para proporcionar automáticamente los mandos de ajuste/asignación de canal a los bancos de canal 31 con base en el uso de canal monitoreado, una vez más evitando la necesidad de controlar la información que va a suministrarse a un operador.

Aunque en las modalidades actualmente preferidas de la invención el tamaño de cada sector de usuario se ajusta a través de la alteración del patrón de haz proyectado por el sistema de antena 29, en otras implementaciones podría lograrse una modificación equivalente del tamaño del sector a través del procesamiento de las señales formadoras de haz suministradas por los bancos de canal 31. En estas implementaciones las señales formadoras de haz procesadas por los bancos de canal 31 podrían ponderarse y combinarse antes de proporcionarse al sistema de antena 29 o recibirse desde el mismo. En esta forma podría lograrse la sectorización dinámica proporcionando información de control a los elementos electrónicos procesadores de señal (que no se muestran) acoplados a los bancos de canal 31, en lugar de suministrar esta información al sistema de antena 29.

Haciendo otra vez referencia a la Figura 1D, aparentemente una forma de acomodar la variación en la demanda del usuario sería configurar el sistema de antena 29 de la estación base para proporcionar una pluralidad de haces de antena fijos utilizando un juego asociado de elementos de antena de haz fijo. En este arreglo, cada antena de estación base proyectaría un haz de anchura fija sobre una de un juego de áreas de cobertura adyacentes. Se

asignarían entonces a cada sector de usuario diferentes números de áreas de cobertura con base en los requerimientos de uso esperados. En esta forma los cambios en la concentración de usuarios podrían compensarse al variar dinámicamente el número de haces de antena fijos utilizados para llevar los canales de tráfico asociados con un sector dado.

Una dificultad que se presenta con este enfoque es que podría esperarse una distorsión considerable del patrón de haz en forma próxima a los límites entre las áreas de cobertura incluidas dentro de un sector de usuario dado. Como ya se discutió en la parte de antecedentes de la invención, en algunos sistemas de comunicación celular, se utiliza un código PN largo de fase determinada para modular las señales de información llevadas por los canales de tráfico de un sector de usuario dado. Si estas señales de información moduladas con el código PN largo del sector de usuario dado fueran a proyectarse por un par de antenas de haz fijo en áreas de cobertura adyacentes, existiría una diferencia de fase arbitraria entre las señales moduladas PN idénticas llevadas por cada haz. Esta diferencia de fase podría engendrarse, por ejemplo, por la variación en las longitudes de las trayectorias de señal provenientes de la red formadora de haz de la estación base de cada antena de haz fijo. Como estas señales moduladas PN no están

alineadas en fase, en el límite del área de cobertura de haz la interferencia coherente resultante tendería a distorsionar el patrón de haz al producir anulaciones de señal u otras irregularidades. El desvanecimiento de la señal resultante que acompaña esta distorsión del patrón degradaría entonces la proporción señal a ruido de la señal modulada PN recibida por cualquiera de los receptores de unidad de suscriptor ubicados en forma próxima.

II. Sectorización Dinámica Utilizando Arreglo de Antena de Transmisión.

Como se describe a continuación, en una modalidad preferida de la presente invención se contempla el uso de un arreglo de antenas de haz fijo para variar dinámicamente el área abarcada por cada sector de usuario. En la forma empleada aquí, el término "sectorización dinámica de usuarios" está destinado a describir el proceso de variación de tamaño de un juego de sectores de usuario entre períodos de operación de sistema sucesivos. De acuerdo con la invención, se introduce un retardo entre cada par de señales moduladas PN idénticas proyectadas a las áreas de cobertura adyacentes dentro de un sector de usuario dado, desincorrelacionando de esta manera cada uno de estos pares de señales. En la modalidad preferida se utiliza un retardo que tiene una duración ligeramente menor

que el periodo de un chip de código largo PN para descorrelacionar las señales proyectadas hacia áreas de cobertura adyacentes dentro de cada sector de usuario. Una unidad de suscriptor colocada en un límite de área de cobertura puede de esta manera discriminarse entre, y por lo tanto recibirse separadamente, las señales moduladas PN descorrelacionadas proporcionadas hacia las áreas de cobertura adyacentes. Las señales recibidas en forma separada se alinean entonces en tiempo dentro del receptor utilizando técnicas convencionales de recepción de diversidad, y se desdispersan utilizando una replica generada localmente del código PN largo.

Al aplicar la técnica de la invención al sistema de la Figura 1A podrían introducirse retardos por lo menos entre las señales proyectadas para las áreas de cobertura C1 y C6 del primer sector de usuario residencial, y entre los pares de señal proporcionados a las áreas de cobertura C2/C3 del sector de usuario rural. Aunque en una modalidad preferida los retardos también se introducen entre los pares de señal proyectados a áreas de cobertura adyacentes dentro de diferentes sectores de usuario (por ejemplo entre el par de señal proporcionados a las áreas de cobertura C3/C4) estos pares de señal se suponen como independientemente descorrelacionados como consecuencia de la diferenciación de la fase de código largo PN asociada

con cada sector de usuario.

Haciendo referencia a la Figura 2, se muestra una representación diagramática en bloques de una red de transmisión 40 de estación base configurada para proporcionar la sectorización dinámica de usuarios de acuerdo con la invención. La red 40 se observa que incluye primero, segundo y tercer transmisores de espectro disperso 42, 44 y 46 para procesar señales de información de banda base que van a transmitirse sobre canales de tráfico asociados con el primer (#1), segundo (#2) y tercero (#3) sectores de usuario. Un generador 50 de código largo PN proporciona el código PN largo utilizado por los transmisores 42, 44 y 46 al modular las señales de información transmitidas a cada sector de usuario. Las fases relativas de los códigos largos PN suministradas a los transmisores 42, 44 y 46 se desvían por márgenes predeterminados mediante elementos de retardo de fase 52 y 54. En la modalidad preferida los elementos de retardo de fase 52 y 54 proporcionan retardos aproximadamente equivalentes en duración a chips de 768 PN. Dentro de los transmisores 42, 44 y 46 las señales de información moduladas PN se utilizan para la modulación bifase de un par de cuadratura de sinusoides. Los sinusoides modulados se suman entonces, se filtran en paso de banda, se desplazan hacia una frecuencia portadora RF y se

proporcionan a los amplificadores de transmisión 58, 60 y 62. Las señales amplificadas producidas por los amplificadores 58, 60 y 62 comprenden las señales de información moduladas PN que van a proporcionarse mediante una portadora RF a los sectores de usuarios #1, #2 y #3, respectivamente. Las salidas de cada uno de los amplificadores 58, 60 y 62 se conectan respectivamente a redes divisoras de seis vías 66, 68 y 70. Como se indica en la Figura 2, las redes divisoras 66, 68 y 70 se acoplan a una matriz de conmutación 74.

Como se describe con mayor detalle en relación a la Figura 3, la matriz de conmutación 74 comprende una conexión conmutable entre la señal de información asociada con cada sector de usuario y un juego de seis manipuladores de antena 75-80. Es decir, la matriz de conmutación 74 permite que las señales de información provenientes de cada sector de usuario se enruten hacia usuarios que están dentro de cualquiera de las áreas de cobertura C1-C6. Los manipuladores de antena 75-80 están asociados con un juego de seis antenas de estación base 85-90, cada una de las antenas 85-90 funcionan para proyectar un haz sobre una de las áreas de cobertura C1-C6 (Figura 1A). Cada manipulador de antena 75-80 se observa además que incluye un nodo de suma de entrada 92. Los nodos de suma de entrada 92 están cada uno acoplados a la matriz de conmutación 74 a través

de un juego de tres líneas de señal de entrada, cada línea de señal lleva las señales de información moduladas PN que corresponden a cualquiera de los sectores de usuario #1, #2 ó #3.

Como se observó antes, en una modalidad preferida se introducen retardos entre las señales proyectadas hacia un par de áreas de cobertura adyacentes. En consecuencia, los manipuladores de antena 75-80 se observa que incluyen elementos de retardo 95a-95f capaces de proporcionar retardos ligeramente mayores que el período de chip del código PN proporcionado por el generador de código largo PN 50. En una modalidad preferida se designa que elementos de retardo alternos a los elementos de retardo 95a-95f (por ejemplo los elementos 95b, 95d y 95f) proporcionan un retardo ligeramente mayor a un solo período de chip PN, mientras que los elementos de retardo restantes (por ejemplo los elementos 95a, 95c y 95e) se omiten (retardo de cero). Los elementos de retardo 95a-95f podrían conceptualizarse usando uno o más filtros de onda acústica de superficie (SAW). Alternativamente, una fibra óptica en espiral de longitud predeterminada podría utilizarse para crear el retardo deseado. Cada manipulador de antena 75-80 podría también incluir un amplificador de energía 96 para proporcionar una señal de salida a una de las antenas 85-90.

Haciendo referencia a la Figura 3, se muestra una representación ilustrativa de esa porción de la matriz de conmutación 74 que funciona para conectar de manera conmutable al divisor de seis vías 68 con cada uno de los manipuladores de antena 75-80. En particular, los atenuadores 97a-97f controlados digitalmente se interponen entre las salidas de los divisores 66 y los manipuladores de antena 75-80. Si, por ejemplo, se deseara que el primer sector de usuario abarcara áreas de cobertura C2-C4, entonces los atenuadores 97a, 97e y 97f podrían ajustarse a la atenuación máxima, mientras que los atenuadores 97b-97d podrían apagarse (es decir ajustarse para proporcionar una atenuación de cero). En una modalidad preferida la matriz de conmutación 74 incluye otros dos juegos de seis atenuadores digitales (no mostrados), prácticamente idénticos a los atenuadores 97a-97f, para conectar de manera conmutable los divisores 68 y 70 a los manipuladores de antena 75-80.

Los atenuadores 97a-97f de preferencia tendrían un intervalo dinámico de aproximadamente 30 dB, y serían capaces de ajustarse en incrementos de 1 dB. En esta forma, el haz proyectado a un área de cobertura particular podría extinguirse gradualmente, y después establecerse gradualmente una vez más, durante una transición entre las configuraciones de sector. Por ejemplo, si se deseara

modificar el alcance del primer sector de usuario de manera que se incluyeran solamente áreas de cobertura C3-C4 en lugar de las C2-C4, el atenuador 97b se ajustaría de manera incrementante de una atenuación cero a una atenuación máxima. Suponiendo que se deseara aumentar simultáneamente el alcance del segundo sector de usuario, el ajuste de un atenuador (no mostrado) conectado entre el segundo manipulador de antena 76 y el divisor 68 el sector cambiaría contemporáneamente de la atenuación máxima a la atenuación cero. Los atenuadores digitales 97a-97f son del tipo disponible de, por ejemplo, Anzac Corp., Parte NO. AT-210.

Aunque en la implementación de la Figura 3 la matriz de conmutación 74 se configura para permitir que cualquier sector de usuario abarque cualquier combinación de áreas de cobertura C1-C6, se entiende que en las modalidades alternas la matriz 74 podría suministrarse limitando el alcance potencial de tres a cuatro áreas de cobertura.

Haciendo referencia a las Figuras 1 y 2, cada una de las antenas 85 a 90 se diseña para proyectar una de 60 grados a una de las seis áreas de cobertura C1-C6. Se entiende, sin embargo, que la sectorización incrementada podría lograrse utilizando nueve antenas, cada una de las cuales se diseñaría para proyectar un haz de 40 grados.

Además, las antenas de modo dual capaces de proporcionar haces polarizados tanto horizontal como verticalmente podrían emplearse para ajustar hasta dos veces más usuarios dentro de cada área de cobertura. Como se describe abajo en relación a la Figura 4, los manipuladores de antena separados se utilizan para generar las señales proyectadas por cada haz polarizado horizontal y verticalmente.

Haciendo referencia a la Figura 4, se muestra un diagrama de bloques de una red 100 de transmisor de estación base, colocada para proporcionar la sectorización aumentada de usuarios al emplear tanto haces de antena polarizados horizontalmente como verticalmente. La red 100 que incluye primero, segundo y tercer pares de transmisores de espectro disperso 102a-102b, 104a-104b y 106a-106b, para procesar señales de información de banda base que van a transmitirse sobre primero (#1a-b), segundo (#2a-b) y tercero (#3-b) juegos pareados de canales de tráfico asociados con un juego correspondiente de tres sectores de usuario. Como se describe abajo, los juegos de canales de tráfico #1a, #2a y #3a pueden proyectarse selectivamente a cada área de cobertura usando haces polarizados horizontalmente, mientras que los canales de tráfico #1b, #2b y #3b pueden proyectarse de manera similar y selectiva utilizando haces polarizados verticalmente. Un generador de código largo PN (no mostrado) proporciona el código PN

largo utilizado por los transmisores 102a-102b, 104a-104b y 106a-106b al modular las señales de información transmitidas a cada sector de usuario. Una vez más, las fases relativas de los códigos largos PN suministrados a los transmisores 102a-102b, 104a-104b y 106a-106b se desvían por márgenes de fase equivalentes a un número predeterminado de chips PN.

Dentro de los transmisores 102a-102b, 104a-104b y 106a-106b las señales de información modulada PN se utilizan para modular en bifase un par de cuadratura de sinusoides. Los sinusoides modulados son entonces sumados, filtrados en paso de banda, desplazados a una frecuencia portadora RF y amplificados. Las salidas de cada uno de los transmisores 102a-102b, 104a-104b y 106a-106b se conectan respectivamente a redes divisoras de seis vías 112a-112b, 114a-114b y 116a-116b. Como se indica en la Figura 4 las redes divisoras 112a-112b, 114a-114b y 116a-116b se acoplan a una matriz de conmutación 120.

La matriz de conmutación 120 proporciona una conexión conmutable entre las señales de información transmitidas sobre los juegos pareados de canales de tráfico (por ejemplo #1a y #1b) de cada sector de usuario en un juego de seis manipuladores de antena 125a-125b hasta 130a-130b. La aplicación de la salida de cada manipulador de antena 125a-130a a las antenas 135-140 da por resultado

la proyección de haces polarizados horizontalmente hacia las áreas de cobertura C1-C6, mientras que la aplicación de la salida de cada manipulador de antena 125b-130b a las antenas 135-140 da por resultado la proyección de un haz polarizado verticalmente a cada una de las áreas de cobertura C1-C6. Como se indica por la Figura 4, la matriz de conmutación 120 está configurada de manera que los dos juegos de usuarios asociados con cada sector de usuario pueden tener servicio dentro de cada una de las áreas de cobertura C1-C6.

Haciendo referencia a la Figura 4, se muestra una representación ilustrativa de la porción de la matriz de conmutación 120 que funciona para conectar conmutablemente los divisores de seis vías 112a-b a cada uno de los manipuladores de antena 125a-b hasta 130a-b. En particular, los atenuadores controlados digitalmente 142 y 144 se interponen entre las salidas de los divisores de seis vías 112a-b y cada uno de los manipuladores de antena 125a-b hasta 130a-b. En una modalidad preferida, la matriz de conmutación 120 incluye otros dos juegos de doce atenuadores digitales (no mostrados) para conectar conmutablemente los divisores 114a-114b y 116a-116b hacia los manipuladores de antena 125a-125b hasta 130a-130b.

Cada par de manipuladores de antena (por ejemplo los manipuladores 125a-b) está conectado a una de las seis

antenas de estación base 135-140, cada antena 135-140 funciona para proyectar un haz polarizado horizontalmente y un haz polarizado verticalmente sobre una de las áreas de cobertura C1-C6 (Figura 1A). Como se observó antes, en una modalidad preferida los retardos se introducen entre las señales proyectadas hacia un par de áreas de cobertura adyacentes. Consecuentemente, los pares alternos de manipuladores de antena (por ejemplo manipuladores 105a-b, 107a-b) se colocan para proporcionar retardos ligeramente más largos que un período de chip PN simple. En otros aspectos los manipuladores de antena 105a-105b hasta 110a-110b son substancialmente similares a los manipuladores de antena 75-80.

Las Figuras 5A y 5B proporcionan respectivamente las vistas superior y lateral de una antena provisional resonante de modo dual capaz de conceptualizar las antenas 135-140. El elemento provisional 160 mostrado en la Figura 5A es de la mitad de la longitud de onda portadora en cada dimensión y se suspende por arriba de un plano de tierra 162 (Figura 5B) mediante un poste 163. El elemento provisional 160 se observa separado del plano de tierra 162 en una distancia de separación S. En la modalidad preferida la distancia S se selecciona de manera que se proporcione suficiente anchura de banda para expandir tanto las bandas de frecuencia de transmisión como de recepción.

El modo polarizado verticalmente se crea mediante la resonancia del elemento provisional 160 de manera que los máximos de voltaje se presentan en forma próxima a los bordes superior e inferior 170 y 172 del elemento provisional 160, y de manera que se presentan un voltaje nulo en la sección media. En forma similar, el modo polarizado horizontalmente se crea haciendo resonar el elemento provisional 160 de manera que los máximos de voltaje surjan en los bordes izquierdo y derecho 176 y 178 del elemento provisional 160. En una modalidad preferida, el modo polarizado verticalmente se excita mediante una sonda de voltaje aplicada al centro de los bordes superior 170 e inferior 172 del elemento provisional 160. En forma semejante el modo horizontal se induce utilizando sondas de voltaje conectadas a los bordes derecho e izquierdo 176 y 178.

IIX. Sectorización Dinámica Dentro de una Red de Recepción.

Haciendo referencia a la Figura 6, se muestra una representación diagramática en bloques de una red receptora 200 de estación base configurada para proporcionar la sectorización dinámica de usuarios de acuerdo a la invención. La red 200 se observa generalmente como complementaria a la red transmisora 40 (Figura 2) ya que se

introduce un retardo de descorrelación entre las señales recibidas desde las áreas de cobertura adyacentes. La red receptora 200 y la red transmisora 40 pueden acoplarse simultáneamente a las antenas 85-90 a través de un duplexor (no mostrado).

Las señales recibidas de las áreas de cobertura C1-C6 a través de las antenas 85 a 90 se proporcionan respectivamente para recibir amplificadores 210-215. Los amplificadores de recepción 210-215 incluyen cada uno un amplificador de bajo ruido (LNA) 220 que tiene una banda de paso centrada aproximadamente en la frecuencia de la portadora RF recibida. Los amplificadores 210-215 se observan además incluyendo elementos de retardo 225a-225f capaces de proporcionar retardos ligeramente mayores al período de chip del código largo PN utilizado para hacer la discriminación entre los sectores de usuario. En una modalidad preferida, se designan elementos alternantes a los elementos de retardo 225a-225f (por ejemplo los elementos 225b, 225d y 225f) para proporcionar un retardo ligeramente mayor a un solo período de chip PN, mientras que los elementos de retardo restantes se omiten (retardo de cero). Los elementos de retardo 225a-225f podrían conceptualizarse utilizando uno o más filtros de onda acústica superficial (SAW). Alternativamente, una fibra óptica en espiral de longitud predeterminada podría

utilizarse para crear el retardo deseado.

La salida de cada elemento de retardo 225a-225f se proporciona hacia un divisor de 3 vías 230 conectado a una matriz de conmutación 232. La matriz de conmutación 232 es esencialmente idéntica a la matriz de conmutación 74, y por lo tanto proporciona una conexión conmutable entre cada salida de los divisores de 3 vías 230 y una entrada hacia uno de las tres redes sumadoras de 6 vías 240-242. Las redes sumadoras 240-242 se acoplan a un juego correspondiente de tres receptores de diversidad 250-252 a través de los amplificadores 254-256, cada receptor de diversidad es capaz de implementarse en la forma descrita abajo en relación a la Figura 10. Cada receptor de diversidad 250-252 hace la conversión descendente en frecuencia y digitaliza la señal recibida en componentes compuestos I y Q. Los componentes compuestos I y Q se demodulan, combinan, desintercalan y decodifican.

Cada componente I y Q puede estar comprendido de señales de datos provenientes de una unidad de suscriptor dada recibida por dos o más de las antenas 88-90 asociadas con las áreas de cobertura adyacentes C1-C6 de un sector de usuario dado. Las señales recibidas asociadas con cada área de cobertura, como se selecciona por un receptor buscador en combinación con un controlador, se procesan cada uno por un receptor o modulador diferente a los

múltiples receptores o demoduladoras de datos, a los que también se hace referencia como "dedos" (no mostrados). A partir de los componentes compuestos I y Q cada dedo extrae, por descispersión, a los componentes I y Q, RI y RQ de las señales de datos y las señales piloto asociadas con cada área de cobertura. Un generador de código largo PN 260 proporciona el código PN largo utilizado por los receptores 250-252 para demodular las señales de información recibidas desde cada sector de usuario. Las fases relativas de los códigos largos PN suministrados a los receptores 251-252 se desvían en márgenes predeterminados por elementos de retardo de fase 270 y 272. En la modalidad preferida los elementos de retardo de fase 52 y 54 proporcionan retardos aproximadamente equivalentes en duración a los chips PN 768.

IV. Sectorización Dinámica Dentro de un Sistema CDMA

Haciendo referencia a la Figura 7, se muestra una representación diagramática en bloques de un transmisor de espectro disperso adecuado para conceptualizar los transmisores de espectro disperso 42, 44 y 46 (Figura 2). El transmisor de espectro disperso de la Figura 7 es del tipo descrito en la Patente de los Estados Unidos NO. 5,103,459 emitido en 1992 y titulada *"System and Method for Generating Signal Waveforms in a CDMA Cellular Telephone*

System", cedida a la titular de la presente invención, y que se incorpora aquí por referencia. En el transmisor de la Figura 7, los bits de datos 300 consisten, por ejemplo, de voz convertida en datos por un vocodificador, y que se suministran a un codificador 302 en donde los bits se codifican convolucionalmente con la repetición de símbolo código de acuerdo con la velocidad de datos de entrada. Cuando la velocidad de bit de datos es menor a la velocidad de procesamiento de bit del codificador 302, la repetición del símbolo código dicta que el codificador 302 repita los bits de datos de entrada 300 con objeto de crear una corriente de datos repetitiva a una velocidad de bits que coincide con la velocidad operativa del codificador 302. Los datos del codificador se proporcionan entonces al intercalador 304 en donde se intercala en forma convolucional. Los datos de símbolo intercalados salen del intercalador 304 a una velocidad ejemplo de 19.2 ksps a una entrada O-exclusiva 306.

En el sistema de la Figura 7 los símbolos de datos intercalados se mezclan para proporcionar una mayor seguridad en las transmisiones sobre el canal. El mezclado de las señales de canal de voz puede lograrse por codificación de pseudoruido (PN) de los datos intercalados con un código PN específico hacia una unidad de suscriptor recipiente pretendida. Estos códigos de mezclado

comprenden los códigos PN "incernos" a los cuales se hace referencia en la sección de antecedentes de la invención. Estos mezclados PN pueden proporcionarse por el generador PN 308 utilizando un esquema de cifrado o secuencia PN. El generador PN 308 incluirá típicamente un generador PN largo para producir un código PN único a una velocidad fija de 1.2288 MHz. Este código PN se hace pasar entonces a través de un decimador (no mostrado) con la secuencia de mezclado resultante de 9.2 MHz suministrándose a otra entrada del O exclusivo 306 de acuerdo con la información de identificación de la unidad del suscriptor proporcionada al mismo. La salida O-exclusiva 306 se proporciona a una entrada O-exclusiva 310.

Otra vez haciendo referencia a la Figura 7, la otra entrada de la compuerta O-exclusiva 310 se conecta a un generador de código Walsh 312. El generador Walsh 312 generá una señal que corresponde a la secuencia Walsh asignada al canal de datos sobre el cual se está transmitiendo la información. El código Walsh proporcionado por el generador 312 se selecciona a partir de un juego de 64 códigos Walsh de longitud 64. Los 64 códigos ortogonales corresponden a los códigos Walsh de una matriz Hadamard de 64 por 64, en donde un código Walsh es una sola hilera o columna de la matriz. Los datos de símbolo mezclados y el código Walsh se hacen pasar por la

compuerta O-exclusiva 310 siendo el resultado una entrada hacia las dos compuertas O-exclusivas 314 y 316.

La compuerta O-exclusiva 314 recibe también una señal PN_I, mientras que la otra entrada de la compuerta O-exclusiva 316 recibe una señal PN_Q. En aplicaciones CDMA, el generador de código largo PN 50 (Figura 2) opera para proporcionar las dos secuencias PN_I y PN_Q a los transmisores de espectro disperso 42, 44 y 46. Las señales PN_I y PN_Q son señales pseudoaleatorias (PN) que corresponden a un sector de usuario particular cubierto por el sistema CDMA y que se relaciona respectivamente con los canales de comunicación de en fase (I) y en cuadratura (Q). Las señales PN_I y PN_Q respectivamente se hacen pasar por una compuerta O-exclusiva con la salida de la compuerta O-exclusiva 310 a fin de dispersar adicionalmente los datos de usuario antes de la transmisión. La secuencia de dispersión 322 de código de canal I resultante y la secuencia de dispersión 326 de código de canal Q se utilizan para modular en bi-fase un par en cuadratura de sinusoides. Cada par en cuadratura de sinusoides se suma dentro de los transmisores 42, 44 y 46, se desplaza a una frecuencia RF y se proporciona a uno de los amplificadores 58, 60 y 62.

En la modalidad preferida, un canal piloto que no contiene modulación de datos se transmite junto con las

secuencias de dispersión S_I y S_Q de los canales I y Q. El canal piloto puede caracterizarse como una señal de espectro disperso no modulada que se utiliza para fines de rastreo y adquisición de señale. En sistemas que incorporan una pluralidad de transmisores de estación base en células adyacentes, el juego de canales de comunicación proporcionado por cada uno se identificará por una señal piloto única. Sin embargo, en lugar de utilizar un juego separado de generadores PN para las señales piloto, se entiende que un enfoque más eficiente para generar un juego de señales pilotos es utilizar desplazamientos en la misma secuencia base. La utilización de esta técnica hace que una unidad receptora destinada busque secuencialmente la totalidad de la secuencia piloto y se sintonice a la desviación o desplazamiento que produce la correlación más fuerte.

En consecuencia, la secuencia piloto de preferencia será lo suficientemente larga para que muchas secuencias diferentes puedan generarse por desplazamientos en la secuencia básica para soportar un gran número de señales piloto en el sistema. Además, la separación o desplazamiento debe ser suficientemente grande para asegurar que no haya interferencia en las señales piloto. Por lo tanto, en una modalidad ejemplaria la longitud de la secuencia piloto se selecciona para sea de 2^{15}, lo que

permite 512 señales piloto distintas que se desvían en una secuencia básica de 64 chips.

Haciendo referencia a la Figura 8, una red de generación piloto 330 incluye un generador Walsh 340 para proporcionar la secuencia Walsh W_0 "cero" que consiste de todos los ceros hacia los combinadores O-exclusivos 344 y 346. La secuencia Walsh W_0 se multiplica por las secuencias PN_I y PN_Q utilizando los combinadores O-exclusivos 344 y 346 respectivamente. Como la secuencia W_0 incluye solamente ceros, el contenido de información de las secuencias resultantes depende solamente de las secuencias PN_I y PN_Q. Las secuencias producidas por los combinadores O-exclusivos 344 y 346 se proporcionan como entradas a los Filtros de Respuesta de Impulso Finito (FIR) 350 y 352. La salida de las secuencias filtradas proveniente de los filtros FIR 350 y 352, corresponde respectivamente a las secuencias piloto P_I y P_Q de los canales I y Q, y se suministra a los transmisores RF 382.

Haciendo referencia a la Figura 9, se muestra una implementación ejemplo del transmisor RF 382. Los transmisores 382 incluyen un sumador de canal I 370 para sumar las señales de datos dispersos PM_I, S_{Ii}, i=1 hasta N, con el piloto P_I de canal I. En forma similar un sumador de canal Q 372 sirve para combinar las señales de datos dispersos PM_Q, S_{Qi}, i=1 a N, con el piloto P_I de canal Q.

Los convertidores digital a analógico (D/A) 374 y 376 se proporcionan para convertir la información digital de los sumadores de canal I y canal Q 370 y 372, respectivamente a la forma analógica. Las formas de onda analógica producidas por los convertidores D/A 374 y 376 se proporcionan junto con las señales de frecuencia portadora de oscilador local (LO), Cos(2πft) y Sen(πft), respectivamente, a los mezcladores 388 y 390 en donde se mezclan y proporcionan al sumador 392. Las señales portadoras de fase en cuadratura Sen(πft) y Cos(2πft) se proporcionan a partir de fuentes de frecuencia adecuadas (no mostradas). Estas señales RF se suman en el sumador 392 y se proporcionan al mezclador 394.

El mezclador 394 mezcla la señal sumada con una señal de frecuencia RF a partir del sintetizador de frecuencia 396 a fin de proporcionar la conversión ascendente en frecuencia a la banda de frecuencia RF. La señal RF incluye componentes en fase (I) y en cuadratura (Q), y se filtra en paso de banda por el filtro de paso de banda 398 y sale a uno de los amplificadores RF 58, 60, 62 (Figura 2). Debe entenderse que el transmisor RF 382 puede emplear diferentes implementaciones con una variedad de técnicas de sumado, mezclado, filtrado y amplificación de señal que no se describen aquí, pero que son bien conocidos en este campo.

La Figura 10 es un diagrama de bloques de un receptor de diversidad ejemplo asociado con una de las unidades de suscriptor 12 (Figura 1A), y por lo tanto se coloca para recibir las señales RF transmitidas por una o más de las antenas 85-90 de la estación base 40 (Figura 2). En la Figura 10 la señal RF transmitida por la estación base 40 es recibida por la antena 410 y proporcionada a un receptor RAKE de diversidad que está comprendido del receptor analógico 412 y el receptor digital 414. La señal como es recibida por la antena 410 y proporcionada al receptor analógico 412 puede estar comprendida de propagaciones de trayectoria múltiple de las mismas señales piloto y de datos destinadas para los receptores de suscriptor individuales o múltiples. Los receptores analógicos 412, que se configuran en la modalidad ejemplo como un modem QPSK, se convierte en forma descendente en frecuencia y digitaliza la señal recibida o los componentes compuestos I y Q. Los componentes compuestos I y Q se proporcionan al receptor digital 414 para la demodulación. Los datos demodulados son proporcionados entonces a la circuiteria digital 416 para la combinación, desintercalación y decodificación.

Cada salida de los componentes I y Q provenientes del receptor analógico 412 puede estar comprendida de señales de datos correspondientes transmitidas por dos o

más de las antenas 85-90 asociadas con las áreas de cobertura adyacentes C1-C6 de un sector de usuario dado. Como se discutió antes, una desviación de fase se introduce entre las señales de datos proporcionadas a las áreas de cobertura adyacentes en un sector de usuario particular. En el receptor digital 414 las señales recibidas asociadas con cada área de cobertura, según se selecciona por un receptor buscador 415 en combinación con un controlador 418, se procesan cada uno por un receptor o demodulador de los varios receptores o demoduladores de datos 420a-420c, a los que también se hace referencia como "dedos". Aunque solo tres de los dedos demoduladores de datos (demoduladores 420a-420c) se ilustran en la figura 10, debe entenderse que pueden utilizarse más o menos dedos. A partir de los componentes compuestos I y Q, cada dedo extrae, por desdispersión, los componentes I y Q PI y PQ de las señales piloto y de datos, asociados con cada área de cobertura.

En una implementación ejemplo, cada unidad de suscriptor 12 es asignada a uno de un juego de 64 códigos Walsh ortogonales W_i de longitud 64. Esto permite que un juego de canales que incluyen a un canal piloto, 61 canales I y 63 canales Q se transmiten utilizando un par dado de secuencias de dispersión PN_I y PN_Q. La señal piloto extraído se utiliza para alinearse en tiempo dentro de un

combinador de símbolo (no mostrado) dentro del receptor de la unidad de suscriptor. Cuando la unidad de suscriptor se coloca en forma próxima al límite de las áreas de cobertura adyacentes asignadas al mismo sector de usuario, los cálculos de los datos admitidos a cada área de cobertura se alinean en tiempo y se adicionan conjuntamente, mejorando así la proporción señal a ruido.

V. Sectorización Dinámica Utilizando Patrón de Haz en Fase.

Como se discutirá antes, en la modalidad preferida se introduce un retardo entre los haces proyectados a áreas de cobertura de antena adyacentes a fin de descorrelacionar las señales transmitidas a cada área. Este enfoque se diseña para eliminar prácticamente toda interferencia destructiva entre los haces proporcionados a áreas de cobertura adyacentes, evitando así la formación de señales nulas y otras distorsiones del patrón de haz. Un receptor de diversidad asociado con una unidad suscriptora colocado cerca del límite del área de cobertura puede por lo tanto recibir de manera separada las señales descorrelacionadas, y subsecuentemente combinar las señales recibidas en forma separada.

En una modalidad alterna de la invención la estación base celular se diseña para efectuar la

sectorización dinámica de usuarios proporcionando un juego de haces fijos proyectados en alineamiento preciso de fase. Haciendo referencia a la Figura 11A, se muestra el patrón de azimuth de un haz fijo de 40 grados que se supone se proyecta mediante una primera antena de estación base asociada con una de las áreas de cobertura C1-C6 (Figura 1A). Si una segunda antena de estación base, dispuesta para proporcionar un segundo haz fijo de 40 grados a un área de cobertura adyacente es manipulada en fase con la primera antena de estación base, el patrón mostrado en la Figura 11B se produce. Por lo tanto es evidente que la anchura de un sector de usuario puede aumentarse en proporción al número de haces excitados. Como los haces se generan en fase, los haces interfieren constructivamente cerca de los límites del área de cobertura y por lo tanto se combinan efectiva y coherentemente dentro del sector base en lugar de dentro del receptor de la unidad de suscriptor.

Haciendo referencia a la Figura 12, se muestra una representación diagramática de bloque de una red de transmisor 440 de estación base configurada para proporcionar la sectorización dinámica de usuarios proyectando un juego de haces en fase a cada sector de usuario. La red 440 se observa prácticamente similar a la red de la Figura 2, en donde se utilizan números iguales

para identificar componentes similares del sistema. En lugar de incluir elementos de retardo de fase 95a-95f, los manipuladores de antena 75-80 incluyen ecualizadores de fase 444a-444f ajustados de manera que las antenas 85-90 sean manipuladas en fase. El ajuste de los ecualizadores 444a-444f puede efectuarse, por ejemplo, durante la instalación de la estación base aplicando una señal de prueba idéntica a cada manipulador 75-80.

Más específicamente, durante un proceso de calibración se proporciona un juego de señales de prueba de amplitud y fase idénticas hacia los manipuladores de antena 75-80. La salida de los pares adyacentes de cables de antena 445a-445f, respectivamente, asociada con las antenas 85-90, se conectan entonces a los portillos de entrada dual de un combinador de energía. El ecualizador de fase dentro de los impulsores de antena acoplados a uno de los cables de antena se ajusta entonces hasta que la salida del combinador de energía se aumente al máximo. Este procedimiento se repite para cada par adyacente de manipuladores de antena, es decir para manipuladores 75 y 76, los manipuladores 76 y 77, y así sucesivamente.

Un procedimiento análogo se utiliza para calibrar la red de recepción 200 (Figura 6). En particular, un juego de señales de prueba de amplitud y fase idénticas que inyectan en los portillos de los cables de antena 224a-224f

acoplados nominalmente a las antenas 85-90. Un combinador de energía que tiene seis portillos de entrada y un solo portillo de salida se conecta entonces a los divisores 230 de un par adyacente de amplificadores de recepción 210-215. Un ecualizador de fase (no mostrado) dentro de uno de los amplificadores de recepción conectado al combinador de energía, se ajusta entonces hasta que la energía de salida del combinador aumenta al máximo. Este proceso se repite para cada par adyacente de amplificadores de recepción 210-215.

La Figura 13 ilustra una configuración 450 de estación de base alternativa para proporcionar sectorización dinámica de usuarios al proyectar un juego de haces en fase. Como se indica en la Figura 13, el alineamiento de fase se mantiene entre haces adyacentes colocando la matriz de conmutación y los manipuladores de antena en forma próxima a las antenas 85-90. Es decir, en la configuración de la Figura 13, la matriz de conmutación 74 y los manipuladores de antena 85-90, le seguirán a los cables de transmisión 452-454, en lugar de precederlos, dentro de la torre de antena 458 de estación base. El acoplamiento directo de los manipuladores 75-80 a las antenas 85-90 evita ventajosamente que las diferencias de fase que se deben a la variación y a la longitud del cable y semejantes, se introduzcan entre los haces transmitidos a

las áreas de cobertura adyacentes.

VI. Subsistema de Antena

En las dos modalidades tanto de la fase descorrelacionada como de la fase controlada de la invención (ver por ejemplo las Figuras 2 y 12), el tamaño de un sector de usuario dado varía utilizando una combinación de uno o más haces para proporcionar la señal de información para el sector. Cada uno de estos haces puede crearse utilizando cualquiera de un número de técnicas convencionales. Por ejemplo un juego de antenas de haz fijo distintas podrían utilizarse para proyectar un juego de haces de ángulo predeterminado. En este enfoque, las antenas se montan y alinean de manera que cada haz abarca un área de cobertura predeterminada. En una modalidad ejemplo un juego de seis antenas se utilizan para proporcionar un haz de 60 grados a cada una de las seis áreas de cobertura (ver por ejemplo Figura 1A).

Alternativamente, una antena de arreglo en fase puede utilizarse para formar simultáneamente más de un solo haz. Por ejemplo, la Figura 14 muestra un arreglo triangular de paneles de antena de arreglo en fase, primero, segundo y tercero, 480, 482 y 484, que colectivamente operan para proporcionar un juego de nueve haces de antena a las áreas de cobertura C1-C9. En

particular, el panel de antena 480 proyecta tres haces fijos de 40 grados para las áreas de cobertura C1-C3, mientras que los paneles de antena 482 y 484 proyectan haces fijos de 40 grados para las áreas de cobertura C4-C6 y C7-C9, respectivamente.

Como se indica en la Figura 15, una implementación preferida de la cara de cada panel de antena incluye un arreglo de 4x4 de elementos provisionales, los elementos dentro de cada columna se identifican respectivamente con los números de referencia 486 a 489. Suponiendo una frecuencia portadora RF de 850 MHz, cada elemento provisional puede fabricarse a partir de una sección cuadrada de un material provisional cargado dialéctricamente con un área de 4 pulgadas^2. Esto da por resultado en cada panel de antena cuadrada 482-484 un área de aproximadamente 4 pies cuadrados.

Haciendo referencia a la Figura 16, se muestra una antena de arreglo en fase y una red formadora de haz 490, colocada para proporcionar tres haces de una sola cara de antena. Una matriz de conmutación (no mostrada) proporciona las señales de información que corresponden a los sectores de usuario #1, #2 y #3 mediante las líneas de señal de entrada 494a-494c. La red formadora de haz 490 incluye divisores de 4 vías 495a-c, respectivamente conectados a las líneas de señal 494a-c. Las cuatro

salidas de cada divisor 455a-c están conectadas mediante elementos de retardo de fase 496 a uno de cuatro nodos de suma 498-501. Las señales compuestas provenientes de los nodos de suma 498-501 se proporcionan respectivamente a amplificadores de potencia 504-507. Como se indica en la Figura 16, cada columna de elementos de arreglo 486-489 es manipulada por uno de los amplificadores 504-507. En implementaciones alternas se utiliza un amplificador de energía separado para manipular cada elemento de arreglo 486-489.

En una modalidad ejemplo los elementos de retardo 496 se ajustan de manera que cada uno de los tres haces se proyectan a un ángulo de 40 grados a una de las tres áreas de cobertura adyacentes. Los tres haces proyectados por un solo panel de antena expandirían entonces en un arco de 120 grados. Tres de estos paneles podrían montarse para proporcionar un juego de nueve haces que abarquen un arco de 360 grados.

La descripción anterior de las modalidades preferidas se proporciona para permitir a cualquier persona con pericia normal en este campo elaborar o utilizar la presente invención. Las diversas modificaciones a estas modalidades se harán evidentes para los expertos en este campo y los principios genéricos definidos aquí pueden aplicarse a otras modalidades sin el uso de la facultad

inventiva. De esta manera, la presente invención no pretende limitarse a las modalidades aquí mostradas sino que tiene el alcance más amplio consistente con los principios y particularidades novedosas que se revelan aquí. Por ejemplo, además de dirigirse a la necesidad de la asignación de canales de tráfico flexibles como consecuencia de los cambios a corto término en la demanda de los usuarios, el método y el aparato de la invención pueden emplearse para ajustarse a cambios a largo término en la demanda de los usuarios. Estas variaciones a largo término en la demanda podrían estar acompañadas, por ejemplo, de desplazamiento en la distribución de la población y en los patrones de construcción dentro de un área geográfica dada.

NOVEDAD DE LA INVENCIÓN

Habiendo descrito el presente invento, se considera como una novedad y, por lo tanto, se reclama como propiedad lo contenido en las siguientes

REIVINDICACIONES:

1. Un sistema para transportar información a por lo menos un usuario en un sistema de comunicación de espectro disperso, que comprende:

un medio para generar, a una velocidad de chip predeterminada, una primera señal de ruido pseudoaleatorio (PN) de un primer código PN predeterminado;

un primer medio para combinar la primera señal PN y una primera señal de información y para proporcionar una primera señal de modulación resultante;

un medio para proporcionar una segunda señal de modulación haciendo retardar la primera señal de modulación en un primer retardo predeterminado que se relaciona inversamente a la velocidad de chip;

un medio para transmitir selectivamente la primera y la segunda señales de modulación respectivamente a la primera y la segunda áreas de cobertura;

mediante lo cual la transmisión selectiva de la primera y la segunda señales de modulación da por resultado la variación en tamaño de un primer sector de usuario en donde se incluye el por lo menos un usuario.

2. El sistema según la reivindicación 1, en donde el medio para transmitir selectivamente incluye medios para transmitir la primera y la segunda señales de modulación de manera que la segunda área de cobertura traslape por lo menos parcialmente a la primera área de cobertura.

3. El sistema según la reivindicación 2, que incluye además:

un medio para proporcionar una tercera señal de modulación y para proporcionar una cuarta señal de modulación que corresponde a una versión retardada de la tercera señal de modulación;

un medio para transmitir selectivamente la tercera y la cuarta señales de modulación respectivamente a la segunda área de cobertura y a la tercera área de cobertura;

mediante lo cual la transmisión selectiva de la tercera y la cuarta señales de modulación da por resultado la variación en tamaño de un segundo sector de usuario.

4. El sistema según la reivindicación 2, en donde el sistema incluye además:

un medio para generar, a una velocidad de chip predeterminada, una segunda señal de ruido pseudoaleatorio del código PN predeterminado, la primera y la segunda señales PN se desvían en fase,

un segundo medio para combinar la segunda señal PN en una segunda señal de información y para proporcionar una tercera señal de modulación resultante, y

un medio para proporcionar una cuarta señal de modulación al retardar la tercer señal de modulación en un retardo predeterminado que está inversamente relacionado con la velocidad de chip predeterminada.

5. El sistema según la reivindicación 4, en donde el medio para transmitir selectivamente incluya un medio para transmitir selectivamente la primera y la segunda señales de modulación respectivamente a la primera y la segunda áreas de cobertura, exclusivamente durante un primer período de operación del sistema, y para transmitir selectivamente la tercera y la cuarta señales de modulación respectivamente a la primera y la segunda áreas de cobertura, exclusivamente durante un segundo período de operación del sistema.

6. El sistema según la reivindicación 1, que incluye además un receptor para recibir la primera y la segunda señales de modulación y para proporcionar la primera señal de información al por lo menos un usuario con base en lo misma.

7. El sistema según la reivindicación 6, en donde el receptor incluya medios para generar una replica del código PN, y medios para demodular la primera y la

segunda señales moduladas, dando una primera y una segunda señales demoduladas que utilizan la replica del primer código PN.

8. El sistema según la reivindicación 7, en donde el receptor incluya medios para combinar coherentemente la primera y la segunda señales demoduladas.

9. En un sistema de comunicación de suscriptor celular en donde los usuarios que están dentro de por lo menos una célula se comunican señales de información entre sí mediante por lo menos un sitio celular que utiliza señales de comunicación de espectro disperso, en donde ese sitio celular incluye un transmisor de sitio celular, el transmisor comprende:

un primer medio para proporcionar primero y segundo juegos de señales de información de espectro disperso para transmitirse a los usuarios dentro de un primer sector de usuario de la primer célula, el medio para proporcionar incluye un medio para generar el segundo juego de señales de información de espectro disperso retardando cada una de las señales de información incluidas dentro del primer juego; y

un primer medio para transmitir selectivamente, durante un primer período de funcionamiento del sistema, al primero y al segundo juegos de señales de información de espectro disperso respectivamente hacia la primera y la

segunda área de cobertura dentro de la por lo menos una célula, en donde el tamaño del primer sector de usuario varía a través de la transmisión selectiva del primero y segundo juegos de señales de información de espectro disperso.

10. El sistema según la reivindicación 9, en donde el primer medio para transmitir selectivamente incluye primera y segunda antenas para proyectar primero y segundo haces sobre la primera y segunda áreas de cobertura, respectivamente, el primer haz lleva el primer juego de señales de información de espectro disperso y el segundo haz lleva el segundo juego de señales de información de espectro disperso.

11. El sistema según la reivindicación 10, en donde el primer medio para proporcionar incluye medios para dividir cada una de las señales de información incluidas dentro del primer juego en un par de subseñales idénticas y para retardar una de las subseñales de cada par.

12. El transmisor según la reivindicación 11, caracterizado porque el medio para transmitir selectivamente incluye:

un medio para atenuar selectivamente cada una de las subseñales, y

un medio para acoplar una de las subseñales dentro de cada par de la primera antena y para acoplar la

otra de las subseñales dentro de cada par de la segunda antena.

13. El transmisor según la reivindicación 9, que incluye además:

un segundo medio para proporcionar tercero y cuarto juegos de señales de información de espectro disperso para su recepción por los usuarios dentro de un segundo sector de usuario de la primera célula, el segundo medio para proporcionar incluye medios para generar el cuarto juego de señales de información de espectro disperso retardando cada una de las señales de información incluidas dentro del tercer juego;

un segundo medio para transmitir selectivamente, durante un segundo periodo de operación del sistema, al tercero y cuarto juegos de señales de información de espectro disperso respectivamente hacia la primera y la segunda área de cobertura dentro de la por lo menos una célula, permitiendo así que el tamaño de un segundo sector de usuario incluido dentro de la por lo menos una célula varíe de acuerdo con la concentración de usuario en el segundo sector.

14. El sistema según la reivindicación 9, que incluye además un receptor, el receptor comprende:

medios para recibir una de las señales de información incluidas dentro del primer juego y para

recibir una versión retardada de la señal de información incluida dentro del segundo juego.

un medio para combinar coherentemente las señales de información recibidas y para proporcionar la señal resultante a un usuario del sistema.

15. Un sistema para transportar información a por lo menos un usuario en un sistema de comunicación de espectro disperso, que comprende:

medios para generar una primera señal de ruido pseudoaleatorio (PN) de un primer código PN predeterminado;

un primer medio para combinar la primera señal PN y una primera señal de información y para proporcionar una primera señal de modulación resultante;

un medio para proporciona una segunda señal de modulación replicando la primera señal de modulación;

un medio para alinear la primera y la segundas señales de modulación en fase, y para transmitir selectivamente la primera y la segunda señales de modulación alineadas en fase resultantes, respectivamente a la primera y a la segunda área de cobertura;

mediante lo cual la transmisión selectiva de la primera y la segunda señales de modulación da por resultado una variación en tamaño de un primer sector de usuario en el que está incluido por lo menos un usuario.

16. El sistema según la reivindicación 15, en

donde el medio para transmitir selectivamente incluye medios para permitir selectivamente la primera y la segunda señales de modulación, respectivamente hacia primera y segunda áreas de coberturas exclusivamente durante un primer periodo de operación del sistema, y para transmitir selectivamente tercera y cuarta señales de modulación respectivamente a la primera y segunda áreas de cobertura, exclusivamente durante un segundo periodo de operación del sistema, la tercer señal de modulación es esencialmente idéntica a la cuarta señal de modulación y está alineada en fase con la misma.

17. Un sistema de comunicación de suscriptor celular en donde los usuarios dentro de por lo menos una de las señales de información de comunicación celular entre ellos mediante por lo menos un sitio celular que utiliza señales de comunicación de espectro de dispersión en donde ese sitio celular incluye un transmisor de sitio celular, el transmisor comprende:

primeros medios para proporcionar el primero y el segundo juegos de señales de información de espectro de dispersión para ser recibidas por los usuarios dentro de un primer sector de usuario de la primera célula, el medio para proporcionar incluye medios del segundo juego de señales de información de espectro disperso replicando cada una de las señales de información dentro del primer juego;

un medio para alinear en fase cada una de las señales de información dentro del primer juego con las correspondientes réplicas de las mismas dentro del segundo juego a fin de formar primero y segundo juegos de las señales de información alineadas en fase;

un primer medio para transmitir selectivamente, durante un primer período de operación del sistema, el primero y el segundo juegos de señales de información alineadas en fase, respectivamente a la primera y a la segunda áreas de cobertura dentro de la por lo menos una célula, en donde el tamaño del primer sector de usuario varía a través de la transmisión selectiva del primero y segundo juegos de señales de información alineadas en fase.

18. Un método para transportar información a por lo menos un usuario en un sistema de comunicación de espectro disperso, que comprende de:

generar a una velocidad de chip predeterminada, una primera señal de ruido pseudoaleatorio (PN) de un primer código PN predeterminado;

combinar la primera señal PN y una primera señal de información, y para proporcionar una primera señal de modulación resultante;

proporcionar una segunda señal de modulación al retardar la primera señal de modulación en un retardo predeterminado que se relaciona inversamente a la velocidad

de chip;

transmitir selectivamente la primera y la segunda señales de modulación respectivamente a la primera y a la segunda áreas de cobertura; mediante lo cual la transmisión selectiva de la primera y la segunda señales de modulación da por resultado una variación en tamaño de un primer sector de usuario en el que está incluido por lo menos un usuario.

19. El método según la reivindicación 18, en donde el paso de transmitir selectivamente incluye el paso de transmitir la primera y la segunda señales de modulación de manera que la segunda área de cobertura traslape por lo menos parcialmente la primer área de cobertura.

20. El método según la reivindicación 19, que incluya además el paso de;

proporcionar una tercera señal de modulación, y proporcionar una cuarta señal de modulación que corresponde a una versión retardada de la tercera señal de modulación;

transmitir selectivamente la tercera y cuarta señales de modulación respectivamente a la segunda área de cobertura y a una tercera área de cobertura;

mediante lo cual la transmisión selectiva de la primera y la segunda señales de modulación da por resultado la variación del tamaño del segundo sector de usuario.

21. El método según la reivindicación 19, que

incluye además el paso de:

generar, a una velocidad de chip predeterminada, una segunda señal de ruido pseudoaleatorio (PN) del código PN predeterminado, la primera y la segunda señales PN están desviadas en fase;

combinar la segunda señal PN y una segunda señal de información, y proporcionar una tercera señal de modulación resultante; y

proporcionar una cuarta señal de modulación al retardar la tercera señal de modulación en un retardo predeterminado que se relaciona inversamente a la velocidad de chip predeterminada.

22. El método según la reivindicación 21, en donde el paso de transmitir selectivamente incluye el paso de transmitir selectivamente la primera y la segunda señales de modulación respectivamente hacia la primera y la segunda áreas de cobertura, exclusivamente durante un primer periodo de operación del sistema, y el paso de transmitir selectivamente la tercera y cuarta señales de modulación respectivamente a la primera y a la segunda áreas de cobertura exclusivamente durante un segundo periodo de operación del sistema.

23. El método según la reivindicación 18, que incluye además el paso de recibir la primera y la segunda señales de modulación y proporcionar la primera señal de

información al por lo menos un usuario con base a la misma.

24. El método según la reivindicación 23, que incluye además el paso de generar una réplica del código PN, y demodular la primera y la segunda señales moduladas hacia la primera y segunda señales demoduladas que utilizan las réplicas del primer código PN.

25. El método según la reivindicación 24, que incluye además el paso de combinar coherentemente la primera y la segunda señales demoduladas.

26. En un sistema de comunicación de subscriptor celular en donde los usuarios que están dentro de por lo menos una célula se comunican entre sí señales de información mediante por lo menos un sitio celular utilizando señales de comunicación de espectro disperso, en donde el sitio celular incluye un transmisor de sitio celular, un método de transmisión de señal proveniente del sitio celular que comprende los pasos de:

proporcionar primero y segundo juegos de señales de información de espectro disperso para transportarse a los usuarios dentro de un primer sector de usuario de la primera célula, el paso de proporcionar incluye el paso de generar el segundo juego de señales de información de espectro disperso retardando cada una de las señales de información incluidas dentro del primer juego; y

transmitir selectivamente, dentro de un primer

periodo de operación del sistema, el primero y segundos juegos de señales de información de espectro disperso respectivamente a la primera y segunda áreas de cobertura dentro de la por lo menos una célula, en donde el tamaño del primer sector de usuario varía a través de la transmisión selectiva del primero y segundo juegos de señales de información de espectro disperso.

27. Un método para transportar información a por lo menos un usuario en un sistema de comunicación de espectro disperso, que comprende los pasos de:

generar, a una velocidad de chip predeterminada, una primera señal de ruido pseudoaleatorio (PN) de un primer código PN predeterminado;

combinar la primera señal PN y un primera señal de información y proporcionar una primera señal de modulación resultante;

proporcionar una segunda señal de modulación replicando la primera señal de modulación;

alinear la primera y la segunda señales de modulación en fase, y transmitir selectivamente la primera y la segunda señales de modulación resultantes alineadas en fase a la primera y a la segunda áreas de cobertura.

28. Un sistema para recibir información transmitido por lo menos a un usuario en un sistema de comunicación de espectro disperso, que comprende:

un medio para recibir selectivamente una primera señal proveniente de una primera área de cobertura y para recibir selectivamente una segunda señal proveniente de una segunda área de cobertura, la primera y la segunda señales son recibidas respectivamente a través de primera y segunda antenas asociadas con la primera y la segunda áreas de cobertura, la primera y la segunda señales están moduladas por una primera señal de ruido pseudoaleatorio de un primer código PN predeterminado;

un medio para retardar la primera señal recibida a través de la segunda antena mediante un primer retardo a fin de producir una señal retardada, el retardo se selecciona inversamente a una velocidad de chip de la señal PN; y

un medio para combinar coherentemente la segunda señal recibida a través de la segunda antena con la señal retardada, y para proporcionar una primera señal de modulación resultante;

mediante lo cual la recepción selectiva de la primera y la segunda señales dan por resultado la variación en tamaño en un primer sector de usuario en el cual está incluido el por lo menos un usuario.

29. El sistema según la reivindicación 28, que incluye además:

un medio para recibir selectivamente una tercera

señal proveniente de la segunda área de cobertura y para recibir selectivamente una cuarta señal proveniente de una tercera área de cobertura, la tercera y la cuarta señales se reciben respectivamente a través de la segunda hasta la tercera antenas;

un medio para retardar la tercer señal recibida a través de la segunda antena en por lo menos un primer retardo a fin de producir una segunda señal retardada; y

un medio para combinar coherentemente la cuarta señal recibida a través de la tercer antena con la segunda señal retardada;

mediante lo cual la recepción selectiva de la tercera y la cuarta señales da por resultado la variación de tamaño de un segundo sector de usuario.

30. El sistema según la reivindicación 1, y en donde el medio para transmitir selectivamente la primera y la segunda señales de modulación incluye el paso de transmitir selectivamente el primero y el segundo componentes de polarización de la primera señal de modulación y el primero y el segundo componentes de polarización de la segunda señal de modulación.

31. Un transceptor de comunicaciones colocado dentro de una primera célula de un sistema de comunicación celular, el transceptor comprende:

un sistema de antena para proyectar un patrón de

haz de antenas sobre la primera célula;

un medio de banco de canal, acoplado electromagnéticamente al sistema de antena, para suministrar señales forzadoras de haz hacia el sistema de antena, de manera que el patrón de haz de antena se proyecte a fin de sectorizar la primer célula en una pluralidad de sectores de usuario;

cada uno de los sectores de usuario tiene una pluralidad de canales de tráfico asociados con el mismo; y

un medio controlador para supervisar el uso de la pluralidad de canales de tráfico asociados con cada sector de usuario, y para suministrar información de control al sistema de antena con objeto de que el tamaño de los sectores de usuario se ajuste de acuerdo al uso de canal de tráfico monitoreado.

32. En sistema de comunicación celular que incluye por lo menos una célula sectorizada en una pluralidad de sectores de usuario, un método para variar dinámicamente la sectorización de usuarios de la por lo menos una célula, que comprende los pasos de:

monitorear el uso de una pluralidad de canales de tráfico asignados a la pluralidad de sectores de usuario, cada uno de los canales de tráfico de usuario es asignado a un usuario dentro de la por lo menos una célula; y

ajustar el tamaño geográfico de los sectores de

usuario con base en el uso monitoreado de la pluralidad de canales de tráfico.

33. El método según la reivindicación 32, que incluye además el paso de:

proyectar un patrón de haz de antena sobre la por lo menos una célula, el patrón de haz de antena lleva señales de información asociadas con la pluralidad de canales de tráfico de usuario,

y variar la proyección del patrón de haz de antena de acuerdo con el uso monitoreado de la pluralidad de canales de tráfico.

RESUMEN DE LA INVENCIÓN

Se revelan un sistema y un método para variar dinámicamente la sectorización de canal de tráfico dentro de un sistema de comunicación de espectro disperso. En una implementación preferida el sistema funciona para transportar información a por lo menos un usuario especificado en un sistema de comunicación de espectro disperso e incluye un generador de códigos pseudoaleatorios (50) para generar, a una velocidad de chip predeterminada, una señal de ruido pseudoaleatorio (PN) de un código PN predeterminado. La señal PN se combina entonces con una primera señal de información en un transmisor de espectro disperso (42) para proporcionar una señal de información dispersa PN. El sistema incluye además por lo menos un transmisor de espectro disperso adicional (44, 46), cada uno para recibir a través del elemento de retardo respectivo (52, 54) versiones retardadas de la señal PN para proporcionar por lo menos una señal de modulación adicional. Una red de transmisión de conmutación (74) se coloca para transmitir selectivamente mediante las antenas (85, 86) la primera señal de modulación y las señales de modulación adicionales respectivamente hacia la primera y la por lo menos una área de cobertura adicional. La transmisión selectiva de la primera y la por lo menos una señal de modulación adicional da por resultado la variación

en tamaño del primer sector de usuario. El primer sector de usuario está asociado con un primer juego de canales de tráfico, uno de los cuales es designado al usuario específico. El sistema también puede configurarse para recibir selectivamente y para combinar coherentemente, la primera y la segunda señales de modulación a partir de la primera y la segunda áreas de cobertura.

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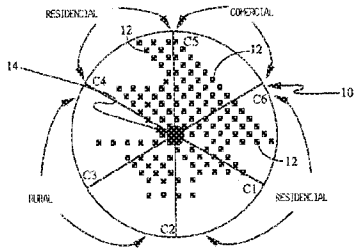

FIG. 1A

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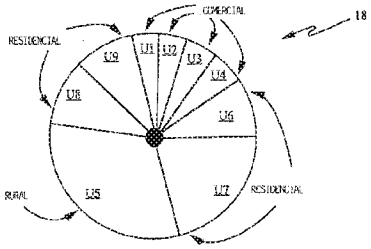

FIG. 1B

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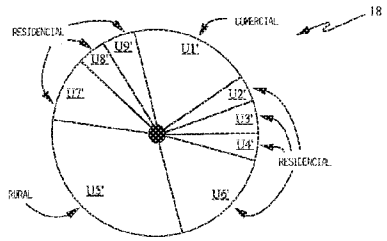


FIG. 1C

4/19

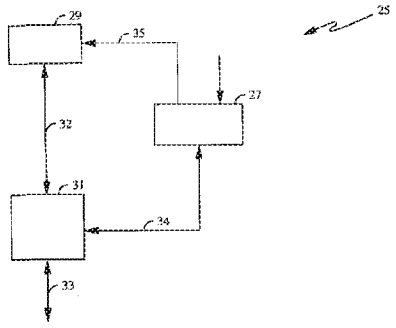
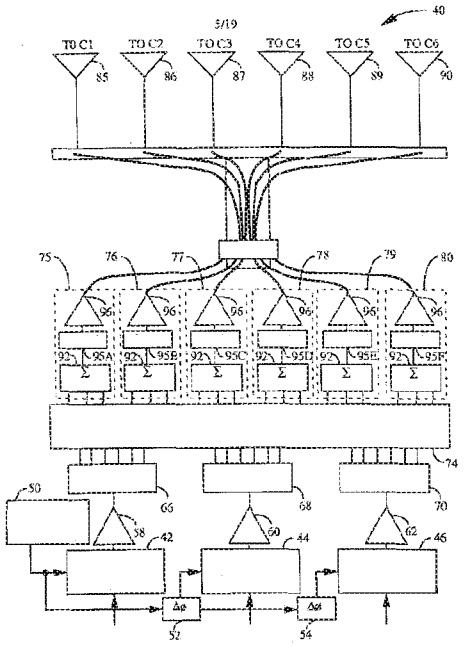


FIG. 1D


40
TO C1
TO C2
TO C3
TO C4
TO C5
TO C6
85
86
87
88
89
90
75
76
77
78
79
80
95
96
92
95A
95B
95C
95D
95E
95F
Σ
74
50
65
68
70
38
42
60
44
62
46
Δφ
52
54

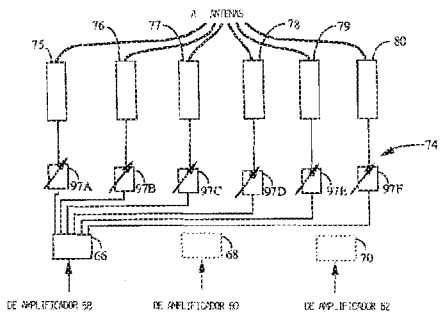

A ANTENAS
75
76
77
78
79
80
74
97A
97B
97C
97D
97E
97F
65
68
70
DE AMPLIFICADOR 58
DE AMPLIFICADOR 60
DE AMPLIFICADOR 62

FIG. 3

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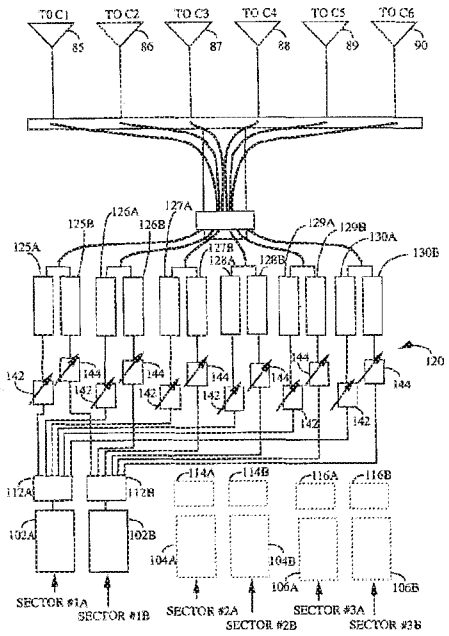


8/19

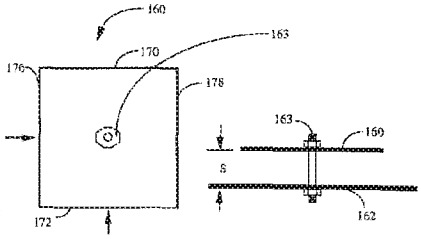
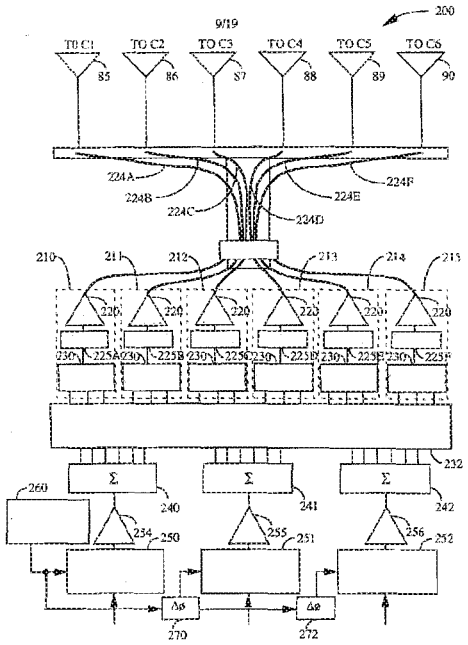


FIG. 5A FIG. 5B


200
TO C1
TO C2
TO C3
TO C4
TO C5
TO C6
85
86
87
88
89
90
224A
224B
224C
224D
224E
224F
210
211
212
213
214
215
220
225A
225B
225C
225D
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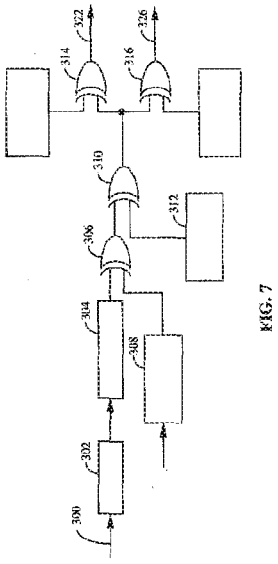
240
241
242
260
234
250
255
251
256
252
Δθ
Δθ
270
272


322
326
314
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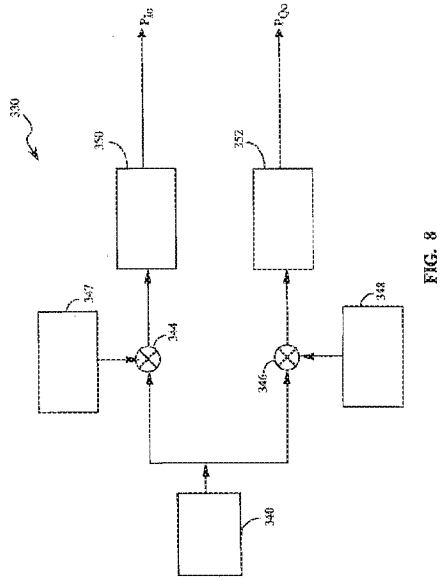
300

FIG. 7


330
350
352
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354
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340

FIG. 8

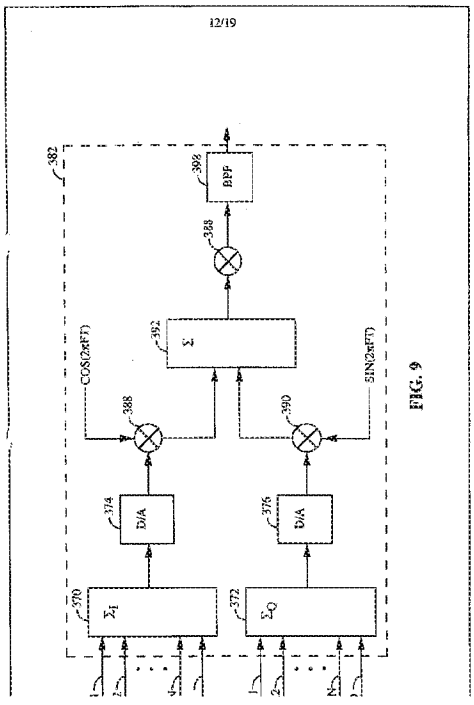

382
398
BPF
388
392
Σ
COS(2πFT)
SIN(2πFT)
386
390
374
D/A
376
D/A
370
372

FIG. 9

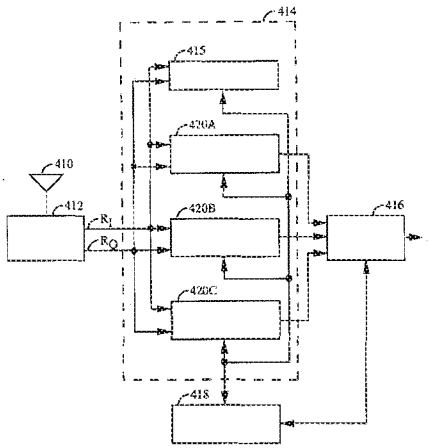


FIG. 10

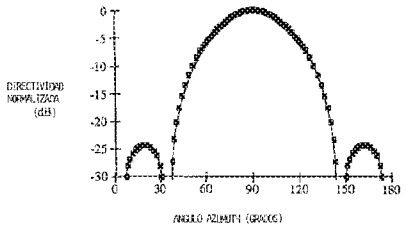


FIG. 11A

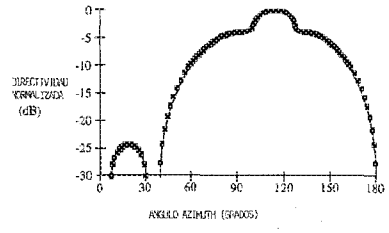
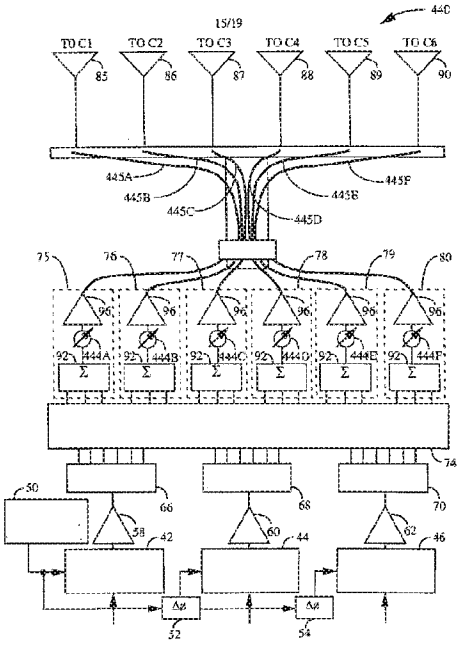


FIG. 11B


15/19
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445C
445D
445E
445F
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76
77
78
79
80
96
92
444A
444B
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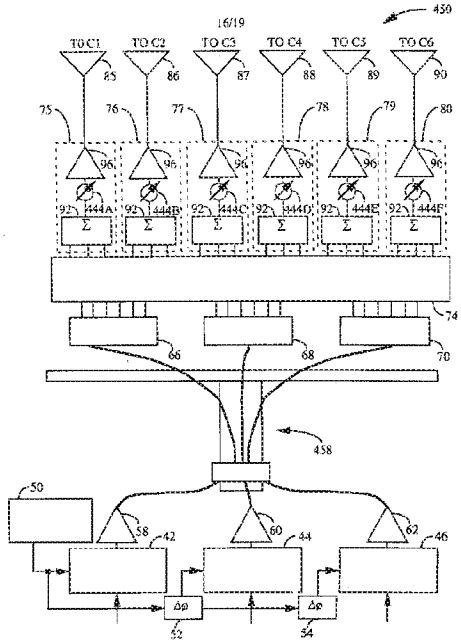
44
46
Δφ
52
54


16/19
450
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TO C3
TO C4
TO C5
TO C6
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86
87
88
89
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76
77
78
79
80
96
92
444A
444B
444C
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46
Δφ
52
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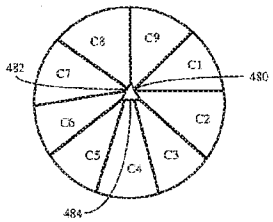


FIG. 14

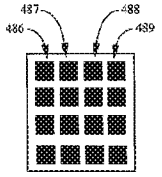
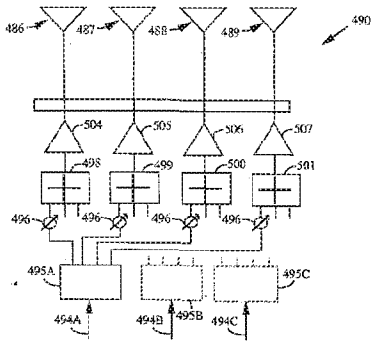


FIG. 15


486
487
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501
496
496
496
496
495A
495C
494A
494B
495B
494C

FIG. 16

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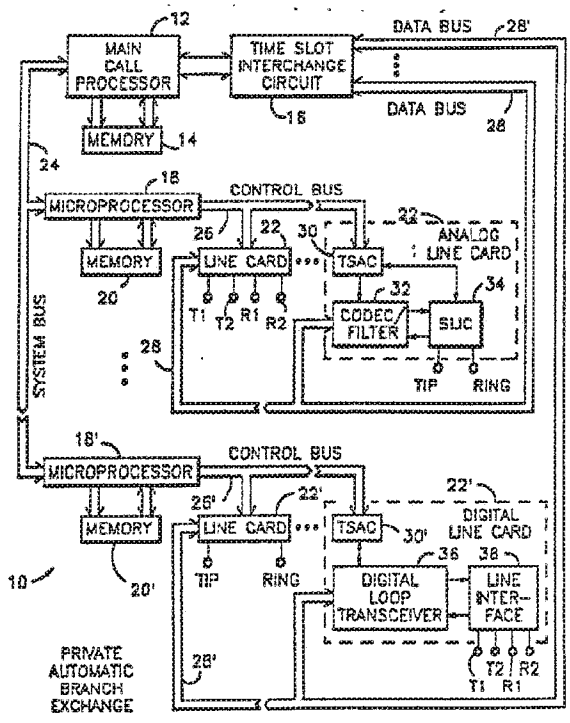
(54) Title: DIGITAL LOOP TRANSCEIVER FOR INTERFACING A DIGITAL PABX TO A DIGITAL SUBSCRIBER SET VIA A SUBSCRIBER LINE

(57) Abstract

In a digital telephone system, a digital private automatic branch exchange (PABX) (10) has a plurality of digital line cards (22-22') for coupling the PABX (10) two respective digital subscriber sets (44) via subscriber lines. In each digital line card (22), a digital loop transceiver (36) operates in a master mode to couple the digital data bus (28') of the PABX (10) to the subscriber line via a subscriber line interface circuit (38) in response to control signals provided by the PABX (10) on the control bus (26') thereof. In each digital subscriber set (44), a digital loop transceiver (36') operates in a slave mode to couple the subscriber set (44) to the subscriber line via a subscriber line interface circuit (38) and to provide the several control signals required by the other components thereof. The digital loop transceivers (36') provide communication on each of two communication channels, with the digital data words of the first channel being treated the same as the digital data words of the second channel.



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DIGITAL LOOP TRANSCEIVER FOR INTERFACING A DIGITAL PABX TO A DIGITAL SUBSCRIBER SET VIA A SUBSCRIBER LINE

Technical Field

This invention relates generally to digital telephone systems and, more particularly, to a digital loop transceiver for use in a digital telephone system comprising a digital PABX and a plurality of digital subscriber sets.

Background Art

When a voice call is made using a conventional analog subscriber set, only a small portion of the frequency spectrum available on the typical subscriber line is utilized. During the development of distributed data processing systems, an effort was made to utilize the existing subscriber line network to facilitate communication of the digital data used by such systems. Various types of modulator/demodulator (modem) devices have been developed to take advantage of the latent capability of the subscriber line network to support digital data communication at data rates significantly greater than that required for analog voice communication. For example, synchronous modems are commercially available which utilize the differential phase shift keyed (DPSK) modulation/demodulation technique to provide data communication at rates up to 9600 baud. However, even in the digital private automatic branch exchanges (PABXs) which support intra-exchange communication of voice information in the form of digital PCM voice data words, the response characteristics of the several analog components of the typical analog line card used therein generally prevent reliable communication at higher rates.

Several techniques have been proposed for providing

higher speed digital data communication between subscribers through such PABXs. However, such proposals typically require the installation of additional pairs of subscriber lines to subscribers requiring the service and/or redesign/modification of the particular PABX to provide the capability to process the pure digital data words in a manner different from the digital PCM voice data words.

Summary of the Invention

Accordingly, it is an object of the present invention to enable digital data words to be communicated at significantly higher speeds over the existing, installed base of subscriber lines, without any redesign or modification whatsoever of the conventional digital PABX.

In accordance with the present invention, the analog to digital conversion function required to support voice communication in the digital PABX is transferred from the PABX to the subscriber set itself, by moving the conventional codec/filter from the analog line card to the subscriber set, and by interfaceing the codec/filter and the PABX to the subscriber line via a pair of digital loop transceivers (DLT) constructed in accordance with the present invention. The existing subscriber line is then converted from the typical, relatively low speed analog link into a high speed data link by providing, at both the subscriber and exchange ends, a subscriber line interface network which is responsive to the much higher frequencies, e.g. up to about 256 kHz, otherwise unavailable on the typical subscriber line.

Once the subscriber set has been converted into a digital form and the existing subscriber line upgraded to a high speed data link in accordance with the present invention, the digital PCM voice data words and associated signalling information for a single voice call will require only about half of the bandwidth available on the

subscriber line. Accordingly, the preferred form of the DLT of the present invention simultaneously supports a second communication channel, with the digital data words and associated signalling information of the second channel being time multiplexed with the digital data words and signalling information of the first channel. However, as far as the DLT is concerned, neither, either or both of these channels may carry PCM voice data words, depending upon the requirements of a given subscriber.

Brief Description of the Drawings

Figure 1 is a block representation of a private automatic branch exchange (PABX) adapted in accordance with the present invention.

Figure 2 is a schematic diagram of an analog line card for use in the PABX of Figure 1.

Figure 3 is a digital line card constructed in accordance with the present invention for use in the PABX of Figure 1.

Figure 4 is a digital subscriber set constructed in accordance with the present invention to communicate over a subscriber line with the digital line card of Figure 3.

Figure 5 is a digital loop transceiver (DLT) constructed in accordance with the present invention for use in the digital line card of Figure 3 and the digital subscriber set of Figure 4.

Figure 6 is a schematic representation of a 4-wire communication system between the DLT in the digital line card of Figure 3 and the DLT in the digital subscriber set of Figure 4.

Figure 7 is a timing diagram illustrating a typical exchange between the DLT in the digital line card of Figure 3 and the PABX of Figure 1.

Figure 8 is a timing diagram illustrating a typical exchange between the DLT in the subscriber set of Figure 4

and the codec/filter therein.

Figure 9 is a schematic representation of a 2-wire communication system between the DLT in the digital line card of Figure 3 and the DLT in the digital subscriber set of Figure 4.

Description of the Preferred Embodiment

Shown in Figure 1 is a conventional private automatic branch exchange (PABX) 10 comprised generally of a main call processor 12 having associated memory 14, a time slot interchange circuit 16, a set of call processing microprocessors 18-18', each having an associated memory 20-20', and a plurality of conventional analog line cards 22. In the illustrated form, the PABX 10 also includes at least two digital line cards 22' constructed in accordance with the present invention.

In a typical digital telephone switching system such as the PABX 10, the main call processor 12 coordinates, via a system bus 24, the call processing activities of each of the several call processing microprocessors 18-18'. In turn, each of the call processing microprocessors 18-18' controls, via respective control buses 26-26', the communication of digital PCM voice data words via respective data buses 28-28' between the several line cards 22 assigned to such microprocessor 18-18'.

In general, each of the analog line cards 22 comprises a time slot assignment and control circuit (TSAC) 30 for selectively enabling a codec/filter 32 to digitally encode an analog voice input signal received via a subscriber line interface circuit (SLIC) 34 from a conventional single channel subscriber set (not shown) coupled to tip and ring conductors for output as a digital pulse code modulation (PCM) voice data word on the respective data bus 28-28', and to decode a digital PCM voice data word received on the data bus 28-28' for output as an analog

voice output signal to the subscriber set (not shown) via the SLIC 34. Shown in Figure 2 is a circuit schematic for such a conventional analog line card 22, using components commercially available from Motorola. The various control and data signals which are provided to or by the line card 22 are generally referred to as the "backplane" of the PABX 10.

In a typical telephone call initiated by a subscriber served by a "source" line card 22 controlled by, say, the call processing microprocessor 18 to a subscriber served by a "destination" line card 22 controlled by, for example, the call processing microprocessor 18', the TSAC 30 on the source line card 22 initially detects via the associated SLIC 34 that the source subscriber set is off hook, and routes the call routing information to the call processing microprocessor 18 for transfer to the main call processor 12. If the destination line card 22 is not indicated in the memory 14 as being busy, the main call processor 12 then requests the call processing microprocessor 18' to notify the destination line card 22 of the call. If, upon providing the system-generated ring signal to the destination subscriber set via the respective SLIC 34, the associated TSAC 30 advises the call processor 18' that the destination subscriber set has been taken off hook, the call processing microprocessor 18' advises the main call processor 12 that the requested connection has been established. During a particular transmit time slot assigned by the main call processor 12, the TSAC 30 on the source line card 22 enables the associated codec/filter 32 to encode the analog voice signal then being received from the source subscriber set via the SLIC 34 for output as a digital PCM voice data word onto the data bus 28. Meanwhile, the main call processor 12 has enabled the time slot interchange circuit 16 to couple the data bus 28 to the data bus 28' to

facilitate the requested intra-exchange communication of the digital PCM voice data word. Simultaneously, the TSAC 30 on the destination line card 22 enables the associated codec/filter 32 to decode the digital PCM voice data word on the data bus 28' for output as an analog voice signal to the destination subscriber set via the SLIC 34. In a similar manner, but during a different receive time slot assigned by the main call processor 12, the destination line card 22 is allowed to encode the analog voice signal received from the destination subscriber set for transmission as a digital PCM voice data word via data bus 28', interchange circuit 16 and data bus 28' to the source line card 22 for decoding and output to the source subscriber set. If this exchange of digital PCM voice data words occurs at a sufficiently high frame rate, say of the order of 8kHz, then it will appear to each of the subscribers that there is a direct analog link between their respective subscriber sets.

In the general form shown in Figure 1, each of the digital line cards 22' comprises a time slot assignment and control circuit (TSAC) 30' for selectively enabling a digital loop tranceiver (DLT) 36 (see Figure 5) to receive digital data words via a subscriber line interface network 38 from a dual channel, digital subscriber set, such as that shown in Figure 4, which is coupled to respective receive and transmit pairs of tip and ring conductors, for direct output on the respective data bus 28-28' in the same manner as the digital PCM voice data words are output by the codec/filter 32 in the analog line cards 22; and to receive digital data words on the data bus 28-28' for direct output to the subscriber set via the subscriber line interface network 38. Shown in Figure 3 is a circuit schematic for the digital line card 22', wherein: the TSAC 30' comprises a pair of the Motorola time slot assignment circuits (TSACs), one for each of the two digital

communication channels the digital line card 22' is capable of simultaneously supporting; the DLT 36 comprises an integrated circuit constructed in accordance with Figure 5; and the subscriber line interface network 38 comprises a transmit isolation transformer 40 coupled to the tip and ring conductors which comprise the receive pair of the subscriber line and a receive isolation transformer 42 coupled to the tip and ring conductors which comprise the transmit pair of the subscriber line. As illustrated in Figure 3, the digital line card 22' responds to and provides the same control and data signals which are provided to or by the analog line card 22 via the backplane of the PABX 10.

Shown in Figure 4 is a dual channel, digital subscriber set 44 constructed in accordance with the present invention. In general, the subscriber set 44 comprises a digital loop transceiver (DLT) 36' (see Figure 5) for receiving digital data words from the digital line card 22' (see Figure 3) via a subscriber line interface network 38' coupled to respective receive and transmit pairs of tip and ring conductors, for output, if digital PCM voice data words, to a conventional codec/filter 32' for subsequent decoding and output as an analog voice output via a voice I/O network 46, or, if digital data words, to a subscriber data processor (not shown) via a data port 48; and for transmitting digital data words provided either by the codec/filter 32' in the form of digital PCM voice data words or by the subscriber data processor in the form of digital data words, to the digital line card 22' via the subscriber line interface network 38'. In the preferred form, the voice I/O network 46 includes a voice input portion 50, and a voice output portion 52; the DLT 36' comprises an integrated circuit constructed in accordance with Figure 5; and the subscriber line interface network 38' comprises a transmit isolation

transformer 40' coupled to the tip and ring conductors which comprise the transmit pair of the subscriber line and a receive isolation transformer 42' coupled to the tip and ring conductors which comprise the receive pair of the subscriber line. In the illustrated form, a conventional tone generator 54, such as the Mostek MK5087, interacts with a dial keypad 56 and the voice I/O network 46 to provide the call routing information required to establish each of the two communication channels, while a conventional hook switch 58 provides call initiation signalling information to the DLT 36'. An audible indication of an incoming call is provided via a ringing transducer 60. A subscriber set power supply 62 derives operating power for the several components of the subscriber set 44 from the subscriber line in a conventional manner.

Shown in Figure 5 is a block diagram of the digital loop transceiver (DLT) 36, constructed in accordance with the present invention. In general, the DLT 36 comprises a digital interface portion 64 for interfacing with the PABX 10 in a master operating mode and with the codec/filter 32 and subscriber data processor in a slave operating mode, a modulator/demodulator portion 66 for transmitting and receiving digital data words via the subscriber line, and a sequencer and control portion 68 for controlling the sequence of operations performed by the digital interface and modulator/demodulator portions 64 and 66, respectively.

In the digital interface portion 64, a receive (RX) control circuit 70 responds to either of two channel receive enable signals, RE1 and RE2, by enabling a receive (RX) register 72 of the shift register type to serially receive digital data bits via a receive (RX) terminal in synchronization with a receive data clock (RDC) on a CLK/RDC terminal. When a predetermined "frame" of data

(see discussion below) has been received, the sequencer and control portion 68 enables the RX register 72 to transfer the "transmit" frame of data in parallel into a transmitter (XMIT) register 74 in the modulator/demodulator portion 66. Simultaneously, the then-current states of the two channel signalling bits on respective S1I and S2I terminals are latched and inserted into the frame of data in the XMIT register 74. Substantially independently, the sequencer and control portion 68 enables a transmit (TX) register 76 to receive a "receive" frame of data in parallel from a receiver (RCV) register 78 in the modulator/demodulator portion 66. Simultaneously, the two channel signalling bits in the receive frame of data are latched and outputted on respective S1O and S2O terminals. In response to either of two channel transmit enable signals, TE1 and TE2, a transmit (TX) control circuit 80 enables the TX register 76 to serially transmit the receive frame of data via a TX terminal in synchronization with a transmit data clock (TDC) on an X1/TDC terminal.

In the modulator/demodulator portion 66, a digital to analog converter (DAC) control circuit 82 periodically enables a digital to analog converter (DAC) 84 to transmit the transmit frame of data in the XMIT register 74 to the transmit transformer 40 in the subscriber line interface network 38 using a differential pair of output drivers 86 and 88 coupled to respective line output terminals LO1 and LO2. In the preferred embodiment, the DAC 84 utilizes a burst differential phase shift keyed (DPSK) modulation technique at a carrier frequency of 256 kHz. Substantially independently, an input buffer 90 of the differential to single ended output type in the modulation/demodulation portion 66 couples the signal received from the receive transformer 42 in the subscriber line interface network 38 via line input terminals LI1 and

LI2 to a sync detector 92 via a window detector 94 and to a correlator 96 via a comparator 98. As phase shifts of the proper form are decoded by the correlator 96, the "decoded" bits are shifted into a shift register portion thereof which maintains the most recently received set of data bits which might constitute a frame. When the energy of a DPSK signal of the proper frame length is detected, the sync detector 92 provides a valid sync signal to enable the correlator 96 to transfer the receive frame of data bits being maintained therein, in parallel to the RCV register 78. A demodulator having a sync detector and correlator of suitable form is shown and described in copending U.S. Patent Application Serial No. 332,408. A switched capacitor bandgap reference 100 similar to that shown and described in copending US Patent Application Serial No. 231,073 provides a precision reference voltage to the DAC 84, the window detector 94, and the comparator 98. Periodically, the offsets of the input buffer 90, the window detector 94, the comparator 98, and the bandgap reference 100 are zeroed by an auto-zero circuit 102 in a manner similar to that shown and described in copending U.S. Patent Application Serial No. 231,079.

In operation, the DLT 36 provides duplex communication of digital data words on a pair of independent channels and a signalling bit associated with each of the channels, between the duplex subscriber line and a digital data port. In a typical line transmission operation, the RX register 72 successively receives a digital data word for each of the channels in synchronization with the receive data clock, with the digital data word for the first of the channels being received from the digital I/O port via the RX terminal in response to the first of the channel receive enable signals, RE1, and the digital data word for the second of the channels being received from the digital

I/O port via the RX terminal in response to the second of the channel receive enable signals, RE2. After the last data bit of the frame has been clocked into the RX register 72, both data words are transferred to the XMIT register 74, and the then-current states of the respective channel signalling bits on the S1I and S2I terminals added to complete the frame. As soon as the frame has been assembled, the DAC control circuit 82 actuates the DAC 84 to serially modulate the first and second digital data words and the respective channel signalling bits in the frame, for transmission via the transmit transformer 40 to one of the pairs of wires in the subscriber line.

In a typical line reception operation, the sync detector 92 monitors the signal received via the receive transformer 42 on the other pair of wires in the subscriber line, and provides a valid sync signal in response to detecting the energy of a DPSK modulated signal of the proper frame length. Meanwhile, the correlator 96 has been serially demodulating the sequentially received bits which might constitute a frame containing a digital data word for each of the channels and the respective channel signalling bits. In response to the valid sync signal, indicating that a valid frame has indeed been received, the correlator 96 transfers the frame to the RCVR register 78. At an appropriate time depending upon the mode of operation, the frame is then transferred from the RCVR register 78 to the TX register 76 and the respective channel signalling bits latched for output on the S1O and S2O terminals. The TX register 76 then sequentially transmits the digital data words in synchronization with the transmit data clock, with the digital data word for the first channel being transmitted to the digital I/O port via the TX terminal in response to the first of the channel transmit enable signals, TE1, and the digital data word for the second channel being

transmitted to the digital I/O port via the TX terminal in response to the second of the channel transmit enable signals, TE2.

Shown in Figure 6 is a schematic representation of a 4-wire or duplex subscriber line which has been coupled at the exchange end thereof to the DLT 36 in the digital line card 22' via the transmit and receive transformers 40 and 42, respectively, and at the subscriber end thereof to the DLT 36' in the digital subscriber set 44 via the transmit and receive transformers 40' and 42', respectively. In the dual-channel form of the duplex system, a frame of data comprises an 8-bit digital data word for the first channel, an 8-bit digital data word for the second channel, and the signalling bits for the first and second channels. Preferably, the frame also includes a parity bit, either even or odd, as desired. A suitable frame format is illustrated in Figure 6.

In the digital line card 22' shown in Figure 3, the DLT 36 is placed in the master mode of operation by a logic high signal on a master/slave (M/S) terminal. In the master mode, the DLT 36 emulates the codec/filter 32 with respect to the backplane by receiving/transmitting the digital data words just like the codec/filter 32, and by responding to the various control signals just like the codec/filter 32. In particular, the RX register 72 successively receives a digital data word for each of the channels in synchronization with the data clock provided by the PABX 10 via the backplane, with the data word for the first channel being received from the backplane via the RX terminal in response to the RE1 signal provided by a respective one of the TSACs 30 during the receive time slot assigned to the first channel, and the data word for the second channel being received from the backplane via the RX terminal in response to the RE2 signal provided by the other TSAC 30 during the receive time slot assigned to

the second channel. In response to the next master sync input (MSI) received via an X2/MSI terminal after the last data bit of the frame has been clocked into the RX register 72, both digital data words are transferred to the XMIT register 74, and the then-current states of the respective channel signalling bits provided via the S1I and S2I terminals by the TSACs 30, respectively, added to complete the frame. As soon as the frame has been assembled, the DAC control circuit 82 actuates the DAC 84 to serially modulate the first and second digital data words and the respective channel signalling bits in the frame, for transmission via the transmit transformer 40 to the receive pair of wires in the subscriber line.

Simultaneously, the sync detector 92 monitors the signal received via the receive transformer 42 on the transmit pair of wires in the subscriber line, and provides the valid sync signal in response to detecting the energy of a DPSK modulated signal of the proper frame length. Meanwhile, the correlator 96 has been serially demodulating the sequentially received bits which might constitute a frame containing a digital data word for each of the channels and the respective channel signalling bits. In response to the valid sync signal, indicating that a valid frame has indeed been received, the correlator 96 transfers the frame to the RCVR register 78. In response to the next MSI, the frame is then transferred from the RCVR register 78 to the TX register 76 and the respective channel signalling bits latched for output on the S1O and S2O terminals. The TX register 76 then sequentially transmits the digital data words in synchronization with the transmit data clock provided by the PABX 10 via the backplane, with the digital data word for the first channel being transmitted to the backplane via the TX terminal in response to the TE1 signal provided by the first one of the TSACs 30 during the transmit time

slot assigned to the first channel, and the digital data word for the second data channel being transmitted to the backplane via the TX terminal in response to the TE2 signal provided by the other TSAC 30 during the transmit time slot assigned to the second channel. A typical sequential interaction of the DLT 36 with the TSACs 30, and with the PABX 10 is illustrated by way of example in the timing diagram of Figure 7.

In the subscriber set 44 shown in Figure 4, the DLT 36' is placed in the slave mode of operation by a logic low on the master/slave (M/S) terminal. In the slave mode, the DLT 36' emulates the functions of the TSAC 30 and the backplane with respect to the codec/filter 32' by providing the digital PCM voice data words and control signals necessary for the codec/filter 32' to operate, and by receiving the digital PCM voice data words provided by the codec/filter 32' just like the backplane. In this mode, the sync detector 92 monitors the signal received via the receive transformer 42' on the receive pair of wires in the subscriber line, and provides the valid sync signal in response to detecting the energy of a DPSK modulated signal of the proper frame length. Meanwhile, the correlator 96 has been serially demodulating the sequentially received bits which might constitute a frame containing a digital data word for each of the channels and the respective channel signalling bits. In response to the valid sync signal, indicating that a valid frame has indeed been received, the correlator 96 transfers the frame to the RCVR register 78. The frame is then promptly transferred from the RCVR register 78 to the TX register 76 and the respective channel signalling bits latched for output on the S10 and S20 terminals. The TX register 76 then sequentially transmits the digital data words in synchronization with a transmit data clock generated by a prescaler and oscillator 104 using a crystal coupled

between the X1/TDC and X2/MSI terminals, with the digital data word for the first channel being transmitted to the codec/filter 32' via the TX terminal in synchronization with a TE1 signal generated by the TX control 80 relative to the last valid sync signal, and the digital data word for the second data channel being transmitted to the data port 48 via the TX terminal in synchronization with a TE2 signal generated by the TX control 80 relative to the last valid sync signal.

In response to each of the valid sync signals provided by the sync detector 92, the RX register 72 successively receives a digital data word for each of the channels in synchronization with a receive data clock generated by the sequencer and control 68, with the digital PCM voice data word for the first channel being received from the codec/filter 32' via the RX terminal in synchronization with an RE1 signal generated by the RX control 70 relative to the last valid sync signal, and the digital data word for the second channel being received from the data port 48 via the RX terminal in response to an RE2 signal generated by the RX control 70 relative to the last valid sync signal. In response to the next valid sync signal provided by the sync detector 92, both digital data words are transferred to the XMIT register 74 and the then-current states of the respective channel signalling bits provided via the S1I and S2I terminals by the hook switch 58 and, if appropriate, the subscriber data processor, respectively, are added to complete the frame. As soon as the frame has been assembled, the DAC control circuit 82 actuates the DAC 84 to serially modulate the first and second digital data words and the respective channel signalling bits in the frame, for transmission via the transmit transformer 40' to the transmit pair of wires in the subscriber line. A typical sequential interaction of the DLT 36' with the codec/filter 32' and the

subscriber data processor is illustrated by way of example in the timing diagram of Figure 8.

Although the DLT 36 is designed to operate primarily in the dual-channel mode over a duplex subscriber line, the DLT 36 may be operated in an exchange which has only one pair of wires in each subscriber line by applying a logic high to a format (FOR) terminal thereof. In the illustrated form of such a 2-wire system shown in Figure 9, the half duplex subscriber line is coupled at the exchange end thereof to the DLT 36 in the digital line card 22' via a transmit/receive isolation transformer 106, and at the subscriber end thereof to the DLT 36' in the digital subscriber set 44 via a transmit/receive isolation transformer 106'. In the dual-channel form of the half duplex system, a frame of data comprises an 8-bit digital data word for the first channel, the signalling bit for the first channel, and a second signalling bit for use by the subscriber data processor as a digital data bit. Preferably, the frame also includes a parity bit, either even or odd, as desired. A suitable frame format is illustrated in Figure 9. Since only a single digital data bit may be transferred in each frame, the effective data bit transmission rate is only 8kHz rather than the 64kHz of the duplex system. However, this reduced data rate may be acceptable in situations where the cost to install the second pair of wires in the subscriber line outweighs the benefits of higher transmission rate.

These and other changes and modifications may be made in the arrangement or construction of the various parts or elements of the preferred embodiments as disclosed herein without departing from the spirit and scope of the present invention as defined in the appended claims.

CLAIMS

1. A digital loop transceiver circuit for providing duplex communication of digital data words on first and second channels and a signalling bit associated with each of said first and second channels, between a duplex subscriber line and a digital I/O port, the transceiver circuit characterized by:

receiver means for successively receiving said first and second of said digital data words and the respective signalling bits in synchronization with a receive data clock, said first digital data word and the respective signalling bit being received from said digital I/O port in response to a first channel receive enable signal, and said second digital data word and the respective signalling bit being received from said digital I/O port in response to a second channel receive enable signal;

modulation means for serially modulating said first and second digital data words and the respective signalling bits for transmission via a first portion of said subscriber line;

sync detection means for detecting a modulated signal on a second portion of said subscriber line, and providing a valid sync signal in response to said detection;

demodulation means for serially demodulating, in response to said valid sync signal, third and fourth of said digital data words and the respective signalling bits received via said second portion of said subscriber line; and

transmitter means for transmitting said third and fourth digital data words and the respective signalling bits in synchronization with a transmit data clock, said third digital data word being transmitted to said digital I/O port in response to a first channel transmit control signal, and said

fourth digital data word being transmitted to said digital data port in response to a second channel transmit control signal.

2. A digital subscriber set having substantially independent voice and data channels, said digital subscriber set characterized by:

voice channel means for periodically providing a digital PCM voice data word representing a digitized voice input signal, and for receiving a digital PCM voice data word for output as a voice output signal;

data channel means for receiving a digital data word provided to said digital subscriber set, and for transmitting from said digital subscriber set a received digital data word;

signalling means for selectively generating call control signals, including a transmit channel signalling bit, for each of said voice and data channels, and for providing an output signal in response to receiving a predetermined receive channel signalling bit for each of said voice and data channels;

subscriber line interface means for coupling said digital subscriber set to transmit and receive portions of a duplex subscriber line; and

the digital loop transceiver means of claim 1 coupled between said subscriber line interface means and said voice channel means, said data channel means and said signalling means.

3. A telecommunication subscriber line interface circuit for coupling a digital switching system having a digital data bus and a control bus via a duplex subscriber line to a digital subscriber set having time multiplexed first and second digital data channels, the interface circuit characterized by:

time slot assignment and control means coupled to said control bus and responsive to control signals received therefrom and to first and second transmit channel signalling bits coupled thereto, for selectively providing first and second receive enable signals during respective first and second receive channel time slots, first and second transmit enable signals during respective first and second transmit channel time slots, and first and second receive channel signalling bits;

subscriber line interface means for coupling said interface circuit to a transmit and a receive portion of said duplex subscriber line; and

the digital loop transceiver means of claim 1 coupled between said subscriber line interface means and said data bus, and to said time slot assignment and control means.

4. A telecommunication subscriber line interface network characterized by a plurality of the digital subscriber sets of claim 2 coupled via respective subscriber lines and respective subscriber line interface circuits of claim 3 to a digital switching system having a digital data bus and a control bus.

5. A digital subscriber set having substantially independent voice and data channels, said digital subscriber set comprising:

voice channel means for periodically providing a digital PCM voice data word representing a digitized voice input signal, and for receiving a digital PCM voice data word for output as a voice output signal;

data channel means for receiving a digital data word provided to said digital subscriber set, and for transmitting from said digital subscriber set a received digital data word;

signalling means for selectively generating call control signals, including a transmit channel signalling bit, for each of said voice and data channels, and for providing an output signal in response to receiving a predetermined receive channel signalling bit for each of said voice and data channels;

subscriber line interface means for coupling said digital subscriber set to transmit and receive portions of a duplex subscriber line; and

digital loop transceiver means coupled between said subscriber line interface means and said voice channel means, said data channel means and said signalling means, characterized by:

sync detection means for detecting a modulated signal on said transmit portion of said subscriber line via said subscriber line interface means, providing a valid sync signal in response to the detection thereof, and providing first and second receive enable signals and first and second transmit enable signals in predetermined relationship to said detection;

demodulation means for serially demodulating, in response to said valid sync signal, a digital PCM voice data word and a digital data word and a receive channel signalling bit associated with each, received from said transmit portion of said subscriber line via said subscriber line interface means;

transmitter means for transmitting said digital PCM voice data word and said digital data word and the respective receive channel signalling bits in synchronization with a data clock developed by said transmitter means, said digital PCM voice data word being transmitted to said voice channel

means in response to said first transmit enable signal, said digital data word being transmitted to said data channel means in response to said second transmit enable signal, and said signalling bits being transmitted to said signalling means;

receiver means for successively receiving a digital PCM voice data word and a digital data word and a transmit channel signalling bit associated with each, in synchronization with said data clock, said digital PCM voice data word being received from said voice channel means in response to said first receive enable signal, said digital data word being received from said data channel means in response to said second receive enable signal, and said transmit channel signalling bits being received from said signalling means; and

modulation means for serially modulating said digital PCM voice data word and said digital data word and the respective transmit channel signalling bits for transmission in response to said valid sync signal to said receive portion of said subscriber line via said subscriber line interface means.

6. A telecommunication subscriber line interface circuit for coupling a digital switching system having a digital data bus and a control bus via a duplex subscriber line to a digital subscriber set having time multiplexed first and second digital data channels, the interface circuit comprising:

time slot assignment and control means coupled to said control bus and responsive to control signals received therefrom and to first and second transmit channel signalling bits coupled thereto, for selectively providing first and second receive

enable signals during respective first and second receive channel time slots, first and second transmit enable signals during respective first and second transmit channel time slots, and first and second receive channel signalling bits;

subscriber line interface means for coupling said interface circuit to a transmit and a receive portion of said duplex subscriber line; and

digital loop transceiver means coupled between said subscriber line interface means and said data bus, and to said time slot assignment and control means, said transceiver characterized by:

receiver means for successively receiving first and second digital data words and the receive channel signalling bit associated with each in synchronization with a receive data clock provided by said switching system, said first digital data word being received from said data bus in response to said first receive enable signal, said second digital data word being received from said data bus in response to said second receive enable signal, and said receive channel signalling bits being received from said time slot assignment and control means;

modulation means for serially modulating said first and second digital data words and the respective receive channel signalling bits for transmission, in response to a sync signal provided by said switching system, to said transmit portion of said subscriber line via said subscriber line interface means;

sync detection means for detecting a modulated signal on said receive portion of said subscriber line via said subscriber line interface means, and for providing a valid sync signal in response

to the detection thereof;

demodulation means for serially demodulating, in response to said valid sync signal, third and fourth digital data words and a transmit channel signalling bit associated with each, received on said receive portion of said subscriber line via said subscriber line interface means; and

transmitter means for transmitting said third and fourth digital data words and the respective transmit channel signalling bits in synchronization with a transmit data clock provided by said switching system, said third digital data word being transmitted to said data bus in response to said first transmit enable signal, said second digital data word being transmitted to said data bus in response to said second transmit enable signal, and said transmit channel signalling bits being transmitted to said time slot assignment and control means.

7. A telecommunication subscriber line interface network comprising:

a digital subscriber set having substantially independent voice and data channels, said digital subscriber set comprising:

voice channel means for periodically providing a digital PCM voice data word representing a digitized voice input signal, and for receiving a digital PCM voice data word for output as a voice output signal;

data channel means for receiving a digital data word provided to said digital subscriber set, and for transmitting from said digital subscriber set a received digital data word;

signalling means for selectively generating call control signals, including a transmit channel

signalling bit, for each of said voice and data channels, and for providing an output signal in response to receiving a predetermined receive channel signalling bit for each of said voice and data channels;

subscriber line interface means for coupling said digital subscriber set to transmit and receive portions of a duplex subscriber line; and

digital loop transceiver means coupled between said subscriber line interface means and said voice channel means, said data channel means and said signalling means, characterized by:

sync detection means for detecting a modulated signal on said transmit portion of said subscriber line via said subscriber line interface means, providing a valid sync signal in response to the detection thereof, and providing first and second receive enable signals and first and second transmit enable signals in predetermined relationship to said detection;

demodulation means for serially demodulating, in response to said valid sync signal, a digital PCM voice data word and a digital data word and a receive channel signalling bit associated with each, received from said transmit portion of said subscriber line via said subscriber line interface means;

transmitter means for transmitting said digital PCM voice data word and said digital data word and the respective receive channel signalling bits in synchronization with a data clock developed by said transmitter means, said digital PCM voice data word being transmitted to said voice channel means in response to said first transmit enable signal, said digital data word being transmitted

to said data channel means in response to said second transmit enable signal, and said signalling bits being transmitted to said signalling means;

receiver means for successively receiving a digital PCM voice data word and a digital data word and a transmit channel signalling bit associated with each, in synchronization with said data clock, said digital PCM voice data word being received from said voice channel means in response to said first receive enable signal, said digital data word being received from said data channel means in response to said second receive enable signal, and said transmit channel signalling bits being received from said signalling means; and

modulation means for serially modulating said digital PCM voice data word and said digital data word and the respective transmit channel signalling bits for transmission in response to said valid sync signal to said receive portion of said subscriber line via said subscriber line interface means; and

a telecommunication subscriber line interface circuit for coupling a digital switching system having a digital data bus and a control bus via said duplex subscriber line to said digital subscriber set, said interface circuit comprising:

time slot assignment and control means coupled to said control bus and responsive to control signals received therefrom and to first and second transmit channel signalling bits coupled thereto, for selectively providing first and second receive enable signals during respective first and second receive channel time slots, first and second transmit enable signals during respective first and

second transmit channel time slots, and first and second receive channel signalling bits;

subscriber line interface means for coupling said interface circuit to a transmit and a receive portion of said duplex subscriber line; and

digital loop transceiver means coupled between said subscriber line interface means and said data bus, and to said time slot assignment and control means, said transceiver comprising:

receiver means for successively receiving first and second digital data words and the receive channel signalling bit associated with each in synchronization with a receive data clock provided by said switching system, said first digital data word being received from said data bus in response to said first receive enable signal, said second digital data word being received from said data bus in response to said second receive enable signal, and said receive channel signalling bits being received from said time slot assignment and control means;

modulation means for serially modulating said first and second digital data words and the respective receive channel signalling bits for transmission, in response to a sync signal provided by said switching system, to said transmit portion of said subscriber line via said subscriber line interface means;

sync detection means for detecting a modulated signal on said receive portion of said subscriber line via said subscriber line interface means, and for providing a valid sync signal in response to the detection thereof;

demodulation means for serially demodulating, in response to said valid sync signal, third and

fourth digital data words and a transmit channel signalling bit associated with each, received on said receive portion of said subscriber line via said subscriber line interface means; and

transmitter means for transmitting said third and fourth digital data words and the respective transmit channel signalling bits in synchronization with a transmit data clock provided by said switching system, said third digital data word being transmitted to said data bus in response to said first transmit enable signal, said second digital data word being transmitted to said data bus in response to said second transmit enable signal, and said transmit channel signalling bits being transmitted to said time slot assignment and control means.

AMENDED CLAIMS
(received by the International Bureau on 21 March 1983 (21.03.83))

1. (Amended) A digital loop transceiver circuit for providing duplex communication of digital data words on first and second channels and a signalling bit associated with each of said first and second channels, between a duplex subscriber line and a digital I/O port, the transceiver circuit characterized by:

receiver means for successively receiving a first and a second of said digital data words and of said signalling bits in synchronization with a receive data clock, said first digital data word and the respective signalling bit being received from said digital I/O port in response to a first channel receive enable signal, and said second digital data word and the respective signalling bit being received from said digital I/O port in response to a second channel receive enable signal;

modulation means for serially modulating said first and second digital data words and the respective signalling bits for transmission via a first portion of said subscriber line;

sync detection means for detecting a modulated signal on a second portion of said subscriber line, and providing a valid sync signal in response to said detection;

demodulation means for serially demodulating, in response to said valid sync signal, a third and a fourth of said digital data words and of said signalling bits received via said second portion of said subscriber line; and

transmitter means for transmitting said third and fourth digital data words and the respective signalling bits in synchronization with a transmit data clock, said third digital data word being transmitted to said digital I/O port in response to

a first channel transmit enable signal, and said fourth digital data word being transmitted to said digital data port in response to a second channel transmit enable signal.

2. (Amended) A digital subscriber set having substantially independent voice and data channels, said digital subscriber set characterized by:

voice channel means for periodically providing a digital PCM voice input data word representing a digitized voice input signal, and for receiving a digital PCM voice output data word for output as a voice output signal;

data channel means for receiving a digital information input data word provided to said digital subscriber set, and for transmitting from said digital subscriber set a received digital information input data word;

signalling means for selectively generating call control signals, including a transmit channel signalling bit, for each of said voice and data channels, and for providing an output signal in response to receiving a predetermined receive channel signalling bit for each of said voice and data channels;

subscriber line interface means for coupling said digital subscriber set to transmit and receive portions of a duplex subscriber line; and

the digital loop transceiver means of claim 1 coupled between said subscriber line interface means and said voice channel means, said data channel means and said signalling means wherein said digital PCM voice input data word, said digital information input data word, said digital PCM voice output data word, and said digital information output data word

comprise said first, second, third and fourth digital data words, respectively, wherein said transmit channel signalling bits comprise said first and second signalling bits, and wherein said receive channel signalling bits comprise said third and fourth signalling bits.

3. (Amended) A telecommunication subscriber line interface circuit for coupling a digital switching system having a digital data bus and a control bus via a duplex subscriber line to a digital subscriber set having time multiplexed first and second digital data channels, the interface circuit characterized by:

time slot assignment and control means coupled to said control bus and responsive to control signals received therefrom and to first and second transmit channel signalling bits coupled thereto, for selectively providing first and second receive enable signals during respective first and second receive channel time slots, first and second transmit enable signals during respective first and second transmit channel time slots, and first and second receive channel signalling bits;

subscriber line interface means for coupling said interface circuit to a transmit and a receive portion of said duplex subscriber line; and

the digital loop transceiver means of claim 1 coupled between said subscriber line interface means and said data bus, and to said time slot assignment and control means, wherein said first and second transmit channel signalling bits comprise said first and second signalling bits and wherein said first and second receive channel signalling bits comprise said third and fourth signalling bits.

4. Cancelled.

5. (Amended) A digital subscriber set having substantially independent voice and data channels, said digital subscriber set characterized by:

voice channel means for periodically providing a digital PCM voice input data word representing a digitized voice input signal, and for receiving a digital PCM voice output data word for output as a voice output signal;

data channel means for receiving a digital information input data word provided to said digital subscriber

set, and for transmitting from said digital subscriber set a received digital information input data word;

signalling means for selectively generating call control signals, including a transmit channel signalling bit, for each of said voice and data channels, and for providing an output signal in response to receiving a predetermined receive channel signalling bit for each of said voice and data channels;

subscriber line interface means for coupling said digital subscriber set to transmit and receive portions of a duplex subscriber line; and

digital loop transceiver means coupled between said subscriber line interface means and said voice channel means, said data channel means and said signalling means, comprising:

sync detection means for detecting a modulated signal on said transmit portion of said subscriber line via said subscriber line interface means, providing a valid sync signal in response to the detection thereof, and providing first and second receive enable signals and first and second transmit enable signals in predetermined relationship to said detection;

demodulation means for serially demodulating, in response to said valid sync signal, a digital PCM voice input data word and a digital output data word and a receive channel signalling bit associated with each, received from said transmit portion of said subscriber line via said subscriber line interface means;

transmitter means for transmitting said digital PCM voice output data word and said digital information input data word and the respective receive channel signalling bits in synchronization with a data clock developed by said transmitter means, said digital PCM voice output data word being transmitted to said voice channel means in response to said first

transmit enable signal, said digital information input data word being transmitted to said data channel means in response to said second transmit enable signal, and said signalling bits being transmitted to said signalling means;

receiver means for successsively receiving a digital PCM voice input data word and a digital information input data word and a transmit channel signalling bit associated with each, in synchronization with said data clock, said digital PCM voice input data word being received from said voice channel means in response to said first receive enable signal, said digital information input data word being received from said data channel means in response to said second receive enable signal, and said transmit channel signalling bits being received from said signalling means; and

modulation means for serially modulating said digital PCM voice input data word and said digital information input data word and the respective transmit channel signalling bits for transmission in response to said valid sync signal to said receive portion of said subscriber line via said subscriber line interface means.

6. (Amended) A telecommunication subscriber line interface circuit for coupling a digital switching system having a digital data bus and a control bus via a duplex subscriber line to a digital subscriber set having time multiplexed first and second digital data channels, the interface circuit characterised by:

time slot assignment and control means coupled to said control bus and responsive to control signals received therefrom and to first and second transmit channel signalling bits coupled thereto, for selectively providing first and second receive

to the detection thereof;

demodulation means for serially demodulating, in response to said valid sync signal, third and fourth digital data words and a transmit channel signalling bit associated with each, received on said receive portion of said subscriber line via said subscriber line interface means; and

transmitter means for transmitting said third and fourth digital data words and the respective transmit channel signalling bits in synchronization with a transmit data clock provided by said switching system, said third digital data word being transmitted to said data bus in response to said first transmit enable signal, said second digital data word being transmitted to said data bus in response to said second transmit enable signal, and said transmit channel signalling bits being transmitted to said time slot assignment and control means.

7. Cancelled.

8. (New Claim) A digital loop transceiver circuit for providing duplex communication of digital data words on first and second channels and a signalling bit associated with said first channel, between a duplex subscriber line and a digital I/O port, the transceiver circuit comprising:

receiver means for successively receiving a first and a second of said digital data words and a first of said signalling bits in synchronization with a receive data clock, said first and second digital data words and said first signalling bit being received from said digital I/O port in response to a channel receive enable signal;

modulation means for serially modulating said first and second digital data words and said signalling bit for transmission via a first portion of said subscriber line;

sync detection means for detecting a modulated signal on a second portion of said subscriber line, and providing a valid sync signal in response to said detection;

demodulation means for serially demodulating, in response to said valid sync signal, a third and a fourth of said digital data words and a second of said signalling bits received via said second portion of said subscriber line; and

transmitter means for transmitting said third and fourth digital data words and said second signalling bit in synchronization with a transmit data clock, said third and fourth digital data words being transmitted to said digital I/O port in response to first channel transmit enable signal.

9. (New Claim) A digital subscriber set having substantially independent voice and data channels, said digital subscriber set comprising:

voice channel means for periodically providing a digital PCM voice input data word representing a digitized voice input signal, and for receiving a digital PCM voice output data word for output as a voice output signal;

data channel means for receiving a digital information input data word provided to said digital subscriber set, and for transmitting from said digital subscriber set a received digital information output data word;

signalling means for selectively generating a call control signal, including a transmit channel

signalling bit, for said voice channel, and for providing an output signal in response to receiving a predetermined receive channel signalling bit for said voice channel;

subscriber line interface means for coupling said digital subscriber set to transmit and receive portions of a duplex subscriber line; and

the digital loop transceiver means of claim 10 coupled between said subscriber line interface means and said voice channel means, said data channel means and said signalling means, wherein said digital PCM voice input data word, said digital information input data word, said digital PCM voice output data word, and said digital information output data word comprise said first, second, third and fourth digital data words, respectively, wherein said transmit channel signalling bit comprises said first signalling bit, and wherein said receive channel signalling bit comprises said second signalling bit.

10. (New Claim) A digital loop transceiver circuit for providing duplex communication of digital data words on a channel and a signalling bit associated with said channel, between a duplex subscriber line and a digital I/O port, the transceiver circuit comprising:

receiver means for successively receiving a first of said digital data words and a first of said signalling bits in synchronization with a receive data clock, said first digital data word and said first signalling bit being received from said digital I/O port in response to a channel receive enable signal;

modulation means for serially modulating said first digital data word and said first signalling bit for transmission via a first portion of said subscriber

line;
sync detection means for detecting a modulated signal on a second portion of said subscriber line, and providing a valid sync signal in response to said detection;
demodulation means for serially demodulating, in response to said valid sync signal, a second of said digital data words and a second of said signalling bits received via said second portion of said subscriber line; and
transmitter means for transmitting said second digital data word and said second signalling bit in synchronization with a transmit data clock, said second digital data word being transmitted to said digital I/O port in response to a channel transmit enable signal.

11. (New Claim) A digital subscriber set comprising:
voice channel means for periodically providing a digital PCM voice input data word representing a digitized voice input signal, and for receiving a digital PCM voice output data word for output as a voice output signal;
signalling means for selectively generating a call control signal, including a transmit channel signalling bit, for said voice channel and for providing an output signal in response to receiving predetermined receive channel signalling bit for said voice channel;
subscriber line interface means for coupling said digital subscriber set to transmit and receive portions of a duplex subscriber line; and
the digital loop transceiver means of claim 10 coupled between said subscriber line interface means and said voice channel means, wherein said digital PCM

voice input data word and said digital PCM voice output data word comprise said first and second digital data words, respectively, wherein said transmit channel signalling bit comprises said first signalling bit, and wherein said receive channel signalling bit comprises said second signalling bit.

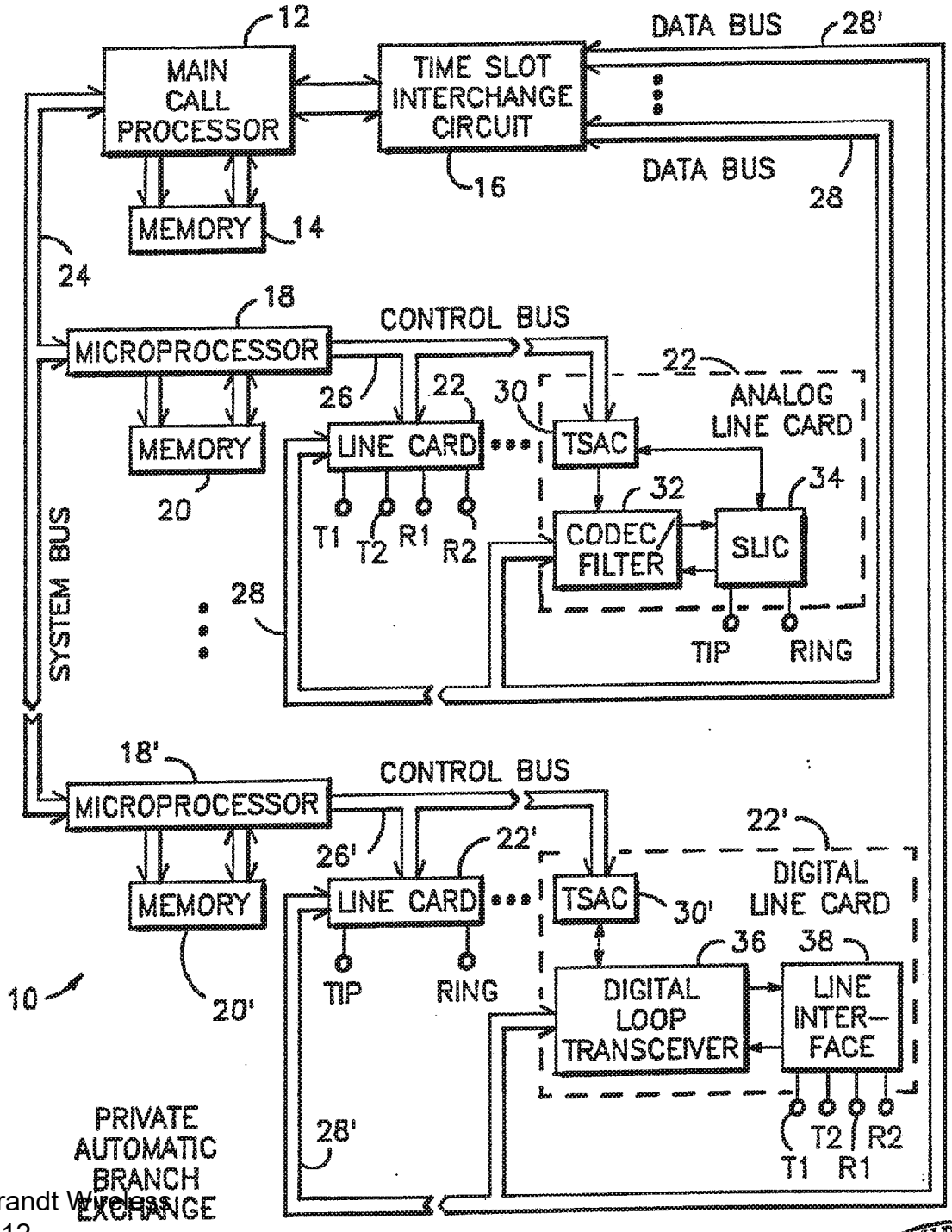
12. (New Claim) A telecommunication subscriber line interface circuit for coupling a digital switching system having a digital data bus and a control bus via a duplex subscriber line to a digital subscriber set, the interface circuit comprising:

time slot assignment and control means coupled to said control bus and responsive to control signals received therefrom and to a transmit channel signalling bit coupled thereto, for selectively providing a receive enable signal during a receive channel time slot, a transmit enable signal during a transmit channel time slot, and a receive channel signalling bit;

subscriber line interface means for coupling said interface circuit to a transmit and a receive portion of said duplex subscriber line; and

the digital loop transceiver means of claim 10 coupled between said subscriber line interface means and said data bus, and to said time slot assignment and control means, wherein said transmit channel signalling bit comprises said first signalling bit, and wherein said receive channel signalling bit comprises said second signalling bit.

Fig. 1



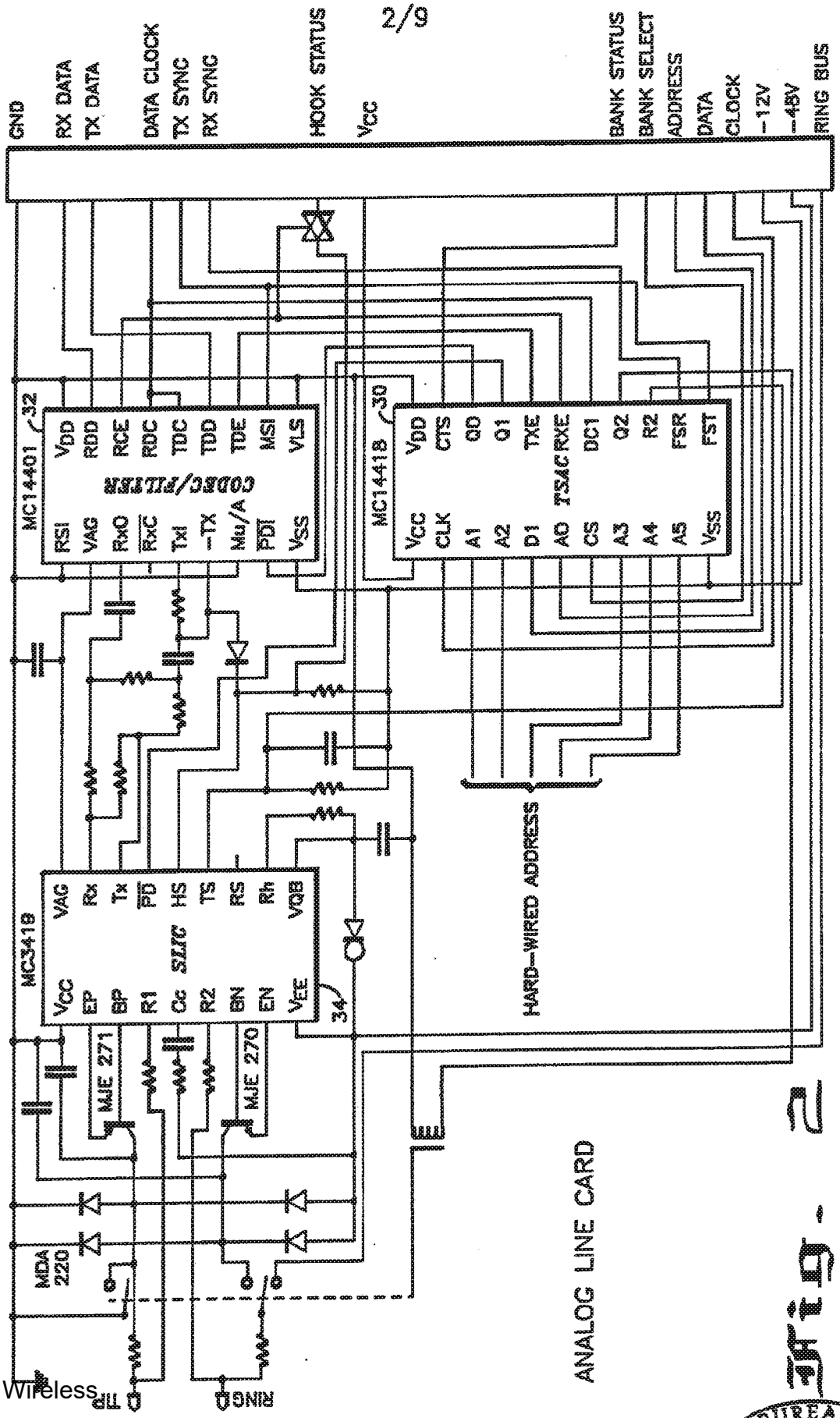
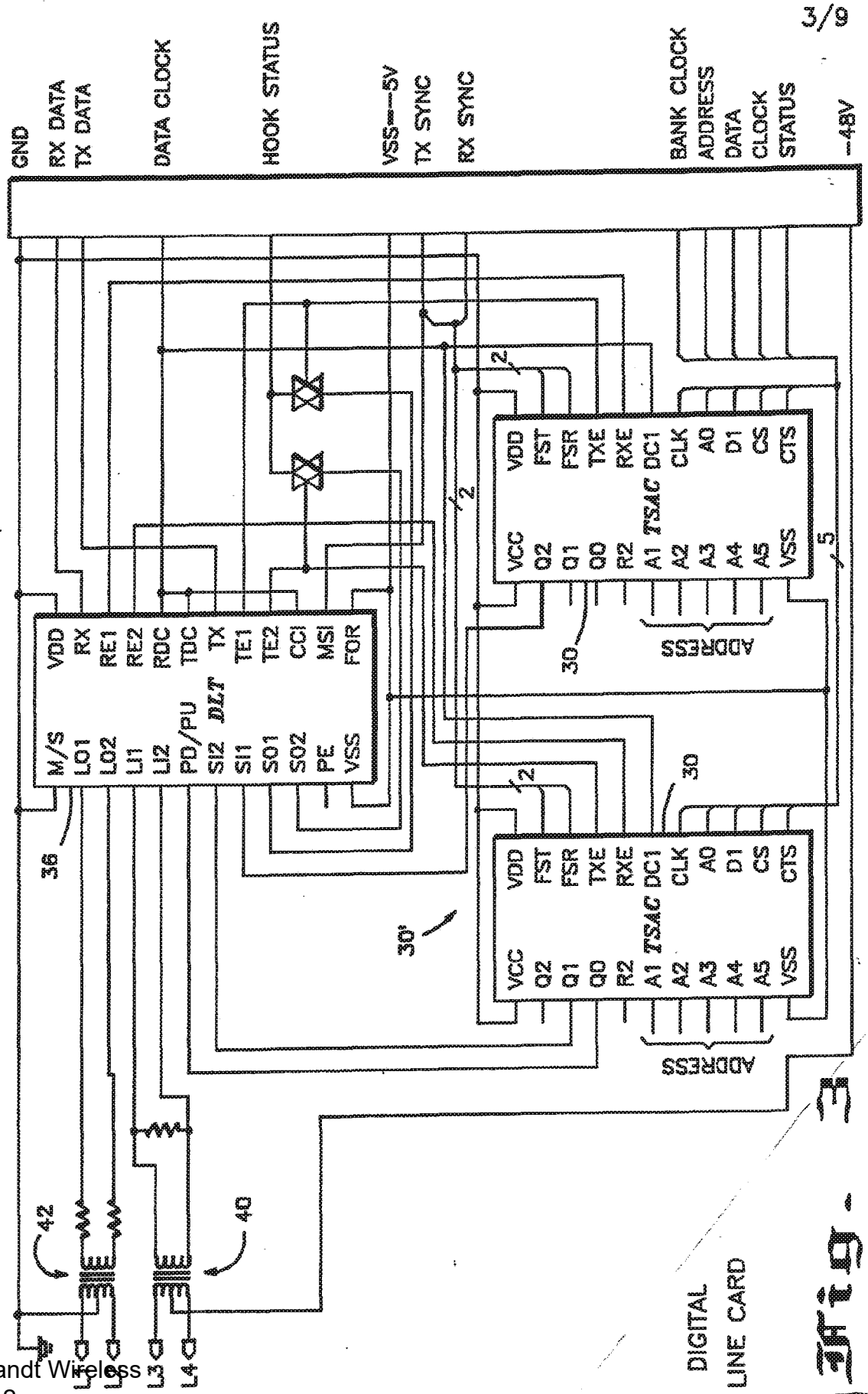


Fig. 2


GND
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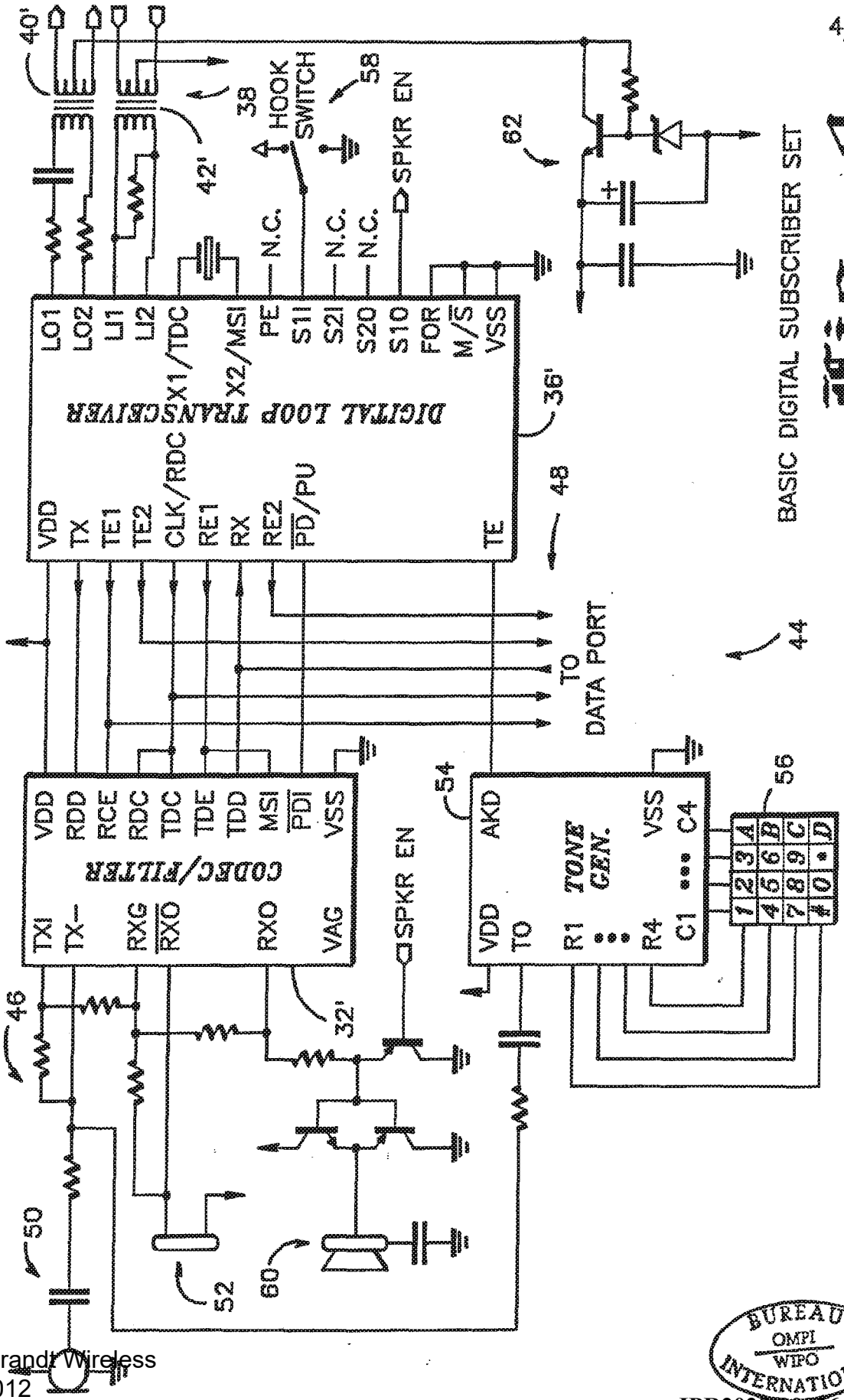
TX DATA
DATA CLOCK
HOOK STATUS
VSS—5V
TX SYNC
RX SYNC
BANK CLOCK
ADDRESS
DATA
CLOCK
STATUS
-48V
VDD FST FSR TXE RXE DC1 CLK A0 D1 CS CTS
VCC Q2 Q1 Q0 R2 A1 TSAC A2 A3 A4 A5 VSS
ADDRESS
30
30'
36
VDD RX RE1 RE2 RDC TDC TX TE1 TE2 CCI MSI FDR
M/S LO1 LO2 LI1 LI2 PD/PU SI2 DLT SI1 SO1 SO2 PE VSS
42
40
L1
L2
L3
L4
DIGITAL
LINE CARD
FIG. 3



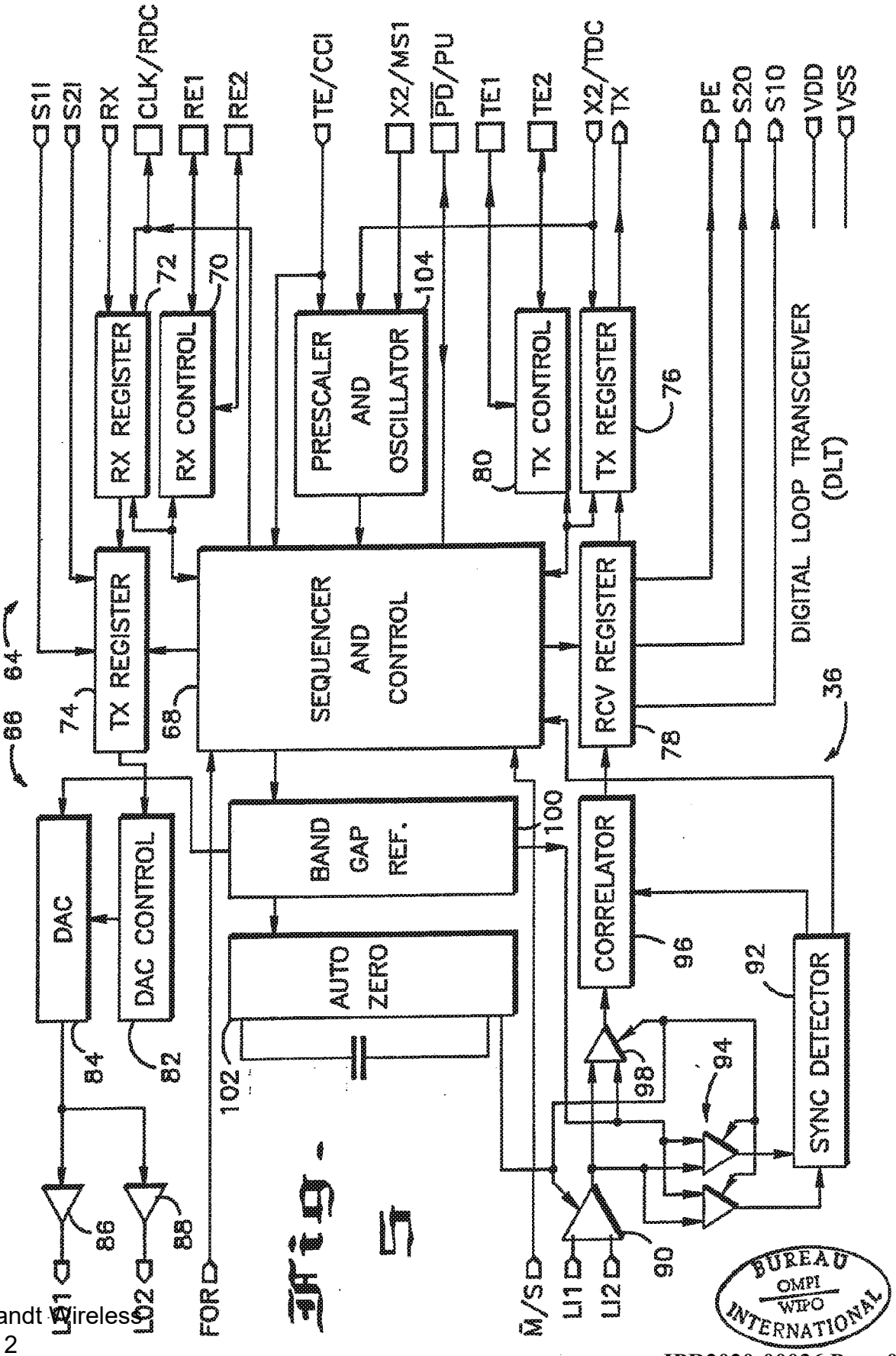


Fig. 5

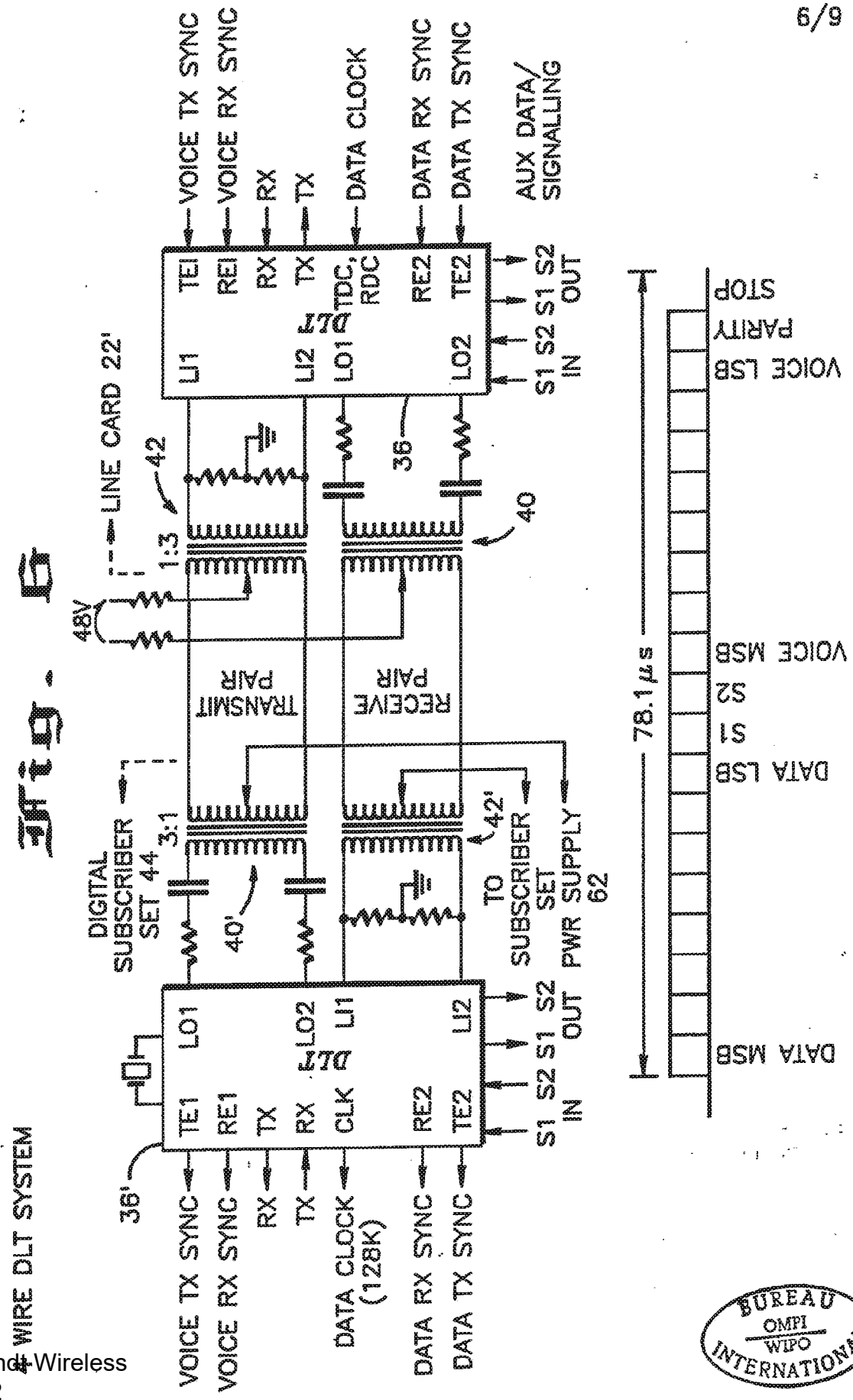


Fig. 5

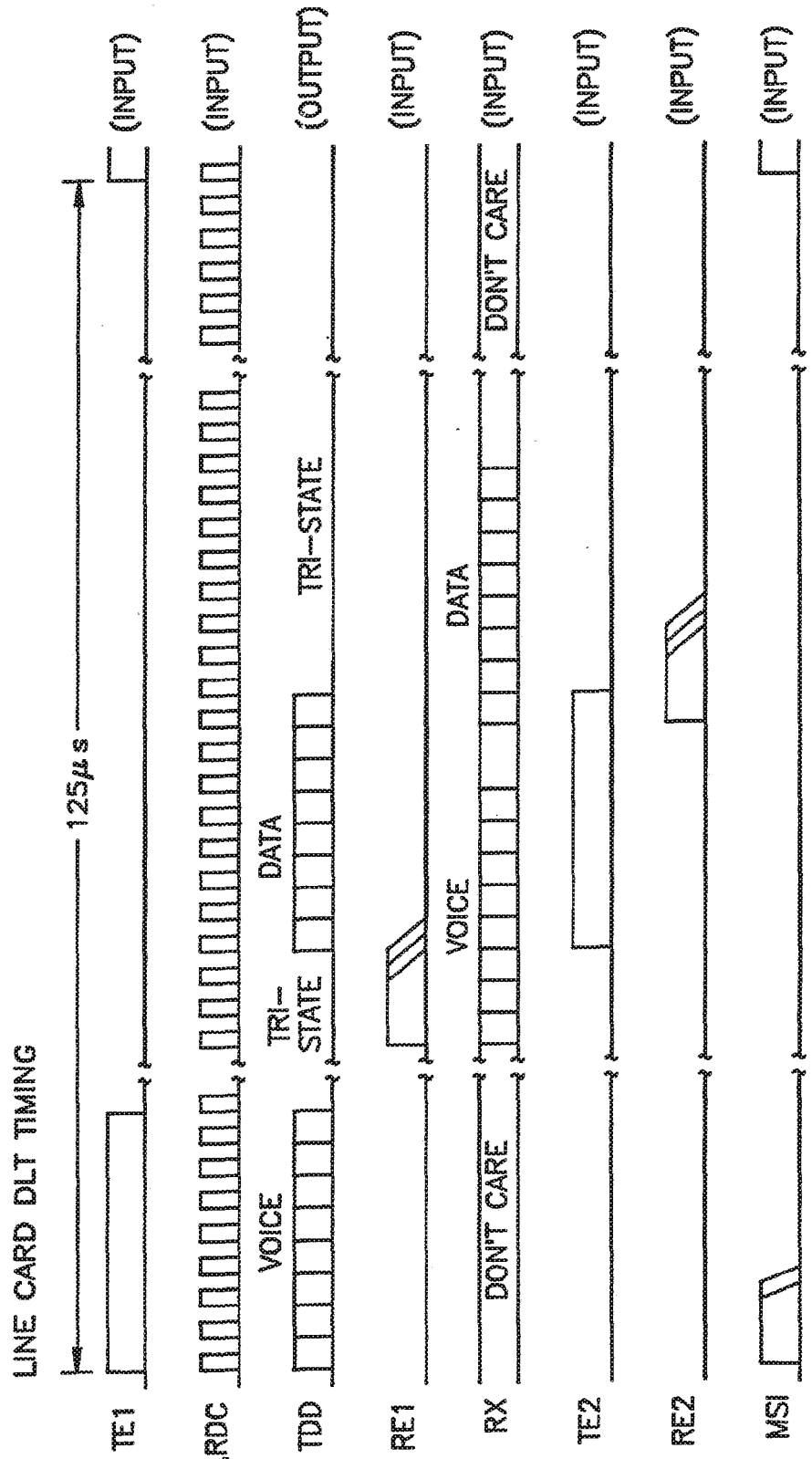


Fig. 7

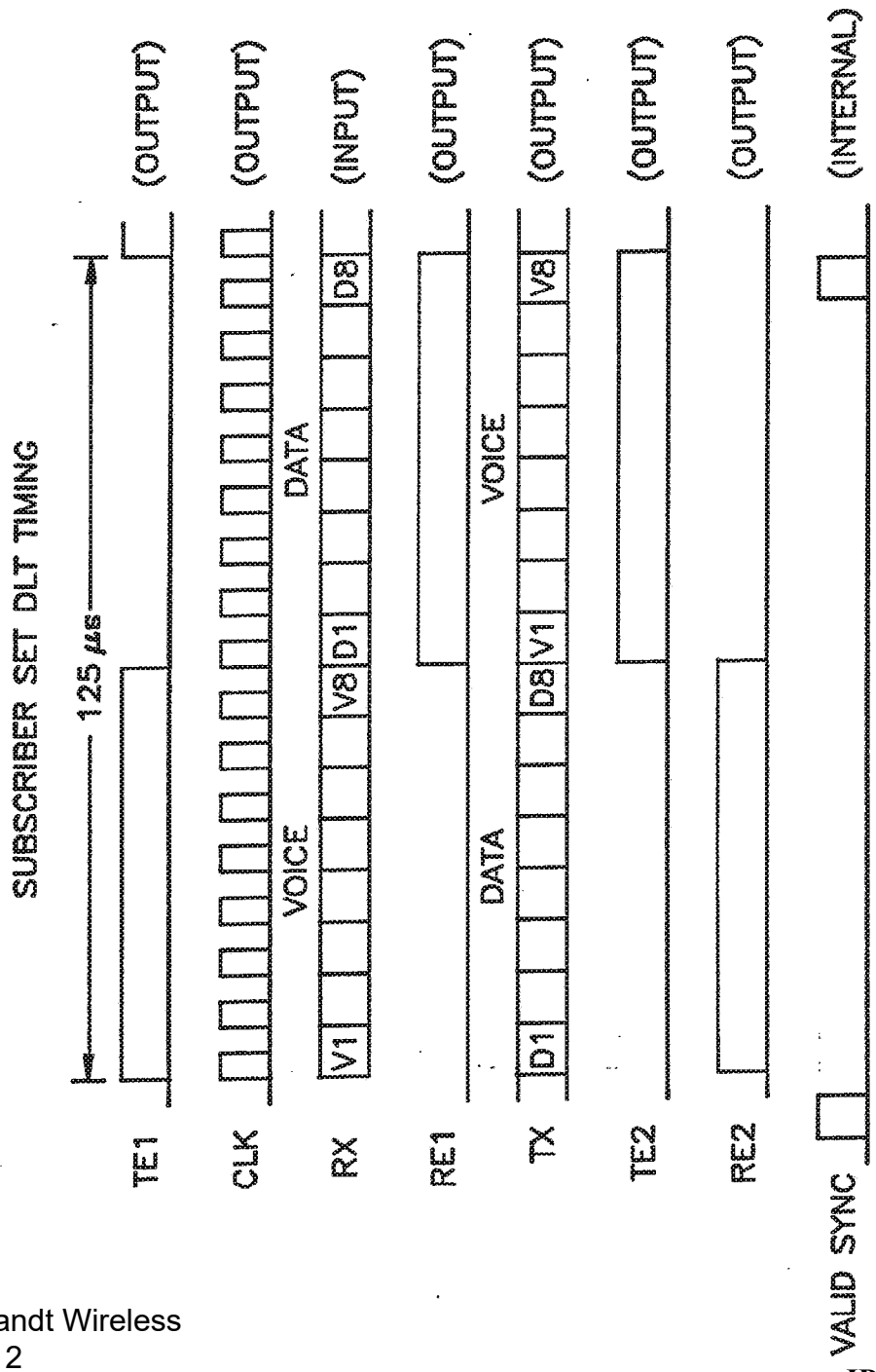


Fig. 8

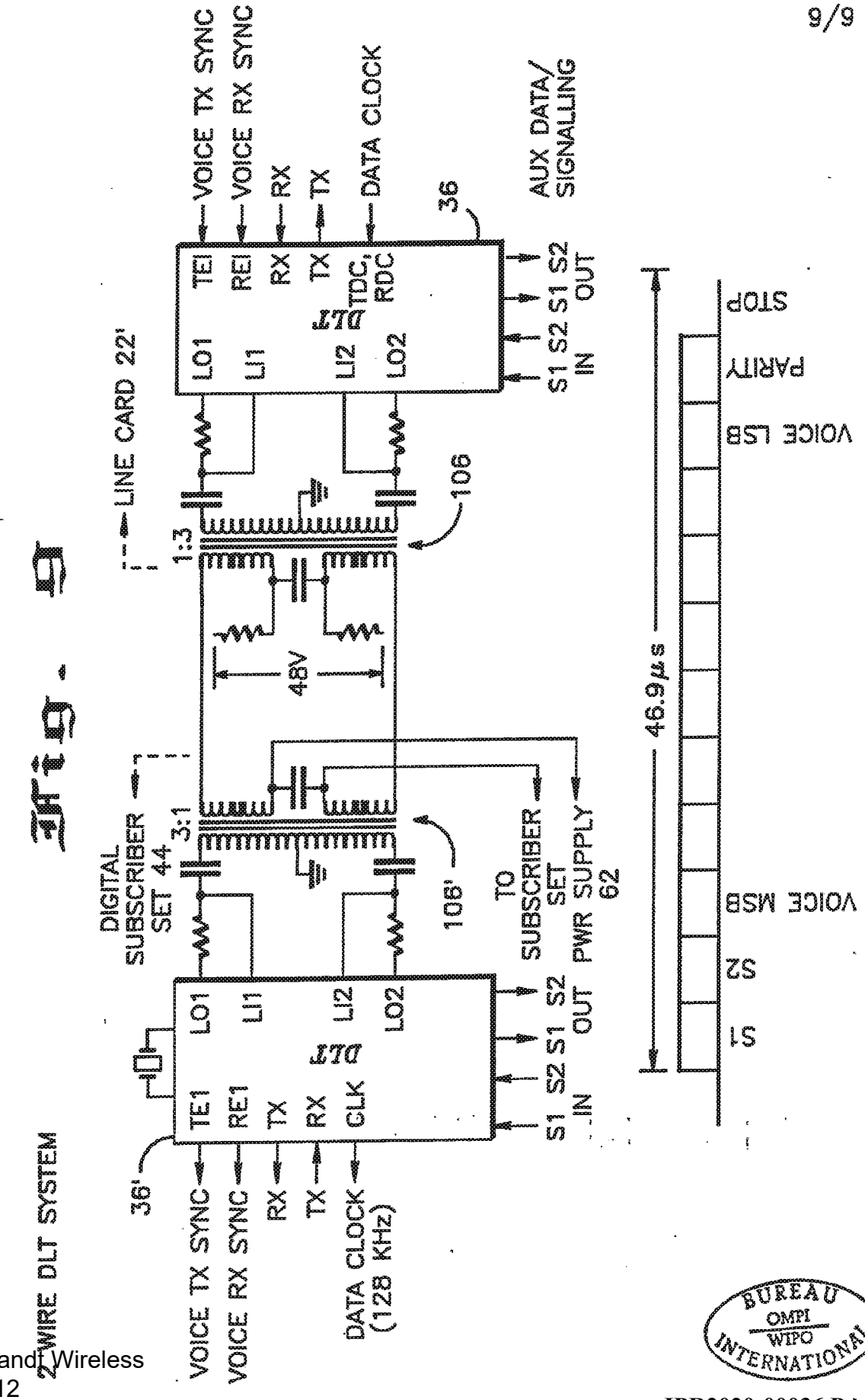


Fig. 9

INTERNATIONAL SEARCH REPORT

International Application No PCT/US82/01435

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.3 H 04 Q 5/20, H 04 M 9/00
U.S. CL. 370/29, 179/18 AD

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	370/24,29,110.1,77 179/18AD,99M

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	International Conference on Communications, IEEE, June 1980, P.K. Desikan and M.K. Warner, "A Data Switching Technique For A Digital PBX"	1-7
A.	US,.A, 3,924,077, Published 02 December, 1975 Blakeslee	1-7
A.	US, A, 3,978,290, Published 31 August, 1976 Sarma	1-7
A	US, A, 4,145,574, Published 20 March, 1979 Wintzer	1-7
A	US, A, 4,281,410, Published 28 July, 1981 Agricola et al	1-7

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IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
1-11/83	21 JAN 1983
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	Gerald J Boyer

Form PCT/ISA/210 (second sheet) (October 1981)

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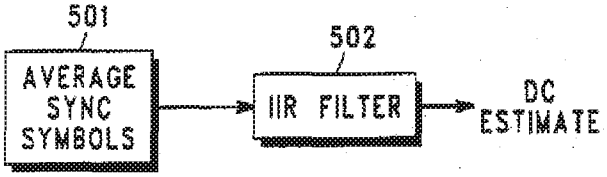
(74) Agents: PARMELEE, Steven, G. et al.; Motorola, Inc., Intellectual Property Dept., 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(81) Designated States: AT (European patent), BE (European patent), CA, CH (European patent), DE (European patent)*, DK (European patent), ES (European patent), FR (European patent), GB (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent).

Published
With international search report.

(54) Title: METHOD OF DC OFFSET COMPENSATION USING A TRANSMITTED DC COMPENSATION SIGNAL



(57) Abstract

A DC offset compensation method that makes use of a received DC compensation signal (107) having a known average value, such as zero. Differences between the known average value and the actually received average value are utilized to calculate a DC compensation value suitable for use in compensating subsequently received data information.

* See back of page

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METHOD OF DC OFFSET COMPENSATION USING A TRANSMITTED DC COMPENSATION SIGNAL

Technical Field

This invention relates generally to DC offset compensation of received data signals.

Background of the Invention

Transmission of data signals through various mediums is known in the art (as used herein, "data" refers to binary or multilevel signalling, as versus analog signal waveforms). When receiving such a signal, it is not uncommon for a varying DC component to become combined therewith and possibly distort data recovery.

To compensate for this, various DC offset compensation methodologies have been proposed. Although at least some of these prior art approaches can be implemented in a digital signal processor (DSP), such implementations require a relatively significant portion of the processing capacity of the DSP. This, in turn, increases current drain requirements for the DSP and/or limits availability of the DSP for support of other desired functions.

Accordingly, a need exists for a method of DC offset compensation that will substantially reliably compensate for DC offset in a received data signal, and that may be implemented, if desired, in a DSP without over burdening the processing capacity of the DSP.

Brief Description of the Drawings

Fig. 1 comprises a timing diagram of a communication resource format implemented in accordance with the invention;

Fig. 2 comprises a depiction of a sync word waveform in accordance with the invention;

Fig. 3 comprises a block diagram of a receiver constructed in accordance with the invention;

Fig. 4 comprises a depiction of a received sync word; and

Fig. 5 comprises a block diagram depiction of a part of the DSP operation when programmed in accordance with the invention.

Best Mode For Carrying Out The Invention

For purposes of this description, an embodiment of the invention will be described in conjunction with a time division multiplexed (TDM) communication resource. In this particular example, the frequency is subdivided into time frames, wherein each time frame is further subdivided into four time slots (101) (Fig. 1). In a given time frame, two of the time slots (102) are used for the transmission of binary signalling information relevant to the allocation of the voice time slots (103) and other system control information.

Each control slot (102) in turn includes space for four commands (104), a slot designation (106), and a sync word (107).

In this embodiment, the sync word (107) is comprised of the hex word zero nine D seven (09D7) (see Fig. 2). In binary form, as represented in Fig. 2, this equates with the sequential transmission of: 0000100111010111. Since this particular sync word, when represented in binary form, includes eight zeroes and eight ones, the average value of the sync word equals zero.

In this embodiment, it will be presumed that the constituent elements of the sync word will be transmitted in a predetermined order, as set forth above, with each broadcast. In a particular application, however, such a requirement may not be necessary. Also, in this particular embodiment, the average value of the sync word elements equals zero, and the importance of this will be made more clear below. (Other elements could perhaps be used in an appropriate application, wherein the average value would not equal zero. What would be important in such an application, however, is that both the average value of the constituent elements of the sync word be predetermined and known to the receiver, and that the system gain also be known to the receiver, since this gain would scale the non-zero average value.)

A receiver (300) (Fig. 3) suitable for practicing the method of the invention will now be described. This receiver (300) includes an antenna (301) for receiving the signalling information (302) transmitted to it, including the data sync words (107). These signals (302)

are processed in an appropriate RF unit (303) and reduced to baseband. An analog to digital convertor (304) then digitizes this representation, and provides the digitized representation to a DSP (306) (such as a 56000 family device as manufactured and sold by Motorola, Inc.) where the signal can be demodulated and processed as desired. Voice transmissions received and processed in this way can then be reconverted to analog form by a digital to analog convertor (307), and the resulting audio signal (308) can be further processed and amplified as appropriate to the particular application.

The receiver (300) further includes a processing unit (309) to control the operation of the RF unit (303) and of the DSP (306). In addition, the processing unit (309) can receive and process recovered signalling information from the DSP (306). Also, an appropriate clock (311) provides necessary clock signals to the DSP (306) and processing unit (309), as may be appropriate to the particular application.

So configured, signals (302) received by the receiver can be processed in various programmable ways in the DSP (306). Such configurations, of course, are known in the art. In this particular embodiment, however, the DSP (306) processes samples (401) of the received sync word (107) (see Fig. 4) at various times. The anticipated time of arrival of the sync word (107), and the constituent elements and order thereof, are of course known to the receiver (300). Therefore, by comparing an average of the sampled values with the value that the receiver (300) would expect to find, the DSP (306) can calculate the difference. These differences can then be used to calculate a DC

compensation value suitable for use with subsequently received data.

In particular, the offset values calculated for this sync word, and also for previously received sync words, can effectively be averaged over time (501 and 502) (see Fig. 5) in the DSP to provide an estimated DC compensation value. As indicated earlier, this DC compensation value can then be used by the DSP to compensate for DC offset in subsequently received data information.

So configured, the DSP (306) is spared the necessity of constantly monitoring the received signal in support of an ongoing DC offset compensation calculation. Instead, by providing for reception of a sync word that effectively also operates as a DC compensation signal, having a substantially known average value, the DSP need only occasionally calculate a substantially reliable DC compensation value that can be used for DC compensation purposes.

What is claimed is:

Claims

1. A method of DC compensating a received signal, characterized by the steps of:

A) receiving a DC compensation signal having a substantially known average value;

B) calculating a DC compensation value using the DC compensation signal.

2. The method of claim 1 wherein the known average value is approximately zero.

3. The method of claim 1 wherein the DC compensation signal comprises a data packet.

4. The method of claim 3 wherein the data packet includes a binary representation of 0, 9, D, and 7.

5. The method of claim 4 wherein the binary representations of 0, 9, D, and 7 are organized in a predetermined manner.

6. The method of claim 3 wherein the known average value of the data packet is zero.

7. The method of claim 1 and further characterized by the steps of:

A) receiving subsequent non-DC compensation signals;

B) using the DC compensation value to DC compensate the non-DC compensation signals.

8. The method of claim 7 wherein the known average value is approximately zero.

9. The method of claim 7 wherein the DC compensation signal comprises a data packet.

10. The method of claim 9 wherein the data packet includes a binary representation of 0, 9, D, and 7.

11. The method of claim 10 wherein the binary representations of 0, 9, D, and 7 are organized in a predetermined manner.

12. The method of claim 9 wherein the known average value of the data packet is zero.

1/1

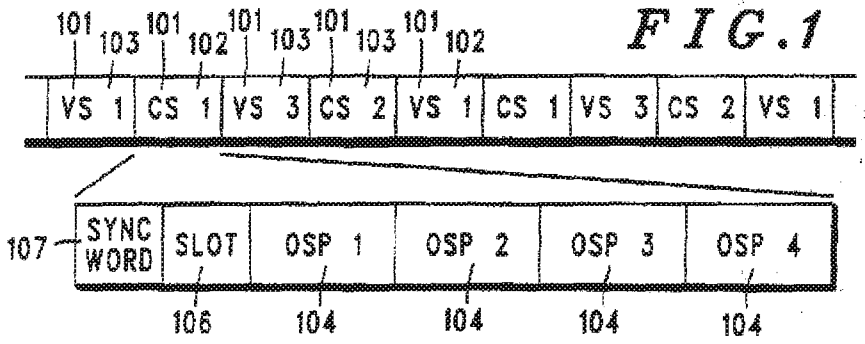


FIG. 1

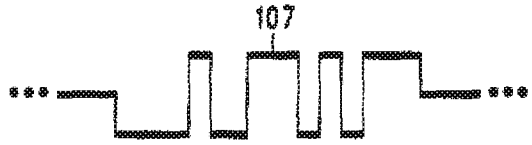


FIG. 2

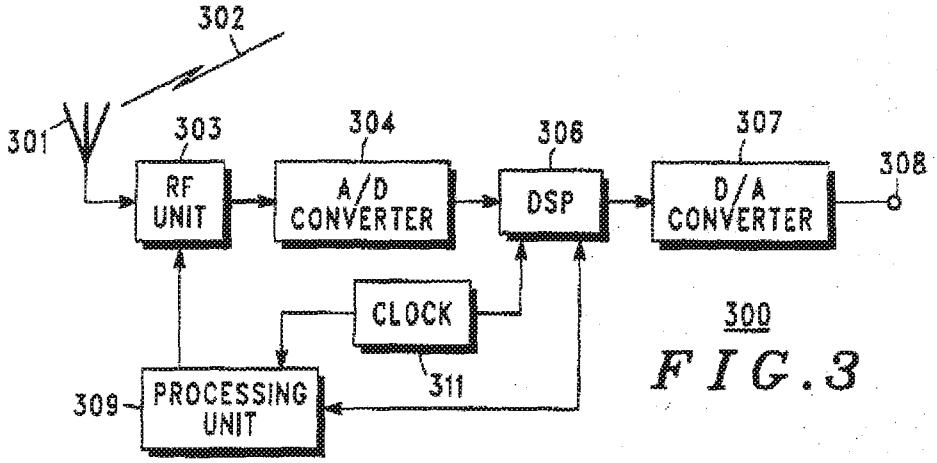
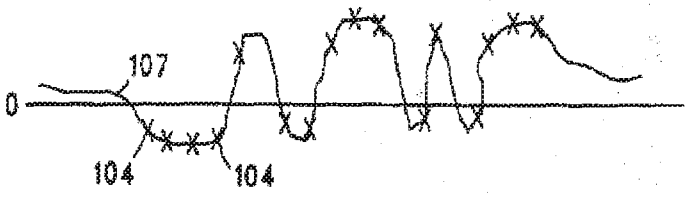


FIG. 3

FIG. 4



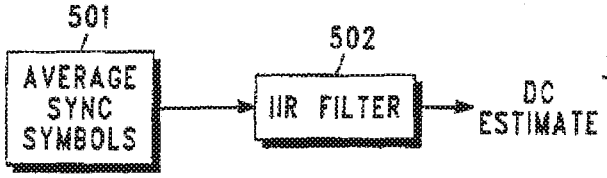


FIG. 5

INTERNATIONAL SEARCH REPORT

International Application No PCT/US90/05358

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) 3

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (5) : H04L 25/06,25/10
U.S. Cl : 375/36

II. FIELDS SEARCHED

Minimum Documentation Searched 4

Classification System	Classification Symbols
U.S.	375/19; 358/171; 307/491; 328/168,173; 330/11

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched 5

III. DOCUMENTS CONSIDERED TO BE RELEVANT 14

Category *	Citation of Document, 16 with indication, where appropriate, of the relevant passages 17	Relevant to Claim No. 18
X / Y P	US,A 4,873,702 (CHIU) 10 October 1989 See the Abstract and Figure 2.	1 & 7 / 2-6 & 8-12
Y	US,A 4,387,364 (SHIROTA) 07 June 1983 See Figures 4-7.	2-6 & 8-12

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IV. CERTIFICATION

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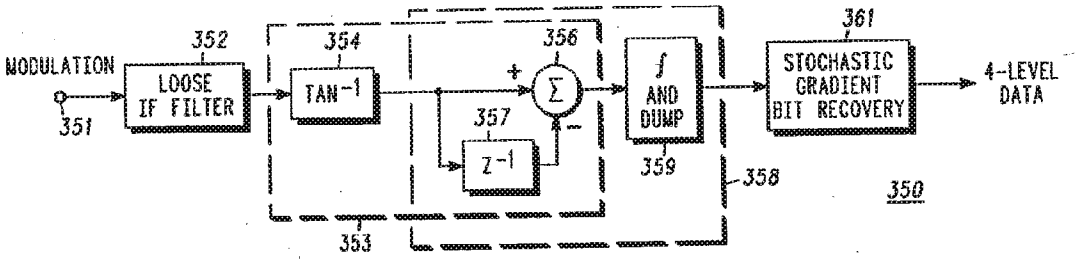

(57) Abstract

A receiver (350) compatible with both wide channel constant envelope 4 level FSK FM modulation and narrow channel $\pi/4$ differential QPSK linear modulation allows compatible interaction between modified constant envelope and non-constant envelope transmitters (300). All Nyquist filtering occurs in the transmitters (300), and none in the receiver (350).

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MULTI-MODULATION SCHEME COMPATIBLE RADIO

Technical Field

This invention relates generally to modulation techniques, including but not limited to constant envelope modulation techniques and non-constant envelope modulation techniques, and transmitters and receivers suitable for use therewith.

Background of the Invention

Various modulation techniques are known to support radio communications. For example, constant envelope modulation techniques, such as frequency modulation (FM), are well known and understood. Non-constant envelope modulation techniques, such as $\pi/4$ differential QPSK, are also known.

Digital signalling techniques suitable for use with various modulation schemes are also known, such as $\pi/4$ differential QPSK (noted above) and 4 level FSK as used with FM. Although both techniques are well understood, present technology readily supports rapid introduction of 4 level FSK FM based radios, whereas $\pi/4$ differential QPSK based non-constant envelope radios pose a greater challenge. Although the various barriers to fielding a

technologically and economically viable platform to support such signalling and modulation will no doubt exist in the near term future, users who require digital signalling will typically find 4 level FSK FM a more likely candidate for relatively immediate implementation.

Radio system users greatly desire immediate availability of digital signalling, in part for reasons of spectral efficiency, and in part to support various desired operating features. These same users, however, do not wish to invest in currently available technology at the expense of being either foreclosed from next generation advances, or at the expense of eliminating a currently acquired digital signalling system in favor of a next generation platform. In short, system users do not wish to acquire a 4 level FSK FM system to serve immediate needs, with the likely availability of $\pi/4$ differential QPSK radios in the future. At the same time, however, these same users want to realize the benefits of digital signalling now.

Accordingly, a need exists for some communications approach that will satisfy the current need for digital signalling, such as 4 level FSK FM, and yet viably accommodate likely future technologies, such as $\pi/4$ differential QPSK, in a cost effective manner.

Summary of the Invention

This need and others are substantially met through provision of a radio transceiver, which transceiver includes a transmitter having a Nyquist filter, and a corresponding receiver that does not include a Nyquist filter.

In one embodiment, the transmitter may be configured to transmit either a constant envelope signal, or a non-constant envelope signal, depending upon the intent of the designer. The receiver, however, functions to receive and properly demodulate either a constant envelope signal or a non-constant envelope signal. So provided, a system can accommodate a plurality of users, wherein some of the users transmit constant envelope signals and other users transmit non-constant envelope signals. Regardless of the transmission type, however, all radios are capable of receiving and demodulating all signals.

So provided, constant envelope transmitters can be coupled with the above receiver to allow provision of 4 level FSK radios to meet near term needs. Later, as economic issues are resolved, radios having $\pi/4$ differential QPSK transmitters can be introduced into the system. A system operator is therefore provided with radios that meet immediate needs, while yet retaining a compatible migration path that readily accommodates a next generation platform.

In one embodiment, the constant envelope signal and the non-constant envelope signal can occupy differing spectral bandwidths. Notwithstanding this difference, the receiver can yet receive and properly demodulate both signals.

Brief Description of the Drawings

FIGS. 1a-b comprise block diagram depictions of prior art 4 level FSK FM transmitter and receiver structures;

FIGS. 2a-b comprise block diagram depictions of prior art π/4 differential QPSK transmitter and receiver structures;

FIGS. 3a-c comprise block diagram depictions of a 4 level FSK transmitter and a π/4 differential QPSK transmitter, respectively, and a receiver suitable for use with both transmitters.

FIG. 4 depicts IF filter design constraints;

FIG. 5a represents the impulse response of an integrate and dump filter;

FIG. 5b represents the frequency response of the integrate and dump filter; and

FIG. 5c represents the band limited frequency response of the integrate and dump filter.

Detailed Description Of A Preferred Embodiment

Prior to describing an embodiment of the invention, it will be helpful to first briefly describe currently proposed 4 level FSK and π/4 differential QPSK transceiver structures.

FIG. 1a depicts pertinent components of a 4 level FSK transmitter (100). The transmitter includes a Nyquist filter (102) designed to have a roll-off factor of 0.2. The Nyquist filter (102) processes the 4 level data as a function of the square root of the raised cosine.

Subsequent to Nyquist filtering, a frequency modulator (103) having a deviation index of 0.27 effectively integrates the previously filtered data, and then frequency modulates the data with respect to a predetermined carrier, as represented by $e^{j(\phi+\omega t)}$. For purposes of simplicity, the above functions are readily

implementable in a DSP, such as a DSP56000 family device as manufactured and sold by Motorola, Inc. The blocks described, and other blocks not described but typically included in a transmitter (such as a power amplifier), are well understood by those skilled in the art, and hence further description would serve no pertinent purpose here.

FIG. 1b depicts relevant components for a proposed 4 level FSK receiver (125). An IF filter (127) filters a received modulation signal (126), which filtered signal is then frequency demodulated. In this embodiment, the frequency demodulator includes an inverse tangent block (128) that feeds its signal to a differential summer (129), the inverting input of which couples to a unit sample delay (131). (Though described as a differential summer, this element really appears as an approximate differentiator. The approximation is based on the first difference in a discrete time system to approximate the true differentiator of a continuous time system.) The output of the differential summer (129) couples to a Nyquist filter (132) (again having a roll-off factor of 0.2), and the resultant data residing within the Nyquist filtered and demodulated signal is recovered by a stochastic gradient bit recovery block (133).

As with the transmitter (100) described above, the above generally referred to functions can be readily implemented in a DSP, and are otherwise sufficiently well known and understood by those skilled in the art such that further elaboration need not be presented here.

FIG. 2a depicts a proposed $\pi/4$ differential QPSK transmitter (200). Again presuming a 4 level data source (201), a summer (202) sums this data with a feed back

signal processed through a unit sample delay (203), the latter components cooperating to realize a differential encoder. A phase modulator (204) then processes the encoded signal as a function of $e^{j\phi}$ to thereby yield complex in phase and quadrature components at, in this embodiment, one sample per symbol. The in phase and quadrature components are then Nyquist filtered (206) (where the roll-off factor = 0.2) and mixed (207) with an appropriate carrier frequency (208) to yield the desired modulation.

FIG. 2b depicts a proposed $\pi/4$ differential QPSK receiver suitable for receiving and demodulating a signal sourced by the above described transmitter (200). The receiver (225) receives the modulation (266) and Nyquist filters (227) the captured signal. The Nyquist filter (227) has a roll-off factor of 0.2. A phase demodulator (228) processes the Nyquist filtered signal as a function of an inverse tangent, and then provides the phase demodulated signal to a differential decoder (229). The differential decoder (229) includes a differential summer (231) that receives the phase demodulated signal and also the phase demodulated signal as processed through a unit sample delay (232). The resultant signal is then processed in an integrate and dump filter (233). A stochastic gradient bit recovery mechanism (234) then processes the decoded information to yield a 4 level data output, as generally referred to above with respect to FIG. 1b.

The blocks generally referred to above with respect to both the transmitter (200) and the receiver (225) for the $\pi/4$ differential QPSK modulation are relatively well understood by those skilled in the art, as well as other

components that would be appropriate to complete a transmitter and receiver, such as power amplifiers, transmission elements, and the like. Therefore, no additional description need be provided here.

The above described constant envelope and non-constant envelope receivers and transmitters are essentially incompatible with one another. For example, the 4 level FSK FM modulation provided by the first described transmitter (100) cannot be properly recovered and decoded using the second described receiver (225). Therefore, a selection of either one or the other transmitter/receiver (100/125 or 200/225) for use in a particular system will preclude an ability to compatibly select later the previously undesignated transmitter/receiver.

Referring now to FIGS. 3a-c, a solution to this dilemma will be presented.

First, in FIG. 3a, a constant envelope transmitter suitable for transmitting 4 level FSK FM modulation in a 12.5 kHz channel appears as generally depicted by reference numeral 300. This constant envelope transmitter (300) processes incoming 4 level data (301) through a raised cosine Nyquist filter (302) having a roll-off factor of 0.2. Those skilled in the art will note that, whereas the previously described proposed transmitters include Nyquist filters wherein the raised cosine function appears in both the transmitter and receiver as a square root function, here the raised cosine function is not so circumscribed. Instead of distributing the Nyquist filtering between the transmitter and receiver, all Nyquist filtering, in this embodiment, occurs at the transmission end.

Subsequent to Nyquist filtering, a differential encoder (303) processes the Nyquist filtered signal in a band limited filter (304) as a function of $\frac{\pi f T}{\sin(\pi f T)}$. A particular design problem, in this embodiment, involves computing the impulse response of this filter (304). Let

$H(\omega)$ = frequency response of ideal Nyquist raised cosine filter
The normalized corner frequency is 1 rad./sec.
The normalized symbol time (denoted by T) is π seconds.

$$H(\omega) = 1 \qquad \text{where } |\omega| \le 1-\alpha$$

$$H(\omega) = \frac{1}{2} + \frac{1}{2}\cos\left(\frac{\pi(|\omega|-1+\alpha)}{2\alpha}\right) \qquad \text{where } 1-\alpha < |\omega| \le 1+\alpha$$

$$H(\omega) = 0 \qquad \text{where } 1+\alpha < |\omega|$$

the impulse response of the filter may then be found using the inverse Fourier transform:

$$h(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} H(\omega)e^{j\omega t}d\omega$$

$$= \frac{1}{\pi}\int_{0}^{\infty} H(\omega)\cos(\omega t)d\omega \qquad \text{since } H(\omega) \text{ is an even function}$$

$$= \frac{1}{\pi}\int_{0}^{1-\alpha}\cos(\omega t)d\omega + \frac{1}{2\pi}\int_{1-\alpha}^{1+\alpha}\cos(\omega t)d\omega + \frac{1}{2\pi}\int_{1-\alpha}^{1+\alpha}\cos\left(\frac{\pi(\omega-1+\alpha)}{2\alpha}\right)\cos(\omega t)d\omega$$

The product rule, cosine (x) cosine (y) equals 0.5 cosine (x + y) + 0.5 cosine (x - y) is then used, and the integration then performed.

$$h(t) = \frac{\sin((1-\alpha)t)}{\pi t} + \frac{\sin((1+\alpha)t)-\sin((1-\alpha)t)}{2\pi t} + \frac{\sin(\pi+(1+\alpha)t)-\sin((1-\alpha)t)}{4\pi\left(\frac{\pi}{2\alpha}+t\right)}$$

$$+ \frac{\sin(\pi-(1+\alpha)t)+\sin((1-\alpha)t)}{4\pi\left(\frac{\pi}{2\alpha}-t\right)}$$

Next, use $\sin(\pi + x) = -\sin(x)$, and algebraically regroup the terms to yield the following result.

$$h(t) = \frac{\pi}{8\alpha^2 t} \frac{\sin((1+\alpha)t) + \sin((1-\alpha)t)}{\left(\frac{\pi}{2\alpha}\right)^2 - t^2}$$

Finally, using sine (x + y) + sine (x - y) equals 2 sine (x) cosine (y), one obtains

$$h(t) = \frac{\pi\sin(t)\cos(\alpha t)}{t(\pi^2-4\alpha^2t^2)}$$

The filter function h(t) can now be sampled at discrete time intervals to realize a Nyquist raised cosine finite impulse response (FIR) filter in a DSP embodiment.

Now, consider the shaping filter f(t). If we let $F(\omega)$ equal the frequency response of the shaping filter (304), and T equals symbol time equal 208.333 microseconds for 9600 bps equal π seconds for the normalized system used in H above, then

$$F(\omega) = \frac{\frac{\omega T}{2}}{\sin\left(\frac{\omega T}{2}\right)}$$

for all frequencies. With a roll-off factor of 0.2 for the Nyquist filter $H(\omega)$, $-1.2\pi < \omega T < 1.2\pi$ becomes the

frequency range of interest for F(ω). Such a filter function cannot be directly integrated with elementary calculus. Numerical methods could be used to compute the inverse Fourier integral, but that presents significant difficulties. A discrete Fourier transform method could be used or the FFT version of this transform could be used, to speed up the calculation. Such methods would be suitable presuming availability of sufficient processing abilities. In this embodiment, however, another method is preferred. Here, the function F will be approximated with a Fourier series of cosine terms that are then transformed to the time domain. To begin, select a suitable time interval that approximates F. This must equal or exceed plus or minus 1.2π and be less than plus or minus 2π since a singularity in F exists at WT equals to π. Plus or minus 1.3333π constitutes a useful interval, since this allows the samples to be spaced six samples apart when over sampling H by a factor of 8.

With the above in mind,

$$F(x) = \frac{\pi x}{\sin(\pi x)} \quad \text{where } x = \text{normalized frequency} = fT = \frac{\omega T}{2\pi}$$

$$= fo + \sum_{k=1}^{\infty} f_k \cos\left(\frac{2\pi k x}{1.33333}\right)$$

which is the Fourier series expansion

$$fo = 0.75 \int_{-2/3}^{2/3} F(x)dx$$

$$f_k = 1.5 \int_{-2/3}^{2/3} F(x)\cos\left(\frac{2\pi k x}{1.33333}\right)dx \quad \text{for } k > 0$$

These integrals are easily evaluated numerically. The first 12 terms are tabulated below.

TABLE 1

k	f_k
0	1.35697
1	-0.4839
2	0.189043
3	-0.0982102
4	0.0594481
5	-0.0396059
6	0.0281791
7	-0.0210304
8	0.0162746
9	-0.0129571
10	0.0105541
11	-0.00875928

Upon plotting the function F(x) and its Fourier series approximation, one ascertains a sufficiently close relationship. The series is within 1% of the desired value at most places in the passband of the Nyquist filter, though the error does approximate 2% near the band edge just before the Nyquist filter cuts off.

The inverse Fourier transform can then be performed on the series as follows:

$$f(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} F(\omega)e^{j\omega t}d\omega$$

$$= \frac{1}{2\pi}\int_{-\infty}^{\infty}\left(fo + \sum_{k=1}^{\infty} f_k \cos\left(\frac{k\omega T}{1.33333}\right)\right)e^{j\omega t}d\omega$$

$$= \frac{1}{2\pi}\left(f_0\,\delta(t) + \sum_{k=1}^{\infty} \frac{f_k}{2}\,\delta(t+0.75kT) + \sum_{k=1}^{\infty} \frac{f_k}{2}\,\delta(t-0.75kT) \right)$$

where the Dirac delta function is represented as $\delta(t)$.

Upon sampling at eight samples per symbol, non-zero samples are obtained at 0.75 X 8 = 6 sample intervals. The middle or zeroth sample has amplitude f0 and the remaining samples have amplitudes f_k /2 for k equals plus or minus 1, plus or minus 2, plus or minus 3, and so forth. This can then be cascaded with the h(t) function computed above to yield the filters necessary for this filter.

Subsequent to filtering, an integration function (306) completes the differential encoding process. Then, the signal can be frequency modulated as a function of $e^{j(\phi+\omega t)}$,while maintaining a deviation index of 0.25. The resultant modulation can then be appropriately amplified and transmitted in accordance with a particular application.

FIG. 3b depicts a non-constant envelope transmitter (325) suitable for use in transmission of a $\pi/4$ differential QPSK signal having a bandwidth of 6.25 kHz. A summer (327) receives a 4 level data input (326) and sums that with a feedback signal (328). This provides a differential encoder process as generally referred to above with respect to FIG. 2a. Also as presented in FIG. 2a, a phase modulator (329) processes the signal and provides complex in-phase and quadrature components at one sample per symbol. These components are then filtered in a raised cosine Nyquist filter (331). As with the constant envelope transmitter (300) described above,

this raised cosine Nyquist filter (331) has a roll-off factor of 0.2, and does not process the signal as a function of a square root of the raised cosine. Instead, all Nyquist processing from source to destination occurs in the transmitter (325). Subsequent to Nyquist filtering, a mixer (332) mixes the information signal with an appropriate carrier frequency (333) and the desired $\pi/4$ differential QPSK modulation results.

FIG. 3c depicts a receiver suitable for use in receiving and decoding modulation from either of the above described transmitters (300 and 325). Received modulation (351) couples to a loose IF filter (352). Design of this IF filter crucially affects the ability of the receiver (350) to properly receive either a wide frequency modulation signal (as presented in a 12.5 kHz channel) or a narrow linear modulation signal (as presented in a 6.25 kHz channel). In particular, the IF design must accommodate a pass bandwidth wide enough and flat enough to avoid intersymbol interference while having a stop bandwidth that is narrow enough to allow 6.25 kHz channel spacing. The constraints on the filter design are presented in FIG. 4 for a system with 9600 bits/second of throughput in a 6.25 kHz channel. As noted above, a Nyquist raised cosine filter having a roll-off factor of 0.2 appears in the transmitter. The stop bandwidth limit is 6.25 kHz while the pass bandwidth limit is designed to exceed

$$(1+\alpha)\frac{9600}{2} = 5.76 \text{ kHz}.$$

Due to the very demanding transition ratio,

$$r = \frac{\text{stop bandwidth}}{\text{pass bandwidth}} < \frac{6.25}{5.76} = 1.085$$

the number of necessary filter coefficients is about 350 when implementing such a filter in a single finite impulse response configuration. Since computation complexity is directly proportional to the number of filter coefficients, this constitutes an obvious drawback. In this embodiment, the loose IF filter (352) uses two FIR filters in a DSP embodiment. In particular, a decimating filter first narrows the bandwidth enough to reduce the sample rate for introduction to the subsequent filter, the latter providing a rapid filter roll-off. Both FIR filters in this embodiment are equi-ripple designs. The first FIR filter attains 80 db of stop band rejection with a stop frequency of 4.68 kHz and a pass frequency of 3 kHz. The second FIR filter has a stop frequency of 3.00 kHz and a pass frequency of 2.88 kHz. Parameters for both FIR filters appear in Table 2, below.

TABLE 2

Parameter	FIR 1	FIR 2
f_s= sample frequency	38.4 kHz	7.68 kHz
f_1= passband corner frequency	3.00 kHz	2.88 kHz
f_2= stopband corner frequency	4.68 kHz	3.00 kHz
r = transition ratio = f_1/f_2	1.56	1.04165
stopband rejection	100 dB	57.5 dB
passband ripple	0.0012 dB	0.4 dB
number of filter coefficients	128	128

Even though the second FIR filter attains a tighter transition ratio than the specified requirement for a 6.25 kHz channel, it does so with fewer filter coefficients than the previously referred to approach.

Subsequent to IF filtering, a frequency demodulator (353) demodulates constant envelope information. To this extent, the frequency demodulator includes an inverse tangent block (354), a differential summer (356) and a unit sample delay path (357) as essentially described above with respect to the proposed 4 level FSK receiver (125).

The receiver (350) also includes a differential decoder (358) substantially as described above for the $\pi/4$ differential QPSK receiver (255), inclusive of the unit sample delay path (357) and the differential summer (356), in conjunction with an integrate and dump filter (359). The integrate and dump filter essentially comprises a linear filter that integrates over a predetermined sample period and then dumps historical data in preparation for a new integration window. The impulse response for the integrate and dump filter appears in FIG. 5a, where the vertical scale represents normalized amplitude and the horizontal scale represents normalized time in seconds for T = 1 second. A corresponding frequency response (reflective of the familiar $\frac{\sin(\pi fT)}{\pi fT}$ filter response) appears in FIG. 5b, where the vertical scale again represents normalized amplitude and the horizontal scale represents normalized frequency in Hertz for T = 1 second. In this integrate and dump filter (359), some portion of the side lobes are filtered out of the frequency response, therefore yielding a band limited filter. To achieve perfect symbol recovery, a frequency response in the range of $\frac{-(1+\alpha)}{2T}$ Hz to $\frac{1+\alpha}{2T}$ Hz

must be retained. Taking advantage of the spectral null at 1/T Hz, the response is restricted to a low pass filter cutoff at 1/T Hz. The resulting frequency response appears in FIG. 5c, where the vertical and horizontal scales are as described earlier for FIG. 5b.

The impulse response for this filter (359) can be directly calculated with an inverse Fourier transform. A closed form solution can be expressed in terms of the sine integral function Si (X) as shown below.

Let H(x) = frequency response of bandlimited filter

$$= \frac{\sin(\pi x)}{\pi x} \qquad \text{for } |x| < 1$$

$$= 0 \qquad \text{for } |x| \geq 1$$

h(t) = inverse Fourier transform of H(x) Let $\omega = 2\pi x$

$$= \frac{1}{\pi}\int_0^{2\pi} \frac{2}{\omega} \sin\left(\frac{\omega}{2}\right)\cos(\omega t)d\omega \quad \text{since } H(\omega) \text{ is an even function}$$

$$= \frac{1}{\pi}\int_0^{2\pi} \frac{1}{\omega} \left(\sin((t+\frac{1}{2})\omega)-\sin((t-\frac{1}{2})\omega)\right)d\omega \quad \text{using a trig identity}$$

$$\frac{1}{\pi}\left(\int_0^{2\pi(t+1/2)} \sin(y)\frac{dy}{y} - \int_0^{2\pi(t-1/2)} \sin(y)\frac{dy}{y}\right) \quad \text{substituting variables}$$

$$= \frac{1}{\pi}\left(\sin(2\pi(t+\frac{1}{2}))-\sin(2\pi(t-\frac{1}{2}))\right) \text{ where } Si(x) = \int_0^x \frac{\sin(t)}{t}\,dt$$

Following this, a stochastic gradient bit recovery mechanism (361) is again provided and the resultant 4 level data recovered.

So configured, a number of salient points should now be evident to those skilled in the art. First, the receiver provides no Nyquist filtering. All Nyquist filtering occurs in the transmitters. (The rolloff ratio constitutes the important variable to be controlled in a Nyquist filter. In prior art transceivers using Nyquist filters, this ratio must be identical for both the transmitter filter and the receiver filter. Here, the receiver is independent of this variable, and can receive signals from different transmitters that use different values for the rolloff ratio.) Second, the receiver can effectively demodulate and recover either constant envelope signals or non-constant envelope signals, such as 4 level FSK FM or $\pi/4$ differential QPSK linear modulation. Third, this receiver can accommodate these alternative modulation types, notwithstanding differing channel widths, in this case 12.5 kHz and 6.25 kHz, respectively.

With the architectures described above, a system operator can select to realize the advantages of digital signalling by fielding 4 level FSK FM transmitters coupled with the described compatible receiver. At such time as linear transmission technologies make viable economic fielding of $\pi/4$ differential QPSK transmitters, the operator can introduce such transmitters into a system in conjunction with the same compatible receiver as used for the constant envelope transceivers. Notwithstanding differing modulation types and differing bandwidth requirements, the same receiver platform allows compatible communication between these differing units.

What is claimed is:

Claims

1. A radio transceiver, comprising:

A) a transmitter, which transmitter includes a Nyquist filter; and

B) a receiver, which receiver does not include a Nyquist filter.

2. A radio transceiver, comprising:

A) a transmitter, comprising at least a Nyquist filter and transmitting at least one of:

i) a constant envelope signal; and

ii) a non-constant envelope signal; and

B) a receiver, which receiver does not have a Nyquist filter, for receiving and properly demodulating both:

i) a constant envelope signal; and

ii) a non-constant envelope signal.

3. A radio transceiver, comprising:

A) a transmitter, comprising at least a Nyquist filter and transmitting at least one of:

i) a constant envelope signal occupying a first spectral bandwidth; and

ii) a non-constant envelope signal occupying a second spectral bandwidth, which second spectral bandwidth is different from the first spectral bandwidth; and

B) a receiver, which receiver does not have a Nyquist filter, for receiving and properly demodulating both:

i) a constant envelope signal occupying the first spectral bandwidth; and

ii) a non-constant envelope signal occupying the second spectral bandwidth.