



US007948290B2

(12) **United States Patent**  
**Kato**

(10) **Patent No.:** **US 7,948,290 B2**  
(45) **Date of Patent:** **May 24, 2011**

- (54) **DIGITAL PLL DEVICE**
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- (\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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- (21) Appl. No.: **12/439,644**
- (22) PCT Filed: **Jul. 8, 2008**
- (86) PCT No.: **PCT/JP2008/001827**  
§ 371 (c)(1),  
(2), (4) Date: **Mar. 2, 2009**
- (87) PCT Pub. No.: **WO2009/013860**  
PCT Pub. Date: **Jan. 29, 2009**

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*Primary Examiner* — Cassandra Cox  
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- (65) **Prior Publication Data**  
US 2010/0001773 A1 Jan. 7, 2010
- (30) **Foreign Application Priority Data**  
Jul. 23, 2007 (JP) ..... 2007-190405

(57) **ABSTRACT**

An input clock dividing unit frequency-divides an input clock, and an input clock multiplying unit frequency-multiplies the input clock. An operation clock selecting unit selects the frequency-divided clock when the input clock is fast and selects the frequency-multiplied clock when the input clock is slow, based on the frequency detection result of frequency detecting unit. The operation clock selecting unit then outputs the selected clock to a phase comparing unit as an operation clock. The phase comparing unit operates according to the frequency-divided or frequency-multiplied clock, and controls an oscillating unit so that the phase difference between a reference signal and a comparison signal becomes zero. The phase of an output clock is thus caused to track the phase of the reference signal.

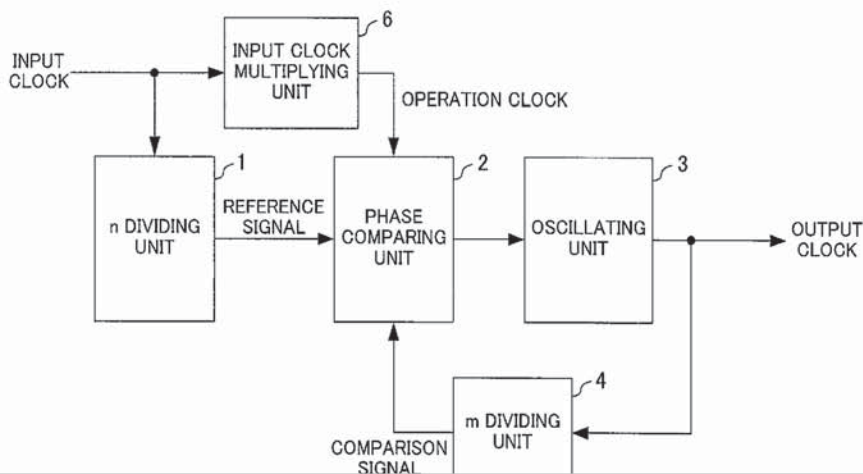
- (51) **Int. Cl.**  
**H03L 7/06** (2006.01)
- (52) **U.S. Cl.** ..... **327/159; 327/150**
- (58) **Field of Classification Search** ..... None  
See application file for complete search history.

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**11 Claims, 7 Drawing Sheets**



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FIG. 1

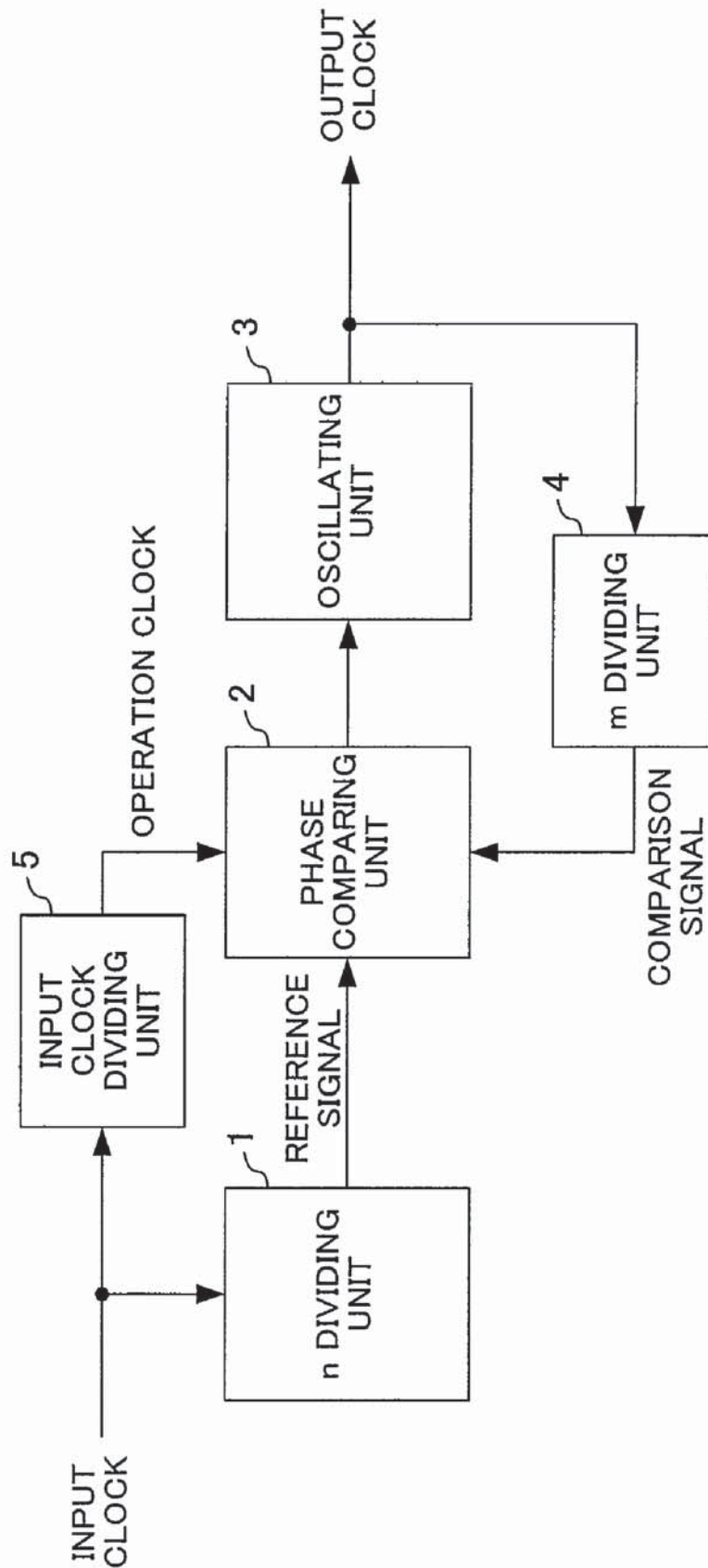
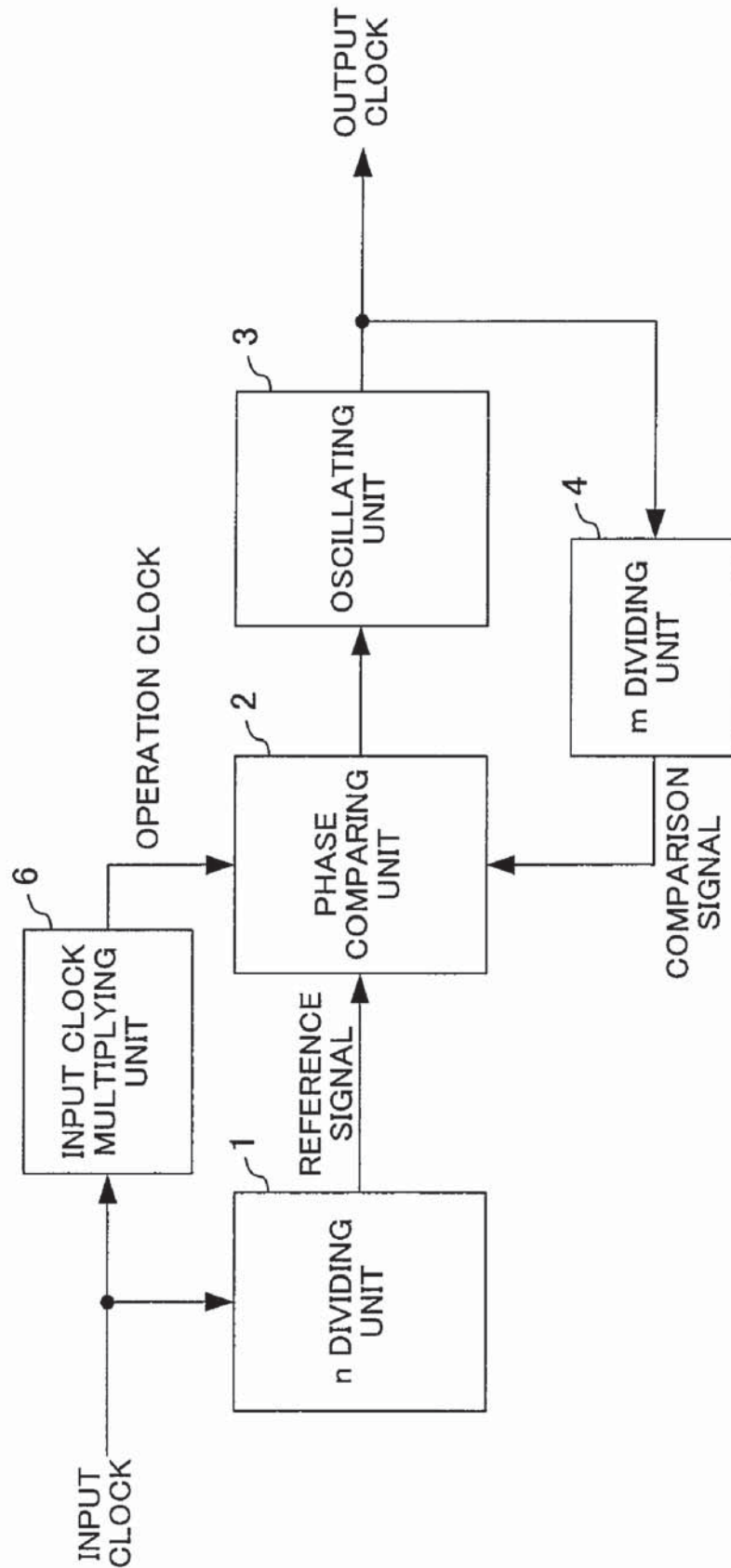


FIG. 2



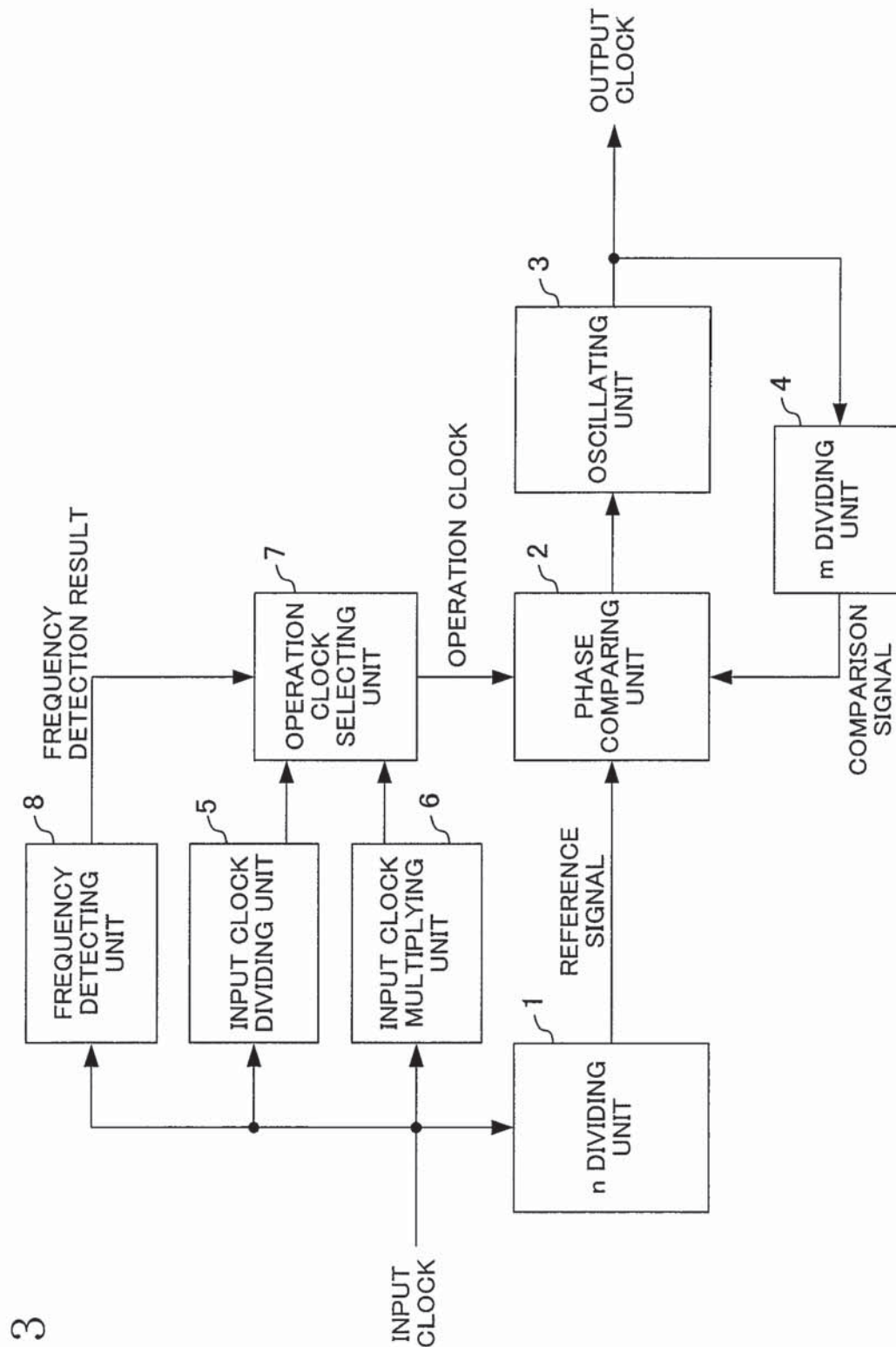


FIG. 3

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