

IN THE UNITED STATES DISTRICT COURT  
FOR THE DISTRICT OF DELAWARE

INFINEON TECHNOLOGIES AG and :  
INFINEON TECHNOLOGY NORTH :  
AMERICA CORP., :  
Plaintiffs, :

v. :

ATMEL CORPORATION, :  
Defendant. :

Civil Action No. 11-307-RGA

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**ORDER**

The Court having considered the Parties' Joint Claim Construction Briefs (D.I. 153, 154), letter (D.I. 159), amended appendices and charts (D.I. 161-165), and oral argument (D.I. 171, 172), **IT IS HEREBY ORDERED** that, as used in the identified patents, the terms below are construed as follows:

**I. U.S. Patent No. 5,539,910**

1. The '910 patent claims a power management system that monitors supply voltage with multiple voltage detectors. The invention is "distinguished above all by low power consumption." Col.2 ll.3-6. It claims power management components turning off and on at different voltage levels to conserve power, as cited below. Accordingly:

a. The term "said undervoltage detector being in operation . . . when a supply voltage is in a range between a lower first limit value and a higher second limit value below the minimum supply voltage" is construed to mean "said undervoltage detector is turned on . . . when a supply voltage is in a range between a lower first limit value and higher second limit value below the minimum supply voltage, and is turned off when the supply voltage is above the second limit value." *See* col.4 ll.62-64; col.3 ll.28-32.

b. The term "said comparator being in operation at a supply voltage above the second limit value" is construed to mean "said comparator is turned on at a supply voltage above the second limit value, and is turned off at a supply voltage below the second limit value." *See* col.4 l.62 - col.5 l.4; col.3 ll. 36-43.

c. The term "the oscillator being in operation at a supply voltage above the second limit value" is construed to mean "the oscillator is turned on at a supply voltage above the second limit value, and is turned off at a supply voltage below the second limit value." *See* col.3 ll. 17-19; col.3 ll.48-50; col.4 ll.5-7, 47-53; col.5 ll.14-21.

2. The term "activation signal" is construed to mean "a signal, other than the reset signal, that turns on or resumes operation of the processor unit." The intrinsic evidence provide sthat the processor unit "is not activated until the activation signal As appears," to the exclusion of the reset signal Rs. Col.3 ll.50-51; Fig.1.

## **II. U.S. Patent No. 6,076,159**

1. The term "loop instructions" is construed to mean "a statement or expression consisting of an operation and its operands (if any), which can be interpreted by a computer in order to perform a loop function or operation." There is no intrinsic evidence to support limiting this term to conditional jump instructions, which the patent distinguishes from loops. *See* col.7 ll.5-8.

2. The term "a second pipeline for executing loop instructions" is construed to mean "a pipeline that only executes loop instructions." The claimed architecture requires a dedicated pipeline for loop instructions. Col.2 l.67 - col.3 l.2; D.I. 164 at 22, 28 (Off. Action dtd. July 12, 1999 at 3; Resp. dtd. Oct. 8, 1999 at 5). Where there is one "main" pipeline as in Claim 5, the

dedicated pipeline is the “second pipeline,” and where there are two “main” pipelines, the dedicated pipeline is the “third pipeline.” *E.g.*, Fig.3; col.2 l.67 - col.3 l.2.

### **III. U.S. Patent No. 6,653,963**

1. The terms "in a channel-specific way as a function of a signal channel which is to be converted," "in a channel-specific way as a function of the signal channel to be converted," and "in a channel specific way . . . as a function of the signal channel to be converted" are given their plain and ordinary meaning. Atmel's proposed construction does not limit or clarify the terms.

2. The term "assigning certain settings for the operating parameters of the A/D converter arrangement which are to be set, to individual requesting means" is given its plain and ordinary meaning. Atmel draws its proposed limitations from claim 18. (D.I. 154 at 35). Because these limitations are already explicitly claimed in independent claim 18, there is no reason to import them into this claim term, which appears in independent claim 1 and its dependent claims.

3. The term “setting the operating parameters of the A/D converter arrangement which are to be set, in agreement with the settings assigned to said requesting means making a request” is given its plain and ordinary meaning. Atmel's proposed limitation is not supported by the specification and does not clarify the term.

### **IV. U.S. Patent No. 6,665,802**

1. The term “bus interface” is construed to mean “a bus interface that includes a software configuration register.” “Bus interface” has a plain and ordinary meaning. The intrinsic evidence indicates that to accomplish the goal of the invention (decentralized and independent power management for peripheral units), each peripheral unit's bus interface (“FPI”) includes a software configuration register. '802 Patent at [57]; col.2 l.62-col.3 l.6. Claim 7 includes the



additional element that each register “allow[s] a corresponding peripheral device to respond independently to the power management controls.” Claim 5 already requires that the peripherals receive “power management controls” through their bus interface, so it is not proper to limit the term “bus interface” to require “storing power modes” as Atmel suggests.

2. The term “each peripheral device including a bus interface” is construed to mean “each peripheral device has its own bus interface.” To accomplish the goal of the invention (decentralized and independent power management for peripheral units), each peripheral unit has its own bus interface. Fig.1; col.2, ll.62-65; col.3, ll.1-6; D.I. 164 at 76-77, 83-85 (Resp. dtd. June 19, 2003 at 9-10, 16-18).

3. The term “individually configuring a response of each of the one or more subsystems to the global power management command through a corresponding register in each of the one or more subsystems” is construed to mean “each subsystem is separately configured to respond to the global power management command through its own separate register.” To accomplish the goal of the invention (decentralized and independent power management for peripheral units), each peripheral unit has its own bus interface (“FPI”) that includes a software configuration register. ‘802 Patent at [57]; Fig.1; col.2, ll.62-65; col.3, ll.1-6; D.I. 164 at 76-77, 83-85 (Resp. dtd. June 19, 2003 at 9-10, 16-18). **V. U.S. Patent No. 6,769,065**

1. The term “access authorization monitoring device” (“AAMD”) is construed to mean “a security device that monitors and prevents any attempted access by a debugger device to protected on-chip components, unless the debugger device has verified authority.” The AAMD monitors for verified authority; neither the AAMD nor the debugger must verify or generate that

authority, and other appliances can produce the authority. Col.4 ll.1-7, 55-57. "Permission" is too broad; the patent discloses the additional concept of verification. D.I. 171 at 14; col.4 ll.1-7.

2. The term "verified authorization" is construed to mean "access permitted only to authorized holders of a debugging device or other appliance but not to others." The intrinsic evidence provides that authorization verification can be produced by "the debugger or other appliance" and authorizes holders of those devices to access the claimed programmable unit. Col.4 ll.55-57.

#### **VI. U.S. Patent No. 6,788,235**

1. The term "synchronizing the analog-to-digital converter with at least one other analog-to-digital converter of the plurality of analog-to-digital converters" is construed to mean "using a bidirectional procedure to cause the analog-to-digital converter to start simultaneously with at least one other analog-to-digital converter of the plurality of analog-to-digital converters." The intrinsic evidence indicates that synchronizing is performed bidirectionally, with a preferred embodiment via handshaking. Col.5 ll.13-19; D.I. 165 at 20 (Resp. dtd. July 30, 2002 at 3). During prosecution, the applicant disclaimed an unidirectional procedure to overcome prior art. (D.I. 165 at 20). While the patent discloses analog-to-digital conversions implemented "absolutely simultaneously or time-synchronously," or with "minimal time offset," during prosecution synchronization was narrowed to modes with "an element of signaling at the beginning or at an impending beginning of an analog-to-digital conversion." D.I. 165 at 10-11, 21 (Resp. dtd. Feb. 1, 2002 at 4; Resp. dtd. July 30, 2002 at 4); *see* col.3 ll.20-24; col.5 ll.13-19. Describing the conversions as "simultaneous" encompasses this element.

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