

Advanced Micro Device
Petitioner

V.

Aquila Innovations, Inc.
Patent Owner

IPR2019-01526 (Patent No. 6,8

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Agenda

- Overview of the '519 patent
- Claim construction
- Ober + Nakazato and “a plurality of ordinary
- Claims 2-6 and Windows ACPI
- Claims 8 & 9 and Doblar

Instituted Grounds

IPR2019-01526 ('519 Patent)

	Claim(s)	References
Ground 1	1, 7, 10, 11	Ober and Nakazato
Ground 2	2-6	Ober, Nakazato, Coo
Ground 3	8, 9	Ober, Nakazato and I

'519 Patent – Claim 1

Claim 1

[1.p] A system LSI having a **plurality of ordinary operation modes** and a plurality of clock frequencies supplied to a central processing unit, comprising:

[1.1] a first memory that stores a clock control library for controlling a **clock frequency transition among said ordinary operation modes**;

[1.2] a system control circuit which has a register, wherein said system control circuit controls a transition between said ordinary operation modes and said special modes in response to a value in said register, and also **carries out the clock frequency transition among said ordinary operation modes according to said clock control library**;

[1.3] a clock generation circuit that receives a plurality of standard clocks, wherein a clock is supplied to said central processing unit according to control by said system control circuit;

[1.4] a second memory that stores an application program, wherein calling of said ordinary operation modes and said special modes in response to a register value are programmably controlled by said application program to enable said transitions,

[1.5] **wherein said special modes comprise** a first special mode in which clock supply to said central processing unit is halted, a second special mode in which clock supply to said central processing unit is halted, and a third special mode in which supply of power to the entirety of said system LSI is halted;

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