Advanced Configuration and Power Interface Specification

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Intel Corporation
Microsoft Corporation
Phoenix Technologies Ltd.
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Revision 2.0
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ii

Revision	Change Description	Affected Sections
Aug. 2000 2.0	Major specification revision. 64-bit addressing support added. Processor and device performance state support added. Numerous multiprocessor workstation and server-related enhancements. Consistency and readability enhancements throughout.	
Feb. 1999 1.0b	Fixed previous errata that deleted wrong paragraph in the RTC_EN description.	4.7.3.1.2
	Clarified P_BLK requirements on multiprocessor systems.	4.7.2.6.3
	Changed definition of SCI_INT pin in Table 5-5.	5.2.5
	Replaced section 5.2.8, adding new structures and clarifications to support multiprocessor configurations.	5.2.8
	Expanded Name Space description—clarified the name search rules, added Parent operator to operator list, described name padding.	5.3
	Expanded ASL definition—defined global objects, clarification that OpRegion accesses may block, added description of the scope and life of variables in control methods.	5.5.3
	Changed notify values.	5.6.3
	Added _PIC method to Table 5-33 and new section 5.8.	5.6.5 & 5.8
	Added USB _ADR values to Table 6-1.	6.1.1
	ACPI Control Method added for floppy enumeration (_FDE).	10.8
	ASL Grammar clarifications—initial and default SyncLevel values, ObjectType behavior for specific objects, usage of the RefOf operator and behavior of non-package method evaluation.	15.2.3
	Added top-level AML definition.	16.2
	Changed concat arguments to be TermArgs resolving to data.	16.2.4.4
	Added the _GLK object and referenced it in the Smart Battery and the Control Method Battery sections.	6.5.6 & 11.1.4 & 11.2.2 & 13.8 & 13.9 &13.12
	Added Video Extensions as an Appendix.	Appendix A
1.0a	Added _PRT requirement for PCI root bridges.	1.7
	Clarification H/W behavior—PM timer may be stopped when not in the G0/S0 state, Lid Switch behavior and correction of the RTC_EN bit in Table 4-10.	4.7.2.1
	Clarification of tables—trailing blank required in signature in Table 5-1, FLUSH_SIZE and FLUSH_STRIDE clarification Table 5-5.	5.2.x
	Clarified placement of APIC-related structures and general clean up, added Interrupt source overrides.	5.2.8
	Various removals—Figure 5-4, DCK_CAP flag from Table 5-6, _SBC and _SBS methods from Table 5-33.	

iv

(continued)

Revision	Change Description	Affected Sections
	Various additions—AC device PnP ID to Table 5-32, _DDN (logical name association) to Table 6-1, _ADR values for floppy, _FDI–floppy configuration info, requirements for _CRS used with bus devices, battery presence bit to _STA definition, QWORD to La rge Resource data type, _INI Method.	5.6.4
	Wake/Sleep clarifications—_PTS not executed for S5 and SCI cannot occur before enabled.	9.1 & 9.3
	Rewrote the IDE Controller Device section.	10.8
	Corrected the passive cooling equation for TC1 and TC2.	12.3.7 (&8)
	Removed requirement that PRx contain numeric lowest state.	7.2.x (0-2)
	Removed Duplicate Section "General-Purpose Register Blocks."	4.7.4.3
	Clarified that C1 is required and C2 & C3 are optional and reiterate requirement for C1 processor state in Table 5-6.	4.7.2.6 & 5.2.5
	Clarified the Passive Cooling Equation.	12.1.5
	Numerous grammar updates and corrections.	15 & 16
	Added SxD objects.	7.2 &7.2.x
1.0	Original Release.	

Contents

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