

UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

AQUILA INNOVATIONS, INC., a Delaware Corporation,	§	No. 1:18-cv-554-LY
	§	
Plaintiff,	§	
	§	
v.	§	
	§	
ADVANCED MICRO DEVICES, INC., a Delaware corporation	§	
	§	
Defendant.	§	
	§	

AQUILA INNOVATIONS, INC.’S
PRELIMINARY INFRINGEMENT CONTENTIONS

Pursuant to the Court’s Scheduling Order, D.I.23, Plaintiff Aquila Innovations, Inc. (“Aquila”) submits the following preliminary infringement contentions for U.S. Patents 6,239,614 (“614 Patent”) and 6,895,519 (“519 Patent”). These preliminary infringement contentions were prepared without the benefit of the Court’s claim construction or the parties’ exchange of constructions. Discovery has been stayed, and AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court’s constructions or to account for new information that becomes available.

(a) Identification of asserted claims

'614 Patent: Claims 1, 2

'519 Patent: Claims 1, 2, 3, 5, 6, 7, 10

(b) Identification of accused products

'614 Patent Accused Products:

Aquila contends that all AMD processor products containing power gate rings infringe each of the asserted claims of the '614 Patent. This specifically includes but is not limited to processors with cores having microarchitectures belonging to the following families:

- AMD 12h Llano Fusion APUs
- AMD 15h Bulldozer APUs
- AMD 15h Piledriver APUs
- AMD 15h Excavator APUs

AMD products belonging to each product family are identified in Exhibits C.1 through C.4. The identification of specific products was prepared without the benefit of discovery from AMD and may not include OEM or custom processor products. Aquila reserves the right to amend or supplement its identification of accused products as AMD provides more information.

'519 Patent Accused Products:

Aquila contends that all AMD processor products capable of entering/exiting the CC1, PC1, and PC6 states infringe each of the asserted claims of the '519 Patent. This specifically includes but is not limited to processors with cores having microarchitectures belonging to the following families:

- AMD Family 12h
- AMD Family 14h
- AMD Family 15h
- AMD Family 16h
- AMD Family 17h

AMD products belonging to each product family are identified in Exhibits C.1 through C.5. The identification of specific products was prepared without the benefit of discovery from AMD and may not include OEM or custom processor products. Aquila reserves the right to amend or supplement its identification of accused products as AMD provides more information.

(c) Claim Charts

Claim charts for each asserted claim corresponding to each representative accused product are contained in the exhibits below.

'614 Patent: Exhibit A

'519 Patent: Exhibit B

(d) Doctrine of Equivalents

Aquila contends that each limitation in each asserted claim is met literally. The Court has not construed the asserted claims, and AMD has not yet provided discovery on the accused products or provided non-infringement contentions. Aquila reserves the right to respond if AMD provides non-infringement contentions, which response may include doctrine of equivalents contentions.

(e) Identification of Priority Date

'614 Patent: Each asserted claim of the '144 Patent is entitled to a priority date as late as January 14, 1999.

'519 Patent: Each asserted claim of the '519 Patent is entitled to a priority date as late as February 25, 2002.

Respectfully submitted,

Dated: February 13, 2019

/s/Jing H. Cherng
Robert E. Freitas (*admitted pro hac vice*)
Jing H. Cherng (*admitted pro hac vice*)
FREITAS & WEINBERG LLP
350 Marine Parkway, Suite 200
Redwood Shores, CA 94065
Telephone: (650) 593-6300
rfreitas@fawlaw.com
gcherng@fawlaw.com

Henry B. Gonzalez III
State Bar No. 00794952
Jeffrie B. Lewis
State Bar No. 24071785
**GONZALEZ, CHISCANO, ANGULO,
& KASSON, PC**
9601 McAllister Freeway, Suite 401
San Antonio, Texas 78216
Tel: (210) 569-8500
hbg@gcaklaw.com
jlewis@gcaklaw.com

Attorneys for Plaintiff
Aquila Innovations, Inc.

CERTIFICATE OF SERVICE

I hereby certify that on this 13th day of February, 2019, a true and correct copy of the foregoing was forwarded to the following:

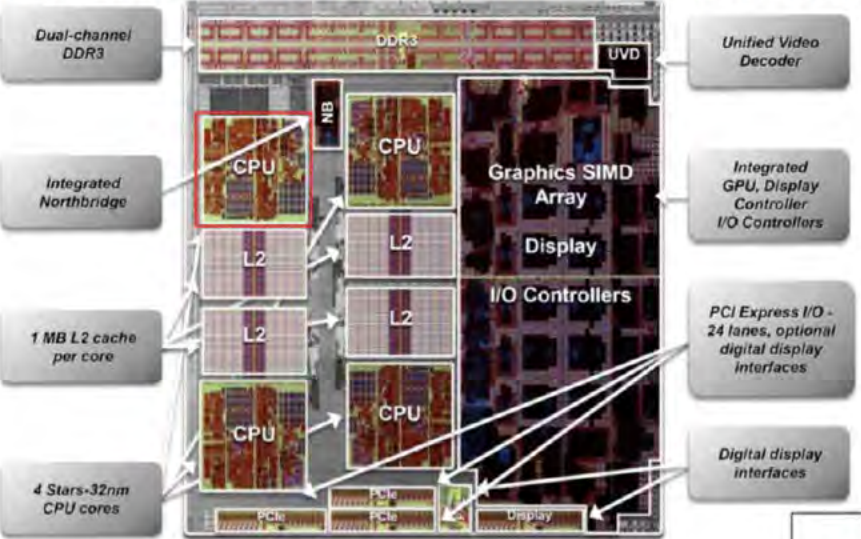
Jennifer Librach Nall
Kevin J. Meek
Aashish Kapadia
Puneet Kohli
jennifer.nall@bakerbotts.com
kevin.meek@bakerbotts.com
aashish.kapadia@bakerbotts.com
puneet.kohli@bakerbotts.com
DLWiLAN_AMD_BakerBotts@BakerBotts.com
BAKER BOTTS LLP

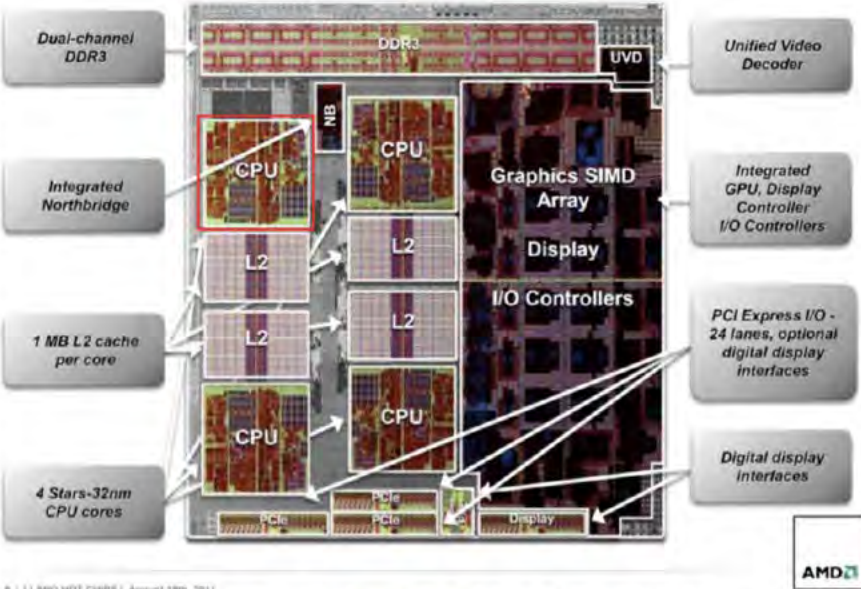
Jing H. Cherng _____
Jing H. Cherng

Exhibit A.1: Preliminary Infringement Contention Claim Chart for U.S. Patent 6,239,614

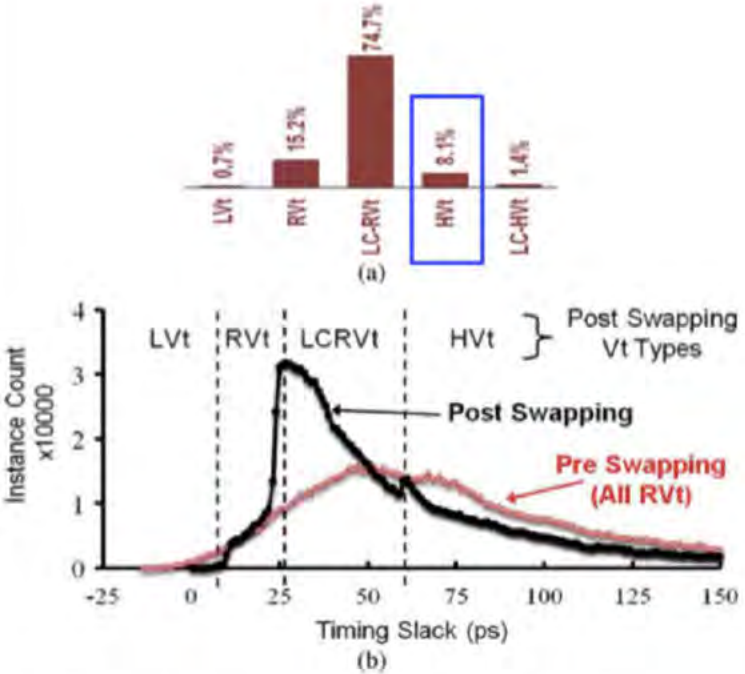
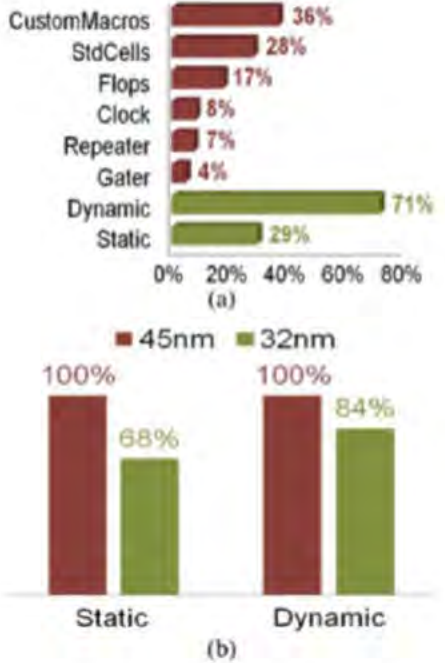
Accused Product: AMD Family 12h Fusion Processors

These preliminary infringement contentions were prepared without the benefit of the Court’s claim construction or the parties’ exchange of constructions. As of the date of these contentions, AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court’s constructions or to account for new information that becomes available.

	<u>Limitation</u>	<u>Contention</u>
1p	A semiconductor integrated circuit device, comprising:	<p>To the extent the preamble is a limitation, the Accused Products are semiconductor integrated circuit devices.</p>  <p>The diagram illustrates the internal architecture of an AMD LLANO Fusion APU. It features four 32nm CPU cores arranged in a 2x2 grid, each with its own 1 MB L2 cache. A central Northbridge (NB) connects the CPU cores to the system memory (DDR3) and the Unified Video Decoder (UVD). The GPU is represented by a Graphics SIMD Array, which is integrated with the CPU cores. The architecture also includes I/O controllers for PCI Express (24 lanes) and digital display interfaces. The AMD logo is visible in the bottom right corner of the diagram.</p> <p><small>© LLANO HOT Chips August 19th, 2011</small></p> <p>Source: AMD'S "LLANO" FUSION APU, Hot Chips 23, 19th August 2011, page 6.</p>

	<u>Limitation</u>	<u>Contention</u>
1a	<p>a plurality of first unit cells each including a plurality of first MOS transistors, each of the first MOS transistors having a first threshold voltage;</p>	<p>The Accused Products contain a plurality of first unit cells:</p>  <p>The diagram shows a die photo of an AMD Llano APU with various components labeled. On the left side, callouts point to: Dual-channel DDR3 (top), Integrated Northbridge (middle), 1 MB L2 cache per core (two locations), and 4 Stars-32nm CPU cores (two locations). On the right side, callouts point to: Unified Video Decoder (top), Integrated GPU, Display Controller I/O Controllers (middle), PCI Express I/O - 24 lanes, optional digital display interfaces (middle), and Digital display interfaces (bottom). The die itself is labeled with components like CPU, NB, L2, Graphics SIMD Array, Display, and I/O Controllers. An AMD logo is at the bottom right of the die photo.</p> <p><small>8 LLMO HOT CHIPSE August 19th, 2011</small></p> <p>Source: AMD'S "LLANO" FUSION APU, Hot Chips 23, 19th August 2011, page 6.</p> <p>As is typical of multi-VT standard cell design methodologies and structures, the Llano Accused Products use a mix of low Vt (LVt), regular Vt (RVt), long channel regular Vt (LC-RVt) and long channel high Vt (LC-Hvt) standard cells.</p>

<u>Limitation</u>	<u>Contention</u>																											
	<div data-bbox="715 277 1542 634" style="border: 2px solid red; padding: 5px;"> <table border="1" style="border-collapse: collapse; text-align: center; width: 100%;"> <tr> <td style="background-color: yellow;">uLvt <small>4</small></td> <td style="background-color: cyan;">Lvt <small>2</small></td> <td style="background-color: lightblue;">Lvt filler <small>2</small></td> <td style="background-color: lightpurple;">Svt <small>4</small></td> <td style="background-color: yellow;">uLvt <small>4</small></td> <td style="background-color: cyan;">Lvt <small>2</small></td> <td style="background-color: lightblue;">Lvt filler <small>2</small></td> <td style="background-color: lightpurple;">Svt <small>4</small></td> </tr> <tr> <td style="background-color: yellow;">uLvt <small>4</small></td> <td style="background-color: cyan;">Lvt <small>2</small></td> <td style="background-color: lightblue;">Lvt filler <small>2</small></td> <td style="background-color: lightpurple;">Svt <small>4</small></td> <td style="background-color: yellow;">uLvt <small>4</small></td> <td style="background-color: cyan;">Lvt <small>2</small></td> <td style="background-color: lightblue;">Lvt filler <small>2</small></td> <td style="background-color: lightcoral;">Svt filler <small>2</small></td> <td style="background-color: lightpurple;">Svt <small>2</small></td> </tr> <tr> <td style="background-color: yellow;">uLvt <small>4</small></td> <td style="background-color: cyan;">Lvt <small>2</small></td> <td style="background-color: lightblue;">Lvt filler <small>2</small></td> <td style="background-color: lightcoral;">Svt filler <small>2</small></td> <td style="background-color: lightpurple;">Svt <small>2</small></td> <td style="background-color: yellow;">uLvt <small>4</small></td> <td style="background-color: cyan;">Lvt <small>2</small></td> <td style="background-color: lightblue;">Lvt filler <small>2</small></td> <td style="background-color: lightcoral;">Svt filler <small>2</small></td> <td style="background-color: lightpurple;">Svt <small>2</small></td> </tr> </table> </div> <p data-bbox="696 691 2386 764">The Accused Products contain a plurality of first MOS transistors, each of the first MOS transistors having a first threshold voltage:</p>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt <small>4</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt <small>4</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt <small>4</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt filler <small>2</small>	Svt <small>2</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt filler <small>2</small>	Svt <small>2</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt filler <small>2</small>	Svt <small>2</small>
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	<u>Limitation</u>	<u>Contention</u>
		<p>JOTWANI <i>et al.</i>: AN x86-64 CORE IN 32 nm SOI CMOS 167</p>  <p>Figure 10(a) is a bar chart showing the distribution of device widths for different Vt types. The x-axis lists Vt types: LVt (0.7%), RVt (15.2%), LC-RVt (74.7%), HVt (8.1%), and LC-HVt (1.4%). The HVt bar is highlighted with a blue box.</p> <p>Figure 10(b) is a line graph of Instance Count (x10000) vs. Timing Slack (ps). It compares 'Pre Swapping (All RVt)' (red line) and 'Post Swapping' (black line). Vertical dashed lines mark Vt types: LVt, RVt, LCRVt, and HVt. The 'Post Swapping' curve shows a significant increase in instances with positive timing slack, indicating better timing margins.</p>  <p>Figure 11(a) is a horizontal bar chart showing TDP power distribution at 1 V. The y-axis lists components: CustomMacros (36%), StdCells (28%), Flops (17%), Clock (8%), Repeater (7%), Gater (4%), Dynamic (71%), and Static (29%).</p> <p>Figure 11(b) is a vertical bar chart comparing power improvement for 45nm (red) and 32nm (green) technologies. For Static power, 45nm is 100% and 32nm is 68%. For Dynamic power, 45nm is 100% and 32nm is 84%.</p> <p>Fig. 10. (a) Core device width histogram by Vt type. (b) Using Vt swaps to reshape critical path timing opportunistically.</p> <p>Fig. 11. (a) TDP power distribution at 1 V. (b) Relative power improvement with respect to 45 nm generation core (normalized for performance).</p> <p><i>Source: An x86-64 Core in 32 nm SOI CMOS, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 1, JANUARY 2011, page 6.</i></p>
1b	a plurality of second unit cells each including a plurality of second MOS	The Accused Products contain a plurality of second unit cells:

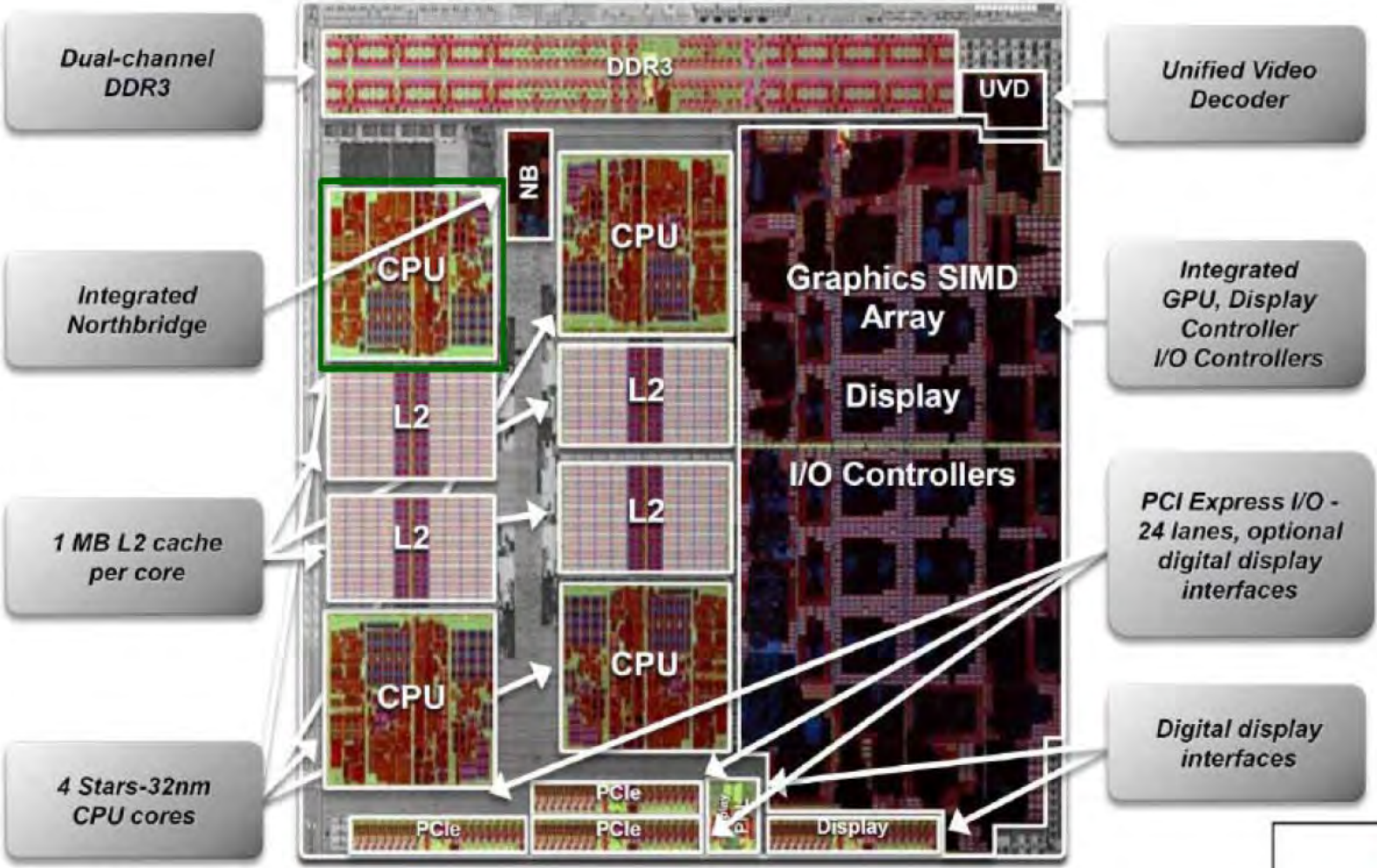
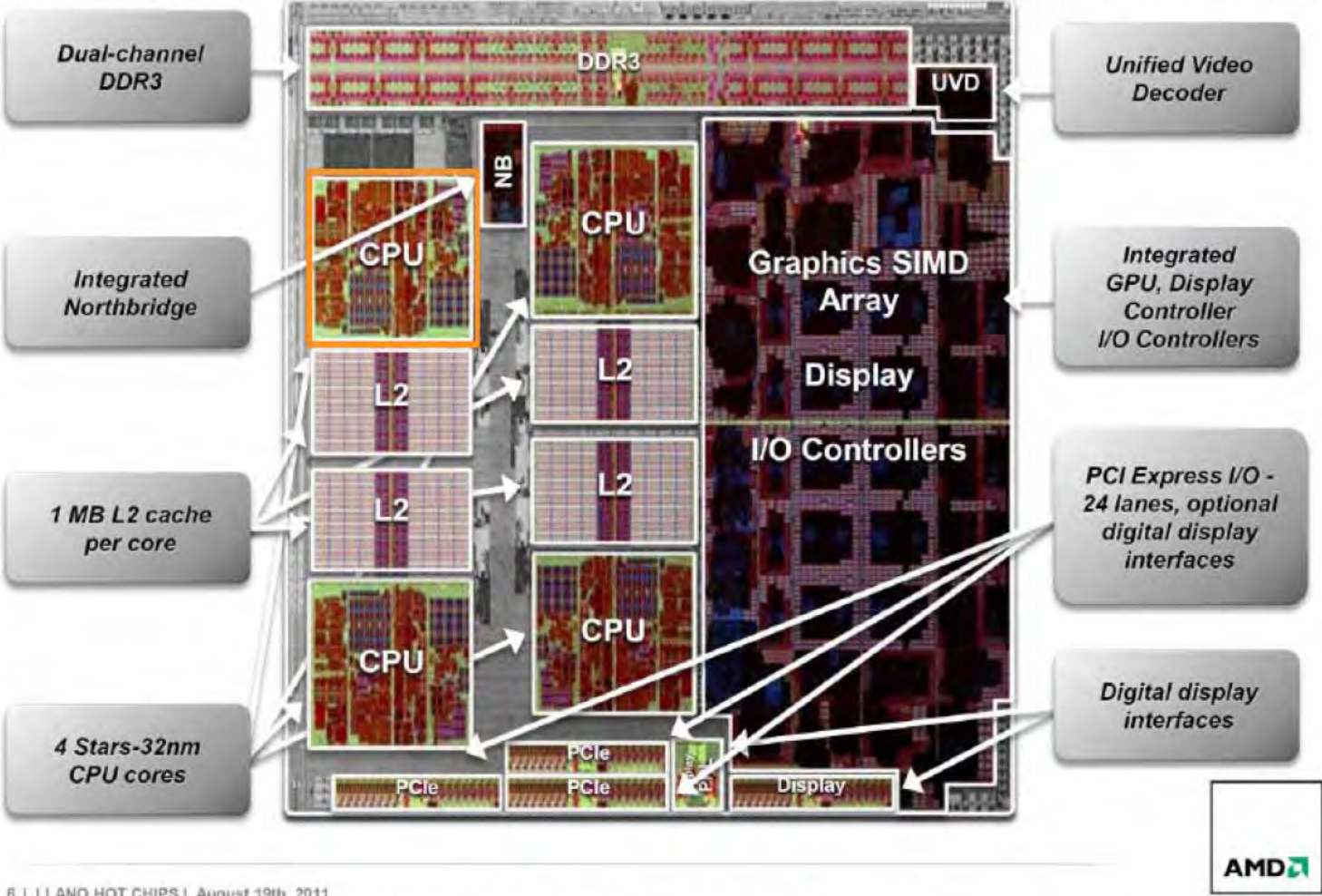
<u>Limitation</u>	<u>Contention</u>
<p>transistors, each of the second MOS transistors having a second threshold voltage;</p>	 <p>The diagram illustrates the die architecture of the AMD LLANO Fusion APU. It features four 32nm CPU cores arranged in a 2x2 grid, each with its own 1 MB L2 cache. A central Northbridge (NB) connects these cores to the system memory (DDR3) and the integrated GPU. The GPU consists of a Graphics SIMD Array, a Display controller, and I/O Controllers. The chip also includes a Unified Video Decoder (UVD) and various I/O interfaces such as PCIe and digital display outputs.</p> <p>Limitation: transistors, each of the second MOS transistors having a second threshold voltage;</p> <p>Contention:</p> <ul style="list-style-type: none"> Dual-channel DDR3 Integrated Northbridge 1 MB L2 cache per core 4 Stars-32nm CPU cores Unified Video Decoder Integrated GPU, Display Controller I/O Controllers PCI Express I/O - 24 lanes, optional digital display interfaces Digital display interfaces <p>AMD</p> <p>8 LLANO HOT CHIPS August 19th, 2011 Source: AMD'S "LLANO" FUSION APU, Hot Chips 23, 19th August 2011, page 6.</p>

Exhibit A.1

<u>Limitation</u>	<u>Contention</u>																											
	<p data-bbox="701 310 2368 418">Modern multi-VT standard cell design methodologies and structures such as those used in the Llano Accused Products use a mix of low Vt (LVt), regular Vt (RVt), long channel regular Vt (LC-RVt) and long channel high Vt (LC-Hvt) standard cells.</p> <div data-bbox="706 469 1615 857" style="border: 2px solid green; padding: 5px; margin: 10px auto; width: fit-content;"> <table border="1" style="border-collapse: collapse; text-align: center; width: 100%;"> <tr> <td style="background-color: #ffffcc;">uLvt <small>4</small></td> <td style="background-color: #e0ffff;">Lvt <small>2</small></td> <td style="background-color: #e0ffff;">Lvt filler <small>2</small></td> <td style="background-color: #ffe0ff;">Svt <small>4</small></td> <td style="background-color: #ffffcc;">uLvt <small>4</small></td> <td style="background-color: #e0ffff;">Lvt <small>2</small></td> <td style="background-color: #e0ffff;">Lvt filler <small>2</small></td> <td style="background-color: #ffe0ff;">Svt <small>4</small></td> </tr> <tr> <td style="background-color: #ffffcc;">uLvt <small>4</small></td> <td style="background-color: #e0ffff;">Lvt <small>2</small></td> <td style="background-color: #e0ffff;">Lvt filler <small>2</small></td> <td style="background-color: #ffe0ff;">Svt <small>4</small></td> <td style="background-color: #ffffcc;">uLvt <small>4</small></td> <td style="background-color: #e0ffff;">Lvt <small>2</small></td> <td style="background-color: #e0ffff;">Lvt filler <small>2</small></td> <td style="background-color: #ffe0ff;">Svt filler <small>2</small></td> <td style="background-color: #ffe0ff;">Svt <small>2</small></td> </tr> <tr> <td style="background-color: #ffffcc;">uLvt <small>4</small></td> <td style="background-color: #e0ffff;">Lvt <small>2</small></td> <td style="background-color: #e0ffff;">Lvt filler <small>2</small></td> <td style="background-color: #ffe0ff;">Svt filler <small>2</small></td> <td style="background-color: #ffe0ff;">Svt <small>2</small></td> <td style="background-color: #ffffcc;">uLvt <small>4</small></td> <td style="background-color: #e0ffff;">Lvt <small>2</small></td> <td style="background-color: #e0ffff;">Lvt filler <small>2</small></td> <td style="background-color: #ffe0ff;">Svt filler <small>2</small></td> <td style="background-color: #ffe0ff;">Svt <small>2</small></td> </tr> </table> </div> <p data-bbox="706 914 1865 1027">DVFS Characteristics Modern computer chips are designed using multiple types of transistors, i.e. a mixture of low-, medium-, and high-threshold transistors, to target different design tradeoffs, e.g. high-performance vs. low power.</p> <p data-bbox="706 1036 1865 1393">Low-threshold voltage (Low-Vt) devices are used in timing-critical paths, but have high leakage power. High-threshold voltage (High-Vt) devices have low leakage power but are slower, and are typically used in circuits that are off the timing-critical paths. Medium-threshold voltage (Mid-Vt) devices offer a tradeoff between High-Vt and Low-Vt devices by having medium power requirements and medium delay. In general, low power chips are designed using a larger percentage of High-Vt devices and high-performance chips with a larger percentage of Mid-Vt and Low-Vt devices. The host processor is assumed to execute compute-intensive code and will therefore be a high-performance device.</p>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt <small>4</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt <small>4</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt <small>4</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt filler <small>2</small>	Svt <small>2</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt filler <small>2</small>	Svt <small>2</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt filler <small>2</small>	Svt <small>2</small>
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<u>Limitation</u>	<u>Contention</u>
	<p data-bbox="701 272 2333 305"><i>Source:</i> Scrbak et al., DVFS Space Exploration in Power Constrained Processing-in-Memory Systems, pp. 4-5.</p> <p data-bbox="701 347 2386 418">The Accused Products contain a plurality of second MOS transistors, each of the second MOS transistors having a second threshold voltage:</p> <div data-bbox="701 428 1499 1143"> <p data-bbox="908 428 1311 727">(a) Core device width histogram by Vt type. The x-axis shows Vt types: LVt (0.7%), RVt (15.2%), LC-RVt (74.7%), HVt (8.1%), and LC-HVt (1.4%).</p> <p data-bbox="701 743 1499 1143">(b) Instance Count (x10000) vs. Timing Slack (ps). The graph shows two curves: 'Post Swapping' (black) and 'Pre Swapping (All RVt)' (red). Vertical dashed lines indicate Vt types: LVt, RVt, LCRVt, and HVt. The 'Post Swapping' curve shows a peak at approximately 25 ps, while the 'Pre Swapping' curve peaks at approximately 50 ps.</p> </div> <div data-bbox="1714 441 2182 1143"> <p data-bbox="1714 441 2182 766">(a) TDP power distribution at 1 V. A horizontal bar chart showing power distribution: CustomMacros (36%), StdCells (28%), Flops (17%), Clock (8%), Repeater (7%), Gater (4%), Dynamic (71%), and Static (29%).</p> <p data-bbox="1714 782 2182 1143">(b) Relative power improvement with respect to 45 nm generation core (normalized for performance). A bar chart comparing 45nm (red) and 32nm (green) for Static and Dynamic power. Static: 45nm is 100%, 32nm is 68%. Dynamic: 45nm is 100%, 32nm is 84%.</p> </div> <p data-bbox="701 1172 1516 1230">Fig. 10. (a) Core device width histogram by Vt type. (b) Using Vt swaps to reshape critical path timing opportunistically.</p> <p data-bbox="1542 1172 2360 1230">Fig. 11. (a) TDP power distribution at 1 V. (b) Relative power improvement with respect to 45 nm generation core (normalized for performance).</p> <p data-bbox="701 1273 2370 1344"><i>Source:</i> An x86-64 Core in 32 nm SOI CMOS, page 6 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 1, JANUARY 2011.</p>

	<u>Limitation</u>	<u>Contention</u>
1c	<p>a unit cell array comprised of said first and second unit cells laid in array form;</p>	<p>The Accused Products contain a unit cell array comprised of said first and second unit cells laid in array form:</p>  <p>8 LLANO HOT CHIPS August 19th, 2011 Source: AMD'S "LLANO" FUSION APU, Hot Chips 23, 19th August 2011, page 6.</p>

<u>Limitation</u>	<u>Contention</u>																											
	<p data-bbox="701 269 2368 375">Modern multi-Vt standard cell design methodologies and structures such as those used in the Llano Accused Products use a mix of low Vt (LVt), regular Vt (RVt), long channel regular Vt (LC-RVt) and long channel high Vt (LC-Hvt) standard cells.</p> <div data-bbox="709 428 1822 899" style="border: 1px solid orange; padding: 10px; margin: 10px auto; width: fit-content;"> <table border="1" style="border-collapse: collapse; text-align: center; width: 100%;"> <tr> <td style="background-color: #ffffcc;">uLvt <small>4</small></td> <td style="background-color: #e0f7fa;">Lvt <small>2</small></td> <td style="background-color: #e0f7fa;">Lvt filler <small>2</small></td> <td style="background-color: #fce4ec;">Svt <small>4</small></td> <td style="background-color: #ffffcc;">uLvt <small>4</small></td> <td style="background-color: #e0f7fa;">Lvt <small>2</small></td> <td style="background-color: #e0f7fa;">Lvt filler <small>2</small></td> <td style="background-color: #fce4ec;">Svt <small>4</small></td> </tr> <tr> <td style="background-color: #ffffcc;">uLvt <small>4</small></td> <td style="background-color: #e0f7fa;">Lvt <small>2</small></td> <td style="background-color: #e0f7fa;">Lvt filler <small>2</small></td> <td style="background-color: #fce4ec;">Svt <small>4</small></td> <td style="background-color: #ffffcc;">uLvt <small>4</small></td> <td style="background-color: #e0f7fa;">Lvt <small>2</small></td> <td style="background-color: #e0f7fa;">Lvt filler <small>2</small></td> <td style="background-color: #fce4ec;">Svt filler <small>2</small></td> <td style="background-color: #fce4ec;">Svt <small>2</small></td> </tr> <tr> <td style="background-color: #ffffcc;">uLvt <small>4</small></td> <td style="background-color: #e0f7fa;">Lvt <small>2</small></td> <td style="background-color: #e0f7fa;">Lvt filler <small>2</small></td> <td style="background-color: #fce4ec;">Svt filler <small>2</small></td> <td style="background-color: #fce4ec;">Svt <small>2</small></td> <td style="background-color: #ffffcc;">uLvt <small>4</small></td> <td style="background-color: #e0f7fa;">Lvt <small>2</small></td> <td style="background-color: #e0f7fa;">Lvt filler <small>2</small></td> <td style="background-color: #fce4ec;">Svt filler <small>2</small></td> <td style="background-color: #fce4ec;">Svt <small>2</small></td> </tr> </table> </div> <p data-bbox="709 959 1865 1073">DVFS Characteristics Modern computer chips are designed using multiple types of transistors, i.e. a mixture of low-, medium-, and high-threshold transistors, to target different design tradeoffs, e.g. high-performance vs. low power.</p> <p data-bbox="709 1081 1865 1154">Low-threshold voltage (Low-Vt) devices are used in timing-critical paths, but have high leakage power. High-threshold voltage (High-Vt) devices have</p>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt <small>4</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt <small>4</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt <small>4</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt filler <small>2</small>	Svt <small>2</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt filler <small>2</small>	Svt <small>2</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt filler <small>2</small>	Svt <small>2</small>
uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt <small>4</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt <small>4</small>																					
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uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt filler <small>2</small>	Svt <small>2</small>	uLvt <small>4</small>	Lvt <small>2</small>	Lvt filler <small>2</small>	Svt filler <small>2</small>	Svt <small>2</small>																			

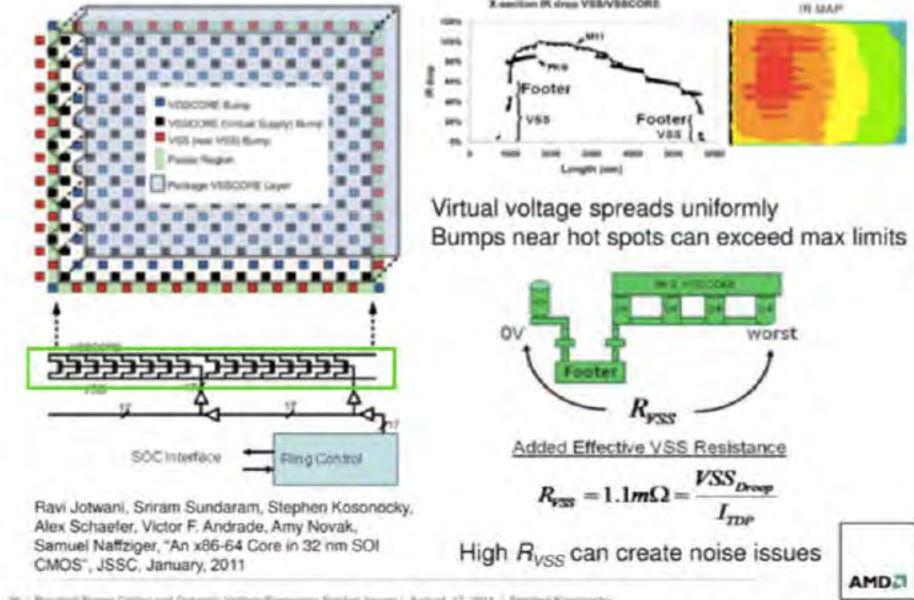
	<u>Limitation</u>	<u>Contention</u>
		<p>low leakage power but are slower, and are typically used in circuits that are off the timing-critical paths. Medium-threshold voltage (Mid-Vt) devices offer a tradeoff between High-Vt and Low-Vt devices by having medium power requirements and medium delay. In general, low power chips are designed using a larger percentage of High-Vt devices and high-performance chips with a larger percentage of Mid-Vt and Low-Vt devices. The host processor is assumed to execute compute-intensive code and will therefore be a high-performance device.</p> <p><i>Source:</i> Scrbak et al., DVFS Space Exploration in Power Constrained Processing-in-Memory Systems, pp. 4-5.</p>
1d	<p>a power switch disposed around said unit cell array and comprised of a plurality of third MOS transistors, each of the third MOS transistors having the second threshold voltage; and</p>	<p>The Accused Products contain a power switch disposed around said unit cell array:</p> <p>LLANO CPU CORE RING GATING WITH PACKAGE LAYER ASSIST</p> <p>Virtual voltage spreads uniformly Bumps near hot spots can exceed max limits</p> <p>Added Effective VSS Resistance</p> $R_{VSS} = 1.1m\Omega = \frac{VSS_{Drop}}{I_{DDP}}$ <p>High R_{VSS} can create noise issues</p> <p>Ravi Jotwani, Sriram Sundaram, Stephen Kosonocky, Alex Schaefer, Victor F. Andrade, Amy Novak, Samuel Naffziger, "An x86-64 Core in 32 nm SOI CMOS", JSSC, January, 2011</p> <p>AMD</p> <p><i>Source: PRACTICAL POWER GATING AND DYNAMIC VOLTAGE/FREQUENCY SCALING by Stephen</i></p>

Exhibit A.1

	<u>Limitation</u>	<u>Contention</u>
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Kosonocky, page 50.

The Accused Products contain a plurality of third MOS transistors:
LLANO CPU CORE RING GATING WITH PACKAGE LAYER ASSIST

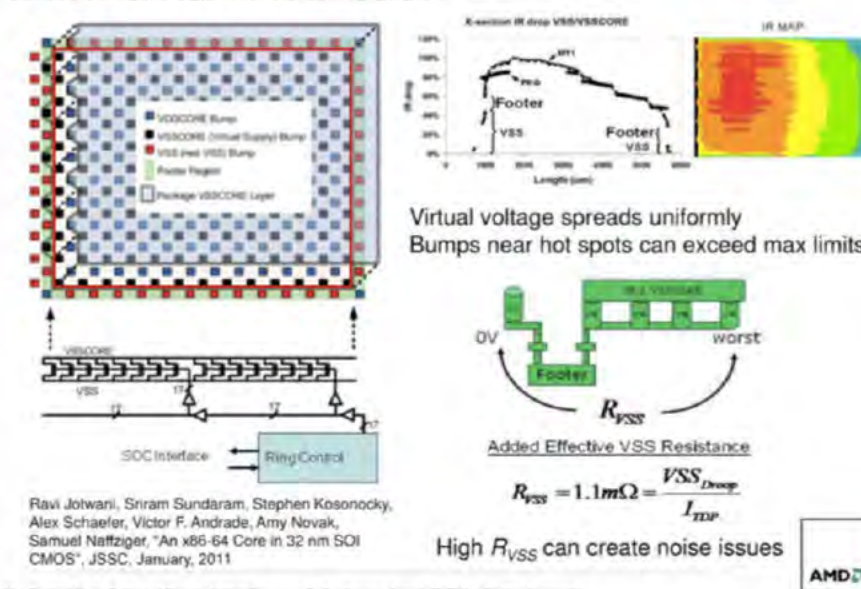


Ravi Jotwani, Sriram Sundaram, Stephen Kosonocky, Alex Schaefer, Victor F. Andrade, Amy Novak, Samuel Naffziger, "An x86-64 Core in 32 nm SOI CMOS", JSSC, January, 2011

Source: *PRACTICAL POWER GATING AND DYNAMIC VOLTAGE/FREQUENCY SCALING* by Stephen Kosonocky, page 50

Each of the third MOS transistors of the power gate ring has the second threshold voltage.

	<u>Limitation</u>	<u>Contention</u>
		<p style="text-align: center;">VII. POWER GATING</p> <p>We defined a low-power mode called core-level C6 (CC6) to allow core-level power gating [5] during periods of inactivity. The core is isolated from the supply during CC6 by a power-gate ring surrounding the CPU and L2 cache pair, allowing core level power down in a chip with multiple cores attached to a common power supply. The SOI process enables the gating of VSS (not VDD), constructing the power-gate with regular V_t nMOS logic devices without the need for extra processing steps to reduce on-state resistance [6]. Fig. 12(a) describes the core operations controlled by the power management system for CC6 entry and exit sequences.</p> <p>Fig. 12(b) details the connections of the power-gate ring with respect to the core and the C4 bumps. In addition to two 16X M10 and M11 on-die metal layers, a low-impedance package layer connected to the die by C4 bumps is dedicated for use as a virtual-ground layer, eliminating the need for any ultra-thick silicon metallization layer [6]. The low-impedance package layer</p> <p><i>Source: An x86-64 Core in 32 nm SOI CMOS, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 1, JANUARY 2011, page 6.</i></p>
1e	a plurality of input/output circuits disposed around said unit cell array.	The Accused Products contain a plurality of input/output circuits disposed around said unit cell array.

	<u>Limitation</u>	<u>Contention</u>
		<p>LLANO CPU CORE RING GATING WITH PACKAGE LAYER ASSIST</p>  <p>Virtual voltage spreads uniformly Bumps near hot spots can exceed max limits</p> <p>Added Effective VSS Resistance</p> $R_{VSS} = 1.1m\Omega = \frac{VSS_{Deep}}{I_{MP}}$ <p>High R_{VSS} can create noise issues</p> <p>AMD</p> <p><small>Ravi Jotwani, Sriram Sundaram, Stephen Kosonocky, Alex Schaefer, Victor F. Andrade, Amy Novak, Samuel Naffziger, "An x86-64 Core in 32 nm SOI CMOS", JSSC, January, 2011</small></p> <p><small>IR - Practical Power Gating and Dynamic Voltage/Frequency Scaling Issues August 11, 2011 Stephen Kosonocky</small></p>
2	A semiconductor integrated circuit device according to claim 1, wherein said power switch is turned off during standby and turned on when taken active.	The power gate ring of the Accused Products is turned off during standby and turned on when taken active.

Source: PRACTICAL POWER GATING AND DYNAMIC VOLTAGE/FREQUENCY SCALING by Stephen Kosonocky, page 50.


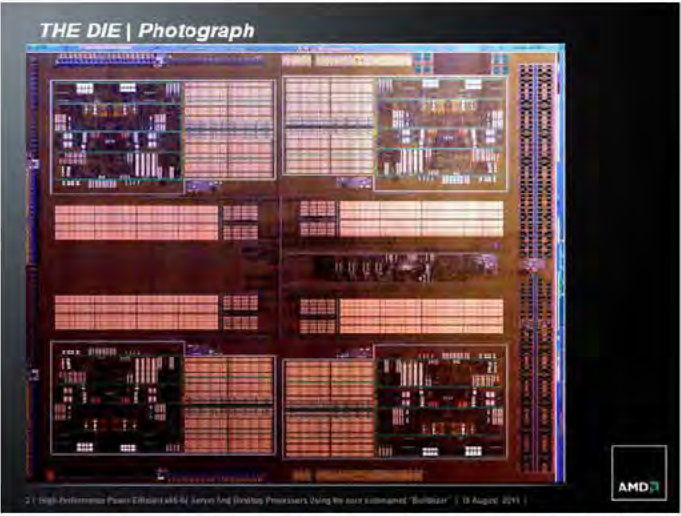
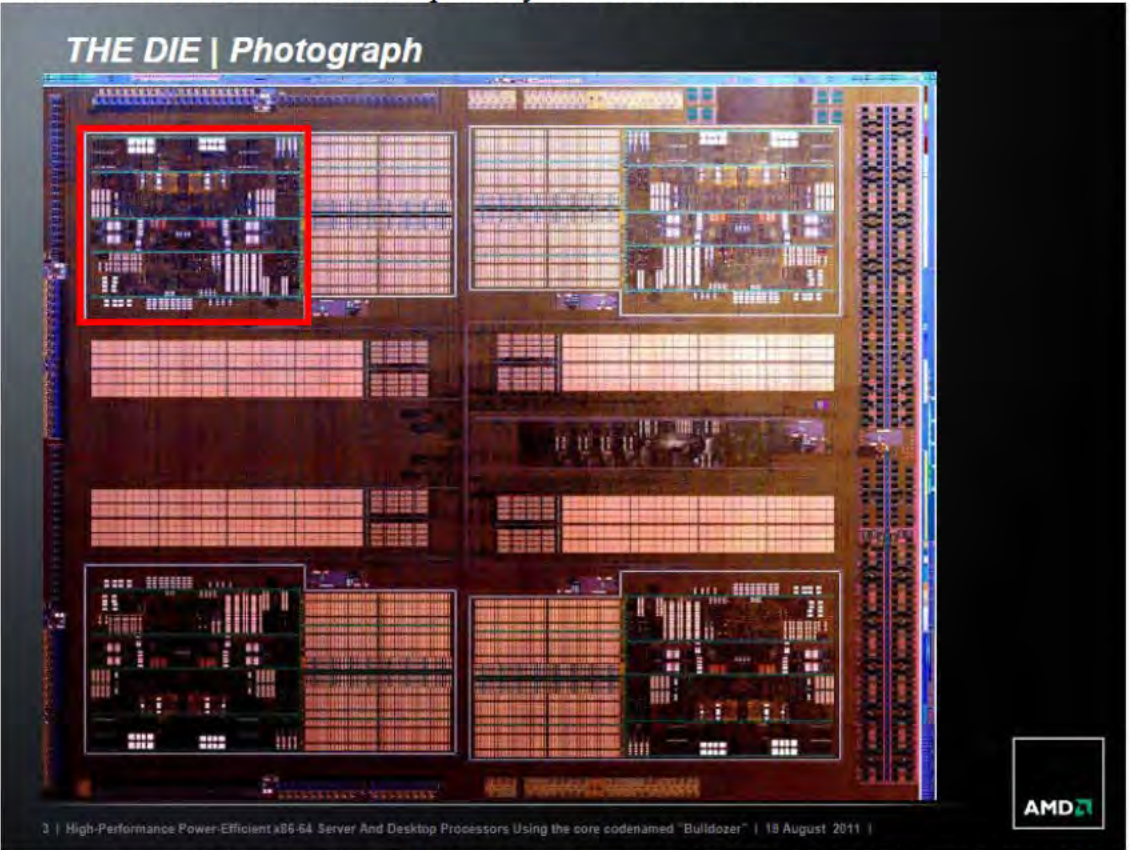
<u>Limitation</u>	<u>Contention</u>
	<p><u>Two major knobs have emerged for controlling power</u></p> <ol style="list-style-type: none"> 1. Dynamic Voltage and Frequency Scaling <ul style="list-style-type: none"> – Optimize performance for the application while it's running 2. Power Gating <ul style="list-style-type: none"> – <u>Gate power during idle periods</u> <p style="text-align: center;">Each present unique challenges for implementation and optimization</p> <div style="text-align: right;">  </div> <p><small>8.1 Practical Power Gating and Dynamic Voltage/Frequency Scaling Issues / August 17, 2011 / Stephen Kosonocky</small></p> <p><i>Source: PRACTICAL POWER GATING AND DYNAMIC VOLTAGE/FREQUENCY SCALING by Stephen Kosonocky, page 8.</i></p>

Exhibit A.2: Preliminary Infringement Contention Claim Chart for U.S. Patent 6,239,614

Accused Products: AMD Family 15h Bulldozer/Piledriver APU Processors

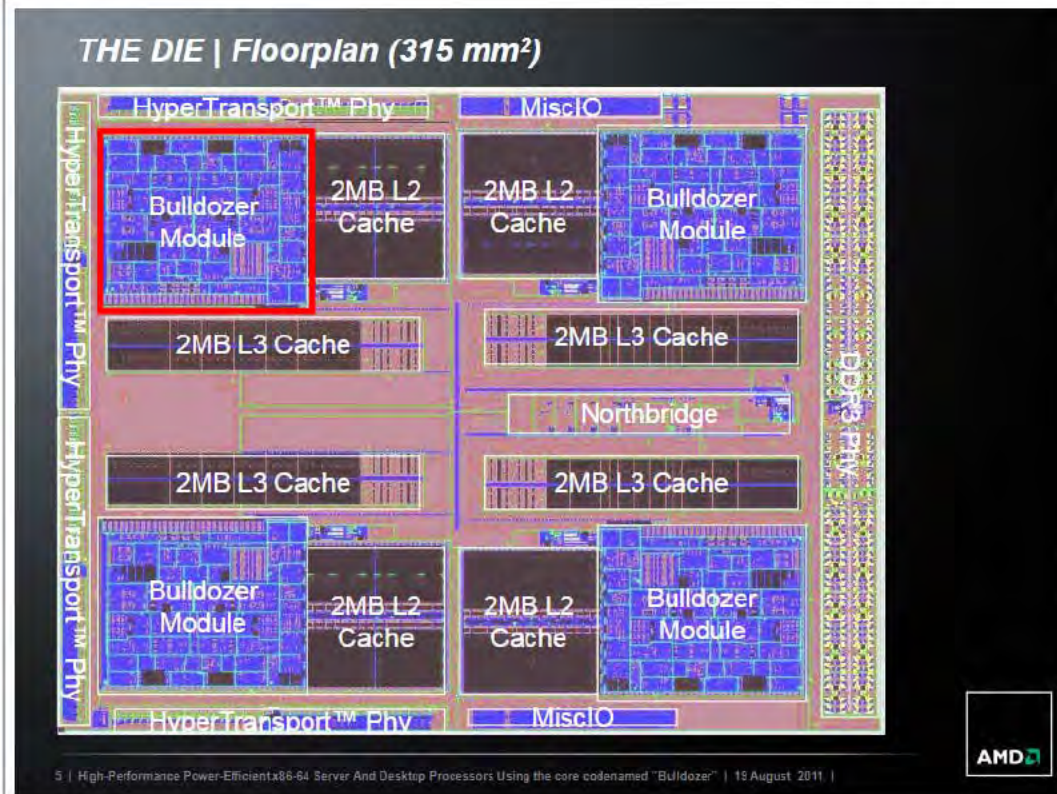
These preliminary infringement contentions were prepared without the benefit of the Court’s claim construction or the parties’ exchange of constructions. As of the date of these contentions, AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court’s constructions or to account for new information that becomes available.

	<u>Limitation</u>	<u>Contention</u>
1p	A semiconductor integrated circuit device, comprising:	<p>To the extent the preamble is a limitation, the Accused Products are a semiconductor integrated device.</p>  <p><i>Source: Sean White, HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named “Bulldozer”, August 18, 2011, page 3.</i></p> <p>Aquila contends that products containing Piledriver cores operate similarly to the Bulldozer cores with respect to the limitations of the asserted claims.</p>

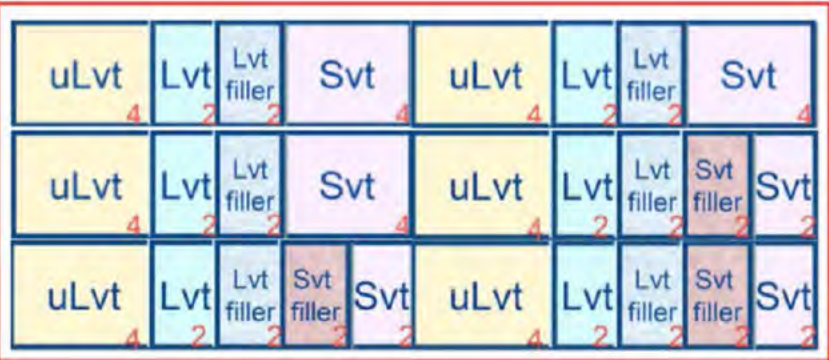
	<u>Limitation</u>	<u>Contention</u>
1a	<p>a plurality of first unit cells each including a plurality of first MOS transistors, each of the first MOS transistors having a first threshold voltage;</p>	<p>The Accused Product discloses a plurality of first unit cells.</p>  <p><i>Source: Sean White, HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer", August 18, 2011, page 3.</i></p>

Limitation


Contention



Source: Sean White, *HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer"*, August 18, 2011, page 5.

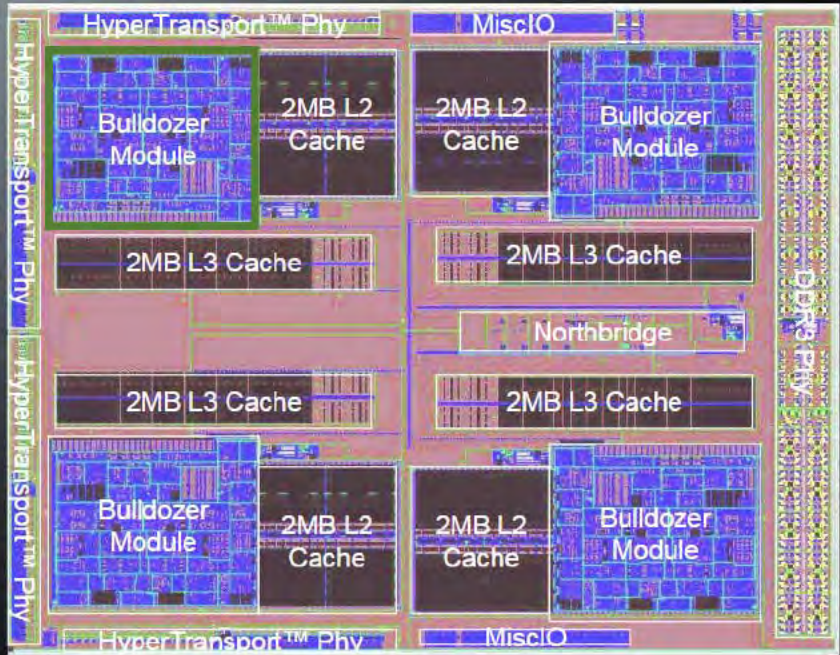
<u>Limitation</u>	<u>Contention</u>
	<p>The Bulldozer module contains 84 unique custom macros and 317,000 scannable flops. Module-level VSS power gating (C6) is used to reduce leakage power by approximately 95% when both cores are idle [4]. The 32 nm SOI process provides three transistor V_T types (low, regular, and high), with longer channel lengths used to achieve even finer-grained trade-offs between leakage and delay. V_T's used across the design consist mostly of regular (47%) and long-channel regular (46%), with less than 1% low-V_T used for the most critical paths.</p> <p><i>Source: McIntyre et al., Design Of The Two-Core x86-64 AMD "Bulldozer" Module In 32 nm SOI CMOS, IEEE Journal of Solid-State Circuits, Vol. 47, No. 1, January 2012, page 165.</i></p> <p>Modern multi-VT standard cell design methodologies and structures such as those used in the Llano Accused Products use a mix of low Vt (LVt), regular Vt (RVt), long channel regular Vt (LC-RVt) and long channel high Vt (LC-Hvt) standard cells.</p> 


	<u>Limitation</u>	<u>Contention</u>
		<p>DVFS Characteristics Modern computer chips are designed using multiple types of transistors, i.e. a mixture of low-, medium-, and high-threshold transistors, to target different design tradeoffs, e.g. high-performance vs. low power.</p> <p>Low-threshold voltage (Low-Vt) devices are used in timing-critical paths, but have high leakage power. High-threshold voltage (High-Vt) devices have low leakage power but are slower, and are typically used in circuits that are off the timing-critical paths. Medium-threshold voltage (Mid-Vt) devices offer a tradeoff between High-Vt and Low-Vt devices by having medium power requirements and medium delay. In general, low power chips are designed using a larger percentage of High-Vt devices and high-performance chips with a larger percentage of Mid-Vt and Low-Vt devices. The host processor is assumed to execute compute-intensive code and will therefore be a high-performance device.</p> <p><i>Source:</i> Scrbak et al., DVFS Space Exploration in Power Constrained Processing-in-Memory Systems, pp. 4-5.</p> <p>The Accused Products contain a plurality of first MOS transistors, each of the first MOS transistors having a first threshold voltage.</p>


<u>Limitation</u>	<u>Contention</u>																																							
	<p>THE DIE Process Technology</p> <ul style="list-style-type: none"> • 32-nm Silicon-On-Insulator (SOI) Hi-K Metal Gate (HKMG) process from GlobalFoundries • 11-metal-layer-stack • Low-k dielectric • Dual strain liners and eSiGe to improve performance. • Multiple VT (HVT, RVT, LVT) and long-channel transistors. <table border="1" data-bbox="1481 350 1849 919"> <thead> <tr> <th>Layer</th> <th>Type</th> <th>Pitch</th> </tr> </thead> <tbody> <tr> <td>CPP¹</td> <td>-</td> <td>130 nm</td> </tr> <tr> <td>M01</td> <td>1x</td> <td>104 nm</td> </tr> <tr> <td>M02</td> <td>1x</td> <td>104 nm</td> </tr> <tr> <td>M03</td> <td>1x</td> <td>104 nm</td> </tr> <tr> <td>M04</td> <td>1.3x</td> <td>130 nm</td> </tr> <tr> <td>M05</td> <td>1.3x</td> <td>130 nm</td> </tr> <tr> <td>M06</td> <td>2x</td> <td>208 nm</td> </tr> <tr> <td>M07</td> <td>2x</td> <td>208 nm</td> </tr> <tr> <td>M08</td> <td>2x</td> <td>208 nm</td> </tr> <tr> <td>M09</td> <td>4x</td> <td>416 nm</td> </tr> <tr> <td>M10</td> <td>16x</td> <td>1.6 μm</td> </tr> <tr> <td>M11</td> <td>16x</td> <td>1.6 μm</td> </tr> </tbody> </table> <p>¹ Contacted poly pitch</p>  <p><small>6 High-Performance Power-Efficient x86-64 Server And Desktop Processors Using the core codenamed "Bulldozer" 19 August 2011 </small></p> <p><i>Source: Sean White, HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer", August 18, 2011, page 6.</i></p>	Layer	Type	Pitch	CPP ¹	-	130 nm	M01	1x	104 nm	M02	1x	104 nm	M03	1x	104 nm	M04	1.3x	130 nm	M05	1.3x	130 nm	M06	2x	208 nm	M07	2x	208 nm	M08	2x	208 nm	M09	4x	416 nm	M10	16x	1.6 μm	M11	16x	1.6 μm
Layer	Type	Pitch																																						
CPP ¹	-	130 nm																																						
M01	1x	104 nm																																						
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M05	1.3x	130 nm																																						
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	<u>Limitation</u>	<u>Contention</u>																																							
		<p>JOTWANI <i>et al.</i>: AN x86-64 CORE IN 32 nm SOI CMOS 167</p> <div style="display: flex; justify-content: space-around;"> <div data-bbox="774 349 1518 1023"> <p>(a) Core device width histogram by Vt type:</p> <table border="1"> <tr><th>Vt Type</th><th>Percentage</th></tr> <tr><td>LVT</td><td>0.7%</td></tr> <tr><td>RVT</td><td>15.2%</td></tr> <tr><td>LC-RVT</td><td>74.7%</td></tr> <tr><td>HVT</td><td>8.1%</td></tr> <tr><td>LC-HVT</td><td>1.4%</td></tr> </table> <p>(b) Timing Slack (ps) vs Instance Count (x10000):</p> <p>Post Swapping Vt Types: LVT, RVT, LCRVt, HVT</p> <p>Post Swapping (black line) vs Pre Swapping (All RVT) (red line)</p> </div> <div data-bbox="1720 357 2163 1023"> <p>(a) TDP power distribution at 1 V:</p> <table border="1"> <tr><th>Component</th><th>Percentage</th></tr> <tr><td>CustomMacros</td><td>36%</td></tr> <tr><td>StdCells</td><td>28%</td></tr> <tr><td>Flops</td><td>17%</td></tr> <tr><td>Clock</td><td>8%</td></tr> <tr><td>Repeater</td><td>7%</td></tr> <tr><td>Gate</td><td>4%</td></tr> <tr><td>Dynamic</td><td>71%</td></tr> <tr><td>Static</td><td>29%</td></tr> </table> <p>(b) Relative power improvement with respect to 45 nm generation core (normalized for performance):</p> <table border="1"> <tr><th>Power Type</th><th>45nm (%)</th><th>32nm (%)</th></tr> <tr><td>Static</td><td>100%</td><td>68%</td></tr> <tr><td>Dynamic</td><td>100%</td><td>84%</td></tr> </table> </div> </div> <p>Fig. 10. (a) Core device width histogram by Vt type. (b) Using Vt swaps to reshape critical path timing opportunistically.</p> <p>Fig. 11. (a) TDP power distribution at 1 V. (b) Relative power improvement with respect to 45 nm generation core (normalized for performance).</p> <p><i>Source: An x86-64 Core in 32 nm SOI CMOS, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 1, JANUARY 2011, page 6.</i></p>	Vt Type	Percentage	LVT	0.7%	RVT	15.2%	LC-RVT	74.7%	HVT	8.1%	LC-HVT	1.4%	Component	Percentage	CustomMacros	36%	StdCells	28%	Flops	17%	Clock	8%	Repeater	7%	Gate	4%	Dynamic	71%	Static	29%	Power Type	45nm (%)	32nm (%)	Static	100%	68%	Dynamic	100%	84%
Vt Type	Percentage																																								
LVT	0.7%																																								
RVT	15.2%																																								
LC-RVT	74.7%																																								
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StdCells	28%																																								
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1b	a plurality of second unit cells each including a plurality of second MOS transistors, each of the	The Accused Products contain a plurality of second unit cells.																																							

<u>Limitation</u>	<u>Contention</u>
<p>second MOS transistors having a second threshold voltage;</p>	<div data-bbox="766 263 1741 993" data-label="Image"> </div> <p data-bbox="766 998 2432 1063"><i>Source: Sean White, HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer", August 18, 2011, page 3.</i></p>

<u>Limitation</u>	<u>Contention</u>
	<p data-bbox="827 289 1295 326">THE DIE Floorplan (315 mm²)</p>  <p data-bbox="803 1024 1588 1040">5 High-Performance Power-Efficient x86-64 Server And Desktop Processors Using the core codenamed "Bulldozer" 18 August 2011 </p> <p data-bbox="1723 948 1809 1032">AMD</p> <p data-bbox="763 1094 2435 1162"><i>Source: Sean White, HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer", August 18, 2011, page 5.</i></p> <p data-bbox="763 1240 2327 1308">The Accused Products contain a plurality of second MOS transistors, each of the second MOS transistors having a second threshold voltage.</p>

<u>Limitation</u>	<u>Contention</u>																																							
	<p>THE DIE Process Technology</p> <ul style="list-style-type: none"> • 32-nm Silicon-On-Insulator (SOI) Hi-K Metal Gate (HKMG) process from GlobalFoundries • 11-metal-layer-stack • Low-k dielectric • Dual strain liners and eSiGe to improve performance. • Multiple VT (HVT, <u>RVT</u>, LVT) and long-channel transistors. <table border="1" data-bbox="1545 357 1948 982"> <thead> <tr> <th>Layer</th> <th>Type</th> <th>Pitch</th> </tr> </thead> <tbody> <tr> <td>CPP¹</td> <td>-</td> <td>130 nm</td> </tr> <tr> <td>M01</td> <td>1x</td> <td>104 nm</td> </tr> <tr> <td>M02</td> <td>1x</td> <td>104 nm</td> </tr> <tr> <td>M03</td> <td>1x</td> <td>104 nm</td> </tr> <tr> <td>M04</td> <td>1.3x</td> <td>130 nm</td> </tr> <tr> <td>M05</td> <td>1.3x</td> <td>130 nm</td> </tr> <tr> <td>M06</td> <td>2x</td> <td>208 nm</td> </tr> <tr> <td>M07</td> <td>2x</td> <td>208 nm</td> </tr> <tr> <td>M08</td> <td>2x</td> <td>208 nm</td> </tr> <tr> <td>M09</td> <td>4x</td> <td>416 nm</td> </tr> <tr> <td>M10</td> <td>16x</td> <td>1.6 μm</td> </tr> <tr> <td>M11</td> <td>16x</td> <td>1.6 μm</td> </tr> </tbody> </table> <p>¹ Contacted poly pitch</p>  <p><small>6 High-Performance Power-Efficient x86-64 Server And Desktop Processors Using the core codenamed "Bulldozer" 19 August 2011 </small></p> <p><i>Source: Sean White, HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer", August 18, 2011, page 6.</i></p>	Layer	Type	Pitch	CPP ¹	-	130 nm	M01	1x	104 nm	M02	1x	104 nm	M03	1x	104 nm	M04	1.3x	130 nm	M05	1.3x	130 nm	M06	2x	208 nm	M07	2x	208 nm	M08	2x	208 nm	M09	4x	416 nm	M10	16x	1.6 μm	M11	16x	1.6 μm
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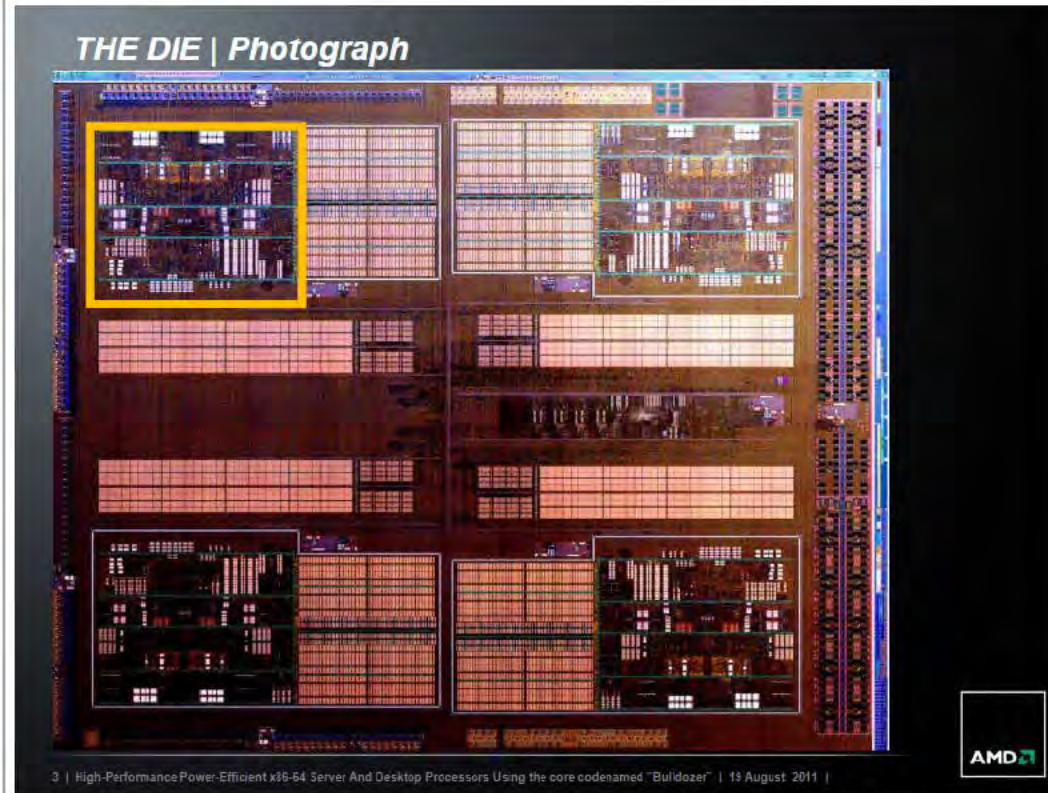
<u>Limitation</u>	<u>Contention</u>
	<p>The Bulldozer module contains 84 unique custom macros and 317,000 scannable flops. Module-level VSS power gating (C6) is used to reduce leakage power by approximately 95% when both cores are idle [4]. The 32 nm SOI process provides three transistor V_T types (low, regular, and high), with longer channel lengths used to achieve even finer-grained trade-offs between leakage and delay. V_T's used across the design consist mostly of regular (47%) and long-channel regular (46%), with less than 1% low-V_T used for the most critical paths.</p> <p><i>Source: McIntyre et al., Design Of The Two-Core x86-64 AMD "Bulldozer" Module In 32 nm SOI CMOS, IEEE Journal of Solid-State Circuits, Vol. 47, No. 1, January 2012, page 165.</i></p> <p>Modern multi-VT standard cell design methodologies and structures such as those used in the Llano Accused Products use a mix of low Vt (LVt), regular Vt (RVt), long channel regular Vt (LC-RVt) and long channel high Vt (LC-Hvt) standard cells.</p> 

	<u>Limitation</u>	<u>Contention</u>
		<p>DVFS Characteristics Modern computer chips are designed using multiple types of transistors, i.e. a mixture of low-, medium-, and high-threshold transistors, to target different design tradeoffs, e.g. high-performance vs. low power.</p> <p>Low-threshold voltage (Low-Vt) devices are used in timing-critical paths, but have high leakage power. High-threshold voltage (High-Vt) devices have low leakage power but are slower, and are typically used in circuits that are off the timing-critical paths. Medium-threshold voltage (Mid-Vt) devices offer a tradeoff between High-Vt and Low-Vt devices by having medium power requirements and medium delay. In general, low power chips are designed using a larger percentage of High-Vt devices and high-performance chips with a larger percentage of Mid-Vt and Low-Vt devices. The host processor is assumed to execute compute-intensive code and will therefore be a high-performance device.</p> <p><i>Source:</i> Scrbak et al., DVFS Space Exploration in Power Constrained Processing-in-Memory Systems, pp. 4-5.</p> <p>The Accused Products contain a plurality of second MOS transistors, each of the second MOS transistors having a second threshold voltage:</p>

	<u>Limitation</u>	<u>Contention</u>																																							
		<div style="display: flex; justify-content: space-around;"> <div data-bbox="774 272 1564 987"> <p>(a) Core device width histogram by Vt type:</p> <table border="1"> <tr><th>Vt Type</th><th>Percentage</th></tr> <tr><td>LVT</td><td>0.7%</td></tr> <tr><td>RVT</td><td>15.2%</td></tr> <tr><td>LC-RVT</td><td>74.7%</td></tr> <tr><td>HVT</td><td>8.1%</td></tr> <tr><td>LC-HVT</td><td>1.4%</td></tr> </table> <p>(b) Instance Count x10000 vs Timing Slack (ps):</p> <p>Post Swapping Vt Types: LVT, RVT, LCRVT, HVT</p> <p>Post Swapping (black line) vs Pre Swapping (All RVT) (red line)</p> </div> <div data-bbox="1787 284 2244 987"> <p>(a) TDP power distribution at 1 V:</p> <table border="1"> <tr><th>Component</th><th>Percentage</th></tr> <tr><td>CustomMacros</td><td>36%</td></tr> <tr><td>StdCells</td><td>28%</td></tr> <tr><td>Flops</td><td>17%</td></tr> <tr><td>Clock</td><td>8%</td></tr> <tr><td>Repeater</td><td>7%</td></tr> <tr><td>Gate</td><td>4%</td></tr> <tr><td>Dynamic</td><td>71%</td></tr> <tr><td>Static</td><td>29%</td></tr> </table> <p>(b) Relative power improvement with respect to 45 nm generation core (normalized for performance):</p> <table border="1"> <tr><th>Power Type</th><th>45nm (%)</th><th>32nm (%)</th></tr> <tr><td>Static</td><td>100%</td><td>68%</td></tr> <tr><td>Dynamic</td><td>100%</td><td>84%</td></tr> </table> </div> </div> <p>Fig. 10. (a) Core device width histogram by Vt type. (b) Using Vt swaps to reshape critical path timing opportunistically.</p> <p>Fig. 11. (a) TDP power distribution at 1 V. (b) Relative power improvement with respect to 45 nm generation core (normalized for performance).</p> <p><i>Source: An x86-64 Core in 32 nm SOI CMOS, page 6 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 1, JANUARY 2011</i></p>	Vt Type	Percentage	LVT	0.7%	RVT	15.2%	LC-RVT	74.7%	HVT	8.1%	LC-HVT	1.4%	Component	Percentage	CustomMacros	36%	StdCells	28%	Flops	17%	Clock	8%	Repeater	7%	Gate	4%	Dynamic	71%	Static	29%	Power Type	45nm (%)	32nm (%)	Static	100%	68%	Dynamic	100%	84%
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1c	a unit cell array comprised of said first and second unit cells laid in array form;	The Accused Products contain a unit cell array comprised of said first and second unit cells laid in array form:																																							

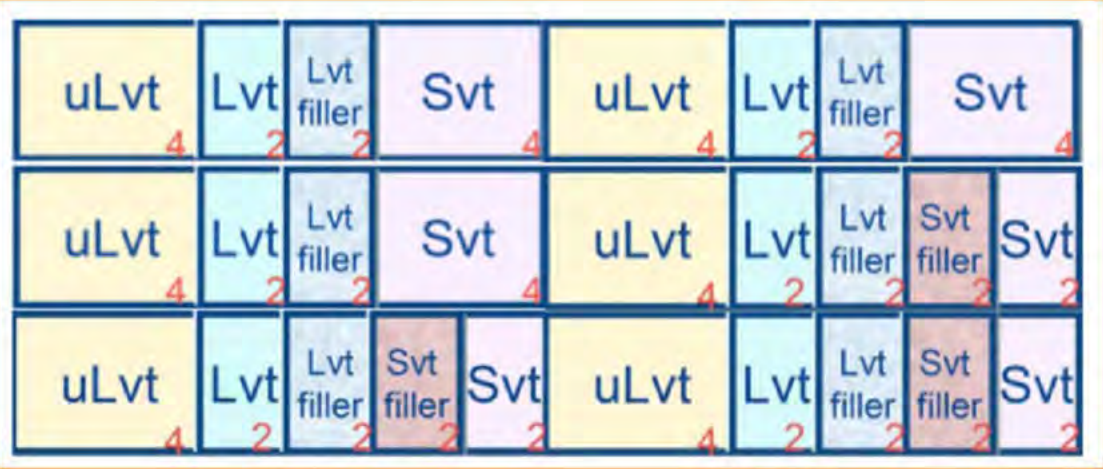
Limitation

Contention



Source: Sean White, *HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer"*, August 18, 2011, page 3.

Modern multi-VT standard cell design methodologies and structures such as those used in the Llano Accused Products use a mix of low Vt (LVt), regular Vt (RVt), long channel regular Vt (LC-RVt) and long channel high Vt (LC-Hvt) standard cells.

<u>Limitation</u>	<u>Contention</u>
	 <p>DVFS Characteristics Modern computer chips are designed using multiple types of transistors, i.e. a mixture of low-, medium-, and high-threshold transistors, to target different design tradeoffs, e.g. high-performance vs. low power.</p> <p>Low-threshold voltage (Low-Vt) devices are used in timing-critical paths, but have high leakage power. High-threshold voltage (High-Vt) devices have low leakage power but are slower, and are typically used in circuits that are off the timing-critical paths. Medium-threshold voltage (Mid-Vt) devices offer a tradeoff between High-Vt and Low-Vt devices by having medium power requirements and medium delay. In general, low power chips are designed using a larger percentage of High-Vt devices and high-performance chips with a larger percentage of Mid-Vt and Low-Vt devices. The host processor is assumed to execute compute-intensive code and will therefore be a high-performance device.</p> <p><i>Source:</i> Scrbak et al., DVFS Space Exploration in Power Constrained Processing-in-Memory Systems, pp. 4-5.</p>

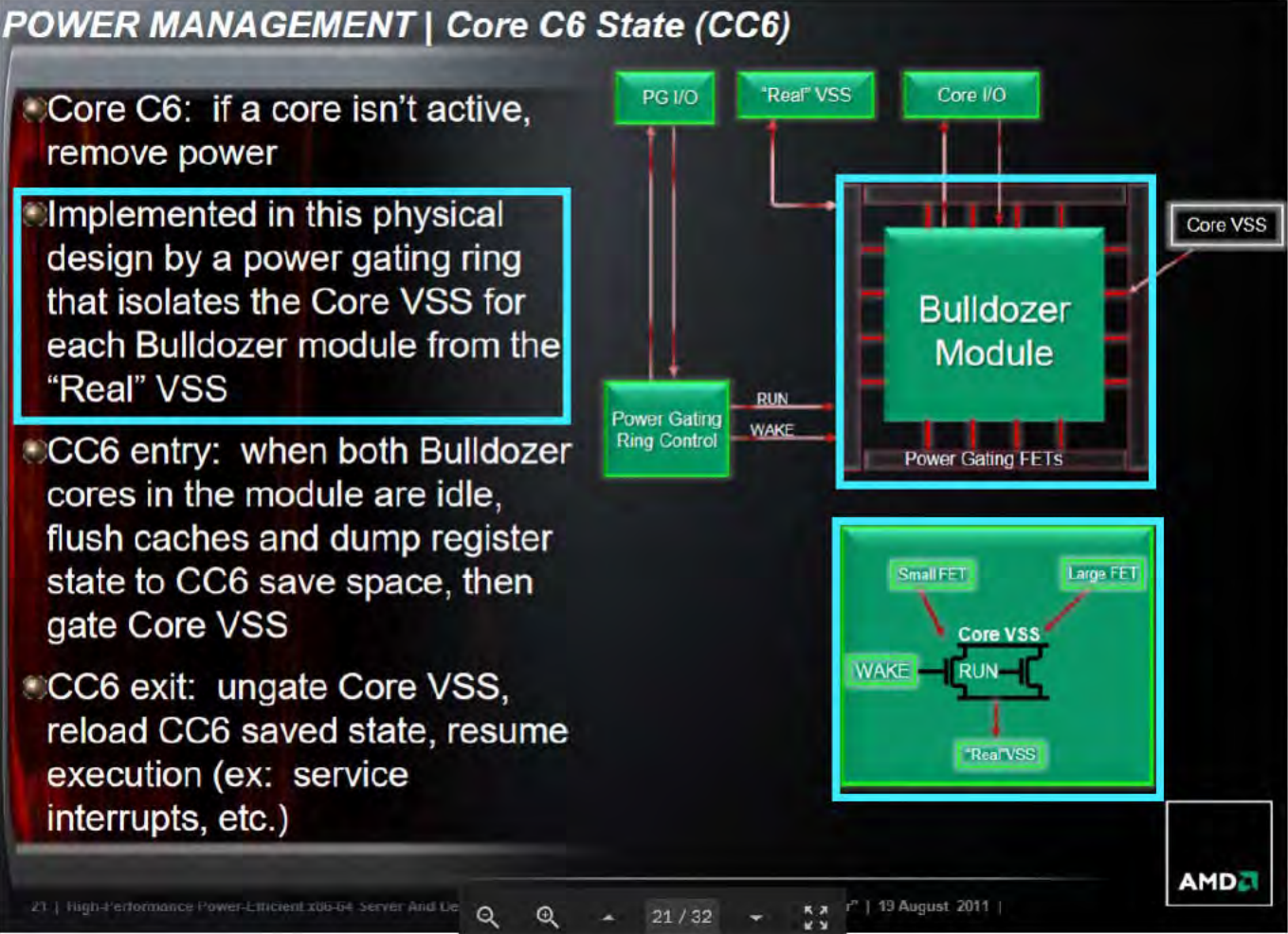

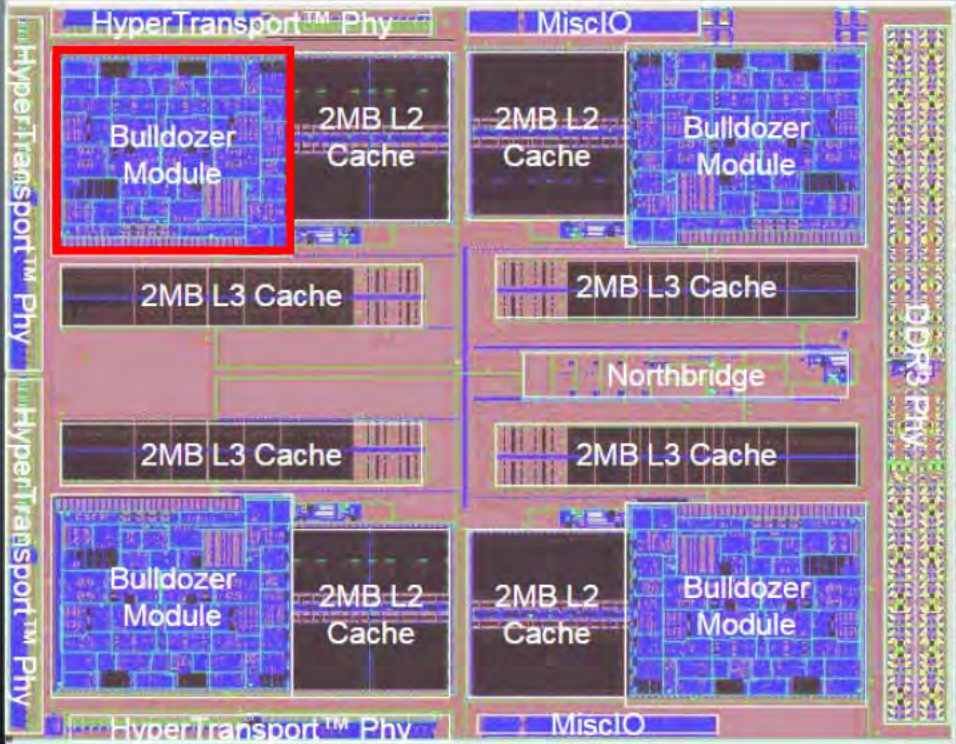
	<u>Limitation</u>	<u>Contention</u>
1d	<p>a power switch disposed around said unit cell array and comprised of a plurality of third MOS transistors, each of the third MOS transistors having the second threshold voltage; and</p>	<p>The Accused Products contain a power switch disposed around said unit cell array and comprised of a plurality of third MOS transistors.</p>  <p>POWER MANAGEMENT Core C6 State (CC6)</p> <ul style="list-style-type: none"> Core C6: if a core isn't active, remove power Implemented in this physical design by a power gating ring that isolates the Core VSS for each Bulldozer module from the "Real" VSS CC6 entry: when both Bulldozer cores in the module are idle, flush caches and dump register state to CC6 save space, then gate Core VSS CC6 exit: ungate Core VSS, reload CC6 saved state, resume execution (ex: service interrupts, etc.) <p>21 High-Performance Power-Efficient x86-64 Server And De... 19 August 2011 AMD</p>

Exhibit A.2

<u>Limitation</u>	<u>Contention</u>																																							
	<p data-bbox="763 269 2435 337"><i>Source: Sean White, HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer", August 18, 2011, page 21.</i></p> <p data-bbox="763 378 1951 407">Each of the third MOS transistors of the Accused Products has the second threshold voltage:</p> <div data-bbox="774 412 2064 1370" style="background-color: #333; color: #fff; padding: 10px;"> <p data-bbox="787 469 1311 508">THE DIE Process Technology</p> <ul data-bbox="838 553 1534 1101" style="list-style-type: none"> <li data-bbox="838 553 1534 621">● 32-nm Silicon-On-Insulator (SOI) Hi-K Metal Gate (HKMG) process from GlobalFoundries <li data-bbox="838 691 1145 721">● 11-metal-layer-stack <li data-bbox="838 797 1085 826">● Low-k dielectric <li data-bbox="838 902 1400 964">● Dual strain liners and eSiGe to improve performance. <li data-bbox="838 1040 1481 1101">● Multiple VT (HVT, RVT, LVT) and long-channel transistors. <table data-bbox="1588 509 2010 1162" style="margin-left: auto; margin-right: auto; border-collapse: collapse; text-align: center;"> <thead> <tr style="background-color: #c00; color: #fff;"> <th>Layer</th> <th>Type</th> <th>Pitch</th> </tr> </thead> <tbody> <tr><td>CPP¹</td><td>-</td><td>130 nm</td></tr> <tr><td>M01</td><td>1x</td><td>104 nm</td></tr> <tr><td>M02</td><td>1x</td><td>104 nm</td></tr> <tr><td>M03</td><td>1x</td><td>104 nm</td></tr> <tr><td>M04</td><td>1.3x</td><td>130 nm</td></tr> <tr><td>M05</td><td>1.3x</td><td>130 nm</td></tr> <tr><td>M06</td><td>2x</td><td>208 nm</td></tr> <tr><td>M07</td><td>2x</td><td>208 nm</td></tr> <tr><td>M08</td><td>2x</td><td>208 nm</td></tr> <tr><td>M09</td><td>4x</td><td>416 nm</td></tr> <tr><td>M10</td><td>16x</td><td>1.6 μm</td></tr> <tr><td>M11</td><td>16x</td><td>1.6 μm</td></tr> </tbody> </table> <p data-bbox="1623 1187 1870 1216">¹ Contacted poly pitch</p> <div data-bbox="1938 1243 2040 1344" style="text-align: right; margin-top: 10px;">  </div> <p data-bbox="822 1336 1776 1354" style="font-size: 8px; margin-top: 10px;">© High-Performance Power-Efficient x86-64 Server And Desktop Processors Using the core codenamed "Bulldozer" 19 August 2011 </p> </div> <p data-bbox="763 1373 2435 1403"><i>Source: Sean White, HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the</i></p>	Layer	Type	Pitch	CPP ¹	-	130 nm	M01	1x	104 nm	M02	1x	104 nm	M03	1x	104 nm	M04	1.3x	130 nm	M05	1.3x	130 nm	M06	2x	208 nm	M07	2x	208 nm	M08	2x	208 nm	M09	4x	416 nm	M10	16x	1.6 μm	M11	16x	1.6 μm
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	<u>Limitation</u>	<u>Contention</u>
		<p><i>core code named "Bulldozer", August 18, 2011, page 6.</i></p> <p>Each of the third MOS transistors of the power gate ring has the second threshold voltage.</p> <div data-bbox="784 386 1575 1068" style="border: 2px solid black; padding: 5px;"> <p style="text-align: center;">VII. POWER GATING</p> <p>We defined a low-power mode called core-level C6 (CC6) to allow core-level power gating [5] during periods of inactivity. The core is isolated from the supply during CC6 by a power-gate ring surrounding the CPU and L2 cache pair, allowing core level power down in a chip with multiple cores attached to a common power supply. The SOI process enables the gating of VSS (not VDD), constructing the power-gate with regular V_t nMOS logic devices without the need for extra processing steps to reduce on-state resistance [6]. Fig. 12(a) describes the core operations controlled by the power management system for CC6 entry and exit sequences.</p> <p>Fig. 12(b) details the connections of the power-gate ring with respect to the core and the C4 bumps. In addition to two 16X M10 and M11 on-die metal layers, a low-impedance package layer connected to the die by C4 bumps is dedicated for use as a virtual-ground layer, eliminating the need for any ultra-thick silicon metallization layer [6]. The low-impedance package layer</p> </div> <p><i>Source: An x86-64 Core in 32 nm SOI CMOS, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 1, JANUARY 2011, page 6.</i></p>
1e	a plurality of input/output circuits disposed around said unit cell array.	The Accused Product has a plurality of input/output circuits disposed around the Bulldozer module.

	<u>Limitation</u>	<u>Contention</u>
		<p data-bbox="846 292 1384 332">THE DIE Floorplan (315 mm²)</p>  <p data-bbox="819 1128 1720 1153">5 High-Performance Power-Efficient x86-64 Server And Desktop Processors Using the core codenamed "Bulldozer" 19 August, 2011 </p> <p data-bbox="1868 1047 1962 1144">AMD</p> <p data-bbox="766 1209 2432 1274"><i>Source: Sean White, HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer", August 18, 2011, page 5.</i></p>
2	A semiconductor integrated circuit	The power gate ring is turned off during standby and turned on when the core exits C6 state.

<u>Limitation</u>	<u>Contention</u>
<p>device according to claim 1, wherein said power switch is turned off during standby and turned on when taken active.</p>	<div data-bbox="774 310 1849 769" style="border: 2px solid black; padding: 10px;"> <p>The Bulldozer module contains 84 unique custom macros and 317,000 scannable flops. Module-level VSS power gating (C6) is used to reduce leakage power by approximately 95% when both cores are idle [4]. The 32 nm SOI process provides three transistor V_T types (low, regular, and high), with longer channel lengths used to achieve even finer-grained trade-offs between leakage and delay. V_T's used across the design consist mostly of regular (47%) and long-channel regular (46%), with less than 1% low-V_T used for the most critical paths.</p> </div> <p><i>Source: McIntyre et al., Design Of The Two-Core x86-64 AMD "Bulldozer" Module In 32 nm SOI CMOS, IEEE Journal of Solid-State Circuits, Vol. 47, No. 1, January 2012, page 165.</i></p>

Limitation

Contention

POWER MANAGEMENT | Core C6 State (CC6)

- Core C6: if a core isn't active, remove power
- Implemented in this physical design by a power gating ring that isolates the Core VSS for each Bulldozer module from the "Real" VSS
- CC6 entry: when both Bulldozer cores in the module are idle, flush caches and dump register state to CC6 save space, then gate Core VSS
- CC6 exit: ungate Core VSS, reload CC6 saved state, resume execution (ex: service interrupts, etc.)

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Source: Sean White, *HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer"*, August 18, 2011, page 21.

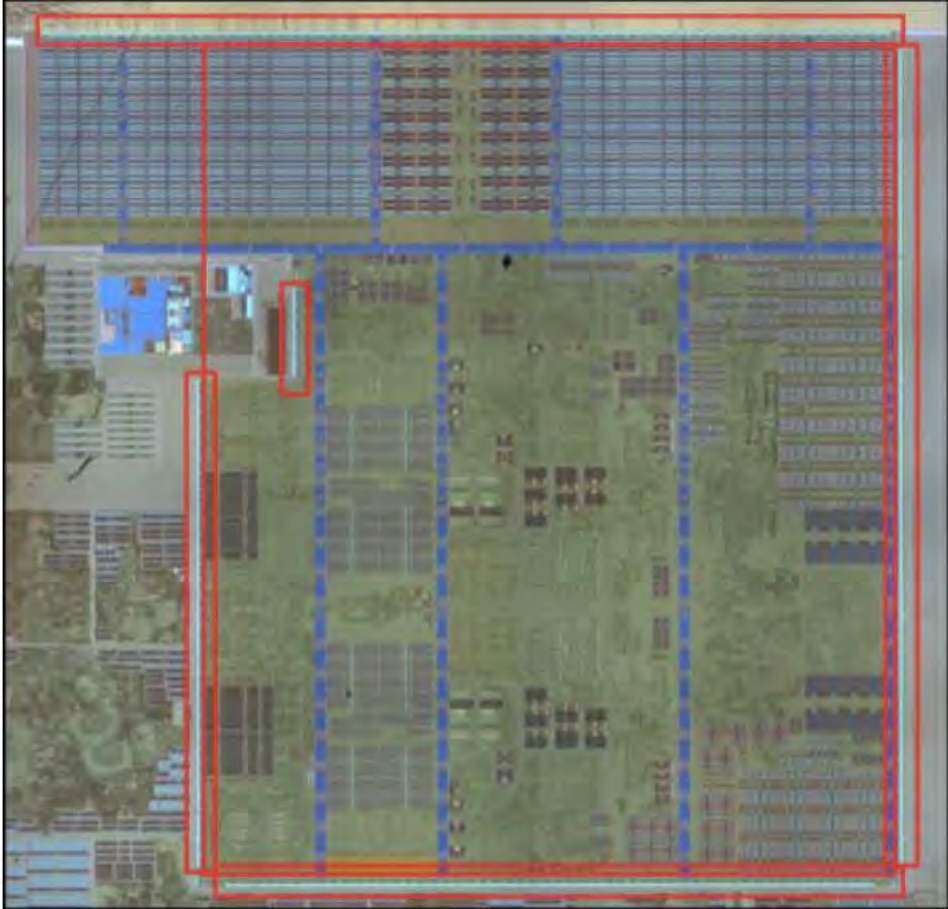
Exhibit A.3: Preliminary Infringement Contention Charts for U.S. Patent 6,239,614

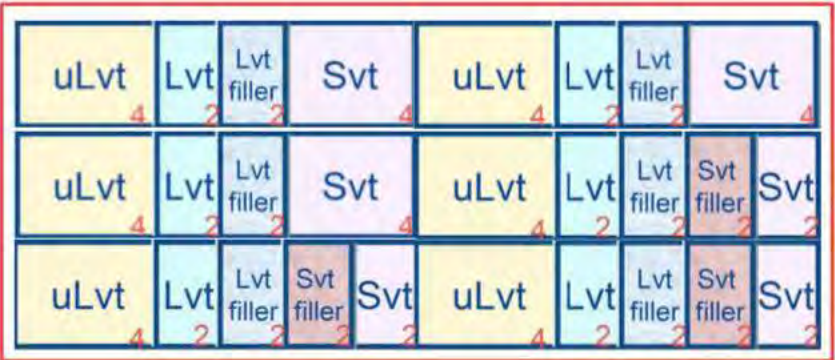
Accused Product: AMD APUs containing Excavator cores (Representative Product: AMD Carrizo APU Processors)

These preliminary infringement contentions were prepared without the benefit of the Court's claim construction or the parties' exchange of constructions. As of the date of these contentions, AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court's constructions or to account for new information that becomes available.

	<u>Limitation</u>	<u>Contention</u>
1p	A semiconductor integrated circuit device, comprising:	To the extent the preamble is a limitation, the Accused Products are semiconductor integrated circuits.

<u>Limitation</u>	<u>Contention</u>
	<div data-bbox="774 264 1884 1138" data-label="Image"> <p>The image is a die photograph of an AMD 6th Generation A-Series Processor. It shows a complex integrated circuit with various functional blocks. At the top, there's a section labeled 'DDR/PHY'. Below that, two 'X86 Module' blocks are visible. In the center, the 'Northbridge' is labeled. To the left, the 'Southbridge' is labeled vertically. At the bottom, 'PCIe/Display' is labeled. On the right side, a large, grid-like area is labeled 'GPU'. The die is shown against a dark background.</p> </div> <p data-bbox="774 1141 2333 1179">Source: Krishnan, Energy Efficient Graphics and Multimedia in 28nm Carrizo APU Hot Chips 27, p. 2.</p> <p data-bbox="774 1252 2446 1369">To the extent that the power gate ring implemented in this product operates similarly to the Bulldozer or Llano power gate rings, for example in terms of the threshold voltages of the MOS transistors in the various unit cells and the power switch, Aquila contends that the charts applicable to those products apply equally to this product,</p>

	<u>Limitation</u>	<u>Contention</u>
		and incorporates those charts by reference.
1a	a plurality of first unit cells each including a plurality of first MOS transistors, each of the first MOS transistors having a first threshold voltage;	<p>The Accused Products disclose a plurality of first unit cells:</p> 


<u>Limitation</u>	<u>Contention</u>
	<p>Modern multi-Vt standard cell design methodologies and structures such as those used in the Llano Accused Products use a mix of low Vt (LVt), regular Vt (RVt), long channel regular Vt (LC-RVt) and long channel high Vt (LC-Hvt) standard cells.</p>  <p>DVFS Characteristics Modern computer chips are designed using multiple types of transistors, i.e. a mixture of low-, medium-, and high-threshold transistors, to target different design tradeoffs, e.g. high-performance vs. low power.</p> <p>Low-threshold voltage (Low-Vt) devices are used in timing-critical paths, but have high leakage power. High-threshold voltage (High-Vt) devices have low leakage power but are slower, and are typically used in circuits that are off the timing-critical paths. Medium-threshold voltage (Mid-Vt) devices offer a tradeoff between High-Vt and Low-Vt devices by having medium power requirements and medium delay. In general, low power chips are designed using a larger percentage of High-Vt devices and high-performance chips with a larger percentage of Mid-Vt and Low-Vt devices. The host processor is assumed to execute compute-intensive code and will therefore be a high-performance device.</p> <p><i>Source:</i> Scrbak et al., DVFS Space Exploration in Power Constrained Processing-in-Memory Systems, pp. 4-5.</p>

<u>Limitation</u>	<u>Contention</u>
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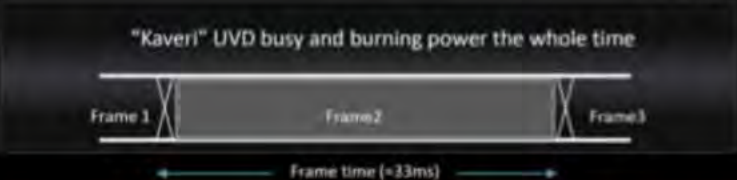
The Accused Products disclose a plurality of first MOS transistors, each of the first MOS transistors having a first threshold voltage, e.g., RVt:

DYNAMIC UVD POWER GATING


- ▲ Dynamic inter frame power gating controlled by microcontroller firmware
 - Pipeline idle detection enables header/footer power gating of the entire IP
- ▲ Dynamic power gating along with low power hardening of the video decoder enables CZ to negate the bigger video decoder needed for H.265 offload
 - ~3X better than KV in net leakage profile²¹



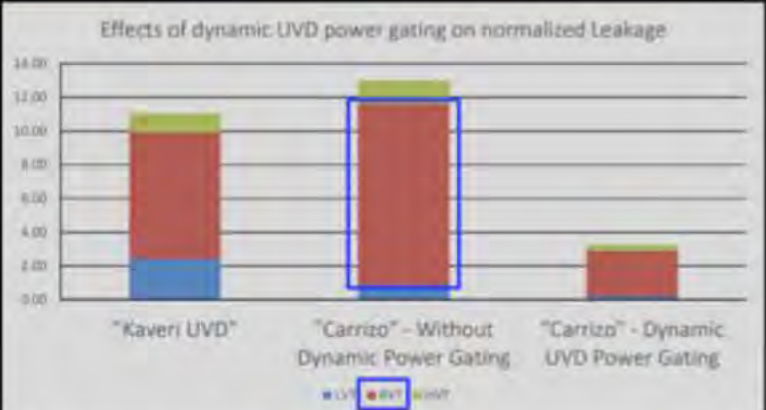
"Kaveri" UVD busy and burning power the whole time



"Carrizo" UVD and power gates itself off and PUTS DRAM into low power mode




Effects of dynamic UVD power gating on normalized Leakage:




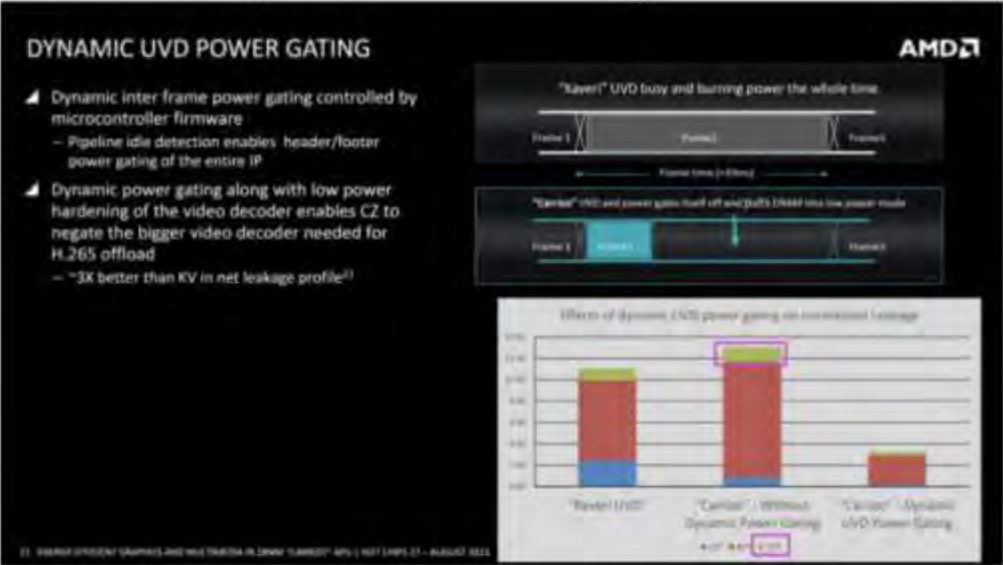
Scenario	UVD	RVt	RVHT
"Kaveri UVD"	~2.5	~8.0	~1.0
"Carrizo" - Without Dynamic Power Gating	~1.0	~11.0	~1.0
"Carrizo" - Dynamic UVD Power Gating	~0.5	~2.5	~0.5


21. ENERGY EFFICIENT GRAPHICS AND MULTIMEDIA IN 28NM "CARRIZO" APU | HOT CHIPS 27 - AUGUST 2015

Source: *ENERGY EFFICIENT GRAPHICS AND MULTIMEDIA IN 28NM CARRIZO APU, page 21 HOT CHIPS 27 – AUGUST 2015*


	<u>Limitation</u>	<u>Contention</u>
1b	<p>a plurality of second unit cells each including a plurality of second MOS transistors, each of the second MOS transistors having a second threshold voltage;</p>	<p>The Accused Products disclose a plurality of second unit cells:</p>  <p>Modern multi-VT standard cell design methodologies and structures such as those used in the Llano Accused Products use a mix of low Vt (LVt), regular Vt (RVt), long channel regular Vt (LC-RVt) and long channel high Vt</p>

<u>Limitation</u>	<u>Contention</u>
	<p data-bbox="776 269 1137 305">(LC-Hvt) standard cells.</p>  <p data-bbox="787 800 1946 911">DVFS Characteristics Modern computer chips are designed using multiple types of transistors, i.e. a mixture of low-, medium-, and high-threshold transistors, to target different design tradeoffs, e.g. high-performance vs. low power.</p> <p data-bbox="787 919 1946 1279">Low-threshold voltage (Low-Vt) devices are used in timing-critical paths, but have high leakage power. High-threshold voltage (High-Vt) devices have low leakage power but are slower, and are typically used in circuits that are off the timing-critical paths. Medium-threshold voltage (Mid-Vt) devices offer a tradeoff between High-Vt and Low-Vt devices by having medium power requirements and medium delay. In general, low power chips are designed using a larger percentage of High-Vt devices and high-performance chips with a larger percentage of Mid-Vt and Low-Vt devices. The host processor is assumed to execute compute-intensive code and will therefore be a high-performance device.</p> <p data-bbox="787 1287 2408 1323"><i>Source:</i> Scrbak et al., DVFS Space Exploration in Power Constrained Processing-in-Memory Systems, pp. 4-5.</p>


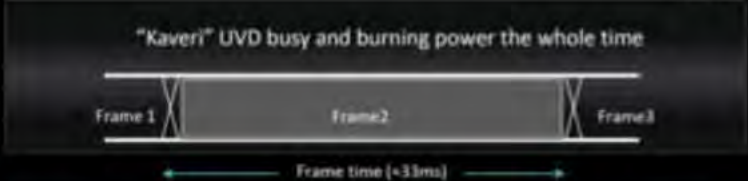

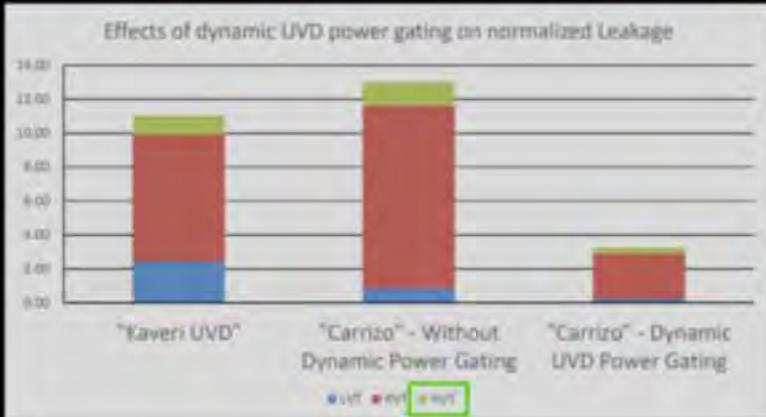
	<u>Limitation</u>	<u>Contention</u>
		<p>The Accused Products disclose a plurality of second unit cells each including a plurality of second MOS transistors having a second threshold voltage:</p>  <p>The slide includes the following text:</p> <ul style="list-style-type: none"> Dynamic inter frame power gating controlled by microcontroller firmware <ul style="list-style-type: none"> Pipeline idle detection enables header/footer power gating of the entire IP Dynamic power gating along with low power hardening of the video decoder enables CZ to negate the bigger video decoder needed for H.265 offload <ul style="list-style-type: none"> ~3X better than KV in net leakage profile⁽¹⁾ <p>The diagrams show: <ul style="list-style-type: none"> "Stayer" UVD busy and burning power the whole time (Frame 1, Frame 2, Frame 3). "Carrier" UVD and power gate half of its pipeline during low power mode (Frame 1, Frame 2, Frame 3). <p>The bar chart, titled "Effects of dynamic UVD power gating on measured leakage", compares three scenarios: <ul style="list-style-type: none"> "Stayer" UVD: High leakage (approx. 1.2 units). "Carrier" UVD without Dynamic Power Gating: High leakage (approx. 1.2 units). "Carrier" UVD with Dynamic UVD Power Gating: Low leakage (approx. 0.4 units). </p> <p>Source: <i>ENERGY EFFICIENT GRAPHICS AND MULTIMEDIA IN 28NM CARRIZO APU, HOT CHIPS 27 – AUGUST 2015</i>, page 21.</p> </p>
1c	a unit cell array comprised of said first and second unit cells laid in array form;	The Accused Products disclose a unit cell array comprised of said first and second unit cells laid in array form:

	<u>Limitation</u>	<u>Contention</u>
		 <p>The image is a micrograph of a semiconductor device. It shows a central unit cell array, which is a grid of small, repeating structures. This array is surrounded by a power gate ring, which is a larger, rectangular structure. The power gate ring is highlighted with a red border, and the unit cell array is highlighted with a blue border. The background of the micrograph is a light green color, and there are various other structures and patterns visible, including some larger rectangular blocks and smaller, more complex structures.</p>
1d	<p>a power switch disposed around said unit cell array and comprised of a plurality of third MOS transistors, each of the third MOS transistors having the second threshold</p>	<p>The Accused Products disclose a power gate ring disposed around said unit cell array:</p>

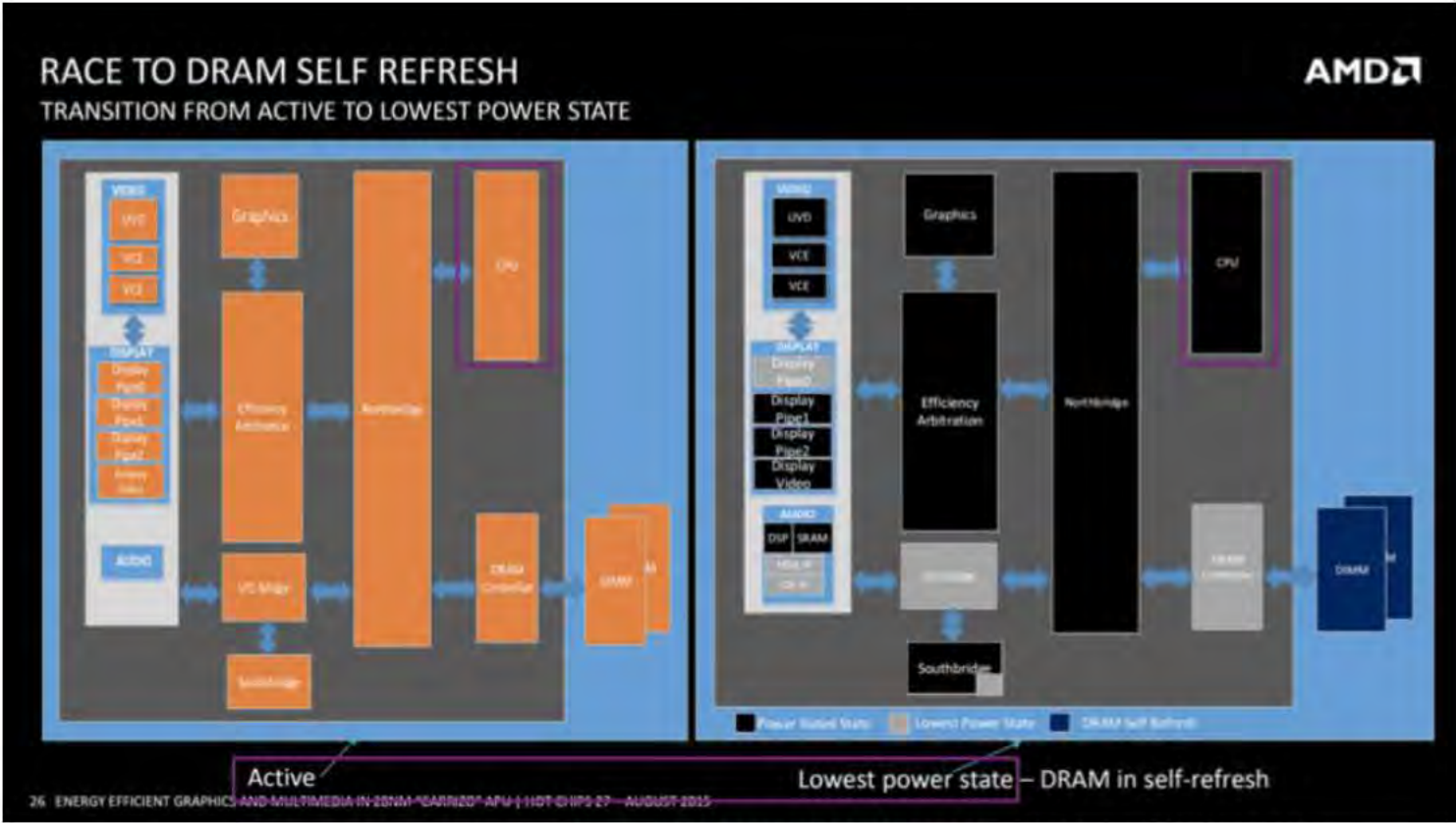
<u>Limitation</u>	<u>Contention</u>
voltage; and	<div data-bbox="787 272 1876 792" style="border: 2px solid black; padding: 10px;"> <p>Instead of the distributed power gate headers used in Steamroller, a power gate ring is used to reduce the size of the power switch required to support Excavator's higher power density. Distributed headers must be sized to accommodate the worst case current draw within small regions of the design, whereas a power gate ring need only be sized to accommodate the worst case across the entire power gated region. This enables a 3.5–4× reduction in FET width in the Excavator power switch and a corresponding leakage power reduction when it is in CC6 (sleep state).</p> </div> <p><i>Source: Carrizo: A High Performance, Energy Efficient 28 nm APU, page 5 IEEE JOURNAL OF SOLID-STATE CIRCUITS</i></p>

<u>Limitation</u>	<u>Contention</u>
	 <p>The Accused Products disclose a power switch comprised of a plurality of third MOS transistors:</p>

<u>Limitation</u>	<u>Contention</u>
	<div data-bbox="787 277 1870 784" style="border: 2px solid black; padding: 10px;"> <p>Instead of the distributed power gate headers used in Steamroller, a power gate ring is used to reduce the size of the power switch required to support Excavator's higher power density. Distributed headers must be sized to accommodate the worst case current draw within small regions of the design, whereas a power gate ring need only be sized to accommodate the worst case across the entire power gated region. This enables a 3.5–4× reduction in FET width in the Excavator power switch and a corresponding leakage power reduction when it is in CC6 (sleep state).</p> </div> <p><i>Source: Carrizo: A High Performance, Energy Efficient 28 nm APU, IEEE JOURNAL OF SOLID-STATE CIRCUITS, page 5.</i></p> <p>The Accused Products disclose each of the third MOS transistors having the second threshold voltage:</p>

	<u>Limitation</u>	<u>Contention</u>																
		<div data-bbox="782 263 2378 1156"> <h3 style="text-align: center;">DYNAMIC UVD POWER GATING</h3> <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <ul style="list-style-type: none"> ▲ Dynamic inter frame power gating controlled by microcontroller firmware <ul style="list-style-type: none"> - Pipeline idle detection enables header/footer power gating of the entire IP ▲ Dynamic power gating along with low power hardening of the video decoder enables CZ to negate the bigger video decoder needed for H.265 offload <ul style="list-style-type: none"> - ~3X better than KV in net leakage profile²¹ </div> <div style="width: 50%; text-align: right;">  <div style="margin-top: 10px;"> <p>"Kaveri" UVD busy and burning power the whole time</p>  </div> <div style="margin-top: 10px;"> <p>"Carrizo" UVD and power gates itself off and puts DRAM into low power mode</p>  </div> <div style="margin-top: 10px;"> <p>Effects of dynamic UVD power gating on normalized Leakage</p>  <table border="1" style="margin-top: 5px; width: 100%; border-collapse: collapse;"> <caption>Normalized Leakage Data (Estimated from Chart)</caption> <thead> <tr> <th>Configuration</th> <th>UVT (Blue)</th> <th>UVD (Red)</th> <th>UVT+UVD (Green)</th> </tr> </thead> <tbody> <tr> <td>"Kaveri UVD"</td> <td>~2.0</td> <td>~7.5</td> <td>~9.5</td> </tr> <tr> <td>"Carrizo" - Without Dynamic Power Gating</td> <td>~1.0</td> <td>~10.5</td> <td>~11.5</td> </tr> <tr> <td>"Carrizo" - Dynamic UVD Power Gating</td> <td>~0.5</td> <td>~2.0</td> <td>~2.5</td> </tr> </tbody> </table> </div> </div> <p style="font-size: small; margin-top: 10px;">21. ENERGY EFFICIENT GRAPHICS AND MULTIMEDIA IN 28NM "CARRIZO" APU HOT CHIPS 27 – AUGUST 2015</p> </div> <p data-bbox="774 1193 2405 1269"><i>Source: ENERGY EFFICIENT GRAPHICS AND MULTIMEDIA IN 28NM CARRIZO APU, HOT CHIPS 27 – AUGUST 2015, page 21.</i></p> </div>	Configuration	UVT (Blue)	UVD (Red)	UVT+UVD (Green)	"Kaveri UVD"	~2.0	~7.5	~9.5	"Carrizo" - Without Dynamic Power Gating	~1.0	~10.5	~11.5	"Carrizo" - Dynamic UVD Power Gating	~0.5	~2.0	~2.5
Configuration	UVT (Blue)	UVD (Red)	UVT+UVD (Green)															
"Kaveri UVD"	~2.0	~7.5	~9.5															
"Carrizo" - Without Dynamic Power Gating	~1.0	~10.5	~11.5															
"Carrizo" - Dynamic UVD Power Gating	~0.5	~2.0	~2.5															
1e	a plurality of input/output circuits disposed around said	The Accused Products disclose the limitation of a plurality of input/output circuits disposed around said unit cell array.																

	<u>Limitation</u>	<u>Contention</u>
	unit cell array.	<div data-bbox="774 263 2217 1075"> <p>6TH GENERATION AMD A-SERIES PROCESSOR: "CARRIZO" AMD</p> <p>DESIGN GOALS</p> <ul style="list-style-type: none"> ▲ Deliver superior performance, battery life and user experience for notebook and convertible form factors ▲ Deliver this energy efficiency gains in a mature, cost effective 28nm process node <p>AMD 6TH GENERATION A-SERIES PROCESSOR</p> <p>Die diagram labels: DDR/PHY, X86 Module, X86 Module, GPU, Northbridge, Southbridge, PCIe/Display</p> <p><small>2: ENERGY EFFICIENT GRAPHICS AND MULTIMEDIA IN 28NM "CARRIZO" APU HOT CHIPS 27 – AUGUST</small></p> </div> <p><i>Source: ENERGY EFFICIENT GRAPHICS AND MULTIMEDIA IN 28NM CARRIZO APU, page 2 HOT CHIPS 27 – AUGUST 2015.</i></p>
2	A semiconductor integrated circuit device according to claim 1, wherein said power	The Accused Products disclose that said power switch is turned off during standby and turned on when taken active.

<u>Limitation</u>	<u>Contention</u>
<p>switch is turned off during standby and turned on when taken active.</p>	 <p>The diagram, titled "RACE TO DRAM SELF REFRESH TRANSITION FROM ACTIVE TO LOWEST POWER STATE" with the AMD logo, illustrates the power state transition of an APU. It is divided into two main sections: "Active" and "Lowest power state - DRAM in self-refresh".</p> <p>Active State: Shows a system with various components in an active state. On the left, there are VIDEO (VPE, VCE, VCE) and AUDIO (ADP, SRAM, DAC, DAC) blocks. The DISPLAY block contains Display Pipe0, Display Pipe1, Display Pipe2, and Display Video. The CPU is active. The DRAM Controller is active, connected to DRAM. The Northbridge and Southbridge are also active. The Efficiency Arbitration block is active, connected to the CPU and DRAM Controller. The Graphics block is active, connected to the CPU and DRAM Controller. The VC-Matrix block is active, connected to the CPU and DRAM Controller. The DRAM Controller is active, connected to the DRAM. The DRAM is active.</p> <p>Lowest Power State - DRAM in self-refresh: Shows the system in a low-power state. The CPU is in a low-power state. The DRAM Controller is in a low-power state, and the DRAM is in self-refresh. The Northbridge and Southbridge are in a low-power state. The Efficiency Arbitration block is in a low-power state. The Graphics block is in a low-power state. The VC-Matrix block is in a low-power state. The DRAM Controller is in a low-power state, and the DRAM is in self-refresh. The DRAM is in self-refresh.</p> <p>Legend: Power Standby State (Black), Lowest Power State (Grey), DRAM Self Refresh (Blue).</p> <p>Source: ENERGY EFFICIENT GRAPHICS AND MULTIMEDIA IN 28NM CARRIZO APU, page 26 HOT CHIPS 27 - AUGUST 2015.</p>

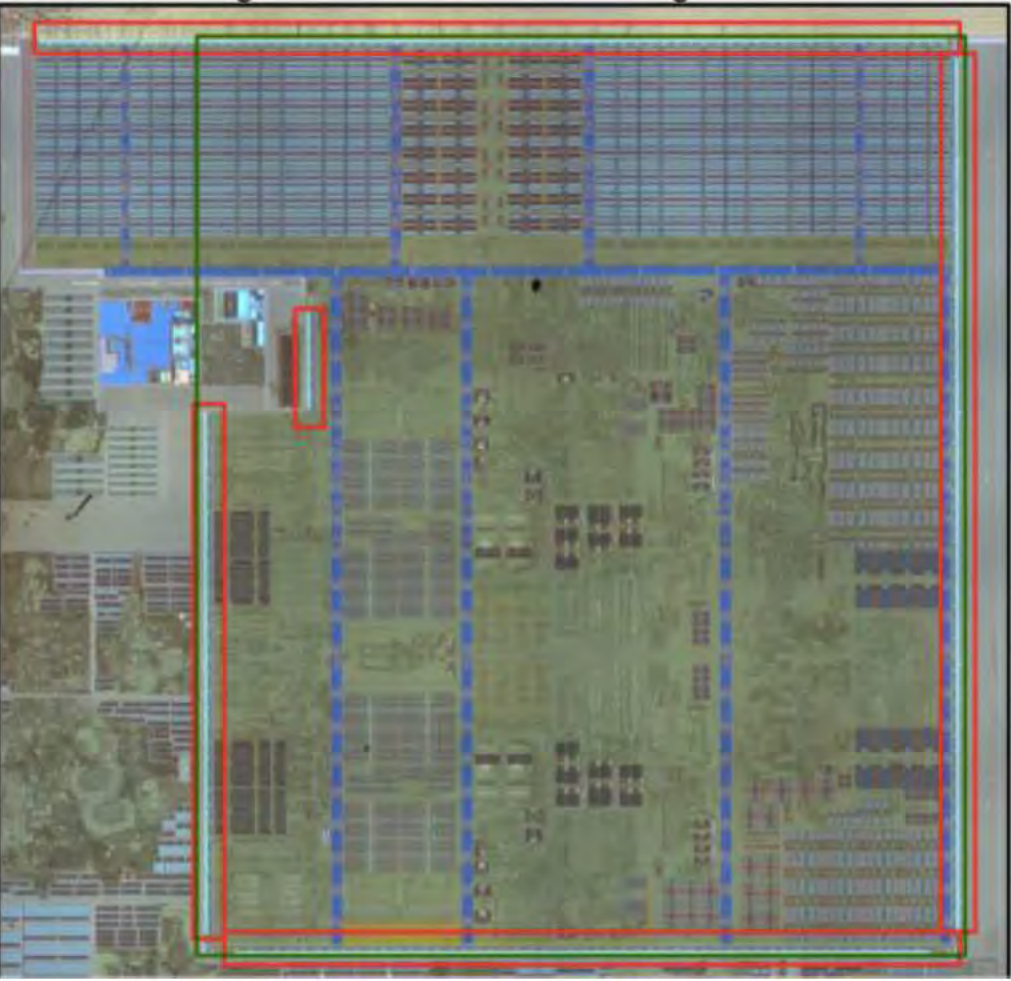
	<u>Limitation</u>	<u>Contention</u>
3	The semiconductor integrated circuit device according to claim 1, wherein parts of said power switch are disposed within said unit cell array.	 A micrograph of a semiconductor chip showing a unit cell array. The array is a large rectangular region with a grid of small, repeating units. A power switch is located within this array, highlighted by a red rectangle. The chip also shows other components like a central processing unit and various interconnects. The unit cell array is outlined in blue, and the power switch is outlined in red. There are also green and orange outlines on the chip.

Exhibit B.1: Preliminary Infringement Claim Chart for U.S. Patent 6,895,519

Accused Products: AMD Family 14h Products

These preliminary infringement contentions were prepared without the benefit of the Court's claim construction or the parties' exchange of constructions. As of the date of these contentions, AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court's constructions or to account for new information that becomes available.

	<u>Limitation</u>	<u>Contention</u>
1p	A system LSI having a plurality of ordinary operation modes and a plurality of special modes in response to clock frequencies supplied to a central processing unit, comprising:	To the extent that the preamble is limiting, Aquila contends that it is met. For example, each product in the 14h Accused Product Family ("Accused Product") is a system LSI. The Accused Product has a plurality of ordinary operation modes, for example the Core P-states. <i>See</i> BIOS and Kernel Developer's Guide for AMD Family 14h Models 00h-0Fh Processors ("BKDG"), §2.5.3.1:

	<u>Limitation</u>	<u>Contention</u>
		<p>2.5.3.1 Core P-states</p> <p>Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states, specified in MSRC001_00[6B:64]. Out of reset, the voltage and frequency of the cores is specified by MSRC001_0071[StartupPstate].</p> <p>Support for dynamic core P-state changes is indicated by more than one enabled selection in MSRC001_00[6B:64][PstateEn]. The DID and VID for each core P-state is specified in MSRC001_00[6B:64]. The COF for core P-states is a function of the main PLL frequency and the DID. See D18F3xD4[MainPllOp-FreqId] for more details on the main PLL frequency and MSRC001_00[6B:64][CpuDidLSD] for more details on the DID.</p> <p>Software requests core P-state changes for each core independently using the hardware P-state control mechanism (also known as “fire and forget”). Support for hardware P-state control is indicated by CUID Fn8000_0007_EDX[HwPstate]=1b. P-state transitions using the hardware P-state control mechanism are not allowed until the P-state initialization requirements defined in 2.5.3.1.7 [BIOS Requirements for Core P-State Initialization and Transitions] are complete.</p> <p>BKDG at p.55:</p>

<u>Limitation</u>	<u>Contention</u>																																								
	<p>Table 9: Software P-state numbering example</p> <table border="1"> <thead> <tr> <th colspan="2" style="text-align: left;">D18F4x15C[NumBoostStates]=1</th> <th colspan="2" style="text-align: left;">D18F4x15C[NumBoostStates]=3</th> </tr> <tr> <th>P-state Name</th> <th>MSR Address</th> <th>P-state Name</th> <th>MSR Address</th> </tr> </thead> <tbody> <tr> <td>Pb0</td> <td>MSRC001_0064</td> <td>Pb0</td> <td>MSRC001_0064</td> </tr> <tr> <td>P0</td> <td>MSRC001_0065</td> <td>Pb1</td> <td>MSRC001_0065</td> </tr> <tr> <td>P1</td> <td>MSRC001_0066</td> <td>Pb2</td> <td>MSRC001_0066</td> </tr> <tr> <td>P2</td> <td>MSRC001_0067</td> <td>P0</td> <td>MSRC001_0067</td> </tr> <tr> <td>P3</td> <td>MSRC001_0068</td> <td>P1</td> <td>MSRC001_0068</td> </tr> <tr> <td>P4</td> <td>MSRC001_0069</td> <td>P2</td> <td>MSRC001_0069</td> </tr> <tr> <td>P5</td> <td>MSRC001_006A</td> <td>P3</td> <td>MSRC001_006A</td> </tr> <tr> <td>P6</td> <td>MSRC001_006B</td> <td>P4</td> <td>MSRC001_006B</td> </tr> </tbody> </table> <p>All sections and register definitions use software P-state numbering unless otherwise specified.</p> <p>The Accused Product Family has a plurality of special modes, for example, the Core C-states or deep sleep modes such as ACPI S3 or connected standby S0i3. <i>See</i> BKDG, §§ 2.5.3.2, 2.5.3.2.1, 2.5:</p>	D18F4x15C[NumBoostStates]=1		D18F4x15C[NumBoostStates]=3		P-state Name	MSR Address	P-state Name	MSR Address	Pb0	MSRC001_0064	Pb0	MSRC001_0064	P0	MSRC001_0065	Pb1	MSRC001_0065	P1	MSRC001_0066	Pb2	MSRC001_0066	P2	MSRC001_0067	P0	MSRC001_0067	P3	MSRC001_0068	P1	MSRC001_0068	P4	MSRC001_0069	P2	MSRC001_0069	P5	MSRC001_006A	P3	MSRC001_006A	P6	MSRC001_006B	P4	MSRC001_006B
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P-state Name	MSR Address	P-state Name	MSR Address																																						
Pb0	MSRC001_0064	Pb0	MSRC001_0064																																						
P0	MSRC001_0065	Pb1	MSRC001_0065																																						
P1	MSRC001_0066	Pb2	MSRC001_0066																																						
P2	MSRC001_0067	P0	MSRC001_0067																																						
P3	MSRC001_0068	P1	MSRC001_0068																																						
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P6	MSRC001_006B	P4	MSRC001_006B																																						

	<u>Limitation</u>	<u>Contention</u>
		<p>2.5.3.2 C-states</p> <p>C-states are processor power states. C0 is the operational state in which instructions are executed. All other C-states are low-power states in which instructions are not executed.</p> <p>2.5.3.2.1 C-state Names and Numbers</p> <p>C-states are often referred to by an alphanumeric naming convention, C1, C2, C3, etc. The mapping between ACPI defined C-states and AMD specified C-state actions is not direct. The actions taken by the processor when entering a low-power C-state are specified by D18F4x118 and D18F4x11C and are configured by software. See 2.5.3.2.3 [C-state Actions] for information about AMD specific actions.</p>

<u>Limitation</u>	<u>Contention</u>																																																
	<p>2.5 Power Management</p> <p>The processor supports many power management features in a variety of systems. Table 8 provides a summary of ACPI states and power management features and indicates whether they are supported.</p> <p>Table 8: Power management support</p> <table border="1"> <thead> <tr> <th>ACPI State/Power Management Feature</th> <th>Supported</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>G0/S0/C0: Working</td> <td>Yes</td> <td></td> </tr> <tr> <td>G0/S0/C0: Core P-state transitions</td> <td>Yes</td> <td>2.5.3.1 [Core P-states]</td> </tr> <tr> <td>G0/S0/C0: NB P-state transitions</td> <td>Yes</td> <td>2.5.4.2 [NB Clock Ramping]</td> </tr> <tr> <td>G0/S0/C0: Hardware thermal control (HTC)</td> <td>Yes</td> <td>2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)]</td> </tr> <tr> <td>G0/S0/C0: Local Hardware thermal control (LHTC)</td> <td>Revision Specific¹</td> <td>2.10.3.2 [Local Hardware Thermal Control (LHTC)]</td> </tr> <tr> <td>G0/S0/C0: Software thermal control (STC)</td> <td>No</td> <td></td> </tr> <tr> <td>G0/S0/C0: Thermal clock throttling (SMC controlled)</td> <td>No</td> <td></td> </tr> <tr> <td>G0/S0: Low power C-states</td> <td>Yes</td> <td>2.5.3.2 [C-states] and 2.5.1.4.2 [Alternate Low Power Voltages]</td> </tr> <tr> <td>G1/S1: Stand By (Powered On Suspend)</td> <td>No</td> <td></td> </tr> <tr> <td>G1/S3: Stand By (Suspend to RAM)</td> <td>Yes</td> <td>2.5.7.1.1 [ACPI Suspend to RAM State (S3)]</td> </tr> <tr> <td>G1/S4, S5: Hibernate (Suspend to Disk), Shut Down (Soft Off)</td> <td>Yes</td> <td></td> </tr> <tr> <td>G3 Mechanical Off</td> <td>Yes</td> <td></td> </tr> <tr> <td>Parallel VID Interface</td> <td>No</td> <td rowspan="4">2.5.1 [Processor Power Planes And Voltage Control]</td> </tr> <tr> <td>Serial VID Interface</td> <td>Yes</td> </tr> <tr> <td>Dual-plane systems</td> <td>Yes</td> </tr> <tr> <td colspan="2">1. Support for this ACPI state or power management feature varies by processor revision. See 1.5.2 [Supported Feature Variations].</td> </tr> </tbody> </table>	ACPI State/Power Management Feature	Supported	Description	G0/S0/C0: Working	Yes		G0/S0/C0: Core P-state transitions	Yes	2.5.3.1 [Core P-states]	G0/S0/C0: NB P-state transitions	Yes	2.5.4.2 [NB Clock Ramping]	G0/S0/C0: Hardware thermal control (HTC)	Yes	2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)]	G0/S0/C0: Local Hardware thermal control (LHTC)	Revision Specific ¹	2.10.3.2 [Local Hardware Thermal Control (LHTC)]	G0/S0/C0: Software thermal control (STC)	No		G0/S0/C0: Thermal clock throttling (SMC controlled)	No		G0/S0: Low power C-states	Yes	2.5.3.2 [C-states] and 2.5.1.4.2 [Alternate Low Power Voltages]	G1/S1: Stand By (Powered On Suspend)	No		G1/S3: Stand By (Suspend to RAM)	Yes	2.5.7.1.1 [ACPI Suspend to RAM State (S3)]	G1/S4, S5: Hibernate (Suspend to Disk), Shut Down (Soft Off)	Yes		G3 Mechanical Off	Yes		Parallel VID Interface	No	2.5.1 [Processor Power Planes And Voltage Control]	Serial VID Interface	Yes	Dual-plane systems	Yes	1. Support for this ACPI state or power management feature varies by processor revision. See 1.5.2 [Supported Feature Variations].	
ACPI State/Power Management Feature	Supported	Description																																															
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G1/S1: Stand By (Powered On Suspend)	No																																																
G1/S3: Stand By (Suspend to RAM)	Yes	2.5.7.1.1 [ACPI Suspend to RAM State (S3)]																																															
G1/S4, S5: Hibernate (Suspend to Disk), Shut Down (Soft Off)	Yes																																																
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1. Support for this ACPI state or power management feature varies by processor revision. See 1.5.2 [Supported Feature Variations].																																																	

<u>Limitation</u>	<u>Contention</u>
	<p>Furthermore, the Core P-states and Core C-states are in response to clock frequencies supplied to a central processing unit. For example, the core P-states are “characterized” by “core frequency;” core P-state changes are further requested by software. <i>See e.g.</i>, BKDG, § 2.5.3.1, 2.5.3.1.3:</p> <p>2.5.3.1 Core P-states</p> <p>Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states, specified in MSRC001_00[6B:64]. Out of reset, the voltage and frequency of the cores is specified by MSRC001_0071[StartupPstate].</p> <p>Support for dynamic core P-state changes is indicated by more than one enabled selection in MSRC001_00[6B:64][PstateEn]. The DID and VID for each core P-state is specified in MSRC001_00[6B:64]. The COF for core P-states is a function of the main PLL frequency and the DID. See D18F3xD4[MainPllOp-FreqId] for more details on the main PLL frequency and MSRC001_00[6B:64][CpuDidLSD] for more details on the DID.</p> <p>Software requests core P-state changes for each core independently using the hardware P-state control mechanism (also known as “fire and forget”). Support for hardware P-state control is indicated by CPUID Fn8000_0007_EDX[HwPstate]=1b. P-state transitions using the hardware P-state control mechanism are not allowed until the P-state initialization requirements defined in 2.5.3.1.7 [BIOS Requirements for Core P-State Initialization and Transitions] are complete.</p> <p style="text-align: right;">Page #57</p>

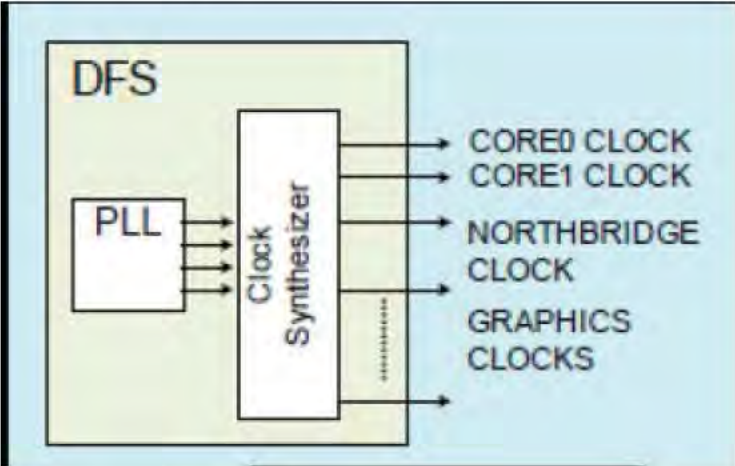
<u>Limitation</u>	<u>Contention</u>
	<p>2.5.3.1.3 Core P-state Control</p> <p>Core P-states are dynamically controlled by software and are exposed through ACPI objects (see 2.5.3.1.9 [ACPI Processor P-State Objects]). Software requests a core P-state change by writing a 3 bit index corresponding to the desired non-boosted P-state number to <code>MSRC001_0062</code> [P-State Control] of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's <code>MSRC001_0062[PstateCmd]</code>. Boosted P-states may not be directly requested by software. Whenever software requests the P0 state (i.e. when software writes 000b to <code>MSRC001_0062[PstateCmd]</code>) on a processor that supports CPB, hardware dynamically places that core into the highest-performance P-state possible as determined by CPB. See 2.5.3.1.1 [Core Performance Boost (CPB)].</p> <p>Hardware sequences the frequency and voltage changes necessary to complete a P-state transition as specified by 2.5.3.1.6 [Core P-state Transition Behavior] with no additional software interaction required. Hardware also coordinates frequency and voltage changes when differing P-state requests are made on cores that share a frequency or voltage plane. See 2.5.2 [Frequency and Voltage Domain Dependencies] for details about hardware coordination.</p> <p>Core P-states are changed without interacting with an external chipset. However, the chipset is notified of core P-state changes by the P-state special cycle if <code>MSRC001_001F[EnaPStateSpCyc]=1</code>. This message is sent regardless of whether the change is to or from a boosted P-state or a non-boosted P-state.</p> <p>Similarly, C-states are “dynamically requested by software” and also dependent upon clock frequency. See BKDG §§ 2.5.3.2.2, 2.5.3.2.3.1, 2.5.3.2.3.2; p.320-321:</p>

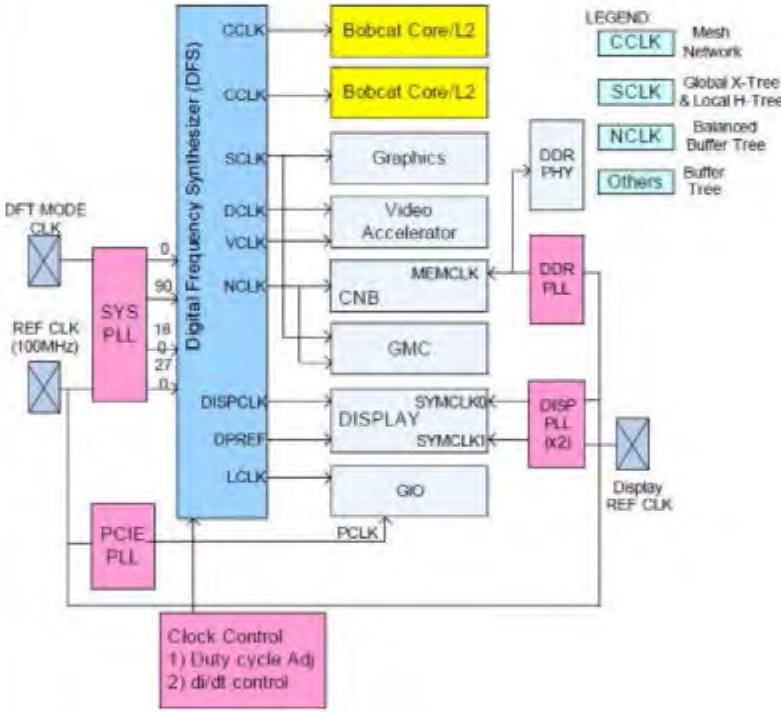
<u>Limitation</u>	<u>Contention</u>
	<p>2.5.3.2.3.1 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x1A8[Single-HaltCpuDid].</p> <p>2.5.3.2.3.2 Core C6 (CC6) State</p> <p>When a core enters the CC6 state, it executes the following sequence:</p> <ol style="list-style-type: none"> 1. L1 and L2 caches are flushed to DRAM by hardware. 2. Internal core state is saved to DRAM by hardware. 3. The core clock ramps down to the frequency specified by D18F4x1AC[C6Did]. 4. Power is removed from the core if possible as specified by D18F4x1AC[CoreC6Cap] and D18F4x1AC[CoreC6Dis]. <p>The events which cause a core to exit the CC6 state are specified in 2.5.3.2.6 [Exiting C-states].</p> <p>If a warm reset occurs while a core is in CC6, all MCA registers in the core shown in Table 41 are cleared to 0. See 2.16 [Machine Check Architecture].</p> <p><u>D18F4x1AC CPU State Power Management Dynamic Control 1</u></p>

	<u>Limitation</u>	<u>Contention</u>														
		<table border="1"> <tr> <td data-bbox="870 263 978 321">9:5</td> <td data-bbox="978 263 2327 360"> C6Did: CC6 divisor. Read-write. Reset: 0. BIOS: 1Fh. Specifies the divisor applied to the core when ramping clocks down for CC6. See 2.5.3.2.3 [C-state Actions] for details. </td> </tr> <tr> <td data-bbox="999 360 1123 393"><u>Bits</u></td> <td data-bbox="1193 360 1300 393"><u>Divisor</u></td> </tr> <tr> <td data-bbox="999 393 1123 425">1Ch-00h</td> <td data-bbox="1193 393 1327 425">Reserved.</td> </tr> <tr> <td data-bbox="999 425 1080 457">1Dh</td> <td data-bbox="1193 425 1247 457">128</td> </tr> <tr> <td data-bbox="999 457 1080 490">1Eh</td> <td data-bbox="1193 457 1247 490">512</td> </tr> <tr> <td data-bbox="999 490 1080 522">1Fh</td> <td data-bbox="1193 490 1354 522">Clocks off.</td> </tr> <tr> <td colspan="2" data-bbox="978 587 1489 620">See D18F4x1A8[SingleHaltCpuDid].</td> </tr> </table>	9:5	C6Did: CC6 divisor. Read-write. Reset: 0. BIOS: 1Fh. Specifies the divisor applied to the core when ramping clocks down for CC6. See 2.5.3.2.3 [C-state Actions] for details.	<u>Bits</u>	<u>Divisor</u>	1Ch-00h	Reserved.	1Dh	128	1Eh	512	1Fh	Clocks off.	See D18F4x1A8[SingleHaltCpuDid].	
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1Eh	512															
1Fh	Clocks off.															
See D18F4x1A8[SingleHaltCpuDid].																
1a	a first memory that stores a clock control library for controlling a clock frequency transition between said ordinary operation modes;	<p>The Accused Products include a first memory that stores a clock control library. For example, the SMU contains memory that stores the firmware and configuration space registers, including a clock control library. The clock control library controls clock frequency transition between the P-states. See e.g., BKDG, 30:</p> <div data-bbox="935 883 1413 1149" data-label="Diagram"> <pre> graph TD NB[Northbridge (NB)] NB --- TR[Transaction routing] NB --- CIR[Configuration and IO-space registers] NB --- RC[Root complex] NB --- GC[Graphics core (optional)] </pre> <p>The diagram shows a box labeled "Northbridge (NB)" containing a list of components: Transaction routing, Configuration and IO-space registers, Root complex, and Graphics core (optional). An arrow points down to the box, and another arrow points left to the right side of the box.</p> </div> <p>BKDG, section 2.12:</p>														

	<u>Limitation</u>	<u>Contention</u>																																																												
		<p>2.12 System Management Unit (SMU)</p> <p>The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details.</p> <p>2.12.1 Microcontroller</p> <p>The SMU contains a microcontroller with a 16k ROM and a 16k RAM.</p> <p>See also BKDG, Table 10:</p> <p>Table 10: P-state control example</p> <table border="1" data-bbox="873 722 2274 1274"> <thead> <tr> <th colspan="3">D18F4x15C[NumBoostStates]=1</th> <th colspan="3">D18F4x15C[NumBoostStates]=3</th> </tr> <tr> <th>P-state Name</th> <th>Index Used for Requests/Status</th> <th>Corresponding MSR Address</th> <th>P-state Name</th> <th>Index Used for Requests/Status</th> <th>Corresponding MSR Address</th> </tr> </thead> <tbody> <tr> <td>Pb0</td> <td>n/a</td> <td>MSRC001_0064</td> <td>Pb0</td> <td>n/a</td> <td>MSRC001_0064</td> </tr> <tr> <td>P0</td> <td>0</td> <td>MSRC001_0065</td> <td>Pb1</td> <td>n/a</td> <td>MSRC001_0065</td> </tr> <tr> <td>P1</td> <td>1</td> <td>MSRC001_0066</td> <td>Pb2</td> <td>n/a</td> <td>MSRC001_0066</td> </tr> <tr> <td>P2</td> <td>2</td> <td>MSRC001_0067</td> <td>P0</td> <td>0</td> <td>MSRC001_0067</td> </tr> <tr> <td>P3</td> <td>3</td> <td>MSRC001_0068</td> <td>P1</td> <td>1</td> <td>MSRC001_0068</td> </tr> <tr> <td>P4</td> <td>4</td> <td>MSRC001_0069</td> <td>P2</td> <td>2</td> <td>MSRC001_0069</td> </tr> <tr> <td>P5</td> <td>5</td> <td>MSRC001_006A</td> <td>P3</td> <td>3</td> <td>MSRC001_006A</td> </tr> <tr> <td>P6</td> <td>6</td> <td>MSRC001_006B</td> <td>P4</td> <td>4</td> <td>MSRC001_006B</td> </tr> </tbody> </table>	D18F4x15C[NumBoostStates]=1			D18F4x15C[NumBoostStates]=3			P-state Name	Index Used for Requests/Status	Corresponding MSR Address	P-state Name	Index Used for Requests/Status	Corresponding MSR Address	Pb0	n/a	MSRC001_0064	Pb0	n/a	MSRC001_0064	P0	0	MSRC001_0065	Pb1	n/a	MSRC001_0065	P1	1	MSRC001_0066	Pb2	n/a	MSRC001_0066	P2	2	MSRC001_0067	P0	0	MSRC001_0067	P3	3	MSRC001_0068	P1	1	MSRC001_0068	P4	4	MSRC001_0069	P2	2	MSRC001_0069	P5	5	MSRC001_006A	P3	3	MSRC001_006A	P6	6	MSRC001_006B	P4	4	MSRC001_006B
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P0	0	MSRC001_0065	Pb1	n/a	MSRC001_0065																																																									
P1	1	MSRC001_0066	Pb2	n/a	MSRC001_0066																																																									
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P6	6	MSRC001_006B	P4	4	MSRC001_006B																																																									
1b	a system control circuit which has a register, wherein said system control	The Accused Product has a system control circuit, for example, the System Management Unit and/or the System Management Controller, that has a register. See e.g., BKDG:																																																												

<u>Limitation</u>	<u>Contention</u>
<p>circuit carries out the clock frequency transition between said ordinary operation modes and said special modes in response to a change of a value in said register, and also carries out the clock frequency transition among said ordinary operation modes in response to said clock control library;</p>	<div data-bbox="935 293 1413 560" data-label="Diagram"> <pre> graph TD NB[Northbridge (NB)] NB --- TR[Transaction routing] NB --- CIO[Configuration and IO-space registers] NB --- RC[Root complex] NB --- GC[Graphics core (optional)] </pre> </div> <p>BKDG, section 2.12: 2.12 System Management Unit (SMU)</p> <p>The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details.</p> <p>2.12.1 Microcontroller</p> <p>The SMU contains a microcontroller with a 16k ROM and a 16k RAM.</p> <p>The NB/SMU controls the clock frequency transitions between the core P-states. See e.g., SATHE et al.: RESONANT-CLOCK DESIGN FOR A POWER-EFFICIENT, HIGH-VOLUME X86-64 MICROPROCESSOR, p.144</p> <p>tion of the configuration programming interface. On receiving notification from the NB of a PState transition, the core implements a PState entry sequence which transitions the core into a clock-gated state. A program sequencer then accesses a</p>

	<u>Limitation</u>	<u>Contention</u>
1c	<p>a clock generation circuit that receives a plurality of standard clocks, wherein said clock generation circuit generates a clock supplied to said central processing unit according to control by said system control circuit; and</p>	<p>The Accused Products include a digital frequency synthesizer clock generation circuit, including the core PLL, clock multipliers and dividers, and/or the digital frequency synthesizer. The DFS receives a plurality of standard clocks, for example, different phases of the PLL clock or reference clock, and outputs the core clock such as CCLK to the CPU.</p> <p>The clock generator circuit includes at least the PLL and the digital frequency synthesizer. The DFS receives a plurality of standard clocks (the 4 phases-offset references provided by the PLL), and generates CCLK according to control by the SMU:</p> 

	<u>Limitation</u>	<u>Contention</u>
		 <p>The diagram illustrates the clock generation architecture. A central 'Digital Frequency Synthesizer (DFS)' block is the core component. It receives two reference clocks: 'DFT MODE CLK' and 'REF CLK (100MHz)'. The DFS outputs several clock signals: GCLK to two 'Bobcat Core/L2' blocks; SCLK to 'Graphics'; DCLK to 'Video Accelerator'; VCLK to 'CNB'; NCLK to 'GMC'; DISPCLK to 'DISPLAY'; DPREF to 'DISPLAY'; and LCLK to 'GIO'. Additionally, it outputs PCLK to a 'PCIE PLL' and MEMCLK to 'DDR PHY'. The 'SYS PLL' provides a 90-degree phase shift to the DFS. The 'DISP PLL (x2)' provides a 27-degree phase shift to the DFS and also receives a 'Display REF CLK'. A 'Clock Control' block manages 'Duty cycle Adj' and 'di/dt control'. A legend defines clock types: CCLK (Mesh Network), SCLK (Global X-Tree & Local H-Tree), NCLK (Balanced Buffer Tree), and Others (Buffer Tree).</p> <p>Fig. 11 DFS clock generation Source: Foley et al., A Low-Power Integrated x86-64 And Graphics Processor For Mobile Computing Devices, Fig. 1., 11; p.224-225.</p>
1d	a second memory that stores an application program, wherein calling of said clock control library and	The Accused Products include a second memory, such as the hierarchy of L1, L2 caches that stores an application program, including but not limited to ACPI drivers, power management utilities, APIs provided by AMD, or any software that causes the SMU/SMC firmware to perform P-state transitions. See BKDG section 2.5.3.1.3; p. 429:

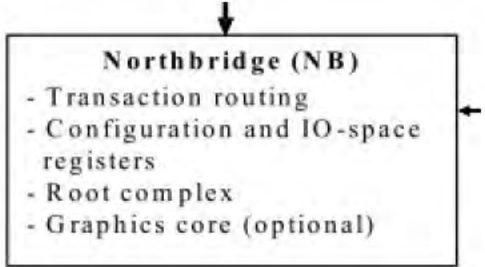
<u>Limitation</u>	<u>Contention</u>						
<p>changing of said register value are programmably controlled by said application program to enable user selectable clock frequency transitions,</p>	<p>2.5.3.1.3 Core P-state Control</p> <p>Core P-states are dynamically controlled by software and are exposed through ACPI objects (see 2.5.3.1.9 [ACPI Processor P-State Objects]). <u>Software requests a core P-state change by writing a 3 bit index corresponding to the desired non-boosted P-state number to MSRC001_0062 [P-State Control] of the appropriate core.</u> For example, to request P3 for core 0 software would write 011b to core 0's MSRC001_0062[PstateCmd]. Boosted P-states may not be directly requested by software. Whenever software requests the P0 state (i.e. when software writes 000b to MSRC001_0062[PstateCmd]) on a processor that supports CPB, hardware dynamically places that core into the highest-performance P-state possible as determined by CPB. See 2.5.3.1.1 [Core Performance Boost (CPB)].</p> <p>Hardware sequences the frequency and voltage changes necessary to complete a P-state transition as specified by 2.5.3.1.6 [Core P-state Transition Behavior] with no additional software interaction required. Hardware also coordinates frequency and voltage changes when differing P-state requests are made on cores that share a frequency or voltage plane. See 2.5.2 [Frequency and Voltage Domain Dependencies] for details about hardware coordination.</p> <p>MSRC001_0062 P-State Control</p> <hr/> <table border="1"> <thead> <tr> <th data-bbox="876 1036 975 1084">Bits</th> <th data-bbox="975 1036 2279 1084">Description</th> </tr> </thead> <tbody> <tr> <td data-bbox="876 1084 975 1133">63:3</td> <td data-bbox="975 1084 2279 1133">MBZ.</td> </tr> <tr> <td data-bbox="876 1133 975 1333">2:0</td> <td data-bbox="975 1133 2279 1333">PstateCmd: P-state change command. Read-write. Reset: Product-specific. <u>Writes to this field cause the core to change to the indicated non-boosted P-state number,</u> specified by MSRC001_00[6B:64]. 0=SWP0, 1=SWP1, etc. P-state limits are applied to any P-state requests made through this register. See sections 2.5.3.1 [Core P-states] and 2.5.3.1.2.1 [Software P-state Numbering]. Reads from this field return the last written value, regardless of whether any limits are applied.</td> </tr> </tbody> </table>	Bits	Description	63:3	MBZ.	2:0	PstateCmd: P-state change command. Read-write. Reset: Product-specific. <u>Writes to this field cause the core to change to the indicated non-boosted P-state number,</u> specified by MSRC001_00[6B:64]. 0=SWP0, 1=SWP1, etc. P-state limits are applied to any P-state requests made through this register. See sections 2.5.3.1 [Core P-states] and 2.5.3.1.2.1 [Software P-state Numbering]. Reads from this field return the last written value, regardless of whether any limits are applied.
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	<u>Limitation</u>	<u>Contention</u>																
1e	<p>wherein said special modes comprise a first special mode in which clock supply to principal constituents of said central processing unit is halted, a second special mode in which clock supply to an entirety of said central processing unit is halted, and a third special mode in which supply of power to the entirety of said central processing unit is halted.</p>	<p>The Accused Products include a first special mode in which clock supply to principal constituents of said central processing unit is halted, for example the core C1 (CC1) state:</p> <p>2.5.3.2.3.1 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x1A8[SingleHaltCpuDid].</p> <hr/> <p>D18F4x1A8 CPU State Power Management Dynamic Control 0</p> <p>Reset: 0000_0000h.</p> <table border="1" data-bbox="870 643 2322 1162"> <tr> <td data-bbox="870 643 978 688">4:0</td> <td data-bbox="978 643 2322 688"> SingleHaltCpuDid. Read-write. BIOS: 1Eh. On a processor with multiple cores, this specifies the divisor used when ramping core clocks down after a single core has entered the clocks ramped state. </td> </tr> <tr> <td data-bbox="870 688 978 727"></td> <td data-bbox="978 688 2322 727"> <table border="1"> <thead> <tr> <th data-bbox="978 688 1166 727"><u>Bits</u></th> <th data-bbox="1166 688 2322 727"><u>Divisor</u></th> </tr> </thead> <tbody> <tr> <td data-bbox="978 727 1166 766">1Ch-00h</td> <td data-bbox="1166 727 2322 766">Reserved.</td> </tr> <tr> <td data-bbox="978 766 1166 805">1Dh</td> <td data-bbox="1166 766 2322 805">128</td> </tr> <tr> <td data-bbox="978 805 1166 844">1Eh</td> <td data-bbox="1166 805 2322 844">512</td> </tr> <tr> <td data-bbox="978 844 1166 883"><u>1Fh</u></td> <td data-bbox="1166 844 2322 883"><u>Clocks off.</u></td> </tr> </tbody> </table> </td> </tr> <tr> <td data-bbox="870 883 978 922"></td> <td data-bbox="978 883 2322 922"> <ul style="list-style-type: none"> • If MSRC001_00[6B:64][CpuDidMSD] of the current P-state is greater than or equal to SingleHaltCpuDid, then no frequency change is made when entering the low-power state associated with this register. • The COF = (the frequency specified by D18F3xD4[MainPllOpFreqId]) / (the divisor specified by this field). </td> </tr> </table> <p>The Accused Products include a second special mode in which clock supply to an entirety of said central processing unit is halted, for example the package C1 (PC1) state:</p>	4:0	SingleHaltCpuDid. Read-write. BIOS: 1Eh. On a processor with multiple cores, this specifies the divisor used when ramping core clocks down after a single core has entered the clocks ramped state.		<table border="1"> <thead> <tr> <th data-bbox="978 688 1166 727"><u>Bits</u></th> <th data-bbox="1166 688 2322 727"><u>Divisor</u></th> </tr> </thead> <tbody> <tr> <td data-bbox="978 727 1166 766">1Ch-00h</td> <td data-bbox="1166 727 2322 766">Reserved.</td> </tr> <tr> <td data-bbox="978 766 1166 805">1Dh</td> <td data-bbox="1166 766 2322 805">128</td> </tr> <tr> <td data-bbox="978 805 1166 844">1Eh</td> <td data-bbox="1166 805 2322 844">512</td> </tr> <tr> <td data-bbox="978 844 1166 883"><u>1Fh</u></td> <td data-bbox="1166 844 2322 883"><u>Clocks off.</u></td> </tr> </tbody> </table>	<u>Bits</u>	<u>Divisor</u>	1Ch-00h	Reserved.	1Dh	128	1Eh	512	<u>1Fh</u>	<u>Clocks off.</u>		<ul style="list-style-type: none"> • If MSRC001_00[6B:64][CpuDidMSD] of the current P-state is greater than or equal to SingleHaltCpuDid, then no frequency change is made when entering the low-power state associated with this register. • The COF = (the frequency specified by D18F3xD4[MainPllOpFreqId]) / (the divisor specified by this field).
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	<p>2.5.3.2.3.3 Package C1 (PC1) State</p> <p>The processor enters the PC1 state with auto-Pmin when all of the following are true:</p> <ul style="list-style-type: none"> All cores are in the CC1 state or deeper. <p>If D18F4x1AC[CstPminEn] indicates that auto-Pmin is enabled when the processor enters PC1, the P-state for all cores is transitioned as specified by 2.5.3.2.7.1 [Auto-Pmin]. Regardless of the state of D18F4x1AC[CstPminEn], all core clocks are ramped to the frequency specified by D18F4x1A8[AllHaltCpuDid].</p> <p>D18F4x1A8 CPU State Power Management Dynamic Control 0</p> <hr/> <p>Reset: 0000_0000h.</p> <table border="1" data-bbox="870 784 2327 1161"> <tr> <td data-bbox="870 784 978 836">9:5</td> <td colspan="2" data-bbox="978 784 2327 836">AllHaltCpuDid. Read-write. BIOS: 1Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State].</td> </tr> <tr> <td data-bbox="870 836 978 873"></td> <td data-bbox="978 836 1177 873"><u>Bits</u></td> <td data-bbox="1177 836 2327 873"><u>Divisor</u></td> </tr> <tr> <td data-bbox="870 873 978 911"></td> <td data-bbox="978 873 1177 911">1Ch-00h</td> <td data-bbox="1177 873 2327 911">Reserved.</td> </tr> <tr> <td data-bbox="870 911 978 948"></td> <td data-bbox="978 911 1177 948">1Dh</td> <td data-bbox="1177 911 2327 948">128</td> </tr> <tr> <td data-bbox="870 948 978 985"></td> <td data-bbox="978 948 1177 985">1Eh</td> <td data-bbox="1177 948 2327 985">512</td> </tr> <tr> <td data-bbox="870 985 978 1023"></td> <td data-bbox="978 985 1177 1023"><u>1Fh</u></td> <td data-bbox="1177 985 2327 1023"><u>Clocks off.</u></td> </tr> <tr> <td data-bbox="870 1023 978 1161"></td> <td colspan="2" data-bbox="978 1023 2327 1161">See D18F4x1A8[SingleHaltCpuDid].</td> </tr> </table> <p>The Accused Products include a third special mode in which supply of power to the entirety of said central processing unit is halted, for example the package C6 (PC6) state:</p>	9:5	AllHaltCpuDid . Read-write. BIOS: 1Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State].			<u>Bits</u>	<u>Divisor</u>		1Ch-00h	Reserved.		1Dh	128		1Eh	512		<u>1Fh</u>	<u>Clocks off.</u>		See D18F4x1A8[SingleHaltCpuDid].	
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<u>Limitation</u>	<u>Contention</u>
	<p>2.5.3.2.3.4 Package C6 (PC6) State</p> <p>The processor enters the PC6 state when all of the following are true:</p> <ul style="list-style-type: none"> • All cores enter the CC6 state. • The C-state action field targeted by each core’s C-state request has the C6Enable bit programmed to indicate entry into PC6 is allowed. See D18F4x118 and D18F4x11C. • PC6 is supported and enabled as specified by D18F4x1AC[PkgC6Cap] and D18F4x1AC[PkgC6Dis]. <p>When the package enters PC6, VDDCR_CPU is transitioned to the VID specified by D18F3x128[C6Vid].</p> <p>2.5.1.4.2 Alternate Low Power Voltages</p> <p>In order to save power, voltages lower than those normally used may be applied to the VDDCR_CPU power plane while the processor is in a C-state.</p> <p>D18F3x128[C6Vid] specifies a VDDCR_CPU voltage that does not retain the CPU caches or the cores’ microarchitectural state, nor allows for execution. As a result, hardware flushes caches and saves the cores’ microarchitectural state to DRAM before transitioning to C6Vid. See 2.5.3.2.3.4 [Package C6 (PC6) State].</p> <p>2.5.1.4.3 Power Gating</p> <p>The processor can remove power from an individual core. This is referred to as power gating. Gating power to a subcomponent causes its internal microarchitectural state and, if applicable, any data in its caches to be lost. When entering a power gated state, hardware saves any needed data, either internally or to DRAM, and flushes caches. When exiting a power gated state, hardware performs any required resets and restores any needed data. See 2.5.3.2.3.2 [Core C6 (CC6) State].</p>

	<u>Limitation</u>	<u>Contention</u>
2p	A system LSI as claimed in claim 1, wherein said clock control library comprises:	
2a	a plurality of libraries that control said system control circuit and said clock generation circuit to transition the clock frequencies supplied to said central processing unit; and	The clock control libraries of the Accused Products contain a plurality of libraries that control the SMU and clock generator to transition clock frequencies. For example, source code provided by AMD to coreboot indicates that P-state and C-state transitions are controlled by separate libraries: https://github.com/coreboot/coreboot/tree/master/src/vendorcode/amd/agesa/f14/Proc/CPU/Feature
2b	a main library which is called by said application program and selects any one of said libraries in correspondence with the clock frequency supplied to said central processing unit.	As discussed above, P-states and C-states may be controlled by software, which includes a main library that calls upon the plurality of libraries.
3p	A system LSI as claimed in claim 2,	
3a	wherein said main library is described using a same program language as said application program.	The main library in the SMU firmware and the application program instructions stored in the caches are both use the same language such as machine code.
5p	A system LSI as claimed in claim 2,	
5a	wherein each of said libraries is described using a program language capable of directly controlling said clock	The SMU firmware directly controls the SMU hardware.

	<u>Limitation</u>	<u>Contention</u>
	generation circuit and said system control circuit.	
6p	A system LSI as claimed in claim 5,	
6a	wherein each of said libraries is described using an assembler language.	The SMU firmware directly controls the SMU hardware and is described using an assembler language such as machine code.
7p	7. A system LSI as claimed in claim 1, wherein said system control circuit comprises:	
7a	a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit;	<p>The NB of the Accused Products contains a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit. The NB contains the configuration register space for the Accused Products.</p> <p>See e.g., BKDG:</p> <div style="text-align: center;">  <pre> graph TD A[] --> NB[Northbridge (NB)] subgraph NB [Northbridge (NB)] B[- Transaction routing] C[- Configuration and IO-space registers] D[- Root complex] E[- Graphics core (optional)] end F[] --> C </pre> <p>The diagram shows a box labeled "Northbridge (NB)" containing a list of components: Transaction routing, Configuration and IO-space registers, Root complex, and Graphics core (optional). An arrow points down to the box from above, and another arrow points left to the "Configuration and IO-space registers" item from the right.</p> </div> <p>BKDG, section 2.12:</p>

<u>Limitation</u>	<u>Contention</u>
	<p>2.12 System Management Unit (SMU)</p> <p>The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details.</p> <p>2.12.1 Microcontroller</p> <p>The SMU contains a microcontroller with a 16k ROM and a 16k RAM.</p> <p>Configuration space register mnemonics are defined in section 3.1 of the BKDG:</p> <ul style="list-style-type: none"> • DXFYxZZZ: PCI-defined configuration space; X specifies the hexadecimal device number (this may be 1 or 2 digits), Y specifies the function number, and ZZZ specifies the hexadecimal byte address (this may be 2 or 3 digits; e.g., D18F3x40 specifies the register at device 18h, function 3, and address 40h). See 2.7 [Configuration Space], for details about configuration space. <p>the core C1 (CC1) state:</p> <p>2.5.3.2.3.1 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x1A8[Single-HaltCpuDid].</p> <hr/> <p>D18F4x1A8 CPU State Power Management Dynamic Control 0</p> <hr/> <p>Reset: 0000_0000h.</p>

<u>Limitation</u>	<u>Contention</u>										
	<p data-bbox="897 277 2300 350">4:0 SingleHaltCpuDid. Read-write. BIOS: 1Eh. On a processor with multiple cores, this specifies the divisor used when ramping core clocks down after a single core has entered the clocks ramped state.</p> <table border="1" data-bbox="983 350 1354 545"> <thead> <tr> <th>Bits</th> <th>Divisor</th> </tr> </thead> <tbody> <tr> <td>1Ch-00h</td> <td>Reserved.</td> </tr> <tr> <td>1Dh</td> <td>128</td> </tr> <tr> <td>1Eh</td> <td>512</td> </tr> <tr> <td>1Fh</td> <td>Clocks off.</td> </tr> </tbody> </table> <ul data-bbox="983 586 2300 773" style="list-style-type: none"> • If MSRC001_00[6B:64][CpuDidMSD] of the current P-state is greater than or equal to SingleHaltCpuDid, then no frequency change is made when entering the low-power state associated with this register. • The COF = (the frequency specified by D18F3xD4[MainPllOpFreqId]) / (the divisor specified by this field). <p data-bbox="870 846 1427 878">2.5.3.2.3.3 Package C1 (PC1) State</p> <p data-bbox="870 919 1999 951">The processor enters the PC1 state with auto-Pmin when all of the following are true:</p> <ul data-bbox="924 992 1481 1024" style="list-style-type: none"> • All cores are in the CC1 state or deeper. <p data-bbox="870 1065 2327 1179">If D18F4x1AC[CstPminEn] indicates that auto-Pmin is enabled when the processor enters PC1, the P-state for all cores is transitioned as specified by 2.5.3.2.7.1 [Auto-Pmin]. Regardless of the state of D18F4x1AC[CstPminEn], all core clocks are ramped to the frequency specified by D18F4x1A8[AllHaltCpuDid].</p> <p data-bbox="870 1243 1771 1276">D18F4x1A8 CPU State Power Management Dynamic Control 0</p> <hr data-bbox="870 1284 2327 1292"/> <p data-bbox="870 1292 1139 1325">Reset: 0000_0000h.</p>	Bits	Divisor	1Ch-00h	Reserved.	1Dh	128	1Eh	512	1Fh	Clocks off.
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		<p>9:5 AllHaltCpuDid. Read-write. BIOS: 1Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State].</p> <table border="1" data-bbox="997 354 1365 516"> <thead> <tr> <th>Bits</th> <th>Divisor</th> </tr> </thead> <tbody> <tr> <td>1Ch-00h</td> <td>Reserved.</td> </tr> <tr> <td>1Dh</td> <td>128</td> </tr> <tr> <td>1Eh</td> <td>512</td> </tr> <tr> <td>1Fh</td> <td>Clocks off.</td> </tr> </tbody> </table> <p>See D18F4x1A8[SingleHaltCpuDid].</p>	Bits	Divisor	1Ch-00h	Reserved.	1Dh	128	1Eh	512	1Fh	Clocks off.
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7b	a clock halting register that receives the clock from said clock generation circuit and individually sets the clock to be halted or supplied;	<p>the core C1 (CC1) state:</p> <p>2.5.3.2.3.1 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x1A8[SingleHaltCpuDid].</p> <hr/> <p>D18F4x1A8 CPU State Power Management Dynamic Control 0</p> <hr/> <p>Reset: 0000_0000h.</p>										

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	See D18F4x1A8[SingleHaltCpuDid].																	

	<u>Limitation</u>	<u>Contention</u>		
7c	<p>And a status register that judges a state of said central processing unit immediately after being released from said third special mode.</p>	<p>2.5.3.2.7.2 Exiting PC6</p> <p>If the PService timer is enabled when the processor exits PC6, all cores transition to the P-state specified by D18F4x1AC[PstateIdCoreOffExit]. The cores remain in this state until one of the following occurs:</p> <ul style="list-style-type: none"> • The PService timer expires while the package is in C0: In this case, the cores transition back to the last P-state requested by software. • The package enters PC1 without auto-Pmin: In this case, the PService timer continues counting. If it expires while in PC1, the cores remain in the P-state specified by D18F4x1AC[PstateIdCoreOffExit] until they return to C0, at which time they transition to the last P-state requested by software. • The package enters PC1 with auto-Pmin: In this case, the PService timer stops counting and the cores enter the PService state. • The package enters PC6: In this case the PService timer stops counting and the actions associated the requested package C-state occur. See 2.5.3.2.3.4 [Package C6 (PC6) State]. <p>If the PService timer is disabled when the processor exits PC6, the cores transition back to the last P-state requested by software.</p> <p>See also BKDG pp.320-321:</p> <p><u>D18F4x1AC CPU State Power Management Dynamic Control 1</u></p> <table border="1" data-bbox="870 1052 2327 1351"> <tr> <td data-bbox="870 1052 978 1351">18:16</td> <td data-bbox="978 1052 2327 1351"> <p>PstateIdCoreOffExit. Read-write. Reset: 0. BIOS: See 2.5.3.2.9. When exiting the package C6 state, the core transitions to the P-state specified by this register. See 2.5.3.2.7.2 [Exiting PC6]. If PC6 is enabled (see 2.5.3.2.9 [BIOS Requirements for C-state Initialization]), PstateIdCoreOffExit must be programmed to the lowest-performance P-state displayed to the operating system or to any lower-performance P-state. This P-state must have a core clock frequency of at least 400 MHz. Programming this field to 0 causes the core to transition to the last P-state requested by software when exiting package C6. This field uses hardware P-state numbering. See 2.5.3.1.2.2 [Hardware P-state Numbering].</p> </td> </tr> </table>	18:16	<p>PstateIdCoreOffExit. Read-write. Reset: 0. BIOS: See 2.5.3.2.9. When exiting the package C6 state, the core transitions to the P-state specified by this register. See 2.5.3.2.7.2 [Exiting PC6]. If PC6 is enabled (see 2.5.3.2.9 [BIOS Requirements for C-state Initialization]), PstateIdCoreOffExit must be programmed to the lowest-performance P-state displayed to the operating system or to any lower-performance P-state. This P-state must have a core clock frequency of at least 400 MHz. Programming this field to 0 causes the core to transition to the last P-state requested by software when exiting package C6. This field uses hardware P-state numbering. See 2.5.3.1.2.2 [Hardware P-state Numbering].</p>
18:16	<p>PstateIdCoreOffExit. Read-write. Reset: 0. BIOS: See 2.5.3.2.9. When exiting the package C6 state, the core transitions to the P-state specified by this register. See 2.5.3.2.7.2 [Exiting PC6]. If PC6 is enabled (see 2.5.3.2.9 [BIOS Requirements for C-state Initialization]), PstateIdCoreOffExit must be programmed to the lowest-performance P-state displayed to the operating system or to any lower-performance P-state. This P-state must have a core clock frequency of at least 400 MHz. Programming this field to 0 causes the core to transition to the last P-state requested by software when exiting package C6. This field uses hardware P-state numbering. See 2.5.3.1.2.2 [Hardware P-state Numbering].</p>			

	<u>Limitation</u>	<u>Contention</u>
10p	A system LSI as claimed in claim 1,	
10a	wherein said first memory and said second memory are two independent memories which are separated from each other.	As detailed above, the first memory in the SMU and the second memory in the caches are independent memories that are separated from each other.

Exhibit B.2: Preliminary Infringement Claim Charts for U.S. Patent 6,895,519

Accused Products: AMD 15h Products

These preliminary infringement contentions were prepared without the benefit of the Court’s claim construction or the parties’ exchange of constructions. As of the date of these contentions, AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court’s constructions or to account for new information that becomes available.

	<u>Limitation</u>	<u>Contention</u>
1p	A system LSI having a plurality of ordinary operation modes and a plurality of special modes in response to clock frequencies supplied to a central processing unit, comprising:	<p>To the extent that the preamble is limiting, Aquila contends that it is met.</p> <p>For example, the 15h Accused Product is a system LSI.</p> <p>The Accused Product has a plurality of ordinary operation modes, for example the Core P-states. <i>See</i> BIOS and Kernel Developer’s Guide for AMD Family 15h Models 60h-6Fh Processors (“BKDG”), §2.5.2.1:</p> <p>2.5.2.1 Core P-states</p> <p>Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states (P0 through P7), specified in MSRC001_00[6B:64]. Out of cold reset, the voltage and frequency of the compute units is specified by MSRC001_0071[StartupPstate].</p> <p>Support for dynamic core P-state changes is indicated by more than one enabled selection in MSRC001_00[6B:64][PstateEn]. Software requests core P-state changes for each core independently. Support for hardware P-state control is indicated by CPUID Fn8000_0007_EDX[HwPstate]=1b. Software may not request any P-state transitions until the P-state initialization requirements defined in 2.5.2.1.5 [BIOS Requirements for Core P-state Initialization and Transitions] are complete.</p> <p>The processor supports independently-controllable frequency planes for each compute unit and independently-controllable voltage plane for all compute units.</p> <p>See also BKDG at p.691:</p>

<u>Limitation</u>	<u>Contention</u>																		
	<p>MSRC001_00[6B:64] P-state [7:0]</p> <hr/> <p>Per-node. Cold reset: Varies by product. Each of these registers specify the frequency and voltage associated with each of the core P-states.</p> <p>Table 270: Register Mapping for MSRC001_00[6B:64]</p> <table border="1" data-bbox="857 461 1723 854"> <thead> <tr> <th>Register</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>MSRC001_0064</td> <td>P-state 0</td> </tr> <tr> <td>MSRC001_0065</td> <td>P-state 1</td> </tr> <tr> <td>MSRC001_0066</td> <td>P-state 2</td> </tr> <tr> <td>MSRC001_0067</td> <td>P-state 3</td> </tr> <tr> <td>MSRC001_0068</td> <td>P-state 4</td> </tr> <tr> <td>MSRC001_0069</td> <td>P-state 5</td> </tr> <tr> <td>MSRC001_006A</td> <td>P-state 6</td> </tr> <tr> <td>MSRC001_006B</td> <td>P-state 7</td> </tr> </tbody> </table> <p>The CpuVid field in these registers is required to be programmed to the same value in all cores of a processor, but are allowed to be different between processors in a multi-processor system. All other fields in these registers are required to be programmed to the same value in each core of the coherent fabric. See 2.5.2 [CPU Core Power Management].</p> <p>BKDG at p.61:</p>	Register	Function	MSRC001_0064	P-state 0	MSRC001_0065	P-state 1	MSRC001_0066	P-state 2	MSRC001_0067	P-state 3	MSRC001_0068	P-state 4	MSRC001_0069	P-state 5	MSRC001_006A	P-state 6	MSRC001_006B	P-state 7
Register	Function																		
MSRC001_0064	P-state 0																		
MSRC001_0065	P-state 1																		
MSRC001_0066	P-state 2																		
MSRC001_0067	P-state 3																		
MSRC001_0068	P-state 4																		
MSRC001_0069	P-state 5																		
MSRC001_006A	P-state 6																		
MSRC001_006B	P-state 7																		

<u>Limitation</u>	<u>Contention</u>																																								
	<p>Table 10: Software P-state Naming</p> <table border="1"> <thead> <tr> <th colspan="2" style="text-align: left;">D18F4x15C[NumBoostStates]=1</th> <th colspan="2" style="text-align: left;">D18F4x15C[NumBoostStates]=3</th> </tr> <tr> <th style="text-align: left;">P-state Name</th> <th style="text-align: left;">Corresponding Register Address</th> <th style="text-align: left;">P-state Name</th> <th style="text-align: left;">Corresponding Register Address</th> </tr> </thead> <tbody> <tr> <td>Pb0</td> <td>MSRC001_0064</td> <td>Pb0</td> <td>MSRC001_0064</td> </tr> <tr> <td>P0 (base)</td> <td>MSRC001_0065</td> <td>Pb1</td> <td>MSRC001_0065</td> </tr> <tr> <td>P1</td> <td>MSRC001_0066</td> <td>Pb2</td> <td>MSRC001_0066</td> </tr> <tr> <td>P2</td> <td>MSRC001_0067</td> <td>P0 (base)</td> <td>MSRC001_0067</td> </tr> <tr> <td>P3</td> <td>MSRC001_0068</td> <td>P1</td> <td>MSRC001_0068</td> </tr> <tr> <td>P4</td> <td>MSRC001_0069</td> <td>P2</td> <td>MSRC001_0069</td> </tr> <tr> <td>P5</td> <td>MSRC001_006A</td> <td>P3</td> <td>MSRC001_006A</td> </tr> <tr> <td>P6</td> <td>MSRC001_006B</td> <td>P4</td> <td>MSRC001_006B</td> </tr> </tbody> </table> <p>All sections and register definitions use software P-state numbering unless otherwise specified.</p> <p>The Carrizo has a plurality of special modes, for example, the Core C-states or deep sleep modes such as ACPI S3 or connected standby S0i3. See BKDG, §§ 2.5.2.2, 2.5.2.2.1, 2.5:</p> <p>2.5.2.2 Core C-states</p> <p>C-states are processor power states. C0 is the operational state in which instructions are executed. All other C-states are low-power states in which instructions are not executed. When coming out of warm and cold reset, the cores are transitioned to the C0 state.</p>	D18F4x15C[NumBoostStates]=1		D18F4x15C[NumBoostStates]=3		P-state Name	Corresponding Register Address	P-state Name	Corresponding Register Address	Pb0	MSRC001_0064	Pb0	MSRC001_0064	P0 (base)	MSRC001_0065	Pb1	MSRC001_0065	P1	MSRC001_0066	Pb2	MSRC001_0066	P2	MSRC001_0067	P0 (base)	MSRC001_0067	P3	MSRC001_0068	P1	MSRC001_0068	P4	MSRC001_0069	P2	MSRC001_0069	P5	MSRC001_006A	P3	MSRC001_006A	P6	MSRC001_006B	P4	MSRC001_006B
D18F4x15C[NumBoostStates]=1		D18F4x15C[NumBoostStates]=3																																							
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P0 (base)	MSRC001_0065	Pb1	MSRC001_0065																																						
P1	MSRC001_0066	Pb2	MSRC001_0066																																						
P2	MSRC001_0067	P0 (base)	MSRC001_0067																																						
P3	MSRC001_0068	P1	MSRC001_0068																																						
P4	MSRC001_0069	P2	MSRC001_0069																																						
P5	MSRC001_006A	P3	MSRC001_006A																																						
P6	MSRC001_006B	P4	MSRC001_006B																																						

	<u>Limitation</u>	<u>Contention</u>
		<p>2.5.2.2.1 C-state Names and Numbers</p> <p>C-states are often referred to by an alphanumeric naming convention, C1, C2, C3, etc. The mapping between ACPI defined C-states and AMD specified C-states is not direct. AMD specified C-states are referred to as IO-based C-states. Up to three IO-based C-states are supported, IO-based C-state 0, 1, and 2. The IO-based C-state index corresponds to the offset added to <code>MSRC001_0073[CstateAddr]</code> to initiate a C-state request. See 2.5.2.2.2 [C-state Request Interface]. The actions taken by the processor when entering a low-power C-state are configured by software. See 2.5.2.2.3 [C-state Actions] for information about AMD specific actions.</p> <p>2.5 Power Management</p> <p>The processor supports a wide variety of power management features, including:</p> <ul style="list-style-type: none"> • OS-directed power management such as ACPI. • Clock frequency and voltage states (referred to as P-states and DPM states), including: <ul style="list-style-type: none"> • CPU core P-states. • Northbridge P-states. • Memory P-states. • Graphics DPM states. • Multi-media block DPM states. • Power and thermal management for performance. <ul style="list-style-type: none"> • Power optimization between blocks for optimal performance. • Voltage transient tolerance. • Power efficiency for battery life, including: <ul style="list-style-type: none"> • Power gating. • Voltage optimization. • Deep sleep modes (e.g., ACPI S3, or connected standby S0i3). • Limiting frequency when it provides little value. • BIOS-configurable specifications. <p>Furthermore, the Core P-states and Core C-states are in response to clock frequencies supplied to a central processing unit. For example, the core P-states are “characterized” by “core frequency;” core P-state changes are further requested by software. See <i>e.g.</i>, BKDG, § 2.5.2.1, 2.5.2.1.2:</p>

	<u>Limitation</u>	<u>Contention</u>
		<p>2.5.2.1 Core P-states</p> <p>Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states (P0 through P7), specified in MSRC001_00[6B:64]. Out of cold reset, the voltage and frequency of the compute units is specified by MSRC001_0071[StartupPstate].</p> <p>Support for dynamic core P-state changes is indicated by more than one enabled selection in MSRC001_00[6B:64][PstateEn]. Software requests core P-state changes for each core independently. Support for hardware P-state control is indicated by CPUID Fn8000_0007_EDX[HwPstate]=1b. Software may not request any P-state transitions until the P-state initialization requirements defined in 2.5.2.1.5 [BIOS Requirements for Core P-state Initialization and Transitions] are complete.</p> <p>The processor supports independently-controllable frequency planes for each compute unit and independently-controllable voltage plane for all compute units.</p> <p>2.5.2.1.2 Core P-state Control</p> <p>Core P-states are dynamically controlled by software and are exposed through ACPI objects (refer to 2.5.2.1.7.3 [ACPI Processor P-state Objects]). Software requests a core P-state change by writing a 3 bit index corresponding to the desired P-state number to MSRC001_0062[PstateCmd] of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's MSRC001_0062[PstateCmd].</p> <p>Similarly, C-states are “dynamically requested by software” and also dependent upon clock frequency. <i>See</i> BKDG §§ 2.5.2.2.2, 2.5.2.2.3, 3.14</p>

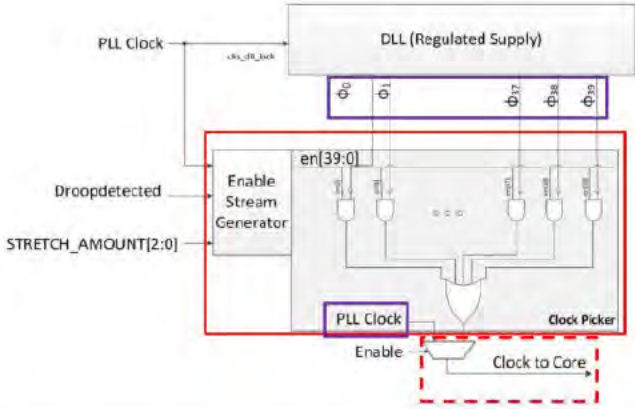
	<u>Limitation</u>	<u>Contention</u>
		<p>2.5.2.2.2 C-state Request Interface</p> <p>C-states are dynamically requested by software and are exposed through ACPI objects (see 2.5.2.2.6 [ACPI Processor C-state Objects]). C-states can be requested on a per-core basis. Software requests a C-state change in one of two ways:</p> <ul style="list-style-type: none"> • Reading from an IO address: The IO address must be the address specified by <code>MSRC001_0073[CstateAddr]</code> plus an offset of 0 through 7. The processor always returns 0 for this IO read. Offsets 2 through 7 result in an offset of 2. • Executing the HLT instruction. This is equivalent to reading from the IO address specified by <code>D18F4x128[HaltCstateIndex]</code>. <p>When software requests a C-state transition, hardware evaluates any frequency and voltage domain dependencies and determines which C-state actions to execute. See 2.5.2.2.3 [C-state Actions].</p> <p>2.5.2.2.3 C-state Actions</p> <p>A core takes one of several different possible actions based upon a C-state change request from software. The C-state action fields are defined in <code>D18F4x11[C:8]</code>.</p> <p><u>D18F4x11[C:8] C-state Control</u></p> <p><code>D18F4x11[C:8]</code> consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.2.2 [Core C-states].</p> <ul style="list-style-type: none"> • <code>D18F4x118[15:0]</code> specifies the actions attempted by the core when software reads from the IO address specified by <code>MSRC001_0073[CstateAddr]</code>. • <code>D18F4x118[31:16]</code> specifies the actions attempted by the core when software reads from the IO address specified by <code>MSRC001_0073[CstateAddr]+1</code>. • <code>D18F4x11C[15:0]</code> specifies the actions attempted by the core when software reads from the IO address specified by <code>MSRC001_0073[CstateAddr]+2</code>. <p>D18F4x118 C-state Control 1</p>

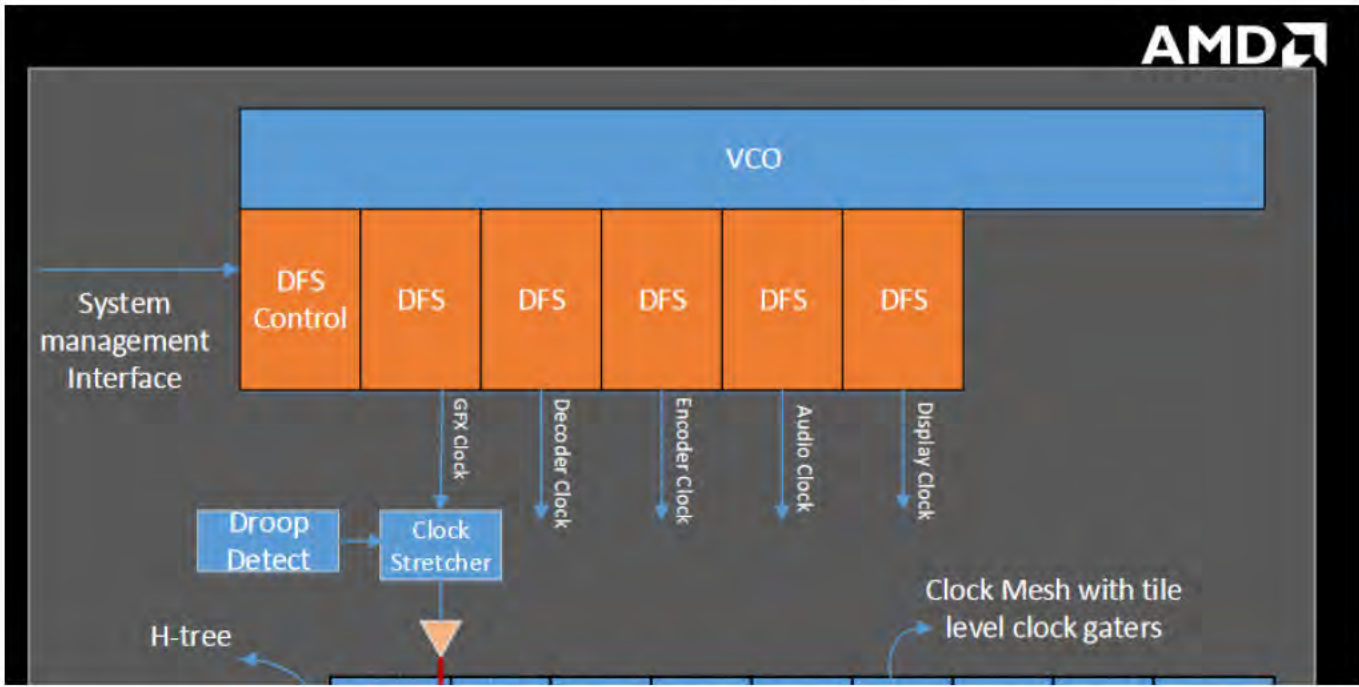
	<u>Limitation</u>	<u>Contention</u>																				
		<p>7:5 ClkDivisorCstAct0: clock divisor. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or:</p> <ul style="list-style-type: none"> • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid[5:0]]) of the current P-state specified by MSRC001_0063[CurPstate]. <p>If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.</p> <table border="1" data-bbox="962 560 1814 738"> <thead> <tr> <th>Bits</th> <th>Description</th> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>/1</td> <td>100b</td> <td>/16</td> </tr> <tr> <td>001b</td> <td>/2</td> <td>101b</td> <td>Reserved</td> </tr> <tr> <td>010b</td> <td>/4</td> <td>110b</td> <td>Reserved</td> </tr> <tr> <td>011b</td> <td>/8</td> <td>111b</td> <td>Turn off clocks.</td> </tr> </tbody> </table> <p>See CacheFlushTmrSelCstAct0.</p>	Bits	Description	Bits	Description	000b	/1	100b	/16	001b	/2	101b	Reserved	010b	/4	110b	Reserved	011b	/8	111b	Turn off clocks.
Bits	Description	Bits	Description																			
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011b	/8	111b	Turn off clocks.																			
1a	a first memory that stores a clock control library for controlling a clock frequency transition between said ordinary operation modes;	The Accused Products include a first memory that stores a clock control library. For example, the SMU contains memory that stores the firmware, including a clock control library. The clock control library controls clock frequency transition between the P-states. See e.g., BKDG, Table 270:																				

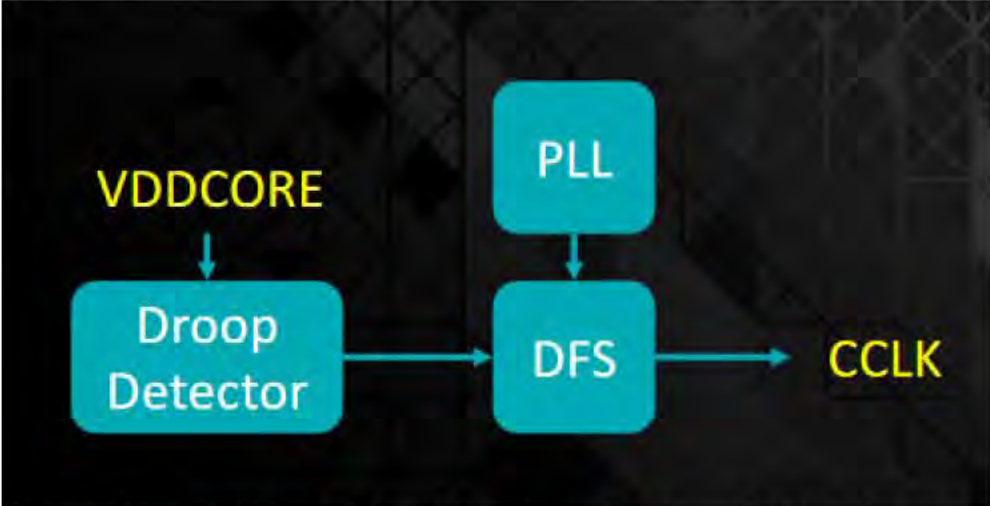
<u>Limitation</u>	<u>Contention</u>																		
	<p>MSRC001_00[6B:64] P-state [7:0]</p> <hr/> <p>Per-node. Cold reset: Varies by product. Each of these registers specify the frequency and voltage associated with each of the core P-states.</p> <p>Table 270: Register Mapping for MSRC001_00[6B:64]</p> <table border="1" data-bbox="857 461 1723 854"> <thead> <tr> <th>Register</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>MSRC001_0064</td> <td>P-state 0</td> </tr> <tr> <td>MSRC001_0065</td> <td>P-state 1</td> </tr> <tr> <td>MSRC001_0066</td> <td>P-state 2</td> </tr> <tr> <td>MSRC001_0067</td> <td>P-state 3</td> </tr> <tr> <td>MSRC001_0068</td> <td>P-state 4</td> </tr> <tr> <td>MSRC001_0069</td> <td>P-state 5</td> </tr> <tr> <td>MSRC001_006A</td> <td>P-state 6</td> </tr> <tr> <td>MSRC001_006B</td> <td>P-state 7</td> </tr> </tbody> </table> <p>The CpuVid field in these registers is required to be programmed to the same value in all cores of a processor, but are allowed to be different between processors in a multi-processor system. All other fields in these registers are required to be programmed to the same value in each core of the coherent fabric. See 2.5.2 [CPU Core Power Management].</p> <p>See also BKDG, Table 10:</p>	Register	Function	MSRC001_0064	P-state 0	MSRC001_0065	P-state 1	MSRC001_0066	P-state 2	MSRC001_0067	P-state 3	MSRC001_0068	P-state 4	MSRC001_0069	P-state 5	MSRC001_006A	P-state 6	MSRC001_006B	P-state 7
Register	Function																		
MSRC001_0064	P-state 0																		
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MSRC001_006B	P-state 7																		

	<u>Limitation</u>	<u>Contention</u>																																								
		<p>Table 10: Software P-state Naming</p> <table border="1" data-bbox="870 318 1741 792"> <thead> <tr> <th colspan="2" data-bbox="870 318 1300 360">D18F4x15C[NumBoostStates]=1</th> <th colspan="2" data-bbox="1300 318 1741 360">D18F4x15C[NumBoostStates]=3</th> </tr> <tr> <th data-bbox="870 360 1064 438">P-state Name</th> <th data-bbox="1064 360 1300 438">Corresponding Register Address</th> <th data-bbox="1300 360 1494 438">P-state Name</th> <th data-bbox="1494 360 1741 438">Corresponding Register Address</th> </tr> </thead> <tbody> <tr> <td data-bbox="870 438 1064 480">Pb0</td> <td data-bbox="1064 438 1300 480">MSRC001_0064</td> <td data-bbox="1300 438 1494 480">Pb0</td> <td data-bbox="1494 438 1741 480">MSRC001_0064</td> </tr> <tr> <td data-bbox="870 480 1064 522">P0 (base)</td> <td data-bbox="1064 480 1300 522">MSRC001_0065</td> <td data-bbox="1300 480 1494 522">Pb1</td> <td data-bbox="1494 480 1741 522">MSRC001_0065</td> </tr> <tr> <td data-bbox="870 522 1064 565">P1</td> <td data-bbox="1064 522 1300 565">MSRC001_0066</td> <td data-bbox="1300 522 1494 565">Pb2</td> <td data-bbox="1494 522 1741 565">MSRC001_0066</td> </tr> <tr> <td data-bbox="870 565 1064 607">P2</td> <td data-bbox="1064 565 1300 607">MSRC001_0067</td> <td data-bbox="1300 565 1494 607">P0 (base)</td> <td data-bbox="1494 565 1741 607">MSRC001_0067</td> </tr> <tr> <td data-bbox="870 607 1064 649">P3</td> <td data-bbox="1064 607 1300 649">MSRC001_0068</td> <td data-bbox="1300 607 1494 649">P1</td> <td data-bbox="1494 607 1741 649">MSRC001_0068</td> </tr> <tr> <td data-bbox="870 649 1064 691">P4</td> <td data-bbox="1064 649 1300 691">MSRC001_0069</td> <td data-bbox="1300 649 1494 691">P2</td> <td data-bbox="1494 649 1741 691">MSRC001_0069</td> </tr> <tr> <td data-bbox="870 691 1064 734">P5</td> <td data-bbox="1064 691 1300 734">MSRC001_006A</td> <td data-bbox="1300 691 1494 734">P3</td> <td data-bbox="1494 691 1741 734">MSRC001_006A</td> </tr> <tr> <td data-bbox="870 734 1064 792">P6</td> <td data-bbox="1064 734 1300 792">MSRC001_006B</td> <td data-bbox="1300 734 1494 792">P4</td> <td data-bbox="1494 734 1741 792">MSRC001_006B</td> </tr> </tbody> </table> <p data-bbox="870 841 2021 873">All sections and register definitions use software P-state numbering unless otherwise specified.</p>	D18F4x15C[NumBoostStates]=1		D18F4x15C[NumBoostStates]=3		P-state Name	Corresponding Register Address	P-state Name	Corresponding Register Address	Pb0	MSRC001_0064	Pb0	MSRC001_0064	P0 (base)	MSRC001_0065	Pb1	MSRC001_0065	P1	MSRC001_0066	Pb2	MSRC001_0066	P2	MSRC001_0067	P0 (base)	MSRC001_0067	P3	MSRC001_0068	P1	MSRC001_0068	P4	MSRC001_0069	P2	MSRC001_0069	P5	MSRC001_006A	P3	MSRC001_006A	P6	MSRC001_006B	P4	MSRC001_006B
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P6	MSRC001_006B	P4	MSRC001_006B																																							
1b	<p>a system control circuit which has a register, wherein said system control circuit carries out the clock frequency transition between said ordinary operation modes and said special modes in response to a change of a value in said register, and also carries out the clock frequency transition among said ordinary operation modes in response to said clock control library;</p>	<p>The Accused Product has a system control circuit, for example, the System Management Unit and/or the System Management Controller, that has a register. See e.g., BKDG:</p> <ul style="list-style-type: none"> • Northbridge: <ul style="list-style-type: none"> • One communication packet routing block referred to as the northbridge (NB). The NB routes transactions between the cores, the link, and the DRAM interfaces. It includes the configuration register space for the device. 																																								

	<u>Limitation</u>	<u>Contention</u>
		<p>2.13 System Management Unit (SMU)</p> <p>The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. The SMU uses two blocks, System Management Controller (SMC) and Platform Security Processor (PSP), in order to assist with many of these tasks. At the architectural level, PSP is known as MP0 and SMC is known as MP1.</p> <p>2.13.1 System Management Controller (SMC)</p> <p>The SMC is a standalone complex within AMD Family 15h Models 60h-6Fh processors that is responsible for maintaining the power management environment. Its functions include dynamic power management, state switching and fan control. <u>The SMC contains a microcontroller</u> to assist with many of these tasks.</p> <p>The SMU controls the clock frequency transitions between the core P-states. See e.g., SATHE et al.: RESONANT-CLOCK DESIGN FOR A POWER-EFFICIENT, HIGH-VOLUME X86-64 MICROPROCESSOR, p.144</p> <p>tion of the configuration programming interface. On receiving notification from the NB of a PState transition, the core implements a PState entry sequence which transitions the core into a clock-gated state. A program sequencer then accesses a</p>
1c	a clock generation circuit that receives a plurality of standard clocks, wherein said clock generation circuit generates a clock supplied to said central processing unit according to control by said system control circuit; and	<p>The Accused Products include a digital frequency synthesizer clock generation circuit, including the core PLL, clock multipliers and dividers, and/or the digital frequency synthesizer. The DFS receives a plurality of standard clocks, for example, different phases of the PLL clock or reference clock, and outputs the core clock such as CCLK to the CPU.</p> <p>The clock generator circuit includes at least the PLL and the digital frequency synthesizer. The DFS receives a plurality of standard clocks (the 40 phases of the reference clocks), and generates CCLK according to control by the SMU:</p>

<u>Limitation</u>	<u>Contention</u>
	<p data-bbox="854 354 1241 376"><i>D. Glitch Less Clock Phase Picker</i></p> <p data-bbox="854 393 1537 711">The glitch-less clock picker (Fig. 6) takes the 40 phases (40 total phases generated from the 20 DLL delay elements) and generates a stretched clock (configurable stretch amount) by selecting different phases of the clock. The clock picker always performs a complete loop through all the phases before selecting the 0th phase (pll_clk) to avoid any contraction of the clock period. When the clock stretcher block is disabled (STRETCH_ENABLE = 0), the clock picker simply picks the pll_clk without any insertion delay of the clock stretcher logic.</p>  <p data-bbox="844 724 2435 750">Source: WILCOX et al.: STEAMROLLER MODULE AND ADAPTIVE CLOCKING SYSTEM IN 28 nm CMOS, Fig. 6</p> <p data-bbox="844 792 2360 857">The digital frequency synthesizer receives multiple phases of the PLL clock (see above), and generates multiple discrete frequencies according to control by the SMU.</p> <div data-bbox="849 857 1951 1305" style="background-color: black; color: white; padding: 10px;"> <p data-bbox="865 899 1860 1084"> ▶ Digital frequency synthesizer (DFS) that generates multiple discrete frequencies from a single VCO </p> <ul data-bbox="946 1110 1913 1286" style="list-style-type: none"> <li data-bbox="946 1110 1349 1156">– Root clock gating <li data-bbox="946 1175 1913 1286">– Disabling VCO and bypassing with low speed fixed clocks </div>

<u>Limitation</u>	<u>Contention</u>
	 <p>The diagram illustrates the clock management architecture of the AMD Carrizo APU. At the top is a blue VCO (Voltage-Controlled Oscillator) block. Below it is a row of six orange blocks: DFS Control, followed by five DFS (Dynamic Frequency Scaling) blocks. A System Management Interface is connected to the DFS Control block. Below the DFS blocks, five clock outputs are shown: GFX clock, Decoder clock, Encoder clock, Audio clock, and Display clock. A Droop Detect block is connected to the DFS Control block, which in turn is connected to a Clock Stretcher block. The Clock Stretcher block is connected to an H-tree clock distribution network. The H-tree network is connected to a Clock Mesh with tile level clock gates. The AMD logo is visible in the top right corner of the diagram.</p> <p>Source: Krishnan et al., "Energy Efficient Graphics and Multimedia in 28nm Carrizo APU," p.14</p>

	<u>Limitation</u>	<u>Contention</u>
		 <p data-bbox="849 773 2370 841"><i>Source: Integrated Power Conversion Strategies Across Laptop, Server, and Graphics Products, 2016 Power SOC Conference, p.4.</i></p>
1d	<p data-bbox="290 899 817 1201">a second memory that stores an application program, wherein calling of said clock control library and changing of said register value are programmably controlled by said application program to enable user selectable clock frequency transitions,</p>	<p data-bbox="849 899 2440 1003">The Accused Products include a second memory, such as the hierarchy of L1, L2 and/or L3 caches that stores an application program, including but not limited to ACPI drivers, power management utilities, APIs provided by AMD, or any software that causes the SMU/SMC firmware to perform P-state transitions.</p>

	<u>Limitation</u>	<u>Contention</u>						
		<p>Core P-states are dynamically controlled by software and are exposed through ACPI objects (refer to 2.5.2.1.7.3 [ACPI Processor P-state Objects]). Software requests a core P-state change by writing a 3 bit index corresponding to the desired P-state number to MSRC001_0062[PstateCmd] of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's MSRC001_0062[PstateCmd].</p> <p>MSRC001_0062 P-state Control</p> <table border="1" data-bbox="873 537 2112 865"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>63:3</td> <td>MBZ.</td> </tr> <tr> <td>2:0</td> <td>PstateCmd: P-state change command. Read-write; Not-same-for-all. Cold reset value varies by product; after a warm reset, value initializes to the P-state the core was in prior to the reset. Writes to this field cause the core to change to the indicated non-boosted P-state number, specified by MSRC001_00[6B:64]. 0=P0, 1=P1, etc. P-state limits are applied to any P-state requests made through this register. Reads from this field return the last written value, regardless of whether any limits are applied. This field uses software P-state numbering. See 2.5.2 [CPU Core Power Management] and 2.5.2.1.1.1 [Software P-state Numbering].</td> </tr> </tbody> </table>	Bits	Description	63:3	MBZ.	2:0	PstateCmd: P-state change command. Read-write; Not-same-for-all. Cold reset value varies by product; after a warm reset, value initializes to the P-state the core was in prior to the reset. Writes to this field cause the core to change to the indicated non-boosted P-state number, specified by MSRC001_00[6B:64]. 0=P0, 1=P1, etc. P-state limits are applied to any P-state requests made through this register. Reads from this field return the last written value, regardless of whether any limits are applied. This field uses software P-state numbering. See 2.5.2 [CPU Core Power Management] and 2.5.2.1.1.1 [Software P-state Numbering].
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1e	<p>wherein said special modes comprise a first special mode in which clock supply to principal constituents of said central processing unit is halted, a second special mode in which clock supply to an entirety of said central processing unit is halted, and a third special mode in which supply of power to the entirety of said central processing unit is halted.</p>	<p>The Accused Products include a first special mode in which clock supply to principal constituents of said central processing unit is halted, for example the core C1 (CC1) state:</p>						

Limitation	Contention																				
	<p>2.5.2.2.3.2 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[CkDivisorCstAct].</p> <p>D18F4x11C[8] C-state Control</p> <p>D18F4x11C[8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.2.2 [Core C-states].</p> <ul style="list-style-type: none"> D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]. D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1. D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2. <p>D18F4x118 C-state Control 1</p> <table border="1"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>31:30</td> <td>Reserved.</td> </tr> <tr> <td>29</td> <td>SelfRefrEarly1. Read-write. Reset: 0. See SelfRefrEarly0. BIOS: 0. IF (D18F4x128[CoreCstate-Mode] == 0) THEN 0.</td> </tr> </tbody> </table> <p>2.5.2.2.3 C-state Actions</p> <p>A core takes one of several different possible actions based upon a C-state change req. C-state action fields are defined in D18F4x11C[8].</p> <p>D18F4x11C[8] C-state Control</p> <p>D18F4x11C[8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.2.2 [Core C-states].</p> <ul style="list-style-type: none"> D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]. D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1. D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2. <p>D18F4x118 C-state Control 1</p> <table border="1"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>31:30</td> <td>Reserved.</td> </tr> <tr> <td>29</td> <td>SelfRefrEarly1. Read-write. Reset: 0. See SelfRefrEarly0. BIOS: 0. IF (D18F4x128[CoreCstate-Mode] == 0) THEN 0.</td> </tr> </tbody> </table>	Bits	Description	31:30	Reserved.	29	SelfRefrEarly1 . Read-write. Reset: 0. See SelfRefrEarly0. BIOS: 0. IF (D18F4x128[CoreCstate-Mode] == 0) THEN 0.	Bits	Description	31:30	Reserved.	29	SelfRefrEarly1 . Read-write. Reset: 0. See SelfRefrEarly0. BIOS: 0. IF (D18F4x128[CoreCstate-Mode] == 0) THEN 0.								
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	<p>13 SelfRefrEarly0: allow early self-refresh. Read-write. Reset: 0. BIOS: 0. 1=Allow self-refresh while cores in PC1 or CC1 are waiting for the cache flush timer to expire. 0=Wait for cache flush timer to expire before allowing self-refresh. See 2.5.6.2 [DRAM Self-Refresh] and 2.5.2.2.3.1 [C-state Probes and Cache Flushing]. IF (D18F4x128[CoreCstateMode] == 0) THEN 0. ENDIF.</p> <p>7.5 CkDivisorCstAct0: clock divisor. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or: • $100 \text{ MHz} * (10b + \text{MSRC001_00[6B:64][CpuFid][5:0]})$ of the current P-state specified by MSRC001_0063[CurPstate]. If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.</p> <table border="1"> <thead> <tr> <th>Bits</th> <th>Description</th> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>/1</td> <td>100b</td> <td>/16</td> </tr> <tr> <td>001b</td> <td>/2</td> <td>101b</td> <td>Reserved</td> </tr> <tr> <td>010b</td> <td>/4</td> <td>110b</td> <td>Reserved</td> </tr> <tr> <td>011b</td> <td>/8</td> <td>111b</td> <td>Turn off clocks.</td> </tr> </tbody> </table> <p>See CacheFlushTrnSelCstAct0.</p> <p>4 Reserved.</p>	Bits	Description	Bits	Description	000b	/1	100b	/16	001b	/2	101b	Reserved	010b	/4	110b	Reserved	011b	/8	111b	Turn off clocks.
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	<p>The Accused Products include a second special mode in which clock supply to an entirety of said central processing unit is halted, for example the package C1 (PC1) state:</p>																				

	<u>Limitation</u>	<u>Contention</u>
		<p>The Accused Products include a third special mode in which supply of power to the entirety of said central processing unit is halted, for example the package C6 (PC6) state:</p> <p>2.5.2.2.3.4 <u>Package C6 (PC6) State</u></p> <p>When all cores enter a non-C0 state, <u>VDD can be reduced to a non-operational voltage</u> that does not retain core state. This state is known as PC6 and reduces the amount of static and dynamic power consumed by all cores. The following actions are taken by hardware prior to PC6 entry:</p> <ol style="list-style-type: none"> 1. If <code>MSRC001_0071[CurPstate] < D18F3xA8[PopDownPstate]</code>, transition the core P-state to <code>D18F3xA8[PopDownPstate]</code>. 2. For all cores not in CC6, L1 and L2 caches are flushed to DRAM. See 2.5.2.2.3.1 [C-state Probes and Cache Flushing]. 3. For all cores not in CC6, internal core state is saved to DRAM. 4. VDD is transitioned to the VID specified by <code>D18F5x128[PC6Vid]</code>. <p>All of the following must be true on all cores in order for a package to be placed into PC6:</p> <ul style="list-style-type: none"> • <code>D18F4x118/D18F4x11C[CacheFlushEn] = 1</code> for the corresponding C-state action field. • <code>D18F4x118/D18F4x11C[CacheFlushTmrSel] != 11b</code> for the corresponding C-state action field. • <code>D18F4x118/D18F4x11C[PwrOffEnCstAct] = 1</code> for the corresponding C-state action field. • <code>D18F2x118[CC6SaveEn] = 1</code>. • <code>D18F2x118[LockDramCfg] = 1</code>. • <code>MSRC001_0015[HltXSpCycEn] = 1</code>.
2p	A system LSI as claimed in claim 1, wherein said clock control library comprises:	

	<u>Limitation</u>	<u>Contention</u>
2a	a plurality of libraries that control said system control circuit and said clock generation circuit to transition the clock frequencies supplied to said central processing unit; and	The clock control libraries of the Accused Products contain a plurality of libraries that control the SMU and clock generator to transition clock frequencies. For example, source code provided by AMD to coreboot indicates that P-state and C-state transitions are controlled by separate libraries: https://chromium.googlesource.com/chromiumos/third_party/coreboot/+/firmware-winky-5216.1.B/src/vendorcode/amd/agesa/f15/Proc/CPU/Family/0x15/OR/
2b	a main library which is called by said application program and selects any one of said libraries in correspondence with the clock frequency supplied to said central processing unit.	As discussed above, P-states and C-states may be controlled by software, which includes a main library that calls upon the plurality of libraries.
3p	A system LSI as claimed in claim 2,	
3a	wherein said main library is described using a same program language as said application program.	The main library in the SMU firmware and the application program instructions stored in the caches are both use the same language such as machine code.
5p	A system LSI as claimed in claim 2,	
5a	wherein each of said libraries is described using a program language capable of directly controlling said clock generation circuit and said system control circuit.	The SMU firmware directly controls the SMU hardware.

	<u>Limitation</u>	<u>Contention</u>
6p	A system LSI as claimed in claim 5,	
6a	wherein each of said libraries is described using an assembler language.	The SMU firmware directly controls the SMU hardware and is described using an assembler language such as machine code.
7p	7. A system LSI as claimed in claim 1, wherein said system control circuit comprises:	
7a	a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit;	<p>The NB of the Accused Products contains a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit. The NB contains the configuration register space for the Accused Products.</p> <p>See BKDG section 2.1:</p> <ul style="list-style-type: none"> • Northbridge: <ul style="list-style-type: none"> • One communication packet routing block referred to as the northbridge (NB). The NB routes transactions between the cores, the link, and the DRAM interfaces. It includes the configuration register space for the device. <p>Configuration space register mnemonics are defined in section 3.1 of the BKDG:</p> <ul style="list-style-type: none"> • DXFYxZZZ: PCI-defined configuration space; X specifies the hexadecimal device number (this may be 1 or 2 digits), Y specifies the function number, and ZZZ specifies the hexadecimal byte address (this may be 2 or 3 digits; e.g., D18F3x40 specifies the register at device 18h, function 3, and address 40h). See 2.7 [Configuration Space], for details about configuration space.

	<u>Limitation</u>	<u>Contention</u>						
		<p>2.5.2.2.3.2 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C ClkDivisorCstAct.</p> <p>D18F4x11C 8 C-state Control</p> <p>D18F4x11C 8 consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.2.2 [Core C-states].</p> <ul style="list-style-type: none"> D18F4x118 15:0 specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073 CstateAddr . D18F4x118 31:16 specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073 CstateAddr +1. D18F4x11C 15:0 specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073 CstateAddr +2. <p>D18F4x118 C-state Control 1</p> <table border="1"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>31:30</td> <td>Reserved.</td> </tr> <tr> <td>29</td> <td>SelfRefrEarly1. Read-write. Reset: 0. See SelfRefrEarly0. BIOS: 0. IF (D18F4x128 CoreCstate-Mode) == 0) THEN 0.</td> </tr> </tbody> </table>	Bits	Description	31:30	Reserved.	29	SelfRefrEarly1 . Read-write. Reset: 0. See SelfRefrEarly0. BIOS: 0. IF (D18F4x128 CoreCstate-Mode) == 0) THEN 0.
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7b	<p>a clock halting register that receives the clock from said clock generation circuit and individually sets the clock to be halted or supplied;</p>	<p>2.5.2.2.3.2 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C ClkDivisorCstAct.</p> <p>D18F4x11C 8 C-state Control</p> <p>D18F4x11C 8 consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.2.2 [Core C-states].</p> <ul style="list-style-type: none"> D18F4x118 15:0 specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073 CstateAddr . D18F4x118 31:16 specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073 CstateAddr +1. D18F4x11C 15:0 specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073 CstateAddr +2. <p>D18F4x118 C-state Control 1</p> <table border="1"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>31:30</td> <td>Reserved.</td> </tr> <tr> <td>29</td> <td>SelfRefrEarly1. Read-write. Reset: 0. See SelfRefrEarly0. BIOS: 0. IF (D18F4x128 CoreCstate-Mode) == 0) THEN 0.</td> </tr> </tbody> </table>	Bits	Description	31:30	Reserved.	29	SelfRefrEarly1 . Read-write. Reset: 0. See SelfRefrEarly0. BIOS: 0. IF (D18F4x128 CoreCstate-Mode) == 0) THEN 0.
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	<u>Limitation</u>	<u>Contention</u>																				
7c	And a status register that judges a state of said central processing unit immediately after being released from said third special mode.	<p data-bbox="868 267 1271 293">D18F3xC8 COFVID Status Low</p> <hr data-bbox="868 305 2145 311"/> <p data-bbox="868 316 1365 342">See 2.5.2 [CPU Core Power Management].</p> <table border="1" data-bbox="868 380 2145 1386"> <thead> <tr> <th data-bbox="868 380 962 418">Bits</th> <th data-bbox="962 380 2145 418">Description</th> </tr> </thead> <tbody> <tr> <td data-bbox="868 423 962 462">31:24</td> <td data-bbox="962 423 2145 500">CurNbVid[7:0]: current NB VID. Read-only; Updated-by-hardware. Cold reset: Product-specific. This field specifies the current VDDNB voltage.</td> </tr> <tr> <td data-bbox="868 505 962 544">23</td> <td data-bbox="962 505 2145 646">NbPstateDis: NB P-states disabled. Value: D18F5x174[NbPstateDis]. MSRC001_0071[NbPstateDis] is an alias of D18F5x174[NbPstateDis]. 0=NB P-state frequency and voltage changes are supported. See D18F5x170[SwNbPstateLoDis, NbPstateDisOnP0]. 1=NB P-state frequency and voltage changes are disabled.</td> </tr> <tr> <td data-bbox="868 651 962 690">22:21</td> <td data-bbox="962 651 2145 690">Reserved.</td> </tr> <tr> <td data-bbox="868 695 962 734">20</td> <td data-bbox="962 695 2145 771">CurCpuVid[7]. Read-only; Updated-by-hardware; Not-same-for-all. Cold reset: Product-specific. See CurCpuVid[6:0].</td> </tr> <tr> <td data-bbox="868 776 962 815">19</td> <td data-bbox="962 776 2145 815">Reserved.</td> </tr> <tr> <td data-bbox="868 820 962 859">18:16</td> <td data-bbox="962 820 2145 987">CurPstate: current P-state. Read-only; Updated-by-hardware; Not-same-for-all. Cold reset: Product-specific. Specifies the current P-state requested by the core. This field uses hardware P-state numbering. See MSRC001_0063[CurPstate] and 2.5.2.1.1.2 [Hardware P-state Numbering]. When a P-state change is requested, the value in this field is updated once all required frequency and voltage transitions are completed.</td> </tr> <tr> <td data-bbox="868 992 962 1031">15:9</td> <td data-bbox="962 992 2145 1096">CurCpuVid[6:0]: current core VID. Read-only; Updated-by-hardware; Not-same-for-all. Cold reset: Product-specific. CurCpuVid = {CurCpuVid[7], CurCpuVid[6:0]}. This field specifies the current VDD voltage.</td> </tr> <tr> <td data-bbox="868 1101 962 1140">8:6</td> <td data-bbox="962 1101 2145 1242">CurCpuDid: current core divisor ID. Read-only; Updated-by-hardware. Cold reset: Product-specific. Specifies the current CpuDid of the core. See MSRC001_00[6B:64]. When a P-state change is requested, the value in this field is updated once all required frequency and voltage transitions are completed.</td> </tr> <tr> <td data-bbox="868 1247 962 1286">5:0</td> <td data-bbox="962 1247 2145 1386">CurCpuFid: current core frequency ID. Read-only; Updated-by-hardware. Cold reset: Product-specific. Specifies the current CpuFid of the core. See MSRC001_00[6B:64]. When a P-state change is requested, the value in this field is updated once all required frequency and voltage transitions are completed.</td> </tr> </tbody> </table>	Bits	Description	31:24	CurNbVid[7:0]: current NB VID. Read-only; Updated-by-hardware. Cold reset: Product-specific. This field specifies the current VDDNB voltage.	23	NbPstateDis: NB P-states disabled. Value: D18F5x174[NbPstateDis]. MSRC001_0071[NbPstateDis] is an alias of D18F5x174[NbPstateDis]. 0=NB P-state frequency and voltage changes are supported. See D18F5x170[SwNbPstateLoDis, NbPstateDisOnP0]. 1=NB P-state frequency and voltage changes are disabled.	22:21	Reserved.	20	CurCpuVid[7]. Read-only; Updated-by-hardware; Not-same-for-all. Cold reset: Product-specific. See CurCpuVid[6:0].	19	Reserved.	18:16	CurPstate: current P-state. Read-only; Updated-by-hardware; Not-same-for-all. Cold reset: Product-specific. Specifies the current P-state requested by the core. This field uses hardware P-state numbering. See MSRC001_0063[CurPstate] and 2.5.2.1.1.2 [Hardware P-state Numbering]. When a P-state change is requested, the value in this field is updated once all required frequency and voltage transitions are completed.	15:9	CurCpuVid[6:0]: current core VID. Read-only; Updated-by-hardware; Not-same-for-all. Cold reset: Product-specific. CurCpuVid = {CurCpuVid[7], CurCpuVid[6:0]}. This field specifies the current VDD voltage.	8:6	CurCpuDid: current core divisor ID. Read-only; Updated-by-hardware. Cold reset: Product-specific. Specifies the current CpuDid of the core. See MSRC001_00[6B:64]. When a P-state change is requested, the value in this field is updated once all required frequency and voltage transitions are completed.	5:0	CurCpuFid: current core frequency ID. Read-only; Updated-by-hardware. Cold reset: Product-specific. Specifies the current CpuFid of the core. See MSRC001_00[6B:64]. When a P-state change is requested, the value in this field is updated once all required frequency and voltage transitions are completed.
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	<u>Limitation</u>	<u>Contention</u>
10p	A system LSI as claimed in claim 1,	
10a	wherein said first memory and said second memory are two independent memories which are separated from each other.	As detailed above, the first memory in the SMU and the second memory in the caches are independent memories that are separated from each other.

Exhibit B.3: Preliminary Infringement Claim Charts for U.S. Patent 6,895,519

Accused Products: AMD Family 16h Products

These preliminary infringement contentions were prepared without the benefit of the Court’s claim construction or the parties’ exchange of constructions. As of the date of these contentions, AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court’s constructions or to account for new information that becomes available.

	<u>Limitation</u>	<u>Contention</u>
1p	A system LSI having a plurality of ordinary operation modes and a plurality of special modes in response to clock frequencies supplied to a central processing unit, comprising:	<p>To the extent that the preamble is limiting, Aquila contends that it is met.</p> <p>For example, each product in the 16h Accused Product Family (“Accused Product”) is a system LSI.</p> <p>The Accused Product has a plurality of ordinary operation modes, for example the Core P-states. <i>See</i> BIOS and Kernel Developer’s Guide for AMD Family 16h Models 00h-0Fh Processors (“BKDG”), §2.5.3.1:</p> <p>2.5.3.1 Core P-states</p> <p>Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states (P0 through P7), specified in MSRC001_00[6B:64]. Out of cold reset, the voltage and frequency of the compute units is specified by MSRC001_0071[StartupPstate].</p> <p>BKDG, Table 9:</p>

<u>Limitation</u>	<u>Contention</u>																																								
	<p>Table 9: Software P-state Naming</p> <table border="1"> <thead> <tr> <th colspan="2" style="text-align: center;">D18F4x15C[NumBoost-States]=1</th> <th colspan="2" style="text-align: center;">D18F4x15C[NumBoost-States]=3</th> </tr> <tr> <th style="text-align: center;">P-state Name</th> <th style="text-align: center;">Corresponding MSR Address</th> <th style="text-align: center;">P-state Name</th> <th style="text-align: center;">Corresponding MSR Address</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Pb0</td> <td style="text-align: center;">MSRC001_0064</td> <td style="text-align: center;">Pb0</td> <td style="text-align: center;">MSRC001_0064</td> </tr> <tr> <td style="text-align: center;">P0</td> <td style="text-align: center;">MSRC001_0065</td> <td style="text-align: center;">Pb1</td> <td style="text-align: center;">MSRC001_0065</td> </tr> <tr> <td style="text-align: center;">P1</td> <td style="text-align: center;">MSRC001_0066</td> <td style="text-align: center;">Pb2</td> <td style="text-align: center;">MSRC001_0066</td> </tr> <tr> <td style="text-align: center;">P2</td> <td style="text-align: center;">MSRC001_0067</td> <td style="text-align: center;">P0</td> <td style="text-align: center;">MSRC001_0067</td> </tr> <tr> <td style="text-align: center;">P3</td> <td style="text-align: center;">MSRC001_0068</td> <td style="text-align: center;">P1</td> <td style="text-align: center;">MSRC001_0068</td> </tr> <tr> <td style="text-align: center;">P4</td> <td style="text-align: center;">MSRC001_0069</td> <td style="text-align: center;">P2</td> <td style="text-align: center;">MSRC001_0069</td> </tr> <tr> <td style="text-align: center;">P5</td> <td style="text-align: center;">MSRC001_006A</td> <td style="text-align: center;">P3</td> <td style="text-align: center;">MSRC001_006A</td> </tr> <tr> <td style="text-align: center;">P6</td> <td style="text-align: center;">MSRC001_006B</td> <td style="text-align: center;">P4</td> <td style="text-align: center;">MSRC001_006B</td> </tr> </tbody> </table> <p>All sections and register definitions use software P-state numbering unless otherwise specified.</p> <p>The Accused Product Family has a plurality of special modes, for example, the Core C-states or deep sleep modes such as ACPI S3 or connected standby S0i3. See BKDG, §§ 2.5.3.2, 2.5.3.2.1, 2.5:</p>	D18F4x15C[NumBoost-States]=1		D18F4x15C[NumBoost-States]=3		P-state Name	Corresponding MSR Address	P-state Name	Corresponding MSR Address	Pb0	MSRC001_0064	Pb0	MSRC001_0064	P0	MSRC001_0065	Pb1	MSRC001_0065	P1	MSRC001_0066	Pb2	MSRC001_0066	P2	MSRC001_0067	P0	MSRC001_0067	P3	MSRC001_0068	P1	MSRC001_0068	P4	MSRC001_0069	P2	MSRC001_0069	P5	MSRC001_006A	P3	MSRC001_006A	P6	MSRC001_006B	P4	MSRC001_006B
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	<u>Limitation</u>	<u>Contention</u>
		<p>2.5.3.2 Core C-states</p> <p>C-states are processor power states. C0 is the operational state in which instructions are executed. All other C-states are low-power states in which instructions are not executed. When coming out of warm and cold reset, the processor is transitioned to the C0 state.</p> <p>2.5.3.2.1 C-state Names and Numbers</p> <p>C-states are often referred to by an alphanumeric naming convention, C1, C2, C3, etc. The mapping between ACPI defined C-states and AMD specified C-states is not direct. AMD specified C-states are referred to as IO-based C-states. Up to three IO-based C-states are supported, IO-based C-state 0, 1, and 2. The IO-based C-state index corresponds to the offset added to MSRC001_0073[CstateAddr] to initiate a C-state request. See 2.5.3.2.2 [C-state Request Interface]. The actions taken by the processor when entering a low-power C-state are configured by software. See 2.5.3.2.3 [C-state Actions] for information about AMD specific actions.</p>

<u>Limitation</u>	<u>Contention</u>																																																																		
	<p>2.5 Power Management</p> <p>The processor supports many power management features in a variety of systems. Table 8 provides a summary of ACPI states and power management features and indicates whether they are supported.</p> <p>Table 8: Power Management Support</p> <table border="1"> <thead> <tr> <th>ACPI/Power Management State</th> <th>Supported</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>G0/S0/C0: Working</td> <td>Yes</td> <td></td> </tr> <tr> <td>G0/S0/C0: Core P-state transitions</td> <td>Yes</td> <td>2.5.3.1 [Core P-states]</td> </tr> <tr> <td>G0/S0/C0: NB P-state transitions</td> <td>Yes</td> <td>2.5.4.1 [NB P-states]</td> </tr> <tr> <td>G0/S0/C0: Hardware thermal control (HTC)</td> <td>Yes</td> <td>2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)]</td> </tr> <tr> <td>G0/S0/Per-core IO-based C-states</td> <td>Yes</td> <td rowspan="2">2.5.3.2 [Core C-states] and 2.5.1.3.2 [Low Power Voltages]</td> </tr> <tr> <td>G0/S0/C1: Halt</td> <td>Yes</td> </tr> <tr> <td>G0/S0/CC6: Per-core Power gating</td> <td>Yes</td> <td>2.5.3.2 [Core C-states]</td> </tr> <tr> <td>G0/S0: CPC-L2 power gating</td> <td>Yes</td> <td>2.5.3.2 [Core C-states]</td> </tr> <tr> <td>G0/S0/PC6: 0V support (VDD power plane).</td> <td>Yes</td> <td>2.5.3.2 [Core C-states] and 2.5.1.3.2 [Low Power Voltages]</td> </tr> <tr> <td>G0/S0/Cx: Cache flushing support</td> <td>Yes</td> <td>2.5.3.2.3.1 [C-state Probes and Cache Flushing]</td> </tr> <tr> <td>G0/S0: Northbridge C-states (DRAM self-refresh, NB clock-gating)</td> <td>Yes</td> <td>2.5.4.2 [NB C-states]</td> </tr> <tr> <td>G1/S1: Stand By (Powered On Suspend)</td> <td>No</td> <td></td> </tr> <tr> <td>G1/S3: Stand By (Suspend to RAM)</td> <td>Yes</td> <td>2.5.8.1 [S-states]</td> </tr> <tr> <td>G1/S4: Hibernate (Suspend to Disk)</td> <td>Yes</td> <td></td> </tr> <tr> <td>G1/S5: Shut Down (Soft Off)</td> <td>Yes</td> <td></td> </tr> <tr> <td>G3 Mechanical Off</td> <td>Yes</td> <td></td> </tr> <tr> <td>Parallel VID Interface</td> <td>No</td> <td rowspan="3">2.5.1 [Processor Power Planes And Voltage Control]</td> </tr> <tr> <td>Serial VID Interface 1</td> <td>No</td> </tr> <tr> <td>Serial VID Interface 2</td> <td>Yes</td> </tr> <tr> <td>Single-plane systems</td> <td>No</td> <td></td> </tr> <tr> <td>Number of voltage planes</td> <td>2</td> <td>2.5.1 [Processor Power Planes And Voltage Control]</td> </tr> <tr> <td>APM: Application Power Management</td> <td>Yes</td> <td>2.5.9 [Application Power Management (APM)]</td> </tr> </tbody> </table>	ACPI/Power Management State	Supported	Description	G0/S0/C0: Working	Yes		G0/S0/C0: Core P-state transitions	Yes	2.5.3.1 [Core P-states]	G0/S0/C0: NB P-state transitions	Yes	2.5.4.1 [NB P-states]	G0/S0/C0: Hardware thermal control (HTC)	Yes	2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)]	G0/S0/Per-core IO-based C-states	Yes	2.5.3.2 [Core C-states] and 2.5.1.3.2 [Low Power Voltages]	G0/S0/C1: Halt	Yes	G0/S0/CC6: Per-core Power gating	Yes	2.5.3.2 [Core C-states]	G0/S0: CPC-L2 power gating	Yes	2.5.3.2 [Core C-states]	G0/S0/PC6: 0V support (VDD power plane).	Yes	2.5.3.2 [Core C-states] and 2.5.1.3.2 [Low Power Voltages]	G0/S0/Cx: Cache flushing support	Yes	2.5.3.2.3.1 [C-state Probes and Cache Flushing]	G0/S0: Northbridge C-states (DRAM self-refresh, NB clock-gating)	Yes	2.5.4.2 [NB C-states]	G1/S1: Stand By (Powered On Suspend)	No		G1/S3: Stand By (Suspend to RAM)	Yes	2.5.8.1 [S-states]	G1/S4: Hibernate (Suspend to Disk)	Yes		G1/S5: Shut Down (Soft Off)	Yes		G3 Mechanical Off	Yes		Parallel VID Interface	No	2.5.1 [Processor Power Planes And Voltage Control]	Serial VID Interface 1	No	Serial VID Interface 2	Yes	Single-plane systems	No		Number of voltage planes	2	2.5.1 [Processor Power Planes And Voltage Control]	APM: Application Power Management	Yes	2.5.9 [Application Power Management (APM)]
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	<u>Limitation</u>	<u>Contention</u>
		<p>Furthermore, the Core P-states and Core C-states are in response to clock frequencies supplied to a central processing unit. For example, the core P-states are “characterized” by “core frequency;” core P-state changes are further requested by software. <i>See e.g.</i>, BKDG, § 2.5.3.1, 2.5.3.1.2:</p> <p>2.5.3.1 Core P-states</p> <p>Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states (P0 through P7), specified in MSRC001_00[6B:64]. Out of cold reset, the voltage and frequency of the compute units is specified by MSRC001_0071[StartupPstate].</p>

	<u>Limitation</u>	<u>Contention</u>
		<p>Support for dynamic core P-state changes is indicated by more than one enabled selection in <code>MSRC001_00[6B:64][PstateEn]</code>. At least one enabled P-state (P0) is specified for all processors.</p> <p>Software requests core P-state changes for each core independently using the hardware P-state control mechanism (a.k.a. fire and forget). Support for hardware P-state control is indicated by <code>CPUID Fn8000_0007_EDX[HwPstate]=1b</code>. Software may not request any P-state transitions using the hardware P-state control mechanism until the P-state initialization requirements defined in 2.5.3.1.6 [BIOS Requirements for Core P-state Initialization and Transitions] are complete.</p> <p>The processor supports independently-controllable frequency planes for each compute unit and the NB; and independently-controllable voltage planes. See 2.5.1 [Processor Power Planes And Voltage Control] for voltage plane definitions.</p> <p>The following terms may be applied to each of these planes:</p> <ul style="list-style-type: none"> • FID: frequency ID. Specifies the PLL frequency multiplier, relative to the reference clock, for a given domain. • DID: divisor ID. Specifies the post-PLL power-of-two divisor that can be used to reduce the operating frequency. • COF: current operating frequency. Specifies the operating frequency as a function of the FID and DID. Refer to <code>CoreCOF</code> for the CPU COF formula and <code>NBCOF</code> for the NB COF formula. • VID: voltage ID. Specifies the voltage level for a given domain. Refer to 2.5.1.2.1 [MinVid and MaxVid Check] for encodings. <p>All FID and DID parameters for software P-states must be programmed to equivalent values for all cores and NBs in the coherent fabric. See 2.5.3.1.1.1 [Software P-state Numbering]. Refer to <code>MSRC001_00[6B:64]</code> and <code>D18F5x16[C:0]</code> for further details on programming requirements.</p>

	<u>Limitation</u>	<u>Contention</u>
		<p>2.5.3.1.2 Core P-state Control</p> <p>Core P-states are dynamically controlled by software and are exposed through ACPI objects (refer to 2.5.3.1.8.3 [ACPI Processor P-state Objects]). Software requests a core P-state change by writing a 3 bit index corresponding to the desired P-state number to <code>MSRC001_0062[PstateCmd]</code> of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's <code>MSRC001_0062[PstateCmd]</code>.</p> <p>Boosted P-states may not be directly requested by software. Whenever software requests the P0 state on a processor that supports APM (i.e. writes 000b to <code>MSRC001_0062[PstateCmd]</code>), hardware dynamically places the core into the highest-performance P-state possible as determined by APM. See 2.5.9 [Application Power Management (APM)].</p> <p>Hardware sequences the frequency and voltage changes necessary to complete a P-state transition as specified by 2.5.3.1.5 [Core P-state Transition Behavior] with no additional software interaction required. Hardware also coordinates frequency and voltage changes when differing P-state requests are made on cores that share a frequency or voltage plane. See 2.5.2 [Frequency and Voltage Domain Dependencies] for details about hardware coordination.</p> <p>Similarly, C-states are “dynamically requested by software” and also dependent upon clock frequency. See BKDG §§ 2.5.3.2.3.2, 2.5.3.2.3.3, 2.5.3.2.3.2; p.320-321:</p>

	<u>Limitation</u>	<u>Contention</u>
		<p>2.5.3.2.3.2 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct].</p> <p>2.5.3.2.3.3 Core C6 (CC6) State</p> <p>A core can gate off power to its internal logic when it enters any non-C0 state. This power gated state is known as CC6. In order to enter CC6, hardware first enters CC1 then checks D18F4x118/D18F4x11C[PwrGateEnCstAct]. Power gating reduces the amount of power consumed by the core. VDD voltage is not reduced when a core is in CC6. The following sequence occurs when a core enters the CC6 state:</p> <ol style="list-style-type: none"> 1. If MSRC001_0071[CurPstate] < D18F3xA8[PopDownPstate], transition the core P-state to D18F3xA8[PopDownPstate]. 2. Internal core state is saved to L1 cache . 3. L1 cache is flushed to L2 cache. See 2.5.3.2.3.1 [C-state Probes and Cache Flushing]. 4. Power is removed from the core and the core PLL/voltage regulator is powered down as specified by D18F5x128[CC6PwrDwnRegEn].

<u>Limitation</u>	<u>Contention</u>																	
	<p>D18F4x11[C:8] C-state Control</p> <p>D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states].</p> <ul style="list-style-type: none"> • D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]. • D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1. • D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2. <p>D18F4x118 C-state Control 1</p> <table border="1" data-bbox="862 732 2319 1328"> <tr> <td data-bbox="862 732 970 1328">7:5</td> <td data-bbox="970 732 2319 1328"> <p>ClkDivisorCstAct0: clock divisor. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or:</p> <ul style="list-style-type: none"> • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. <p>If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.</p> <table border="1" data-bbox="970 1084 1803 1279"> <thead> <tr> <th data-bbox="970 1084 1104 1117"><u>Bits</u></th> <th data-bbox="1104 1084 1373 1117"><u>DescriptionBits</u></th> <th data-bbox="1373 1084 1803 1117"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td data-bbox="970 1117 1104 1149">000b</td> <td data-bbox="1104 1117 1373 1149">/1 100b</td> <td data-bbox="1373 1117 1803 1149">/16</td> </tr> <tr> <td data-bbox="970 1149 1104 1182">001b</td> <td data-bbox="1104 1149 1373 1182">/2 101b</td> <td data-bbox="1373 1149 1803 1182">/128</td> </tr> <tr> <td data-bbox="970 1182 1104 1214">010b</td> <td data-bbox="1104 1182 1373 1214">/4 110b</td> <td data-bbox="1373 1182 1803 1214">/512</td> </tr> <tr> <td data-bbox="970 1214 1104 1247">011b</td> <td data-bbox="1104 1214 1373 1247">/8 111b</td> <td data-bbox="1373 1214 1803 1247">Turn off clocks.</td> </tr> </tbody> </table> <p>See CacheFlushTmrSelCstAct0.</p> </td> </tr> </table>	7:5	<p>ClkDivisorCstAct0: clock divisor. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or:</p> <ul style="list-style-type: none"> • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. <p>If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.</p> <table border="1" data-bbox="970 1084 1803 1279"> <thead> <tr> <th data-bbox="970 1084 1104 1117"><u>Bits</u></th> <th data-bbox="1104 1084 1373 1117"><u>DescriptionBits</u></th> <th data-bbox="1373 1084 1803 1117"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td data-bbox="970 1117 1104 1149">000b</td> <td data-bbox="1104 1117 1373 1149">/1 100b</td> <td data-bbox="1373 1117 1803 1149">/16</td> </tr> <tr> <td data-bbox="970 1149 1104 1182">001b</td> <td data-bbox="1104 1149 1373 1182">/2 101b</td> <td data-bbox="1373 1149 1803 1182">/128</td> </tr> <tr> <td data-bbox="970 1182 1104 1214">010b</td> <td data-bbox="1104 1182 1373 1214">/4 110b</td> <td data-bbox="1373 1182 1803 1214">/512</td> </tr> <tr> <td data-bbox="970 1214 1104 1247">011b</td> <td data-bbox="1104 1214 1373 1247">/8 111b</td> <td data-bbox="1373 1214 1803 1247">Turn off clocks.</td> </tr> </tbody> </table> <p>See CacheFlushTmrSelCstAct0.</p>	<u>Bits</u>	<u>DescriptionBits</u>	<u>Description</u>	000b	/1 100b	/16	001b	/2 101b	/128	010b	/4 110b	/512	011b	/8 111b	Turn off clocks.
7:5	<p>ClkDivisorCstAct0: clock divisor. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or:</p> <ul style="list-style-type: none"> • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. <p>If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.</p> <table border="1" data-bbox="970 1084 1803 1279"> <thead> <tr> <th data-bbox="970 1084 1104 1117"><u>Bits</u></th> <th data-bbox="1104 1084 1373 1117"><u>DescriptionBits</u></th> <th data-bbox="1373 1084 1803 1117"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td data-bbox="970 1117 1104 1149">000b</td> <td data-bbox="1104 1117 1373 1149">/1 100b</td> <td data-bbox="1373 1117 1803 1149">/16</td> </tr> <tr> <td data-bbox="970 1149 1104 1182">001b</td> <td data-bbox="1104 1149 1373 1182">/2 101b</td> <td data-bbox="1373 1149 1803 1182">/128</td> </tr> <tr> <td data-bbox="970 1182 1104 1214">010b</td> <td data-bbox="1104 1182 1373 1214">/4 110b</td> <td data-bbox="1373 1182 1803 1214">/512</td> </tr> <tr> <td data-bbox="970 1214 1104 1247">011b</td> <td data-bbox="1104 1214 1373 1247">/8 111b</td> <td data-bbox="1373 1214 1803 1247">Turn off clocks.</td> </tr> </tbody> </table> <p>See CacheFlushTmrSelCstAct0.</p>	<u>Bits</u>	<u>DescriptionBits</u>	<u>Description</u>	000b	/1 100b	/16	001b	/2 101b	/128	010b	/4 110b	/512	011b	/8 111b	Turn off clocks.		
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	<u>Limitation</u>	<u>Contention</u>
1a	a first memory that stores a clock control library for controlling a clock frequency transition between said ordinary operation modes;	<p>The Accused Products include a first memory that stores a clock control library. For example, the SMU contains memory that stores the firmware and configuration space registers, including a clock control library. The clock control library controls clock frequency transition between the P-states. See e.g., BKDG, 29:</p> <ul style="list-style-type: none"> • Northbridge: <ul style="list-style-type: none"> • One communication packet routing block referred to as the northbridge (NB). The NB routes transactions between the cores, the link, and the DRAM interfaces. It includes the configuration register space for the device. <p>BKDG, section 2.12: 2.12 System Management Unit (SMU)</p> <p>The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. The SMU contains a microcontroller to assist with many of these tasks.</p> <p>See also BKDG, Table 10:</p>

	<u>Limitation</u>	<u>Contention</u>																																																												
		<p>Table 10: Software P-state Control</p> <table border="1"> <thead> <tr> <th colspan="3">D18F4x15C[NumBoostStates]=1</th> <th colspan="3">D18F4x15C[NumBoostStates]=3</th> </tr> <tr> <th>P-state Name</th> <th>Index Used for Requests/Status</th> <th>Corresponding MSR Address</th> <th>P-state Name</th> <th>Index Used for Requests/Status</th> <th>Corresponding MSR Address</th> </tr> </thead> <tbody> <tr> <td>Pb0</td> <td>n/a</td> <td>MSRC001_0064</td> <td>Pb0</td> <td>n/a</td> <td>MSRC001_0064</td> </tr> <tr> <td>P0</td> <td>0</td> <td>MSRC001_0065</td> <td>Pb1</td> <td>n/a</td> <td>MSRC001_0065</td> </tr> <tr> <td>P1</td> <td>1</td> <td>MSRC001_0066</td> <td>Pb2</td> <td>n/a</td> <td>MSRC001_0066</td> </tr> <tr> <td>P2</td> <td>2</td> <td>MSRC001_0067</td> <td>P0</td> <td>0</td> <td>MSRC001_0067</td> </tr> <tr> <td>P3</td> <td>3</td> <td>MSRC001_0068</td> <td>P1</td> <td>1</td> <td>MSRC001_0068</td> </tr> <tr> <td>P4</td> <td>4</td> <td>MSRC001_0069</td> <td>P2</td> <td>2</td> <td>MSRC001_0069</td> </tr> <tr> <td>P5</td> <td>5</td> <td>MSRC001_006A</td> <td>P3</td> <td>3</td> <td>MSRC001_006A</td> </tr> <tr> <td>P6</td> <td>6</td> <td>MSRC001_006B</td> <td>P4</td> <td>4</td> <td>MSRC001_006B</td> </tr> </tbody> </table>	D18F4x15C[NumBoostStates]=1			D18F4x15C[NumBoostStates]=3			P-state Name	Index Used for Requests/Status	Corresponding MSR Address	P-state Name	Index Used for Requests/Status	Corresponding MSR Address	Pb0	n/a	MSRC001_0064	Pb0	n/a	MSRC001_0064	P0	0	MSRC001_0065	Pb1	n/a	MSRC001_0065	P1	1	MSRC001_0066	Pb2	n/a	MSRC001_0066	P2	2	MSRC001_0067	P0	0	MSRC001_0067	P3	3	MSRC001_0068	P1	1	MSRC001_0068	P4	4	MSRC001_0069	P2	2	MSRC001_0069	P5	5	MSRC001_006A	P3	3	MSRC001_006A	P6	6	MSRC001_006B	P4	4	MSRC001_006B
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P1	1	MSRC001_0066	Pb2	n/a	MSRC001_0066																																																									
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P6	6	MSRC001_006B	P4	4	MSRC001_006B																																																									
1b	<p>a system control circuit which has a register, wherein said system control circuit carries out the clock frequency transition between said ordinary operation modes and said special modes in response to a change of a value in said register, and also carries out the clock frequency transition among said ordinary operation modes in response to said clock control library;</p>	<p>The Accused Product has a system control circuit, for example, the System Management Unit and/or the System Management Controller, that has a register. See e.g., BKDG:</p> <ul style="list-style-type: none"> Northbridge: <ul style="list-style-type: none"> One communication packet routing block referred to as the northbridge (NB). The NB routes transactions between the cores, the link, and the DRAM interfaces. It includes the configuration register space for the device. <p>BKDG, section 2.12: 2.12 System Management Unit (SMU)</p> <p>The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. The SMU contains a microcontroller to assist with many of these tasks.</p>																																																												

	<u>Limitation</u>	<u>Contention</u>
		<p>See also BKDG for 14h Family 00h-0Fh Processors, section 2.12:</p> <p>2.12 System Management Unit (SMU)</p> <p>The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details.</p> <p>2.12.1 Microcontroller</p> <p>The SMU contains a microcontroller with a 16k ROM and a 16k RAM.</p> <p>The NB/SMU controls the clock frequency transitions between the core P-states. See e.g., SATHE et al.: RESONANT-CLOCK DESIGN FOR A POWER-EFFICIENT, HIGH-VOLUME X86-64 MICROPROCESSOR, p.144</p> <p>tion of the configuration programming interface. On receiving notification from the NB of a PState transition, the core implements a PState entry sequence which transitions the core into a clock-gated state. A program sequencer then accesses a</p>
1c	<p>a clock generation circuit that receives a plurality of standard clocks, wherein said clock generation circuit generates a clock supplied to said central processing unit according to control by said system control circuit; and</p>	<p>The Accused Products include a digital frequency synthesizer clock generation circuit, including the core PLL, clock multipliers and dividers, and/or the digital frequency synthesizer. The DFS receives a plurality of standard clocks, for example, different phases of the PLL clock or reference clock, and outputs the core clock such as CCLK to the CPU.</p> <p>The clock generator circuit includes at least the PLL and the digital frequency synthesizer. The DFS receives a plurality of standard clocks (the 4 phases-offset references provided by the PLL), and generates CCLK according to control by the SMU:</p> <p>Singh et al., Jaguar: A Next-Generation Low-Power x86-64 Core, pp. 25-26:</p>

Limitation

Contention

3.4: Jaguar: A Next-Generation Low-Power x86-64 Core

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CU Level Clock Distribution

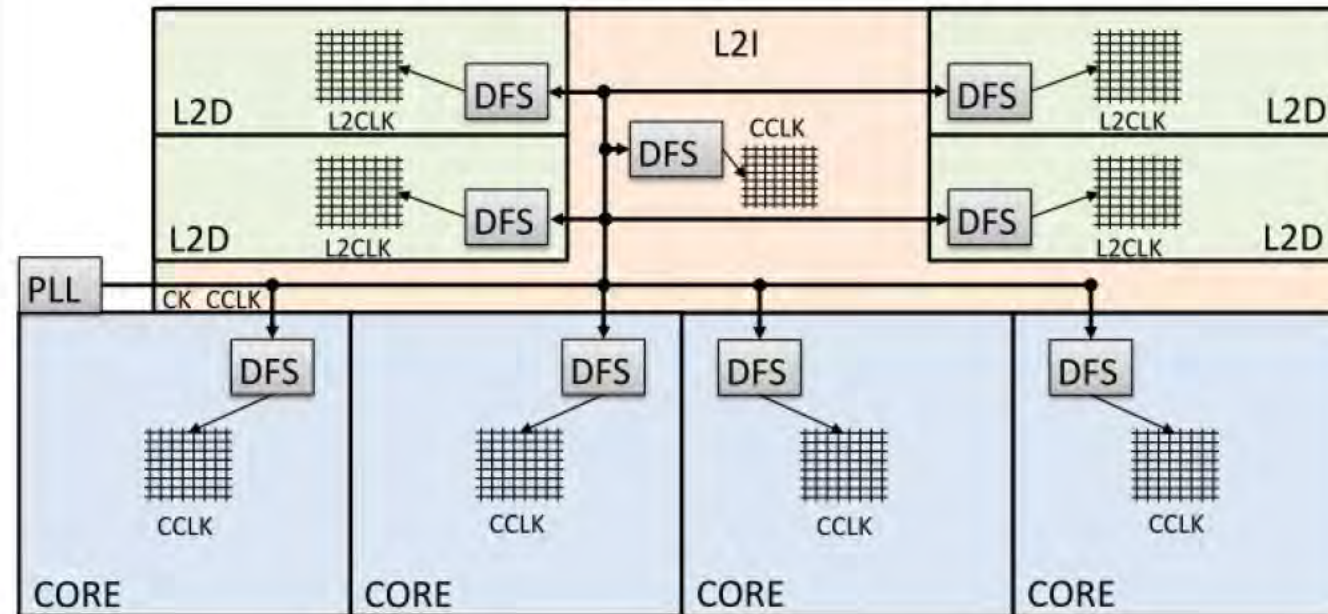
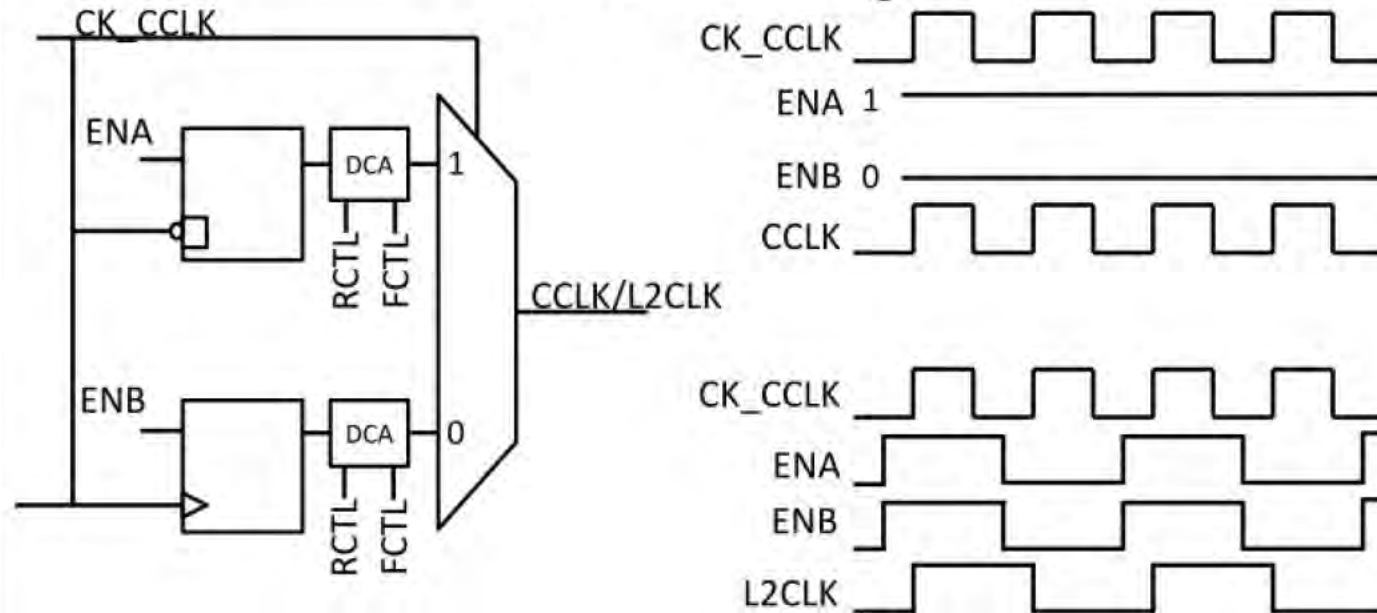


Exhibit B.3

Limitation

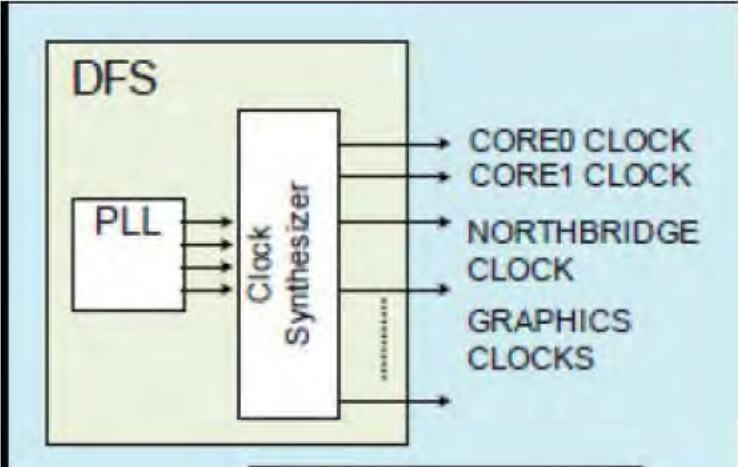
Contention

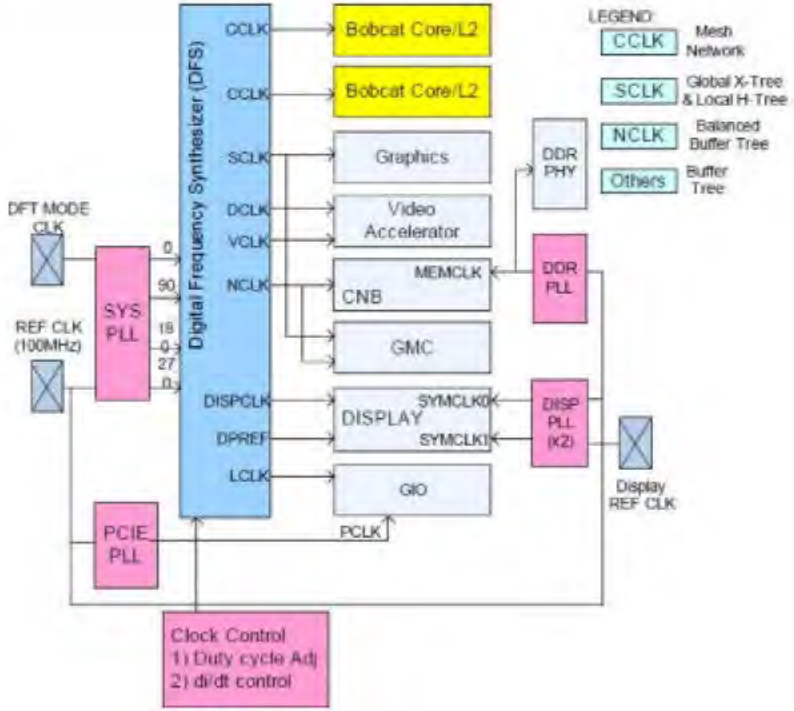
DFS Design



- Clock dividing for various operating modes
- Duty cycle adjuster for independent control of duty cycle within each block

See also:

	<u>Limitation</u>	<u>Contention</u>
		 <p>The diagram illustrates the clock distribution within a Dynamic Frequency Scaling (DFS) block. A Phase-Locked Loop (PLL) provides input to a Clock Synthesizer. The Clock Synthesizer then generates four distinct clock signals: CORE0 CLOCK, CORE1 CLOCK, NORTHBRIDGE CLOCK, and GRAPHICS CLOCKS.</p>

	<u>Limitation</u>	<u>Contention</u>
		 <p>The diagram illustrates the clock generation architecture. It starts with two reference clocks: DFT MODE CLK and REF CLK (100MHz). These feed into a Digital Frequency Synthesizer (DFS) block. The DFS outputs various clock signals: CCLK to Bobcat Core/L2, SCLK to Graphics, DCLK to Video Accelerator, VCLK to MEMCLK, NCLK to CNB, DISPCLK to DISPLAY, DPREF to DISPLAY, LCLK to GIO, and PCLK to PCIE PLL. The PCIE PLL also feeds into the DFS. The DFS also outputs signals to a DDR PHY and a DISP PLL (K2). A Clock Control block (containing Duty cycle Adj and di/dt control) is connected to the DFS. A legend defines the clock types: CCLK (Mesh Network), SCLK (Global X-Tree & Local H-Tree), NCLK (Balanced Buffer Tree), and Others (Buffer Tree).</p> <p>Fig. 11 DFS clock generation Source: Foley et al., A Low-Power Integrated x86-64 And Graphics Processor For Mobile Computing Devices, Fig. 1., 11; p.224-225.</p>
1d	a second memory that stores an application program, wherein calling of said clock control library	The Accused Products include a second memory, such as the hierarchy of L1, L2 caches that stores an application program, including but not limited to ACPI drivers, power management utilities, APIs provided by AMD, or any software that causes the SMU/SMC firmware to perform P-state transitions. See BKDG section 2.5.3.1.2; p. 548:

	<u>Limitation</u>	<u>Contention</u>
	<p>and changing of said register value are programmably controlled by said application program to enable user selectable clock frequency transitions,</p>	<p>2.5.3.1.2 Core P-state Control</p> <p>Core P-states are dynamically controlled by software and are exposed through ACPI objects (refer to 2.5.3.1.8.3 [ACPI Processor P-state Objects]). Software requests a core P-state change by writing a 3 bit index corresponding to the desired P-state number to <u>MSRC001_0062[PstateCmd]</u> of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's <u>MSRC001_0062[PstateCmd]</u>.</p> <p>Boosted P-states may not be directly requested by software. Whenever software requests the P0 state on a processor that supports APM (i.e. writes 000b to <u>MSRC001_0062[PstateCmd]</u>), hardware dynamically places the core into the highest-performance P-state possible as determined by APM. See 2.5.9 [Application Power Management (APM)].</p> <p>Hardware sequences the frequency and voltage changes necessary to complete a P-state transition as specified by 2.5.3.1.5 [Core P-state Transition Behavior] with no additional software interaction required. Hardware also coordinates frequency and voltage changes when differing P-state requests are made on cores that share a frequency or voltage plane. See 2.5.2 [Frequency and Voltage Domain Dependencies] for details about hardware coordination.</p>

	<u>Limitation</u>	<u>Contention</u>						
		<p>MSRC001_0062 P-state Control</p> <hr/> <table border="1"> <thead> <tr> <th data-bbox="844 354 951 402">Bits</th> <th data-bbox="951 354 2311 402">Description</th> </tr> </thead> <tbody> <tr> <td data-bbox="844 402 951 451">63:3</td> <td data-bbox="951 402 2311 451">MBZ.</td> </tr> <tr> <td data-bbox="844 451 951 743">2:0</td> <td data-bbox="951 451 2311 743"> PstateCmd: P-state change command. Read-write; Not-same-for-all. Cold reset value varies by product; after a warm reset, value initializes to the P-state the core was in prior to the reset. <u>Writes to this field cause the core to change to the indicated non-boosted P-state number, specified by MSRC001_00[6B:64]. 0=P0, 1=P1, etc.</u> P-state limits are applied to any P-state requests made through this register. Reads from this field return the last written value, regardless of whether any limits are applied. This field uses software P-state numbering. See 2.5.3 [CPU Power Management] and 2.5.3.1.1.1 [Software P-state Numbering]. </td> </tr> </tbody> </table>	Bits	Description	63:3	MBZ.	2:0	PstateCmd: P-state change command. Read-write; Not-same-for-all. Cold reset value varies by product; after a warm reset, value initializes to the P-state the core was in prior to the reset. <u>Writes to this field cause the core to change to the indicated non-boosted P-state number, specified by MSRC001_00[6B:64]. 0=P0, 1=P1, etc.</u> P-state limits are applied to any P-state requests made through this register. Reads from this field return the last written value, regardless of whether any limits are applied. This field uses software P-state numbering. See 2.5.3 [CPU Power Management] and 2.5.3.1.1.1 [Software P-state Numbering].
Bits	Description							
63:3	MBZ.							
2:0	PstateCmd: P-state change command. Read-write; Not-same-for-all. Cold reset value varies by product; after a warm reset, value initializes to the P-state the core was in prior to the reset. <u>Writes to this field cause the core to change to the indicated non-boosted P-state number, specified by MSRC001_00[6B:64]. 0=P0, 1=P1, etc.</u> P-state limits are applied to any P-state requests made through this register. Reads from this field return the last written value, regardless of whether any limits are applied. This field uses software P-state numbering. See 2.5.3 [CPU Power Management] and 2.5.3.1.1.1 [Software P-state Numbering].							
1e	<p>wherein said special modes comprise a first special mode in which clock supply to principal constituents of said central processing unit is halted, a second special mode in which clock supply to an entirety of said central processing unit is halted, and a third special mode in which supply of power to the entirety of said central processing unit is halted.</p>	<p>The Accused Products include a first special mode in which clock supply to principal constituents of said central processing unit is halted, for example the core C1 (CC1) state:</p> <p>2.5.3.2.3.2 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct].</p>						

	<u>Limitation</u>	<u>Contention</u>
		<p>2.5.3.2.3.2 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct].</p> <p>2.5.3.2.3.3 Core C6 (CC6) State</p> <p>A core can gate off power to its internal logic when it enters any non-C0 state. This power gated state is known as CC6. In order to enter CC6, hardware first enters CC1 then checks D18F4x118/D18F4x11C[PwrGateEnCstAct]. Power gating reduces the amount of power consumed by the core. VDD voltage is not reduced when a core is in CC6. The following sequence occurs when a core enters the CC6 state:</p> <ol style="list-style-type: none"> 1. If MSRC001_0071[CurPstate] < D18F3xA8[PopDownPstate], transition the core P-state to D18F3xA8[PopDownPstate]. 2. Internal core state is saved to L1 cache . 3. L1 cache is flushed to L2 cache. See 2.5.3.2.3.1 [C-state Probes and Cache Flushing]. 4. Power is removed from the core and the core PLL/voltage regulator is powered down as specified by D18F5x128[CC6PwrDwnRegEn].

<u>Limitation</u>	<u>Contention</u>																						
	<p>D18F4x11[C:8] C-state Control</p> <p>D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states].</p> <ul style="list-style-type: none"> • D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]. • D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1. • D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2. <p>D18F4x118 C-state Control 1</p> <table border="1" data-bbox="862 732 2319 1328"> <tr> <td data-bbox="862 732 970 1328">7:5</td> <td data-bbox="970 732 2319 1328"> <p>ClkDivisorCstAct0: clock divisor. Read-write. Reset: 0. BIOS: 000b.</p> <p>Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or:</p> <ul style="list-style-type: none"> • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. <p>If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.</p> <table border="1" data-bbox="970 1084 1809 1279"> <thead> <tr> <th data-bbox="970 1084 1104 1117"><u>Bits</u></th> <th data-bbox="1104 1084 1373 1117"><u>Description</u></th> <th data-bbox="1373 1084 1809 1117"><u>Bits</u></th> <th data-bbox="1809 1084 2319 1117"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td data-bbox="970 1117 1104 1149">000b</td> <td data-bbox="1104 1117 1373 1149">/1</td> <td data-bbox="1373 1117 1809 1149">100b</td> <td data-bbox="1809 1117 2319 1149">/16</td> </tr> <tr> <td data-bbox="970 1149 1104 1182">001b</td> <td data-bbox="1104 1149 1373 1182">/2</td> <td data-bbox="1373 1149 1809 1182">101b</td> <td data-bbox="1809 1149 2319 1182">/128</td> </tr> <tr> <td data-bbox="970 1182 1104 1214">010b</td> <td data-bbox="1104 1182 1373 1214">/4</td> <td data-bbox="1373 1182 1809 1214">110b</td> <td data-bbox="1809 1182 2319 1214">/512</td> </tr> <tr> <td data-bbox="970 1214 1104 1247">011b</td> <td data-bbox="1104 1214 1373 1247">/8</td> <td data-bbox="1373 1214 1809 1247">111b</td> <td data-bbox="1809 1214 2319 1247"><u>Turn off clocks.</u></td> </tr> </tbody> </table> <p>See CacheFlushTmrSelCstAct0.</p> </td> </tr> </table>	7:5	<p>ClkDivisorCstAct0: clock divisor. Read-write. Reset: 0. BIOS: 000b.</p> <p>Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or:</p> <ul style="list-style-type: none"> • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. <p>If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.</p> <table border="1" data-bbox="970 1084 1809 1279"> <thead> <tr> <th data-bbox="970 1084 1104 1117"><u>Bits</u></th> <th data-bbox="1104 1084 1373 1117"><u>Description</u></th> <th data-bbox="1373 1084 1809 1117"><u>Bits</u></th> <th data-bbox="1809 1084 2319 1117"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td data-bbox="970 1117 1104 1149">000b</td> <td data-bbox="1104 1117 1373 1149">/1</td> <td data-bbox="1373 1117 1809 1149">100b</td> <td data-bbox="1809 1117 2319 1149">/16</td> </tr> <tr> <td data-bbox="970 1149 1104 1182">001b</td> <td data-bbox="1104 1149 1373 1182">/2</td> <td data-bbox="1373 1149 1809 1182">101b</td> <td data-bbox="1809 1149 2319 1182">/128</td> </tr> <tr> <td data-bbox="970 1182 1104 1214">010b</td> <td data-bbox="1104 1182 1373 1214">/4</td> <td data-bbox="1373 1182 1809 1214">110b</td> <td data-bbox="1809 1182 2319 1214">/512</td> </tr> <tr> <td data-bbox="970 1214 1104 1247">011b</td> <td data-bbox="1104 1214 1373 1247">/8</td> <td data-bbox="1373 1214 1809 1247">111b</td> <td data-bbox="1809 1214 2319 1247"><u>Turn off clocks.</u></td> </tr> </tbody> </table> <p>See CacheFlushTmrSelCstAct0.</p>	<u>Bits</u>	<u>Description</u>	<u>Bits</u>	<u>Description</u>	000b	/1	100b	/16	001b	/2	101b	/128	010b	/4	110b	/512	011b	/8	111b	<u>Turn off clocks.</u>
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	<p>The Accused Products include a second special mode in which clock supply to an entirety of said central processing unit is halted, for example the package C1 (PC1) state. See e.g., 14h BKDG:</p> <p>2.5.3.2.3.3 Package C1 (PC1) State</p> <p>The processor enters the PC1 state with auto-Pmin when all of the following are true:</p> <ul style="list-style-type: none"> • All cores are in the CC1 state or deeper. <p>If D18F4x1AC[CstPminEn] indicates that auto-Pmin is enabled when the processor enters PC1, the P-state for all cores is transitioned as specified by 2.5.3.2.7.1 [Auto-Pmin]. Regardless of the state of D18F4x1AC[CstPminEn], all core clocks are ramped to the frequency specified by D18F4x1A8[AllHaltCpuDid].</p> <p>D18F4x1A8 CPU State Power Management Dynamic Control 0</p> <hr/> <p>Reset: 0000_0000h.</p> <table border="1" data-bbox="846 901 2306 1274"> <tr> <td data-bbox="846 901 954 1274">9:5</td> <td data-bbox="954 901 2306 1274"> <p>AllHaltCpuDid. Read-write. BIOS: 1Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State].</p> <table border="1" data-bbox="954 990 1330 1185"> <thead> <tr> <th data-bbox="954 990 1115 1031"><u>Bits</u></th> <th data-bbox="1115 990 1330 1031"><u>Divisor</u></th> </tr> </thead> <tbody> <tr> <td data-bbox="954 1031 1115 1063">1Ch-00h</td> <td data-bbox="1115 1031 1330 1063">Reserved.</td> </tr> <tr> <td data-bbox="954 1063 1115 1096">1Dh</td> <td data-bbox="1115 1063 1330 1096">128</td> </tr> <tr> <td data-bbox="954 1096 1115 1128">1Eh</td> <td data-bbox="1115 1096 1330 1128">512</td> </tr> <tr> <td data-bbox="954 1128 1115 1185"><u>1Fh</u></td> <td data-bbox="1115 1128 1330 1185"><u>Clocks off.</u></td> </tr> </tbody> </table> <p>See D18F4x1A8[SingleHaltCpuDid].</p> </td> </tr> </table> <p>The Accused Products include a third special mode in which supply of power to the entirety of said central processing unit is halted, for example the package C6 (PC6) state:</p>	9:5	<p>AllHaltCpuDid. Read-write. BIOS: 1Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State].</p> <table border="1" data-bbox="954 990 1330 1185"> <thead> <tr> <th data-bbox="954 990 1115 1031"><u>Bits</u></th> <th data-bbox="1115 990 1330 1031"><u>Divisor</u></th> </tr> </thead> <tbody> <tr> <td data-bbox="954 1031 1115 1063">1Ch-00h</td> <td data-bbox="1115 1031 1330 1063">Reserved.</td> </tr> <tr> <td data-bbox="954 1063 1115 1096">1Dh</td> <td data-bbox="1115 1063 1330 1096">128</td> </tr> <tr> <td data-bbox="954 1096 1115 1128">1Eh</td> <td data-bbox="1115 1096 1330 1128">512</td> </tr> <tr> <td data-bbox="954 1128 1115 1185"><u>1Fh</u></td> <td data-bbox="1115 1128 1330 1185"><u>Clocks off.</u></td> </tr> </tbody> </table> <p>See D18F4x1A8[SingleHaltCpuDid].</p>	<u>Bits</u>	<u>Divisor</u>	1Ch-00h	Reserved.	1Dh	128	1Eh	512	<u>1Fh</u>	<u>Clocks off.</u>
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	<u>Limitation</u>	<u>Contention</u>		
		<p>2.5.3.2.3.4 Package C6 (PC6) State</p> <p>When all cores enter a non-C0 state, VDD can be reduced to a non-operational voltage that does not retain core state. This state is known as PC6 and reduces the amount of static and dynamic power consumed by all cores. The following actions are taken by hardware prior to PC6 entry:</p> <ol style="list-style-type: none"> 1. If MSRC001_0071[CurPstate] < D18F3xA8[PopDownPstate], transition the core P-state to D18F3xA8[PopDownPstate]. 2. For all cores not in CC6, internal core state is saved to L1 cache . 3. For all cores not in CC6, L1 cache is flushed to L2 cache. See 2.5.3.2.3.1 [C-state Probes and Cache Flushing]. 4. VDD is transitioned to the VID specified by D18F5x128[PC6Vid]. 5. If the core PLLs are not powered down during CC6 entry (see 2.5.3.2.3.3 [Core C6 (CC6) State]), then they are powered down as specified by D18F5x128[PC6PwrDwnRegEn]. <p>D18F5x128 Clock Power/Timing Control 3</p> <hr/> <table border="1" data-bbox="844 961 2319 1094"> <tr> <td data-bbox="844 961 951 1094">6:0</td> <td data-bbox="951 961 2319 1094">PC6Vid[6:0]: package C6 vid. Read-write. Cold reset: Product-specific. PC6Vid[7:0] = {PC6Vid[7], PC6Vid[6:0]}. PC6Vid[7:0] specifies the VID driven in the PC6 state. See 2.5.3.2.3.4 [Package C6 (PC6) State] and 2.5.1.3.2 [Low Power Voltages].</td> </tr> </table>	6:0	PC6Vid[6:0]: package C6 vid. Read-write. Cold reset: Product-specific. PC6Vid[7:0] = {PC6Vid[7], PC6Vid[6:0]}. PC6Vid[7:0] specifies the VID driven in the PC6 state. See 2.5.3.2.3.4 [Package C6 (PC6) State] and 2.5.1.3.2 [Low Power Voltages].
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	<u>Limitation</u>	<u>Contention</u>
		<p>2.5.1.3.2 Low Power Voltages</p> <p>In order to save power, voltages lower than those normally needed for operation may be applied to the VDD power plane while the processor is in a C-state or S-state. The lower voltage is defined as follows:</p> <ul style="list-style-type: none"> • PC6Vid: D18F5x128[PC6Vid] specifies a voltage that does not retain the CPU caches or the core microarchitectural state. PC6Vid does not allow execution and is only applied to the cores. See 2.5.3.2.3.4 [Package C6 (PC6) State]. <p>2.5.1.4.1 Hardware-Initiated Voltage Transitions</p> <p>When software requests any of the following state changes, or hardware determines that any of the following state changes are necessary, hardware coordinates the necessary voltage changes:</p> <ul style="list-style-type: none"> • VDD: <ul style="list-style-type: none"> • Core P-state transition. See 2.5.3.1 [Core P-states]. • Package C-state transition. D18F5x128[PC6Vid] specifies a voltage that does not retain the CPU caches or the core microarchitectural state. PC6Vid does not allow execution and is only applied to the cores. See 2.5.3.2.3.4 [Package C6 (PC6) State]. • S-state transition. See 2.5.8.1 [S-states].
2p	A system LSI as claimed in claim 1, wherein said clock control library comprises:	
2a	a plurality of libraries that control said system control circuit and said	The clock control libraries of the Accused Products contain a plurality of libraries that control the SMU and clock generator to transition clock frequencies. For example, source code provided by AMD to coreboot indicates that P-state

	<u>Limitation</u>	<u>Contention</u>
	clock generation circuit to transition the clock frequencies supplied to said central processing unit; and	and C-state transitions are controlled by separate libraries: https://github.com/coreboot/coreboot/tree/master/src/vendorcode/amd/agesa/f14/Proc/CPU/Feature
2b	a main library which is called by said application program and selects any one of said libraries in correspondence with the clock frequency supplied to said central processing unit.	As discussed above, P-states and C-states may be controlled by software, which includes a main library that calls upon the plurality of libraries.
3p	A system LSI as claimed in claim 2,	
3a	wherein said main library is described using a same program language as said application program.	The main library in the SMU firmware and the application program instructions stored in the caches are both use the same language such as machine code.
5p	A system LSI as claimed in claim 2,	
5a	wherein each of said libraries is described using a program language capable of directly controlling said clock generation circuit and said system control circuit.	The SMU firmware directly controls the SMU hardware.
6p	A system LSI as claimed in claim 5,	
6a	wherein each of said libraries is described using an assembler	The SMU firmware directly controls the SMU hardware and is described using an assembler language such as machine code.

	<u>Limitation</u>	<u>Contention</u>
	language.	
7p	7. A system LSI as claimed in claim 1, wherein said system control circuit comprises:	
7a	a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit;	<p>The NB of the Accused Products contains a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit. The NB contains the configuration register space for the Accused Products.</p> <p>See BKDG: See e.g., BKDG:</p> <div style="text-align: center;"> <pre> graph TD A[] --> NB[Northbridge (NB)] B[] --> NB NB --- NB_L[Transaction routing] NB --- NB_R[Configuration and IO-space registers] NB --- NB_C[Root complex] NB --- NB_D[Graphics core (optional)] </pre> </div> <p>BKDG, section 2.12:</p>

	<u>Limitation</u>	<u>Contention</u>
		<p>2.12 System Management Unit (SMU)</p> <p>The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details.</p> <p>2.12.1 Microcontroller</p> <p>The SMU contains a microcontroller with a 16k ROM and a 16k RAM.</p> <p>Configuration space register mnemonics are defined in section 3.1 of the BKDG:</p> <ul style="list-style-type: none"> • DXFYxZZZ: PCI-defined configuration space; X specifies the hexadecimal device number (this may be 1 or 2 digits), Y specifies the function number, and ZZZ specifies the hexadecimal byte address (this may be 2 or 3 digits; e.g., D18F3x40 specifies the register at device 18h, function 3, and address 40h). See 2.7 [Configuration Space], for details about configuration space. <p>the core C1 (CC1) state:</p> <p>2.5.3.2.3.2 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct].</p>

<u>Limitation</u>	<u>Contention</u>																						
	<p>D18F4x11[C:8] C-state Control</p> <p>D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states].</p> <ul style="list-style-type: none"> • D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]. • D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1. • D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2. <p>D18F4x118 C-state Control 1</p> <table border="1" data-bbox="862 732 2319 1328"> <tr> <td data-bbox="862 732 970 1328">7:5</td> <td data-bbox="970 732 2319 1328"> <p>ClkDivisorCstAct0: clock divisor. Read-write. Reset: 0. BIOS: 000b.</p> <p>Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or:</p> <ul style="list-style-type: none"> • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. <p>If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.</p> <table border="1" data-bbox="983 1078 1776 1247"> <thead> <tr> <th>Bits</th> <th>Description</th> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>/1</td> <td>100b</td> <td>/16</td> </tr> <tr> <td>001b</td> <td>/2</td> <td>101b</td> <td>/128</td> </tr> <tr> <td>010b</td> <td>/4</td> <td>110b</td> <td>/512</td> </tr> <tr> <td>011b</td> <td>/8</td> <td>111b</td> <td>Turn off clocks.</td> </tr> </tbody> </table> <p>See CacheFlushTmrSelCstAct0.</p> </td> </tr> </table>	7:5	<p>ClkDivisorCstAct0: clock divisor. Read-write. Reset: 0. BIOS: 000b.</p> <p>Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or:</p> <ul style="list-style-type: none"> • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. <p>If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.</p> <table border="1" data-bbox="983 1078 1776 1247"> <thead> <tr> <th>Bits</th> <th>Description</th> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>/1</td> <td>100b</td> <td>/16</td> </tr> <tr> <td>001b</td> <td>/2</td> <td>101b</td> <td>/128</td> </tr> <tr> <td>010b</td> <td>/4</td> <td>110b</td> <td>/512</td> </tr> <tr> <td>011b</td> <td>/8</td> <td>111b</td> <td>Turn off clocks.</td> </tr> </tbody> </table> <p>See CacheFlushTmrSelCstAct0.</p>	Bits	Description	Bits	Description	000b	/1	100b	/16	001b	/2	101b	/128	010b	/4	110b	/512	011b	/8	111b	Turn off clocks.
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	<u>Limitation</u>	<u>Contention</u>
7b	a clock halting register that receives the clock from said clock generation circuit and individually sets the clock to be halted or supplied;	<p>the core C1 (CC1) state:</p> <p>2.5.3.2.3.2 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct].</p> <p>D18F4x11[C:8] C-state Control</p> <hr/> <p>D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states].</p> <ul style="list-style-type: none"> • D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]. • D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1. • D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2. <p>D18F4x118 C-state Control 1</p>

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7c	And a status register that judges a state of said central processing unit immediately after being released from said third special mode.	The Accused Products contain a status register that judges a state of the CPU after waking from PC6. See 14h BKDG:																				

	<u>Limitation</u>	<u>Contention</u>		
		<p>2.5.3.2.7.2 Exiting PC6</p> <p>If the PService timer is enabled when the processor exits PC6, all cores transition to the P-state specified by D18F4x1AC[PstateIdCoreOffExit]. The cores remain in this state until one of the following occurs:</p> <ul style="list-style-type: none"> • The PService timer expires while the package is in C0: In this case, the cores transition back to the last P-state requested by software. • The package enters PC1 without auto-Pmin: In this case, the PService timer continues counting. If it expires while in PC1, the cores remain in the P-state specified by D18F4x1AC[PstateIdCoreOffExit] until they return to C0, at which time they transition to the last P-state requested by software. • The package enters PC1 with auto-Pmin: In this case, the PService timer stops counting and the cores enter the PService state. • The package enters PC6: In this case the PService timer stops counting and the actions associated the requested package C-state occur. See 2.5.3.2.3.4 [Package C6 (PC6) State]. <p>If the PService timer is disabled when the processor exits PC6, the cores transition back to the last P-state requested by software.</p> <p>See also 14h BKDG pp.320-321:</p> <p><u>D18F4x1AC CPU State Power Management Dynamic Control 1</u></p> <table border="1" data-bbox="846 1052 2306 1352"> <tr> <td data-bbox="846 1052 954 1352">18:16</td> <td data-bbox="954 1052 2306 1352">PstateIdCoreOffExit. Read-write. Reset: 0. BIOS: See 2.5.3.2.9. When exiting the package C6 state, the core transitions to the P-state specified by this register. See 2.5.3.2.7.2 [Exiting PC6]. If PC6 is enabled (see 2.5.3.2.9 [BIOS Requirements for C-state Initialization]), PstateIdCoreOffExit must be programmed to the lowest-performance P-state displayed to the operating system or to any lower-performance P-state. This P-state must have a core clock frequency of at least 400 MHz. Programming this field to 0 causes the core to transition to the last P-state requested by software when exiting package C6. This field uses hardware P-state numbering. See 2.5.3.1.2.2 [Hardware P-state Numbering].</td> </tr> </table>	18:16	PstateIdCoreOffExit. Read-write. Reset: 0. BIOS: See 2.5.3.2.9 . When exiting the package C6 state, the core transitions to the P-state specified by this register. See 2.5.3.2.7.2 [Exiting PC6] . If PC6 is enabled (see 2.5.3.2.9 [BIOS Requirements for C-state Initialization]), PstateIdCoreOffExit must be programmed to the lowest-performance P-state displayed to the operating system or to any lower-performance P-state. This P-state must have a core clock frequency of at least 400 MHz. Programming this field to 0 causes the core to transition to the last P-state requested by software when exiting package C6. This field uses hardware P-state numbering. See 2.5.3.1.2.2 [Hardware P-state Numbering] .
18:16	PstateIdCoreOffExit. Read-write. Reset: 0. BIOS: See 2.5.3.2.9 . When exiting the package C6 state, the core transitions to the P-state specified by this register. See 2.5.3.2.7.2 [Exiting PC6] . If PC6 is enabled (see 2.5.3.2.9 [BIOS Requirements for C-state Initialization]), PstateIdCoreOffExit must be programmed to the lowest-performance P-state displayed to the operating system or to any lower-performance P-state. This P-state must have a core clock frequency of at least 400 MHz. Programming this field to 0 causes the core to transition to the last P-state requested by software when exiting package C6. This field uses hardware P-state numbering. See 2.5.3.1.2.2 [Hardware P-state Numbering] .			

	<u>Limitation</u>	<u>Contention</u>
10p	A system LSI as claimed in claim 1,	
10a	wherein said first memory and said second memory are two independent memories which are separated from each other.	As detailed above, the first memory in the SMU and the second memory in the caches are independent memories that are separated from each other.

Exhibit B.4: Preliminary Infringement Contention Claim Chart for U.S. Patent 6,895,519

Accused Products: AMD Family 17h Products

These preliminary infringement contentions were prepared without the benefit of the Court’s claim construction or the parties’ exchange of constructions. As of the date of these contentions, AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court’s constructions or to account for new information that becomes available.

	<u>Limitation</u>	<u>Contention</u>
1p	A system LSI having a plurality of ordinary operation modes and a plurality of special modes in response to clock frequencies supplied to a central processing unit, comprising:	<p>To the extent that the preamble is limiting, Aquila contends that it is met.</p> <p>For example, each product in the 17h Accused Product Family (“Accused Product”) is a system LSI.</p> <p>The Accused Product has a plurality of ordinary operation modes, for example the Core P-states. See e.g., AMD Ryzen Master Overclocking Guide (“OC Guide”), p.11:</p> <ol style="list-style-type: none"> 1. The frequency of processor core clock is determined by a combination of the software-requested p-state and then adjusted by a combination of numerous power and performance optimizing features to attain any of number of fine grain p-states around that software-requested p-state. <p>See also OC Guide, p.13:</p> <ol style="list-style-type: none"> 3) CPU low power c-states (CC1, CC6, and PC6) and software visible p-states (P1 and P2) remain operational and may be requested by software so that power savings can be achieved. <p>Documentation from other AMD products provide exemplary guidance on the AMD’s implementation of P-states and C-states. See, e.g., BIOS and Kernel Developer’s Guide for AMD Family 16h Models 00h-0Fh Processors (“16h BKDG”), §2.5.3.1:</p>

<u>Limitation</u>	<u>Contention</u>																																								
	<p>2.5.3.1 Core P-states</p> <p>Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states (P0 through P7), specified in <code>MSRC001_00[6B:64]</code>. Out of cold reset, the voltage and frequency of the compute units is specified by <code>MSRC001_0071[StartupPstate]</code>.</p> <p>16h BKDG, Table 9: Table 9: Software P-state Naming</p> <table border="1"> <thead> <tr> <th colspan="2" style="text-align: center;">D18F4x15C[NumBoost-States]=1</th> <th colspan="2" style="text-align: center;">D18F4x15C[NumBoost-States]=3</th> </tr> <tr> <th style="text-align: center;">P-state Name</th> <th style="text-align: center;">Corresponding MSR Address</th> <th style="text-align: center;">P-state Name</th> <th style="text-align: center;">Corresponding MSR Address</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Pb0</td> <td style="text-align: center;">MSRC001_0064</td> <td style="text-align: center;">Pb0</td> <td style="text-align: center;">MSRC001_0064</td> </tr> <tr> <td style="text-align: center;">P0</td> <td style="text-align: center;">MSRC001_0065</td> <td style="text-align: center;">Pb1</td> <td style="text-align: center;">MSRC001_0065</td> </tr> <tr> <td style="text-align: center;">P1</td> <td style="text-align: center;">MSRC001_0066</td> <td style="text-align: center;">Pb2</td> <td style="text-align: center;">MSRC001_0066</td> </tr> <tr> <td style="text-align: center;">P2</td> <td style="text-align: center;">MSRC001_0067</td> <td style="text-align: center;">P0</td> <td style="text-align: center;">MSRC001_0067</td> </tr> <tr> <td style="text-align: center;">P3</td> <td style="text-align: center;">MSRC001_0068</td> <td style="text-align: center;">P1</td> <td style="text-align: center;">MSRC001_0068</td> </tr> <tr> <td style="text-align: center;">P4</td> <td style="text-align: center;">MSRC001_0069</td> <td style="text-align: center;">P2</td> <td style="text-align: center;">MSRC001_0069</td> </tr> <tr> <td style="text-align: center;">P5</td> <td style="text-align: center;">MSRC001_006A</td> <td style="text-align: center;">P3</td> <td style="text-align: center;">MSRC001_006A</td> </tr> <tr> <td style="text-align: center;">P6</td> <td style="text-align: center;">MSRC001_006B</td> <td style="text-align: center;">P4</td> <td style="text-align: center;">MSRC001_006B</td> </tr> </tbody> </table> <p>All sections and register definitions use software P-state numbering unless otherwise specified.</p> <p>The Accused Product Family has a plurality of special modes, for example, the Core C-states or deep sleep modes such as ACPI S3 or connected standby S0i3. <i>See</i> OC Guide, p.13:</p>	D18F4x15C[NumBoost-States]=1		D18F4x15C[NumBoost-States]=3		P-state Name	Corresponding MSR Address	P-state Name	Corresponding MSR Address	Pb0	MSRC001_0064	Pb0	MSRC001_0064	P0	MSRC001_0065	Pb1	MSRC001_0065	P1	MSRC001_0066	Pb2	MSRC001_0066	P2	MSRC001_0067	P0	MSRC001_0067	P3	MSRC001_0068	P1	MSRC001_0068	P4	MSRC001_0069	P2	MSRC001_0069	P5	MSRC001_006A	P3	MSRC001_006A	P6	MSRC001_006B	P4	MSRC001_006B
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P-state Name	Corresponding MSR Address	P-state Name	Corresponding MSR Address																																						
Pb0	MSRC001_0064	Pb0	MSRC001_0064																																						
P0	MSRC001_0065	Pb1	MSRC001_0065																																						
P1	MSRC001_0066	Pb2	MSRC001_0066																																						
P2	MSRC001_0067	P0	MSRC001_0067																																						
P3	MSRC001_0068	P1	MSRC001_0068																																						
P4	MSRC001_0069	P2	MSRC001_0069																																						
P5	MSRC001_006A	P3	MSRC001_006A																																						
P6	MSRC001_006B	P4	MSRC001_006B																																						

	<u>Limitation</u>	<u>Contention</u>
		<p>3) CPU low power c-states (CC1, CC6, and PC6) and software visible p-states (P1 and P2) remain operational and may be requested by software so that power savings can be achieved.</p> <p>See also OC guide, p.11:</p> <p>4. Software requested p-state or halt states adjust the level of power to which those internal control mechanisms manage. For example, when software executes a HALT instruction on a processor core, that core will enter the C1 reduced-power state. If that core does not receive an interrupt to resume execution, it will progress to increasingly-lower power states until finally saving the state of the core and being powered off.</p> <p>See also 16h BKDG, §§ 2.5.3.2, 2.5.3.2.1, 2.5:</p>

	<u>Limitation</u>	<u>Contention</u>
		<p>2.5.3.2 Core C-states</p> <p>C-states are processor power states. C0 is the operational state in which instructions are executed. All other C-states are low-power states in which instructions are not executed. When coming out of warm and cold reset, the processor is transitioned to the C0 state.</p> <p>2.5.3.2.1 C-state Names and Numbers</p> <p>C-states are often referred to by an alphanumeric naming convention, C1, C2, C3, etc. The mapping between ACPI defined C-states and AMD specified C-states is not direct. AMD specified C-states are referred to as IO-based C-states. Up to three IO-based C-states are supported, IO-based C-state 0, 1, and 2. The IO-based C-state index corresponds to the offset added to MSRC001_0073[CstateAddr] to initiate a C-state request. See 2.5.3.2.2 [C-state Request Interface]. The actions taken by the processor when entering a low-power C-state are configured by software. See 2.5.3.2.3 [C-state Actions] for information about AMD specific actions.</p>

<u>Limitation</u>	<u>Contention</u>																																																																		
	<p>2.5 Power Management</p> <p>The processor supports many power management features in a variety of systems. Table 8 provides a summary of ACPI states and power management features and indicates whether they are supported.</p> <p>Table 8: Power Management Support</p> <table border="1"> <thead> <tr> <th>ACPI/Power Management State</th> <th>Supported</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>G0/S0/C0: Working</td> <td>Yes</td> <td></td> </tr> <tr> <td>G0/S0/C0: Core P-state transitions</td> <td>Yes</td> <td>2.5.3.1 [Core P-states]</td> </tr> <tr> <td>G0/S0/C0: NB P-state transitions</td> <td>Yes</td> <td>2.5.4.1 [NB P-states]</td> </tr> <tr> <td>G0/S0/C0: Hardware thermal control (HTC)</td> <td>Yes</td> <td>2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)]</td> </tr> <tr> <td>G0/S0/Per-core IO-based C-states</td> <td>Yes</td> <td>2.5.3.2 [Core C-states] and 2.5.1.3.2 [Low Power Voltages]</td> </tr> <tr> <td>G0/S0/C1: Halt</td> <td>Yes</td> <td></td> </tr> <tr> <td>G0/S0/CC6: Per-core Power gating</td> <td>Yes</td> <td>2.5.3.2 [Core C-states]</td> </tr> <tr> <td>G0/S0: CPC-L2 power gating</td> <td>Yes</td> <td>2.5.3.2 [Core C-states]</td> </tr> <tr> <td>G0/S0/PC6: 0V support (VDD power plane).</td> <td>Yes</td> <td>2.5.3.2 [Core C-states] and 2.5.1.3.2 [Low Power Voltages]</td> </tr> <tr> <td>G0/S0/Cx: Cache flushing support</td> <td>Yes</td> <td>2.5.3.2.3.1 [C-state Probes and Cache Flushing]</td> </tr> <tr> <td>G0/S0: Northbridge C-states (DRAM self-refresh, NB clock-gating)</td> <td>Yes</td> <td>2.5.4.2 [NB C-states]</td> </tr> <tr> <td>G1/S1: Stand By (Powered On Suspend)</td> <td>No</td> <td></td> </tr> <tr> <td>G1/S3: Stand By (Suspend to RAM)</td> <td>Yes</td> <td>2.5.8.1 [S-states]</td> </tr> <tr> <td>G1/S4: Hibernate (Suspend to Disk)</td> <td>Yes</td> <td></td> </tr> <tr> <td>G1/S5: Shut Down (Soft Off)</td> <td>Yes</td> <td></td> </tr> <tr> <td>G3 Mechanical Off</td> <td>Yes</td> <td></td> </tr> <tr> <td>Parallel VID Interface</td> <td>No</td> <td rowspan="4">2.5.1 [Processor Power Planes And Voltage Control]</td> </tr> <tr> <td>Serial VID Interface 1</td> <td>No</td> </tr> <tr> <td>Serial VID Interface 2</td> <td>Yes</td> </tr> <tr> <td>Single-plane systems</td> <td>No</td> </tr> <tr> <td>Number of voltage planes</td> <td>2</td> <td>2.5.1 [Processor Power Planes And Voltage Control]</td> </tr> <tr> <td>APM: Application Power Management</td> <td>Yes</td> <td>2.5.9 [Application Power Management (APM)]</td> </tr> </tbody> </table>	ACPI/Power Management State	Supported	Description	G0/S0/C0: Working	Yes		G0/S0/C0: Core P-state transitions	Yes	2.5.3.1 [Core P-states]	G0/S0/C0: NB P-state transitions	Yes	2.5.4.1 [NB P-states]	G0/S0/C0: Hardware thermal control (HTC)	Yes	2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)]	G0/S0/Per-core IO-based C-states	Yes	2.5.3.2 [Core C-states] and 2.5.1.3.2 [Low Power Voltages]	G0/S0/C1: Halt	Yes		G0/S0/CC6: Per-core Power gating	Yes	2.5.3.2 [Core C-states]	G0/S0: CPC-L2 power gating	Yes	2.5.3.2 [Core C-states]	G0/S0/PC6: 0V support (VDD power plane).	Yes	2.5.3.2 [Core C-states] and 2.5.1.3.2 [Low Power Voltages]	G0/S0/Cx: Cache flushing support	Yes	2.5.3.2.3.1 [C-state Probes and Cache Flushing]	G0/S0: Northbridge C-states (DRAM self-refresh, NB clock-gating)	Yes	2.5.4.2 [NB C-states]	G1/S1: Stand By (Powered On Suspend)	No		G1/S3: Stand By (Suspend to RAM)	Yes	2.5.8.1 [S-states]	G1/S4: Hibernate (Suspend to Disk)	Yes		G1/S5: Shut Down (Soft Off)	Yes		G3 Mechanical Off	Yes		Parallel VID Interface	No	2.5.1 [Processor Power Planes And Voltage Control]	Serial VID Interface 1	No	Serial VID Interface 2	Yes	Single-plane systems	No	Number of voltage planes	2	2.5.1 [Processor Power Planes And Voltage Control]	APM: Application Power Management	Yes	2.5.9 [Application Power Management (APM)]
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<u>Limitation</u>	<u>Contention</u>		
	<p>Furthermore, the Core P-states and Core C-states are in response to clock frequencies supplied to a central processing unit. For example, the core P-states are “characterized” by “core frequency;” core P-state changes are further requested by software. <i>See</i> OC Guide p.13:</p> <p>a. The P1 and P2 p-state tables may also be modified to adjust the voltage and frequency of the CPU when running in software-requested, reduced-performance states. These may also be left at stock values.</p> <p>See also OSRR for AMD Family 17h processors, Models 00h-2Fh, p.130: MSRC001_006[4...B] [P-state [7:0]] (Core::X86::Msr::PStateDef)</p> <table border="1" data-bbox="749 768 2198 950"> <tr> <td>Read-write. Reset: X000_0000_XXXX_XXXXh.</td> </tr> <tr> <td>Each of these registers specify the frequency and voltage associated with each of the core P-states. The CpuVid field in these registers is required to be programmed to the same value in all cores of a processor, but are allowed to be different between processors in a multi-processor system. All other fields in these registers are required to be programmed to the same value in each core of the coherent fabric.</td> </tr> </table> <p><i>See e.g.</i>, 16h BKDG, § 2.5.3.1, 2.5.3.1.2:</p> <p>2.5.3.1 Core P-states</p> <p>Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states (P0 through P7), specified in MSRC001_00[6B:64]. Out of cold reset, the voltage and frequency of the compute units is specified by MSRC001_0071[StartupPstate].</p>	Read-write. Reset: X000_0000_XXXX_XXXXh.	Each of these registers specify the frequency and voltage associated with each of the core P-states. The CpuVid field in these registers is required to be programmed to the same value in all cores of a processor, but are allowed to be different between processors in a multi-processor system. All other fields in these registers are required to be programmed to the same value in each core of the coherent fabric.
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<u>Limitation</u>	<u>Contention</u>
	<p>Support for dynamic core P-state changes is indicated by more than one enabled selection in MSRC001_00[6B:64][PstateEn]. At least one enabled P-state (P0) is specified for all processors.</p> <p>Software requests core P-state changes for each core independently using the hardware P-state control mechanism (a.k.a. fire and forget). Support for hardware P-state control is indicated by CPUID Fn8000_0007_EDX[Hwpstate]=1b. Software may not request any P-state transitions using the hardware P-state control mechanism until the P-state initialization requirements defined in 2.5.3.1.6 [BIOS Requirements for Core P-state Initialization and Transitions] are complete.</p> <p>The processor supports independently-controllable frequency planes for each compute unit and the NB; and independently-controllable voltage planes. See 2.5.1 [Processor Power Planes And Voltage Control] for voltage plane definitions.</p> <p>The following terms may be applied to each of these planes:</p> <ul style="list-style-type: none"> • FID: frequency ID. Specifies the PLL frequency multiplier, relative to the reference clock, for a given domain. • DID: divisor ID. Specifies the post-PLL power-of-two divisor that can be used to reduce the operating frequency. • COF: current operating frequency. Specifies the operating frequency as a function of the FID and DID. Refer to CoreCOF for the CPU COF formula and NBCOF for the NB COF formula. • VID: voltage ID. Specifies the voltage level for a given domain. Refer to 2.5.1.2.1 [MinVid and MaxVid Check] for encodings. <p>All FID and DID parameters for software P-states must be programmed to equivalent values for all cores and NBs in the coherent fabric. See 2.5.3.1.1.1 [Software P-state Numbering]. Refer to MSRC001_00[6B:64] and D18F5x16[C:0] for further details on programming requirements.</p>

<u>Limitation</u>	<u>Contention</u>
	<p>2.5.3.1.2 Core P-state Control</p> <p>Core P-states are dynamically controlled by software and are exposed through ACPI objects (refer to 2.5.3.1.8.3 [ACPI Processor P-state Objects]). Software requests a core P-state change by writing a 3 bit index corresponding to the desired P-state number to <code>MSRC001_0062[PstateCmd]</code> of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's <code>MSRC001_0062[PstateCmd]</code>.</p> <p>Boosted P-states may not be directly requested by software. Whenever software requests the P0 state on a processor that supports APM (i.e. writes 000b to <code>MSRC001_0062[PstateCmd]</code>), hardware dynamically places the core into the highest-performance P-state possible as determined by APM. See 2.5.9 [Application Power Management (APM)].</p> <p>Hardware sequences the frequency and voltage changes necessary to complete a P-state transition as specified by 2.5.3.1.5 [Core P-state Transition Behavior] with no additional software interaction required. Hardware also coordinates frequency and voltage changes when differing P-state requests are made on cores that share a frequency or voltage plane. See 2.5.2 [Frequency and Voltage Domain Dependencies] for details about hardware coordination.</p> <p>Similarly, C-states are requested by software, for example when executing a HALT instruction, and also dependent upon clock frequency (“reduced power” or “lower power” state). See OC Guide, p.11:</p> <p>4. Software requested p-state or halt states adjust the level of power to which those internal control mechanisms manage. For example, when software executes a HALT instruction on a processor core, that core will enter the C1 reduced-power state. If that core does not receive an interrupt to resume execution, it will progress to increasingly-lower power states until finally saving the state of the core and being powered off.</p>

<u>Limitation</u>	<u>Contention</u>
	<p data-bbox="736 269 1736 305"><i>See also</i> 16h BKDG §§ 2.5.3.2.3.2, 2.5.3.2.3.3, 2.5.3.2.3.2; p.320-321:</p> <p data-bbox="760 331 1271 367">2.5.3.2.3.2 Core C1 (CC1) State</p> <p data-bbox="760 402 1892 477">When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct].</p> <p data-bbox="760 519 1271 555">2.5.3.2.3.3 Core C6 (CC6) State</p> <p data-bbox="760 591 2214 776">A core can gate off power to its internal logic when it enters any non-C0 state. This power gated state is known as CC6. In order to enter CC6, hardware first enters CC1 then checks D18F4x118/D18F4x11C[PwrGateEnCstAct]. Power gating reduces the amount of power consumed by the core. VDD voltage is not reduced when a core is in CC6. The following sequence occurs when a core enters the CC6 state:</p> <ol data-bbox="760 824 2150 1052" style="list-style-type: none"> 1. If MSRC001_0071[CurPstate] < D18F3xA8[PopDownPstate], transition the core P-state to D18F3xA8[PopDownPstate]. 2. Internal core state is saved to L1 cache . 3. L1 cache is flushed to L2 cache. See 2.5.3.2.3.1 [C-state Probes and Cache Flushing]. 4. Power is removed from the core and the core PLL/voltage regulator is powered down as specified by D18F5x128[CC6PwrDwnRegEn].

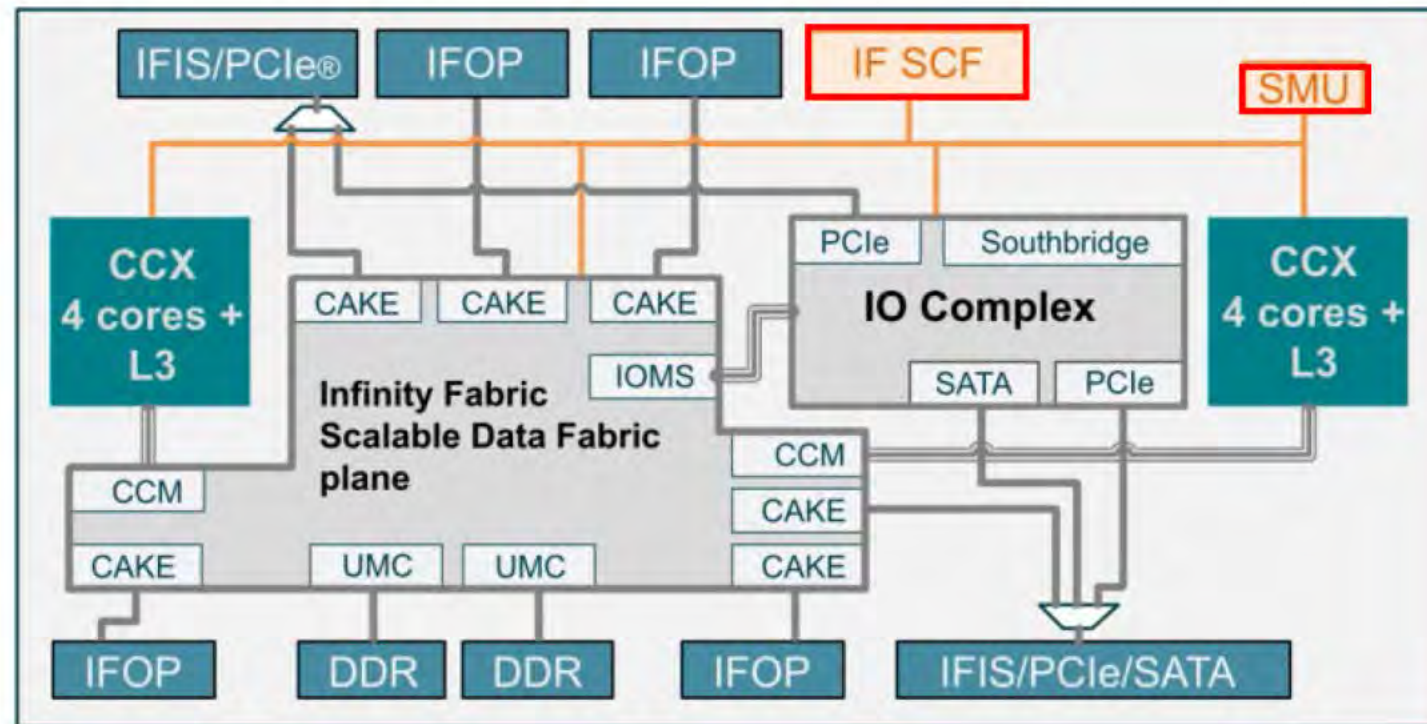
<u>Limitation</u>	<u>Contention</u>																						
	<p>D18F4x11[C:8] C-state Control</p> <p>D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states].</p> <ul style="list-style-type: none"> • D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]. • D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1. • D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2. <p>D18F4x118 C-state Control 1</p> <table border="1" data-bbox="758 735 2214 1333"> <tr> <td data-bbox="758 735 862 776">7:5</td> <td data-bbox="868 735 2214 1333"> <p>ClkDivisorCstAct0: clock divisor. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or:</p> <ul style="list-style-type: none"> • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. <p>If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.</p> <table border="1" data-bbox="868 1089 1704 1284"> <thead> <tr> <th><u>Bits</u></th> <th><u>Description</u></th> <th><u>Bits</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>/1</td> <td>100b</td> <td>/16</td> </tr> <tr> <td>001b</td> <td>/2</td> <td>101b</td> <td>/128</td> </tr> <tr> <td>010b</td> <td>/4</td> <td>110b</td> <td>/512</td> </tr> <tr> <td>011b</td> <td>/8</td> <td>111b</td> <td>Turn off clocks.</td> </tr> </tbody> </table> <p>See CacheFlushTmrSelCstAct0.</p> </td> </tr> </table>	7:5	<p>ClkDivisorCstAct0: clock divisor. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or:</p> <ul style="list-style-type: none"> • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. <p>If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.</p> <table border="1" data-bbox="868 1089 1704 1284"> <thead> <tr> <th><u>Bits</u></th> <th><u>Description</u></th> <th><u>Bits</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>/1</td> <td>100b</td> <td>/16</td> </tr> <tr> <td>001b</td> <td>/2</td> <td>101b</td> <td>/128</td> </tr> <tr> <td>010b</td> <td>/4</td> <td>110b</td> <td>/512</td> </tr> <tr> <td>011b</td> <td>/8</td> <td>111b</td> <td>Turn off clocks.</td> </tr> </tbody> </table> <p>See CacheFlushTmrSelCstAct0.</p>	<u>Bits</u>	<u>Description</u>	<u>Bits</u>	<u>Description</u>	000b	/1	100b	/16	001b	/2	101b	/128	010b	/4	110b	/512	011b	/8	111b	Turn off clocks.
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	<u>Limitation</u>	<u>Contention</u>
1a	a first memory that stores a clock control library for controlling a clock frequency transition between said ordinary operation modes;	<p>The Accused Products include a first memory that stores a clock control library. For example, the SMU and/or Scalable Control Fabric and Scalable Data Fabric contains memory that stores the firmware and configuration space registers, including a clock control library. The clock control library controls clock frequency transition between the P-states.</p> <p>PPR for AMD Family 17h Models 00h-0Fh, pp. 26-27:</p> <ul style="list-style-type: none"> • 16MB L3 total • Scalable Data Fabric. This provides the data path that connects the compute complexes, the I/O interfaces, and the memory interfaces to each other. <ul style="list-style-type: none"> • Handles request, response, and data traffic • Handles probe traffic to facilitate coherency, including a probe filter supporting up to 512GB per DRAM channel • Handles interrupt request routing (APIC) • PSP and SMU <ul style="list-style-type: none"> • MP0 (PSP) and MP1 (SMU) microcontrollers <ul style="list-style-type: none"> • This document refers to the AMD Secure Processor technology as Platform Security Processor (PSP). • Thermal monitoring • Fuses • Clock control

Limitation

Contention

Chip Architecture



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2.4: "Zeppelin": an SoC for Multi-chip Architectures

5 of 29

Source: Beck et al., "Zeppelin": an SoC for Multi-chip Architectures, p. 5.

<u>Limitation</u>	<u>Contention</u>
	<p data-bbox="790 293 1763 354">Hierarchical Power Management</p> <ul data-bbox="790 440 1688 1040" style="list-style-type: none"> <li data-bbox="790 440 1688 548">▪ System Management Unit (SMU) uses IF Scalable Control Fabric (SCF) plane <li data-bbox="790 565 1688 673">▪ SCF: single-lane IFIS SerDes link for chip-to-chip or socket-to-socket <li data-bbox="790 690 1688 1040">▪ SMU calculation hierarchy for voltage level control, C-State Boost, thermal management, electrical design current management <ul style="list-style-type: none"> <li data-bbox="854 938 1360 982">– Local chip SMU fast loop <li data-bbox="854 998 1440 1040">– Master chip SMU slower loop <div data-bbox="1768 354 2290 1117" style="text-align: center;"> <p>The diagram illustrates a hierarchical power management architecture across four dies. Die 0 is the Master SMU, while Dies 1, 2, and 3 are NWS (Non-Master Work Stealing) SMUs. They are connected via a central vertical bus labeled 'To other socket'.</p> </div> <p data-bbox="763 1138 1150 1154">© 2018 IEEE International Solid-State Circuits Conference</p> <p data-bbox="1392 1138 1741 1154">2.4: "Zepelin": an SoC for Multi-chip Architectures</p> <p data-bbox="2333 1138 2386 1154">12 of 29</p> <p data-bbox="736 1179 1016 1211">Source: Beck, p.12.</p>

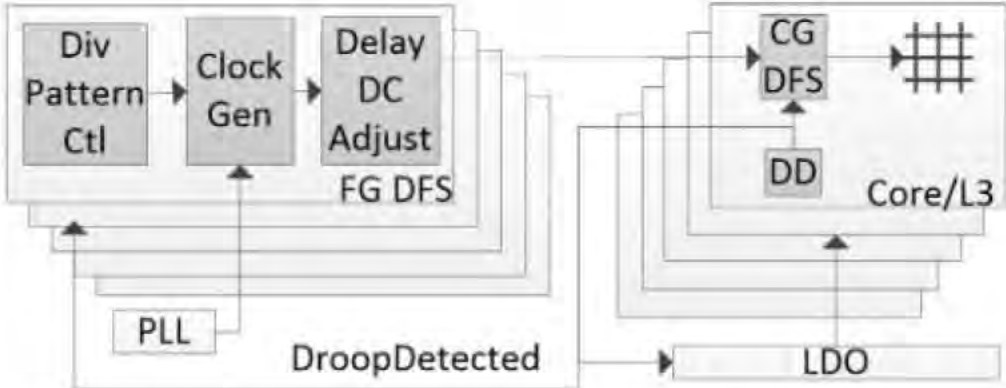
<u>Limitation</u>	<u>Contention</u>
	<p>Source: Bouvier et al., Delivering A New Level Of Visual Performance In An SOC, p.3</p> <p>See e.g., 16h BKDG, 29:</p>

Exhibit B.4

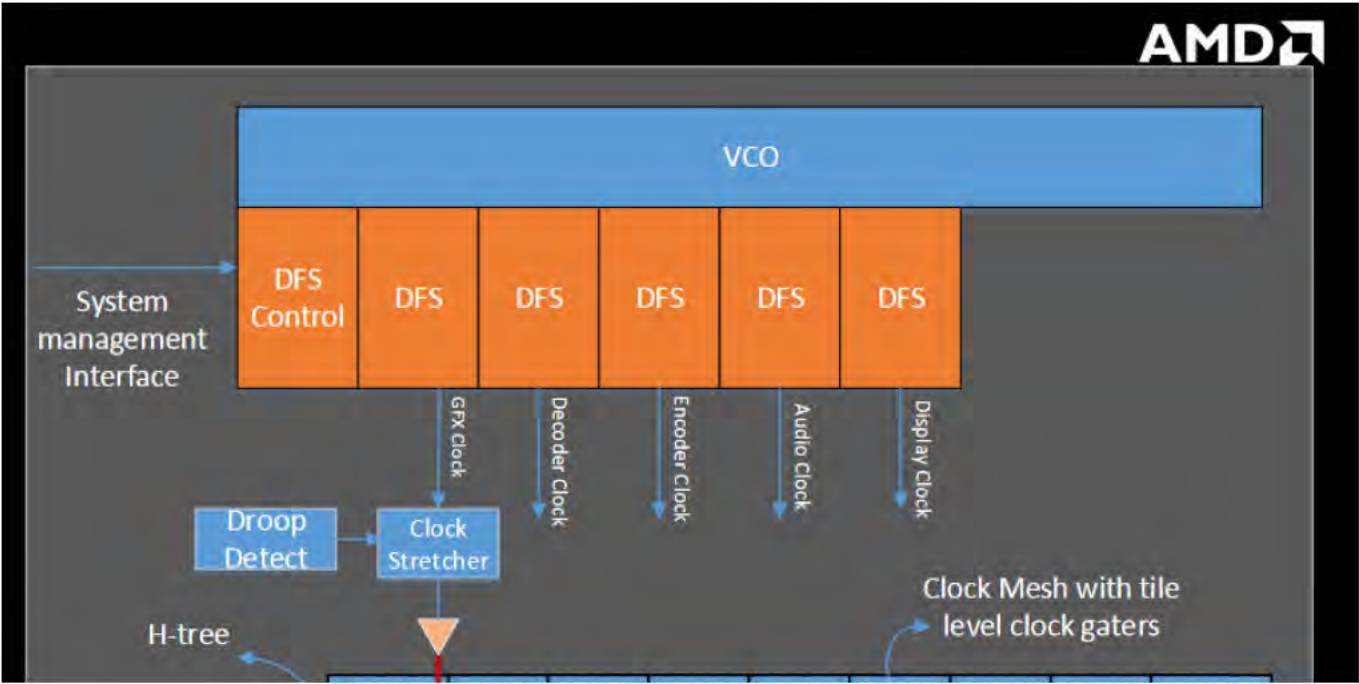
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		<ul style="list-style-type: none"> • Northbridge: <ul style="list-style-type: none"> • One communication packet routing block referred to as the northbridge (NB). The NB routes transactions between the cores, the link, and the DRAM interfaces. It includes the configuration register space for the device. <p>16h BKDG, section 2.12: 2.12 System Management Unit (SMU)</p> <p>The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. The SMU contains a microcontroller to assist with many of these tasks.</p> <p>See also 16h BKDG, Table 10: Table 10: Software P-state Control</p> <table border="1" data-bbox="736 833 1833 1240"> <thead> <tr> <th colspan="3">D18F4x15C[NumBoostStates]=1</th> <th colspan="3">D18F4x15C[NumBoostStates]=3</th> </tr> <tr> <th>P-state Name</th> <th>Index Used for Requests/Status</th> <th>Corresponding MSR Address</th> <th>P-state Name</th> <th>Index Used for Requests/Status</th> <th>Corresponding MSR Address</th> </tr> </thead> <tbody> <tr> <td>Pb0</td> <td>n/a</td> <td>MSRC001_0064</td> <td>Pb0</td> <td>n/a</td> <td>MSRC001_0064</td> </tr> <tr> <td>P0</td> <td>0</td> <td>MSRC001_0065</td> <td>Pb1</td> <td>n/a</td> <td>MSRC001_0065</td> </tr> <tr> <td>P1</td> <td>1</td> <td>MSRC001_0066</td> <td>Pb2</td> <td>n/a</td> <td>MSRC001_0066</td> </tr> <tr> <td>P2</td> <td>2</td> <td>MSRC001_0067</td> <td>P0</td> <td>0</td> <td>MSRC001_0067</td> </tr> <tr> <td>P3</td> <td>3</td> <td>MSRC001_0068</td> <td>P1</td> <td>1</td> <td>MSRC001_0068</td> </tr> <tr> <td>P4</td> <td>4</td> <td>MSRC001_0069</td> <td>P2</td> <td>2</td> <td>MSRC001_0069</td> </tr> <tr> <td>P5</td> <td>5</td> <td>MSRC001_006A</td> <td>P3</td> <td>3</td> <td>MSRC001_006A</td> </tr> <tr> <td>P6</td> <td>6</td> <td>MSRC001_006B</td> <td>P4</td> <td>4</td> <td>MSRC001_006B</td> </tr> </tbody> </table>	D18F4x15C[NumBoostStates]=1			D18F4x15C[NumBoostStates]=3			P-state Name	Index Used for Requests/Status	Corresponding MSR Address	P-state Name	Index Used for Requests/Status	Corresponding MSR Address	Pb0	n/a	MSRC001_0064	Pb0	n/a	MSRC001_0064	P0	0	MSRC001_0065	Pb1	n/a	MSRC001_0065	P1	1	MSRC001_0066	Pb2	n/a	MSRC001_0066	P2	2	MSRC001_0067	P0	0	MSRC001_0067	P3	3	MSRC001_0068	P1	1	MSRC001_0068	P4	4	MSRC001_0069	P2	2	MSRC001_0069	P5	5	MSRC001_006A	P3	3	MSRC001_006A	P6	6	MSRC001_006B	P4	4	MSRC001_006B
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1b	a system control circuit which has a register, wherein	The Accused Product has a system control circuit, for example, the System Management Unit and/or the System Management Controller, that has a register. See PPR, p.27:																																																												

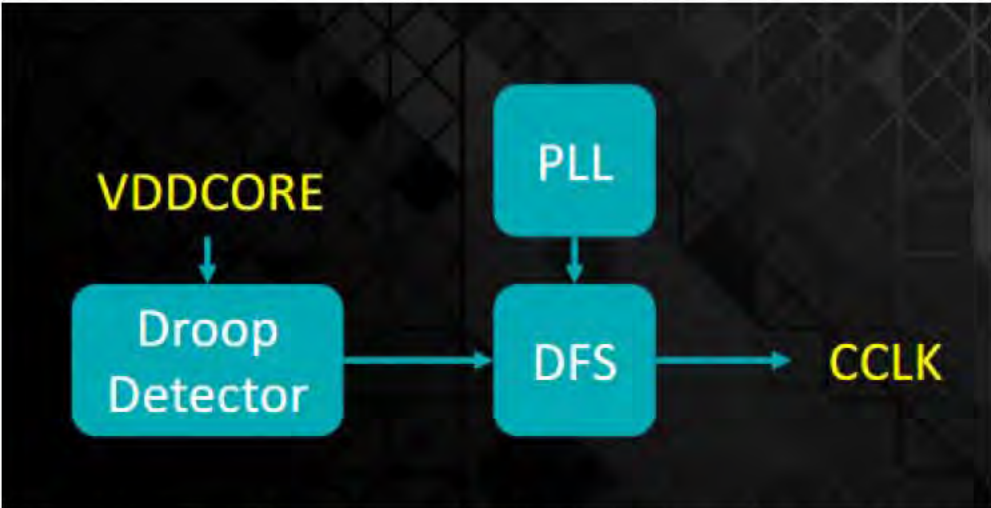
<u>Limitation</u>	<u>Contention</u>
<p>said system control circuit carries out the clock frequency transition between said ordinary operation modes and said special modes in response to a change of a value in said register, and also carries out the clock frequency transition among said ordinary operation modes in response to said clock control library;</p>	<ul style="list-style-type: none"> • PSP and SMU <ul style="list-style-type: none"> • MP0 (PSP) and MP1 (SMU) microcontrollers <ul style="list-style-type: none"> • This document refers to the AMD Secure Processor technology as Platform Security Processor (PSP). • Thermal monitoring • Fuses • Clock control <p>See e.g., 16h BKDG:</p> <ul style="list-style-type: none"> • Northbridge: <ul style="list-style-type: none"> • One communication packet routing block referred to as the northbridge (NB). The NB routes transactions between the cores, the link, and the DRAM interfaces. It includes the configuration register space for the device. <p>16h BKDG, section 2.12: 2.12 System Management Unit (SMU)</p> <p>The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. The SMU contains a microcontroller to assist with many of these tasks.</p> <p>See also BKDG for 14h Family 00h-0Fh Processors, section 2.12:</p>

	<u>Limitation</u>	<u>Contention</u>
		<p>2.12 System Management Unit (SMU)</p> <p>The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details.</p> <p>2.12.1 Microcontroller</p> <p>The SMU contains a microcontroller with a 16k ROM and a 16k RAM.</p> <p>The NB/SMU controls the clock frequency transitions between the core P-states. See e.g., SATHE et al.: RESONANT-CLOCK DESIGN FOR A POWER-EFFICIENT, HIGH-VOLUME X86-64 MICROPROCESSOR, p.144</p> <p>tion of the configuration programming interface. On receiving notification from the NB of a PState transition, the core implements a PState entry sequence which transitions the core into a clock-gated state. A program sequencer then accesses a</p>
1c	a clock generation circuit that receives a plurality of standard clocks, wherein said clock generation circuit generates a clock supplied to said central processing unit according to control by said system control circuit; and	The Accused Products include a digital frequency synthesizer clock generation circuit, including the core PLL, clock multipliers and dividers, and/or the digital frequency synthesizer. The DFS receives a plurality of standard clocks, for example, different phases of the PLL clock or reference clock, and outputs the core clock such as CCLK to the CPU.

<u>Limitation</u>	<u>Contention</u>
	 <p>The diagram illustrates the clock stretch mechanism. On the left, a PLL feeds into a Div Pattern Ctl, which then feeds into a Clock Gen. The Clock Gen outputs to a Delay DC Adjust block, which is part of the FG DFS (Fine Grain Dynamic Frequency Scaling) block. A DroopDetected signal is fed into the Delay DC Adjust block. The Delay DC Adjust block outputs to a CG DFS (Coarse Grain Dynamic Frequency Scaling) block, which is part of the Core/L3 block. The CG DFS block outputs to a DD (Dynamic Duty) block, which then feeds into a Core/L3 block. The Core/L3 block outputs to a LDO (Low Dropout Regulator) block. The LDO block outputs to a Core/L3 block. The Core/L3 block also outputs to a grid symbol.</p> <p>Fig. 15. Coarse grain (CG) and fine grain (FG) clock stretch.</p> <p>Source: Singh et al.: Energy-Efficient High-Performance x86 Core, Fig. 15:</p> <p>See also PPR at p.138-139:</p> <p>MSRC001_0064 [P-state [7:0]] (PStateDef)</p> <p>Read-write. Reset: X000 0000 XXXX XXXXh.</p> <p>Each of these registers specify the frequency and voltage associated with each of the core P-states. The CpuVid field in these registers is required to be programmed to the same value in all cores of a processor, but are allowed to be different between processors in a multi-processor system. All other fields in these registers are required to be programmed to the same value in each core of the coherent fabric.</p> <p>See 2.1.3 [CPU Power Management].</p> <p>Core::X86::Msr::PStateDef lthree[1:0] core[3:0] thread[1:0] n[7:0]; MSRC001_006[B:4]</p>

<u>Limitation</u>	<u>Contention</u>
	<div data-bbox="736 269 2440 532" style="border: 1px solid black; padding: 5px;"> <p>13:8 CpuDfsId: core divisor ID. Read-write. Reset: XXXXXXb. Specifies the core frequency divisor; see CpuFid. For values [1Ah:08h], 1/8th integer divide steps supported down to VCO/3.25 (Note, L3/L2 fifo logic related to 4-cycle data heads-up requires core to be 1/3 of L3 frequency or higher). For values [30h:1Ch], 1/4th integer divide steps supported down to VCO/6 (DID[0] should zero if DID[5:0]>1Ah). (Note, core and L3 frequencies below 400MHz are not supported by the architecture). Core supports DID up to 30h, but L3 must be 2Ch (VCO/5.5) or less.</p> </div> <p>The digital frequency synthesizer receives multiple phases of the PLL clock (see above), and generates multiple discrete frequencies according to control by the SMU.</p> <div data-bbox="736 649 1833 1094" style="background-color: black; color: white; padding: 10px;"> <p>▲ Digital frequency synthesizer (DFS) that generates multiple discrete frequencies from a single VCO</p> <ul style="list-style-type: none"> – Root clock gating – Disabling VCO and bypassing with low speed fixed clocks </div>

<u>Limitation</u>	<u>Contention</u>
	 <p>The diagram illustrates the clock management architecture of the AMD Carrizo APU. At the top is a blue VCO (Voltage-Controlled Oscillator) block. Below it is a row of six orange DFS (Dynamic Frequency Scaling) blocks, with the first one labeled 'DFS Control'. A 'System management Interface' is connected to the DFS Control block. Arrows from the DFS blocks lead to various clock outputs: 'GFX Clock', 'Decoder Clock', 'Encoder Clock', 'Audio Clock', and 'Display Clock'. A 'Droop Detect' block is connected to a 'Clock Stretcher' block, which in turn feeds into an 'H-tree' distribution network. The H-tree is connected to a 'Clock Mesh with tile level clock gates' at the bottom of the chip.</p> <p>Source: Krishnan et al., "Energy Efficient Graphics and Multimedia in 28nm Carrizo APU," p.14</p>

<u>Limitation</u>	<u>Contention</u>
	 <p>The diagram illustrates a power management control loop. VDDCORE provides input to a Droop Detector. The Droop Detector outputs to a DFS (Dynamic Frequency Scaling) block. A PLL (Phase-Locked Loop) also provides input to the DFS block. The DFS block outputs the CCLK (Core Clock).</p> <pre> graph TD VDDCORE[VDDCORE] --> DD[Droop Detector] DD --> DFS[DFS] PLL[PLL] --> DFS DFS --> CCLK[CCLK] </pre> <p><i>Source: Integrated Power Conversion Strategies Across Laptop, Server, and Graphics Products, 2016 Power SOC Conference, p.4</i></p> <p>See also, e.g., Singh et al., Jaguar: A Next-Generation Low-Power x86-64 Core, pp. 25-26:</p>

Limitation

Contention

3.4: Jaguar: A Next-Generation Low-Power x86-64 Core

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CU Level Clock Distribution

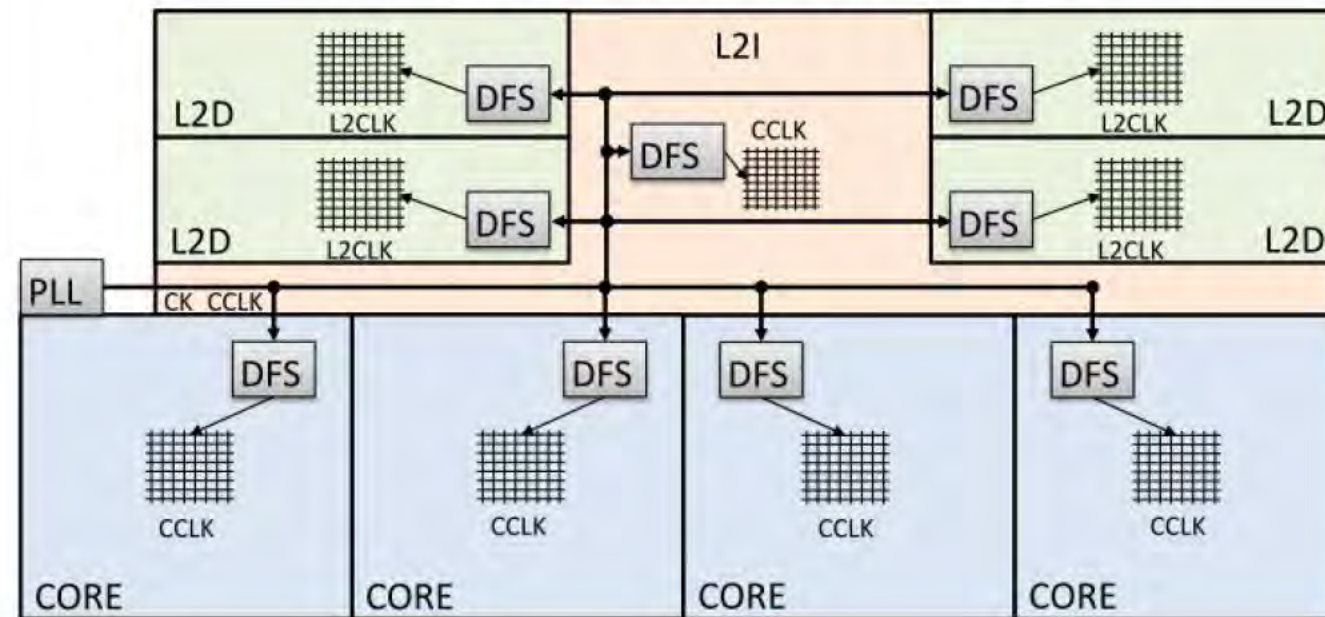
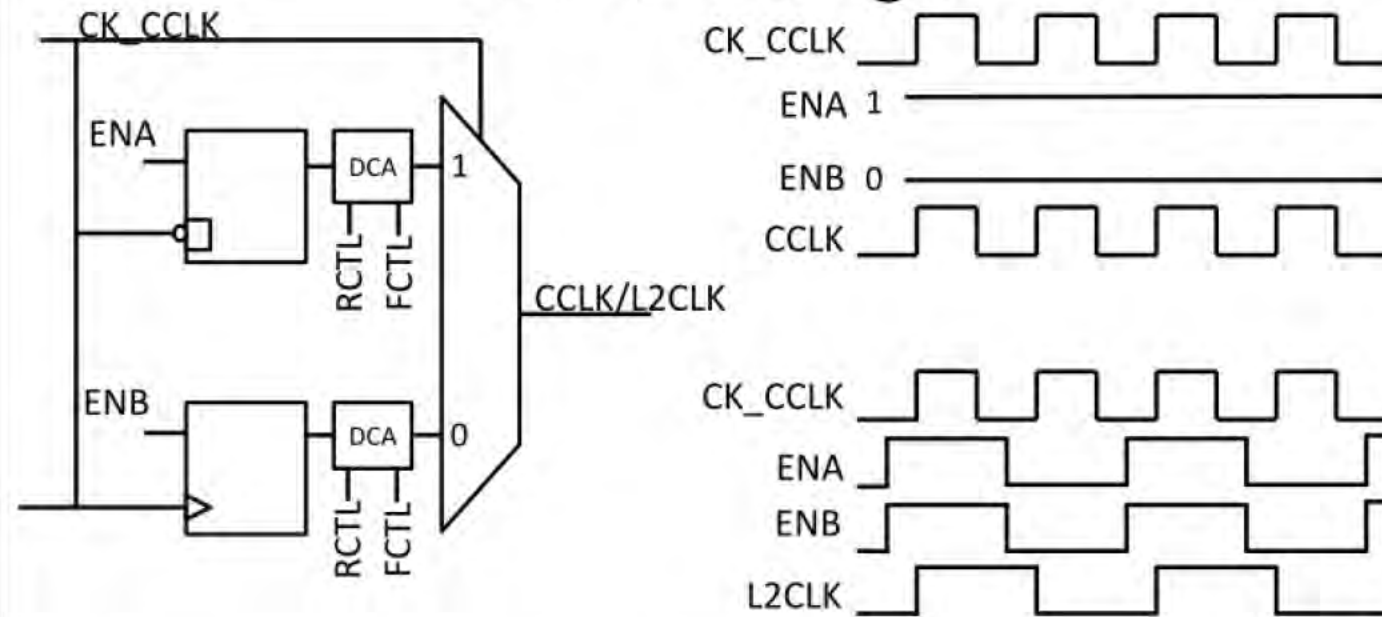


Exhibit B.4

Limitation

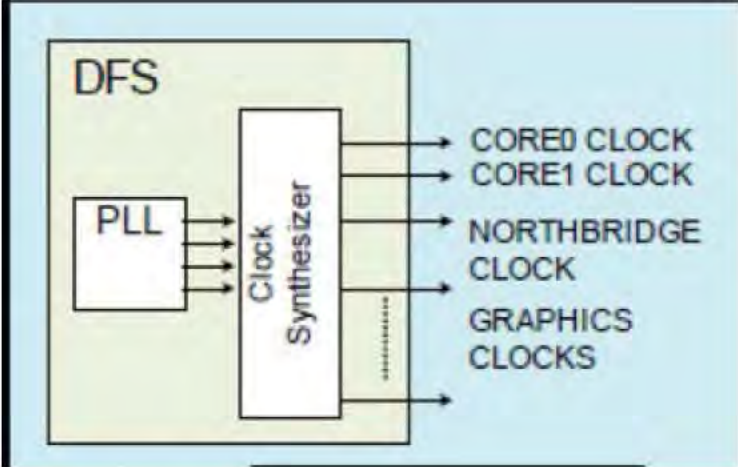
Contention

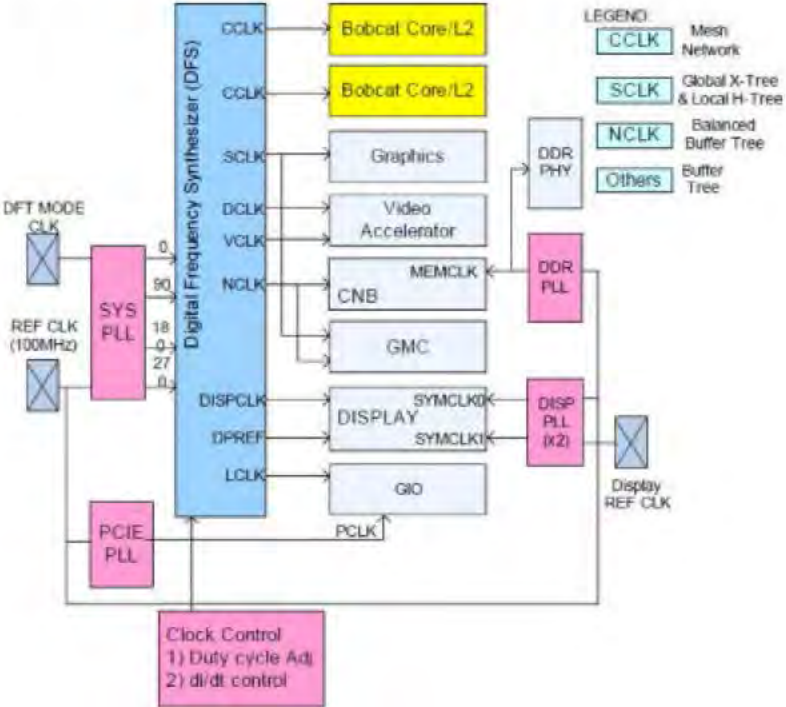
DFS Design

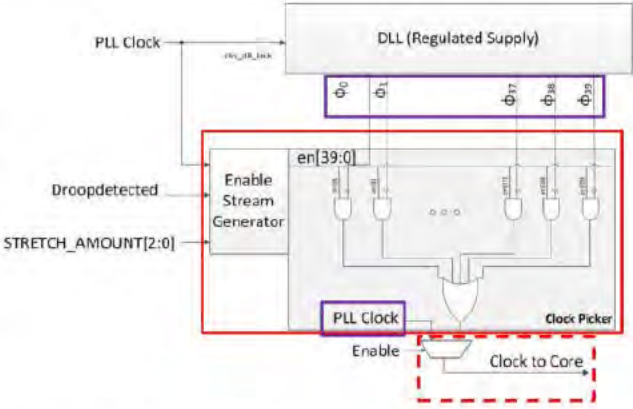


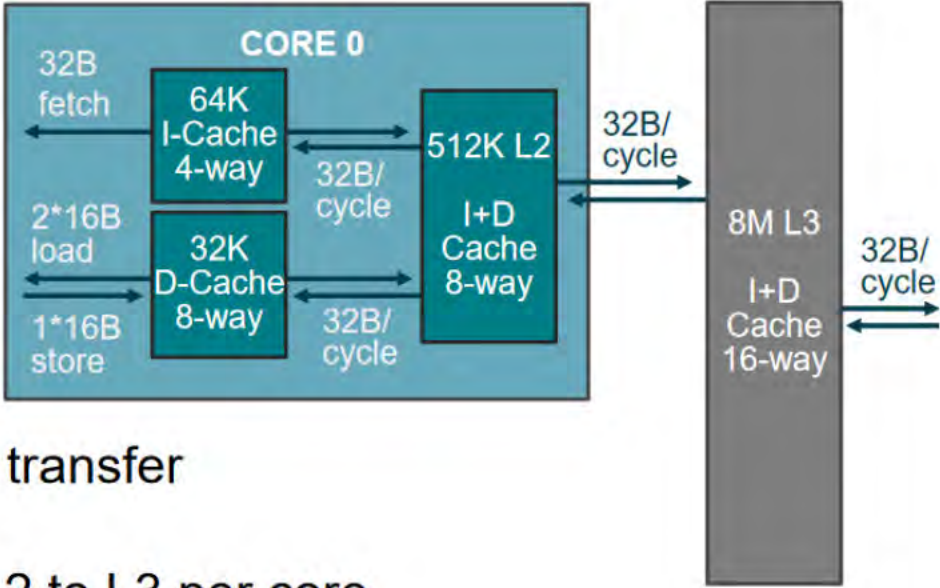
- Clock dividing for various operating modes
- Duty cycle adjuster for independent control of duty cycle within each block

See also:

<u>Limitation</u>	<u>Contention</u>
	 <p>The diagram illustrates the Dynamic Frequency Scaling (DFS) architecture. It features a central 'Clock Synthesizer' block. To its left is a 'PLL' (Phase-Locked Loop) block, which provides input to the synthesizer. The synthesizer outputs several clock signals: 'CORE0 CLOCK', 'CORE1 CLOCK', 'NORTHBRIDGE CLOCK', and 'GRAPHICS CLOCKS'. A vertical ellipsis indicates additional clock outputs. The entire system is contained within a light blue area labeled 'DFS'.</p>

<u>Limitation</u>	<u>Contention</u>
	 <p data-bbox="747 1044 1064 1065">Fig. 11 DFS clock generation</p> <p data-bbox="747 1068 2451 1138">Source: Foley et al., A Low-Power Integrated x86-64 And Graphics Processor For Mobile Computing Devices, Fig. 1., 11; p.224-225.</p> <p data-bbox="747 1179 916 1216">See also e.g.,</p>

	<u>Limitation</u>	<u>Contention</u>
		<p data-bbox="739 354 1128 381"><i>D. Glitch Less Clock Phase Picker</i></p> <p data-bbox="739 394 1424 711">The glitch-less clock picker (Fig. 6) takes the 40 phases (40 total phases generated from the 20 DLL delay elements) and generates a stretched clock (configurable stretch amount) by selecting different phases of the clock. The clock picker always performs a complete loop through all the phases before selecting the 0th phase (pll_clk) to avoid any contraction of the clock period. When the clock stretcher block is disabled (STRETCH_ENABLE = 0), the clock picker simply picks the pll_clk without any insertion delay of the clock stretcher logic.</p> <p data-bbox="739 724 2325 751">Source: WILCOX et al.: STEAMROLLER MODULE AND ADAPTIVE CLOCKING SYSTEM IN 28 nm CMOS, Fig. 6</p> 
1d	<p data-bbox="268 862 698 1198">a second memory that stores an application program, wherein calling of said clock control library and changing of said register value are programmably controlled by said application program to enable user selectable clock frequency transitions,</p>	<p data-bbox="739 862 2405 971">The Accused Products include a second memory, such as the hierarchy of L1, L2 caches that stores an application program, including but not limited to ACPI drivers, power management utilities, APIs provided by AMD, or any software that causes the SMU/SMC firmware to perform P-state transitions.</p>

<u>Limitation</u>	<u>Contention</u>
	<p data-bbox="747 277 1473 342">“Zen” Cache hierarchy</p> <ul data-bbox="747 391 1849 1040" style="list-style-type: none"> <li data-bbox="747 391 1311 496">▪ Fast private L2 cache, 12 cycles <li data-bbox="747 513 1311 618">▪ Fast shared L3 cache, 35 cycles <li data-bbox="747 634 1346 740">▪ L3 filled from L2 victims of all four cores <li data-bbox="747 756 1661 862">▪ L2 tags duplicated in L3 for probe filtering and fast cache transfer <li data-bbox="747 878 1400 919">▪ Multiple smart prefetchers <li data-bbox="747 935 1849 976">▪ 50 outstanding misses from L2 to L3 per core <li data-bbox="747 992 1768 1040">▪ 96 outstanding misses from L3 to memory <p data-bbox="728 1057 989 1089">Source: Beck, p.7</p>  <p>The diagram illustrates the cache hierarchy for CORE 0. It features a private L2 cache (512K) with a 64K 4-way I-Cache and a 32K 8-way D-Cache. The L2 is connected to an 8M L3 I+D Cache (16-way) via a 32B/cycle interface. Data flow includes 32B fetch, 2*16B load, and 1*16B store.</p>

<u>Limitation</u>	<u>Contention</u>
	<div data-bbox="728 264 2373 857"> <p>The diagram, titled "SUMMIT RIDGE" and "DATA FLOW", illustrates the data flow in an AMD processor. It shows a 64K I-Cache (4-way) and a 32K D-Cache (8-way) connected to a 512K L2 I+D Cache (8-way), which is in turn connected to an 8M L3 I+D Cache (16-way). Data flows from the L3 cache through a Data Fabric to a Unified Memory Controller (32B/cycle) and an IO Hub Controller (32B/cycle). The Unified Memory Controller is connected to a DRAM Channel (16B/cycle). Clock signals are labeled as @cclk and @memclk. The AMD logo is in the top right corner.</p> </div> <p>Source: Mitchell et al., GDC18 AMD Ryzen™ CPU Optimization, p.10.</p> <p>The frequency changes are programmable to enable user-selectable frequency transitions. See e.g., AMD Ryzen Master Overclocking Guide (“OC Guide”), p.11:</p> <ol style="list-style-type: none"> 1. <u>The frequency of processor core clock is determined by a combination of the software-requested p-state</u> and then adjusted by a combination of numerous power and performance optimizing features to attain any of number of fine grain p-states around that software-requested p-state. <p>See also OC Guide, p.13:</p>

	<u>Limitation</u>	<u>Contention</u>
		<p data-bbox="741 272 2064 399">3) CPU low power c-states (CC1, CC6, and PC6) and software visible p-states (P1 and P2) remain operational and may be requested by software so that power savings can be achieved.</p> <p data-bbox="741 456 1096 488">See also OC guide, p.11:</p> <p data-bbox="768 505 2381 737">4. Software requested p-state or halt states adjust the level of power to which those internal control mechanisms manage. For example, <u>when software executes a HALT instruction on a processor core, that core will enter the C1 reduced-power state.</u> If that core does not receive an interrupt to resume execution, it will progress to increasingly-lower power states until finally saving the state of the core and being powered off.</p> <p data-bbox="741 797 1467 829">See also, e.g., 16h BKDG section 2.5.3.1.2; p. 548:</p>

<u>Limitation</u>	<u>Contention</u>
	<p>2.5.3.1.2 Core P-state Control</p> <p>Core P-states are dynamically controlled by software and are exposed through ACPI objects (refer to 2.5.3.1.8.3 [ACPI Processor P-state Objects]). Software requests a core P-state change by writing a 3 bit index corresponding to the desired P-state number to <u>MSRC001_0062[PstateCmd]</u> of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's <u>MSRC001_0062[PstateCmd]</u>.</p> <p>Boosted P-states may not be directly requested by software. Whenever software requests the P0 state on a processor that supports APM (i.e. writes 000b to <u>MSRC001_0062[PstateCmd]</u>), hardware dynamically places the core into the highest-performance P-state possible as determined by APM. See 2.5.9 [Application Power Management (APM)].</p> <p>Hardware sequences the frequency and voltage changes necessary to complete a P-state transition as specified by 2.5.3.1.5 [Core P-state Transition Behavior] with no additional software interaction required. Hardware also coordinates frequency and voltage changes when differing P-state requests are made on cores that share a frequency or voltage plane. See 2.5.2 [Frequency and Voltage Domain Dependencies] for details about hardware coordination.</p>

	<u>Limitation</u>	<u>Contention</u>						
		<p>MSRC001_0062 P-state Control</p> <hr/> <table border="1"> <thead> <tr> <th data-bbox="741 358 849 407">Bits</th> <th data-bbox="849 358 2206 407">Description</th> </tr> </thead> <tbody> <tr> <td data-bbox="741 407 849 456">63:3</td> <td data-bbox="849 407 2206 456">MBZ.</td> </tr> <tr> <td data-bbox="741 456 849 743">2:0</td> <td data-bbox="849 456 2206 743"> PstateCmd: P-state change command. Read-write; Not-same-for-all. Cold reset value varies by product; after a warm reset, value initializes to the P-state the core was in prior to the reset. <u>Writes to this field cause the core to change to the indicated non-boosted P-state number, specified by MSRC001_00[6B:64].</u> 0=P0, 1=P1, etc. P-state limits are applied to any P-state requests made through this register. Reads from this field return the last written value, regardless of whether any limits are applied. This field uses software P-state numbering. See 2.5.3 [CPU Power Management] and 2.5.3.1.1.1 [Software P-state Numbering]. </td> </tr> </tbody> </table>	Bits	Description	63:3	MBZ.	2:0	PstateCmd: P-state change command. Read-write; Not-same-for-all. Cold reset value varies by product; after a warm reset, value initializes to the P-state the core was in prior to the reset. <u>Writes to this field cause the core to change to the indicated non-boosted P-state number, specified by MSRC001_00[6B:64].</u> 0=P0, 1=P1, etc. P-state limits are applied to any P-state requests made through this register. Reads from this field return the last written value, regardless of whether any limits are applied. This field uses software P-state numbering. See 2.5.3 [CPU Power Management] and 2.5.3.1.1.1 [Software P-state Numbering].
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1e	<p>wherein said special modes comprise a first special mode in which clock supply to principal constituents of said central processing unit is halted, a second special mode in which clock supply to an entirety of said central processing unit is halted, and a third special mode in which supply of power to the entirety of said central processing unit is halted.</p>	<p>The Accused Products include a first special mode in which clock supply to principal constituents of said central processing unit is halted, for example the core C1 (CC1) state:</p> <p>See OC guide, p.11:</p> <p>4. Software requested p-state or halt states adjust the level of power to which those internal control mechanisms manage. For example, when software executes a HALT instruction on a processor core, that core will enter the C1 reduced-power state. If that core does not receive an interrupt to resume execution, it will progress to increasingly-lower power states until finally saving the state of the core and being powered off.</p> <p>See https://www.reddit.com/r/Amd/comments/6w793f/how_to_reduce_idle_clock_speed_on_a_manually/dm6gfkv/</p>						

	<u>Limitation</u>	<u>Contention</u>
		<p>The Ryzen Balanced plan tells Windows to keep a core in p0 for the fastest possible ramp time to max clock. "Keep this core in p0" is only true when the core is actively being used. When the core is not being used, our microcode will put the core into core-c1 (cc1) through core-c6 (cc6) sleep states. The cores are so dormant in the CC sleep states that their true clockspeed cannot be probed, though the core's current VID can be.</p> <p>Zen cores can enter into and out of the CC sleep states up to 1000 times a second, and will spend the majority of their time in a CC sleep state when not under active load. The effective frequency for a core in this condition is sub-1GHz and sub-1V. Unfortunately there isn't really a tool that can capture this, because the act of probing the core's sleep condition is sufficient load to wake the core and ruin the power savings of the CC state.</p>

<u>Limitation</u>	<u>Contention</u>
	<p>Region Power Gating by LDO PG Headers Latencies 100us or less</p> <p>Multiple LDO Regions Gated Latencies 1.5ms or less</p> <p>Input VDD Rail Off</p> <p>Active States, Clock Gated States</p> <p>Active States, Deep Sleep States, Clock Gated States</p> <p>CC6 Meet CC6 Entry Timer</p> <p>Graphics Power Gating Meet GFX Idle Entry Timer</p> <p>CPUOFF All Cores in CC6 and Meet CPUOFF Entry Timer</p> <p>GFXOFF Meet GFXOFF Entry Timer</p> <p>VDDOFF Enter if simultaneous CPUOFF & GFX OFF</p> <p>Deeper Low Power States</p> <p>Faster Entry/Exit Latencies</p>
	<p>Source: Anderson, AMD Ryzen™ Processor With Radeon Vega Graphics, p. 41</p> <p>See also, e.g., 16h BKDG:</p>

<u>Limitation</u>	<u>Contention</u>
	<p>2.5.3.2.3.2 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct].</p> <p>2.5.3.2.3.2 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct].</p> <p>2.5.3.2.3.3 Core C6 (CC6) State</p> <p>A core can gate off power to its internal logic when it enters any non-C0 state. This power gated state is known as CC6. In order to enter CC6, hardware first enters CC1 then checks D18F4x118/D18F4x11C[PwrGateEnCstAct]. Power gating reduces the amount of power consumed by the core. VDD voltage is not reduced when a core is in CC6. The following sequence occurs when a core enters the CC6 state:</p> <ol style="list-style-type: none"> 1. If MSRC001_0071[CurPstate] < D18F3xA8[PopDownPstate], transition the core P-state to D18F3xA8[PopDownPstate]. 2. Internal core state is saved to L1 cache . 3. L1 cache is flushed to L2 cache. See 2.5.3.2.3.1 [C-state Probes and Cache Flushing]. 4. Power is removed from the core and the core PLL/voltage regulator is powered down as specified by D18F5x128[CC6PwrDwnRegEn].

<u>Limitation</u>	<u>Contention</u>																						
	<p>D18F4x11[C:8] C-state Control</p> <p>D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states].</p> <ul style="list-style-type: none"> • D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]. • D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1. • D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2. <p>D18F4x118 C-state Control 1</p> <table border="1" data-bbox="758 735 2214 1330"> <tr> <td data-bbox="758 735 862 1330">7:5</td> <td data-bbox="870 735 2214 1330"> <p>ClkDivisorCstAct0: clock divisor. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or:</p> <ul style="list-style-type: none"> • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. <p>If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.</p> <table border="1" data-bbox="870 1089 1704 1284"> <thead> <tr> <th><u>Bits</u></th> <th><u>Description</u></th> <th><u>Bits</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>/1</td> <td>100b</td> <td>/16</td> </tr> <tr> <td>001b</td> <td>/2</td> <td>101b</td> <td>/128</td> </tr> <tr> <td>010b</td> <td>/4</td> <td>110b</td> <td>/512</td> </tr> <tr> <td>011b</td> <td>/8</td> <td>111b</td> <td><u>Turn off clocks.</u></td> </tr> </tbody> </table> <p>See CacheFlushTmrSelCstAct0.</p> </td> </tr> </table>	7:5	<p>ClkDivisorCstAct0: clock divisor. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or:</p> <ul style="list-style-type: none"> • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. <p>If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.</p> <table border="1" data-bbox="870 1089 1704 1284"> <thead> <tr> <th><u>Bits</u></th> <th><u>Description</u></th> <th><u>Bits</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>/1</td> <td>100b</td> <td>/16</td> </tr> <tr> <td>001b</td> <td>/2</td> <td>101b</td> <td>/128</td> </tr> <tr> <td>010b</td> <td>/4</td> <td>110b</td> <td>/512</td> </tr> <tr> <td>011b</td> <td>/8</td> <td>111b</td> <td><u>Turn off clocks.</u></td> </tr> </tbody> </table> <p>See CacheFlushTmrSelCstAct0.</p>	<u>Bits</u>	<u>Description</u>	<u>Bits</u>	<u>Description</u>	000b	/1	100b	/16	001b	/2	101b	/128	010b	/4	110b	/512	011b	/8	111b	<u>Turn off clocks.</u>
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	<p>The Accused Products include a second special mode in which clock supply to an entirety of said central processing unit is halted, for example the package C1 (PC1) state.</p> <p>See e.g., 14h BKDG:</p> <p>2.5.3.2.3.3 Package C1 (PC1) State</p> <p>The processor enters the PC1 state with auto-Pmin when all of the following are true:</p> <ul style="list-style-type: none"> • All cores are in the CC1 state or deeper. <p>If D18F4x1AC[CstPminEn] indicates that auto-Pmin is enabled when the processor enters PC1, the P-state for all cores is transitioned as specified by 2.5.3.2.7.1 [Auto-Pmin]. Regardless of the state of D18F4x1AC[CstPminEn], all core clocks are ramped to the frequency specified by D18F4x1A8[AllHaltCpuDid].</p> <p>D18F4x1A8 CPU State Power Management Dynamic Control 0</p> <hr/> <p>Reset: 0000_0000h.</p> <table border="1" data-bbox="747 1019 2198 1393"> <tr> <td data-bbox="747 1019 854 1393">9:5</td> <td data-bbox="854 1019 2198 1393"> <p>AllHaltCpuDid. Read-write. BIOS: 1Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State].</p> <table border="1"> <thead> <tr> <th><u>Bits</u></th> <th><u>Divisor</u></th> </tr> </thead> <tbody> <tr> <td>1Ch-00h</td> <td>Reserved.</td> </tr> <tr> <td>1Dh</td> <td>128</td> </tr> <tr> <td>1Eh</td> <td>512</td> </tr> <tr> <td><u>1Fh</u></td> <td><u>Clocks off.</u></td> </tr> </tbody> </table> <p>See D18F4x1A8[SingleHaltCpuDid].</p> </td> </tr> </table>	9:5	<p>AllHaltCpuDid. Read-write. BIOS: 1Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State].</p> <table border="1"> <thead> <tr> <th><u>Bits</u></th> <th><u>Divisor</u></th> </tr> </thead> <tbody> <tr> <td>1Ch-00h</td> <td>Reserved.</td> </tr> <tr> <td>1Dh</td> <td>128</td> </tr> <tr> <td>1Eh</td> <td>512</td> </tr> <tr> <td><u>1Fh</u></td> <td><u>Clocks off.</u></td> </tr> </tbody> </table> <p>See D18F4x1A8[SingleHaltCpuDid].</p>	<u>Bits</u>	<u>Divisor</u>	1Ch-00h	Reserved.	1Dh	128	1Eh	512	<u>1Fh</u>	<u>Clocks off.</u>
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	<p>The Accused Products include a third special mode in which supply of power to the entirety of said central processing unit is halted, for example the package C6 (PC6) state:</p> <p>See also OC Guide, p.13:</p> <p>3) CPU low power c-states (CC1, CC6, and <u>PC6</u>) and software visible p-states (P1 and P2) remain operational and may be requested by software so that power savings can be achieved.</p> <div data-bbox="733 643 1607 1312" data-label="Diagram"> </div> <p>Source: Anderson, AMD Ryzen™ Processor With Radeon Vega Graphics, p. 41</p>

<u>Limitation</u>	<u>Contention</u>		
	<p>See also, e.g., 16h BKDG:</p> <p>2.5.3.2.3.4 Package C6 (PC6) State</p> <p>When all cores enter a non-C0 state, VDD can be reduced to a non-operational voltage that does not retain core state. This state is known as PC6 and reduces the amount of static and dynamic power consumed by all cores. The following actions are taken by hardware prior to PC6 entry:</p> <ol style="list-style-type: none"> 1. If MSRC001_0071[CurPstate] < D18F3xA8[PopDownPstate], transition the core P-state to D18F3xA8[PopDownPstate]. 2. For all cores not in CC6, internal core state is saved to L1 cache . 3. For all cores not in CC6, L1 cache is flushed to L2 cache. See 2.5.3.2.3.1 [C-state Probes and Cache Flushing]. 4. VDD is transitioned to the VID specified by D18F5x128[PC6Vid]. 5. If the core PLLs are not powered down during CC6 entry (see 2.5.3.2.3.3 [Core C6 (CC6) State]), then they are powered down as specified by D18F5x128[PC6PwrDwnRegEn]. <p>D18F5x128 Clock Power/Timing Control 3</p> <hr/> <table border="1" data-bbox="741 971 2214 1101"> <tr> <td data-bbox="741 971 849 1101">6:0</td> <td data-bbox="854 971 2214 1101">PC6Vid[6:0]: package C6 vid. Read-write. Cold reset: Product-specific. PC6Vid[7:0] = {PC6Vid[7], PC6Vid[6:0]}. PC6Vid[7:0] specifies the VID driven in the PC6 state. See 2.5.3.2.3.4 [Package C6 (PC6) State] and 2.5.1.3.2 [Low Power Voltages].</td> </tr> </table>	6:0	PC6Vid[6:0]: package C6 vid. Read-write. Cold reset: Product-specific. PC6Vid[7:0] = {PC6Vid[7], PC6Vid[6:0]}. PC6Vid[7:0] specifies the VID driven in the PC6 state. See 2.5.3.2.3.4 [Package C6 (PC6) State] and 2.5.1.3.2 [Low Power Voltages].
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	<u>Limitation</u>	<u>Contention</u>
		<p>2.5.1.3.2 Low Power Voltages</p> <p>In order to save power, voltages lower than those normally needed for operation may be applied to the VDD power plane while the processor is in a C-state or S-state. The lower voltage is defined as follows:</p> <ul style="list-style-type: none"> • PC6Vid: D18F5x128[PC6Vid] specifies a voltage that does not retain the CPU caches or the core microarchitectural state. PC6Vid does not allow execution and is only applied to the cores. See 2.5.3.2.3.4 [Package C6 (PC6) State]. <p>2.5.1.4.1 Hardware-Initiated Voltage Transitions</p> <p>When software requests any of the following state changes, or hardware determines that any of the following state changes are necessary, hardware coordinates the necessary voltage changes:</p> <ul style="list-style-type: none"> • VDD: <ul style="list-style-type: none"> • Core P-state transition. See 2.5.3.1 [Core P-states]. • Package C-state transition. D18F5x128[PC6Vid] specifies a voltage that does not retain the CPU caches or the core microarchitectural state. PC6Vid does not allow execution and is only applied to the cores. See 2.5.3.2.3.4 [Package C6 (PC6) State]. • S-state transition. See 2.5.8.1 [S-states].
2p	A system LSI as claimed in claim 1, wherein said clock control library comprises:	
2a	a plurality of libraries that	The clock control libraries of the Accused Products contain a plurality of libraries that control the SMU and clock

	<u>Limitation</u>	<u>Contention</u>
	control said system control circuit and said clock generation circuit to transition the clock frequencies supplied to said central processing unit; and	generator to transition clock frequencies. For example, source code provided by AMD to coreboot indicates that P-state and C-state transitions are controlled by separate libraries: https://github.com/coreboot/coreboot/tree/master/src/vendorcode/amd/agesa/f14/Proc/CPU/Feature
2b	a main library which is called by said application program and selects any one of said libraries in correspondence with the clock frequency supplied to said central processing unit.	As discussed above, P-states and C-states may be controlled by software, which includes a main library that calls upon the plurality of libraries.
3p	A system LSI as claimed in claim 2,	
3a	wherein said main library is described using a same program language as said application program.	The main library in the SMU firmware and the application program instructions stored in the caches are both use the same language such as machine code.
5p	A system LSI as claimed in claim 2,	

	<u>Limitation</u>	<u>Contention</u>
5a	wherein each of said libraries is described using a program language capable of directly controlling said clock generation circuit and said system control circuit.	The SMU firmware directly controls the SMU hardware.
6p	A system LSI as claimed in claim 5,	
6a	wherein each of said libraries is described using an assembler language.	The SMU firmware directly controls the SMU hardware and is described using an assembler language such as machine code.
7p	7. A system LSI as claimed in claim 1, wherein said system control circuit comprises:	
7a	a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit;	The system control circuit of the Accused Products as described above contains a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit. See e.g., 16h BKDG:

<u>Limitation</u>	<u>Contention</u>
	<div data-bbox="811 263 1284 529" data-label="Diagram"> <p style="text-align: center;">Northbridge (NB)</p> <ul style="list-style-type: none"> - Transaction routing - Configuration and IO-space registers - Root complex - Graphics core (optional) </div> <p data-bbox="731 607 1034 638">BKDG, section 2.12:</p> <p data-bbox="747 651 1257 682">2.12 System Management Unit (SMU)</p> <p data-bbox="747 716 2085 818">The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details.</p> <p data-bbox="747 862 1085 893">2.12.1 Microcontroller</p> <p data-bbox="747 927 1623 958">The SMU contains a microcontroller with a 16k ROM and a 16k RAM.</p> <p data-bbox="731 1008 1919 1039">Configuration space register mnemonics are defined in section 3.1 of the BKG:</p> <ul data-bbox="747 1047 2161 1192" style="list-style-type: none"> • DXFYxZZZ: PCI-defined configuration space; X specifies the hexadecimal device number (this may be 1 or 2 digits), Y specifies the function number, and ZZZ specifies the hexadecimal byte address (this may be 2 or 3 digits; e.g., D18F3x40 specifies the register at device 18h, function 3, and address 40h). See 2.7 [Configuration Space], for details about configuration space. <p data-bbox="731 1240 1091 1271">the core C1 (CC1) state:</p>

<u>Limitation</u>	<u>Contention</u>
	<p>2.5.3.2.3.2 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct].</p> <p><u>D18F4x11[C:8] C-state Control</u></p> <p>D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states].</p> <ul style="list-style-type: none"> • D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]. • D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1. • D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2. <p>D18F4x118 C-state Control 1</p>

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7b	a clock halting register that receives the clock from said clock generation circuit and individually sets the clock to be halted or supplied;	the core C1 (CC1) state:																				

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		<p>2.5.3.2.3.2 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct].</p> <p><u>D18F4x11[C:8] C-state Control</u></p> <p>D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states].</p> <ul style="list-style-type: none"> • D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]. • D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1. • D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2. <p>D18F4x118 C-state Control 1</p>

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7c	And a status register that judges a state of said central processing unit immediately after being released from said third special mode.	The Accused Products contain a status register that judges a state of the CPU after waking from PC6. See 14h BKDG:																				

<u>Limitation</u>	<u>Contention</u>		
	<p>2.5.3.2.7.2 Exiting PC6</p> <p>If the PService timer is enabled when the processor exits PC6, all cores transition to the P-state specified by D18F4x1AC[PstateIdCoreOffExit]. The cores remain in this state until one of the following occurs:</p> <ul style="list-style-type: none"> • The PService timer expires while the package is in C0: In this case, the cores transition back to the last P-state requested by software. • The package enters PC1 without auto-Pmin: In this case, the PService timer continues counting. If it expires while in PC1, the cores remain in the P-state specified by D18F4x1AC[PstateIdCoreOffExit] until they return to C0, at which time they transition to the last P-state requested by software. • The package enters PC1 with auto-Pmin: In this case, the PService timer stops counting and the cores enter the PService state. • The package enters PC6: In this case the PService timer stops counting and the actions associated the requested package C-state occur. See 2.5.3.2.3.4 [Package C6 (PC6) State]. <p>If the PService timer is disabled when the processor exits PC6, the cores transition back to the last P-state requested by software.</p> <p>See also 14h BKDG pp.320-321:</p> <p><u>D18F4x1AC CPU State Power Management Dynamic Control 1</u></p> <table border="1" data-bbox="747 1063 2198 1360"> <tr> <td data-bbox="747 1063 854 1360">18:16</td> <td data-bbox="854 1063 2198 1360">PstateIdCoreOffExit. Read-write. Reset: 0. BIOS: See 2.5.3.2.9. When exiting the package C6 state, the core transitions to the P-state specified by this register. See 2.5.3.2.7.2 [Exiting PC6]. If PC6 is enabled (see 2.5.3.2.9 [BIOS Requirements for C-state Initialization]), PstateIdCoreOffExit must be programmed to the lowest-performance P-state displayed to the operating system or to any lower-performance P-state. This P-state must have a core clock frequency of at least 400 MHz. Programming this field to 0 causes the core to transition to the last P-state requested by software when exiting package C6. This field uses hardware P-state numbering. See 2.5.3.1.2.2 [Hardware P-state Numbering].</td> </tr> </table>	18:16	PstateIdCoreOffExit. Read-write. Reset: 0. BIOS: See 2.5.3.2.9. When exiting the package C6 state, the core transitions to the P-state specified by this register. See 2.5.3.2.7.2 [Exiting PC6]. If PC6 is enabled (see 2.5.3.2.9 [BIOS Requirements for C-state Initialization]), PstateIdCoreOffExit must be programmed to the lowest-performance P-state displayed to the operating system or to any lower-performance P-state. This P-state must have a core clock frequency of at least 400 MHz. Programming this field to 0 causes the core to transition to the last P-state requested by software when exiting package C6. This field uses hardware P-state numbering. See 2.5.3.1.2.2 [Hardware P-state Numbering].
18:16	PstateIdCoreOffExit. Read-write. Reset: 0. BIOS: See 2.5.3.2.9. When exiting the package C6 state, the core transitions to the P-state specified by this register. See 2.5.3.2.7.2 [Exiting PC6]. If PC6 is enabled (see 2.5.3.2.9 [BIOS Requirements for C-state Initialization]), PstateIdCoreOffExit must be programmed to the lowest-performance P-state displayed to the operating system or to any lower-performance P-state. This P-state must have a core clock frequency of at least 400 MHz. Programming this field to 0 causes the core to transition to the last P-state requested by software when exiting package C6. This field uses hardware P-state numbering. See 2.5.3.1.2.2 [Hardware P-state Numbering].		

	<u>Limitation</u>	<u>Contention</u>
10p	A system LSI as claimed in claim 1,	
10a	wherein said first memory and said second memory are two independent memories which are separated from each other.	As detailed above, the first memory in the SMU and the second memory in the caches are independent memories that are separated from each other.

Exhibit B.5: Preliminary Infringement Claim Chart for U.S. Patent 6,895,519

Accused Products: AMD Family 12h Products

These preliminary infringement contentions were prepared without the benefit of the Court's claim construction or the parties' exchange of constructions. As of the date of these contentions, AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court's constructions or to account for new information that becomes available.

	<u>Limitation</u>	<u>Contention</u>
1p	A system LSI having a plurality of ordinary operation modes and a plurality of special modes in response to clock frequencies supplied to a central processing unit, comprising:	<p>To the extent that the preamble is limiting, Aquila contends that it is met.</p> <p>For example, each product in the 12h Accused Product Family ("Accused Product") is a system LSI.</p> <p>The Accused Product has a plurality of ordinary operation modes, for example the Core P-states. <i>See</i> BIOS and Kernel Developer's Guide for AMD Family 12h Models 00h-0Fh Processors ("BKDG"), §2.5.3.1:</p>

	<u>Limitation</u>	<u>Contention</u>
		<p>2.5.3.1 Core P-states</p> <p>Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states, specified in MSRC001_00[6B:64]. Out of reset, the voltage and frequency of the cores is specified by MSRC001_0071[StartupPstate].</p> <p>Support for dynamic core P-state changes is indicated by more than one enabled selection in MSRC001_00[6B:64][PstateEn]. All FID and DID parameters for equivalent P-states must be programmed to equivalent values for all cores. For examples, P0 on core0 must have the same FID and DID values as P0 on core1, P1 on core0 must have the same FID and DID values as P1 on core1, and so on. Refer to MSRC001_00[6B:64] for further details on programming requirements. The COF for core P-states is a function of the FID and the DID. See MSRC001_00[6B:64][CpuFid, CpuDid] for more details.</p> <p>Software requests core P-state changes for each core independently using the hardware P-state control mechanism (a.k.a. fire and forget). Support for hardware P-state control is indicated by CPUID Fn8000_0007_EDX[HwPstate]=1b. P-state transitions using the hardware P-state control mechanism are not allowed until the P-state initialization requirements defined in 2.5.3.1.7 [BIOS Requirements for Core P-State Initialization and Transitions] are complete.</p> <p>BKDG at p.47:</p>

<u>Limitation</u>	<u>Contention</u>																																								
	<p>Table 5: Software P-state numbering example</p> <table border="1"> <thead> <tr> <th colspan="2" style="text-align: left;">D18F4x15C[NumBoostStates]=1</th> <th colspan="2" style="text-align: left;">D18F4x15C[NumBoostStates]=3</th> </tr> <tr> <th>P-state Name</th> <th>MSR Address</th> <th>P-state Name</th> <th>MSR Address</th> </tr> </thead> <tbody> <tr> <td>Pb0</td> <td>MSRC001_0064</td> <td>Pb0</td> <td>MSRC001_0064</td> </tr> <tr> <td>P0</td> <td>MSRC001_0065</td> <td>Pb1</td> <td>MSRC001_0065</td> </tr> <tr> <td>P1</td> <td>MSRC001_0066</td> <td>Pb2</td> <td>MSRC001_0066</td> </tr> <tr> <td>P2</td> <td>MSRC001_0067</td> <td>P0</td> <td>MSRC001_0067</td> </tr> <tr> <td>P3</td> <td>MSRC001_0068</td> <td>P1</td> <td>MSRC001_0068</td> </tr> <tr> <td>P4</td> <td>MSRC001_0069</td> <td>P2</td> <td>MSRC001_0069</td> </tr> <tr> <td>P5</td> <td>MSRC001_006A</td> <td>P3</td> <td>MSRC001_006A</td> </tr> <tr> <td>P6</td> <td>MSRC001_006B</td> <td>P4</td> <td>MSRC001_006B</td> </tr> </tbody> </table> <p>All sections and register definitions use software P-state numbering unless otherwise specified.</p> <p>The Accused Product Family has a plurality of special modes, for example, the Core C-states or deep sleep modes such as ACPI S3 or connected standby S0i3. See BKDG, §§ 2.5.3.2, 2.5.3.2.1, 2.5:</p>	D18F4x15C[NumBoostStates]=1		D18F4x15C[NumBoostStates]=3		P-state Name	MSR Address	P-state Name	MSR Address	Pb0	MSRC001_0064	Pb0	MSRC001_0064	P0	MSRC001_0065	Pb1	MSRC001_0065	P1	MSRC001_0066	Pb2	MSRC001_0066	P2	MSRC001_0067	P0	MSRC001_0067	P3	MSRC001_0068	P1	MSRC001_0068	P4	MSRC001_0069	P2	MSRC001_0069	P5	MSRC001_006A	P3	MSRC001_006A	P6	MSRC001_006B	P4	MSRC001_006B
D18F4x15C[NumBoostStates]=1		D18F4x15C[NumBoostStates]=3																																							
P-state Name	MSR Address	P-state Name	MSR Address																																						
Pb0	MSRC001_0064	Pb0	MSRC001_0064																																						
P0	MSRC001_0065	Pb1	MSRC001_0065																																						
P1	MSRC001_0066	Pb2	MSRC001_0066																																						
P2	MSRC001_0067	P0	MSRC001_0067																																						
P3	MSRC001_0068	P1	MSRC001_0068																																						
P4	MSRC001_0069	P2	MSRC001_0069																																						
P5	MSRC001_006A	P3	MSRC001_006A																																						
P6	MSRC001_006B	P4	MSRC001_006B																																						

	<u>Limitation</u>	<u>Contention</u>
		<p>2.5.3.2 C-states</p> <p>C-states are processor power states. C0 is the operational state in which instructions are executed. All other C-states are low-power states in which instructions are not executed.</p> <p>2.5.3.2.1 C-state Names and Numbers</p> <p>C-states are often referred to by an alphanumeric naming convention, C1, C2, C3, etc. The mapping between ACPI defined C-states and AMD specified C-state actions is not direct. The actions taken by the processor when entering a low-power C-state are specified by D18F4x118 and D18F4x11C and are configured by software. See 2.5.3.2.3 [C-state Actions] for information about AMD specific actions.</p>

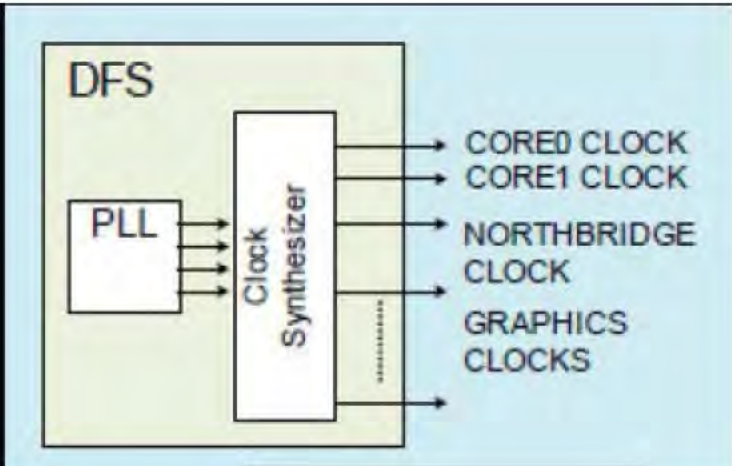
<u>Limitation</u>	<u>Contention</u>																											
	<p data-bbox="720 266 1091 298">2.5 Power Management</p> <p data-bbox="720 337 2177 409">The processor supports many power management features in a variety of systems. Table 4 provides a summary of ACPI states and power management features and indicates whether they are supported.</p> <p data-bbox="720 448 1244 480">Table 4: Power management support</p> <table border="1" data-bbox="720 496 2174 948"> <thead> <tr> <th data-bbox="720 496 1534 545">ACPI/Power Management State</th> <th data-bbox="1534 496 1749 545">Supported</th> <th data-bbox="1749 496 2174 545">Description</th> </tr> </thead> <tbody> <tr> <td data-bbox="720 545 1534 586">G0/S0/C0: Working</td> <td data-bbox="1534 545 1749 586">Yes</td> <td data-bbox="1749 545 2174 586"></td> </tr> <tr> <td data-bbox="720 586 1534 626">G0/S0/C0: Core P-state transitions</td> <td data-bbox="1534 586 1749 626">Yes</td> <td data-bbox="1749 586 2174 626">2.5.3.1 [Core P-states]</td> </tr> <tr> <td data-bbox="720 626 1534 667">G0/S0/C0: NB P-state transitions</td> <td data-bbox="1534 626 1749 667">Yes</td> <td data-bbox="1749 626 2174 667">2.5.4.2 [NB Clock Ramping]</td> </tr> <tr> <td data-bbox="720 667 1534 748">G0/S0/C0: Hardware thermal control (HTC)</td> <td data-bbox="1534 667 1749 748">Yes</td> <td data-bbox="1749 667 2174 748">2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)]</td> </tr> <tr> <td data-bbox="720 748 1534 789">G0/S0/C0: Software thermal control (STC)</td> <td data-bbox="1534 748 1749 789">No</td> <td data-bbox="1749 748 2174 789"></td> </tr> <tr> <td data-bbox="720 789 1534 829">G0/S0/C0: Thermal clock throttling (SMC controlled)</td> <td data-bbox="1534 789 1749 829">No</td> <td data-bbox="1749 789 2174 829"></td> </tr> <tr> <td data-bbox="720 829 1534 911">G0/S0: Low power C-states</td> <td data-bbox="1534 829 1749 911">Yes</td> <td data-bbox="1749 829 2174 911">2.5.3.2 [C-states] and 2.5.1.4.2 [Alternate Low Power Voltages]</td> </tr> <tr> <td data-bbox="720 911 1534 948">G1/S1: Stand By (Powered On Suspend)</td> <td data-bbox="1534 911 1749 948">No</td> <td data-bbox="1749 911 2174 948"></td> </tr> </tbody> </table>	ACPI/Power Management State	Supported	Description	G0/S0/C0: Working	Yes		G0/S0/C0: Core P-state transitions	Yes	2.5.3.1 [Core P-states]	G0/S0/C0: NB P-state transitions	Yes	2.5.4.2 [NB Clock Ramping]	G0/S0/C0: Hardware thermal control (HTC)	Yes	2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)]	G0/S0/C0: Software thermal control (STC)	No		G0/S0/C0: Thermal clock throttling (SMC controlled)	No		G0/S0: Low power C-states	Yes	2.5.3.2 [C-states] and 2.5.1.4.2 [Alternate Low Power Voltages]	G1/S1: Stand By (Powered On Suspend)	No	
ACPI/Power Management State	Supported	Description																										
G0/S0/C0: Working	Yes																											
G0/S0/C0: Core P-state transitions	Yes	2.5.3.1 [Core P-states]																										
G0/S0/C0: NB P-state transitions	Yes	2.5.4.2 [NB Clock Ramping]																										
G0/S0/C0: Hardware thermal control (HTC)	Yes	2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)]																										
G0/S0/C0: Software thermal control (STC)	No																											
G0/S0/C0: Thermal clock throttling (SMC controlled)	No																											
G0/S0: Low power C-states	Yes	2.5.3.2 [C-states] and 2.5.1.4.2 [Alternate Low Power Voltages]																										
G1/S1: Stand By (Powered On Suspend)	No																											

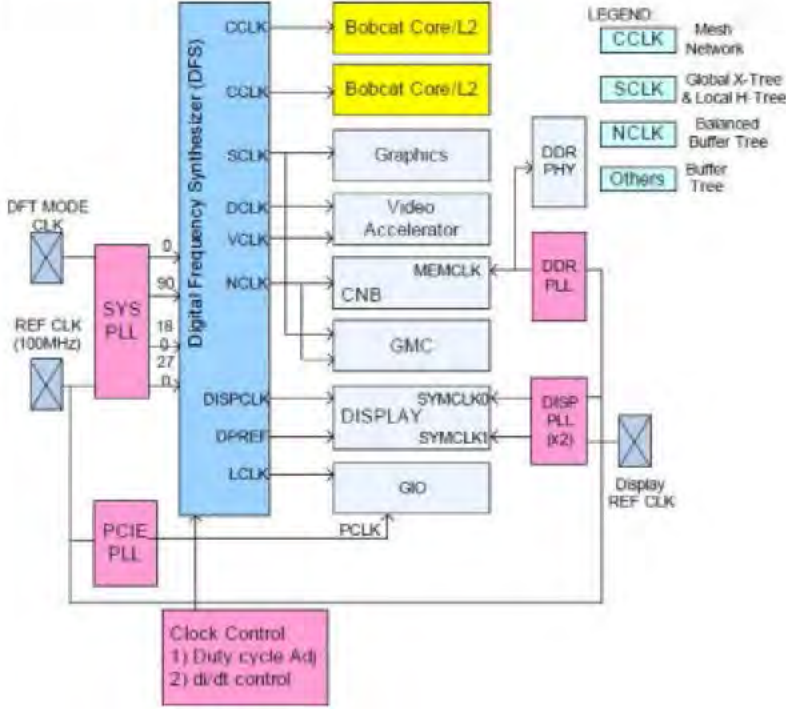
	<u>Limitation</u>	<u>Contention</u>																			
		<p>Table 4: Power management support</p> <table border="1" data-bbox="728 337 2171 667"> <thead> <tr> <th data-bbox="728 337 1529 383">ACPI/Power Management State</th> <th data-bbox="1529 337 1744 383">Supported</th> <th data-bbox="1744 337 2171 383">Description</th> </tr> </thead> <tbody> <tr> <td data-bbox="728 383 1529 459">G1/S3: Stand By (Suspend to RAM)</td> <td data-bbox="1529 383 1744 459">Yes</td> <td data-bbox="1744 383 2171 459">2.5.7.1.1 [ACPI Suspend to RAM State (S3)]</td> </tr> <tr> <td data-bbox="728 459 1529 500">G1/S4, S5: Hibernate (Suspend to Disk), Shut Down (Soft Off)</td> <td data-bbox="1529 459 1744 500">Yes</td> <td data-bbox="1744 459 2171 500"></td> </tr> <tr> <td data-bbox="728 500 1529 540">G3 Mechanical Off</td> <td data-bbox="1529 500 1744 540">Yes</td> <td data-bbox="1744 500 2171 540"></td> </tr> <tr> <td data-bbox="728 540 1529 581">Parallel VID Interface</td> <td data-bbox="1529 540 1744 581">No</td> <td data-bbox="1744 540 2171 630" rowspan="3">2.5.1 [Processor Power Planes And Voltage Control]</td> </tr> <tr> <td data-bbox="728 581 1529 621">Serial VID Interface</td> <td data-bbox="1529 581 1744 621">Yes</td> </tr> <tr> <td data-bbox="728 621 1529 667">Dual-plane systems</td> <td data-bbox="1529 621 1744 667">Yes</td> </tr> </tbody> </table> <p data-bbox="715 768 2483 867">Furthermore, the Core P-states and Core C-states are in response to clock frequencies supplied to a central processing unit. For example, the core P-states are “characterized” by “core frequency;” core P-state changes are further requested by software. <i>See e.g.</i>, BKDG, § 2.5.3.1, 2.5.3.1.3.</p> <p data-bbox="715 906 2483 972">Similarly, C-states are “dynamically requested by software” and also dependent upon clock frequency. <i>See</i> BKDG §§ 2.5.3.2.2, 2.5.3.2.3.1, 2.5.3.2.3.2, p.343.</p>	ACPI/Power Management State	Supported	Description	G1/S3: Stand By (Suspend to RAM)	Yes	2.5.7.1.1 [ACPI Suspend to RAM State (S3)]	G1/S4, S5: Hibernate (Suspend to Disk), Shut Down (Soft Off)	Yes		G3 Mechanical Off	Yes		Parallel VID Interface	No	2.5.1 [Processor Power Planes And Voltage Control]	Serial VID Interface	Yes	Dual-plane systems	Yes
ACPI/Power Management State	Supported	Description																			
G1/S3: Stand By (Suspend to RAM)	Yes	2.5.7.1.1 [ACPI Suspend to RAM State (S3)]																			
G1/S4, S5: Hibernate (Suspend to Disk), Shut Down (Soft Off)	Yes																				
G3 Mechanical Off	Yes																				
Parallel VID Interface	No	2.5.1 [Processor Power Planes And Voltage Control]																			
Serial VID Interface	Yes																				
Dual-plane systems	Yes																				
1a	a first memory that stores a clock control library for controlling a clock frequency transition between said ordinary operation modes;	The Accused Products include a first memory that stores a clock control library. For example, the SMU contains memory that stores the firmware and configuration space registers, including a clock control library. The clock control library controls clock frequency transition between the P-states. <i>See e.g.</i> , BKDG, Fig. 1:																			

	<u>Limitation</u>	<u>Contention</u>
		<div data-bbox="790 261 1266 526" style="border: 1px solid black; padding: 5px; margin-bottom: 10px;"> <p style="text-align: center;">↓</p> <p style="text-align: center;">Northbridge (NB)</p> <ul style="list-style-type: none"> - Transaction routing - Configuration and IO-space registers - Root complex - Graphics core (optional) <p style="text-align: right;">←</p> </div> <p>BKDG, section 2.12: 2.12 System Management Unit (SMU)</p> <p>The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details.</p> <p>2.12.1 Microcontroller</p> <p>The SMU contains a microcontroller with a 16k ROM and a 16k RAM.</p> <p>See also BKDG, Table 10:</p>

	<u>Limitation</u>	<u>Contention</u>																																																												
		<p>Table 6: P-state control example</p> <table border="1"> <thead> <tr> <th colspan="3" data-bbox="728 337 1462 391">D18F4x15C[NumBoostStates]=1</th> <th colspan="3" data-bbox="1462 337 2196 391">D18F4x15C[NumBoostStates]=3</th> </tr> <tr> <th data-bbox="728 391 943 483">P-state Name</th> <th data-bbox="943 391 1204 483">Index Used for Requests/Status</th> <th data-bbox="1204 391 1462 483">Corresponding MSR Address</th> <th data-bbox="1462 391 1677 483">P-state Name</th> <th data-bbox="1677 391 1938 483">Index Used for Requests/Status</th> <th data-bbox="1938 391 2196 483">Corresponding MSR Address</th> </tr> </thead> <tbody> <tr> <td data-bbox="728 483 943 537">Pb0</td> <td data-bbox="943 483 1204 537">n/a</td> <td data-bbox="1204 483 1462 537">MSRC001_0064</td> <td data-bbox="1462 483 1677 537">Pb0</td> <td data-bbox="1677 483 1938 537">n/a</td> <td data-bbox="1938 483 2196 537">MSRC001_0064</td> </tr> <tr> <td data-bbox="728 537 943 591">P0</td> <td data-bbox="943 537 1204 591">0</td> <td data-bbox="1204 537 1462 591">MSRC001_0065</td> <td data-bbox="1462 537 1677 591">Pb1</td> <td data-bbox="1677 537 1938 591">n/a</td> <td data-bbox="1938 537 2196 591">MSRC001_0065</td> </tr> <tr> <td data-bbox="728 591 943 644">P1</td> <td data-bbox="943 591 1204 644">1</td> <td data-bbox="1204 591 1462 644">MSRC001_0066</td> <td data-bbox="1462 591 1677 644">Pb2</td> <td data-bbox="1677 591 1938 644">n/a</td> <td data-bbox="1938 591 2196 644">MSRC001_0066</td> </tr> <tr> <td data-bbox="728 644 943 698">P2</td> <td data-bbox="943 644 1204 698">2</td> <td data-bbox="1204 644 1462 698">MSRC001_0067</td> <td data-bbox="1462 644 1677 698">P0</td> <td data-bbox="1677 644 1938 698">0</td> <td data-bbox="1938 644 2196 698">MSRC001_0067</td> </tr> <tr> <td data-bbox="728 698 943 751">P3</td> <td data-bbox="943 698 1204 751">3</td> <td data-bbox="1204 698 1462 751">MSRC001_0068</td> <td data-bbox="1462 698 1677 751">P1</td> <td data-bbox="1677 698 1938 751">1</td> <td data-bbox="1938 698 2196 751">MSRC001_0068</td> </tr> <tr> <td data-bbox="728 751 943 805">P4</td> <td data-bbox="943 751 1204 805">4</td> <td data-bbox="1204 751 1462 805">MSRC001_0069</td> <td data-bbox="1462 751 1677 805">P2</td> <td data-bbox="1677 751 1938 805">2</td> <td data-bbox="1938 751 2196 805">MSRC001_0069</td> </tr> <tr> <td data-bbox="728 805 943 859">P5</td> <td data-bbox="943 805 1204 859">5</td> <td data-bbox="1204 805 1462 859">MSRC001_006A</td> <td data-bbox="1462 805 1677 859">P3</td> <td data-bbox="1677 805 1938 859">3</td> <td data-bbox="1938 805 2196 859">MSRC001_006A</td> </tr> <tr> <td data-bbox="728 859 943 912">P6</td> <td data-bbox="943 859 1204 912">6</td> <td data-bbox="1204 859 1462 912">MSRC001_006B</td> <td data-bbox="1462 859 1677 912">P4</td> <td data-bbox="1677 859 1938 912">4</td> <td data-bbox="1938 859 2196 912">MSRC001_006B</td> </tr> </tbody> </table>	D18F4x15C[NumBoostStates]=1			D18F4x15C[NumBoostStates]=3			P-state Name	Index Used for Requests/Status	Corresponding MSR Address	P-state Name	Index Used for Requests/Status	Corresponding MSR Address	Pb0	n/a	MSRC001_0064	Pb0	n/a	MSRC001_0064	P0	0	MSRC001_0065	Pb1	n/a	MSRC001_0065	P1	1	MSRC001_0066	Pb2	n/a	MSRC001_0066	P2	2	MSRC001_0067	P0	0	MSRC001_0067	P3	3	MSRC001_0068	P1	1	MSRC001_0068	P4	4	MSRC001_0069	P2	2	MSRC001_0069	P5	5	MSRC001_006A	P3	3	MSRC001_006A	P6	6	MSRC001_006B	P4	4	MSRC001_006B
D18F4x15C[NumBoostStates]=1			D18F4x15C[NumBoostStates]=3																																																											
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P0	0	MSRC001_0065	Pb1	n/a	MSRC001_0065																																																									
P1	1	MSRC001_0066	Pb2	n/a	MSRC001_0066																																																									
P2	2	MSRC001_0067	P0	0	MSRC001_0067																																																									
P3	3	MSRC001_0068	P1	1	MSRC001_0068																																																									
P4	4	MSRC001_0069	P2	2	MSRC001_0069																																																									
P5	5	MSRC001_006A	P3	3	MSRC001_006A																																																									
P6	6	MSRC001_006B	P4	4	MSRC001_006B																																																									
1b	<p>a system control circuit which has a register, wherein said system control circuit carries out the clock frequency transition between said ordinary operation modes and said special modes in response to a change of a value in said register, and also carries out the clock</p>	<p>The Accused Product has a system control circuit, for example, the System Management Unit and/or the System Management Controller, that has a register. See e.g., BKDG:</p> <div data-bbox="790 1094 1244 1360" style="border: 1px solid black; padding: 5px; margin: 10px auto; width: fit-content;"> <p style="text-align: center;">↓</p> <p style="text-align: center;">Northbridge (NB)</p> <ul style="list-style-type: none"> - Transaction routing - Configuration and IO-space registers - Root complex - Graphics core (optional) <p style="text-align: center;">←</p> </div>																																																												

	<u>Limitation</u>	<u>Contention</u>
	<p>frequency transition among said ordinary operation modes in response to said clock control library;</p>	<p>BKDG, section 2.12: 2.12 System Management Unit (SMU)</p> <p>The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details.</p> <p>2.12.1 Microcontroller</p> <p>The SMU contains a microcontroller with a 16k ROM and a 16k RAM.</p> <p>The NB/SMU controls the clock frequency transitions between the core P-states. See e.g., SATHE et al.: RESONANT-CLOCK DESIGN FOR A POWER-EFFICIENT, HIGH-VOLUME X86-64 MICROPROCESSOR, p.144</p> <p>tion of the configuration programming interface. On receiving notification from the NB of a PState transition, the core implements a PState entry sequence which transitions the core into a clock-gated state. A program sequencer then accesses a</p>
1c	<p>a clock generation circuit that receives a plurality of standard clocks, wherein said clock generation circuit generates a clock supplied to said central processing unit according to control by said system control circuit; and</p>	<p>The Accused Products include a digital frequency synthesizer clock generation circuit, including the core PLL, clock multipliers and dividers, and/or the digital frequency synthesizer. The DFS receives a plurality of standard clocks, for example, different phases of the PLL clock or reference clock, and outputs the core clock such as CCLK to the CPU.</p> <p>The Accused Products operate similarly to other product families with regards to this limitation. The clock generator circuit includes at least the PLL and the digital frequency synthesizer. The DFS receives a plurality of standard clocks (the 4 phases-offset references provided by the PLL), and generates CCLK according to control by the SMU:</p>

	<u>Limitation</u>	<u>Contention</u>
	 <p>The diagram illustrates the clock management architecture within the Dynamic Frequency Scaling (DFS) block. A Phase-Locked Loop (PLL) feeds into a Clock Synthesizer. The Clock Synthesizer then distributes clock signals to various system components, including CORE0 CLOCK, CORE1 CLOCK, NORTHBRIDGE CLOCK, and GRAPHICS CLOCKS. A vertical ellipsis indicates that other clocks are also generated.</p>	

	<u>Limitation</u>	<u>Contention</u>
	 <p style="text-align: center;">Fig. 11 DFS clock generation</p> <p>Source: Foley et al., A Low-Power Integrated x86-64 And Graphics Processor For Mobile Computing Devices, Fig. 1., 11; p.224-225.</p>	
1d	<p>a second memory that stores an application program, wherein calling of said clock control library</p>	<p>The Accused Products include a second memory, such as the hierarchy of L1, L2 caches that stores an application program, including but not limited to ACPI drivers, power management utilities, APIs provided by AMD, or any software that causes the SMU/SMC firmware to perform P-state transitions. See BKDG section 2.5.3.1.3; p. 429:</p>

<u>Limitation</u>	<u>Contention</u>						
<p>and changing of said register value are programmably controlled by said application program to enable user selectable clock frequency transitions,</p>	<p>2.5.3.1.3 Core P-state Control</p> <p>Core P-states are dynamically controlled by software and are exposed through ACPI objects (see 2.5.3.1.9 [ACPI Processor P-State Objects]). <u>Software requests a core P-state change by writing a 3 bit index corresponding to the desired non-boosted P-state number to MSRC001_0062 [P-State Control] of the appropriate core.</u> For example, to request P3 for core 0 software would write 011b to core 0's MSRC001_0062[PstateCmd]. Boosted P-states may not be directly requested by software. Whenever software requests the P0 state (i.e. when software writes 000b to MSRC001_0062[PstateCmd]) on a processor that supports CPB, hardware dynamically places that core into the highest-performance P-state possible as determined by CPB. See 2.5.3.1.1 [Core Performance Boost (CPB)].</p> <p>Hardware sequences the frequency and voltage changes necessary to complete a P-state transition as specified by 2.5.3.1.6 [Core P-state Transition Behavior] with no additional software interaction required. Hardware also coordinates frequency and voltage changes when differing P-state requests are made on cores that share a frequency or voltage plane. See 2.5.2 [Frequency and Voltage Domain Dependencies] for details about hardware coordination.</p> <p>MSRC001_0062 P-State Control Register</p> <hr/> <table border="1" data-bbox="728 1036 2134 1338"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>63:3</td> <td>MBZ.</td> </tr> <tr> <td>2:0</td> <td>PstateCmd: P-state change command. Read-write. Reset: Product-specific. <u>Writes to this field cause the core to change to the indicated non-boosted P-state number,</u> specified by MSRC001_00[6B:64]. 0=SWP0, 1=SWP1, etc. P-state limits are applied to any P-state requests made through this register. See 2.5.3.1 [Core P-states] and 2.5.3.1.2.1 [Software P-state Numbering]. Reads from this field return the last written value, regardless of whether any limits are applied.</td> </tr> </tbody> </table>	Bits	Description	63:3	MBZ.	2:0	PstateCmd: P-state change command. Read-write. Reset: Product-specific. <u>Writes to this field cause the core to change to the indicated non-boosted P-state number,</u> specified by MSRC001_00[6B:64]. 0=SWP0, 1=SWP1, etc. P-state limits are applied to any P-state requests made through this register. See 2.5.3.1 [Core P-states] and 2.5.3.1.2.1 [Software P-state Numbering]. Reads from this field return the last written value, regardless of whether any limits are applied.
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	<u>Limitation</u>	<u>Contention</u>
1e	<p>wherein said special modes comprise a first special mode in which clock supply to principal constituents of said central processing unit is halted, a second special mode in which clock supply to an entirety of said central processing unit is halted, and a third special mode in which supply of power to the entirety of said central processing unit is halted.</p>	<p>The Accused Products include a first special mode in which clock supply to principal constituents of said central processing unit is halted, for example the core C6 (CC6) state:</p> <p>2.5.3.2.3.2 Core C6 (CC6) State</p> <p>When a core enters the CC6 state, it executes the following sequence:</p> <ol style="list-style-type: none"> 1. L1 and L2 caches are flushed to DRAM by hardware. 2. Internal core state is saved to DRAM by hardware. 3. The core clock ramps down to the frequency specified by D18F4x1AC[C6Did]. 4. Power is removed from the core if possible as specified by D18F4x1AC[CoreC6Cap] and D18F4x1AC[CoreC6Dis]. <p>The events which cause a core to exit the CC6 state are specified in 2.5.3.2.6 [Exiting C-states].</p> <p>If a warm reset occurs while a core is in CC6, all MCA registers in the core shown in Table 41 are cleared to 0. See 2.16 [Machine Check Architecture].</p> <p><u>D18F4x1AC CPU State Power Management Dynamic Control 1</u></p> <hr/>

<u>Limitation</u>	<u>Contention</u>																																								
	<p data-bbox="760 272 2145 347">9:5 C6Did: CC6 divisor. Read-write. Reset: 0. BIOS: 0Fh. Specifies the divisor applied to the core when ramping clocks down for CC6. See 2.5.3.2.3.2 [Core C6 (CC6) State].</p> <table border="1" data-bbox="854 386 1787 764"> <thead> <tr> <th data-bbox="854 386 916 418"><u>Bits</u></th> <th data-bbox="1005 386 1112 418"><u>Divisor</u></th> <th data-bbox="1486 386 1548 418"><u>Bits</u></th> <th data-bbox="1636 386 1744 418"><u>Divisor</u></th> </tr> </thead> <tbody> <tr> <td data-bbox="854 427 916 459">00h</td> <td data-bbox="1005 427 1112 459">Reserved</td> <td data-bbox="1486 427 1548 459">09h</td> <td data-bbox="1636 427 1744 459">Reserved</td> </tr> <tr> <td data-bbox="854 467 916 500">01h</td> <td data-bbox="1005 467 1112 500">Reserved</td> <td data-bbox="1486 467 1548 500">0Ah</td> <td data-bbox="1636 467 1744 500">Reserved</td> </tr> <tr> <td data-bbox="854 508 916 540">02h</td> <td data-bbox="1005 508 1112 540">Reserved</td> <td data-bbox="1486 508 1548 540">0Bh</td> <td data-bbox="1636 508 1744 540">Reserved</td> </tr> <tr> <td data-bbox="854 548 916 581">03h</td> <td data-bbox="1005 548 1112 581">Reserved</td> <td data-bbox="1486 548 1548 581">0Ch</td> <td data-bbox="1636 548 1744 581">/128</td> </tr> <tr> <td data-bbox="854 589 916 621">04h</td> <td data-bbox="1005 589 1112 621">Reserved</td> <td data-bbox="1486 589 1548 621">0Dh</td> <td data-bbox="1636 589 1744 621">/512</td> </tr> <tr> <td data-bbox="854 630 916 662">05h</td> <td data-bbox="1005 630 1112 662">Reserved</td> <td data-bbox="1486 630 1548 662">0Eh</td> <td data-bbox="1636 630 1744 662">Reserved</td> </tr> <tr> <td data-bbox="854 670 916 703">06h</td> <td data-bbox="1005 670 1112 703">Reserved</td> <td data-bbox="1486 670 1548 703">0Fh</td> <td data-bbox="1636 670 1744 703"><u>Clocks off</u></td> </tr> <tr> <td data-bbox="854 711 916 743">07h</td> <td data-bbox="1005 711 1112 743">Reserved</td> <td data-bbox="1486 711 1548 743">1Fh-10h</td> <td data-bbox="1636 711 1744 743">Reserved</td> </tr> <tr> <td data-bbox="854 751 916 784">08h</td> <td data-bbox="1005 751 1112 784">Reserved</td> <td></td> <td></td> </tr> </tbody> </table> <p data-bbox="841 805 1327 837">See D18F4x1A8[SingleHaltCpuDid].</p> <p data-bbox="715 894 2475 959">The Accused Products include a second special mode in which clock supply to an entirety of said central processing unit is halted, for example the package C1 (PC1) state:</p> <p data-bbox="715 979 1274 1011">2.5.3.2.3.3 Package C1 (PC1) State</p> <p data-bbox="715 1052 1849 1084">The processor enters the PC1 state with auto-Pmin when all of the following are true:</p> <ul data-bbox="774 1130 1327 1162" style="list-style-type: none"> • All cores are in the CC1 state or deeper. <p data-bbox="715 1206 2179 1317">If D18F4x1AC[CstPminEn] indicates that auto-Pmin is enabled when the processor enters PC1, the P-state for all cores is transitioned as specified by 2.5.3.2.7.1 [Auto-Pmin]. Regardless of the state of D18F4x1AC[CstPminEn], all core clocks are ramped to the frequency specified by D18F4x1A8[AllHaltCpuDid].</p>	<u>Bits</u>	<u>Divisor</u>	<u>Bits</u>	<u>Divisor</u>	00h	Reserved	09h	Reserved	01h	Reserved	0Ah	Reserved	02h	Reserved	0Bh	Reserved	03h	Reserved	0Ch	/128	04h	Reserved	0Dh	/512	05h	Reserved	0Eh	Reserved	06h	Reserved	0Fh	<u>Clocks off</u>	07h	Reserved	1Fh-10h	Reserved	08h	Reserved		
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<u>Limitation</u>	<u>Contention</u>																																																							
	<p>D18F4x1A8 CPU State Power Management Dynamic Control 0</p> <p>Reset: 0000_0000h.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 5%; text-align: center;">9:5</td> <td colspan="4">AllHaltCpuDid. Read-write. BIOS: 0Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State]. This field must be set to a divisor deeper than D18F4x1A8[SingleHaltCpuDid] or undefined behavior may result.</td> </tr> <tr> <td></td> <td style="text-align: center;"><u>Bits</u></td> <td style="text-align: center;"><u>Divisor</u></td> <td style="text-align: center;"><u>Bits</u></td> <td style="text-align: center;"><u>Divisor</u></td> </tr> <tr> <td></td> <td style="text-align: center;">00h</td> <td style="text-align: center;">Reserved</td> <td style="text-align: center;">09h</td> <td style="text-align: center;">Reserved</td> </tr> <tr> <td></td> <td style="text-align: center;">01h</td> <td style="text-align: center;">Reserved</td> <td style="text-align: center;">0Ah</td> <td style="text-align: center;">Reserved</td> </tr> <tr> <td></td> <td style="text-align: center;">02h</td> <td style="text-align: center;">Reserved</td> <td style="text-align: center;">0Bh</td> <td style="text-align: center;">Reserved</td> </tr> <tr> <td></td> <td style="text-align: center;">03h</td> <td style="text-align: center;">Reserved</td> <td style="text-align: center;">0Ch</td> <td style="text-align: center;">/128</td> </tr> <tr> <td></td> <td style="text-align: center;">04h</td> <td style="text-align: center;">Reserved</td> <td style="text-align: center;">0Dh</td> <td style="text-align: center;">/512</td> </tr> <tr> <td></td> <td style="text-align: center;">05h</td> <td style="text-align: center;">Reserved</td> <td style="text-align: center;">0Eh</td> <td style="text-align: center;">Reserved</td> </tr> <tr> <td></td> <td style="text-align: center;">06h</td> <td style="text-align: center;">Reserved</td> <td style="text-align: center;"><u>0Fh</u></td> <td style="text-align: center;"><u>Clocks off</u></td> </tr> <tr> <td></td> <td style="text-align: center;">07h</td> <td style="text-align: center;">Reserved</td> <td style="text-align: center;">1Fh-10h</td> <td style="text-align: center;">Reserved</td> </tr> <tr> <td></td> <td style="text-align: center;">08h</td> <td style="text-align: center;">Reserved</td> <td></td> <td></td> </tr> </table> <p style="text-align: right;">2/13/2019</p> <p>The Accused Products include a third special mode in which supply of power to the entirety of said central processing unit is halted, for example the package C6 (PC6) state:</p>	9:5	AllHaltCpuDid. Read-write. BIOS: 0Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State]. This field must be set to a divisor deeper than D18F4x1A8[SingleHaltCpuDid] or undefined behavior may result.					<u>Bits</u>	<u>Divisor</u>	<u>Bits</u>	<u>Divisor</u>		00h	Reserved	09h	Reserved		01h	Reserved	0Ah	Reserved		02h	Reserved	0Bh	Reserved		03h	Reserved	0Ch	/128		04h	Reserved	0Dh	/512		05h	Reserved	0Eh	Reserved		06h	Reserved	<u>0Fh</u>	<u>Clocks off</u>		07h	Reserved	1Fh-10h	Reserved		08h	Reserved		
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<u>Limitation</u>	<u>Contention</u>
	<p>2.5.3.2.3.4 Package C6 (PC6) State</p> <p>The processor enters the PC6 state when all of the following are true:</p> <ul style="list-style-type: none"> • All cores enter the CC6 state. • The C-state action field targeted by each core’s C-state request has the C6Enable bit programmed to indicate entry into PC6 is allowed. See D18F4x118 and D18F4x11C. • PC6 is supported and enabled as specified by D18F4x1AC[PkgC6Cap] and D18F4x1AC[PkgC6Dis]. <p>When the package enters PC6, VDDCR_CPU is transitioned to the VID specified by D18F3x128[C6Vid].</p> <p>2.5.1.4.2 Alternate Low Power Voltages</p> <p>In order to save power, voltages lower than those normally used may be applied to the VDDCR_CPU power plane while the processor is in a C-state.</p> <p>D18F3x128[C6Vid] specifies a VDDCR_CPU voltage that does not retain the CPU caches or the cores’ microarchitectural state, nor allows for execution. As a result, hardware flushes caches and saves the cores’ microarchitectural state to DRAM before transitioning to C6Vid. See 2.5.3.2.3.4 [Package C6 (PC6) State].</p> <p>2.5.1.4.3 Power Gating</p> <p>The processor can remove power from an individual core. This is referred to as power gating. Gating power to a subcomponent causes its internal microarchitectural state and, if applicable, any data in its caches to be lost. When entering a power gated state, hardware saves any needed data, either internally or to DRAM, and flushes caches. When exiting a power gated state, hardware performs any required resets and restores any needed data. See 2.5.3.2.3.2 [Core C6 (CC6) State].</p>

	<u>Limitation</u>	<u>Contention</u>
2p	A system LSI as claimed in claim 1, wherein said clock control library comprises:	
2a	a plurality of libraries that control said system control circuit and said clock generation circuit to transition the clock frequencies supplied to said central processing unit; and	The clock control libraries of the Accused Products contain a plurality of libraries that control the SMU and clock generator to transition clock frequencies. For example, source code provided by AMD to coreboot indicates that P-state and C-state transitions are controlled by separate libraries: https://github.com/coreboot/coreboot/tree/master/src/vendorcode/amd/agesa/f14/Proc/CPU/Feature
2b	a main library which is called by said application program and selects any one of said libraries in correspondence with the clock frequency supplied to said central processing unit.	As discussed above, P-states and C-states may be controlled by software, which includes a main library that calls upon the plurality of libraries.
3p	A system LSI as claimed in claim 2,	
3a	wherein said main library is described using a same program language as said application program.	The main library in the SMU firmware and the application program instructions stored in the caches are both use the same language such as machine code.

	<u>Limitation</u>	<u>Contention</u>
5p	A system LSI as claimed in claim 2,	
5a	wherein each of said libraries is described using a program language capable of directly controlling said clock generation circuit and said system control circuit.	The SMU firmware directly controls the SMU hardware.
6p	A system LSI as claimed in claim 5,	
6a	wherein each of said libraries is described using an assembler language.	The SMU firmware directly controls the SMU hardware and is described using an assembler language such as machine code.
7p	7. A system LSI as claimed in claim 1, wherein said system control circuit comprises:	
7a	a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit;	The NB of the Accused Products contains a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit. The NB contains the configuration register space for the Accused Products. See e.g., BKDG:

<u>Limitation</u>	<u>Contention</u>
	<div data-bbox="790 261 1244 524" style="border: 1px solid black; padding: 5px; margin-bottom: 10px;"> <p style="text-align: center;">↓</p> <p style="text-align: center;">Northbridge (NB)</p> <ul style="list-style-type: none"> - Transaction routing - Configuration and IO-space registers - Root complex - Graphics core (optional) <p style="text-align: right;">←</p> </div> <p>BKDG, section 2.12:</p> <p>2.12 System Management Unit (SMU)</p> <p>The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details.</p> <p>2.12.1 Microcontroller</p> <p>The SMU contains a microcontroller with a 16k ROM and a 16k RAM.</p> <p>Configuration space register mnemonics are defined in section 3.1 of the BKDG:</p> <ul style="list-style-type: none"> • DZFYxXXX: PCI-defined configuration space; XXX specifies the hexadecimal byte address of the configuration register (this may be 2 or 3 digits); Y specifies the function number; Z defined the device number; e.g., D0F3x40 specifies the register of device 0 at function 3, address 40. See 2.7 [Configuration Space], for details about configuration space. <p>the core C1 (CC1) state:</p>

<u>Limitation</u>	<u>Contention</u>												
	<p>2.5.3.2.3.1 Core C1 (CC1) State</p> <p>When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x1A8[SingleHaltCpuDid].</p> <hr/> <p>D18F4x1A8 CPU State Power Management Dynamic Control 0</p> <p>Reset: 0000_0000h.</p> <table border="1" data-bbox="720 565 2171 1084"> <tr> <td data-bbox="728 573 827 602">4:0</td> <td data-bbox="827 573 2163 651"> SingleHaltCpuDid. Read-write. BIOS: 1Eh. On a processor with multiple cores, this specifies the divisor used when ramping core clocks down after a single core has entered the clocks ramped state. </td> </tr> <tr> <td data-bbox="835 651 1032 686"><u>Bits</u></td> <td data-bbox="1032 651 1204 686"><u>Divisor</u></td> </tr> <tr> <td data-bbox="835 686 1032 722">1Ch-00h</td> <td data-bbox="1032 686 1204 722">Reserved.</td> </tr> <tr> <td data-bbox="835 722 1032 758">1Dh</td> <td data-bbox="1032 722 1204 758">128</td> </tr> <tr> <td data-bbox="835 758 1032 794">1Eh</td> <td data-bbox="1032 758 1204 794">512</td> </tr> <tr> <td data-bbox="835 794 1032 829">1Fh</td> <td data-bbox="1032 794 1204 829">Clocks off.</td> </tr> </table> <ul style="list-style-type: none"> • If MSRC001_00[6B:64][CpuDidMSD] of the current P-state is greater than or equal to SingleHaltCpuDid, then no frequency change is made when entering the low-power state associated with this register. • The COF = (the frequency specified by D18F3xD4[MainPllOpFreqId]) / (the divisor specified by this field). 	4:0	SingleHaltCpuDid. Read-write. BIOS: 1Eh. On a processor with multiple cores, this specifies the divisor used when ramping core clocks down after a single core has entered the clocks ramped state.	<u>Bits</u>	<u>Divisor</u>	1Ch-00h	Reserved.	1Dh	128	1Eh	512	1Fh	Clocks off.
4:0	SingleHaltCpuDid. Read-write. BIOS: 1Eh. On a processor with multiple cores, this specifies the divisor used when ramping core clocks down after a single core has entered the clocks ramped state.												
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1Fh	Clocks off.												

<u>Limitation</u>	<u>Contention</u>												
	<p>2.5.3.2.3.3 Package C1 (PC1) State</p> <p>The processor enters the PC1 state with auto-Pmin when all of the following are true:</p> <ul style="list-style-type: none"> • All cores are in the CC1 state or deeper. <p>If D18F4x1AC[CstPminEn] indicates that auto-Pmin is enabled when the processor enters PC1, the P-state for all cores is transitioned as specified by 2.5.3.2.7.1 [Auto-Pmin]. Regardless of the state of D18F4x1AC[CstPminEn], all core clocks are ramped to the frequency specified by D18F4x1A8[AllHaltCpuDid].</p> <p>D18F4x1A8 CPU State Power Management Dynamic Control 0</p> <hr/> <p>Reset: 0000_0000h.</p> <table border="1" data-bbox="720 784 2179 1159"> <tr> <td data-bbox="728 797 827 833">9:5</td> <td data-bbox="827 797 2171 873">AllHaltCpuDid. Read-write. BIOS: 1Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State].</td> </tr> <tr> <td data-bbox="844 878 916 911"><u>Bits</u></td> <td data-bbox="1042 878 1158 911"><u>Divisor</u></td> </tr> <tr> <td data-bbox="844 915 970 948">1Ch-00h</td> <td data-bbox="1042 915 1185 948">Reserved.</td> </tr> <tr> <td data-bbox="844 953 916 985">1Dh</td> <td data-bbox="1042 953 1104 985">128</td> </tr> <tr> <td data-bbox="844 990 916 1023">1Eh</td> <td data-bbox="1042 990 1104 1023">512</td> </tr> <tr> <td data-bbox="844 1027 916 1060">1Fh</td> <td data-bbox="1042 1027 1185 1060">Clocks off.</td> </tr> </table> <p>See D18F4x1A8[SingleHaltCpuDid].</p>	9:5	AllHaltCpuDid. Read-write. BIOS: 1Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State].	<u>Bits</u>	<u>Divisor</u>	1Ch-00h	Reserved.	1Dh	128	1Eh	512	1Fh	Clocks off.
9:5	AllHaltCpuDid. Read-write. BIOS: 1Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State].												
<u>Bits</u>	<u>Divisor</u>												
1Ch-00h	Reserved.												
1Dh	128												
1Eh	512												
1Fh	Clocks off.												

	<u>Limitation</u>	<u>Contention</u>																																																							
7b	a clock halting register that receives the clock from said clock generation circuit and individually sets the clock to be halted or supplied;	<p>2.5.3.2.3.3 Package C1 (PC1) State</p> <p>The processor enters the PC1 state with auto-Pmin when all of the following are true:</p> <ul style="list-style-type: none"> All cores are in the CC1 state or deeper. <p>If D18F4x1AC[CstPminEn] indicates that auto-Pmin is enabled when the processor enters PC1, the P-state for all cores is transitioned as specified by 2.5.3.2.7.1 [Auto-Pmin]. Regardless of the state of D18F4x1AC[CstPminEn], all core clocks are ramped to the frequency specified by D18F4x1A8[AllHaltCpuDid].</p> <p>D18F4x1A8 CPU State Power Management Dynamic Control 0</p> <hr/> <p>Reset: 0000_0000h.</p> <table border="1" data-bbox="720 792 2214 1377"> <tr> <td data-bbox="747 808 827 841">9:5</td> <td colspan="4" data-bbox="835 808 2198 922">AllHaltCpuDid. Read-write. BIOS: 0Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State]. This field must be set to a divisor deeper than D18F4x1A8[SingleHaltCpuDid] or undefined behavior may result.</td> </tr> <tr> <td></td> <td data-bbox="835 971 916 1003"><u>Bits</u></td> <td data-bbox="1005 971 1131 1003"><u>Divisor</u></td> <td data-bbox="1516 971 1596 1003"><u>Bits</u></td> <td data-bbox="1669 971 1795 1003"><u>Divisor</u></td> </tr> <tr> <td></td> <td>00h</td> <td>Reserved</td> <td>09h</td> <td>Reserved</td> </tr> <tr> <td></td> <td>01h</td> <td>Reserved</td> <td>0Ah</td> <td>Reserved</td> </tr> <tr> <td></td> <td>02h</td> <td>Reserved</td> <td>0Bh</td> <td>Reserved</td> </tr> <tr> <td></td> <td>03h</td> <td>Reserved</td> <td>0Ch</td> <td>/128</td> </tr> <tr> <td></td> <td>04h</td> <td>Reserved</td> <td>0Dh</td> <td>/512</td> </tr> <tr> <td></td> <td>05h</td> <td>Reserved</td> <td>0Eh</td> <td>Reserved</td> </tr> <tr> <td></td> <td>06h</td> <td>Reserved</td> <td><u>0Fh</u></td> <td><u>Clocks off</u></td> </tr> <tr> <td></td> <td>07h</td> <td>Reserved</td> <td>1Fh-10h</td> <td>Reserved</td> </tr> <tr> <td></td> <td>08h</td> <td>Reserved</td> <td></td> <td></td> </tr> </table>	9:5	AllHaltCpuDid. Read-write. BIOS: 0Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State]. This field must be set to a divisor deeper than D18F4x1A8[SingleHaltCpuDid] or undefined behavior may result.					<u>Bits</u>	<u>Divisor</u>	<u>Bits</u>	<u>Divisor</u>		00h	Reserved	09h	Reserved		01h	Reserved	0Ah	Reserved		02h	Reserved	0Bh	Reserved		03h	Reserved	0Ch	/128		04h	Reserved	0Dh	/512		05h	Reserved	0Eh	Reserved		06h	Reserved	<u>0Fh</u>	<u>Clocks off</u>		07h	Reserved	1Fh-10h	Reserved		08h	Reserved		
9:5	AllHaltCpuDid. Read-write. BIOS: 0Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State]. This field must be set to a divisor deeper than D18F4x1A8[SingleHaltCpuDid] or undefined behavior may result.																																																								
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	01h	Reserved	0Ah	Reserved																																																					
	02h	Reserved	0Bh	Reserved																																																					
	03h	Reserved	0Ch	/128																																																					
	04h	Reserved	0Dh	/512																																																					
	05h	Reserved	0Eh	Reserved																																																					
	06h	Reserved	<u>0Fh</u>	<u>Clocks off</u>																																																					
	07h	Reserved	1Fh-10h	Reserved																																																					
	08h	Reserved																																																							

2/13/2019

	<u>Limitation</u>	<u>Contention</u>
7c	<p>And a status register that judges a state of said central processing unit immediately after being released from said third special mode.</p>	<p>2.5.3.2.7.2 Exiting PC6</p> <p>If the PService timer is enabled when the processor exits PC6, all cores transition to the P-state specified by <u>D18F4x1AC[PstateIdCoreOffExit]</u>. The cores remain in this state until one of the following occurs:</p> <ul style="list-style-type: none"> • The PService timer expires while the package is in C0: In this case, the cores transition back to the last P-state requested by software. • The package enters PC1 without auto-Pmin: In this case, the PService timer continues counting. If it expires while in PC1, the cores remain in the P-state specified by D18F4x1AC[PstateIdCoreOffExit] until they return to C0, at which time they transition to the last P-state requested by software. • The package enters PC1 with auto-Pmin: In this case, the PService timer stops counting and the cores enter the PService state. • The package enters PC6: In this case the PService timer stops counting and the actions associated the requested package C-state occur. See 2.5.3.2.3.4 [Package C6 (PC6) State]. <p>If the PService timer is disabled when the processor exits PC6, the cores transition back to the last P-state requested by software.</p> <p>See also BKDG pp.320-321:</p> <p><u>D18F4x1AC CPU State Power Management Dynamic Control 1</u></p> <hr/>

	<u>Limitation</u>	<u>Contention</u>		
		<table border="1"> <tr> <td data-bbox="720 261 854 623">18:16</td> <td data-bbox="854 261 2483 623"> PstateIdCoreOffExit. Read-write. Reset: 0. BIOS: 2.5.3.2.9. When exiting the package C6 state, the core transitions to the P-state specified by this register. See 2.5.3.2.7.2 [Exiting PC6]. If PC6 is enabled (see 2.5.3.2.9 [BIOS Requirements for C-state Initialization]), PstateIdCoreOffExit must be programmed to lowest-performance P-state displayed to the operating system or to any lower-performance P-state. Programming this field to 0 causes the core to transition to the last P-state requested by software when exiting package C6. This field uses hardware P-state numbering. See 2.5.3.1.2.2 [Hardware P-state Numbering]. </td> </tr> </table>	18:16	PstateIdCoreOffExit. Read-write. Reset: 0. BIOS: 2.5.3.2.9. When exiting the package C6 state, the core transitions to the P-state specified by this register. See 2.5.3.2.7.2 [Exiting PC6]. If PC6 is enabled (see 2.5.3.2.9 [BIOS Requirements for C-state Initialization]), PstateIdCoreOffExit must be programmed to lowest-performance P-state displayed to the operating system or to any lower-performance P-state. Programming this field to 0 causes the core to transition to the last P-state requested by software when exiting package C6. This field uses hardware P-state numbering. See 2.5.3.1.2.2 [Hardware P-state Numbering].
18:16	PstateIdCoreOffExit. Read-write. Reset: 0. BIOS: 2.5.3.2.9. When exiting the package C6 state, the core transitions to the P-state specified by this register. See 2.5.3.2.7.2 [Exiting PC6]. If PC6 is enabled (see 2.5.3.2.9 [BIOS Requirements for C-state Initialization]), PstateIdCoreOffExit must be programmed to lowest-performance P-state displayed to the operating system or to any lower-performance P-state. Programming this field to 0 causes the core to transition to the last P-state requested by software when exiting package C6. This field uses hardware P-state numbering. See 2.5.3.1.2.2 [Hardware P-state Numbering].			
10p	A system LSI as claimed in claim 1,			
10a	wherein said first memory and said second memory are two independent memories which are separated from each other.	As detailed above, the first memory in the SMU and the second memory in the caches are independent memories that are separated from each other.		

**Exhibit C.1 – Preliminary Accused Product Identification for '614 Patent –
AMD Family 12h Processors**

This identification of products is based on information reasonably available to Polaris, and was prepared without the benefit of discovery from AMD. Accordingly, this chart may not include non-public AMD products such as OEM or custom products. Aquila reserves the right to modify or supplement its identification of Accused Products when AMD provides more information.

Model	Family	Line	uArch
641	AMD Athlon Processors	AMD Athlon II X4	Llano
638	AMD Athlon Processors	AMD Athlon II X4	Llano
631	AMD Athlon Processors	AMD Athlon II X4	Llano
631	AMD Athlon Processors	AMD Athlon II X4	Llano
620e	AMD Athlon Processors	AMD Athlon II X4	Llano
E2-3000M	AMD E-Series Processors		Llano
A4-3300M	AMD A-Series Processors		Llano
A4-3305M	AMD A-Series Processors		Llano
A4-3310MX	AMD A-Series Processors		Llano
A4-3320M	AMD A-Series Processors		Llano
A4-3330MX	AMD A-Series Processors		Llano
A6-3400M	AMD A-Series Processors		Llano
A6-3410MX	AMD A-Series Processors		Llano
A6-3420M	AMD A-Series Processors		Llano
A6-3430MX	AMD A-Series Processors		Llano
A8-3500M	AMD A-Series Processors		Llano
A8-3510MX	AMD A-Series Processors		Llano
A8-3520M	AMD A-Series Processors		Llano
A8-3530MX	AMD A-Series Processors		Llano
A8-3550MX	AMD A-Series Processors		Llano
Sempron X2 198	AMD Sempron Processors		Llano
Athlon II X2 221	AMD Athlon Processors		Llano
Athlon II X4 651	AMD Athlon Processors		Llano
Athlon II X4 651K	AMD Athlon Processors		Llano
E2-3200	AMD E-Series Processors		Llano
A4-3300	AMD A-Series Processors		Llano
A4-3400	AMD A-Series Processors		Llano
A4-3420	AMD A-Series Processors		Llano

Model	Family	Line	uArch
A6-3500	AMD A-Series Processors		Llano
A6-3600	AMD A-Series Processors		Llano
A6-3620	AMD A-Series Processors		Llano
A6-3650	AMD A-Series Processors		Llano
A6-3670K	AMD A-Series Processors		Llano
A8-3800	AMD A-Series Processors		Llano
A8-3820	AMD A-Series Processors		Llano
A8-3850	AMD A-Series Processors		Llano
A8-3870K	AMD A-Series Processors		Llano

**Exhibit C.2 – Preliminary Accused Product Identification for '614 Patent –
AMD Bulldozer/Piledriver Processors**

This identification of products is based on information reasonably available to Polaris, and was prepared without the benefit of discovery from AMD. Accordingly, this chart may not include non-public AMD products such as OEM or custom products. Aquila reserves the right to modify or supplement its identification of Accused Products when AMD provides more information.

Model	Family	Line	uArch
A10-6800B with Radeon HD 8670D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6800K with Radeon HD 8670D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6790K with Radeon HD 8670D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6790B	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6700 with Radeon HD 8670D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6700T with Radeon HD 8650D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-5800K	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-5700	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A8-6600K with Radeon HD 8570D	AMD A-Series Processors	AMD A8-Series APU for Desktops	Piledriver
A8-6500B	AMD A-Series Processors	AMD A8-Series APU for Desktops	Piledriver
A8-6500 with Radeon HD 8570D	AMD A-Series Processors	AMD A8-Series APU for Desktops	Piledriver
A8-6500T with Radeon HD 8550D	AMD A-Series Processors	AMD A8-Series APU for Desktops	Piledriver
A6-6420K with Radeon HD 8470D	AMD A-Series Processors	AMD A6-Series APU for Desktops	Piledriver
A6-6400K with Radeon HD 8470D	AMD A-Series Processors	AMD A6-Series APU for Desktops	Piledriver
A6-5400K	AMD A-Series Processors	AMD A6-Series APU for Desktops	Piledriver
A4-7300 with Radeon HD 8470D	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-6320B	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver

Model	Family	Line	uArch
A4-6320 with Radeon HD 8370D	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-6300	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-6300B	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-6300 with Radeon HD 8370D	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
FX-9590	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-9370	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8370 with Wraith cooler	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8370E	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8370	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8350 with Wraith cooler	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8350	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8320E	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8320	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8310	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8300	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8170	AMD FX-Series Processors		Bulldozer
FX-8150	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Bulldozer
FX-8140	AMD FX-Series Processors		Bulldozer
FX-8120	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Bulldozer
FX-8100	AMD FX-Series Processors		Bulldozer
FX-6350 with Wraith cooler	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Piledriver

Model	Family	Line	uArch
A4-4020	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-4000	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A8-7200P with Radeon R5 Graphics	AMD A-Series Processors	AMD A8-Series APU for Laptops	Piledriver
FX-6350	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Piledriver
FX-6300	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Piledriver
FX-6200	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Bulldozer
FX-6130	AMD FX-Series Processors		Bulldozer
FX-6120	AMD FX-Series Processors		Bulldozer
FX 6100	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Bulldozer
FX-4350	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Piledriver
FX-4320	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Piledriver
FX-4300	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Piledriver
FX-4170	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Bulldozer
FX-4150	AMD FX-Series Processors		Bulldozer
FX-4130	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Bulldozer
FX-4120	AMD FX-Series Processors		Bulldozer
FX-4100	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Bulldozer
A6-5350M with Radeon HD 8450G	AMD A-Series Processors	AMD A6-Series APU for Laptops	Piledriver
A10-6800B with Radeon HD 8670D	AMD A-Series Processors	AMD Business Class - Quad-Core A10-Series APU for Desktops	Piledriver
A10-6790B with Radeon HD 8670D	AMD A-Series Processors	AMD Business Class - Quad-Core A10-Series APU for Desktops	Piledriver

Model	Family	Line	uArch
A8-6500B with Radeon HD 8570D	AMD A-Series Processors	AMD Business Class - Quad-Core A8-Series APU for Desktops	Piledriver
760K	AMD Athlon Processors	AMD Athlon X4	Piledriver
750	AMD Athlon Processors	AMD Athlon X4	Piledriver
A6-6420B with Radeon HD 8470D	AMD A-Series Processors	AMD Business Class - Dual-Core A6-Series APU for Desktops	Piledriver
750K	AMD Athlon Processors	AMD Athlon X4	Piledriver
A6-6400B with Radeon HD 8470D	AMD A-Series Processors	AMD Business Class - Dual-Core A6-Series APU for Desktops	Piledriver
740	AMD Athlon Processors	AMD Athlon X4	Piledriver
6386 SE	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6380	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6378	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6376	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6370P	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6366 HE	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6348	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
A4 PRO-7300B with Radeon HD 8470D	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Desktops	Piledriver
6344	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6338P	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6328	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6320	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6308	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver

Model	Family	Line	uArch
6287 SE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6284 SE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6282 SE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6278	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6276	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6274	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6272	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6262 HE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6230 HE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6238	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6234	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6220	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6212	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6204	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
4386	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
43GK HE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4376 HE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4365	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4340	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4334	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4332 HE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
43CX EE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver

Model	Family	Line	uArch
4310 EE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4284	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4280	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4276 HE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4274 HE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
42MX EE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4256 EE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4240	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4238	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4234	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4230 HE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4228 HE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4226	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
42DX EE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
3380	AMD Opteron	AMD Opteron 3300 Series Processor	Piledriver
3365	AMD Opteron	AMD Opteron 3300 Series Processor	Piledriver
3350 HE	AMD Opteron	AMD Opteron 3300 Series Processor	Piledriver
3320 EE	AMD Opteron	AMD Opteron 3300 Series Processor	Piledriver
3280	AMD Opteron	AMD Opteron 3200 Series Processor	Bulldozer
3260 HE	AMD Opteron	AMD Opteron 3200 Series Processor	Bulldozer
3250 HE	AMD Opteron	AMD Opteron 3200 Series Processor	Bulldozer

Model	Family	Line	uArch
R-252F	AMD Embedded R-Series Processors		Piledriver
R-260H	AMD Embedded R-Series Processors		Piledriver
R-268D	AMD Embedded R-Series Processors		Piledriver
R-272F	AMD Embedded R-Series Processors		Piledriver
R-452L	AMD Embedded R-Series Processors		Piledriver
R-460H	AMD Embedded R-Series Processors		Piledriver
R-460L	AMD Embedded R-Series Processors		Piledriver
R-464L	AMD Embedded R-Series Processors		Piledriver
A10-5750M	AMD A-Series Processors		Piledriver
A10-4600M	AMD A-Series Processors		Piledriver
A8-5550M	AMD A-Series Processors		Piledriver
A8-4500M	AMD A-Series Processors		Piledriver
A6-5350M	AMD A-Series Processors		Piledriver
A6-4400M	AMD A-Series Processors		Piledriver
A4-5150M	AMD A-Series Processors		Piledriver
A4-4300M	AMD A-Series Processors		Piledriver
A10-5757M	AMD A-Series Processors		Piledriver
A10-5745M	AMD A-Series Processors		Piledriver
A10-4655M	AMD A-Series Processors		Piledriver
A8-5557M	AMD A-Series Processors		Piledriver
A8-5545M	AMD A-Series Processors		Piledriver
A8-4555M	AMD A-Series		Piledriver

Model	Family	Line	uArch
	Processors		
A6-5357M	AMD A-Series Processors		Piledriver
A6-5345M	AMD A-Series Processors		Piledriver
A6-4455M	AMD A-Series Processors		Piledriver
A4-5145M	AMD A-Series Processors		Piledriver
A4-4355M	AMD A-Series Processors		Piledriver

**Exhibit C.3 – Preliminary Accused Product Identification for '614 Patent –
AMD Excavator(+) Processors**

This identification of products is based on information reasonably available to Polaris, and was prepared without the benefit of discovery from AMD. Accordingly, this chart may not include non-public AMD products such as OEM or custom products. Aquila reserves the right to modify or supplement its identification of Accused Products when AMD provides more information.

Model	Family	Line	uArch
7th Gen AMD PRO A4-4350B APU	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Laptops	Excavator+
7th Gen AMD PRO A6-7350B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Excavator+
7th Gen A12 9800 APU	AMD A-Series Processors	AMD A12-Series APU for Desktops	Excavator+
7th Gen A12 9800E APU	AMD A-Series Processors	AMD A12-Series APU for Desktops	Excavator+
7th Gen A12 9720P APU	AMD A-Series Processors	AMD A10-Series APU for Desktops	Excavator+
7th Gen A10 9700 APU	AMD A-Series Processors	AMD A10-Series APU for Desktops	Excavator+
7th Gen A10 9700E APU	AMD A-Series Processors	AMD A10-Series APU for Desktops	Excavator+
7th Gen A10-9620P APU	AMD A-Series Processors	AMD A10-Series APU for Laptops	Excavator+
7th Gen A8 9600 APU	AMD A-Series Processors	AMD A8-Series APU for Desktops	Excavator+
7th Gen A6 9550 APU	AMD A-Series Processors	AMD A6-Series APU for Desktops	Excavator+
7th Gen A6 9500 APU	AMD A-Series Processors	AMD A6-Series APU for Desktops	Excavator+
7th Gen A6 9500E APU	AMD A-Series Processors	AMD A6-Series APU for Desktops	Excavator+
7th Gen A12-9730P APU	AMD A-Series Processors	AMD A12-Series APU for Laptops	Excavator+
7th Gen A12-9700P APU	AMD A-Series Processors	AMD A12-Series APU for Laptops	Excavator+
7th Gen A10-9630P APU	AMD A-Series Processors	AMD A10-Series APU for Laptops	Excavator+
7th Gen A10-9600P APU	AMD A-Series Processors	AMD A10-Series APU for Laptops	Excavator+
7th Gen A9-9425 APU	AMD A-Series Processors	AMD A9-Series APU for Laptops	Excavator+
7th Gen A9 9420 APU	AMD A-Series	AMD A9-Series APU	Excavator+

Model	Family	Line	uArch
	Processors	for Laptops	
7th Gen A9 9410 APU	AMD A-Series Processors	AMD A9-Series APU for Laptops	Excavator+
7th Gen A6-9225 APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6 9220 APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6-9220C APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6 9210 APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6-9200 APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6 9200e APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A4-9120 APU	AMD A-Series Processors	AMD A4-Series APU for Laptops	Excavator+
7th Gen A49120C APU	AMD A-Series Processors	AMD A4-Series APU for Laptops	Excavator+
7th Gen AMD PRO A12-9800 APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Desktops	Excavator+
7th Gen AMD PRO A12-9800E APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Desktops	Excavator+
7th Gen AMD PRO A10-9700 APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Excavator+
7th Gen AMD PRO A10-9700E APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Excavator+
7th Gen AMD PRO A8-9600 APU	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Desktops	Excavator+
7th Gen AMD PRO A6-9500 APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator+
7th Gen AMD PRO A6-9500E APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator+
7th Gen AMD PRO A12-9830B APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Laptops	Excavator+
7th Gen AMD PRO A12-9800B APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Laptops	Excavator+
7th Gen AMD PRO A10-9730B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator+

Model	Family	Line	uArch
7th Gen AMD PRO A10-9700B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator+
7th Gen AMD PRO A8-9630B	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Laptops	Excavator+
7th Gen AMD PRO A8-9600B APU	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Laptops	Excavator+
7th Gen AMD PRO A6-9500B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Excavator+
7th Gen FX 9830P APU	AMD FX-Series Processors	AMD FX-Series Processors for Laptops	Excavator+
7th Gen FX 9800P APU	AMD FX-Series Processors	AMD FX-Series Processors for Laptops	Excavator+
7th Gen E2 9010 APU	AMD E-Series Processors	AMD E2-Series APU for Laptops	Excavator+
6th Gen A10-8700P APU	AMD A-Series Processors	AMD A10-Series APU for Laptops	Excavator
6th Gen A8-8600P APU	AMD A-Series Processors	AMD A8-Series APU for Laptops	Excavator
6th Gen AMD PRO A12-8870 APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Desktops	Excavator
6th Gen AMD PRO A12-8870E APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Desktops	Excavator
6th Gen AMD PRO A10-8770 APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Excavator
6th Gen AMD PRO A10-8770E APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Excavator
6th Gen AMD PRO A8-8650B APU	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Desktops	Excavator
6th Gen AMD PRO A6-8570 APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator
6th Gen AMD PRO A6-8570E APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator
6th Gen AMD PRO A6-8550B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator
6th Gen AMD PRO A4-8350B APU	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Desktops	Excavator
6th Gen AMD PRO A12-	AMD PRO A-Series	AMD PRO A-Series	Excavator

Model	Family	Line	uArch
8830B APU	Processors	A12 APU for Laptops	
6th Gen AMD PRO A12-8800B APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Laptops	Excavator
6th Gen AMD PRO A10-8780P APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator
6th Gen AMD PRO A10-8730B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator
6th Gen AMD PRO A10-8700B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator
6th Gen AMD PRO A8-8600B APU	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Laptops	Excavator
6th Gen AMD PRO A6-8530B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Excavator
6th Gen AMD PRO A6-8500B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Excavator
6th Gen FX-8800P APU	AMD FX-Series Processors	AMD FX-Series Processors for Laptops	Excavator
A6-8500P with Radeon R5 Graphics	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator
A10-8700P with Radeon R6 Graphics	AMD A-Series Processors	AMD A10-Series APU for AIOs	Excavator
7th Gen AMD Athlon X4 970	AMD Athlon Processors	AMD Athlon X4	Excavator
A8-8600P with Radeon R6 Graphics	AMD A-Series Processors	AMD A8-Series APU for AIOs	Excavator
7th Gen AMD Athlon X4 950	AMD Athlon Processors	AMD Athlon X4	Excavator
7th Gen AMD Athlon X4 940	AMD Athlon Processors	AMD Athlon X4	Excavator
A6-8500P with Radeon R5 Graphics	AMD A-Series Processors	AMD A6-Series APU for AIOs	Excavator
835	AMD Athlon Processors	AMD Athlon X4	Excavator
845 with Near Silent Thermal Solution	AMD Athlon Processors	AMD Athlon X4	Excavator
FX-8800P with Radeon R7 Graphics	AMD FX-Series Processors	AMD FX-Series Processors for AIOs	Excavator
RX-421ND	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-421BD	AMD Embedded R-Series Processors	R-Series SOC	Excavator

Model	Family	Line	uArch
RX-418GD	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-416GD	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-216TD	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-216GD	AMD Embedded R-Series Processors	R-Series SOC	Excavator
GX-224IJ	AMD Embedded G-Series Processors	3rd Generation G-Series SOC J Family	Excavator
GX-215JJ	AMD Embedded G-Series Processors	3rd Generation G-Series SOC J Family	Excavator
GX-217GI	AMD Embedded G-Series Processors	3rd Generation G-Series SOC I Family	Excavator
GX-420GI	AMD Embedded G-Series Processors		Excavator
GX-212JJ	AMD Embedded G-Series Processors		Excavator
GX-220IJ	AMD Embedded G-Series Processors		Excavator
X3216	AMD Opteron	AMD Opteron X3000-series	Excavator
X3418	AMD Opteron	AMD Opteron X3000-series	Excavator
X3421	AMD Opteron	AMD Opteron X3000-series	Excavator
Athlon X4 835	AMD Athlon Processors		Excavator
Athlon X4 845	AMD Athlon Processors		Excavator

**Exhibit D.1 – Preliminary Accused Product Identification for '519 Patent –
AMD Family 12h Processors**

This identification of products is based on information reasonably available to Polaris, and was prepared without the benefit of discovery from AMD. Accordingly, this chart may not include non-public AMD products such as OEM or custom products. Aquila reserves the right to modify or supplement its identification of Accused Products when AMD provides more information.

Model	Family	Line	uArch
641	AMD Athlon Processors	AMD Athlon II X4	Llano
638	AMD Athlon Processors	AMD Athlon II X4	Llano
631	AMD Athlon Processors	AMD Athlon II X4	Llano
631	AMD Athlon Processors	AMD Athlon II X4	Llano
620e	AMD Athlon Processors	AMD Athlon II X4	Llano
E2-3000M	AMD E-Series Processors		Llano
A4-3300M	AMD A-Series Processors		Llano
A4-3305M	AMD A-Series Processors		Llano
A4-3310MX	AMD A-Series Processors		Llano
A4-3320M	AMD A-Series Processors		Llano
A4-3330MX	AMD A-Series Processors		Llano
A6-3400M	AMD A-Series Processors		Llano
A6-3410MX	AMD A-Series Processors		Llano
A6-3420M	AMD A-Series Processors		Llano
A6-3430MX	AMD A-Series Processors		Llano
A8-3500M	AMD A-Series Processors		Llano
A8-3510MX	AMD A-Series Processors		Llano
A8-3520M	AMD A-Series Processors		Llano
A8-3530MX	AMD A-Series Processors		Llano
A8-3550MX	AMD A-Series Processors		Llano
Sempron X2 198	AMD Sempron Processors		Llano
Athlon II X2 221	AMD Athlon Processors		Llano
Athlon II X4 651	AMD Athlon Processors		Llano
Athlon II X4 651K	AMD Athlon Processors		Llano
E2-3200	AMD E-Series Processors		Llano
A4-3300	AMD A-Series Processors		Llano
A4-3400	AMD A-Series Processors		Llano
A4-3420	AMD A-Series Processors		Llano

Model	Family	Line	uArch
A6-3500	AMD A-Series Processors		Llano
A6-3600	AMD A-Series Processors		Llano
A6-3620	AMD A-Series Processors		Llano
A6-3650	AMD A-Series Processors		Llano
A6-3670K	AMD A-Series Processors		Llano
A8-3800	AMD A-Series Processors		Llano
A8-3820	AMD A-Series Processors		Llano
A8-3850	AMD A-Series Processors		Llano
A8-3870K	AMD A-Series Processors		Llano

**Exhibit D.2 – Preliminary Accused Product Identification for '519 Patent –
AMD Family 14h Processors**

This identification of products is based on information reasonably available to Polaris, and was prepared without the benefit of discovery from AMD. Accordingly, this chart may not include non-public AMD products such as OEM or custom products. Aquila reserves the right to modify or supplement its identification of Accused Products when AMD provides more information.

Model	Family	uArch
G-Series T24L	AMD Embedded G-Series Processors	Bobcat
G-Series T30L	AMD Embedded G-Series Processors	Bobcat
G-Series T48L	AMD Embedded G-Series Processors	Bobcat
G-Series T16R	AMD Embedded G-Series Processors	Bobcat
G-Series T40R	AMD Embedded G-Series Processors	Bobcat
G-Series T40E	AMD Embedded G-Series Processors	Bobcat
G-Series T40N	AMD Embedded G-Series Processors	Bobcat
G-Series T40R	AMD Embedded G-Series Processors	Bobcat
G-Series T44R	AMD Embedded G-Series Processors	Bobcat
G-Series T48E	AMD Embedded G-Series Processors	Bobcat
G-Series T48N	AMD Embedded G-Series Processors	Bobcat
G-Series T52R	AMD Embedded G-Series Processors	Bobcat
G-Series T56E	AMD Embedded G-Series Processors	Bobcat
G-Series T56N	AMD Embedded G-Series Processors	Bobcat
C-50	C-Series	Bobcat
C-60	C-Series	Bobcat
C-70	C-Series	Bobcat
E-240	AMD E-Series Processors	Bobcat
E-300	AMD E-Series Processors	Bobcat

Model	Family	uArch
E-350	AMD E-Series Processors	Bobcat
E-450	AMD E-Series Processors	Bobcat
E1-1200	AMD E-Series Processors	Bobcat
E1-1500[23]	AMD E-Series Processors	Bobcat
E2-1800	AMD E-Series Processors	Bobcat
E2-2000[23]	AMD E-Series Processors	Bobcat
Z-01	Z-Series	Bobcat
Z-60[24]	Z-Series	Bobcat

**Exhibit D.3 – Preliminary Accused Product Identification for '519 Patent –
AMD Family 15h Processors**

This identification of products is based on information reasonably available to Polaris, and was prepared without the benefit of discovery from AMD. Accordingly, this chart may not include non-public AMD products such as OEM or custom products. Aquila reserves the right to modify or supplement its identification of Accused Products when AMD provides more information.

Model	Family	Line	uArch
7th Gen AMD PRO A4-4350B APU	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Laptops	Excavator+
7th Gen AMD PRO A6-7350B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Excavator+
7th Gen A12 9800 APU	AMD A-Series Processors	AMD A12-Series APU for Desktops	Excavator+
7th Gen A12 9800E APU	AMD A-Series Processors	AMD A12-Series APU for Desktops	Excavator+
7th Gen A12 9720P APU	AMD A-Series Processors	AMD A10-Series APU for Desktops	Excavator+
7th Gen A10 9700 APU	AMD A-Series Processors	AMD A10-Series APU for Desktops	Excavator+
7th Gen A10 9700E APU	AMD A-Series Processors	AMD A10-Series APU for Desktops	Excavator+
7th Gen A10-9620P APU	AMD A-Series Processors	AMD A10-Series APU for Laptops	Excavator+
7th Gen A8 9600 APU	AMD A-Series Processors	AMD A8-Series APU for Desktops	Excavator+
7th Gen A6 9550 APU	AMD A-Series Processors	AMD A6-Series APU for Desktops	Excavator+
7th Gen A6 9500 APU	AMD A-Series Processors	AMD A6-Series APU for Desktops	Excavator+
7th Gen A6 9500E APU	AMD A-Series Processors	AMD A6-Series APU for Desktops	Excavator+
7th Gen A12-9730P APU	AMD A-Series Processors	AMD A12-Series APU for Laptops	Excavator+
7th Gen A12-9700P APU	AMD A-Series Processors	AMD A12-Series APU for Laptops	Excavator+
7th Gen A10-9630P APU	AMD A-Series Processors	AMD A10-Series APU for Laptops	Excavator+
7th Gen A10-9600P APU	AMD A-Series Processors	AMD A10-Series APU for Laptops	Excavator+
7th Gen A9-9425	AMD A-Series	AMD A9-Series APU for	Excavator+

Model	Family	Line	uArch
APU	Processors	Laptops	
7th Gen A9 9420 APU	AMD A-Series Processors	AMD A9-Series APU for Laptops	Excavator+
7th Gen A9 9410 APU	AMD A-Series Processors	AMD A9-Series APU for Laptops	Excavator+
7th Gen A6-9225 APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6 9220 APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6-9220C APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6 9210 APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6-9200 APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6 9200e APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A4-9120 APU	AMD A-Series Processors	AMD A4-Series APU for Laptops	Excavator+
7th Gen A49120C APU	AMD A-Series Processors	AMD A4-Series APU for Laptops	Excavator+
7th Gen AMD PRO A12-9800 APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Desktops	Excavator+
7th Gen AMD PRO A12-9800E APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Desktops	Excavator+
7th Gen AMD PRO A10-9700 APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Excavator+
7th Gen AMD PRO A10-9700E APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Excavator+
7th Gen AMD PRO A8-9600 APU	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Desktops	Excavator+
7th Gen AMD PRO A6-9500 APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator+
7th Gen AMD PRO A6-9500E APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator+
7th Gen AMD PRO A12-9830B	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Laptops	Excavator+

Model	Family	Line	uArch
APU			
7th Gen AMD PRO A12-9800B APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Laptops	Excavator+
7th Gen AMD PRO A10-9730B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator+
7th Gen AMD PRO A10-9700B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator+
7th Gen AMD PRO A8-9630B	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Laptops	Excavator+
7th Gen AMD PRO A8-9600B APU	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Laptops	Excavator+
7th Gen AMD PRO A6-9500B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Excavator+
7th Gen FX 9830P APU	AMD FX-Series Processors	AMD FX-Series Processors for Laptops	Excavator+
7th Gen FX 9800P APU	AMD FX-Series Processors	AMD FX-Series Processors for Laptops	Excavator+
7th Gen E2 9010 APU	AMD E-Series Processors	AMD E2-Series APU for Laptops	Excavator+
6th Gen A10-8700P APU	AMD A-Series Processors	AMD A10-Series APU for Laptops	Excavator
6th Gen A8-8600P APU	AMD A-Series Processors	AMD A8-Series APU for Laptops	Excavator
6th Gen AMD PRO A12-8870 APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Desktops	Excavator
6th Gen AMD PRO A12-8870E APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Desktops	Excavator
6th Gen AMD PRO A10-8850B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Steamroller
6th Gen AMD PRO A10-8770 APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Excavator
6th Gen AMD PRO A10-8770E APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Excavator

Model	Family	Line	uArch
6th Gen AMD PRO A10-8750B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Steamroller
6th Gen AMD PRO A8-8650B APU	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Desktops	Excavator
6th Gen AMD PRO A6-8570 APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator
6th Gen AMD PRO A6-8570E APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator
6th Gen AMD PRO A6-8550B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator
6th Gen AMD PRO A4-8350B APU	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Desktops	Excavator
6th Gen AMD PRO A12-8830B APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Laptops	Excavator
6th Gen AMD PRO A12-8800B APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Laptops	Excavator
6th Gen AMD PRO A10-8780P APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator
6th Gen AMD PRO A10-8730B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator
6th Gen AMD PRO A10-8700B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator
6th Gen AMD PRO A8-8600B APU	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Laptops	Excavator
6th Gen AMD PRO A6-8530B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Excavator
6th Gen AMD PRO A6-8500B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Excavator
6th Gen FX-8800P APU	AMD FX-Series Processors	AMD FX-Series Processors for Laptops	Excavator

Model	Family	Line	uArch
A10-7890K with Radeon R7 Graphics and Wraith cooler	AMD A-Series Processors	AMD A10-Series APU for Desktops	Steamroller
A10-7870K with Radeon R7 Series	AMD A-Series Processors	AMD A10-Series APU for Desktops	Steamroller
A10-7870K with Radeon R7 Graphics and Near Silent Thermal Solution	AMD A-Series Processors	AMD A10-Series APU for Desktops	Steamroller
A10-7860K with Radeon R7 Series	AMD A-Series Processors	AMD A10-Series APU for Desktops	Steamroller
A10-7860K with Radeon R7 Graphics and Near Silent Thermal Solution	AMD A-Series Processors	AMD A10-Series APU for Desktops	Steamroller
A10-7850K with Radeon R7 Series	AMD A-Series Processors	AMD A10-Series APU for Desktops	Steamroller
A10-7800 with Radeon R7 Series	AMD A-Series Processors	AMD A10-Series APU for Desktops	Steamroller
A10-7700K with Radeon R7 Series	AMD A-Series Processors	AMD A10-Series APU for Desktops	Steamroller
A10-6800B with Radeon HD 8670D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6800K with Radeon HD 8670D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6790K with Radeon HD 8670D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6790B	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6700 with Radeon HD 8670D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6700T with Radeon HD 8650D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A8-7670K with Radeon R7 Graphics and	AMD A-Series Processors	AMD A8-Series APU for Desktops	Steamroller

Model	Family	Line	uArch
Near Silent Thermal Solution			
A8-7650K with Radeon R7 Series	AMD A-Series Processors	AMD A8-Series APU for Desktops	Steamroller
A8-7650K with Radeon R7 Graphics and Near Silent Thermal Solution	AMD A-Series Processors	AMD A8-Series APU for Desktops	Steamroller
A8-7600 with Radeon R7 Series	AMD A-Series Processors	AMD A8-Series APU for Desktops	Steamroller
A10-5800K	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-5700	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A8-6600K with Radeon HD 8570D	AMD A-Series Processors	AMD A8-Series APU for Desktops	Piledriver
A8-6500B	AMD A-Series Processors	AMD A8-Series APU for Desktops	Piledriver
A8-6500 with Radeon HD 8570D	AMD A-Series Processors	AMD A8-Series APU for Desktops	Piledriver
A8-6500T with Radeon HD 8550D	AMD A-Series Processors	AMD A8-Series APU for Desktops	Piledriver
A6-7470K with Radeon R5 Series	AMD A-Series Processors	AMD A6-Series APU for Desktops	Steamroller
A6-7400K with Radeon R5 Series	AMD A-Series Processors	AMD A6-Series APU for Desktops	Steamroller
A6-6420K with Radeon HD 8470D	AMD A-Series Processors	AMD A6-Series APU for Desktops	Piledriver
A6-6400K with Radeon HD 8470D	AMD A-Series Processors	AMD A6-Series APU for Desktops	Piledriver
A6-5400K	AMD A-Series Processors	AMD A6-Series APU for Desktops	Piledriver
A4-7300 with Radeon HD 8470D	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-6320B	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver

Model	Family	Line	uArch
A4-6320 with Radeon HD 8370D	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-6300	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-6300B	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-6300 with Radeon HD 8370D	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
FX-9590	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-9370	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8370 with Wraith cooler	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8370E	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
A10-7400P with Radeon R6 Graphics	AMD A-Series Processors	AMD A10-Series APU for Laptops	Steamroller
FX-8370	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
A10-7300 with Radeon R6 Graphics	AMD A-Series Processors	AMD A10-Series APU for Laptops	Steamroller
FX-8350 with Wraith cooler	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8350	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8320E	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8320	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8310	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8300	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8170	AMD FX-Series Processors		Bulldozer
FX-8150	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Bulldozer
FX-8140	AMD FX-Series		Bulldozer

Model	Family	Line	uArch
	Processors		
FX-8120	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Bulldozer
FX-8100	AMD FX-Series Processors		Bulldozer
FX-6350 with Wraith cooler	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Piledriver
A4-4020	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-4000	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A8-7200P with Radeon R5 Graphics	AMD A-Series Processors	AMD A8-Series APU for Laptops	Piledriver
FX-6350	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Piledriver
A8-7100 with Radeon R5 Graphics	AMD A-Series Processors	AMD A8-Series APU for Laptops	Steamroller
FX-6300	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Piledriver
FX-6200	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Bulldozer
FX-6130	AMD FX-Series Processors		Bulldozer
FX-6120	AMD FX-Series Processors		Bulldozer
FX 6100	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Bulldozer
FX-4350	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Piledriver
FX-4320	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Piledriver
FX-4300	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Piledriver
FX-4170	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Bulldozer
FX-4150	AMD FX-Series Processors		Bulldozer
FX-4130	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Bulldozer
FX-4120	AMD FX-Series Processors		Bulldozer

Model	Family	Line	uArch
FX-4100	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Bulldozer
A6-8500P with Radeon R5 Graphics	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator
A6-7000 with Radeon R4 Graphics	AMD A-Series Processors	AMD A6-Series APU for Laptops	Steamroller
A6-5350M with Radeon HD 8450G	AMD A-Series Processors	AMD A6-Series APU for Laptops	Piledriver
A10-8700P with Radeon R6 Graphics	AMD A-Series Processors	AMD A10-Series APU for AIOs	Excavator
7th Gen AMD Athlon X4 970	AMD Athlon Processors	AMD Athlon X4	Excavator
A8-8600P with Radeon R6 Graphics	AMD A-Series Processors	AMD A8-Series APU for AIOs	Excavator
7th Gen AMD Athlon X4 950	AMD Athlon Processors	AMD Athlon X4	Excavator
7th Gen AMD Athlon X4 940	AMD Athlon Processors	AMD Athlon X4	Excavator
A6-8500P with Radeon R5 Graphics	AMD A-Series Processors	AMD A6-Series APU for AIOs	Excavator
830	AMD Athlon Processors	AMD Athlon X4	Steamroller
840	AMD Athlon Processors	AMD Athlon X4	Steamroller
880K with Near Silent Thermal Solution	AMD Athlon Processors	AMD Athlon X4	Steamroller
870K with Near Silent Thermal Solution	AMD Athlon Processors	AMD Athlon X4	Steamroller
860K	AMD Athlon Processors	AMD Athlon X4	Steamroller
A10-6800B with Radeon HD 8670D	AMD A-Series Processors	AMD Business Class - Quad-Core A10-Series APU for Desktops	Piledriver
860K with Near Silent Thermal Solution	AMD Athlon Processors	AMD Athlon X4	Steamroller
A10-6790B with Radeon HD	AMD A-Series Processors	AMD Business Class - Quad-Core A10-Series APU for	Piledriver

Model	Family	Line	uArch
8670D		Desktops	
835	AMD Athlon Processors	AMD Athlon X4	Excavator
845 with Near Silent Thermal Solution	AMD Athlon Processors	AMD Athlon X4	Excavator
A8-6500B with Radeon HD 8570D	AMD A-Series Processors	AMD Business Class - Quad-Core A8-Series APU for Desktops	Piledriver
760K	AMD Athlon Processors	AMD Athlon X4	Piledriver
750	AMD Athlon Processors	AMD Athlon X4	Piledriver
A6-6420B with Radeon HD 8470D	AMD A-Series Processors	AMD Business Class - Dual-Core A6-Series APU for Desktops	Piledriver
750K	AMD Athlon Processors	AMD Athlon X4	Piledriver
A6-6400B with Radeon HD 8470D	AMD A-Series Processors	AMD Business Class - Dual-Core A6-Series APU for Desktops	Piledriver
740	AMD Athlon Processors	AMD Athlon X4	Piledriver
6386 SE	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6380	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
A10 PRO-7850B with Radeon R7 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Steamroller
6378	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6376	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
A10 PRO-7800B with Radeon R7 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Steamroller
A8 PRO-7600B with Radeon R7 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Desktops	Steamroller
6370P	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
A6 PRO-7400B with Radeon R5 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Steamroller
6366 HE	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver

Model	Family	Line	uArch
A4 PRO-7350B with Radeon R5 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Desktops	Steamroller
6348	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
A4 PRO-7300B with Radeon HD 8470D	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Desktops	Piledriver
6344	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
A10 PRO-7350B with Radeon R6 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Steamroller
6338P	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6328	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
A8 PRO-7150B with Radeon R5 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Laptops	Steamroller
6320	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
A6 PRO-7050B with Radeon R4 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Steamroller
6308	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6287 SE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6284 SE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
FX-7600P with Radeon R7 Graphics	AMD FX-Series Processors	AMD FX-Series Processors for Laptops	Steamroller
6282 SE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
FX-7500 with Radeon R7 Graphics	AMD FX-Series Processors	AMD FX-Series Processors for Laptops	Steamroller
6278	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6276	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer

Model	Family	Line	uArch
FX-8800P with Radeon R7 Graphics	AMD FX-Series Processors	AMD FX-Series Processors for AIOs	Excavator
6274	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6272	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6262 HE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6230 HE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6238	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6234	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6220	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6212	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6204	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
4386	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
43GK HE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4376 HE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4365	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4340	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4334	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4332 HE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
43CX EE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4310 EE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4284	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4280	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4276 HE	AMD Opteron	AMD Opteron 4200 Series	Bulldozer

Model	Family	Line	uArch
		Processor	
4274 HE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
42MX EE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4256 EE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4240	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4238	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4234	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4230 HE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4228 HE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4226	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
42DX EE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
3380	AMD Opteron	AMD Opteron 3300 Series Processor	Piledriver
3365	AMD Opteron	AMD Opteron 3300 Series Processor	Piledriver
3350 HE	AMD Opteron	AMD Opteron 3300 Series Processor	Piledriver
3320 EE	AMD Opteron	AMD Opteron 3300 Series Processor	Piledriver
3280	AMD Opteron	AMD Opteron 3200 Series Processor	Bulldozer
3260 HE	AMD Opteron	AMD Opteron 3200 Series Processor	Bulldozer
3250 HE	AMD Opteron	AMD Opteron 3200 Series Processor	Bulldozer
RX-421ND	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-421BD	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-418GD	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-416GD	AMD Embedded R-Series Processors	R-Series SOC	Excavator

Model	Family	Line	uArch
RX-216TD	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-216GD	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-427NB	AMD Embedded R-Series Processors	2nd Generation R-Series APU	Steamroller
RX-427BB	AMD Embedded R-Series Processors	2nd Generation R-Series APU	Steamroller
RX-425BB	AMD Embedded R-Series Processors	2nd Generation R-Series APU	Steamroller
RX-225FB	AMD Embedded R-Series Processors	2nd Generation R-Series APU	Steamroller
RX-219NB	AMD Embedded R-Series Processors	2nd Generation R-Series APU	Steamroller
GX-224IJ	AMD Embedded G-Series Processors	3rd Generation G-Series SOC J Family	Excavator
GX-215JJ	AMD Embedded G-Series Processors	3rd Generation G-Series SOC J Family	Excavator
GX-217GI	AMD Embedded G-Series Processors	3rd Generation G-Series SOC I Family	Excavator
GX-420GI	AMD Embedded G-Series Processors		Excavator
GX-212JJ	AMD Embedded G-Series Processors		Excavator
GX-220IJ	AMD Embedded G-Series Processors		Excavator
R-252F	AMD Embedded R-Series Processors		Piledriver
R-260H	AMD Embedded R-Series Processors		Piledriver
R-268D	AMD Embedded R-Series Processors		Piledriver
R-272F	AMD Embedded R-Series Processors		Piledriver
R-452L	AMD Embedded R-Series Processors		Piledriver
R-460H	AMD Embedded R-Series Processors		Piledriver
R-460L	AMD Embedded R-Series Processors		Piledriver

Model	Family	Line	uArch
R-464L	AMD Embedded R-Series Processors		Piledriver
X3216	AMD Opteron	AMD Operton X3000-series	Excavator
X3418	AMD Opteron	AMD Operton X3000-series	Excavator
X3421	AMD Opteron	AMD Operton X3000-series	Excavator
A10-5750M	AMD A-Series Processors		Piledriver
A10-4600M	AMD A-Series Processors		Piledriver
A8-5550M	AMD A-Series Processors		Piledriver
A8-4500M	AMD A-Series Processors		Piledriver
A6-5350M	AMD A-Series Processors		Piledriver
A6-4400M	AMD A-Series Processors		Piledriver
A4-5150M	AMD A-Series Processors		Piledriver
A4-4300M	AMD A-Series Processors		Piledriver
A10-5757M	AMD A-Series Processors		Piledriver
A10-5745M	AMD A-Series Processors		Piledriver
A10-4655M	AMD A-Series Processors		Piledriver
A8-5557M	AMD A-Series Processors		Piledriver
A8-5545M	AMD A-Series Processors		Piledriver
A8-4555M	AMD A-Series Processors		Piledriver
A6-5357M	AMD A-Series Processors		Piledriver
A6-5345M	AMD A-Series Processors		Piledriver
A6-4455M	AMD A-Series Processors		Piledriver
A4-5145M	AMD A-Series		Piledriver

Model	Family	Line	uArch
	Processors		
A4-4355M	AMD A-Series Processors		Piledriver
Athlon X2 450	AMD Athlon Processors		Steamroller
Athlon X4 830	AMD Athlon Processors		Steamroller
Athlon X4 840	AMD Athlon Processors		Steamroller
Athlon X4 860K	AMD Athlon Processors		Steamroller
Athlon X4 870K	AMD Athlon Processors		Steamroller
Athlon X4 880K	AMD Athlon Processors		Steamroller
Athlon X4 835	AMD Athlon Processors		Excavator
Athlon X4 845	AMD Athlon Processors		Excavator

**Exhibit D.4 – Preliminary Accused Product Identification for '519 Patent –
AMD 16h Product Family**

This identification of products is based on information reasonably available to Polaris, and was prepared without the benefit of discovery from AMD. Accordingly, this chart may not include non-public AMD products such as OEM or custom products. Aquila reserves the right to modify or supplement its identification of Accused Products when AMD provides more information.

Model	Family	Line	uArch
A6-6310 with Radeon R4 Graphics	AMD A-Series Processors	AMD A6-Series APU for Desktops	Jaguar+
A6-5200 with Radeon HD 8400	AMD A-Series Processors	AMD A6-Series APU for Desktops	Jaguar
A4-5100 with Radeon HD 8330	AMD A-Series Processors	AMD A4-Series APU for Desktops	Jaguar
A4-5000 with Radeon HD 8330	AMD A-Series Processors	AMD A4-Series APU for Desktops	Jaguar
A10 Micro-6700T with Radeon R6 Graphics	AMD A-Series Processors	AMD A10-Series APU for Laptops	Jaguar+
A6 Micro 6500T	AMD A-Series Processors		Jaguar+
A8-7410 with Radeon R5 Graphics	AMD A-Series Processors	AMD A8-Series APU for Laptops	Jaguar+
A8-6410 with Radeon R5 Graphics	AMD A-Series Processors	AMD A8-Series APU for Laptops	Jaguar+
A6-7310 with Radeon R4 Graphics	AMD A-Series Processors	AMD A6-Series APU for Laptops	Jaguar+
A6-6310 with Radeon R4 Graphics	AMD A-Series Processors	AMD A6-Series APU for Laptops	Jaguar+
A6-5200M with Radeon HD 8400	AMD A-Series Processors	AMD A6-Series APU for Laptops	Jaguar
A4-7210 with Radeon R3 Graphics	AMD A-Series Processors	AMD A4-Series APU for Laptops	Jaguar+
A4 Micro-6400T with Radeon R3 Graphics	AMD A-Series Processors	AMD A4-Series APU for Laptops	Jaguar+
A4-6210 with Radeon R3 Graphics	AMD A-Series Processors	AMD A4-Series APU for Laptops	Jaguar+
A4-5100 with Radeon HD 8330	AMD A-Series Processors	AMD A4-Series APU for Laptops	Jaguar
A4-5000 with Radeon HD 8330	AMD A-Series Processors	AMD A4-Series APU for Laptops	Jaguar
A4-6250J	AMD A-Series Processors		Jaguar+

Model	Family	Line	uArch
A6-6310	AMD A-Series Processors		Jaguar+
A8-6410 with Radeon R5 Graphics	AMD A-Series Processors	AMD A8-Series APU for AIOs	Jaguar+
A6-7310 with Radeon R4 Graphics	AMD A-Series Processors	AMD A6-Series APU for AIOs	Jaguar+
A4-7210 with Radeon R3 Graphics	AMD A-Series Processors	AMD A4-Series APU for AIOs	Jaguar+
X1150	AMD Opteron	AMD Opteron X1100 Series Processors	Jaguar
A4 PRO-3350B with Radeon R4 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Laptops	Jaguar+
A4 PRO-3340B with Radeon HD 8240 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Laptops	Jaguar
Athlon 5370 APU with Radeon R3 Series	AMD Athlon Processors	AMD Athlon Quad-Core APU	Jaguar
Athlon 5350 APU with Radeon R3 Series	AMD Athlon Processors	AMD Athlon Quad-Core APU	Jaguar
Athlon 5150 APU with Radeon R3 Series	AMD Athlon Processors	AMD Athlon Quad-Core APU	Jaguar
Sempron 3850 APU with Radeon R3 Series	AMD Sempron	AMD Sempron Quad-Core APU	Jaguar
Sempron 2650 APU with Radeon R3 Series	AMD Sempron	AMD Sempron Dual-Core APU	Jaguar
E2-7110 with Radeon R2 Graphics	AMD E-Series Processors	AMD E2-Series APU for Laptops	Jaguar+
E2-7110 with Radeon R2 Graphics	AMD E-Series Processors	AMD E2-Series APU for Laptops	Jaguar+
E2-6110 with Radeon R2 Graphics	AMD E-Series Processors	AMD E2-Series APU for Laptops	Jaguar+
E2-3800 with Radeon HD 8280	AMD E-Series Processors	AMD E2-Series APU for Laptops	Jaguar
E2-3000 with Radeon HD 8280	AMD E-Series Processors	AMD E2-Series APU for Laptops	Jaguar
E2-7110 with Radeon R2 Graphics	AMD E-Series Processors	AMD E2-Series APU for AIOs	Jaguar+
E1-7010 with Radeon R2 Graphics	AMD E-Series Processors	AMD E1-Series APU for Laptops	Jaguar+
E1 Micro-6200T with Radeon R2 Graphics	AMD E-Series Processors	AMD E1-Series APU for Laptops	Jaguar+
E1-6010 with Radeon R2 Graphics	AMD E-Series Processors	AMD E1-Series APU for Laptops	Jaguar+

Model	Family	Line	uArch
E1-6015	AMD E-Series Processors	AMD E1-Series APU for Laptops	Jaguar+
E1-2500 with Radeon HD 8240	AMD E-Series Processors	AMD E1-Series APU for Laptops	Jaguar
E1-2200 with Radeon HD 8210	AMD E-Series Processors	AMD E1-Series APU for Laptops	Jaguar
E1-2100 with Radeon HD 8210	AMD E-Series Processors	AMD E1-Series APU for Laptops	Jaguar
E1-7010 with Radeon R2 Graphics	AMD E-Series Processors	AMD E1-Series APU for AIOs	Jaguar
AMD Opteron X2170	AMD Opteron	AMD Opteron X2100 Series APU	Jaguar
AMD Opteron X2150 APU	AMD Opteron	AMD Opteron X2100 Series APU	Jaguar
GX-424CC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-420MC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-412TC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-412HC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-410VC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-224PC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-222GC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-216HC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-212JC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-210JC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-420CA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-416RA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-415GA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-411GA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar

Model	Family	Line	uArch
GX-218TF	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-217GA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-210UA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-210JA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-210HA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-209HA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-208VF	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-218GL	AMD Embedded G-Series Processors	G-Series LX SOC	Jaguar+
GX-215GL	AMD Embedded G-Series Processors	G-Series LX SOC	Jaguar+
GX-210KL	AMD Embedded G-Series Processors	G-Series LX SOC	Jaguar+
GX-210HL	AMD Embedded G-Series Processors	G-Series LX SOC	Jaguar+
GX-216HC	AMD Embedded G-Series Processors		Jaguar+
GX-222GC	AMD Embedded G-Series Processors		Jaguar+
GX-424CC	AMD Embedded G-Series Processors		Jaguar+
GX-208JL	AMD Embedded G-Series Processors		Jaguar+
GX-210HL	AMD Embedded G-Series Processors		Jaguar+
GX-210JL	AMD Embedded G-Series Processors		Jaguar+
A6-1450	AMD A-Series Processors		Jaguar
A4-1350	AMD A-Series Processors		Jaguar
A4-1250	AMD A-Series Processors		Jaguar
A4-1200	AMD A-Series Processors		Jaguar

Model	Family	Line	uArch
Playstation 4 APU			Jaguar
Playstation 4 Slim APU			Jaguar
Playstation 4 Pro APU			Jaguar
Xbox One APU			Jaguar
Xbox One S APU			Jaguar
Xbox one X APU			Jaguar

**Exhibit D.5 – Preliminary Accused Product Identification for '519 Patent –
Products Containing Zen or Zen+ Cores**

This identification of products is based on information reasonably available to Polaris, and was prepared without the benefit of discovery from AMD. Accordingly, this chart may not include non-public AMD products such as OEM or custom products. Aquila reserves the right to modify or supplement its identification of Accused Products when AMD provides more information.

Model	Family	Line	uArch
AMD Athlon 240GE	AMD Athlon Processors	AMD Athlon Desktop Processors with Radeon Vega Graphics	Zen
AMD Athlon 220GE	AMD Athlon Processors	AMD Athlon Desktop Processors with Radeon Vega Graphics	Zen
AMD Athlon 200GE	AMD Athlon Processors	AMD Athlon Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 7 3750H	AMD Ryzen Processors	AMD Ryzen 7 Mobile Processors with Radeon RX Vega Graphics	Zen+
AMD Ryzen 7 3700U	AMD Ryzen Processors	AMD Ryzen 7 Mobile Processors with Radeon RX Vega Graphics	Zen+
AMD Ryzen 5 3550H	AMD Ryzen Processors	AMD Ryzen 5 Mobile Processors with Radeon Vega Graphics	Zen+
AMD Ryzen 5 3500U	AMD Ryzen Processors	AMD Ryzen 5 Mobile Processors with Radeon Vega Graphics	Zen+
AMD Ryzen 3 3300U	AMD Ryzen Processors	AMD Ryzen 3 Mobile Processors with Radeon Vega Graphics	Zen+
AMD Ryzen 3 3200U	AMD Ryzen Processors	AMD Ryzen 3 Mobile Processors with Radeon Vega Graphics	Zen+
AMD Athlon 300U	AMD Athlon Processors	AMD Athlon Mobile Processors with Radeon Vega Graphics	Zen
AMD Ryzen Threadripper 2990WX	AMD Ryzen Processors	AMD Ryzen Threadripper Processors	Zen+
AMD Ryzen Threadripper	AMD Ryzen Processors	AMD Ryzen Threadripper Processors	Zen+

Model	Family	Line	uArch
2970WX			
AMD Ryzen Threadripper 2950X	AMD Ryzen Processors	AMD Ryzen Threadripper Processors	Zen+
AMD Ryzen Threadripper 2920X	AMD Ryzen Processors	AMD Ryzen Threadripper Processors	Zen+
AMD Ryzen 7 2700X	AMD Ryzen Processors	AMD Ryzen 7 Desktop Processors	Zen+
AMD Ryzen 7 2700	AMD Ryzen Processors	AMD Ryzen 7 Desktop Processors	Zen+
AMD Ryzen 7 2700E Processor	AMD Ryzen Processors	AMD Ryzen 7 Desktop Processors	Zen+
AMD Ryzen 5 2600X	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors	Zen+
AMD Ryzen 5 2600	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors	Zen+
AMD Ryzen 5 2600E	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors	Zen+
AMD Ryzen 5 2500X	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors	Zen+
AMD Ryzen 5 2400G with Radeon RX Vega 11 Graphics	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 5 2400GE with Radeon RX Vega 11 Graphics	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 3 2300X	AMD Ryzen Processors	AMD Ryzen 3 Desktop Processors	Zen+
AMD Ryzen 3 2200G with Radeon Vega 8 Graphics	AMD Ryzen Processors	AMD Ryzen 3 Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 3 2200GE with Radeon Vega 8 Graphics	AMD Ryzen Processors	AMD Ryzen 3 Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 7 2800H	AMD Ryzen Processors	AMD Ryzen 7 Mobile Processors with Radeon RX Vega Graphics	Zen
AMD Ryzen 5 2600H	AMD Ryzen Processors	AMD Ryzen 5 Mobile Processors with Radeon Vega	Zen

Model	Family	Line	uArch
		Graphics	
AMD Ryzen 7 2700U	AMD Ryzen Processors	AMD Ryzen 7 Mobile Processors with Radeon RX Vega Graphics	Zen
AMD Ryzen 5 2500U	AMD Ryzen Processors	AMD Ryzen 5 Mobile Processors with Radeon Vega Graphics	Zen
AMD Ryzen 3 2300U	AMD Ryzen Processors	AMD Ryzen 3 Mobile Processors with Radeon Vega Graphics	Zen
AMD Ryzen 3 2200U	AMD Ryzen Processors	AMD Ryzen 3 Mobile Processors with Radeon Vega Graphics	Zen
AMD Ryzen Threadripper 1950X	AMD Ryzen Processors	AMD Ryzen Threadripper Processors	Zen
AMD Ryzen Threadripper 1920X	AMD Ryzen Processors	AMD Ryzen Threadripper Processors	Zen
AMD Ryzen Threadripper 1900X	AMD Ryzen Processors	AMD Ryzen Threadripper Processors	Zen
AMD Ryzen 7 1800X	AMD Ryzen Processors	AMD Ryzen 7 Desktop Processors	Zen
AMD Ryzen 7 1700X	AMD Ryzen Processors	AMD Ryzen 7 Desktop Processors	Zen
AMD Ryzen 7 1700 Processor	AMD Ryzen Processors	AMD Ryzen 7 Desktop Processors	Zen
AMD Ryzen 5 1600X	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors	Zen
AMD Ryzen 5 1600	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors	Zen
AMD Ryzen 5 1500X	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors	Zen
AMD Ryzen 5 1400	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors	Zen
AMD Ryzen 3 1300X	AMD Ryzen Processors	AMD Ryzen 3 Desktop Processors	Zen
AMD Ryzen 3 1200	AMD Ryzen Processors	AMD Ryzen 3 Desktop Processors	Zen
AMD Ryzen 7 PRO 2700X	AMD Ryzen PRO Processors	AMD Ryzen 7 PRO Desktop Processors	Zen+
AMD Ryzen 7	AMD Ryzen PRO	AMD Ryzen 7 PRO Desktop	Zen+

Model	Family	Line	uArch
PRO 2700	Processors	Processors	
AMD Ryzen 7 PRO 1700X Processor	AMD Ryzen PRO Processors	AMD Ryzen 7 PRO Desktop Processors	Zen
AMD Ryzen 7 PRO 1700	AMD Ryzen PRO Processors	AMD Ryzen 7 PRO Desktop Processors	Zen
AMD Ryzen 5 PRO 2600	AMD Ryzen PRO Processors	AMD Ryzen 5 PRO Desktop Processors	Zen+
AMD Ryzen 5 PRO 1600	AMD Ryzen PRO Processors	AMD Ryzen 5 PRO Desktop Processors	Zen
AMD Ryzen 5 PRO 1500	AMD Ryzen PRO Processors	AMD Ryzen 5 PRO Desktop Processors	Zen
AMD Ryzen 7 PRO 2700U	AMD Ryzen PRO Processors	AMD Ryzen 7 PRO Mobile Processors with Radeon Vega Graphics	Zen
AMD Ryzen 5 PRO 2400G with Radeon Vega 11 Graphics	AMD Ryzen PRO Processors	AMD Ryzen 5 PRO Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 5 PRO 2400GE with Radeon Vega 11 Graphics	AMD Ryzen PRO Processors	AMD Ryzen 5 PRO Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 3 PRO 1300	AMD Ryzen PRO Processors	AMD Ryzen 3 PRO Desktop Processors	Zen
AMD Ryzen 5 PRO 2500U	AMD Ryzen PRO Processors	AMD Ryzen 5 PRO Mobile Processors with Radeon Vega Graphics	Zen
AMD Ryzen 3 PRO 2200G with Radeon Vega 8 Graphics	AMD Ryzen PRO Processors	AMD Ryzen 3 PRO Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 3 PRO 2200GE with Radeon Vega 8 Graphics	AMD Ryzen PRO Processors	AMD Ryzen 3 PRO Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 3 PRO 1200	AMD Ryzen PRO Processors	AMD Ryzen 3 PRO Desktop Processors	Zen
AMD Ryzen 3 PRO 2300U	AMD Ryzen PRO Processors	AMD Ryzen 3 PRO Mobile Processors with Radeon Vega Graphics	Zen
AMD EPYC 7601	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7551P	AMD EPYC	AMD EPYC 7000 Series	Zen

Model	Family	Line	uArch
AMD EPYC 7551	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7501	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7451	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7401P	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7401	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7351P	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7351	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7301	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7281	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7261	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7251	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD Athlon 240GE	AMD Athlon Processors	AMD Athlon Desktop Processors with Radeon Vega Graphics	Zen
AMD Athlon 220GE	AMD Athlon Processors	AMD Athlon Desktop Processors with Radeon Vega Graphics	Zen
AMD Athlon 200GE	AMD Athlon Processors	AMD Athlon Desktop Processors with Radeon Vega Graphics	Zen
AMD Athlon PRO 200GE	AMD Athlon PRO Processors	AMD Athlon PRO Desktop Processors with Radeon Vega Graphics	Zen
AMD EPYC Embedded 3251	AMD EPYC Embedded Processors	EPYC Embedded SOC	Zen
AMD EPYC Embedded 3201	AMD EPYC Embedded Processors	EPYC Embedded SOC	Zen
AMD EPYC Embedded 3151	AMD EPYC Embedded Processors	EPYC Embedded SOC	Zen
AMD EPYC Embedded 3101	AMD EPYC Embedded Processors	EPYC Embedded SOC	Zen
AMD Ryzen Embedded V1807B	AMD Ryzen Embedded V-series Processors	V-Series V1000	Zen
AMD Ryzen Embedded V1756B	AMD Ryzen Embedded V-series Processors	V-Series V1000	Zen
AMD Ryzen Embedded V1605B	AMD Ryzen Embedded V-series Processors	V-Series V1000	Zen

Model	Family	Line	uArch
AMD Ryzen Embedded V1202B	AMD Ryzen Embedded V-series Processors	V-Series V1000	Zen
V1202B	Ryzen Embedded		Zen
V1605B	Ryzen Embedded		Zen
V1756B	Ryzen Embedded		Zen
V1807B	Ryzen Embedded		Zen
3101	Epyc Embedded		Zen
3151	Epyc Embedded		Zen
3201	Epyc Embedded		Zen
3251	Epyc Embedded		Zen
3301	Epyc Embedded		Zen
3351	Epyc Embedded		Zen
3401	Epyc Embedded		Zen
3451	Epyc Embedded		Zen