ARM920T

(Rev 1)

Technical Reference Manual





ARM920T

Technical Reference Manual

Copyright © 2000, 2001 ARM Limited. All rights reserved.

Release Information

Change history

Date	Issue Change	
31st January 2000	A	First release
5th September 2000	В	Second release
18th April 2001	С	Third release

Proprietary Notice

Words and logos marked with ® or ™ are registered trademarks or trademarks owned by ARM Limited, except as otherwise stated below in this proprietary notice. Other brands and names mentioned herein may be the trademarks of their respective owners.

Neither the whole nor any part of the information contained in, or the product described in, this document may be adapted or reproduced in any material form except with the prior written permission of the copyright holder.

The product described in this document is subject to continuous developments and improvements. All particulars of the product and its use contained in this document are given by ARM in good faith. However, all warranties implied or expressed, including but not limited to implied warranties of merchantability, or fitness for purpose, are excluded.

This document is intended only to assist the reader in the use of the product. ARM Limited shall not be liable for any loss or damage arising from the use of any information in this document, or any error or omission in such information, or any incorrect use of the product.

Figure 9-5 on page 9-12 reprinted with permission IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture Copyright 2000, by IEEE. The IEEE disclaims any responsibility or liability resulting from the placement and use in the described manner

Confidentiality Status

This document is Non-Confidential. The right to use, copy and disclose this document may be subject to license restrictions in accordance with the terms of the agreement entered into by ARM and the party that ARM delivered this document to.

Product Status

The information in this document is final, that is for a developed product.

Web Address

http://www.arm.com



Contents

ARM920T Technical Reference Manual

	Pref	ace	
		About this document	xvi
		Further reading	xix
		Feedback	xx
Chapter 1	Introduction		
•	1.1	About the ARM920T	1-2
	1.2	Processor functional block diagram	
Chapter 2	Programmer's Model		
•	2.1	About the programmer's model	2-2
	2.2	About the ARM9TDMI programmer's model	
	2.3	CP15 register map summary	
Chapter 3	Memory Management Unit		
•	3.1	About the MMU	3-2
	3.2	MMU program accessible registers	
	3.3	Address translation	
	3.4	MMU faults and CPU aborts	3-21
	3.5	Fault address and fault status registers	
	3.6	Domain access control	
	3.7	Fault checking sequence	3-25



Contents

	3.8	External aborts	3-28		
	3.9	Interaction of the MMU and caches	3-29		
Chapter 4	Caches, Write Buffer, and Physical Address TAG (PA TAG) F				
•	4.1	About the caches and write buffer			
	4.2	ICache			
	4.3	DCache and write buffer	4-9		
	4.4	Cache coherence	4-16		
	4.5	Cache cleaning when lockdown is in use	4-19		
	4.6	Implementation notes			
	4.7	Physical address TAG RAM	4-21		
	4.8	Drain write buffer	4-22		
	4.9	Wait for interrupt	4-23		
Chapter 5	Cloc	ck Modes			
•	5.1	About ARM920T clocking	5-2		
	5.2	FastBus mode			
	5.3	Synchronous mode			
	5.4	Asynchronous mode			
Chapter 6	Bus Interface Unit				
	6.1	About the ARM920T bus interface	6-2		
	6.2	Unidirectional AMBA ASB interface	_		
	6.3	Fully-compliant AMBA ASB interface			
	6.4	AMBA AHB interface			
	6.5	Level 2 cache support and performance analysis			
Chapter 7	Coprocessor Interface				
onapion .	7.1	About the ARM920T coprocessor interface	7-2		
	7.2	LDC/STC			
	7.3	MCR/MRC			
	7.4	Interlocked MCR	_		
	7.5	CDP			
	7.6	Privileged instructions			
	7.7	Busy-waiting and interrupts			
Chapter 8	Trace Interface Port				
onapioi o	8.1	About the ETM interface	8-2		
Chapter 9	Deb	ug Support			
Unapier 3	9.1	About debug	0.2		
	9.1	Debug systems			
	9.2	Debug systems Debug interface signals			
	9.3 9.4	Scan chains and JTAG interface			
	9.4	The JTAG state machine			
	9.6	Test data registers			
	9.0	rost data registers	9-19		



Contents

	9.7	ARM9201 core clocks		
	9.8	Clock switching during debug		
	9.9	Clock switching during test		
	9.10	Determining the core state and system state		
	9.11	Exit from debug state		
	9.12	The behavior of the program counter during debug		
	9.13	EmbeddedICE macrocell	9-53	
	9.14	Vector catching		
	9.15	Single-stepping		
	9.16	Debug communications channel	9-62	
Chapter 10	TrackingICE			
	10.1	About TrackingICE	10-2	
	10.2	Timing requirements	10-3	
	10.3	TrackingICE outputs	10-4	
Chapter 11	AMB	A Test Interface		
•	11.1	About the AMBA test interface	11-2	
	11.2	Entering and exiting AMBA Test		
	11.3	Functional test		
	11.4	Burst operations		
	11.5	PA TAG RAM test	11-12	
	11.6	Cache test	11-15	
	11.7	MMU test	11-19	
Chapter 12	Instru	uction Cycle Summary and Interlocks		
•	12.1	About the instruction cycle summary	12-2	
	12.2	Instruction cycle times		
	12.3	Interlocks		
Chapter 13	AC C	haracteristics		
	13.1	ARM920T timing diagrams	13-2	
	13.2	ARM920T timing parameters		
	13.3	Timing definitions for the ARM920T Trace Interface Port		
Appendix A	Signa	al Descriptions		
пропаж и	A.1	AMBA signals	Δ-2	
	A.2	Coprocessor interface signals		
	A.3	JTAG and TAP controller signals		
	A.4	Debug signals		
	A.5	Miscellaneous signals		
	A.6	ARM920T Trace Interface Port signals	A-13	
Appendix B	A.6	·	A-13	
Appendix B	A.6 CP15	i Test Registers		
Appendix B	A.6	·	B-2	



DOCKET

Explore Litigation Insights



Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time** alerts and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.

