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Paper 13
Date: March 13, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

AQUILA INNOVATIONS, INC.,
Patent Owner.

IPR2019-01526
Patent 6,895,519 B2

Before SALLY C. MEDLEY, DENISE M. POTHIER, and AMBER L. HAGY, *Administrative Patent Judges.*

POTHIER, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

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I. INTRODUCTION

Advanced Micro Devices, Inc. ("Petitioner")[1] requests an *inter partes* review of all claims (claims 1–11) in U.S. Patent No. 6,895,519 B2 (Ex. 1001, "the '519 patent"). Paper 2 ("Petition" or "Pet."), 16. Aquila Innovations Inc. ("Patent Owner") filed a Preliminary Response. Paper 10 ("Prelim. Resp."). With authorization, Petitioner filed a Reply (Paper 11, "Reply"), and Patent Owner filed a Sur-Reply (Paper 12, "Sur-Reply").

Under 35 U.S.C. § 314, an *inter partes* review may not be instituted "unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." Upon consideration of the Petition, Preliminary Response, Reply, and Sur-Reply, we determine that Petitioner has shown that there is a reasonable likelihood that it would prevail in showing the unpatentability of claims 1–11 of the '519 patent. We institute an *inter partes* review of all challenged claims of the '519 patent.

A. Related Proceedings

The parties indicate the '519 patent is at issue in a pending lawsuit, *Aquila Innovations Inc. v. Advanced Micro Devices*, Case No. 1:18-cv-00554-LY (W.D. Tex. filed July 2, 2018). Pet. 74; Paper 6, 2.

B. The '519 Patent

The '519 patent was filed on September 23, 2002, and claims priority to a Japanese application filed on February 25, 2002. Ex. 1001, codes (22) and (30). The '519 patent relates to a system large scale integration (LSI). *Id.* at 1:7–10. As background, the '519 describes a prior art microcontroller

[1] Petitioner identifies itself and ATI Technologies ULC as the real parties-in-interest. Pet. 4.

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power management that includes four clock operation modes: high-speed operation mode (operating at ½ of the oscillation frequency), low-speed operation mode (operating at 1/4, 1/8, 1/16, and 1/32 of the oscillation frequency respectively), wait mode, and halt mode. *Id.* at 1:63–2:6, 2:61–67, Fig. 10.

The '519 patent describes an "improved system LSI" that overcomes various problems in the prior art system LSIs. *Id.* at 3:24; *id.* at 3:21–34. The '519 patent discloses "[a] system LSI dynamically and speedily controls clocks of various frequencies as used in a wide range of operation modes from high-speed to low-speed operation modes, enabling user selection of a system of power consumption type most suitable." *Id.* at code (57); *see also id.* at 3:23–34.

Figure 2 of the '519 patent below shows an LSI:

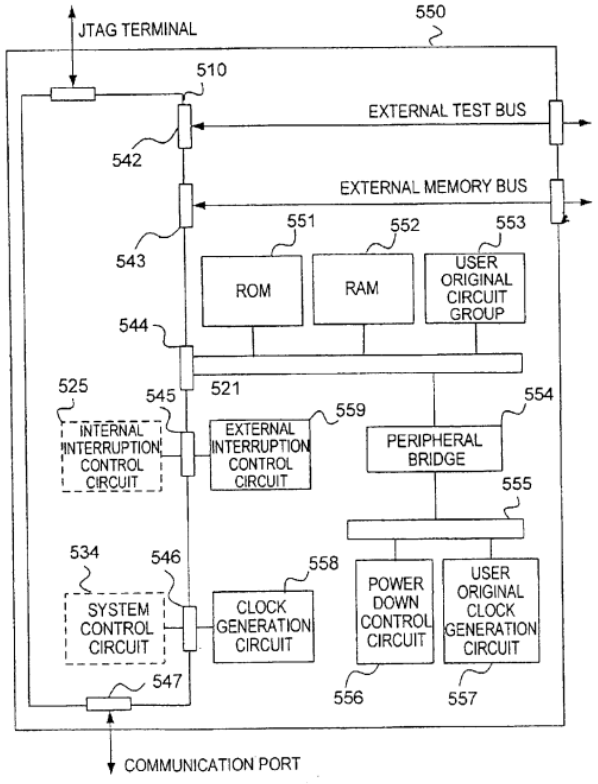

Figure 2 shows a system LSI using a CPU.

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Id., 5:60–61, Fig. 2. As shown above, LSI 550 includes CPU 510, ROM 551 for storing a clock control library and an application program, system control circuit 534, and clock generation circuit 558. *Id.* at 6:50–57, 7:9–12, 7:60–67, Figs. 2–4. According to the '519 patent, the LSI's system control circuit 534 and clock generation circuit 558 reduce consumed power without losing the core CPU's versatility. *Id.* at 11:50–54, Figs. 1–5.

The '519 patent's clock control library (e.g., 32 in Figure 6) manages power using an application program (e.g., 31 in Figure 6). *Id.* at 11:61–65, Fig. 6. A main library (e.g., 33 in Figure 6) selects one of the libraries (e.g., 34 in Figure 6) corresponding with the application program's state and permits transitions between clock operating modes. *Id.* at 12:2–5, 12:27–30, Figs. 6, 8(a). Below, Figure 5 illustrates an example of clock operation mode (i.e., eight operation modes STNn (n:integer of 0 through 7)) and the state transitions.

FIG.5

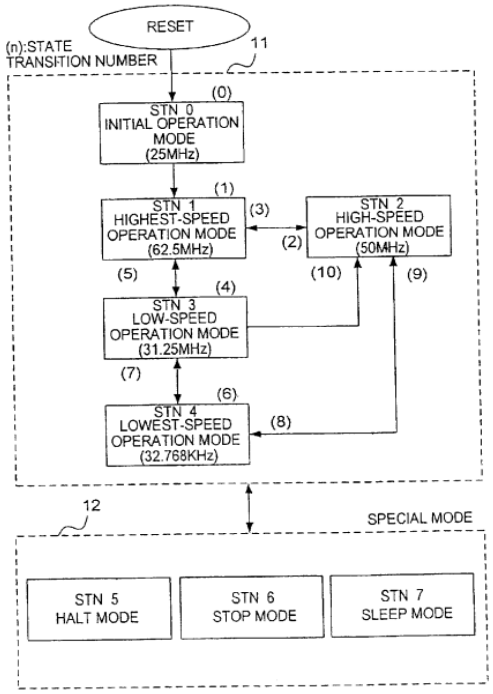

Figure 5 shows clock operation modes and state transitions.

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Id. at 5:66–67, 9:4–8, Fig. 5. Figure 5's arrows show transitions among various states (modes). *Id.* at 11:18–22, Fig. 5.

A "clock gear" concept permits transitions between the ordinary operation modes (e.g., STN0–STN4). *Id.* at 9:4–6, 11:33–39, Fig. 5. For example, the '519 patent describes the state transition number becomes (5) in Figure 5, when switching the current clock mode from the low-speed operation mode (STN3) to the high-speed operation mode. *Id.* at 13:9–19, Fig. 5. Figure 5 further shows five "ordinary operation modes" (e.g., STN0–4) and three "special modes" (e.g., STN5–STN7). *Id.* at 9:46–47, Fig. 5. Figure 5's ordinary operation modes include: (1) an initial operation mode (STN0, 25 MHz), (2) a highest-speed operation mode (STN1, 62.5 MHz), (3) a high-speed operation mode (STN2, 50 MHz), (4) a low-speed operation mode (STN3, 31.25 MHz), and (5) a lowest-speed operation mode (STN4, 32.768 MHz). *Id.* at 9:12–17, 9:38–41, 9:49–10:17, Fig. 5.

C. Illustrative Claim

Petitioner challenges all the claims of the '519 patent. Of the contested claims, claim 1 is the only independent claim. Claims 2 through 11 ultimately depend from claim 1. Independent claim 1, reproduced below, illustrates the claimed subject matter.

> 1. A system LSI having a plurality of ordinary operation modes and a plurality of special modes in response to clock frequencies supplied to a central processing unit, comprising:
>
> a first memory that stores a clock control library for controlling a clock frequency transition between said ordinary operation modes;
>
> a system control circuit which has a register, wherein said system control circuit carries out the clock frequency transition between said ordinary operation modes and said special modes in response to a change of a value in said

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