

UNITED STATES DISTRICT COURT  
WESTERN DISTRICT OF TEXAS  
AUSTIN DIVISION

AQUILA INNOVATIONS INC., a Delaware corporation,	§	No. 1:18-cv-00554-LY
	§	
Plaintiff,	§	
	§	
v.	§	
	§	
ADVANCED MICRO DEVICES, INC., a Delaware corporation	§	
	§	
Defendant.	§	
	§	
	§	

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**REVISED JOINT CLAIM CONSTRUCTION STATEMENT**

Pursuant to the Court’s request during the August 23, 2019 Claims Construction Hearing, Plaintiff Aquila Innovations Inc. (“Aquila”) and Defendant Advanced Micro Devices, Inc. (“AMD”) submit this Revised Joint Claim Construction Statement for U.S. Patent Nos. 6,895,519 (“the ’519 Patent”) and 6,239,614 (“the ’614 Patent”). Alternative proposed constructions based on the Claims Construction Hearing are designated as “(Alternative based on CC hearing).”

**I. '519 PATENT AGREED CONSTRUCTIONS**

<b><u>Term</u></b>	<b><u>Agreed Construction</u></b>
Whether the preamble of claim 1 is limiting.  “A system LSI having a plurality of ordinary operation modes and a plurality of special modes in response to clock frequencies supplied to a central processing unit”	The preamble of claim 1 is limiting. The disputed constructions for the term “system LSI” are below. No other terms within the preamble require construction.

**II. '519 PATENT DISPUTED CONSTRUCTIONS**

[Exhibit A](#) contains the parties’ respective proposed constructions of disputed claim terms in the ’519 Patent, together with an identification of supporting intrinsic and extrinsic evidence upon which they intend to rely. The proposed terms for construction are:

- [“system LSI”](#) (claim 1)
- [“plurality of standard clocks”](#) (claim 1)
- [“generates a clock”](#) (claim 1)
- [“a clock control library for controlling a clock frequency transition between said ordinary operation modes”](#) (claim 1)
- [“user selectable”](#) (claim 1)
- [“an application program wherein calling of said clock control library and changing of said register value are programmably controlled by said application program to enable user selectable clock frequency transitions”<sup>1</sup>](#) (claim 1)
- [“halted”](#) (claim 1, 7)
- [“principal constituents of said central processing unit”](#) (claim 1)
- [“a main library which is called by said application program and selects any one of said libraries”](#) (claim 2)
- [“a status register that judges a state of said central processing unit immediately after being released from said third special mode”](#) (claim 7)

<sup>1</sup> The parties agree that this term is not subject to § 112, para. 6.

**III. '614 PATENT DISPUTED CONSTRUCTIONS**

[Exhibit B](#) contains the parties' respective proposed constructions of disputed claim terms in the '614 Patent, together with an identification of supporting intrinsic and extrinsic evidence upon which they intend to rely. The proposed terms for construction are:

- [“unit cells”](#) (claim 1)
- [“unit cell array”](#) (claims 1, 3)
- [“a unit cell array comprised of first and second unit cells laid in array form”](#) (claim 1)
- [“a power switch”](#) (claims 1, 2, 3)
- [“disposed around”](#) (claim 1)<sup>2</sup>
- [“parts of said power switch disposed within said unit cell array”](#) (claim 3)

**IV. EXPERT IDENTIFICATION**

<u>Patent</u>	<u>Plaintiff's Expert</u>	<u>Defendant's Expert</u>
'519 Patent	Dr. Vojin Oklobdzija	Dr. David Albonesi
'614 Patent	Dr. Vojin Oklobdzija	Dr. Douglas Holberg

The parties rely upon the opinions of their respective experts (identified above) regarding how a person of ordinary skill in the art (“POSITA”) would understand the meaning of each disputed term.

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<sup>2</sup> The parties have agreed that “disposed around” is the disputed term for both previously proposed terms: “a power switch **disposed around** said unit cell array and comprised of a plurality of third MOS transistors” and “a plurality of input / output circuits **disposed around** said unit cell array.”

Dated: November 1, 2019

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**Exhibit A**

<b>U.S. Patent 6,895,519</b>		
<u>Term</u>	<u>Plaintiff's Proposed Construction and Evidence</u>	<u>Defendant's Proposed Construction and Evidence</u>
<p>“system LSI” (claim 1)</p>	<p><i>system on a chip</i></p> <p><b>’519 Patent</b> 1:5-10, 26-30, 2:10-30, 2:43-55.</p> <p>Fig. 1, 2</p> <p>Cl. 1</p> <p>“<b>LSI</b>”: McDaniel, G., <i>IBM Dictionary of Computing</i> (McGraw-Hill 10th ed. 1993) at 375; Laplante, P.A., <i>Comprehensive Dictionary of Electrical Engineering</i> (CRC Press 2005) at 361.</p> <p>Declaration of Vojin Oklobdzija, ECF No. 41-7.</p>	<p><i>single integrated chip, which has a central processing unit, first memory, second memory, and I/O capability</i></p> <p><b>OR</b></p> <p><i>system on a single integrated chip (Alternative based on CC hearing)</i></p> <p>’519 Patent: Figs. 1, 2, 1:5–15, 1:26–30, 2:10–30, 2:43–55, 9:7–11:17, 12:33–37; claims 1–11.</p> <p>Certified Translation of Japanese Patent 2002-047696, ¶¶ [0002], [0010], Explanation of Reference Numerals, Figs. 1, 2, claims 1–8.</p> <p>“<b>LSI</b>”: McDaniel, G., <i>IBM Dictionary of Computing</i> (McGraw-Hill 10th ed. 1993) at 375; Laplante, P.A., <i>Comprehensive Dictionary of Electrical Engineering</i> (CRC Press 1999) at 361.</p> <p>“<b>microcontroller</b>”: Graf, R.F., <i>Modern Dictionary of Electronics</i> (7th ed. 1999) at 470; McGraw-Hill Dictionary of Scientific and Technical Terms (6th ed. 2003) at 1334; Laplante, P.A., <i>Comprehensive Dictionary of Electrical Engineering</i> (CRC Press 1999) at 410-11; Microsoft Computer Dictionary (5th ed. 2002) at</p>

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