

*Advanced Micro  
Devices, Inc.*

*v.*

*Aquila Innovations Inc.*

U.S. Patent No. 6,895,519

IPR2019-01526

Aquila Innovation Inc.'s Demonstratives

# Grounds

Grounds	References	Type	Challenged Claims
1	Ober <sup>1</sup> and Nakazato <sup>2</sup>	§103	1, 7, 10, and 11
2	Ober, Nakazato, Cooper <sup>3</sup> , and Windows ACPI <sup>4</sup>	§103	2-6
3	Ober, Nakazato, and Doblar <sup>5</sup>	§103	8 and 9

# Ground 1 – Ober + Nakazato

- What is Petitioner’s Combination?
- Multiple Limitations Not Disclosed In Combination
  - “plurality of ordinary operation modes”
  - “clock frequency transitions between said ordinary operation modes”
- Combination Not Obvious
  - Unpredictable to write to unused bits in register
  - Power Management State Machine unpredictable outside of defined states
  - Ober teaches away from Nakazato

# Ground 1 – What Is Petitioner’s Combination?

- Petition: Ober’s Hardware + Nakazato’s Power-Saving Driver

1. **Like the challenged claims of the ’519 patent, Ober discloses a System LSI with a clock generation circuit that receives a plurality of clocks and a system control circuit that can switch between ordinary operation modes and special operation modes via a register.**
2. **Nakazato discloses “a clock control library” and an “application” for controlling CPU frequency.**

# Ground 1 – What Is Petitioner’s Combination?

- Petition: Ober’s Hardware + Nakazato’s Power-Saving Driver

In Nakazato, the Geyserville register is controlled by a driver (i.e., a *clock control library*). *Id.*, 7:3-6. And the driver is controlled by a user application. *Id.*, 7:6-8. Specifically, the user can select a “user-designated speed” (i.e. highest, high, middle, low, lowest) via an “*application*” as shown below in Figure 2:

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