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Gary et al.

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(45) **Date of Patent:** **Dec. 26, 2006**

(54) **METHODS AND SYSTEMS FOR
PERFORMING DYNAMIC POWER
MANAGEMENT VIA FREQUENCY AND
VOLTAGE SCALING**

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(*) Notice: Subject to any disclaimer, the term of this
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U.S.C. 154(b) by 433 days.

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(65) **Prior Publication Data**

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Related U.S. Application Data

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1, 2002.

(57) **ABSTRACT**

(51) **Int. Cl.**

G06F 1/26 (2006.01)
G06F 1/32 (2006.01)
G06F 9/44 (2006.01)
G06F 13/10 (2006.01)
G06F 9/45 (2006.01)

Methods and systems are provided for dynamically managing
the power consumption of a digital system. These
methods and systems broadly provide for varying the fre-
quency and voltage of one or more clocks of a digital system
upon request by an entity of the digital system. An entity
may request that the frequency of a clock of the processor of
the digital system be changed. After the frequency is
changed, the voltage point of the voltage regulator of the
digital system is automatically changed to the lowest voltage
point required for the new frequency if there is a single clock
on the processor. If the processor is comprised of multiple
processing cores with associated clocks, the frequency is
changed to the lowest voltage point required by all frequen-
cies of all clocks.

(52) **U.S. Cl.** **713/300**; 713/310; 713/320;
713/322; 703/21; 703/22

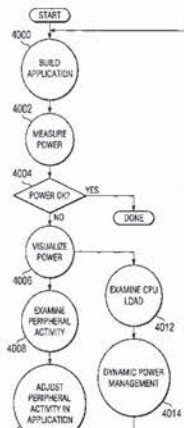
(58) **Field of Classification Search** 713/300,
713/310, 321, 322, 324, 330
See application file for complete search history.

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33 Claims, 5 Drawing Sheets



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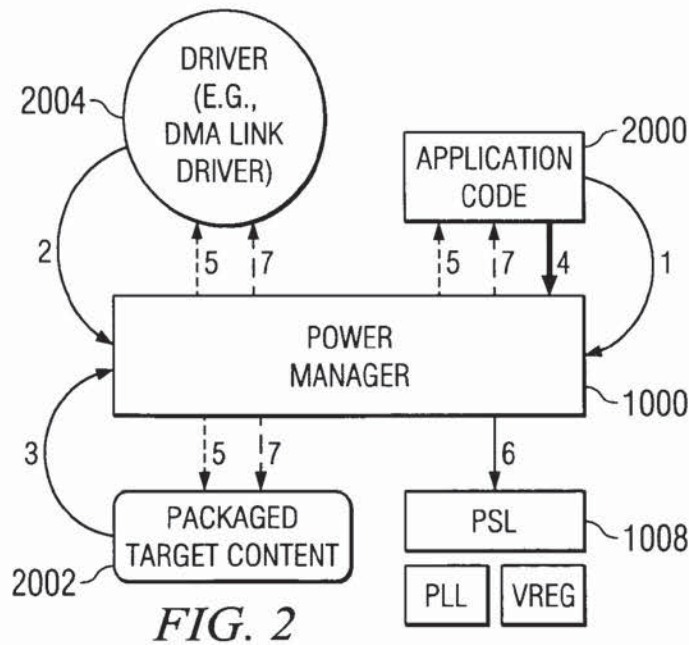
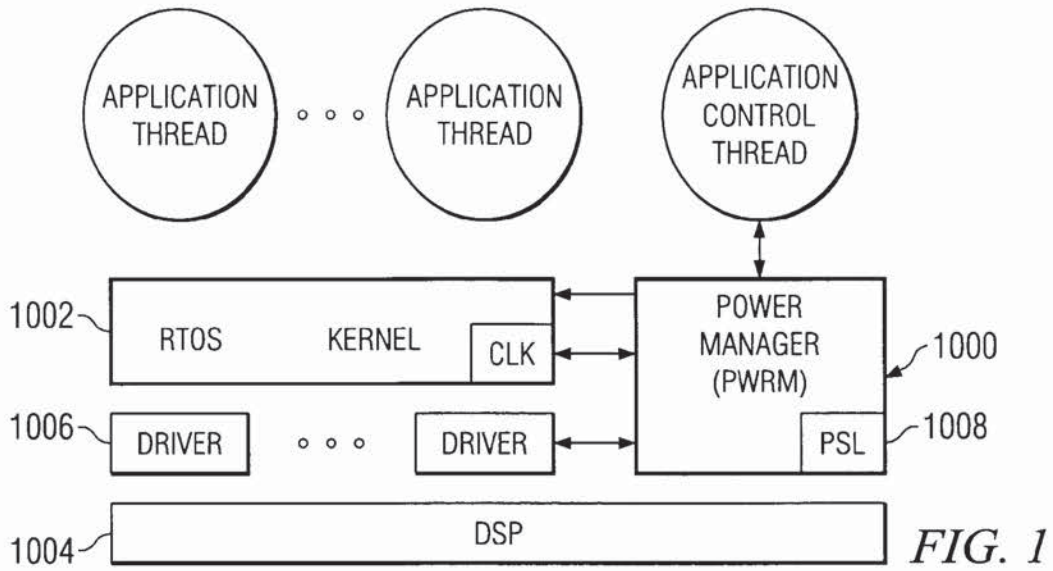
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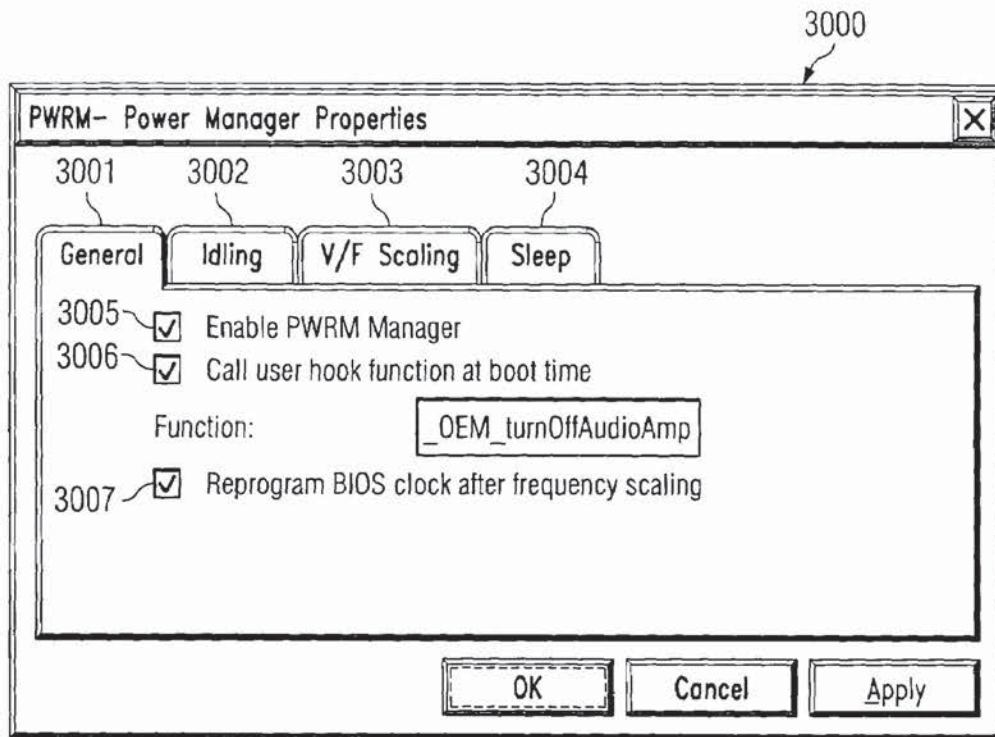


FIG. 3A

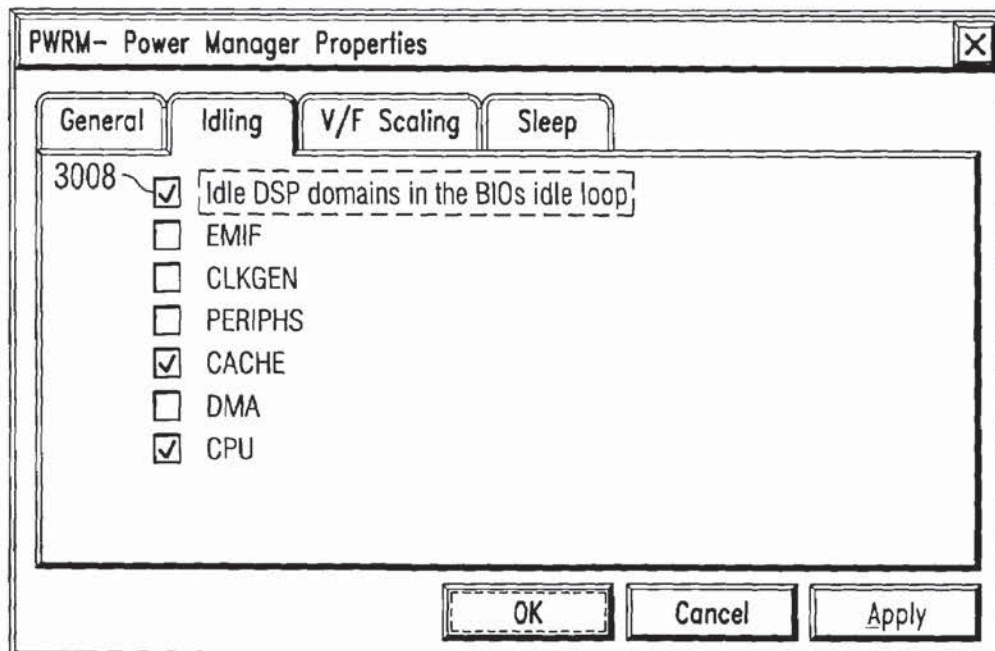


FIG. 3B

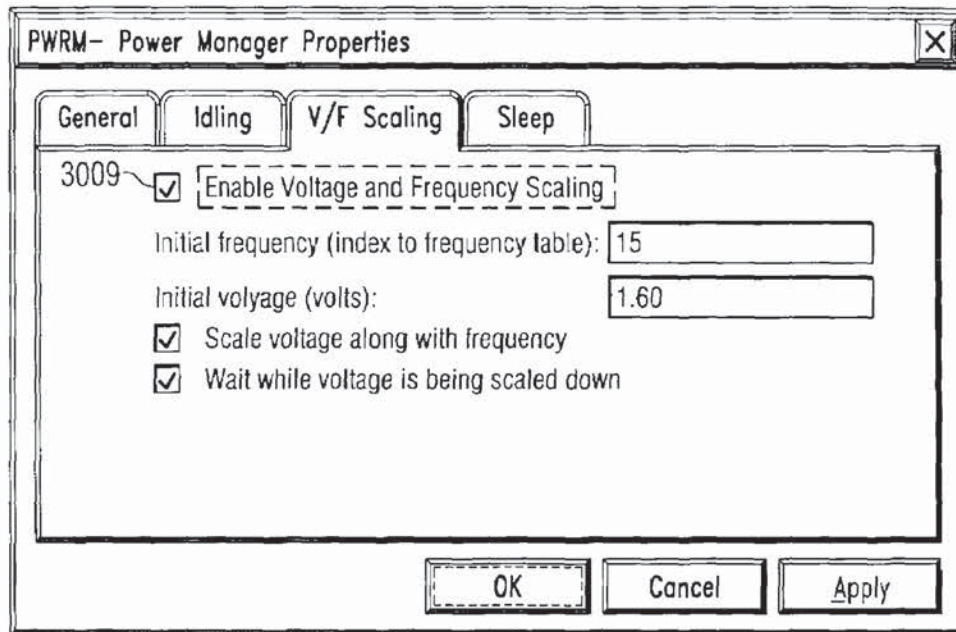


FIG. 3C

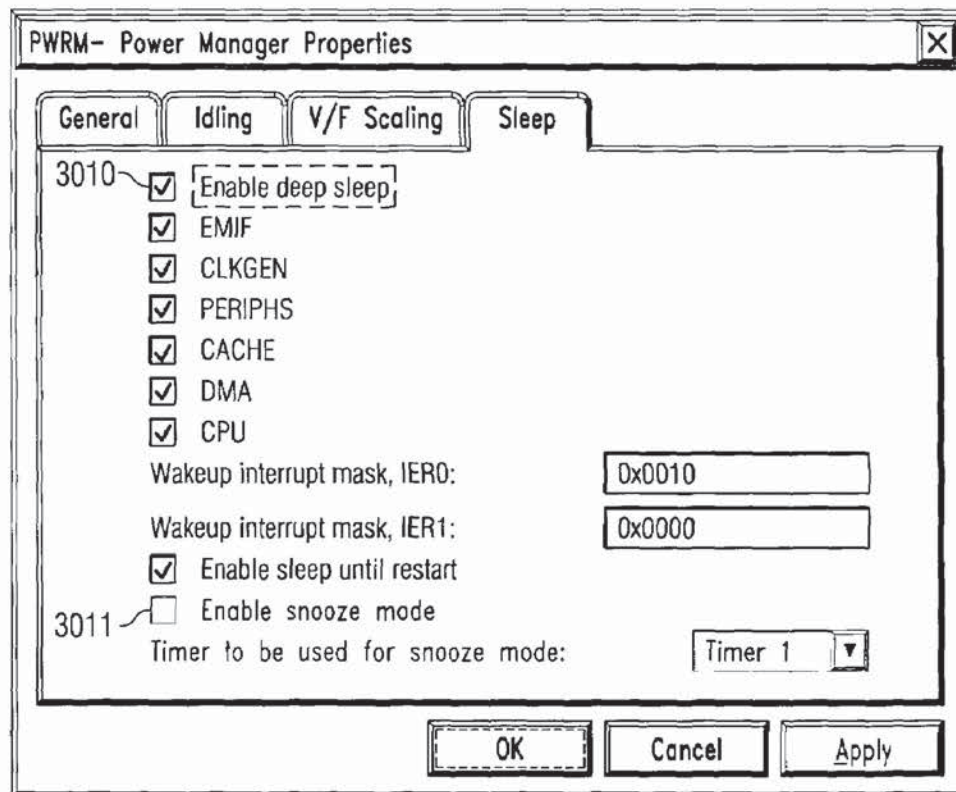


FIG. 3D

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