UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

AQUILA INNOVATIONS, INC., a Delaware Corporation, Plaintiff, v. ADVANCED MICRO DEVICES, INC., a Delaware corporation Defendant.	§ § § § § § § § §	No. 1:18-cv-554-LY

AQUILA INNOVATIONS, INC.'S
PRELIMINARY INFRINGEMENT CONTENTIONS

Pursuant to the Court's Scheduling Order, D.I.23, Plaintiff Aquila Innovations, Inc. ("Aquila") submits the following preliminary infringement contentions for U.S. Patents 6,239,614 ("'614 Patent") and 6,895,519 ("'519 Patent"). These preliminary infringement contentions were prepared without the benefit of the Court's claim construction or the parties' exchange of constructions. Discovery has been stayed, and AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court's constructions or to account for new information that becomes available.

(a) Identification of asserted claims

'614 Patent: Claims 1, 2

'519 Patent: Claims 1, 2, 3, 5, 6, 7, 10

(b) Identification of accused products

'614 Patent Accused Products:

Aquila contends that all AMD processor products containing power gate rings infringe each of the asserted claims of the '614 Patent. This specifically includes but is not limited to processors with cores having microarchitectures belonging to the following families:

- AMD 12h Llano Fusion APUs
- AMD 15h Bulldozer APUs
- AMD 15h Piledriver APUs
- AMD 15h Excavator APUs

AMD products belonging to each product family are identified in Exhibits C.1 through C.4. The identification of specific products was prepared without the benefit of discovery from AMD and may not include OEM or custom processor products. Aquila reserves the right to amend or supplement its identification of accused products as AMD provides more information.

'519 Patent Accused Products:

Aquila contends that all AMD processor products capable of entering/exiting the CC1, PC1, and PC6 states infringe each of the asserted claims of the '519 Patent. This specifically includes but is not limited to processors with cores having microarchitectures belonging to the following families:

- AMD Family 12h
- AMD Family 14h
- AMD Family 15h
- AMD Family 16h
- AMD Family 17h

AMD products belonging to each product family are identified in Exhibits C.1 through C.5. The identification of specific products was prepared without the benefit of discovery from AMD and may not include OEM or custom processor products. Aquila reserves the right to amend or supplement its identification of accused products as AMD provides more information.

(c) Claim Charts

Claim charts for each asserted claim corresponding to each representative accused product are contained in the exhibits below.

'614 Patent: Exhibit A

'519 Patent: Exhibit B

(d) Doctrine of Equivalents

Aquila contends that each limitation in each asserted claim is met literally. The Court has not construed the asserted claims, and AMD has not yet provided discovery on the accused products or provided non-infringement contentions. Aquila reserves the right to respond if AMD provides non-infringement contentions, which response may include doctrine of equivalents contentions.

(e) Identification of Priority Date

'614 Patent: Each asserted claim of the '144 Patent is entitled to a priority date as late as January 14, 1999.

'519 Patent: Each asserted claim of the '519 Patent is entitled to a priority date as late as February 25, 2002.

Respectfully submitted,

Dated: February 13, 2019

/s/Jing H. Cherng

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CERTIFICATE OF SERVICE

I hereby certify that on this 13th day of February, 2019, a true and correct copy of the foregoing was forwarded to the following:

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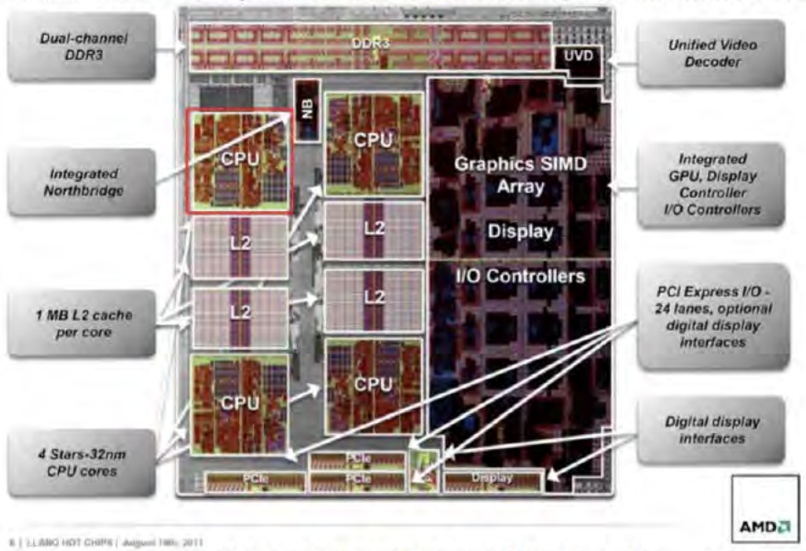
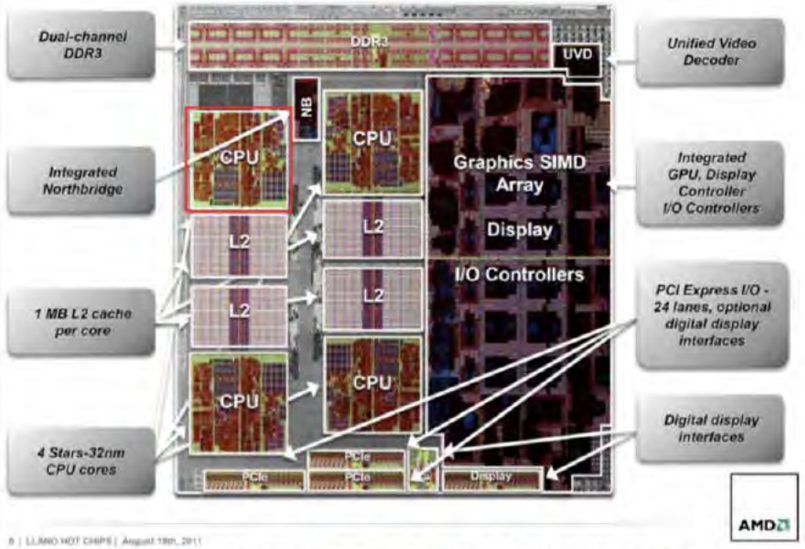
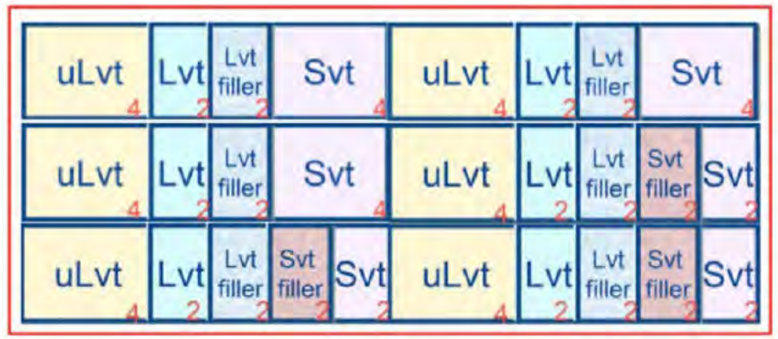
Exhibit A.1: Preliminary Infringement Contention Claim Chart for U.S. Patent 6,239,614

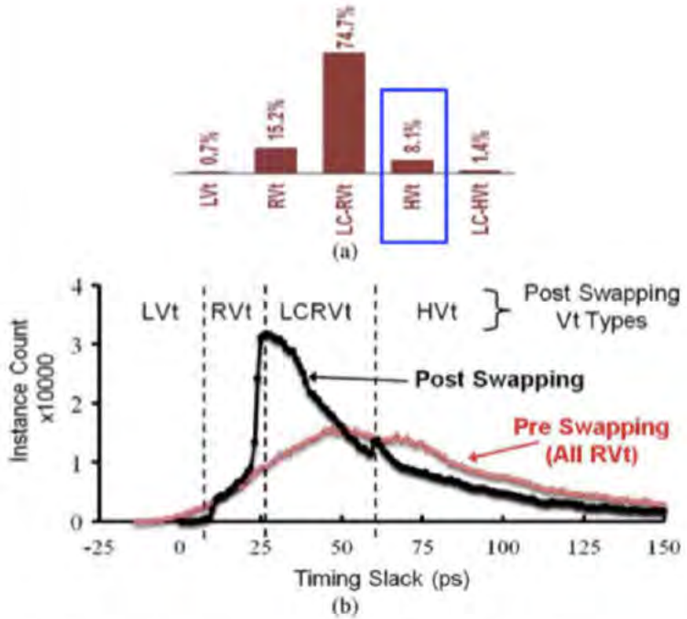
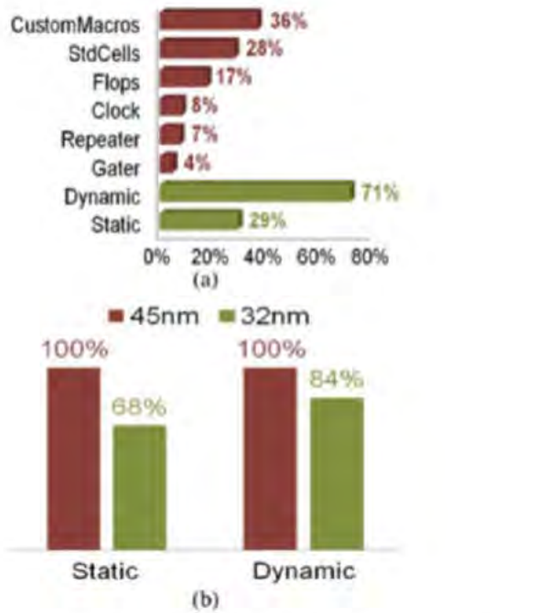
Accused Product: AMD Family 12h Fusion Processors

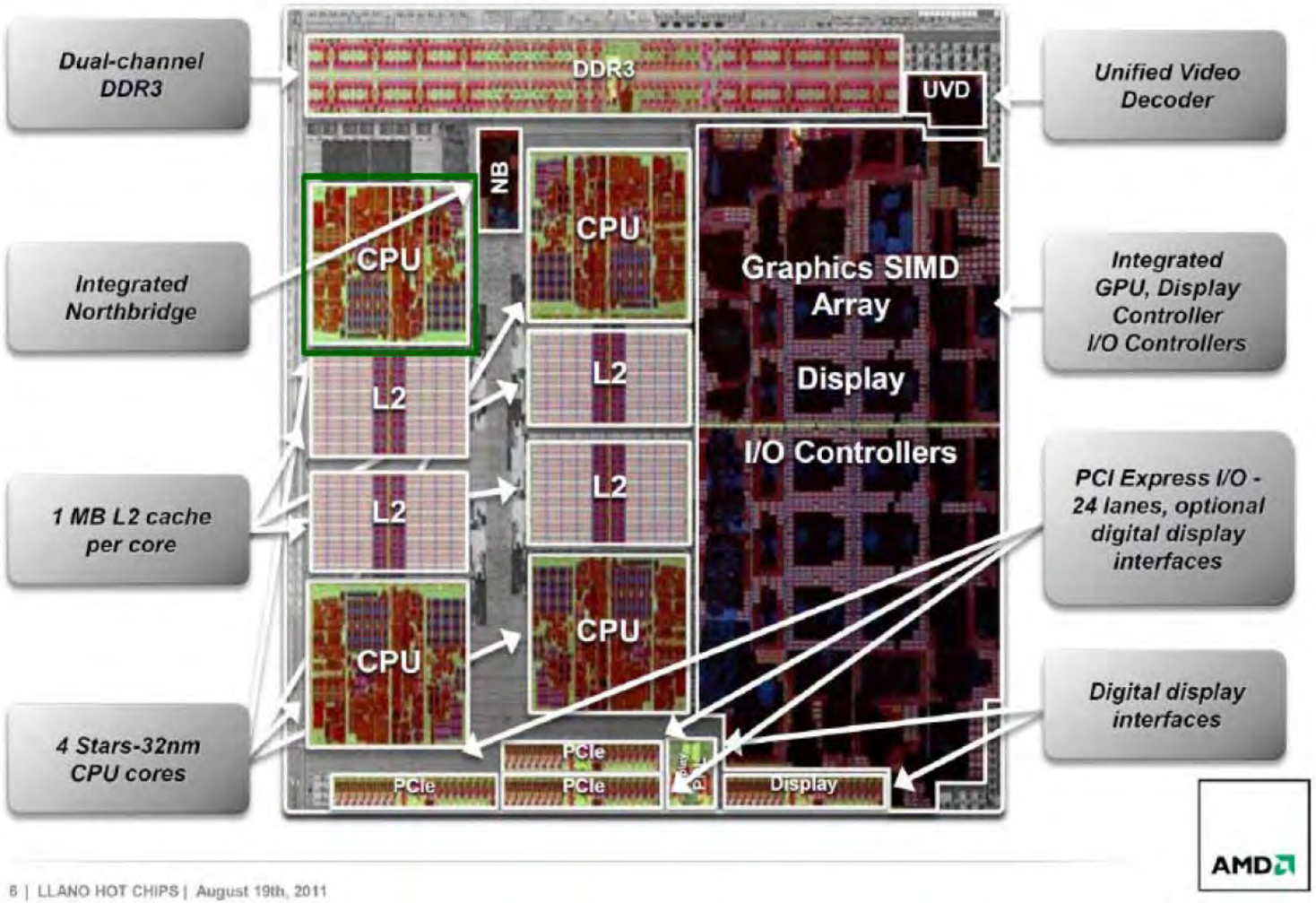
These preliminary infringement contentions were prepared without the benefit of the Court's claim construction or the parties' exchange of constructions. As of the date of these contentions, AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court's constructions or to account for new information that becomes available.

	Limitation	Contention
1p	A semiconductor integrated circuit device, comprising:	To the extent the preamble is a limitation, the Accused Products are semiconductor integrated circuit devices.  *Source: AMD'S "LLANO" FUSION APU, Hot Chips 23, 19th August 2011,* page 6.

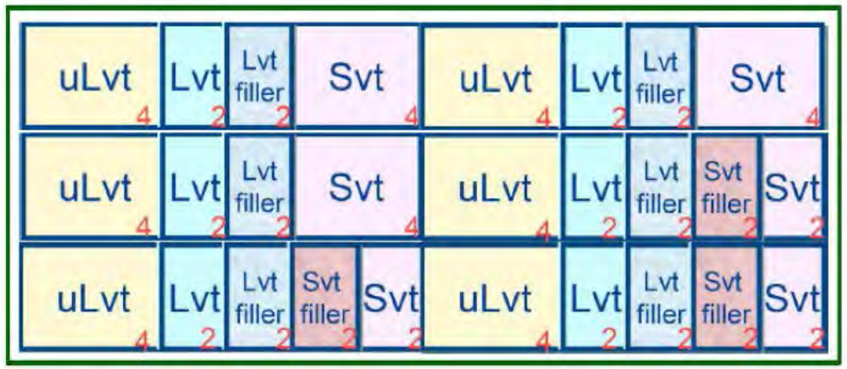
	Limitation	Contention
1a	a plurality of first unit cells each including a plurality of first MOS transistors, each of the first MOS transistors having a first threshold voltage;	The Accused Products contain a plurality of first unit cells:  *Source: AMD'S "LLANO" FUSION APU, Hot Chips 23, 19th August 2011,* page 6. As is typical of multi-VT standard cell design methodologies and structures, the Llano Accused Products use a mix of low Vt (LVt), regular Vt (RVt), long channel regular Vt (LC-RVt) and long channel high Vt (LC-Hvt) standard cells.

	Limitation	Contention
		 The Accused Products contain a plurality of first MOS transistors, each of the first MOS transistors having a first threshold voltage:

	Limitation	Contention
		JOTWANI *et al.*: AN x86-64 CORE IN 32 nm SOI CMOS 167  Fig. 10. (a) Core device width histogram by Vt type. (b) Using Vt swaps to reshape critical path timing opportunistically.  Fig. 11. (a) TDP power distribution at 1 V. (b) Relative power improvement with respect to 45 nm generation core (normalized for performance). *Source: An x86-64 Core in 32 nm SOI CMOS, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 1, JANUARY 2011*, page 6.
1b	a plurality of second unit cells each including a plurality of second MOS	The Accused Products contain a plurality of second unit cells:

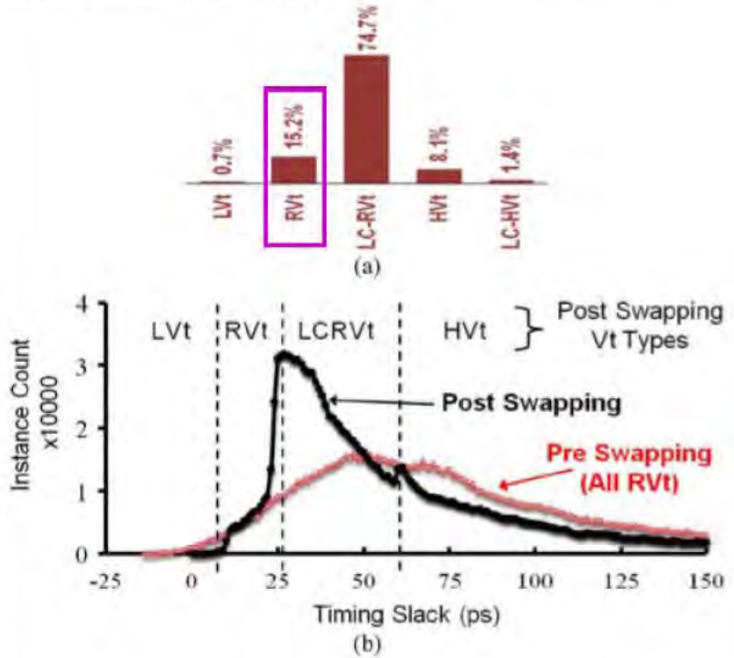
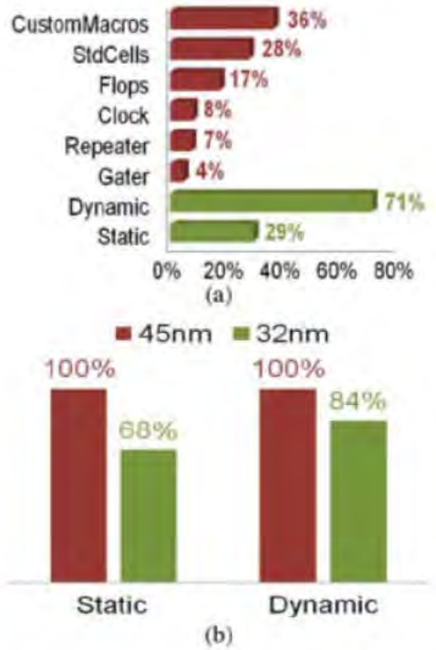
	Limitation	Contention
	transistors, each of the second MOS transistors having a second threshold voltage;	 *Source: AMD'S "LLANO" FUSION APU, Hot Chips 23, 19th August 2011,* page 6.

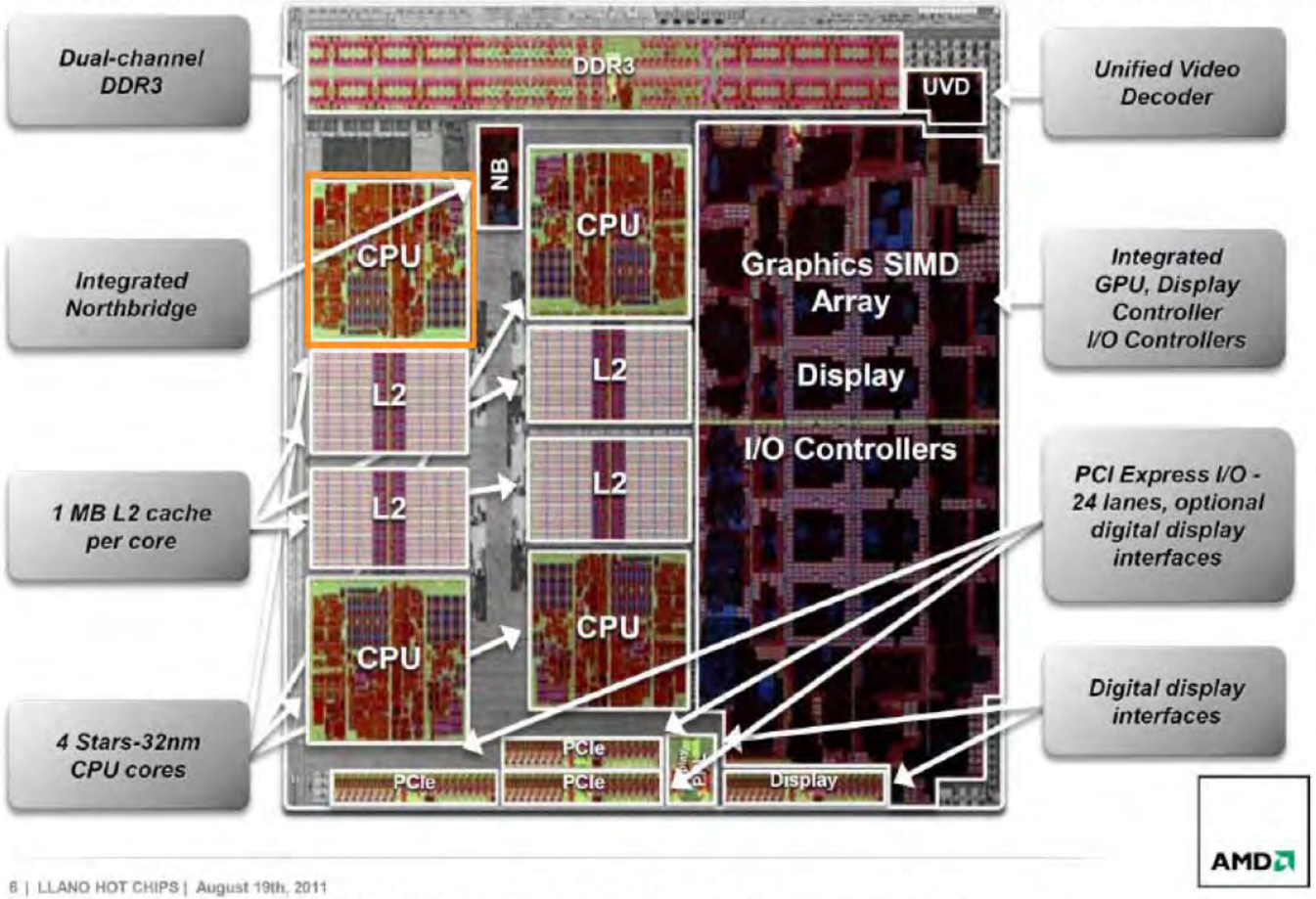
	Limitation	Contention
		Modern multi-VT standard cell design methodologies and structures such as those used in the Llano Accused Products use a mix of low Vt (LVt), regular Vt (RVt), long channel regular Vt (LC-RVt) and long channel high Vt (LC-Hvt) standard cells.



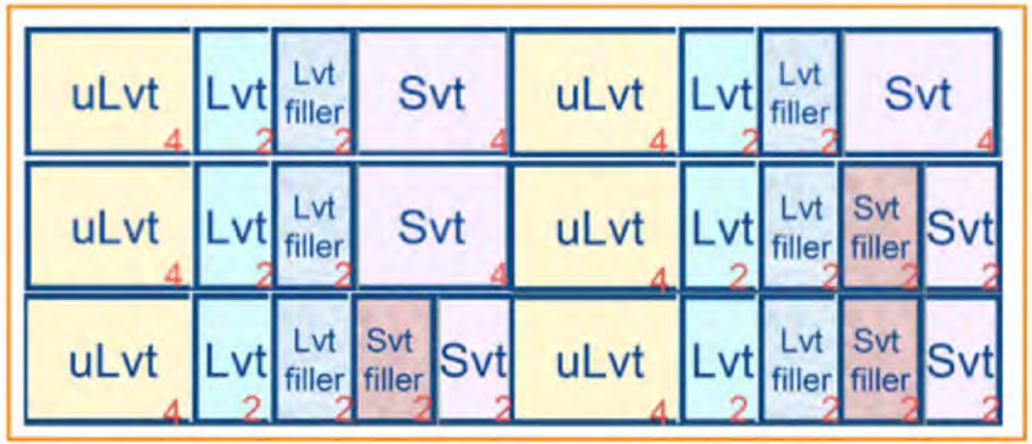
DVFS Characteristics Modern computer chips are designed using multiple types of transistors, i.e. a mixture of low-, medium-, and high-threshold transistors, to target different design tradeoffs, e.g. high-performance vs. low power.

Low-threshold voltage (Low-Vt) devices are used in timing-critical paths, but have high leakage power. High-threshold voltage (High-Vt) devices have low leakage power but are slower, and are typically used in circuits that are off the timing-critical paths. Medium-threshold voltage (Mid-Vt) devices offer a tradeoff between High-Vt and Low-Vt devices by having medium power requirements and medium delay. In general, low power chips are designed using a larger percentage of High-Vt devices and high-performance chips with a larger percentage of Mid-Vt and Low-Vt devices. The host processor is assumed to execute compute-intensive code and will therefore be a high-performance device.

	Limitation	Contention
		Source: Scrbak et al., DVFS Space Exploration in Power Constrained Processing-in-Memory Systems, pp. 4-5. The Accused Products contain a plurality of second MOS transistors, each of the second MOS transistors having a second threshold voltage:  Fig. 10. (a) Core device width histogram by Vt type. (b) Using Vt swaps to reshape critical path timing opportunistically.  Fig. 11. (a) TDP power distribution at 1 V. (b) Relative power improvement with respect to 45 nm generation core (normalized for performance). *Source: An x86-64 Core in 32 nm SOI CMOS, page 6 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 1, JANUARY 2011.*

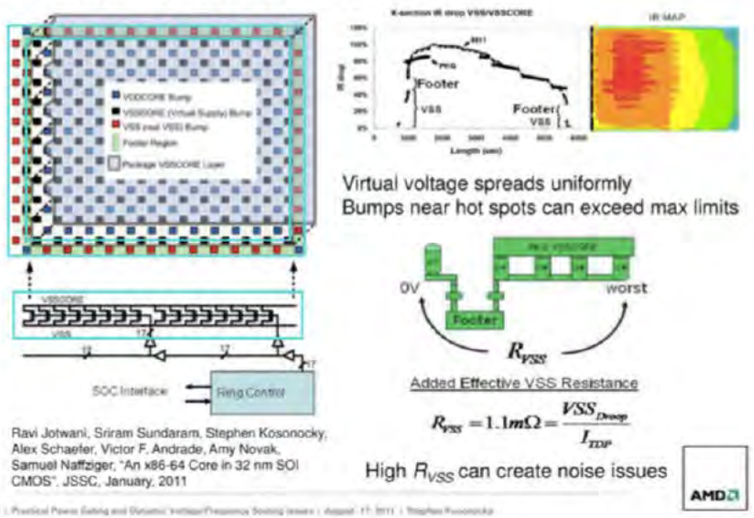
	Limitation	Contention
1c	a unit cell array comprised of said first and second unit cells laid in array form;	The Accused Products contain a unit cell array comprised of said first and second unit cells laid in array form:  *Source: AMD'S "LLANO" FUSION APU, Hot Chips 23, 19th August 2011*, page 6.

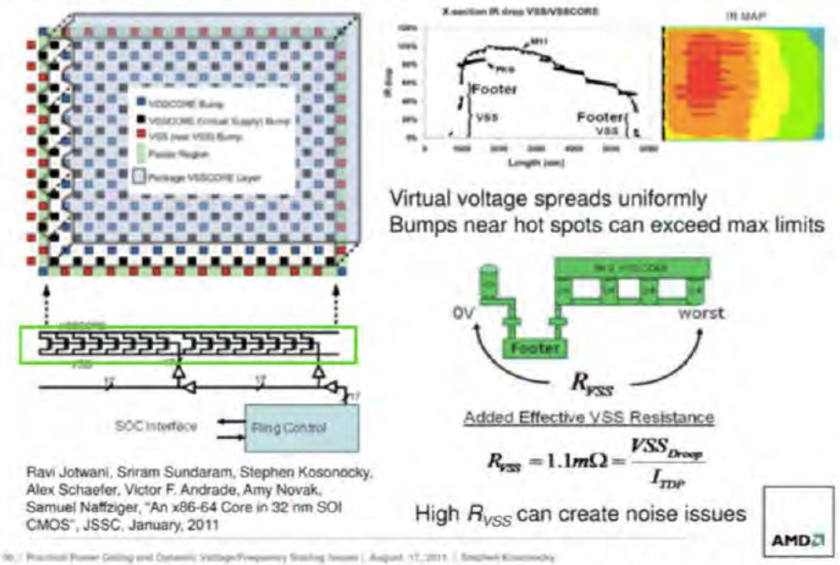
	Limitation	Contention
		Modern multi-VT standard cell design methodologies and structures such as those used in the Llano Accused Products use a mix of low Vt (LVt), regular Vt (RVt), long channel regular Vt (LC-RVt) and long channel high Vt (LC-Hvt) standard cells.

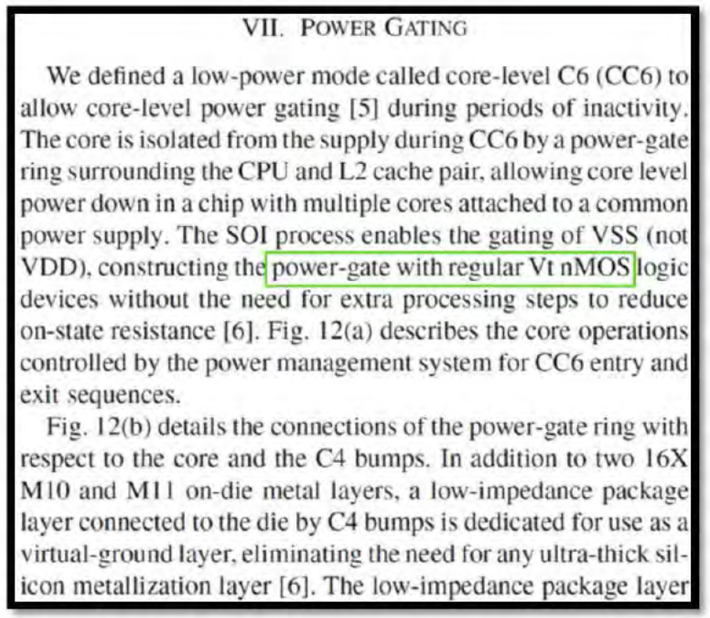


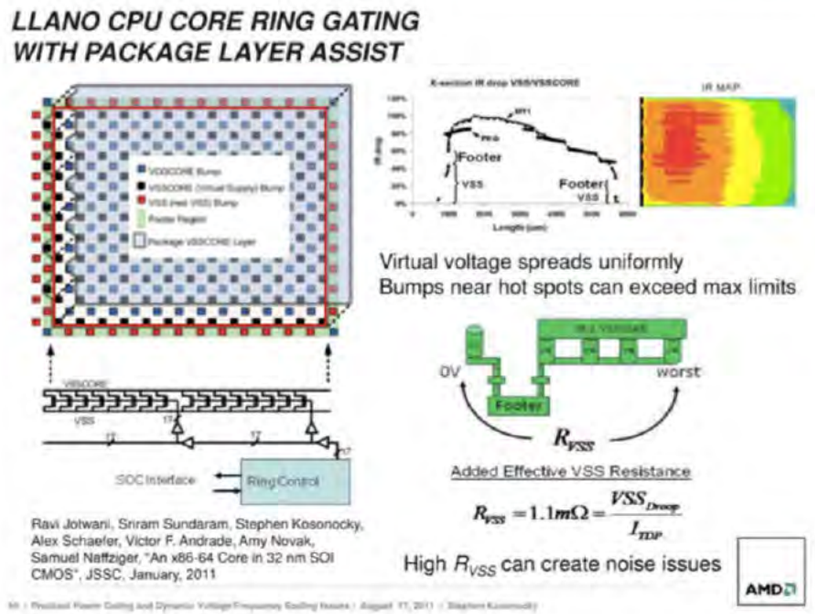
DVFS Characteristics Modern computer chips are designed using multiple types of transistors, i.e. a mixture of low-, medium-, and high-threshold transistors, to target different design tradeoffs, e.g. high-performance vs. low power.

Low-threshold voltage (Low-Vt) devices are used in timing-critical paths, but have high leakage power. High-threshold voltage (High-Vt) devices have

	Limitation	Contention
		low leakage power but are slower, and are typically used in circuits that are off the timing-critical paths. Medium-threshold voltage (Mid-Vt) devices offer a tradeoff between High-Vt and Low-Vt devices by having medium power requirements and medium delay. In general, low power chips are designed using a larger percentage of High-Vt devices and high-performance chips with a larger percentage of Mid-Vt and Low-Vt devices. The host processor is assumed to execute compute-intensive code and will therefore be a high-performance device. *Source:* Scrbak et al., DVFS Space Exploration in Power Constrained Processing-in-Memory Systems, pp. 4-5.
1d	a power switch disposed around said unit cell array and comprised of a plurality of third MOS transistors, each of the third MOS transistors having the second threshold voltage; and	The Accused Products contain a power switch disposed around said unit cell array: ***LLANO CPU CORE RING GATING WITH PACKAGE LAYER ASSIST***  *Source: PRACTICAL POWER GATING AND DYNAMIC VOLTAGE/FREQUENCY SCALING by Stephen*

	Limitation	Contention
		Kosonocky, page 50. The Accused Products contain a plurality of third MOS transistors: ***LLANO CPU CORE RING GATING WITH PACKAGE LAYER ASSIST***  *Source: PRACTICAL POWER GATING AND DYNAMIC VOLTAGE/FREQUENCY SCALING by Stephen Kosonocky, page 50* Each of the third MOS transistors of the power gate ring has the second threshold voltage.

	Limitation	Contention
		 VII. Power Gating We defined a low-power mode called core-level C6 (CC6) to allow core-level power gating [5] during periods of inactivity. The core is isolated from the supply during CC6 by a power-gate ring surrounding the CPU and L2 cache pair, allowing core level power down in a chip with multiple cores attached to a common power supply. The SOI process enables the gating of VSS (not VDD), constructing the power-gate with regular Vt nMOS logic devices without the need for extra processing steps to reduce on-state resistance [6]. Fig. 12(a) describes the core operations controlled by the power management system for CC6 entry and exit sequences. Fig. 12(b) details the connections of the power-gate ring with respect to the core and the C4 bumps. In addition to two 16X M10 and M11 on-die metal layers, a low-impedance package layer connected to the die by C4 bumps is dedicated for use as a virtual-ground layer, eliminating the need for any ultra-thick silicon metallization layer [6]. The low-impedance package layer *Source: An x86-64 Core in 32 nm SOI CMOS, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 1, JANUARY 2011,* page 6.
1e	a plurality of input/output circuits disposed around said unit cell array.	The Accused Products contain a plurality of input/output circuits disposed around said unit cell array.

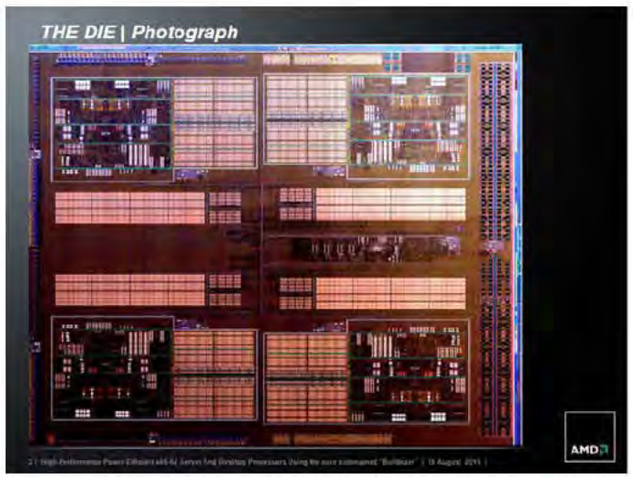
	Limitation	Contention
		 *Source: PRACTICAL POWER GATING AND DYNAMIC VOLTAGE/FREQUENCY SCALING by Stephen Kosonocky*, page 50.
2	A semiconductor integrated circuit device according to claim 1, wherein said power switch is turned off during standby and turned on when taken active.	The power gate ring of the Accused Products is turned off during standby and turned on when taken active.

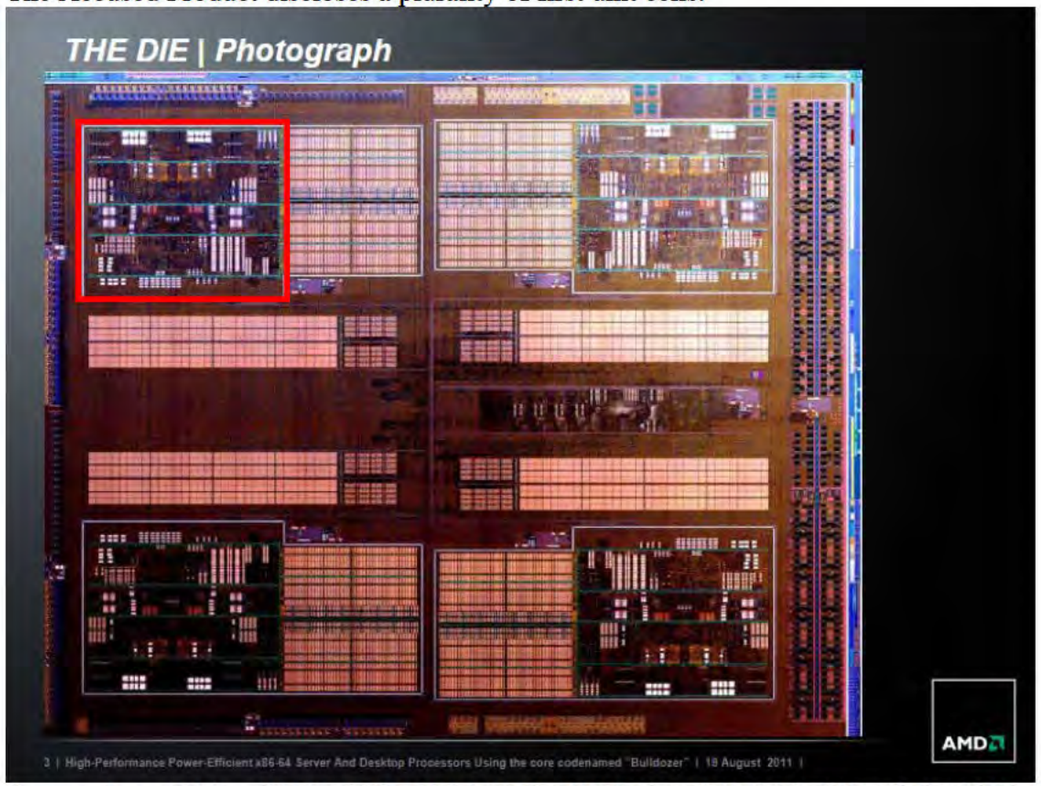
	Limitation	Contention
		Two major knobs have emerged for controlling power 1. Dynamic Voltage and Frequency Scaling – Optimize performance for the application while it's running 2. Power Gating – Gate power during idle periods Each present unique challenges for implementation and optimization AMD *Source: PRACTICAL POWER GATING AND DYNAMIC VOLTAGE/FREQUENCY SCALING by Stephen Kosonocky*, page 8.

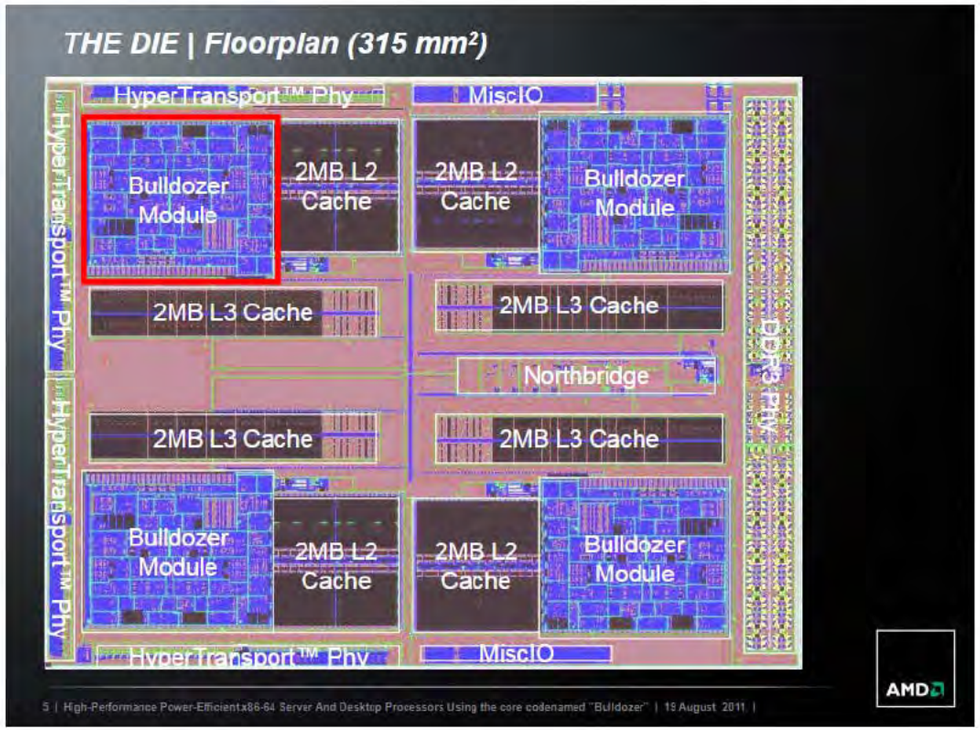
Exhibit A.2: Preliminary Infringement Contention Claim Chart for U.S. Patent 6,239,614

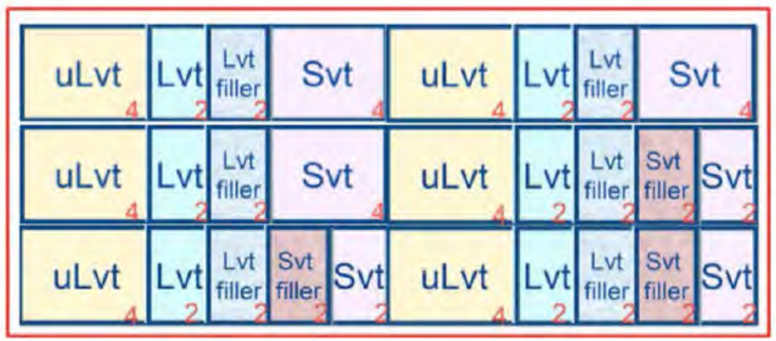
Accused Products: AMD Family 15h Bulldozer/Piledriver APU Processors

These preliminary infringement contentions were prepared without the benefit of the Court's claim construction or the parties' exchange of constructions. As of the date of these contentions, AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court's constructions or to account for new information that becomes available.

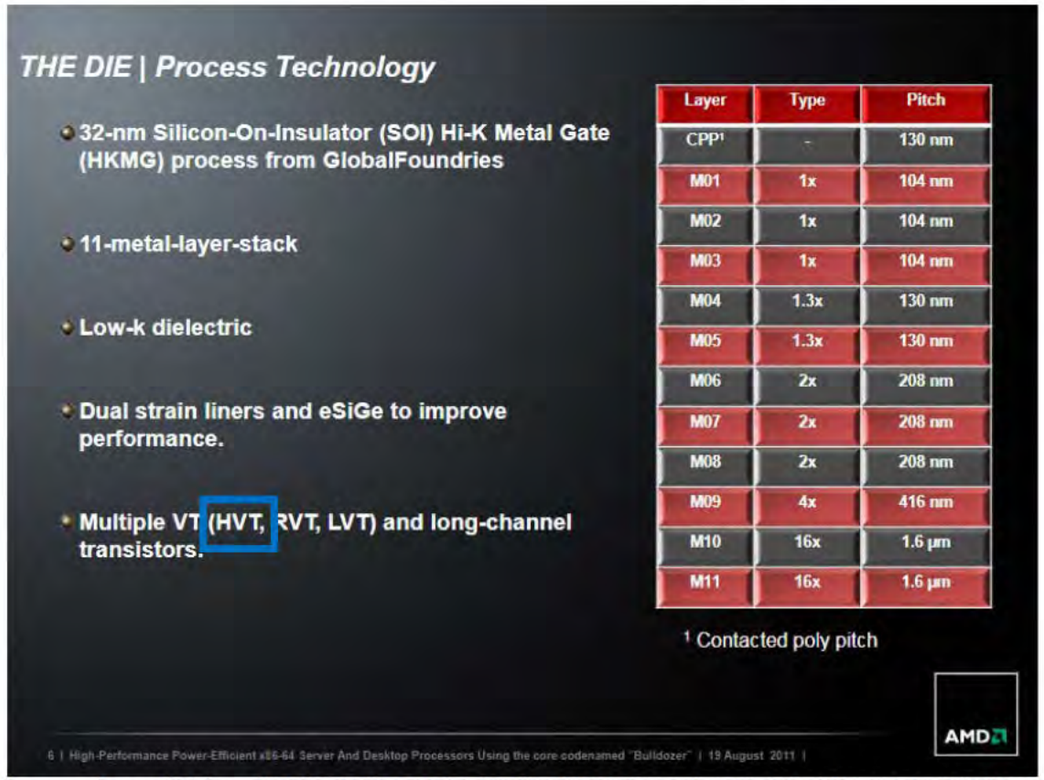
	Limitation	Contention
1p	A semiconductor integrated circuit device, comprising:	To the extent the preamble is a limitation, the Accused Products are a semiconductor integrated device.  *Source:* Sean White, *HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer"*, August 18, 2011, page 3. Aquila contends that products containing Piledriver cores operate similarly to the Bulldozer cores with respect to the limitations of the asserted claims.

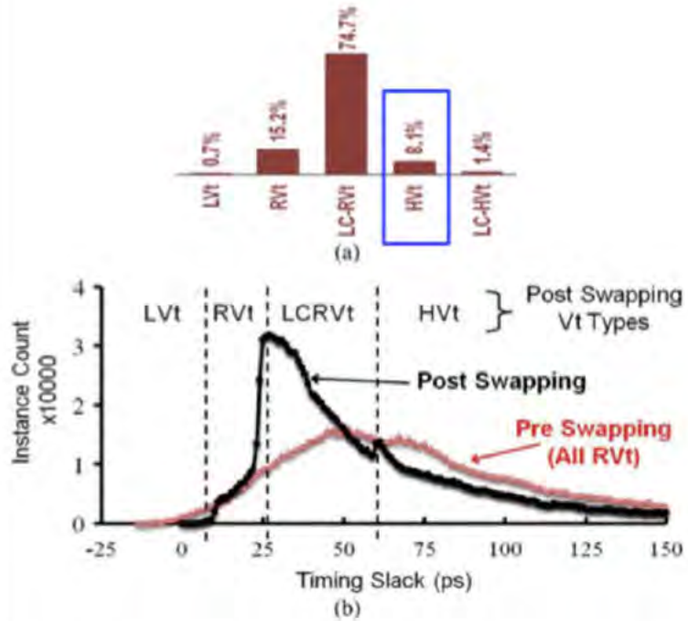
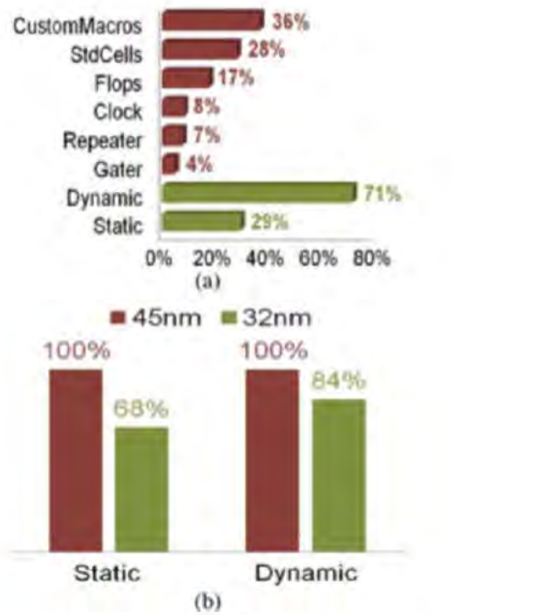
	Limitation	Contention
1a	a plurality of first unit cells each including a plurality of first MOS transistors, each of the first MOS transistors having a first threshold voltage;	The Accused Product discloses a plurality of first unit cells.  *Source:* Sean White, *HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer"*, August 18, 2011, page 3.

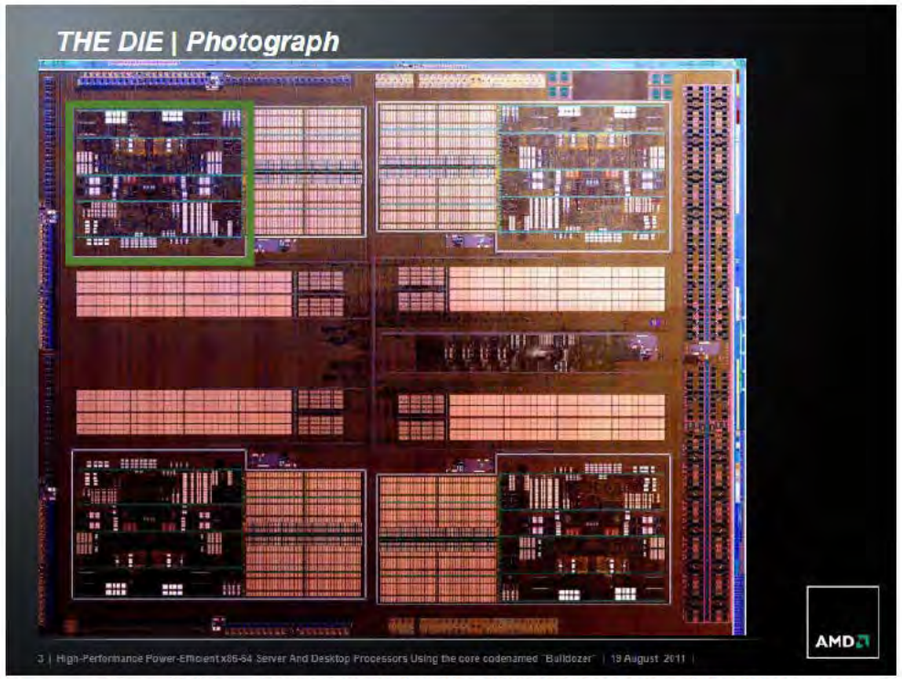
	Limitation	Contention
		 *Source:* Sean White, *HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer"*, August 18, 2011, page 5.

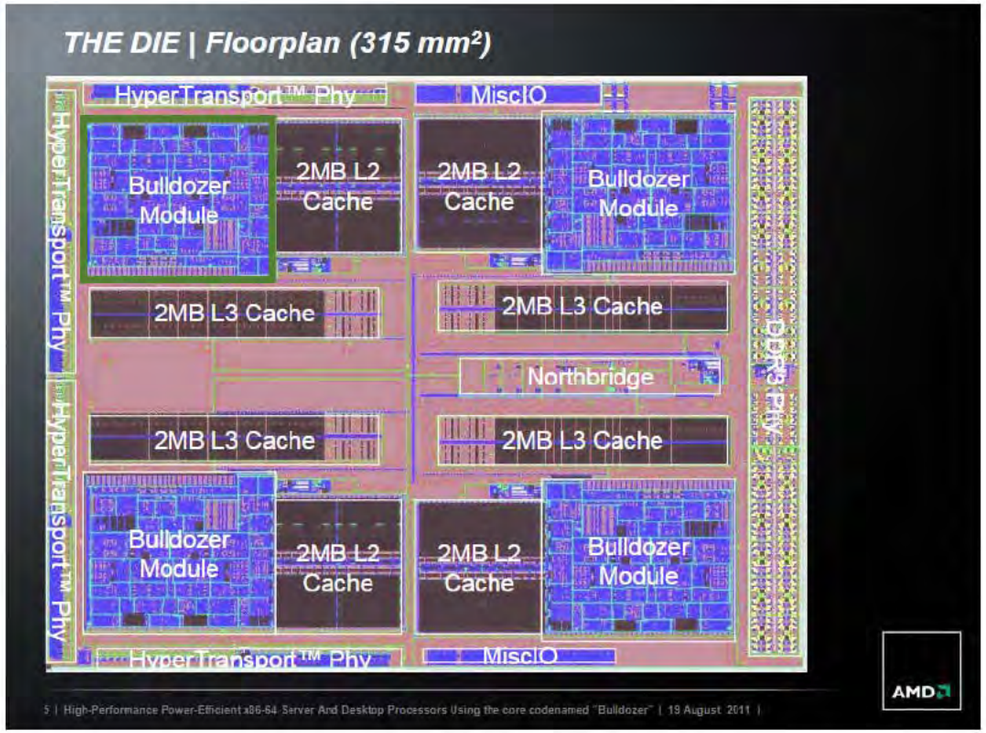
	Limitation	Contention
		The Bulldozer module contains 84 unique custom macros and 317,000 scannable flops. Module-level VSS power gating (C6) is used to reduce leakage power by approximately 95% when both cores are idle [4]. The 32 nm SOI process provides three transistor V_T types (low, regular, and high), with longer channel lengths used to achieve even finer-grained trade-offs between leakage and delay. V_T's used across the design consist mostly of regular (47%) and long-channel regular (46%), with less than 1% low-V_T used for the most critical paths. *Source:* McIntyre *et al.*, *Design Of The Two-Core x86-64 AMD "Bulldozer" Module In 32 nm SOI CMOS*, IEEE Journal of Solid-State Circuits, Vol. 47, No. 1, January 2012, page 165. Modern multi-VT standard cell design methodologies and structures such as those used in the Llano Accused Products use a mix of low Vt (LVt), regular Vt (RVt), long channel regular Vt (LC-RVt) and long channel high Vt (LC-Hvt) standard cells. 

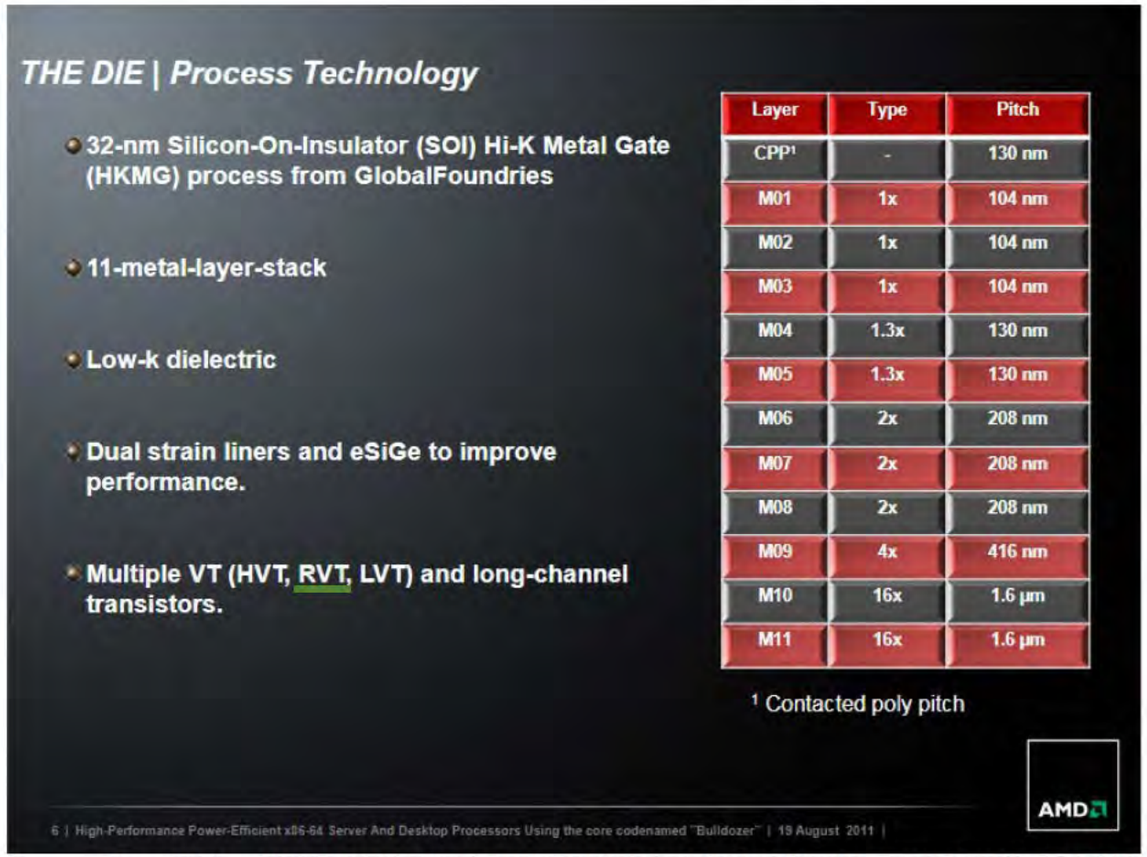
	Limitation	Contention
		DVFS Characteristics Modern computer chips are designed using multiple types of transistors, i.e. a mixture of low-, medium-, and high-threshold transistors, to target different design tradeoffs, e.g. high-performance vs. low power. Low-threshold voltage (Low-Vt) devices are used in timing-critical paths, but have high leakage power. High-threshold voltage (High-Vt) devices have low leakage power but are slower, and are typically used in circuits that are off the timing-critical paths. Medium-threshold voltage (Mid-Vt) devices offer a tradeoff between High-Vt and Low-Vt devices by having medium power requirements and medium delay. In general, low power chips are designed using a larger percentage of High-Vt devices and high-performance chips with a larger percentage of Mid-Vt and Low-Vt devices. The host processor is assumed to execute compute-intensive code and will therefore be a high-performance device. *Source:* Scrbak et al., DVFS Space Exploration in Power Constrained Processing-in-Memory Systems, pp. 4-5. The Accused Products contain a plurality of first MOS transistors, each of the first MOS transistors having a first threshold voltage.

	Limitation	Contention
		 *Source:* Sean White, *HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer"*, August 18, 2011, page 6.

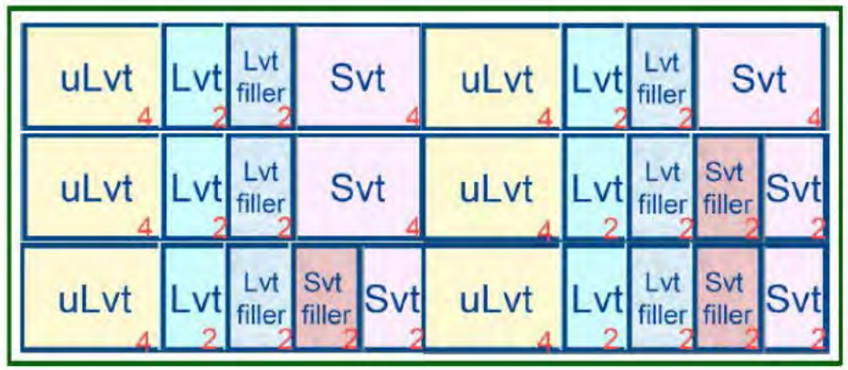
	Limitation	Contention
		JOTWANI *et al.*: AN x86-64 CORE IN 32 nm SOI CMOS 167  Fig. 10. (a) Core device width histogram by Vt type. (b) Using Vt swaps to reshape critical path timing opportunistically.  Fig. 11. (a) TDP power distribution at 1 V. (b) Relative power improvement with respect to 45 nm generation core (normalized for performance). *Source: An x86-64 Core in 32 nm SOI CMOS, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 1, JANUARY 2011,* page 6.
1b	a plurality of second unit cells each including a plurality of second MOS transistors, each of the	The Accused Products contain a plurality of second unit cells.

	Limitation	Contention
	second MOS transistors having a second threshold voltage;	 *Source:* Sean White, *HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer"*, August 18, 2011, page 3.

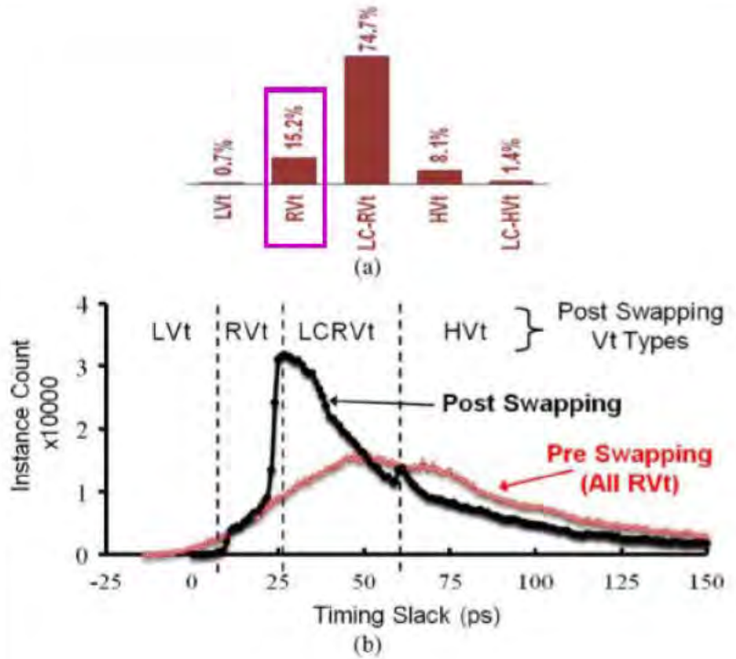
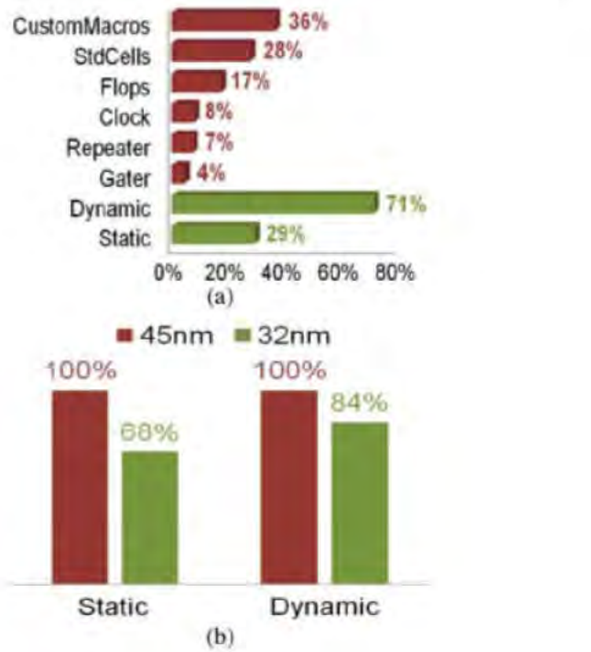
	Limitation	Contention
		 *Source:* Sean White, *HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer"*, August 18, 2011, page 5. The Accused Products contain a plurality of second MOS transistors, each of the second MOS transistors having a second threshold voltage.

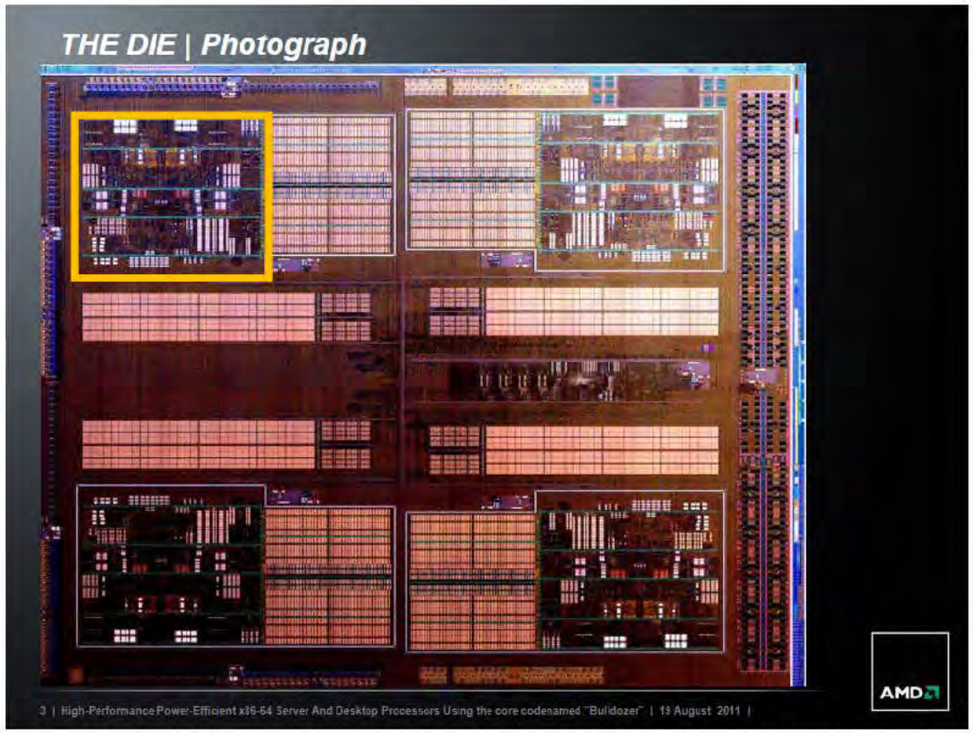
	Limitation	Contention
		

Source: Sean White, *HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer"*, August 18, 2011, page 6.

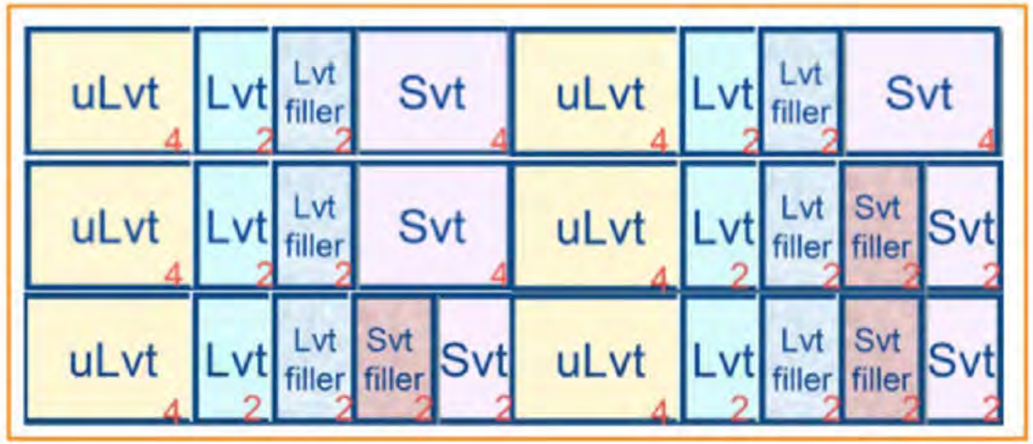
	Limitation	Contention
		The Bulldozer module contains 84 unique custom macros and 317,000 scannable flops. Module-level VSS power gating (C6) is used to reduce leakage power by approximately 95% when both cores are idle [4]. The 32 nm SOI process provides three transistor V_T types (low, regular, and high), with longer channel lengths used to achieve even finer-grained trade-offs between leakage and delay. V_T's used across the design consist mostly of regular (47%) and long-channel regular (46%), with less than 1% low-V_T used for the most critical paths. *Source:* McIntyre *et al.*, *Design Of The Two-Core x86-64 AMD "Bulldozer" Module In 32 nm SOI CMOS*, IEEE Journal of Solid-State Circuits, Vol. 47, No. 1, January 2012, page 165. Modern multi-VT standard cell design methodologies and structures such as those used in the Llano Accused Products use a mix of low Vt (LVt), regular Vt (RVt), long channel regular Vt (LC-RVt) and long channel high Vt (LC-Hvt) standard cells. 

	Limitation	Contention
		DVFS Characteristics Modern computer chips are designed using multiple types of transistors, i.e. a mixture of low-, medium-, and high-threshold transistors, to target different design tradeoffs, e.g. high-performance vs. low power. Low-threshold voltage (Low-Vt) devices are used in timing-critical paths, but have high leakage power. High-threshold voltage (High-Vt) devices have low leakage power but are slower, and are typically used in circuits that are off the timing-critical paths. Medium-threshold voltage (Mid-Vt) devices offer a tradeoff between High-Vt and Low-Vt devices by having medium power requirements and medium delay. In general, low power chips are designed using a larger percentage of High-Vt devices and high-performance chips with a larger percentage of Mid-Vt and Low-Vt devices. The host processor is assumed to execute compute-intensive code and will therefore be a high-performance device. *Source:* Scrbak et al., DVFS Space Exploration in Power Constrained Processing-in-Memory Systems, pp. 4-5. The Accused Products contain a plurality of second MOS transistors, each of the second MOS transistors having a second threshold voltage:

	Limitation	Contention
		 Fig. 10. (a) Core device width histogram by Vt type. (b) Using Vt swaps to reshape critical path timing opportunistically.  Fig. 11. (a) TDP power distribution at 1 V. (b) Relative power improvement with respect to 45 nm generation core (normalized for performance). *Source: An x86-64 Core in 32 nm SOI CMOS, page 6 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 1, JANUARY 2011*
1c	a unit cell array comprised of said first and second unit cells laid in array form;	The Accused Products contain a unit cell array comprised of said first and second unit cells laid in array form:

	Limitation	Contention
		 *Source:* Sean White, *HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer"*, August 18, 2011, page 3. Modern multi-VT standard cell design methodologies and structures such as those used in the Llano Accused Products use a mix of low Vt (LVt), regular Vt (RVt), long channel regular Vt (LC-RVt) and long channel high Vt (LC-Hvt) standard cells.

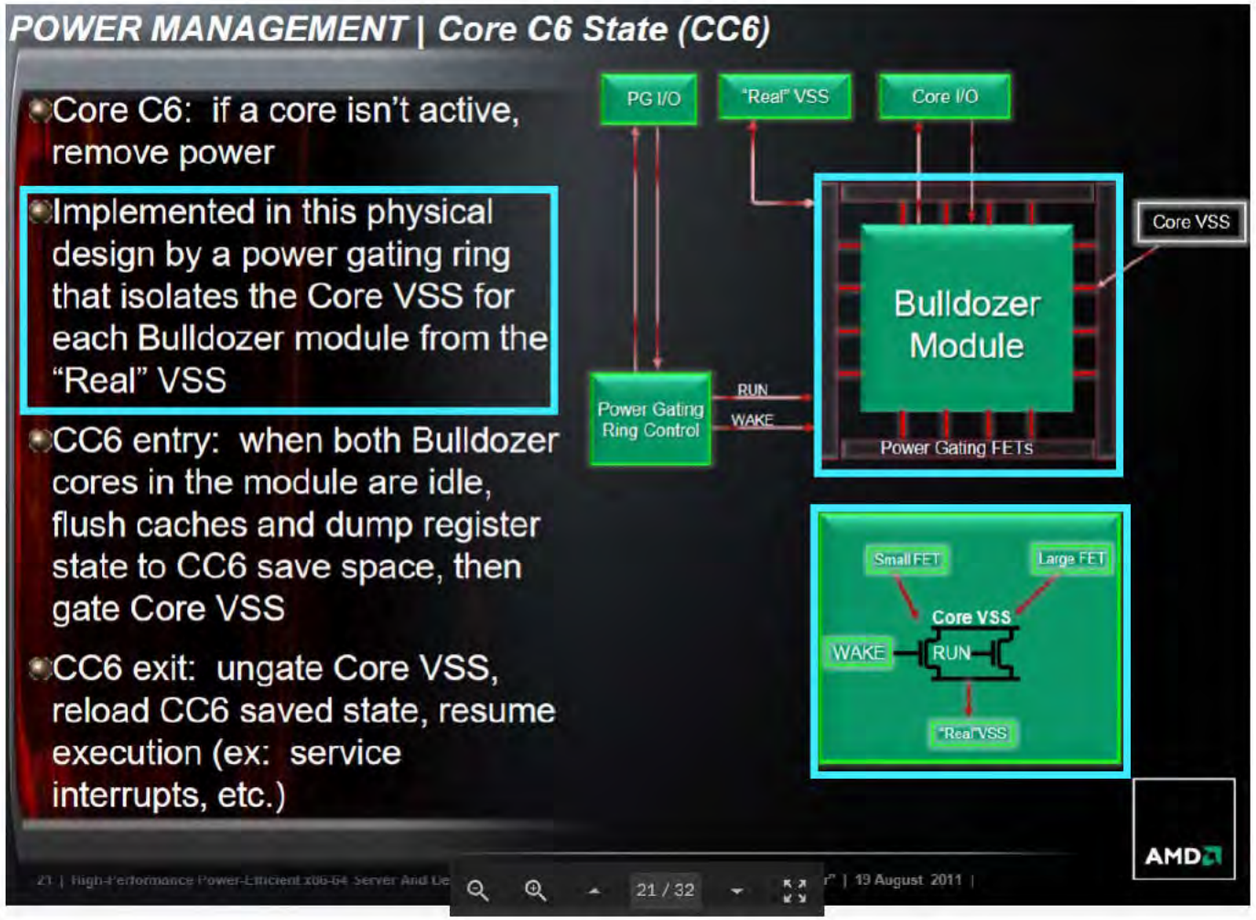
	Limitation	Contention

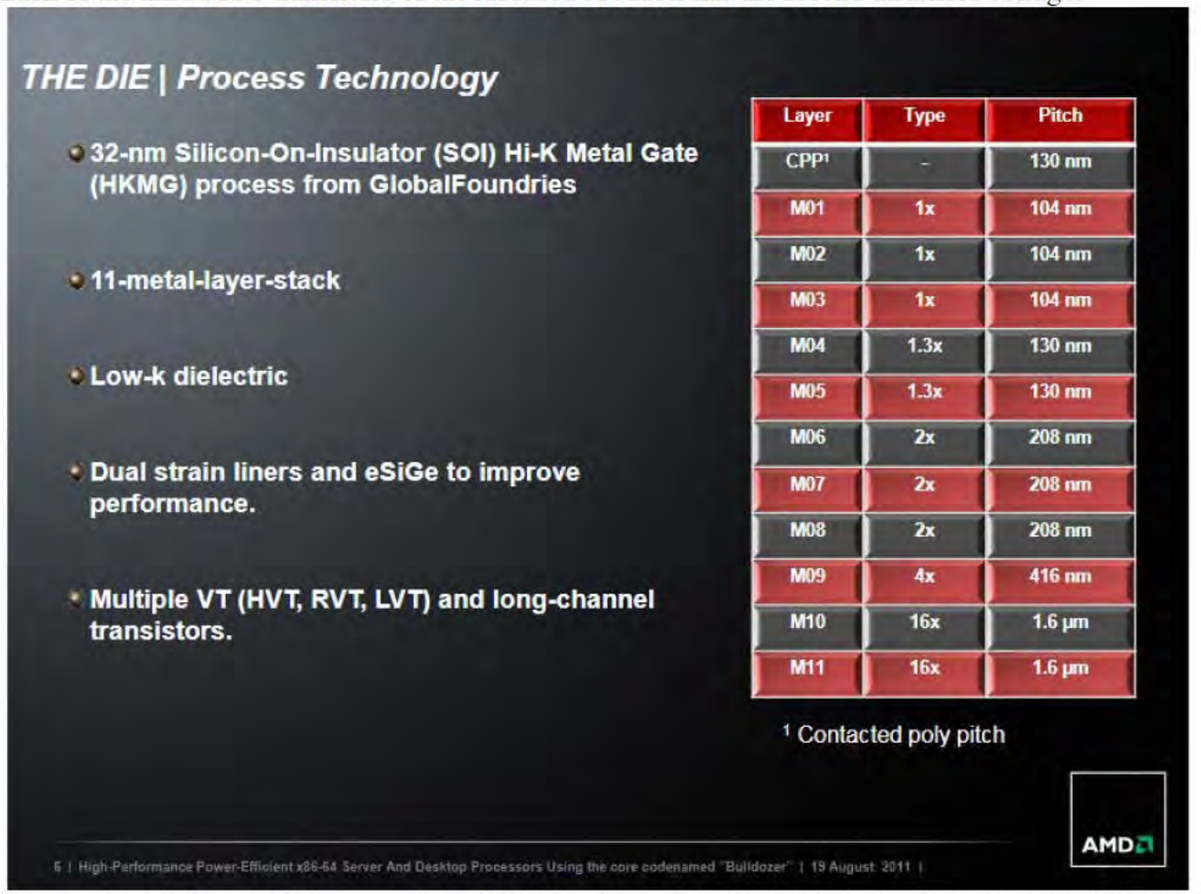


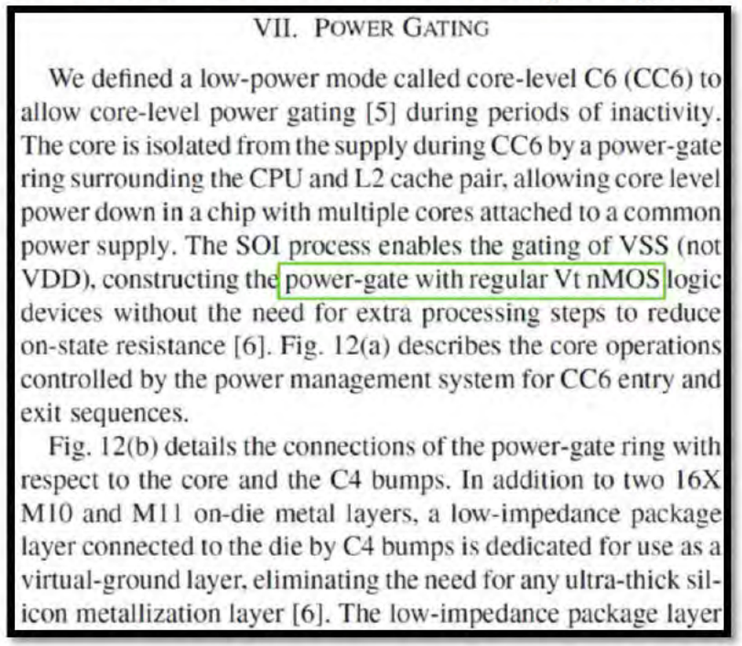
DVFS Characteristics Modern computer chips are designed using multiple types of transistors, i.e. a mixture of low-, medium-, and high-threshold transistors, to target different design tradeoffs, e.g. high-performance vs. low power.

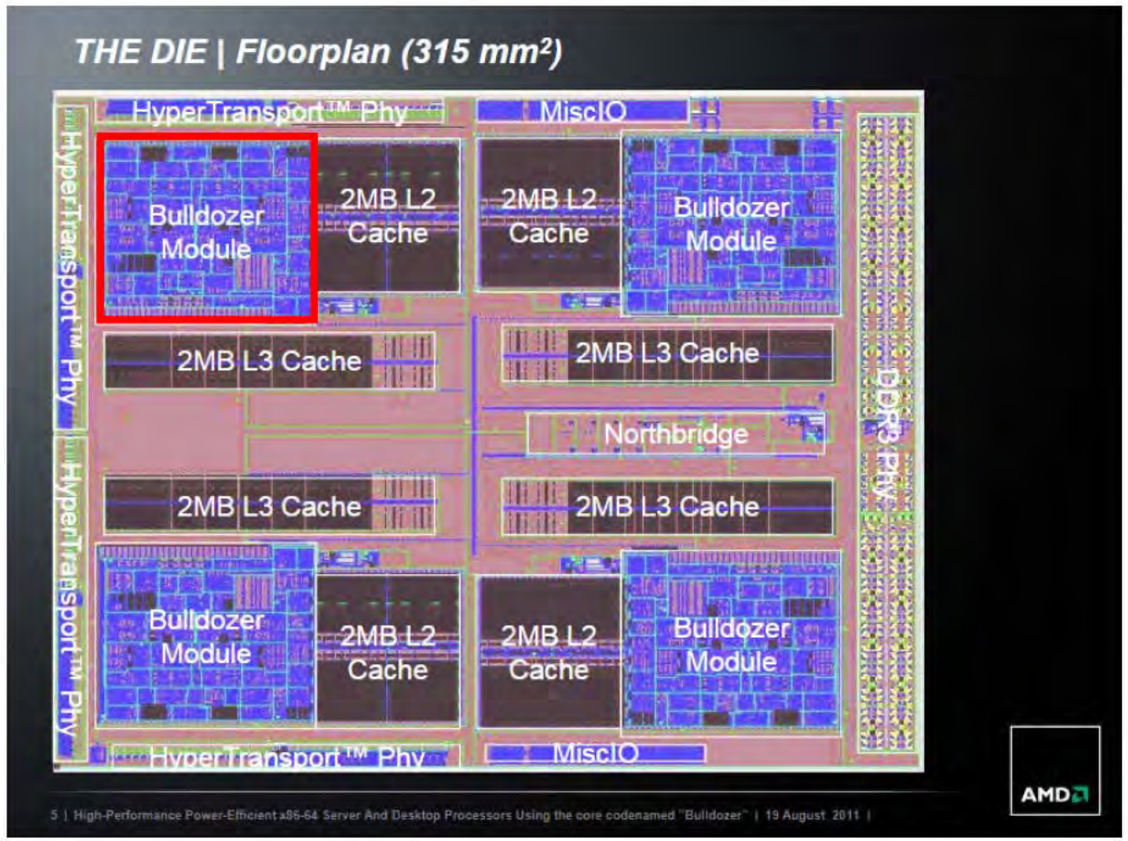
Low-threshold voltage (Low-Vt) devices are used in timing-critical paths, but have high leakage power. High-threshold voltage (High-Vt) devices have low leakage power but are slower, and are typically used in circuits that are off the timing-critical paths. Medium-threshold voltage (Mid-Vt) devices offer a tradeoff between High-Vt and Low-Vt devices by having medium power requirements and medium delay. In general, low power chips are designed using a larger percentage of High-Vt devices and high-performance chips with a larger percentage of Mid-Vt and Low-Vt devices. The host processor is assumed to execute compute-intensive code and will therefore be a high-performance device.

Source: Scrbak et al., DVFS Space Exploration in Power Constrained Processing-in-Memory Systems, pp. 4-5.

	Limitation	Contention
1d	a power switch disposed around said unit cell array and comprised of a plurality of third MOS transistors, each of the third MOS transistors having the second threshold voltage; and	The Accused Products contain a power switch disposed around said unit cell array and comprised of a pluraility of third MOS transistors. 

	Limitation	Contention
		Source: Sean White, *HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer"*, August 18, 2011, page 21. Each of the third MOS transistors of the Accused Products has the second threshold voltage:  *Source:* Sean White, *HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the*

	Limitation	Contention
		core code named "Bulldozer", August 18, 2011, page 6. Each of the third MOS transistors of the power gate ring has the second threshold voltage.  VII. POWER GATING We defined a low-power mode called core-level C6 (CC6) to allow core-level power gating [5] during periods of inactivity. The core is isolated from the supply during CC6 by a power-gate ring surrounding the CPU and L2 cache pair, allowing core level power down in a chip with multiple cores attached to a common power supply. The SOI process enables the gating of VSS (not VDD), constructing the power-gate with regular Vt nMOS logic devices without the need for extra processing steps to reduce on-state resistance [6]. Fig. 12(a) describes the core operations controlled by the power management system for CC6 entry and exit sequences. Fig. 12(b) details the connections of the power-gate ring with respect to the core and the C4 bumps. In addition to two 16X M10 and M11 on-die metal layers, a low-impedance package layer connected to the die by C4 bumps is dedicated for use as a virtual-ground layer, eliminating the need for any ultra-thick silicon metallization layer [6]. The low-impedance package layer *Source: An x86-64 Core in 32 nm SOI CMOS, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 1, JANUARY 2011,* page 6.
1e	a plurality of input/output circuits disposed around said unit cell array.	The Accused Product has a plurality of input/output circuits disposed around the Bulldozer module.

	Limitation	Contention
		 *Source:* Sean White, *HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer"*, August 18, 2011, page 5.
2	A semiconductor integrated circuit	The power gate ring is turned off during standby and turned on when the core exits C6 state.

	Limitation	Contention
	device according to claim 1, wherein said power switch is turned off during standby and turned on when taken active.	The Bulldozer module contains 84 unique custom macros and 317,000 scannable flops. Module-level VSS power gating (C6) is used to reduce leakage power by approximately 95% when both cores are idle [4]. The 32 nm SOI process provides three transistor V_T types (low, regular, and high), with longer channel lengths used to achieve even finer-grained trade-offs between leakage and delay. V_T's used across the design consist mostly of regular (47%) and long-channel regular (46%), with less than 1% low-V_T used for the most critical paths. *Source:* McIntyre *et al.*, *Design Of The Two-Core x86-64 AMD "Bulldozer" Module In 32 nm SOI CMOS*, IEEE Journal of Solid-State Circuits, Vol. 47, No. 1, January 2012, page 165.

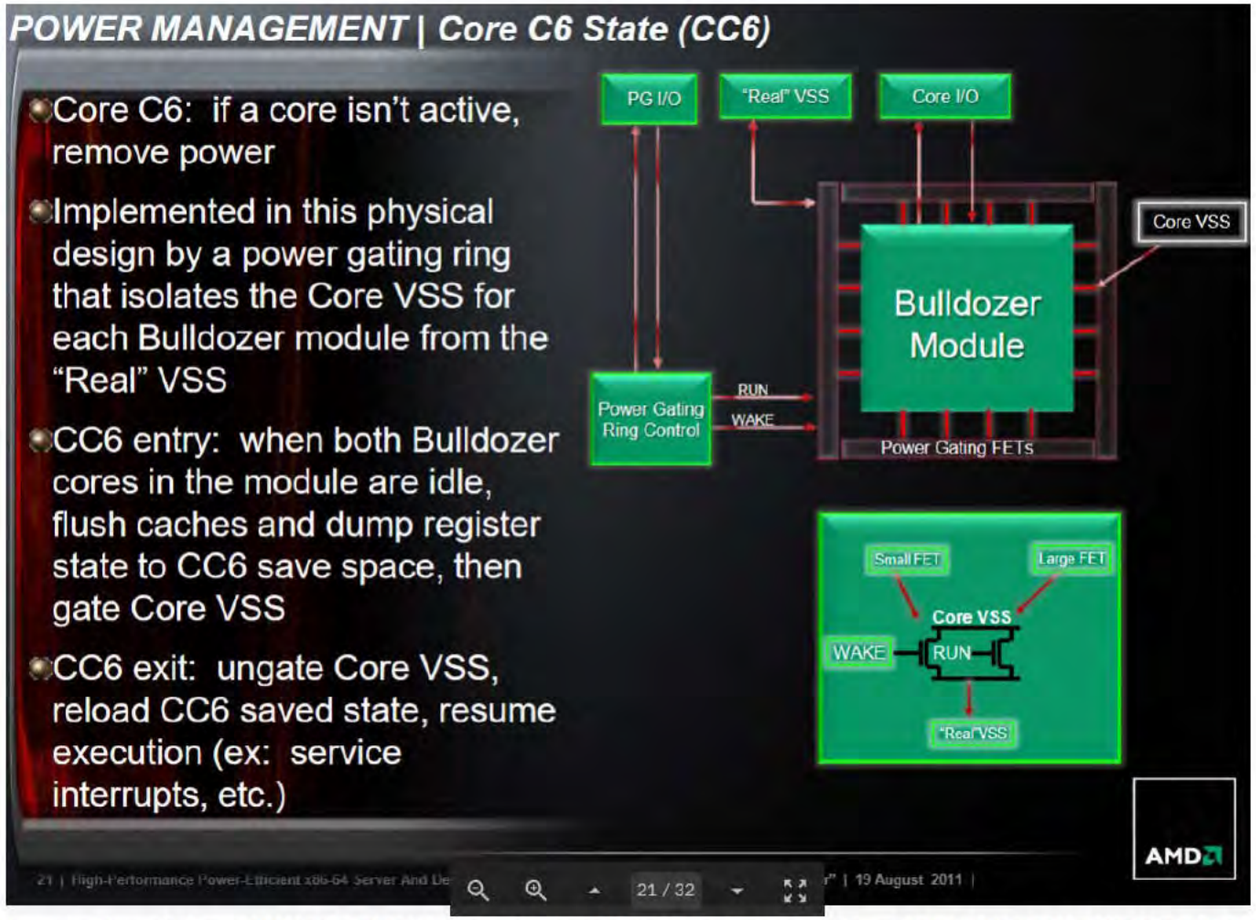
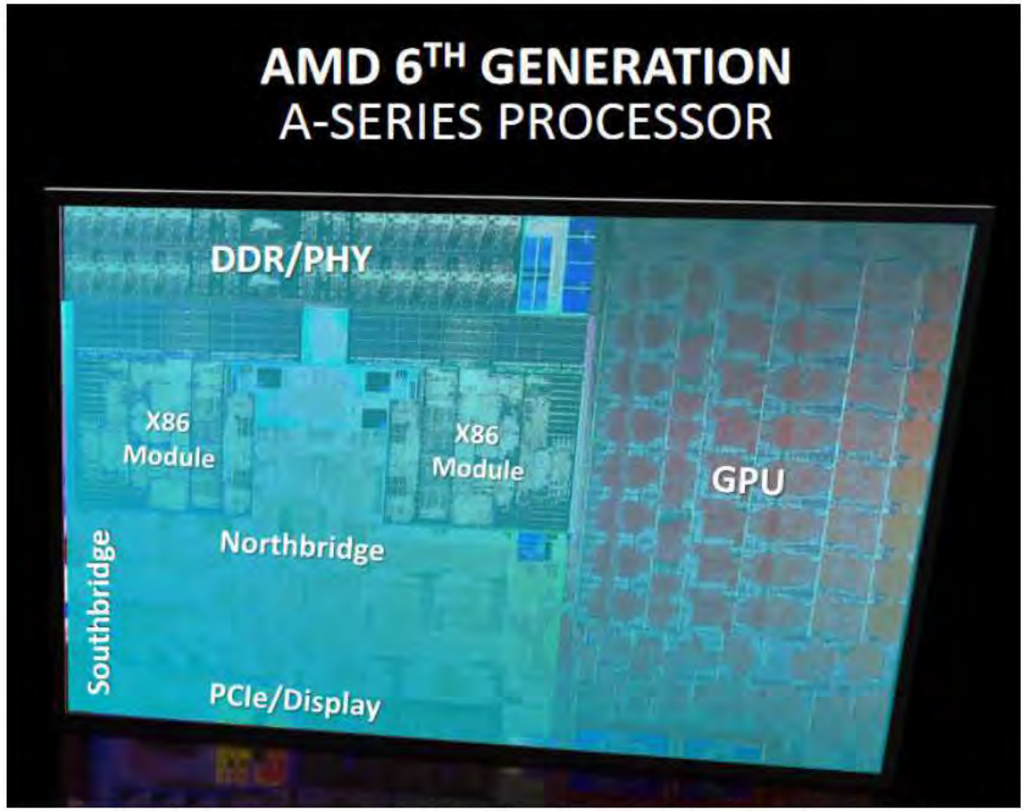
	Limitation	Contention
		 *Source:* Sean White, *HIGH-PERFORMANCE POWER-EFFICIENT X86-64 SERVER AND DESKTOP PROCESSORS: Using the core code named "Bulldozer"*, August 18, 2011, page 21.

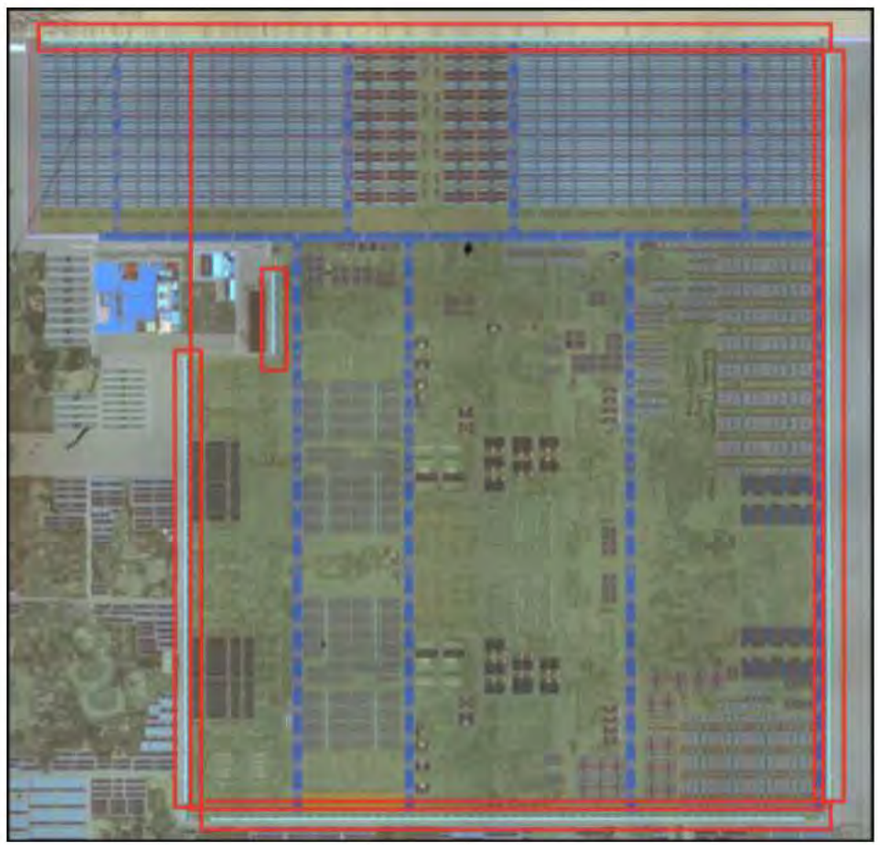
Exhibit A.3: Preliminary Infringement Contention Charts for U.S. Patent 6,239,614

Accused Product: AMD APUs containing Excavator cores (Representative Product: AMD Carrizo APU Processors)

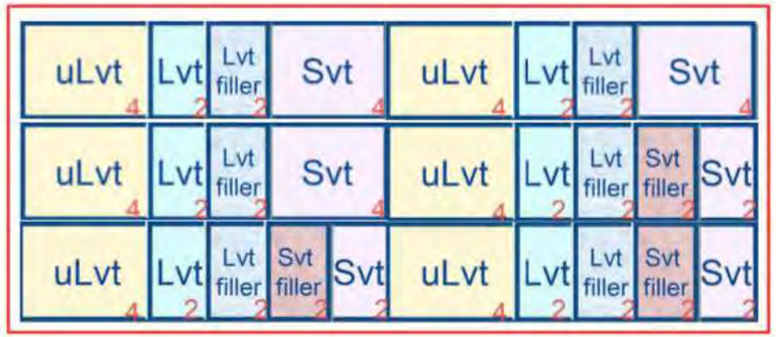
These preliminary infringement contentions were prepared without the benefit of the Court's claim construction or the parties' exchange of constructions. As of the date of these contentions, AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court's constructions or to account for new information that becomes available.

	Limitation	Contention
1p	A semiconductor integrated circuit device, comprising:	To the extent the preamble is a limitation, the Accused Products are semiconductor integrated circuits.

	Limitation	Contention
		 Source: Krishnan, Energy Efficient Graphics and Multimedia in 28nm Carrizo APU | Hot Chips 27, p. 2. To the extent that the power gate ring implemented in this product operates similarly to the Bulldozer or Llano power gate rings, for example in terms of the threshold voltages of the MOS transistors in the various unit cells and the power switch, Aquila contends that the charts applicable to those products apply equally to this product,

	Limitation	Contention
		and incorporates those charts by reference.
1a	a plurality of first unit cells each including a plurality of first MOS transistors, each of the first MOS transistors having a first threshold voltage;	The Accused Products disclose a plurality of first unit cells: 

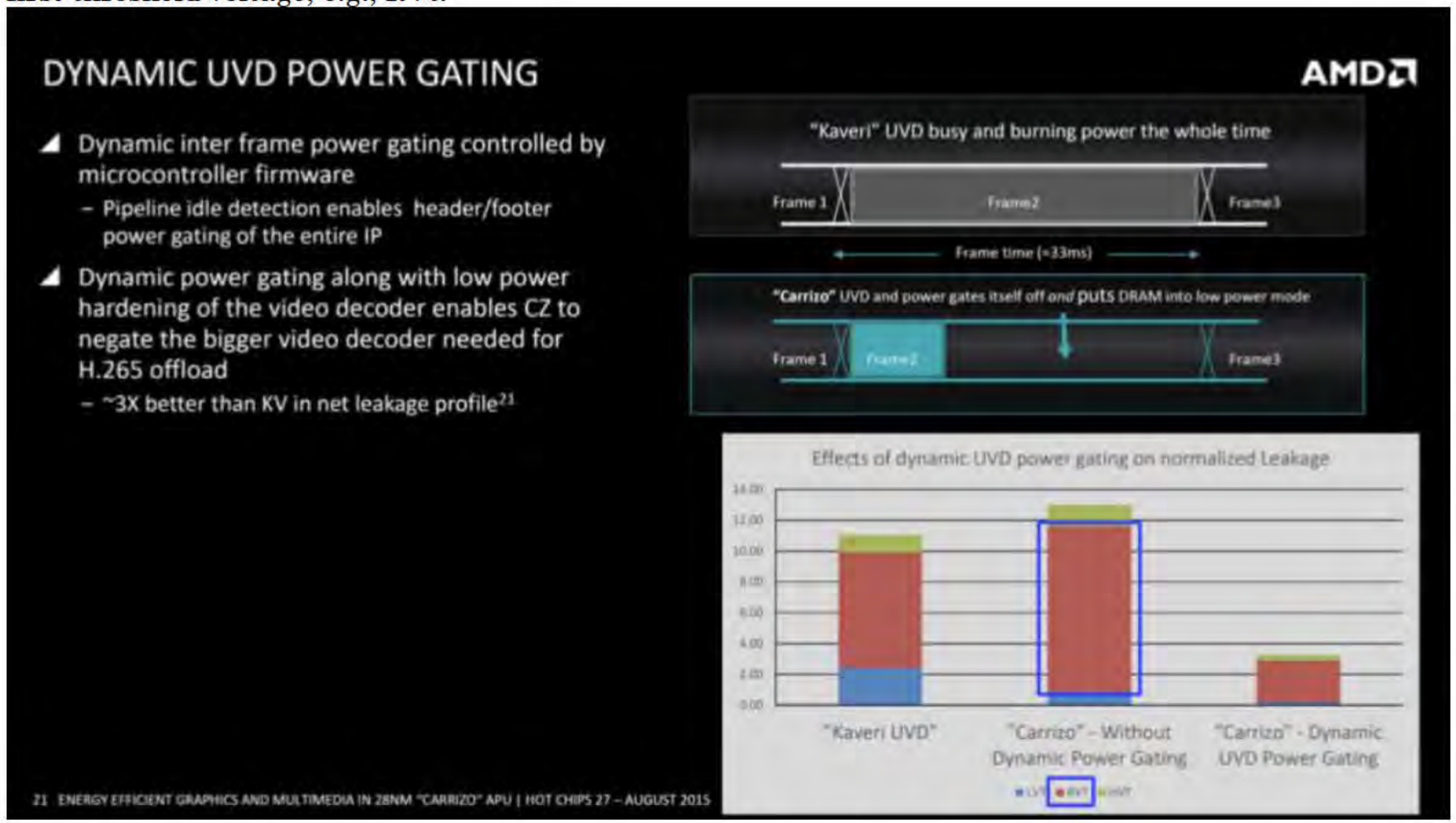
	Limitation	Contention
		Modern multi-VT standard cell design methodologies and structures such as those used in the Llano Accused Products use a mix of low Vt (LVt), regular Vt (RVt), long channel regular Vt (LC-RVt) and long channel high Vt (LC-Hvt) standard cells.

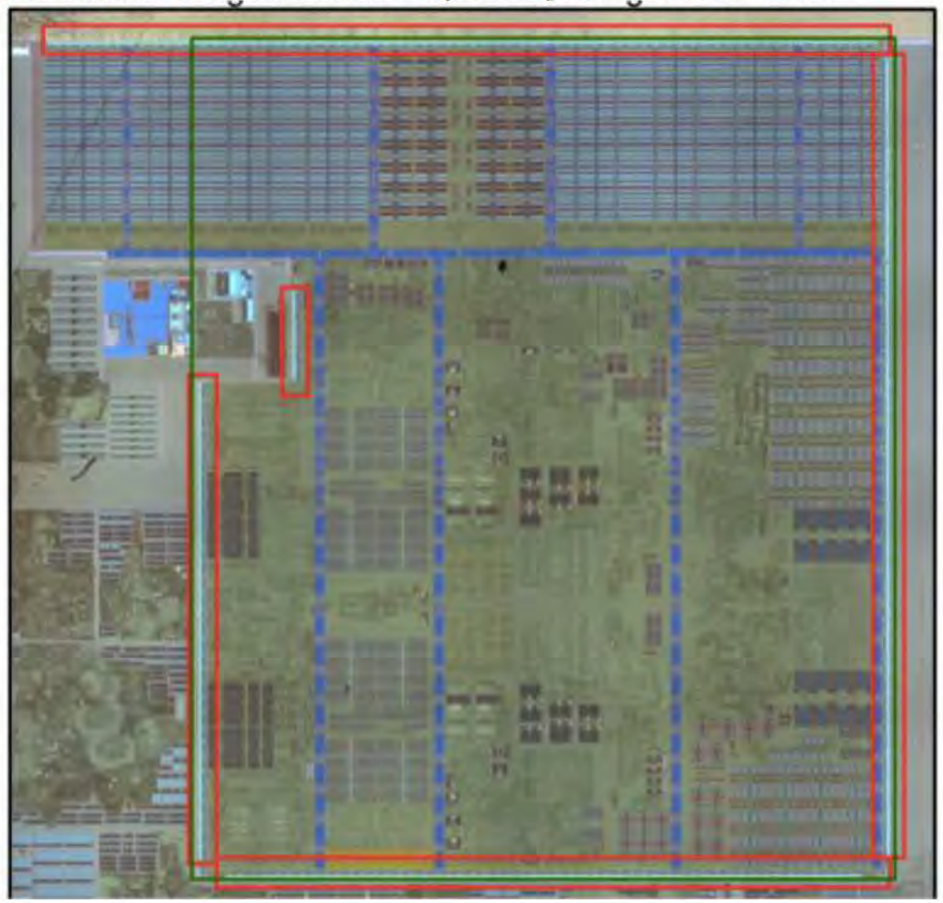


DVFS Characteristics Modern computer chips are designed using multiple types of transistors, i.e. a mixture of low-, medium-, and high-threshold transistors, to target different design tradeoffs, e.g. high-performance vs. low power.

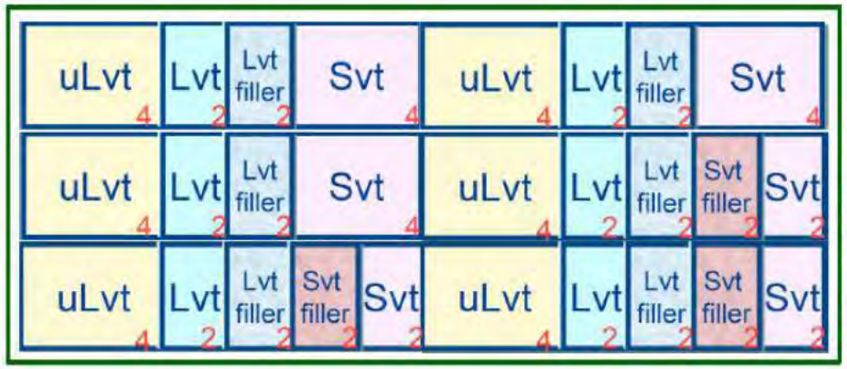
Low-threshold voltage (Low-Vt) devices are used in timing-critical paths, but have high leakage power. High-threshold voltage (High-Vt) devices have low leakage power but are slower, and are typically used in circuits that are off the timing-critical paths. Medium-threshold voltage (Mid-Vt) devices offer a tradeoff between High-Vt and Low-Vt devices by having medium power requirements and medium delay. In general, low power chips are designed using a larger percentage of High-Vt devices and high-performance chips with a larger percentage of Mid-Vt and Low-Vt devices. The host processor is assumed to execute compute-intensive code and will therefore be a high-performance device.

Source: Scrbak et al., DVFS Space Exploration in Power Constrained Processing-in-Memory Systems, pp. 4-5.

	Limitation	Contention
		The Accused Products disclose a plurality of first MOS transistors, each of the first MOS transistors having a first threshold voltage, e.g., RVt:  *Source: ENERGY EFFICIENT GRAPHICS AND MULTIMEDIA IN 28NM CARRIZO APU, page 21 HOT CHIPS 27 – AUGUST 2015*

	Limitation	Contention
1b	a plurality of second unit cells each including a plurality of second MOS transistors, each of the second MOS transistors having a second threshold voltage;	The Accused Products disclose a plurality of second unit cells:  Modern multi-VT standard cell design methodologies and structures such as those used in the Llano Accused Products use a mix of low Vt (LVt), regular Vt (RVt), long channel regular Vt (LC-RVt) and long channel high Vt

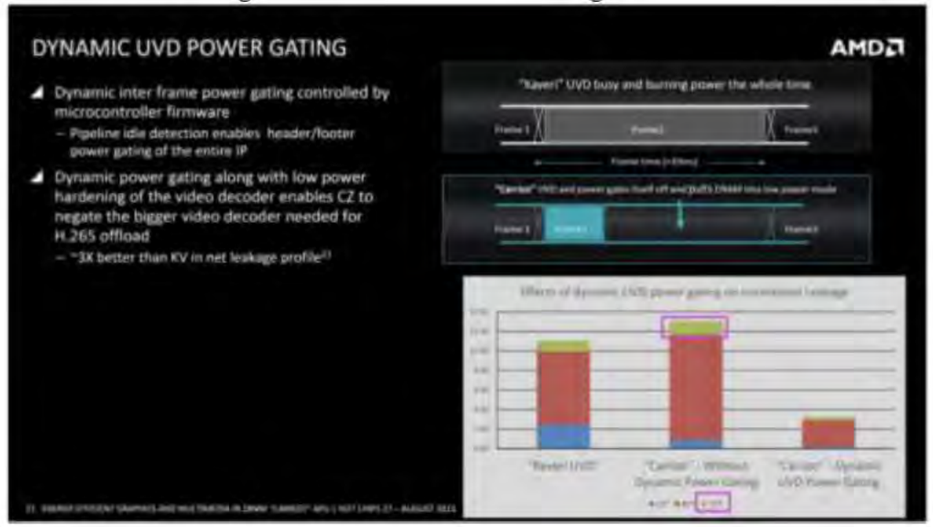
	Limitation	Contention
		(LC-Hvt) standard cells.

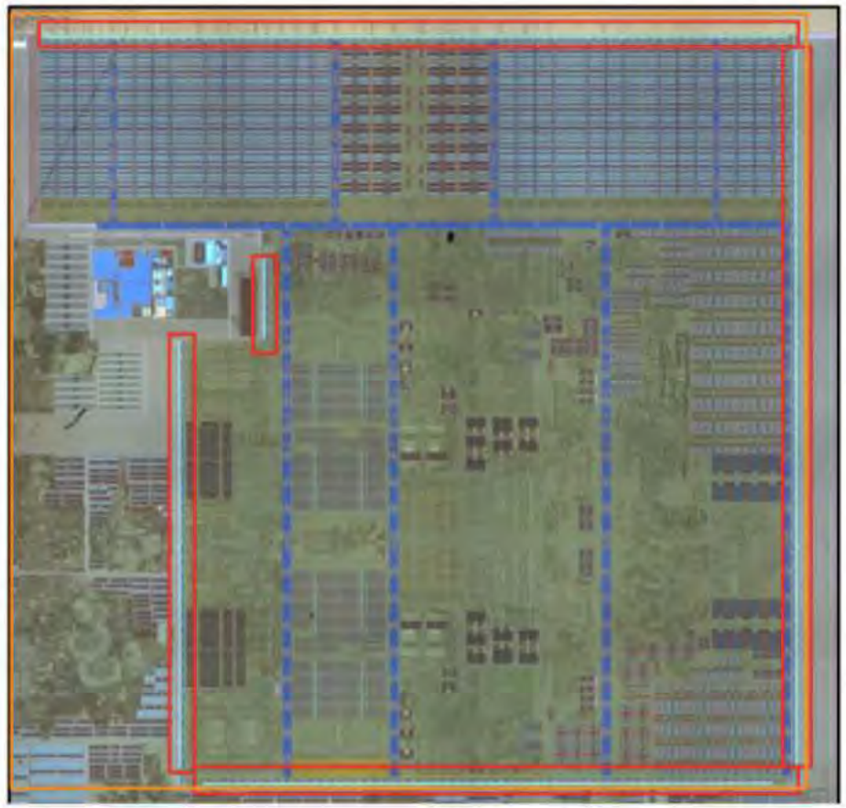


DVFS Characteristics Modern computer chips are designed using multiple types of transistors, i.e. a mixture of low-, medium-, and high-threshold transistors, to target different design tradeoffs, e.g. high-performance vs. low power.

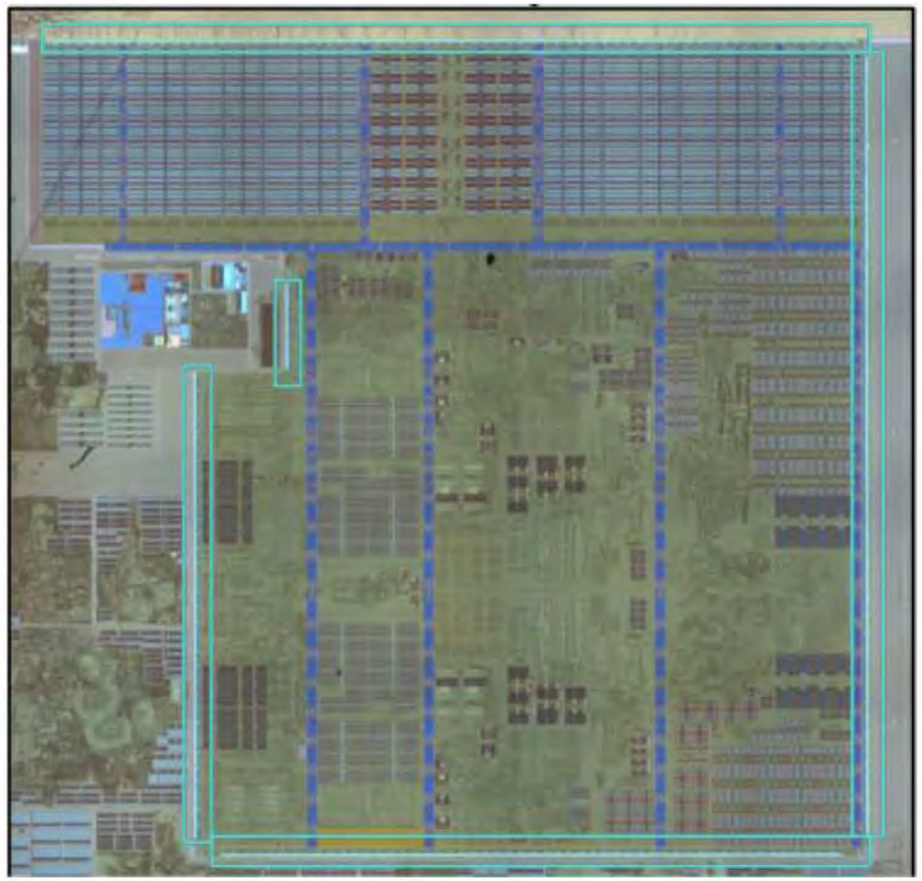
Low-threshold voltage (Low-Vt) devices are used in timing-critical paths, but have high leakage power. High-threshold voltage (High-Vt) devices have low leakage power but are slower, and are typically used in circuits that are off the timing-critical paths. Medium-threshold voltage (Mid-Vt) devices offer a tradeoff between High-Vt and Low-Vt devices by having medium power requirements and medium delay. In general, low power chips are designed using a larger percentage of High-Vt devices and high-performance chips with a larger percentage of Mid-Vt and Low-Vt devices. The host processor is assumed to execute compute-intensive code and will therefore be a high-performance device.

Source: Scrbak et al., DVFS Space Exploration in Power Constrained Processing-in-Memory Systems, pp. 4-5.

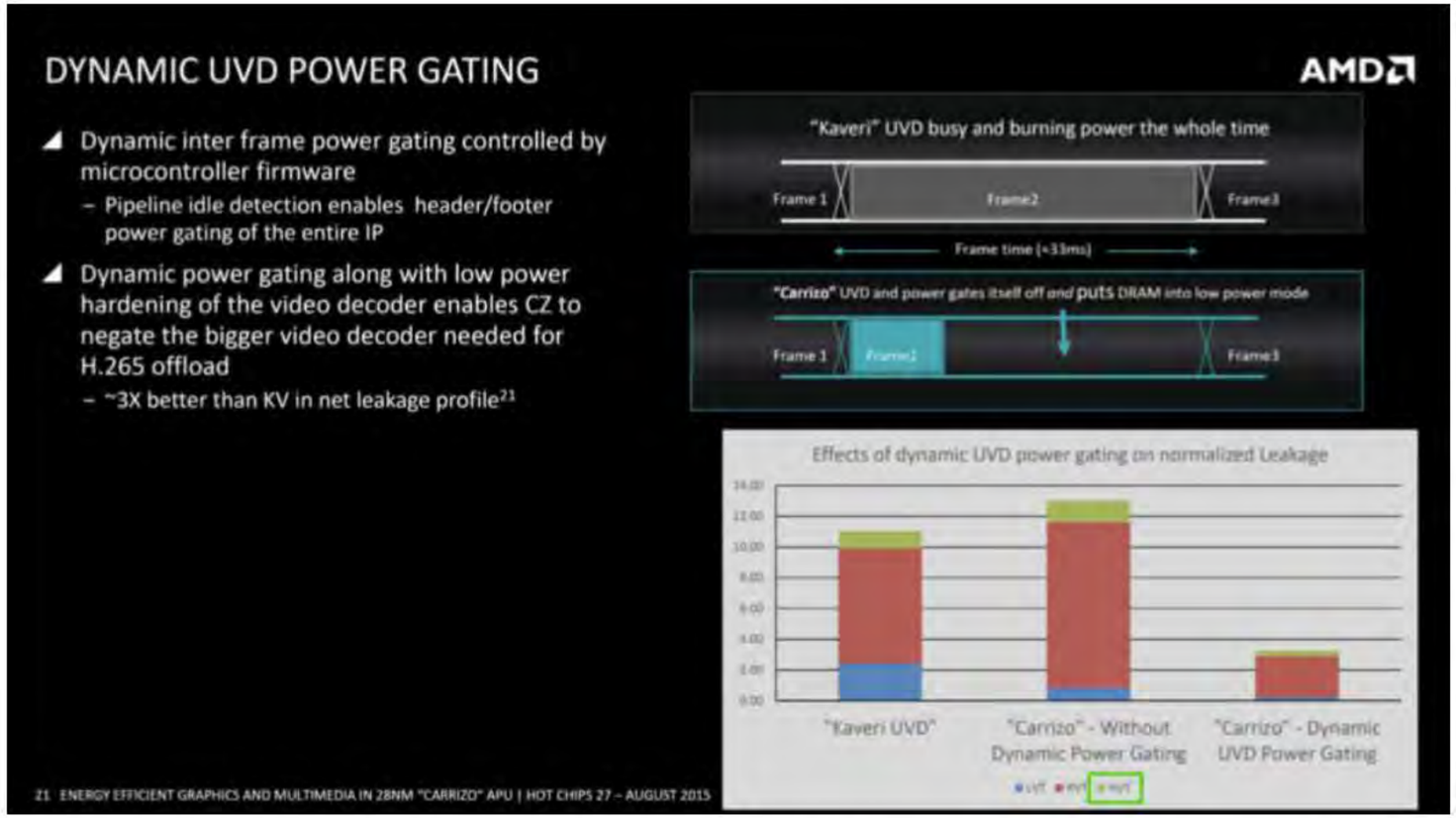
	Limitation	Contention
		The Accused Products disclose a plurality of second unit cells each including a plurality of second MOS transistors having a second threshold voltage:  *Source: ENERGY EFFICIENT GRAPHICS AND MULTIMEDIA IN 28NM CARRIZO APU, HOT CHIPS 27 – AUGUST 2015,* page 21.
1c	a unit cell array comprised of said first and second unit cells laid in array form;	The Accused Products disclose a unit cell array comprised of said first and second unit cells laid in array form:

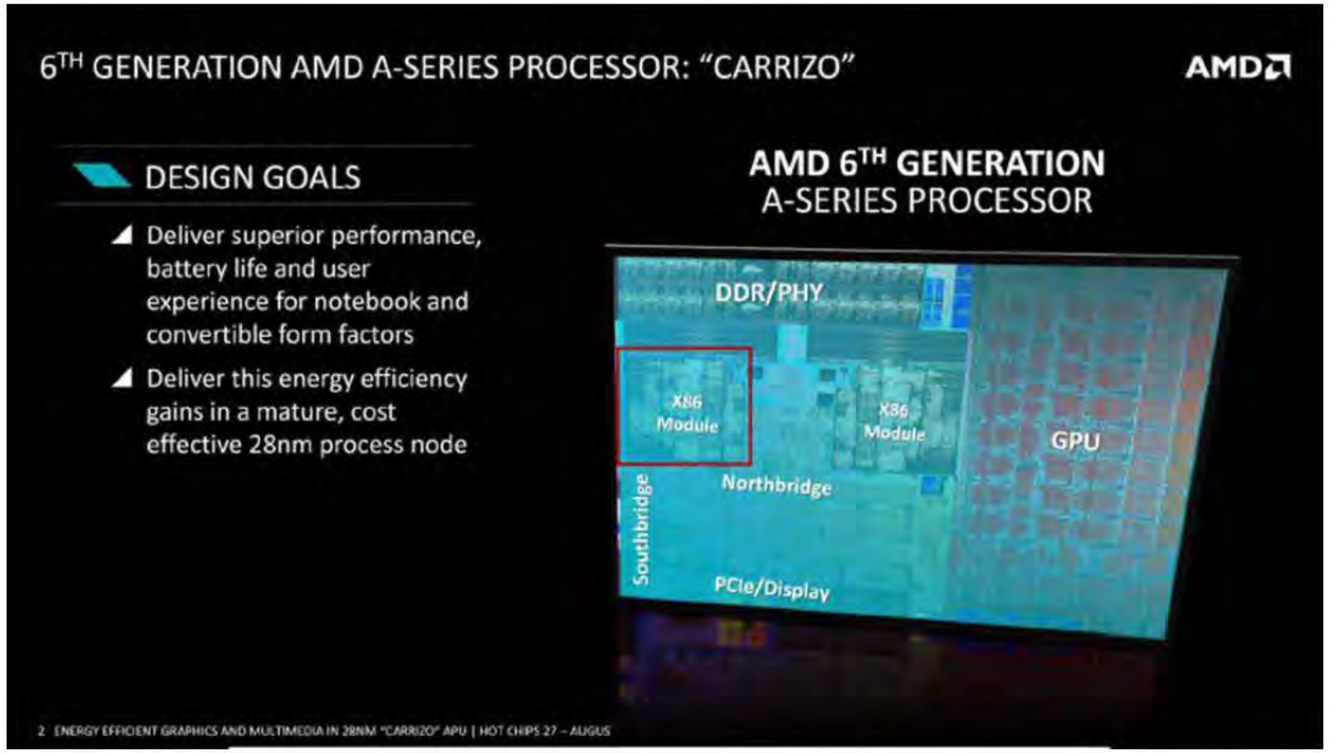
	Limitation	Contention
		
1d	a power switch disposed around said unit cell array and comprised of a plurality of third MOS transistors, each of the third MOS transistors having the second threshold	The Accused Products disclose a power gate ring disposed around said unit cell array:

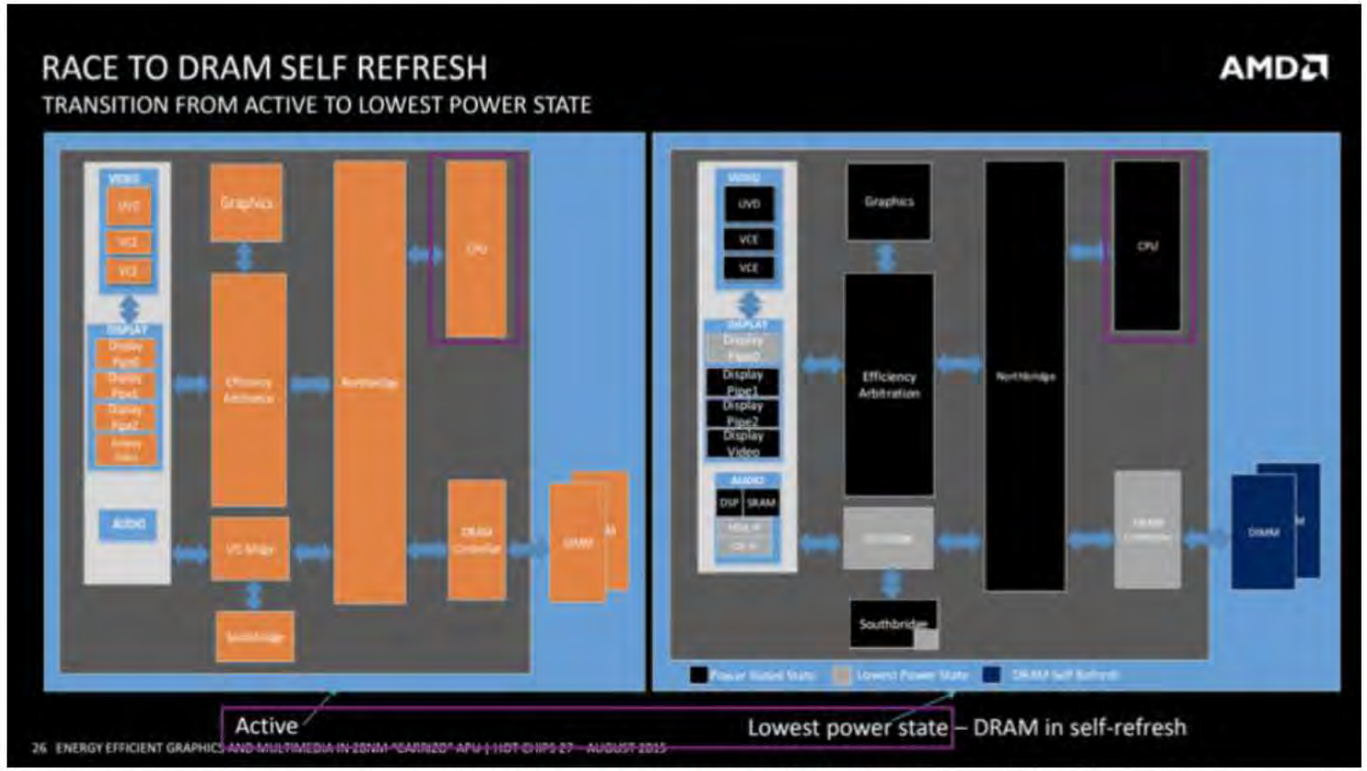
	Limitation	Contention
	voltage; and	Instead of the distributed power gate headers used in Steamroller, a power gate ring is used to reduce the size of the power switch required to support Excavator's higher power density. Distributed headers must be sized to accommodate the worst case current draw within small regions of the design, whereas a power gate ring need only be sized to accommodate the worst case across the entire power gated region. This enables a 3.5–4× reduction in FET width in the Excavator power switch and a corresponding leakage power reduction when it is in CC6 (sleep state). *Source: Carrizo: A High Performance, Energy Efficient 28 nm APU, page 5 IEEE JOURNAL OF SOLID-STATE CIRCUITS*

	Limitation	Contention
		 The Accused Products disclose a power switch comprised of a pluraility of third MOS transistors:

	Limitation	Contention
		Instead of the distributed power gate headers used in Steamroller, a power gate ring is used to reduce the size of the power switch required to support Excavator's higher power density. Distributed headers must be sized to accommodate the worst case current draw within small regions of the design, whereas a power gate ring need only be sized to accommodate the worst case across the entire power gated region. This enables a 3.5–4× reduction in FET width in the Excavator power switch and a corresponding leakage power reduction when it is in CC6 (sleep state). *Source: Carrizo: A High Performance, Energy Efficient 28 nm APU, IEEE JOURNAL OF SOLID-STATE CIRCUITS,* page 5. The Accused Products disclose each of the third MOS transistors having the second threshold voltage:

	Limitation	Contention
		 *Source: ENERGY EFFICIENT GRAPHICS AND MULTIMEDIA IN 28NM CARRIZO APU, HOT CHIPS 27 – AUGUST 2015*, page 21.
1e	a plurality of input/output circuits disposed around said	The Accused Products disclose the limitation of a plurality of input/output circuits disposed around said unit cell array.

	Limitation	Contention
	unit cell array.	 *Source: ENERGY EFFICIENT GRAPHICS AND MULTIMEDIA IN 28NM CARRIZO APU, page 2 HOT CHIPS 27 – AUGUST 2015.*
2	A semiconductor integrated circuit device according to claim 1, wherein said power	The Accused Products disclose that said power switch is turned off during standby and turned on when taken active.

	Limitation	Contention
	switch is turned off during standby and turned on when taken active.	 *Source: ENERGY EFFICIENT GRAPHICS AND MULTIMEDIA IN 28NM CARRIZO APU, page 26 HOT CHIPS 27 – AUGUST 2015.*

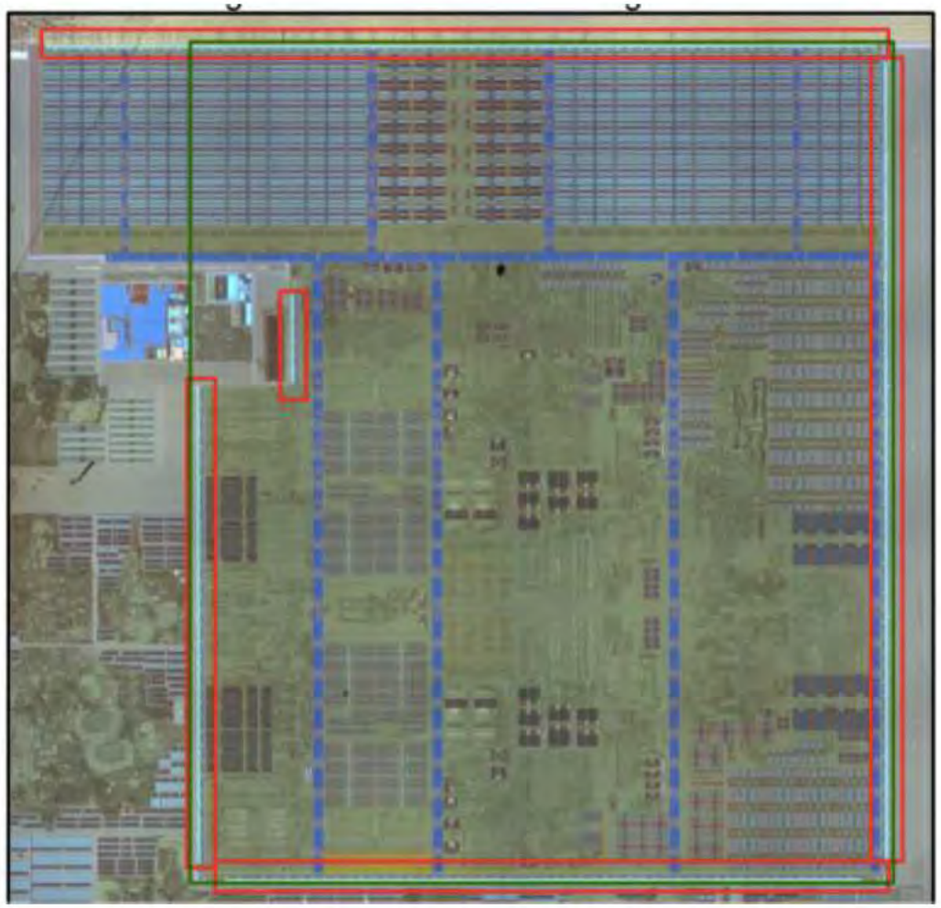
	Limitation	Contention
3	The semiconductor integrated circuit device according to claim 1, wherein parts of said power switch are disposed within said unit cell array.	

Exhibit B.1: Preliminary Infringement Claim Chart for U.S. Patent 6,895,519

Accused Products: AMD Family 14h Products

These preliminary infringement contentions were prepared without the benefit of the Court's claim construction or the parties' exchange of constructions. As of the date of these contentions, AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court's constructions or to account for new information that becomes available.

	Limitation	Contention
1p	A system LSI having a plurality of ordinary operation modes and a plurality of special modes in response to clock frequencies supplied to a central processing unit, comprising:	To the extent that the preamble is limiting, Aquila contends that it is met. For example, each product in the 14h Accused Product Family ("Accused Product") is a system LSI. The Accused Product has a plurality of ordinary operation modes, for example the Core P-states. *See* BIOS and Kernel Developer's Guide for AMD Family 14h Models 00h-0Fh Processors ("BKDG"), §2.5.3.1:

	Limitation	Contention
		2.5.3.1 Core P-states Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states, specified in MSRC001_00[6B:64]. Out of reset, the voltage and frequency of the cores is specified by MSRC001_0071[StartupPstate]. Support for dynamic core P-state changes is indicated by more than one enabled selection in MSRC001_00[6B:64][PstateEn]. The DID and VID for each core P-state is specified in MSRC001_00[6B:64]. The COF for core P-states is a function of the main PLL frequency and the DID. See D18F3xD4[MainPllOpFreqId] for more details on the main PLL frequency and MSRC001_00[6B:64][CpuDidLSD] for more details on the DID. Software requests core P-state changes for each core independently using the hardware P-state control mechanism (also known as "fire and forget"). Support for hardware P-state control is indicated by CPUID Fn8000_0007_EDX[HwPstate]=1b. P-state transitions using the hardware P-state control mechanism are not allowed until the P-state initialization requirements defined in 2.5.3.1.7 [BIOS Requirements for Core P-State Initialization and Transitions] are complete. BKDG at p.55:

	Limitation	Contention
		Table 9: Software P-state numbering example

D18F4x15C[NumBoostStates]=1		D18F4x15C[NumBoostStates]=3	
P-state Name	**MSR Address**	**P-state Name**	**MSR Address**
Pb0	MSRC001_0064	Pb0	MSRC001_0064
P0	MSRC001_0065	Pb1	MSRC001_0065
P1	MSRC001_0066	Pb2	MSRC001_0066
P2	MSRC001_0067	P0	MSRC001_0067
P3	MSRC001_0068	P1	MSRC001_0068
P4	MSRC001_0069	P2	MSRC001_0069
P5	MSRC001_006A	P3	MSRC001_006A
P6	MSRC001_006B	P4	MSRC001_006B

All sections and register definitions use software P-state numbering unless otherwise specified.

The Accused Product Family has a plurality of special modes, for example, the Core C-states or deep sleep modes such as ACPI S3 or connected standby S0i3. *See* BKDG, §§ 2.5.3.2, 2.5.3.2.1, 2.5:

	Limitation	Contention
		2.5.3.2 C-states C-states are processor power states. C0 is the operational state in which instructions are executed. All other C-states are low-power states in which instructions are not executed. **2.5.3.2.1 C-state Names and Numbers** C-states are often referred to by an alphanumeric naming convention, C1, C2, C3, etc. The mapping between ACPI defined C-states and AMD specified C-state actions is not direct. The actions taken by the processor when entering a low-power C-state are specified by D18F4x118 and D18F4x11C and are configured by software. See 2.5.3.2.3 [C-state Actions] for information about AMD specific actions.

	Limitation	Contention

2.5 Power Management

The processor supports many power management features in a variety of systems. Table 8 provides a summary of ACPI states and power management features and indicates whether they are supported.

Table 8: Power management support

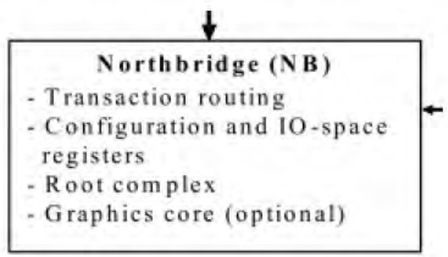
ACPI State/Power Management Feature	Supported	Description
G0/S0/C0: Working	Yes	
G0/S0/C0: Core P-state transitions	Yes	2.5.3.1 [Core P-states]
G0/S0/C0: NB P-state transitions	Yes	2.5.4.2 [NB Clock Ramping]
G0/S0/C0: Hardware thermal control (HTC)	Yes	2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)]
G0/S0/C0: Local Hardware thermal control (LHTC)	Revision Specific[1]	2.10.3.2 [Local Hardware Thermal Control (LHTC)]
G0/S0/C0: Software thermal control (STC)	No	
G0/S0/C0: Thermal clock throttling (SMC controlled)	No	
G0/S0: Low power C-states	Yes	2.5.3.2 [C-states] and 2.5.1.4.2 [Alternate Low Power Voltages]
G1/S1: Stand By (Powered On Suspend)	No	
G1/S3: Stand By (Suspend to RAM)	Yes	2.5.7.1.1 [ACPI Suspend to RAM State (S3)]
G1/S4, S5: Hibernate (Suspend to Disk), Shut Down (Soft Off)	Yes	
G3 Mechanical Off	Yes	
Parallel VID Interface	No	2.5.1 [Processor Power Planes And Voltage Control]
Serial VID Interface	Yes	
Dual-plane systems	Yes	

1. Support for this ACPI state or power management feature varies by processor revision. See 1.5.2 [Supported Feature Variations].

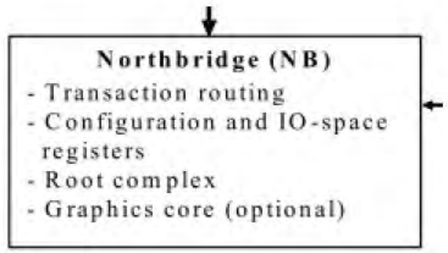
	Limitation	Contention
		Furthermore, the Core P-states and Core C-states are in response to clock frequencies supplied to a central processing unit. For example, the core P-states are "characterized" by "core frequency;" core P-state changes are further requested by software. *See e.g.,* BKDG, § 2.5.3.1, 2.5.3.1.3: **2.5.3.1 Core P-states** Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states, specified in MSRC001_00[6B:64]. Out of reset, the voltage and frequency of the cores is specified by MSRC001_0071[StartupPstate]. Support for dynamic core P-state changes is indicated by more than one enabled selection in MSRC001_00[6B:64][PstateEn]. The DID and VID for each core P-state is specified in MSRC001_00[6B:64]. The COF for core P-states is a function of the main PLL frequency and the DID. See D18F3xD4[MainPllOpFreqId] for more details on the main PLL frequency and MSRC001_00[6B:64][CpuDidLSD] for more details on the DID. Software requests core P-state changes for each core independently using the hardware P-state control mechanism (also known as "fire and forget"). Support for hardware P-state control is indicated by CPUID Fn8000_0007_EDX[HwPstate]=1b. P-state transitions using the hardware P-state control mechanism are not allowed until the P-state initialization requirements defined in 2.5.3.1.7 [BIOS Requirements for Core P-State Initialization and Transitions] are complete. Page #57

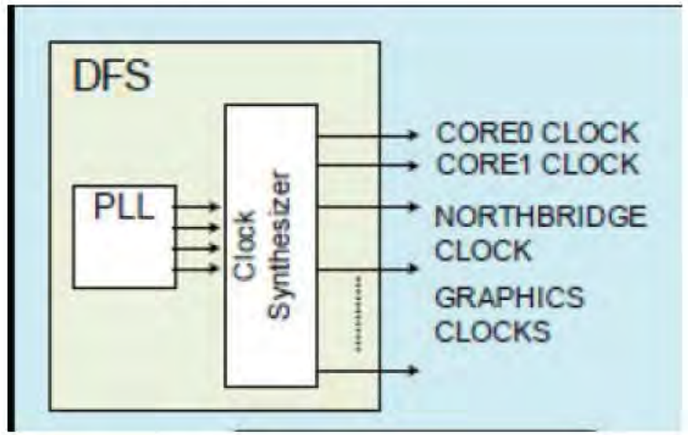
	Limitation	Contention
		2.5.3.1.3 Core P-state Control Core P-states are dynamically controlled by software and are exposed through ACPI objects (see 2.5.3.1.9 [ACPI Processor P-State Objects]). Software requests a core P-state change by writing a 3 bit index corresponding to the desired non-boosted P-state number to MSRC001_0062 [P-State Control] of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's MSRC001_0062[PstateCmd]. Boosted P-states may not be directly requested by software. Whenever software requests the P0 state (i.e. when software writes 000b to MSRC001_0062[PstateCmd]) on a processor that supports CPB, hardware dynamically places that core into the highest-performance P-state possible as determined by CPB. See 2.5.3.1.1 [Core Performance Boost (CPB)]. Hardware sequences the frequency and voltage changes necessary to complete a P-state transition as specified by 2.5.3.1.6 [Core P-state Transition Behavior] with no additional software interaction required. Hardware also coordinates frequency and voltage changes when differing P-state requests are made on cores that share a frequency or voltage plane. See 2.5.2 [Frequency and Voltage Domain Dependencies] for details about hardware coordination. Core P-states are changed without interacting with an external chipset. However, the chipset is notified of core P-state changes by the P-state special cycle if MSRC001_001F[EnaPStateSpCyc]=1. This message is sent regardless of whether the change is to or from a boosted P-state or a non-boosted P-state. Similarly, C-states are "dynamically requested by software" and also dependent upon clock frequency. *See* BKDG §§ 2.5.3.2.2, 2.5.3.2.3.1, 2.5.3.2.3.2; p.320-321:

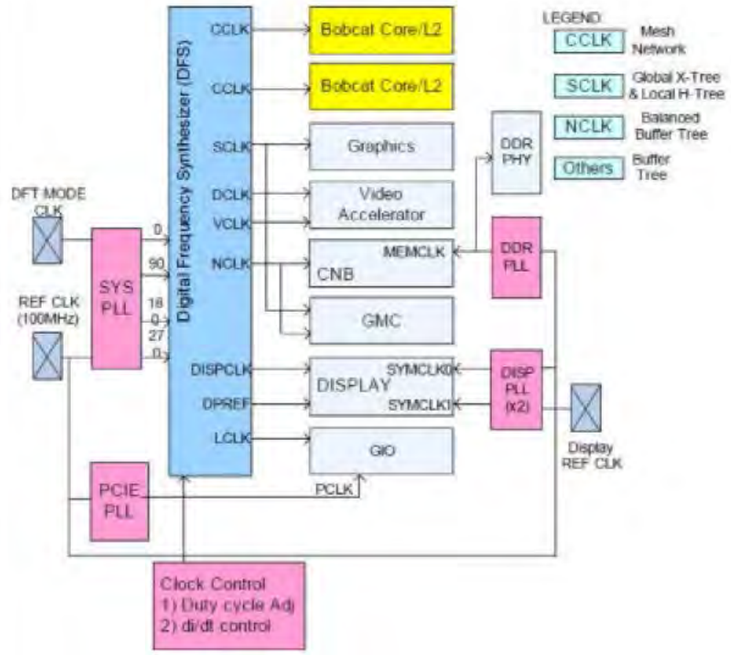
	Limitation	Contention
		2.5.3.2.3.1 Core C1 (CC1) State When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x1A8[Single-HaltCpuDid]. **2.5.3.2.3.2 Core C6 (CC6) State** When a core enters the CC6 state, it executes the following sequence: 1. L1 and L2 caches are flushed to DRAM by hardware. 2. Internal core state is saved to DRAM by hardware. 3. The core clock ramps down to the frequency specified by D18F4x1AC[C6Did]. 4. Power is removed from the core if possible as specified by D18F4x1AC[CoreC6Cap] and D18F4x1AC[CoreC6Dis]. The events which cause a core to exit the CC6 state are specified in 2.5.3.2.6 [Exiting C-states]. If a warm reset occurs while a core is in CC6, all MCA registers in the core shown in Table 41 are cleared to 0. See 2.16 [Machine Check Architecture]. **D18F4x1AC CPU State Power Management Dynamic Control 1**

	Limitation	Contention
		9:5 **C6Did: CC6 divisor**. Read-write. Reset: 0. BIOS: 1Fh. Specifies the divisor applied to the core when ramping clocks down for CC6. See 2.5.3.2.3 [C-state Actions] for details. Bits — Divisor 1Ch-00h — Reserved. 1Dh — 128 1Eh — 512 1Fh — Clocks off. See D18F4x1A8[SingleHaltCpuDid].
1a	a first memory that stores a clock control library for controlling a clock frequency transition between said ordinary operation modes;	The Accused Products include a first memory that stores a clock control library. For example, the SMU contains memory that stores the firmware and configuration space registers, including a clock control library. The clock control library controls clock frequency transition between the P-states. See e.g., BKDG, 30:  BKDG, section 2.12:

	Limitation	Contention
		2.12 System Management Unit (SMU) The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details. **2.12.1 Microcontroller** The SMU contains a microcontroller with a 16k ROM and a 16k RAM. See also BKDG, Table 10: **Table 10: P-state control example** D18F4x15C[NumBoostStates]=1 / D18F4x15C[NumBoostStates]=3 **P-state Name** | **Index Used for Requests/Status** | **Corresponding MSR Address** | **P-state Name** | **Index Used for Requests/Status** | **Corresponding MSR Address** Pb0 | n/a | MSRC001_0064 | Pb0 | n/a | MSRC001_0064 P0 | 0 | MSRC001_0065 | Pb1 | n/a | MSRC001_0065 P1 | 1 | MSRC001_0066 | Pb2 | n/a | MSRC001_0066 P2 | 2 | MSRC001_0067 | P0 | 0 | MSRC001_0067 P3 | 3 | MSRC001_0068 | P1 | 1 | MSRC001_0068 P4 | 4 | MSRC001_0069 | P2 | 2 | MSRC001_0069 P5 | 5 | MSRC001_006A | P3 | 3 | MSRC001_006A P6 | 6 | MSRC001_006B | P4 | 4 | MSRC001_006B
1b	a system control circuit which has a register, wherein said system control	The Accused Product has a system control circuit, for example, the System Management Unit and/or the System Management Controller, that has a register. See e.g., BKDG:

	Limitation	Contention
	circuit carries out the clock frequency transition between said ordinary operation modes and said special modes in response to a change of a value in said register, and also carries out the clock frequency transition among said ordinary operation modes in response to said clock control library;	 BKDG, section 2.12: **2.12 System Management Unit (SMU)** The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details. **2.12.1 Microcontroller** The SMU contains a microcontroller with a 16k ROM and a 16k RAM. The NB/SMU controls the clock frequency transitions between the core P-states. See e.g., SATHE et al.: RESONANT-CLOCK DESIGN FOR A POWER-EFFICIENT, HIGH-VOLUME X86-64 MICROPROCESSOR, p.144 tion of the configuration programming interface. On receiving notification from the NB of a PState transition, the core implements a PState entry sequence which transitions the core into a clock-gated state. A program sequencer then accesses a

	Limitation	Contention
1c	a clock generation circuit that receives a plurality of standard clocks, wherein said clock generation circuit generates a clock supplied to said central processing unit according to control by said system control circuit; and	The Accused Products include a digital frequency synthesizer clock generation circuit, including the core PLL, clock multipliers and dividers, and/or the digital frequency synthesizer. The DFS receives a plurality of standard clocks, for example, different phases of the PLL clock or reference clock, and outputs the core clock such as CCLK to the CPU. The clock generator circuit includes at least the PLL and the digital frequency synthesizer. The DFS receives a plurality of standard clocks (the 4 phases-offset references provided by the PLL), and generates CCLK according to control by the SMU: 

	Limitation	Contention
		 Source: Foley et al., A Low-Power Integrated x86-64 And Graphics Processor For Mobile Computing Devices, Fig. 1., 11; p.224-225.
1d	a second memory that stores an application program, wherein calling of said clock control library and	The Accused Products include a second memory, such as the hierarchy of L1, L2 caches that stores an application program, including but not limited to ACPI drivers, power management utilities, APIs provided by AMD, or any software that causes the SMU/SMC firmware to perform P-state transitions. See BKDG section 2.5.3.1.3; p. 429:

	Limitation	Contention
	changing of said register value are programmably controlled by said application program to enable user selectable clock frequency transitions,	**2.5.3.1.3 Core P-state Control** Core P-states are dynamically controlled by software and are exposed through ACPI objects (see 2.5.3.1.9 [ACPI Processor P-State Objects]). Software requests a core P-state change by writing a 3 bit index corresponding to the desired non-boosted P-state number to MSRC001_0062 [P-State Control] of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's MSRC001_0062[PstateCmd]. Boosted P-states may not be directly requested by software. Whenever software requests the P0 state (i.e. when software writes 000b to MSRC001_0062[PstateCmd]) on a processor that supports CPB, hardware dynamically places that core into the highest-performance P-state possible as determined by CPB. See 2.5.3.1.1 [Core Performance Boost (CPB)]. Hardware sequences the frequency and voltage changes necessary to complete a P-state transition as specified by 2.5.3.1.6 [Core P-state Transition Behavior] with no additional software interaction required. Hardware also coordinates frequency and voltage changes when differing P-state requests are made on cores that share a frequency or voltage plane. See 2.5.2 [Frequency and Voltage Domain Dependencies] for details about hardware coordination. **MSRC001_0062 P-State Control** Bits | Description 63:3 | MBZ. 2:0 | **PstateCmd: P-state change command**. Read-write. Reset: Product-specific. Writes to this field cause the core to change to the indicated non-boosted P-state number, specified by MSRC001_00[6B:64]. 0=SWP0, 1=SWP1, etc. P-state limits are applied to any P-state requests made through this register. See sections 2.5.3.1 [Core P-states] and 2.5.3.1.2.1 [Software P-state Numbering]. Reads from this field return the last written value, regardless of whether any limits are applied.

	Limitation	Contention
1e	wherein said special modes comprise a first special mode in which clock supply to principal constituents of said central processing unit is halted, a second special mode in which clock supply to an entirety of said central processing unit is halted, and a third special mode in which supply of power to the entirety of said central processing unit is halted.	The Accused Products include a first special mode in which clock supply to principal constituents of said central processing unit is halted, for example the core C1 (CC1) state: **2.5.3.2.3.1 Core C1 (CC1) State** When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x1A8[Single-HaltCpuDid]. **D18F4x1A8 CPU State Power Management Dynamic Control 0** Reset: 0000_0000h. 4:0 **SingleHaltCpuDid**. Read-write. BIOS: 1Eh. On a processor with multiple cores, this specifies the divisor used when ramping core clocks down after a single core has entered the clocks ramped state. Bits — Divisor 1Ch-00h — Reserved. 1Dh — 128 1Eh — 512 1Fh — Clocks off. • If MSRC001_00[6B:64][CpuDidMSD] of the current P-state is greater than or equal to Single-HaltCpuDid, then no frequency change is made when entering the low-power state associated with this register. • The COF = (the frequency specified by D18F3xD4[MainPllOpFreqId]) / (the divisor specified by this field). The Accused Products include a second special mode in which clock supply to an entirety of said central processing unit is halted, for example the package C1 (PC1) state:

	Limitation	Contention

2.5.3.2.3.3 Package C1 (PC1) State

The processor enters the PC1 state with auto-Pmin when all of the following are true:

- All cores are in the CC1 state or deeper.

If D18F4x1AC[CstPminEn] indicates that auto-Pmin is enabled when the processor enters PC1, the P-state for all cores is transitioned as specified by 2.5.3.2.7.1 [Auto-Pmin]. Regardless of the state of D18F4x1AC[CstPminEn], all core clocks are ramped to the frequency specified by D18F4x1A8[AllHaltCpuDid].

D18F4x1A8 CPU State Power Management Dynamic Control 0

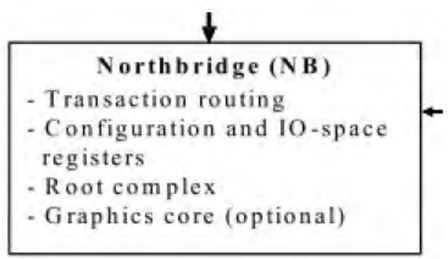
Reset: 0000_0000h.

9:5	**AllHaltCpuDid**. Read-write. BIOS: 1Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State]. Bits — Divisor 1Ch-00h — Reserved. 1Dh — 128 1Eh — 512 1Fh — Clocks off. See D18F4x1A8[SingleHaltCpuDid].

The Accused Products include a third special mode in which supply of power to the entirety of said central processing unit is halted, for example the package C6 (PC6) state:

	Limitation	Contention
		2.5.3.2.3.4 Package C6 (PC6) State The processor enters the PC6 state when all of the following are true: • All cores enter the CC6 state. • The C-state action field targeted by each core's C-state request has the C6Enable bit programmed to indicated entry into PC6 is allowed. See D18F4x118 and D18F4x11C. • PC6 is supported and enabled as specified by D18F4x1AC[PkgC6Cap] and D18F4x1AC[PkgC6Dis]. When the package enters PC6, VDDCR_CPU is transitioned to the VID specified by D18F3x128[C6Vid]. **2.5.1.4.2 Alternate Low Power Voltages** In order to save power, voltages lower than those normally used may be applied to the VDDCR_CPU power plane while the processor is in a C-state. D18F3x128[C6Vid] specifies a VDDCR_CPU voltage that does not retain the CPU caches or the cores' microarchitectural state, nor allows for execution. As a result, hardware flushes caches and saves the cores' microarchitectural state to DRAM before transitioning to C6Vid. See 2.5.3.2.3.4 [Package C6 (PC6) State]. **2.5.1.4.3 Power Gating** The processor can remove power from an individual core. This is referred to as power gating. Gating power to a subcomponent causes its internal microarchitectural state and, if applicable, any data in its caches to be lost. When entering a power gated state, hardware saves any needed data, either internally or to DRAM, and flushes caches. When exiting a power gated state, hardware performs any required resets and restores any needed data. See 2.5.3.2.3.2 [Core C6 (CC6) State].

	Limitation	Contention
2p	A system LSI as claimed in claim 1, wherein said clock control library comprises:	
2a	a plurality of libraries that control said system control circuit and said clock generation circuit to transition the clock frequencies supplied to said central processing unit; and	The clock control libraries of the Accused Products contain a plurality of libraries that control the SMU and clock generator to transition clock frequencies. For example, source code provided by AMD to coreboot indicates that P-state and C-state transitions are controlled by separate libraries: https://github.com/coreboot/coreboot/tree/master/src/vendorcode/amd/agesa/f14/Proc/CPU/Feature
2b	a main library which is called by said application program and selects any one of said libraries in correspondence with the clock frequency supplied to said central processing unit.	As discussed above, P-states and C-states may be controlled by software, which includes a main library that calls upon the plurality of libraries.
3p	A system LSI as claimed in claim 2,	
3a	wherein said main library is described using a same program language as said application program.	The main library in the SMU firmware and the application program instructions stored in the caches are both use the same language such as machine code.
5p	A system LSI as claimed in claim 2,	
5a	wherein each of said libraries is described using a program language capable of directly controlling said clock	The SMU firmware directly controls the SMU hardware.

	Limitation	Contention
	generation circuit and said system control circuit.	
6p	A system LSI as claimed in claim 5,	
6a	wherein each of said libraries is described using an assembler language.	The SMU firmware directly controls the SMU hardware and is described using an assembler language such as machine code.
7p	7. A system LSI as claimed in claim 1, wherein said system control circuit comprises:	
7a	a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit;	The NB of the Accused Products contains a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit. The NB contains the configuration register space for the Accused Products. See e.g., BKDG:  BKDG, section 2.12:

	Limitation	Contention
		2.12 System Management Unit (SMU) The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details. **2.12.1 Microcontroller** The SMU contains a microcontroller with a 16k ROM and a 16k RAM. Configuration space register mnemonics are defined in section 3.1 of the BKDG: • **DXFYxZZZ**: PCI-defined configuration space; X specifies the hexadecimal device number (this may be 1or 2 digits), Y specifies the function number, and ZZZ specifies the hexidecimal byte address (this may be 2 or 3 digits; e.g., D18F3x40 specifies the register at device 18h, function 3, and address 40h). See 2.7 [Configuration Space], for details about configuration space. the core C1 (CC1) state: **2.5.3.2.3.1 Core C1 (CC1) State** When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x1A8[SingleHaltCpuDid]. **D18F4x1A8 CPU State Power Management Dynamic Control 0** Reset: 0000_0000h.

	Limitation	Contention

4:0	**SingleHaltCpuDid**. Read-write. BIOS: 1Eh. On a processor with multiple cores, this specifies the divisor used when ramping core clocks down after a single core has entered the clocks ramped state. Bits — Divisor 1Ch-00h — Reserved. 1Dh — 128 1Eh — 512 1Fh — Clocks off. • If MSRC001_00[6B:64][CpuDidMSD] of the current P-state is greater than or equal to SingleHaltCpuDid, then no frequency change is made when entering the low-power state associated with this register. • The COF = (the frequency specified by D18F3xD4[MainPllOpFreqId]) / (the divisor specified by this field).

2.5.3.2.3.3 Package C1 (PC1) State

The processor enters the PC1 state with auto-Pmin when all of the following are true:

- All cores are in the CC1 state or deeper.

If D18F4x1AC[CstPminEn] indicates that auto-Pmin is enabled when the processor enters PC1, the P-state for all cores is transitioned as specified by 2.5.3.2.7.1 [Auto-Pmin]. Regardless of the state of D18F4x1AC[CstPminEn], all core clocks are ramped to the frequency specified by D18F4x1A8[AllHaltCpuDid].

D18F4x1A8 CPU State Power Management Dynamic Control 0

Reset: 0000_0000h.

	Limitation	Contention
		9:5 **AllHaltCpuDid**. Read-write. BIOS: 1Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State]. Bits — Divisor 1Ch-00h — Reserved. 1Dh — 128 1Eh — 512 1Fh — Clocks off. See D18F4x1A8[SingleHaltCpuDid].
7b	a clock halting register that receives the clock from said clock generation circuit and individually sets the clock to be halted or supplied;	the core C1 (CC1) state: **2.5.3.2.3.1 Core C1 (CC1) State** When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x1A8[SingleHaltCpuDid]. **D18F4x1A8 CPU State Power Management Dynamic Control 0** Reset: 0000_0000h.

	Limitation	Contention

4:0	**SingleHaltCpuDid**. Read-write. BIOS: 1Eh. On a processor with multiple cores, this specifies the divisor used when ramping core clocks down after a single core has entered the clocks ramped state. Bits — Divisor 1Ch-00h — Reserved. 1Dh — 128 1Eh — 512 1Fh — Clocks off. • If MSRC001_00[6B:64][CpuDidMSD] of the current P-state is greater than or equal to SingleHaltCpuDid, then no frequency change is made when entering the low-power state associated with this register. • The COF = (the frequency specified by D18F3xD4[MainPllOpFreqId]) / (the divisor specified by this field).

The Accused Products include a second special mode in which clock supply to an entirety of said central processing unit is halted, for example the package C1 (PC1) state:

2.5.3.2.3.3 Package C1 (PC1) State

The processor enters the PC1 state with auto-Pmin when all of the following are true:

- All cores are in the CC1 state or deeper.

If D18F4x1AC[CstPminEn] indicates that auto-Pmin is enabled when the processor enters PC1, the P-state for all cores is transitioned as specified by 2.5.3.2.7.1 [Auto-Pmin]. Regardless of the state of D18F4x1AC[CstPminEn], all core clocks are ramped to the frequency specified by D18F4x1A8[AllHaltCpuDid].

	Limitation	Contention
		D18F4x1A8 CPU State Power Management Dynamic Control 0 Reset: 0000_0000h. 9:5 **AllHaltCpuDid**. Read-write. BIOS: 1Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State]. Bits — Divisor 1Ch-00h — Reserved. 1Dh — 128 1Eh — 512 1Fh — Clocks off. See D18F4x1A8[SingleHaltCpuDid].

	Limitation	Contention
7c	And a status register that judges a state of said central processing unit immediately after being released from said third special mode.	**2.5.3.2.7.2 Exiting PC6** If the PService timer is enabled when the processor exits PC6, all cores transition to the P-state specified by D18F4x1AC[PstateIdCoreOffExit]. The cores remain in this state until one of the following occurs: • The PService timer expires while the package is in C0: In this case, the cores transition back to the last P-state requested by software. • The package enters PC1 without auto-Pmin: In this case, the PService timer continues counting. If it expires while in PC1, the cores remain in the P-state specified by D18F4x1AC[PstateIdCoreOffExit] until they return to C0, at which time they transition to the last P-state requested by software. • The package enters PC1 with auto-Pmin: In this case, the PService timer stops counting and the cores enter the PService state. • The package enters PC6: In this case the PService timer stops counting and the actions associated the requested package C-state occur. See 2.5.3.2.3.4 [Package C6 (PC6) State]. If the PService timer is disabled when the processor exits PC6, the cores transition back to the last P-state requested by software. See also BKDG pp.320-321: **D18F4x1AC CPU State Power Management Dynamic Control 1** 18:16 **PstateIdCoreOffExit**. Read-write. Reset: 0. BIOS: See 2.5.3.2.9. When exiting the package C6 state, the core transitions to the P-state specified by this register. See 2.5.3.2.7.2 [Exiting PC6]. If PC6 is enabled (see 2.5.3.2.9 [BIOS Requirements for C-state Initialization]), PstateIdCoreOffExit must be programmed to the lowest-performance P-state displayed to the operating system or to any lower-performance P-state. This P-state must have a core clock frequency of at least 400 MHz. Programming this field to 0 causes the core to transition to the last P-state requested by software when exiting package C6. This field uses hardware P-state numbering. See 2.5.3.1.2.2 [Hardware P-state Numbering].

	Limitation	Contention
10p	A system LSI as claimed in claim 1,	
10a	wherein said first memory and said second memory are two independent memories which are separated from each other.	As detailed above, the first memory in the SMU and the second memory in the caches are independent memories that are separated from each other.

Exhibit B.2: Preliminary Infringement Claim Charts for U.S. Patent 6,895,519

Accused Products: AMD 15h Products

These preliminary infringement contentions were prepared without the benefit of the Court's claim construction or the parties' exchange of constructions. As of the date of these contentions, AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court's constructions or to account for new information that becomes available.

	Limitation	Contention
1p	A system LSI having a plurality of ordinary operation modes and a plurality of special modes in response to clock frequencies supplied to a central processing unit, comprising:	To the extent that the preamble is limiting, Aquila contends that it is met. For example, the 15h Accused Product is a system LSI. The Accused Product has a plurality of ordinary operation modes, for example the Core P-states. *See* BIOS and Kernel Developer's Guide for AMD Family 15h Models 60h-6Fh Processors ("BKDG"), §2.5.2.1: **2.5.2.1 Core P-states** Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states (P0 through P7), specified in MSRC001_00[6B:64]. Out of cold reset, the voltage and frequency of the compute units is specified by MSRC001_0071[StartupPstate]. Support for dynamic core P-state changes is indicated by more than one enabled selection in MSRC001_00[6B:64][PstateEn]. Software requests core P-state changes for each core independently. Support for hardware P-state control is indicated by CPUID Fn8000_0007_EDX[HwPstate]=1b. Software may not request any P-state transitions until the P-state initialization requirements defined in 2.5.2.1.5 [BIOS Requirements for Core P-state Initialization and Transitions] are complete. The processor supports independently-controllable frequency planes for each compute unit and independently-controllable voltage plane for all compute units. See also BKDG at p.691:

	Limitation	Contention
		MSRC001_00[6B:64] P-state [7:0] Per-node. Cold reset: Varies by product. Each of these registers specify the frequency and voltage associated with each of the core P-states. Table 270: Register Mapping for MSRC001_00[6B:64] Register / Function MSRC001_0064 / P-state 0 MSRC001_0065 / P-state 1 MSRC001_0066 / P-state 2 MSRC001_0067 / P-state 3 MSRC001_0068 / P-state 4 MSRC001_0069 / P-state 5 MSRC001_006A / P-state 6 MSRC001_006B / P-state 7 The CpuVid field in these registers is required to be programmed to the same value in all cores of a processor, but are allowed to be different between processors in a multi-processor system. All other fields in these registers are required to be programmed to the same value in each core of the coherent fabric. See 2.5.2 [CPU Core Power Management]. BKDG at p.61:

	Limitation	Contention
		Table 10: Software P-state Naming

D18F4x15C[NumBoostStates]=1		D18F4x15C[NumBoostStates]=3	
P-state Name	**Corresponding Register Address**	**P-state Name**	**Corresponding Register Address**
Pb0	MSRC001_0064	Pb0	MSRC001_0064
P0 (base)	MSRC001_0065	Pb1	MSRC001_0065
P1	MSRC001_0066	Pb2	MSRC001_0066
P2	MSRC001_0067	P0 (base)	MSRC001_0067
P3	MSRC001_0068	P1	MSRC001_0068
P4	MSRC001_0069	P2	MSRC001_0069
P5	MSRC001_006A	P3	MSRC001_006A
P6	MSRC001_006B	P4	MSRC001_006B

All sections and register definitions use software P-state numbering unless otherwise specified.

The Carrizo has a plurality of special modes, for example, the Core C-states or deep sleep modes such as ACPI S3 or connected standby S0i3. *See* BKDG, §§ 2.5.2.2, 2.5.2.2.1, 2.5:

2.5.2.2 Core C-states

C-states are processor power states. C0 is the operational state in which instructions are executed. All other C-states are low-power states in which instructions are not executed. When coming out of warm and cold reset,

the cores are transitioned to the C0 state.

	Limitation	Contention

		2.5.2.2.1 C-state Names and Numbers
		
		C-states are often referred to by an alphanumeric naming convention, C1, C2, C3, etc. The mapping between ACPI defined C-states and AMD specified C-states is not direct. AMD specified C-states are referred to as IO-based C-states. Up to three IO-based C-states are supported, IO-based C-state 0, 1, and 2. The IO-based C-state index corresponds to the offset added to MSRC001_0073[CstateAddr] to initiate a C-state request. See 2.5.2.2.2 [C-state Request Interface]. The actions taken by the processor when entering a low-power C-state are configured by software. See 2.5.2.2.3 [C-state Actions] for information about AMD specific actions.
		
		2.5 Power Management
		
		The processor supports a wide variety of power management features, including:
		• OS-directed power management such as ACPI.
		• Clock frequency and voltage states (refered to as P-states and DPM states), including:
		  • CPU core P-states.
		  • Northbridge P-states.
		  • Memory P-states.
		  • Graphics DPM states.
		  • Multi-media block DPM states.
		• Power and thermal management for performance.
		  • Power optimization between blocks for optimal performance.
		  • Voltage transient tolerance.
		• Power efficiency for battery life, including:
		  • Power gating.
		  • Voltage optimization.
		  • Deep sleep modes (e.g., ACPI S3, or connected standby S0i3).
		  • Limiting frequency when it provides little value.
		• BIOS-configurable specifications.
		
		Furthermore, the Core P-states and Core C-states are in response to clock frequencies supplied to a central processing unit. For example, the core P-states are "characterized" by "core frequency;" core P-state changes are further requested by software. *See e.g.*, BKDG, § 2.5.2.1, 2.5.2.1.2:

	Limitation	Contention
		2.5.2.1 Core P-states Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states (P0 through P7), specified in MSRC001_00[6B:64]. Out of cold reset, the voltage and frequency of the compute units is specified by MSRC001_0071[StartupPstate]. Support for dynamic core P-state changes is indicated by more than one enabled selection in MSRC001_00[6B:64][PstateEn]. Software requests core P-state changes for each core independently. Support for hardware P-state control is indicated by CPUID Fn8000_0007_EDX[HwPstate]=1b. Software may not request any P-state transitions until the P-state initialization requirements defined in 2.5.2.1.5 [BIOS Requirements for Core P-state Initialization and Transitions] are complete. The processor supports independently-controllable frequency planes for each compute unit and independently-controllable voltage plane for all compute units. **2.5.2.1.2 Core P-state Control** Core P-states are dynamically controlled by software and are exposed through ACPI objects (refer to 2.5.2.1.7.3 [ACPI Processor P-state Objects]). Software requests a core P-state change by writing a 3 bit index corresponding to the desired P-state number to MSRC001_0062[PstateCmd] of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's MSRC001_0062[PstateCmd]. Similarly, C-states are "dynamically requested by software" and also dependent upon clock frequency. *See* BKDG §§ 2.5.2.2.2, 2.5.2.2.3, 3.14

	Limitation	Contention
		2.5.2.2.2 C-state Request Interface C-states are dynamically requested by software and are exposed through ACPI objects (see 2.5.2.2.6 [ACPI Processor C-state Objects]). C-states can be requested on a per-core basis. Software requests a C-state change in one of two ways: • Reading from an IO address: The IO address must be the address specified by MSRC001_0073[CstateAddr] plus an offset of 0 through 7. The processor always returns 0 for this IO read. Offsets 2 through 7 result in an offset of 2. • Executing the HLT instruction. This is equivalent to reading from the IO address specified by D18F4x128[HaltCstateIndex]. When software requests a C-state transition, hardware evaluates any frequency and voltage domain dependencies and determines which C-state actions to execute. See 2.5.2.2.3 [C-state Actions]. **2.5.2.2.3 C-state Actions** A core takes one of several different possible actions based upon a C-state change request from software. The C-state action fields are defined in D18F4x11[C:8]. **D18F4x11[C:8] C-state Control** D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.2.2 [Core C-states]. • D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]. • D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1. • D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2. **D18F4x118 C-state Control 1**

<table>
<tr><th></th><th>Limitation</th><th>Contention</th></tr>
<tr><td></td><td></td><td>
<table>
<tr><td>7:5</td><td>ClkDivisorCstAct0: clock divisor. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or:
• 100 MHz * (10h + MSRC001_00[6B:64][CpuFid[5:0]]) of the current P-state specified by MSRC001_0063[CurPstate].
If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.
<table>
<tr><th>Bits</th><th>Description</th><th>Bits</th><th>Description</th></tr>
<tr><td>000b</td><td>/1</td><td>100b</td><td>/16</td></tr>
<tr><td>001b</td><td>/2</td><td>101b</td><td>Reserved</td></tr>
<tr><td>010b</td><td>/4</td><td>110b</td><td>Reserved</td></tr>
<tr><td>011b</td><td>/8</td><td>111b</td><td>Turn off clocks.</td></tr>
</table>
See CacheFlushTmrSelCstAct0.</td></tr>
</table>
</td></tr>
<tr><td>1a</td><td>a first memory that stores a clock control library for controlling a clock frequency transition between said ordinary operation modes;</td><td>The Accused Products include a first memory that stores a clock control library. For example, the SMU contains memory that stores the firmware, including a clock control library. The clock control library controls clock frequency transition between the P-states. See e.g., BKDG, Table 270:</td></tr>
</table>

	Limitation	Contention
		MSRC001_00[6B:64] P-state [7:0] Per-node. Cold reset: Varies by product. Each of these registers specify the frequency and voltage associated with each of the core P-states. Table 270: Register Mapping for MSRC001_00[6B:64] Register / Function MSRC001_0064 / P-state 0 MSRC001_0065 / P-state 1 MSRC001_0066 / P-state 2 MSRC001_0067 / P-state 3 MSRC001_0068 / P-state 4 MSRC001_0069 / P-state 5 MSRC001_006A / P-state 6 MSRC001_006B / P-state 7 The CpuVid field in these registers is required to be programmed to the same value in all cores of a processor, but are allowed to be different between processors in a multi-processor system. All other fields in these registers are required to be programmed to the same value in each core of the coherent fabric. See 2.5.2 [CPU Core Power Management]. See also BKDG, Table 10:

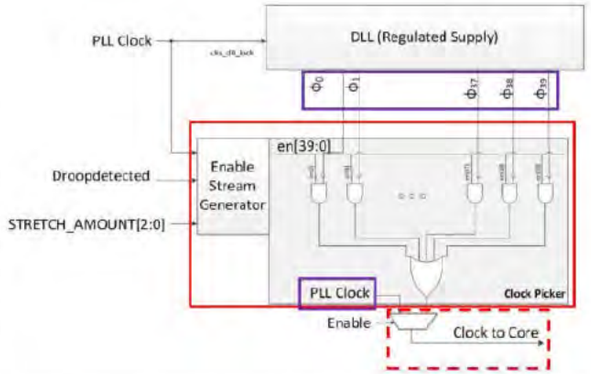
	Limitation	Contention
		Table 10: Software P-state Naming D18F4x15C[NumBoostStates]=1 / D18F4x15C[NumBoostStates]=3 **P-state Name** | **Corresponding Register Address** | **P-state Name** | **Corresponding Register Address** Pb0 | MSRC001_0064 | Pb0 | MSRC001_0064 P0 (base) | MSRC001_0065 | Pb1 | MSRC001_0065 P1 | MSRC001_0066 | Pb2 | MSRC001_0066 P2 | MSRC001_0067 | P0 (base) | MSRC001_0067 P3 | MSRC001_0068 | P1 | MSRC001_0068 P4 | MSRC001_0069 | P2 | MSRC001_0069 P5 | MSRC001_006A | P3 | MSRC001_006A P6 | MSRC001_006B | P4 | MSRC001_006B All sections and register definitions use software P-state numbering unless otherwise specified.
1b	a system control circuit which has a register, wherein said system control circuit carries out the clock frequency transition between said ordinary operation modes and said special modes in response to a change of a value in said register, and also carries out the clock frequency transition among said ordinary operation modes in response to said clock control library;	The Accused Product has a system control circuit, for example, the System Management Unit and/or the System Management Controller, that has a register. See e.g., BKDG: • Northbridge: • One communication packet routing block referred to as the northbridge (NB). The NB routes transactions between the cores, the link, and the DRAM interfaces. It includes the configuration register space for the device.

	Limitation	Contention
		2.13 System Management Unit (SMU) The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. The SMU uses two blocks, System Management Controller (SMC) and Platform Security Processor (PSP), in order to assist with many of these tasks. At the architectural level, PSP is known as MP0 and SMC is known as MP1. **2.13.1 System Management Controller (SMC)** The SMC is a standalone complex within AMD Family 15h Models 60h-6Fh processors that is responsible for maintaining the power management environment. Its functions include dynamic power management, state switching and fan control. The SMC contains a microcontroller to assist with many of these tasks. The SMU controls the clock frequency transitions between the core P-states. See e.g., SATHE et al.: RESONANT-CLOCK DESIGN FOR A POWER-EFFICIENT, HIGH-VOLUME X86-64 MICROPROCESSOR, p.144 tion of the configuration programming interface. On receiving notification from the NB of a PState transition, the core implements a PState entry sequence which transitions the core into a clock-gated state. A program sequencer then accesses a
1c	a clock generation circuit that receives a plurality of standard clocks, wherein said clock generation circuit generates a clock supplied to said central processing unit according to control by said system control circuit; and	The Accused Products include a digital frequency synthesizer clock generation circuit, including the core PLL, clock multipliers and dividers, and/or the digital frequency synthesizer. The DFS receives a plurality of standard clocks, for example, different phases of the PLL clock or reference clock, and outputs the core clock such as CCLK to the CPU. The clock generator circuit includes at least the PLL and the digital frequency synthesizer. The DFS receives a plurality of standard clocks (the 40 phases of the reference clocks), and generates CCLK according to control by the SMU:

	Limitation	Contention

D. Glitch Less Clock Phase Picker

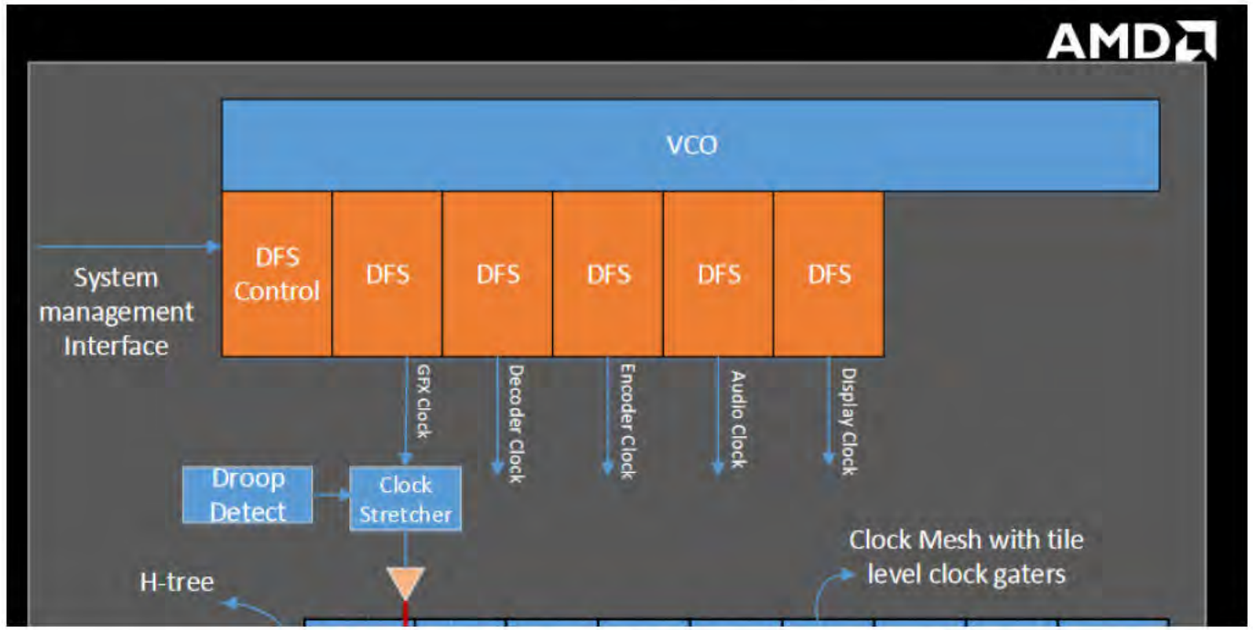
The glitch-less clock picker (Fig. 6) takes the 40 phases (40 total phases generated from the 20 DLL delay elements) and generates a stretched clock (configurable stretch amount) by selecting different phases of the clock. The clock picker always performs a complete loop through all the phases before selecting the 0^{th} phase (pll_clk) to avoid any contraction of the clock period. When the clock stretcher block is disabled (STRETCH_ENABLE = 0), the clock picker simply picks the pll_clk without any insertion delay of the clock stretcher logic.



Source: WILCOX et al.: STEAMROLLER MODULE AND ADAPTIVE CLOCKING SYSTEM IN 28 nm CMOS, Fig. 6

The digital frequency synthesizer receives multiple phases of the PLL clock (see above), and generates multiple discrete frequencies according to control by the SMU.

- Digital frequency synthesizer (DFS) that generates multiple discrete frequencies from a single VCO
  - Root clock gating
  - Disabling VCO and bypassing with low speed fixed clocks

	Limitation	Contention
		 Source: Krishnan et al., "Energy Efficient Graphics and Multimedia in 28nm Carrizo APU," p.14

	Limitation	Contention
		 *Source: Integrated Power Conversion Strategies Across Laptop, Server, and Graphics Products, 2016 Power SOC Conference, p.4.*
1d	a second memory that stores an application program, wherein calling of said clock control library and changing of said register value are programmably controlled by said application program to enable user selectable clock frequency transitions,	The Accused Products include a second memory, such as the hierarchy of L1, L2 and/or L3 caches that stores an application program, including but not limited to ACPI drivers, power management utilities, APIs provided by AMD, or any software that causes the SMU/SMC firmware to perform P-state transitions.

	Limitation	Contention
		Core P-states are dynamically controlled by software and are exposed through ACPI objects (refer to 2.5.2.1.7.3 [ACPI Processor P-state Objects]). Software requests a core P-state change by writing a 3 bit index corresponding to the desired P-state number to MSRC001_0062[PstateCmd] of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's MSRC001_0062[PstateCmd]. **MSRC001_0062 P-state Control** Bits: 63:3 — MBZ. Bits: 2:0 — **PstateCmd: P-state change command**. Read-write; Not-same-for-all. Cold reset value varies by product; after a warm reset, value initializes to the P-state the core was in prior to the reset. Writes to this field cause the core to change to the indicated non-boosted P-state number, specified by MSRC001_00[6B:64]. 0=P0, 1=P1, etc. P-state limits are applied to any P-state requests made through this register. Reads from this field return the last written value, regardless of whether any limits are applied. This field uses software P-state numbering. See 2.5.2 [CPU Core Power Management] and 2.5.2.1.1.1 [Software P-state Numbering].
1e	wherein said special modes comprise a first special mode in which clock supply to principal constituents of said central processing unit is halted, a second special mode in which clock supply to an entirety of said central processing unit is halted, and a third special mode in which supply of power to the entirety of said central processing unit is halted.	The Accused Products include a first special mode in which clock supply to principal constituents of said central processing unit is halted, for example the core C1 (CC1) state:

	Limitation	Contention

2.5.2.2.3.2 Core C1 (CC1) State

When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct].

D18F4x11[C:8] C-state Control

D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.2.2 [Core C-states].

- D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr].
- D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1.
- D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2.

D18F4x118 C-state Control 1

Bits	Description
31:30	Reserved.
29	**SelfRefrEarly1**: Read-write. Reset: 0. See: SelfRefrEarly0. BIOS: 0. IF (D18F4x128[CoreCstateMode] == 0) THEN 0.

13	**SelfRefrEarly0: allow early self-refresh**. Read-write. Reset: 0. BIOS: 0. 1=Allow self-refresh while cores in PC1 or CC1 are waiting for the cache flush timer to expire. 0=Wait for cache flush timer to expire before allowing self-refresh. See 2.5.6.2 [DRAM Self-Refresh] and 2.5.2.2.3.1 [C-state Probes and Cache Flushing]. IF (D18F4x128[CoreCstateMode] == 0) THEN 0. ENDIF.
7:5	**ClkDivisorCstAct0: clock divisor**. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or: • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid[5:0]]) of the current P-state specified by MSRC001_0063[CurPstate]. If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register. Bits / Description: 000b /1; 001b /2; 010b /4; 011b /8; 100b /16; 101b Reserved; 110b Reserved; 111b Turn off clocks. See CacheFlushTmrSelCstAct0.
4	Reserved.

The Accused Products include a second special mode in which clock supply to an entirety of said central processing unit is halted, for example the package C1 (PC1) state:

2.5.2.2.3 C-state Actions

A core takes one of several different possible actions based upon a C-state change req
C-state action fields are defined in D18F4x11[C:8].

D18F4x11[C:8] C-state Control

D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.2.2 [Core C-states].

- D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr].
- D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1.
- D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2.

D18F4x118 C-state Control 1

Bits	Description
31:30	Reserved.
29	**SelfRefrEarly1**: Read-write. Reset: 0. See: SelfRefrEarly0. BIOS: 0. IF (D18F4x128[CoreCstate-Mode] == 0) THEN 0.

13	**SelfRefrEarly0: allow early self-refresh**. Read-write. Reset: 0. BIOS: 0. 1=Allow self-refresh while cores in PC1 or CC1 are waiting for the cache flush timer to expire. 0=Wait for cache flush timer to expire before allowing self-refresh. See 2.5.6.2 [DRAM Self-Refresh] and 2.5.2.2.3.1 [C-state Probes and Cache Flushing]. IF (D18F4x128[CoreCstateMode] == 0) THEN 0. ENDIF.
7:5	**ClkDivisorCstAct0: clock divisor**. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or: • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid[5:0]]) of the current P-state specified by MSRC001_0063[CurPstate]. If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register. Bits / Description: 000b /1; 001b /2; 010b /4; 011b /8; 100b /16; 101b Reserved; 110b Reserved; 111b Turn off clocks. See CacheFlushTmrSelCstAct0.
4	Reserved.

	Limitation	Contention
		The Accused Products include a third special mode in which supply of power to the entirety of said central processing unit is halted, for example the package C6 (PC6) state: **2.5.2.2.3.4 Package C6 (PC6) State** When all cores enter a non-C0 state, VDD can be reduced to a non-operational voltage that does not retain core state. This state is known as PC6 and reduces the amount of static and dynamic power consumed by all cores. The following actions are taken by hardware prior to PC6 entry: 1. If MSRC001_0071[CurPstate] < D18F3xA8[PopDownPstate], transition the core P-state to D18F3xA8[PopDownPstate]. 2. For all cores not in CC6, L1 and L2 caches are flushed to DRAM. See 2.5.2.2.3.1 [C-state Probes and Cache Flushing]. 3. For all cores not in CC6, internal core state is saved to DRAM. 4. VDD is transitioned to the VID specified by D18F5x128[PC6Vid]. All of the following must be true on all cores in order for a package to be placed into PC6: • D18F4x118/D18F4x11C[CacheFlushEn] == 1 for the corresponding C-state action field. • D18F4x118/D18F4x11C[CacheFlushTmrSel] != 11b for the corresponding C-state action field. • D18F4x118/D18F4x11C[PwrOffEnCstAct] == 1 for the corresponding C-state action field. • D18F2x118[CC6SaveEn] == 1. • D18F2x118[LockDramCfg] == 1. • MSRC001_0015[HltXSpCycEn] == 1.
2p	A system LSI as claimed in claim 1, wherein said clock control library comprises:	

	Limitation	Contention
2a	a plurality of libraries that control said system control circuit and said clock generation circuit to transition the clock frequencies supplied to said central processing unit; and	The clock control libraries of the Accused Products contain a plurality of libraries that control the SMU and clock generator to transition clock frequencies. For example, source code provided by AMD to coreboot indicates that P-state and C-state transitions are controlled by separate libraries: https://chromium.googlesource.com/chromiumos/third_party/coreboot/+/firmware-winky-5216.1.B/src/vendorcode/amd/agesa/f15/Proc/CPU/Family/0x15/OR/
2b	a main library which is called by said application program and selects any one of said libraries in correspondence with the clock frequency supplied to said central processing unit.	As discussed above, P-states and C-states may be controlled by software, which includes a main library that calls upon the plurality of libraries.
3p	A system LSI as claimed in claim 2,	
3a	wherein said main library is described using a same program language as said application program.	The main library in the SMU firmware and the application program instructions stored in the caches are both use the same language such as machine code.
5p	A system LSI as claimed in claim 2,	
5a	wherein each of said libraries is described using a program language capable of directly controlling said clock generation circuit and said system control circuit.	The SMU firmware directly controls the SMU hardware.

	Limitation	Contention
6p	A system LSI as claimed in claim 5,	
6a	wherein each of said libraries is described using an assembler language.	The SMU firmware directly controls the SMU hardware and is described using an assembler language such as machine code.
7p	7. A system LSI as claimed in claim 1, wherein said system control circuit comprises:	
7a	a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit;	The NB of the Accused Products contains a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit. The NB contains the configuration register space for the Accused Products. *See* BKDG section 2.1: • Northbridge: • One communication packet routing block referred to as the northbridge (NB). The NB routes transactions between the cores, the link, and the DRAM interfaces. It includes the configuration register space for the device. Configuration space register mnemonics are defined in section 3.1 of the BKDG: • **DXFYxZZZ**: PCI-defined configuration space; X specifies the hexadecimal device number (this may be 1or 2 digits), Y specifies the function number, and ZZZ specifies the hexidecimal byte address (this may be 2 or 3 digits; e.g., D18F3x40 specifies the register at device 18h, function 3, and address 40h). See 2.7 [Configuration Space], for details about configuration space.

	Limitation	Contention
		2.5.2.2.3.2 Core C1 (CC1) State When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct]. **D18F4x11[C:8] C-state Control** D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAT) associated with an IO address that is read to enter C-states. Refer to 2.5.2.2 [Core C-states]. • D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]. • D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1. • D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2. **D18F4x118 C-state Control 1** Bits: Description 31:30: Reserved. 29: **SelfRefrEarly1**. Read-write. Reset: 0. See: SelfRefrEarly0. BIOS: 0. IF (D18F4x128[CoreCstateMode] == 0) THEN 0. 13: **SelfRefrEarly0: allow early self-refresh**. Read-write. Reset: 0. BIOS: 0. 1=Allow self-refresh while cores in PC1 or CC1 are waiting for the cache flush timer to expire. 0=Wait for cache flush timer to expire before allowing self-refresh. See 2.5.6.2 [DRAM Self-Refresh] and 2.5.2.2.3.1 [C-state Probes and Cache Flushing]. IF (D18F4x128[CoreCstateMode] == 0) THEN 0. ENDIF. 7:5: **ClkDivisorCstAct0: clock divisor**. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or: • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid[5:0]]) of the current P-state specified by MSRC001_0063[CurPstate]. If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register. Bits: Description 000b: /1 001b: /2 010b: /4 011b: /8 100b: /16 101b: Reserved 110b: Reserved 111b: Turn off clocks. See CacheFlushTmrSelCstAct0. 4: Reserved.
7b	a clock halting register that receives the clock from said clock generation circuit and individually sets the clock to be halted or supplied;	2.5.2.2.3.2 Core C1 (CC1) State When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct]. **D18F4x11[C:8] C-state Control** D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAT) associated with an IO address that is read to enter C-states. Refer to 2.5.2.2 [Core C-states]. • D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]. • D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1. • D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2. **D18F4x118 C-state Control 1** Bits: Description 31:30: Reserved. 29: **SelfRefrEarly1**. Read-write. Reset: 0. See: SelfRefrEarly0. BIOS: 0. IF (D18F4x128[CoreCstateMode] == 0) THEN 0. 13: **SelfRefrEarly0: allow early self-refresh**. Read-write. Reset: 0. BIOS: 0. 1=Allow self-refresh while cores in PC1 or CC1 are waiting for the cache flush timer to expire. 0=Wait for cache flush timer to expire before allowing self-refresh. See 2.5.6.2 [DRAM Self-Refresh] and 2.5.2.2.3.1 [C-state Probes and Cache Flushing]. IF (D18F4x128[CoreCstateMode] == 0) THEN 0. ENDIF. 7:5: **ClkDivisorCstAct0: clock divisor**. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or: • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid[5:0]]) of the current P-state specified by MSRC001_0063[CurPstate]. If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register. Bits: Description 000b: /1 001b: /2 010b: /4 011b: /8 100b: /16 101b: Reserved 110b: Reserved 111b: Turn off clocks. See CacheFlushTmrSelCstAct0. 4: Reserved.

	Limitation	Contention
7c	And a status register that judges a state of said central processing unit immediately after being released from said third special mode.	**D18F3xC8 COFVID Status Low** See 2.5.2 [CPU Core Power Management]. Bits | Description 31:24 | **CurNbVid[7:0]: current NB VID**. Read-only; Updated-by-hardware. Cold reset: Product-specific. This field specifies the current VDDNB voltage. 23 | **NbPstateDis: NB P-states disabled**. Value: D18F5x174[NbPstateDis]. MSRC001_0071[NbPstateDis] is an alias of D18F5x174[NbPstateDis]. 0=NB P-state frequency and voltage changes are supported. See D18F5x170[SwNbPstateLoDis, NbPstateDisOnP0]. 1=NB P-state frequency and voltage changes are disabled. 22:21 | Reserved. 20 | **CurCpuVid[7]**. Read-only; Updated-by-hardware; Not-same-for-all. Cold reset: Product-specific. See CurCpuVid[6:0]. 19 | Reserved. 18:16 | **CurPstate: current P-state**. Read-only; Updated-by-hardware; Not-same-for-all. Cold reset: Product-specific. Specifies the current P-state requested by the core. This field uses hardware P-state numbering. See MSRC001_0063[CurPstate] and 2.5.2.1.1.2 [Hardware P-state Numbering]. When a P-state change is requested, the value in this field is updated once all required frequency and voltage transitions are completed. 15:9 | **CurCpuVid[6:0]: current core VID**. Read-only; Updated-by-hardware; Not-same-for-all. Cold reset: Product-specific. CurCpuVid = {CurCpuVid[7], CurCpuVid[6:0]}. This field specifies the current VDD voltage. 8:6 | **CurCpuDid: current core divisor ID**. Read-only; Updated-by-hardware. Cold reset: Product-specific. Specifies the current CpuDid of the core. See MSRC001_00[6B:64]. When a P-state change is requested, the value in this field is updated once all required frequency and voltage transitions are completed. 5:0 | **CurCpuFid: current core frequency ID**. Read-only; Updated-by-hardware. Cold reset: Product-specific. Specifies the current CpuFid of the core. See MSRC001_00[6B:64]. When a P-state change is requested, the value in this field is updated once all required frequency and voltage transitions are completed.

	Limitation	Contention
10p	A system LSI as claimed in claim 1,	
10a	wherein said first memory and said second memory are two independent memories which are separated from each other.	As detailed above, the first memory in the SMU and the second memory in the caches are independent memories that are separated from each other.

Exhibit B.3: Preliminary Infringement Claim Charts for U.S. Patent 6,895,519

Accused Products: AMD Family 16h Products

These preliminary infringement contentions were prepared without the benefit of the Court's claim construction or the parties' exchange of constructions. As of the date of these contentions, AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court's constructions or to account for new information that becomes available.

	Limitation	Contention
1p	A system LSI having a plurality of ordinary operation modes and a plurality of special modes in response to clock frequencies supplied to a central processing unit, comprising:	To the extent that the preamble is limiting, Aquila contends that it is met. For example, each product in the 16h Accused Product Family ("Accused Product") is a system LSI. The Accused Product has a plurality of ordinary operation modes, for example the Core P-states. *See* BIOS and Kernel Developer's Guide for AMD Family 16h Models 00h-0Fh Processors ("BKDG"), §2.5.3.1: **2.5.3.1 Core P-states** Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states (P0 through P7), specified in MSRC001_00[6B:64]. Out of cold reset, the voltage and frequency of the compute units is specified by MSRC001_0071[StartupPstate]. BKDG, Table 9:

	Limitation	Contention

Table 9: Software P-state Naming

D18F4x15C[NumBoost-States]=1		D18F4x15C[NumBoost-States]=3	
P-state Name	**Corresponding MSR Address**	**P-state Name**	**Corresponding MSR Address**
Pb0	MSRC001_0064	Pb0	MSRC001_0064
P0	MSRC001_0065	Pb1	MSRC001_0065
P1	MSRC001_0066	Pb2	MSRC001_0066
P2	MSRC001_0067	P0	MSRC001_0067
P3	MSRC001_0068	P1	MSRC001_0068
P4	MSRC001_0069	P2	MSRC001_0069
P5	MSRC001_006A	P3	MSRC001_006A
P6	MSRC001_006B	P4	MSRC001_006B

All sections and register definitions use software P-state numbering unless otherwise specified.

The Accused Product Family has a plurality of special modes, for example, the Core C-states or deep sleep modes such as ACPI S3 or connected standby S0i3. *See* BKDG, §§ 2.5.3.2, 2.5.3.2.1, 2.5:

	Limitation	Contention
		2.5.3.2 Core C-states C-states are processor power states. C0 is the operational state in which instructions are executed. All other C-states are low-power states in which instructions are not executed. When coming out of warm and cold reset, the processor is transitioned to the C0 state. **2.5.3.2.1 C-state Names and Numbers** C-states are often referred to by an alphanumeric naming convention, C1, C2, C3, etc. The mapping between ACPI defined C-states and AMD specified C-states is not direct. AMD specified C-states are referred to as IO-based C-states. Up to three IO-based C-states are supported, IO-based C-state 0, 1, and 2. The IO-based C-state index corresponds to the offset added to MSRC001_0073[CstateAddr] to initiate a C-state request. See 2.5.3.2.2 [C-state Request Interface]. The actions taken by the processor when entering a low-power C-state are configured by software. See 2.5.3.2.3 [C-state Actions] for information about AMD specific actions.

Limitation	Contention
	2.5 Power Management The processor supports many power management features in a variety of systems. Table 8 provides a summary of ACPI states and power management features and indicates whether they are supported. **Table 8: Power Management Support**

ACPI/Power Management State	Supported	Description
G0/S0/C0: Working	Yes	
G0/S0/C0: Core P-state transitions	Yes	2.5.3.1 [Core P-states]
G0/S0/C0: NB P-state transitions	Yes	2.5.4.1 [NB P-states]
G0/S0/C0: Hardware thermal control (HTC)	Yes	2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)]
G0/S0/Per-core IO-based C-states	Yes	2.5.3.2 [Core C-states] and 2.5.1.3.2 [Low Power Voltages]
G0/S0/C1: Halt	Yes	
G0/S0/CC6: Per-core Power gating	Yes	2.5.3.2 [Core C-states]
G0/S0: CPC-L2 power gating	Yes	2.5.3.2 [Core C-states]
G0/S0/PC6: 0V support (VDD power plane).	Yes	2.5.3.2 [Core C-states] and 2.5.1.3.2 [Low Power Voltages]
G0/S0/Cx: Cache flushing support	Yes	2.5.3.2.3.1 [C-state Probes and Cache Flushing]
G0/S0: Northbridge C-states (DRAM self-refresh, NB clock-gating)	Yes	2.5.4.2 [NB C-states]
G1/S1: Stand By (Powered On Suspend)	No	
G1/S3: Stand By (Suspend to RAM)	Yes	2.5.8.1 [S-states]
G1/S4: Hibernate (Suspend to Disk)	Yes	
G1/S5: Shut Down (Soft Off)	Yes	
G3 Mechanical Off	Yes	
Parallel VID Interface	No	2.5.1 [Processor Power Planes And Voltage Control]
Serial VID Interface 1	No	
Serial VID Interface 2	Yes	
Single-plane systems	No	
Number of voltage planes	2	2.5.1 [Processor Power Planes And Voltage Control]
APM: Application Power Management	Yes	2.5.9 [Application Power Management (APM)]

	Limitation	Contention
		Furthermore, the Core P-states and Core C-states are in response to clock frequencies supplied to a central processing unit. For example, the core P-states are "characterized" by "core frequency;" core P-state changes are further requested by software. *See e.g.,* BKDG, § 2.5.3.1, 2.5.3.1.2: **2.5.3.1 Core P-states** Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states (P0 through P7), specified in MSRC001_00[6B:64]. Out of cold reset, the voltage and frequency of the compute units is specified by MSRC001_0071[StartupPstate].

	Limitation	Contention
		Support for dynamic core P-state changes is indicated by more than one enabled selection in MSRC001_00[6B:64][PstateEn]. At least one enabled P-state (P0) is specified for all processors. Software requests core P-state changes for each core independently using the hardware P-state control mechanism (a.k.a. fire and forget). Support for hardware P-state control is indicated by CPUID Fn8000_0007_EDX[HwPstate]=1b. Software may not request any P-state transitions using the hardware P-state control mechanism until the P-state initialization requirements defined in 2.5.3.1.6 [BIOS Requirements for Core P-state Initialization and Transitions] are complete. The processor supports independently-controllable frequency planes for each compute unit and the NB; and independently-controllable voltage planes. See 2.5.1 [Processor Power Planes And Voltage Control] for voltage plane definitions. The following terms may be applied to each of these planes: • FID: frequency ID. Specifies the PLL frequency multiplier, relative to the reference clock, for a given domain. • DID: divisor ID. Specifies the post-PLL power-of-two divisor that can be used to reduce the operating frequency. • COF: current operating frequency. Specifies the operating frequency as a function of the FID and DID. Refer to CoreCOF for the CPU COF formula and NBCOF for the NB COF formula. • VID: voltage ID. Specifies the voltage level for a given domain. Refer to 2.5.1.2.1 [MinVid and MaxVid Check] for encodings. All FID and DID parameters for software P-states must be programmed to equivalent values for all cores and NBs in the coherent fabric. See 2.5.3.1.1.1 [Software P-state Numbering]. Refer to MSRC001_00[6B:64] and D18F5x16[C:0] for further details on programming requirements.

	Limitation	Contention
		2.5.3.1.2 Core P-state Control Core P-states are dynamically controlled by software and are exposed through ACPI objects (refer to 2.5.3.1.8.3 [ACPI Processor P-state Objects]). Software requests a core P-state change by writing a 3 bit index corresponding to the desired P-state number to MSRC001_0062[PstateCmd] of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's MSRC001_0062[PstateCmd]. Boosted P-states may not be directly requested by software. Whenever software requests the P0 state on a processor that supports APM (i.e. writes 000b to MSRC001_0062[PstateCmd]), hardware dynamically places the core into the highest-performance P-state possible as determined by APM. See 2.5.9 [Application Power Management (APM)]. Hardware sequences the frequency and voltage changes necessary to complete a P-state transition as specified by 2.5.3.1.5 [Core P-state Transition Behavior] with no additional software interaction required. Hardware also coordinates frequency and voltage changes when differing P-state requests are made on cores that share a frequency or voltage plane. See 2.5.2 [Frequency and Voltage Domain Dependencies] for details about hardware coordination. Similarly, C-states are "dynamically requested by software" and also dependent upon clock frequency. *See* BKDG §§ 2.5.3.2.3.2, 2.5.3.2.3.3, 2.5.3.2.3.2; p.320-321:

	Limitation	Contention
		2.5.3.2.3.2 Core C1 (CC1) State When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct]. **2.5.3.2.3.3 Core C6 (CC6) State** A core can gate off power to its internal logic when it enters any non-C0 state. This power gated state is known as CC6. In order to enter CC6, hardware first enters CC1 then checks D18F4x118/D18F4x11C[PwrGateEnCstAct]. Power gating reduces the amount of power consumed by the core. VDD voltage is not reduced when a core is in CC6. The following sequence occurs when a core enters the CC6 state: 1. If MSRC001_0071[CurPstate] < D18F3xA8[PopDownPstate], transition the core P-state to D18F3xA8[PopDownPstate]. 2. Internal core state is saved to L1 cache . 3. L1 cache is flushed to L2 cache. See 2.5.3.2.3.1 [C-state Probes and Cache Flushing]. 4. Power is removed from the core and the core PLL/voltage regulator is powered down as specified by D18F5x128[CC6PwrDwnRegEn].

	Limitation	Contention

D18F4x11[C:8] C-state Control

D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states].

- D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr].
- D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1.
- D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2.

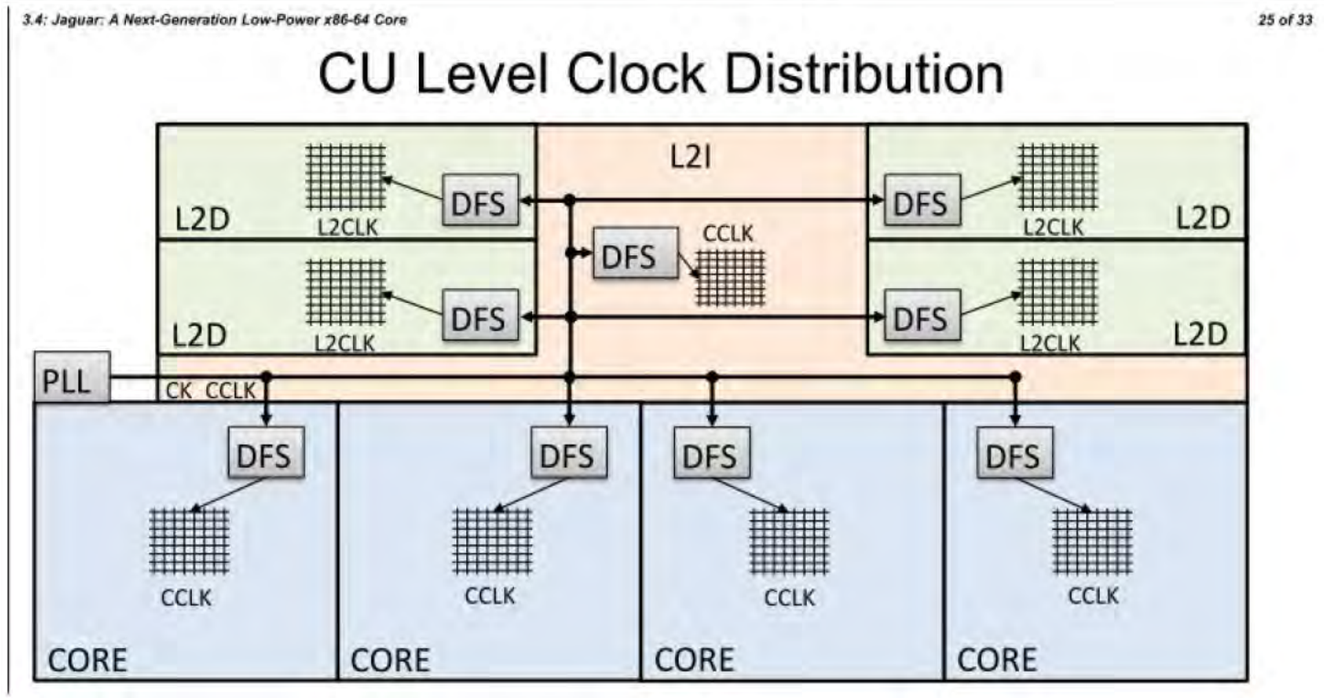
D18F4x118 C-state Control 1

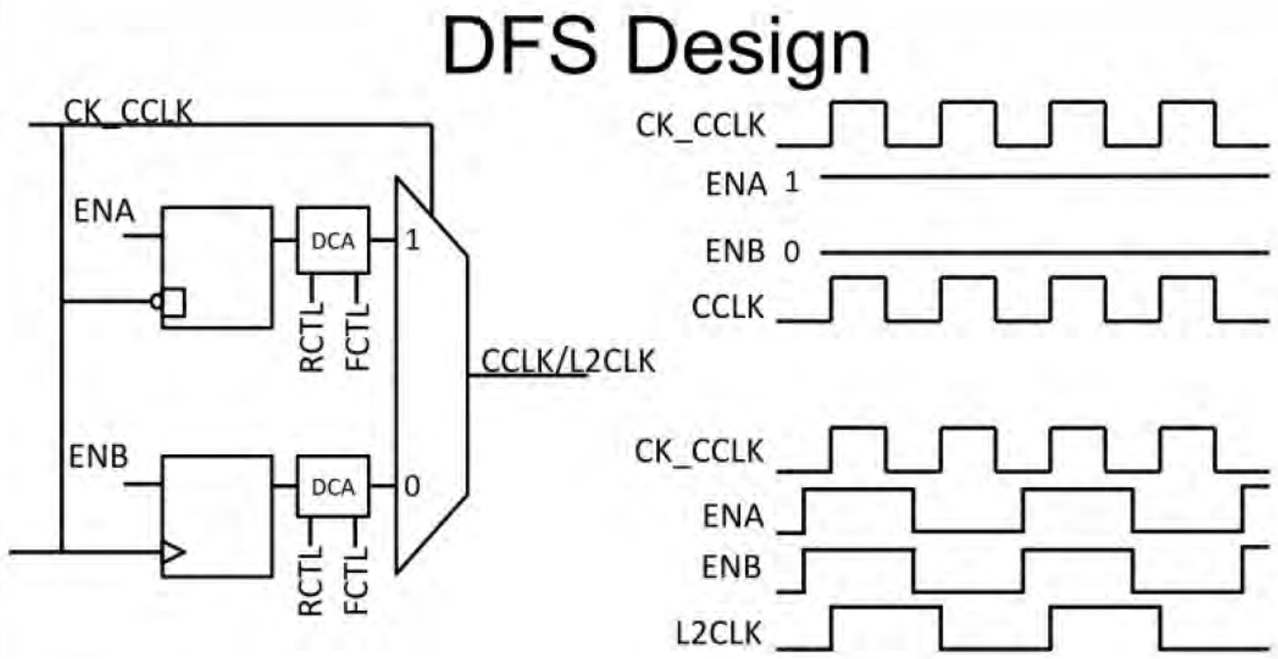
7:5	**ClkDivisorCstAct0: clock divisor**. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or: • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register. Bits Description Bits Description 000b /1 100b /16 001b /2 101b /128 010b /4 110b /512 011b /8 111b Turn off clocks. See CacheFlushTmrSelCstAct0.

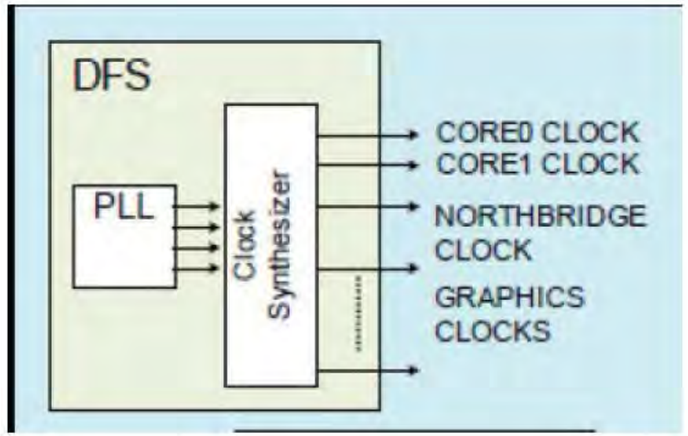
	Limitation	Contention
1a	a first memory that stores a clock control library for controlling a clock frequency transition between said ordinary operation modes;	The Accused Products include a first memory that stores a clock control library. For example, the SMU contains memory that stores the firmware and configuration space registers, including a clock control library. The clock control library controls clock frequency transition between the P-states. See e.g., BKDG, 29: • Northbridge: • One communication packet routing block referred to as the northbridge (NB). The NB routes transactions between the cores, the link, and the DRAM interfaces. It includes the configuration register space for the device. BKDG, section 2.12: **2.12 System Management Unit (SMU)** The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. The SMU contains a microcontroller to assist with many of these tasks. See also BKDG, Table 10:

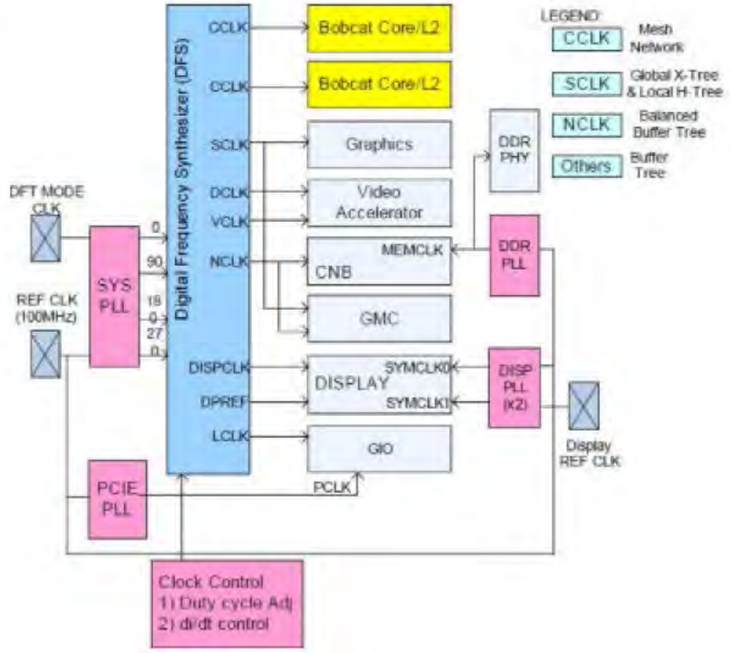
	Limitation	Contention
		Table 10: Software P-state Control D18F4x15C[NumBoostStates]=1 / D18F4x15C[NumBoostStates]=3 P-state Name | Index Used for Requests/Status | Corresponding MSR Address | P-state Name | Index Used for Requests/Status | Corresponding MSR Address Pb0 | n/a | MSRC001_0064 | Pb0 | n/a | MSRC001_0064 P0 | 0 | MSRC001_0065 | Pb1 | n/a | MSRC001_0065 P1 | 1 | MSRC001_0066 | Pb2 | n/a | MSRC001_0066 P2 | 2 | MSRC001_0067 | P0 | 0 | MSRC001_0067 P3 | 3 | MSRC001_0068 | P1 | 1 | MSRC001_0068 P4 | 4 | MSRC001_0069 | P2 | 2 | MSRC001_0069 P5 | 5 | MSRC001_006A | P3 | 3 | MSRC001_006A P6 | 6 | MSRC001_006B | P4 | 4 | MSRC001_006B
1b	a system control circuit which has a register, wherein said system control circuit carries out the clock frequency transition between said ordinary operation modes and said special modes in response to a change of a value in said register, and also carries out the clock frequency transition among said ordinary operation modes in response to said clock control library;	The Accused Product has a system control circuit, for example, the System Management Unit and/or the System Management Controller, that has a register. See e.g., BKDG: • Northbridge: • One communication packet routing block referred to as the northbridge (NB). The NB routes transactions between the cores, the link, and the DRAM interfaces. It includes the configuration register space for the device. BKDG, section 2.12: **2.12 System Management Unit (SMU)** The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. The SMU contains a microcontroller to assist with many of these tasks.

	Limitation	Contention
		See also BKDG for 14h Family 00h-0Fh Processors, section 2.12: **2.12 System Management Unit (SMU)** The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details. **2.12.1 Microcontroller** The SMU contains a microcontroller with a 16k ROM and a 16k RAM. The NB/SMU controls the clock frequency transitions between the core P-states. See e.g., SATHE et al.: RESONANT-CLOCK DESIGN FOR A POWER-EFFICIENT, HIGH-VOLUME X86-64 MICROPROCESSOR, p.144 tion of the configuration programming interface. On receiving notification from the NB of a PState transition, the core implements a PState entry sequence which transitions the core into a clock-gated state. A program sequencer then accesses a
1c	a clock generation circuit that receives a plurality of standard clocks, wherein said clock generation circuit generates a clock supplied to said central processing unit according to control by said system control circuit; and	The Accused Products include a digital frequency synthesizer clock generation circuit, including the core PLL, clock multipliers and dividers, and/or the digital frequency synthesizer. The DFS receives a plurality of standard clocks, for example, different phases of the PLL clock or reference clock, and outputs the core clock such as CCLK to the CPU. The clock generator circuit includes at least the PLL and the digital frequency synthesizer. The DFS receives a plurality of standard clocks (the 4 phases-offset references provided by the PLL), and generates CCLK according to control by the SMU: Singh et al., Jaguar: A Next-Generation Low-Power x86-64 Core, pp. 25-26:

	Limitation	Contention
		

	Limitation	Contention
		 • Clock dividing for various operating modes • Duty cycle adjuster for independent control of duty cycle within each block See also:

	Limitation	Contention
		

	Limitation	Contention
		 Source: Foley et al., A Low-Power Integrated x86-64 And Graphics Processor For Mobile Computing Devices, Fig. 1., 11; p.224-225.
1d	a second memory that stores an application program, wherein calling of said clock control library	The Accused Products include a second memory, such as the hierarchy of L1, L2 caches that stores an application program, including but not limited to ACPI drivers, power management utilities, APIs provided by AMD, or any software that causes the SMU/SMC firmware to perform P-state transitions. See BKDG section 2.5.3.1.2; p. 548:

	Limitation	Contention
	and changing of said register value are programmably controlled by said application program to enable user selectable clock frequency transitions,	**2.5.3.1.2 Core P-state Control** Core P-states are dynamically controlled by software and are exposed through ACPI objects (refer to 2.5.3.1.8.3 [ACPI Processor P-state Objects]). Software requests a core P-state change by writing a 3 bit index corresponding to the desired P-state number to MSRC001_0062[PstateCmd] of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's MSRC001_0062[PstateCmd]. Boosted P-states may not be directly requested by software. Whenever software requests the P0 state on a processor that supports APM (i.e. writes 000b to MSRC001_0062[PstateCmd]), hardware dynamically places the core into the highest-performance P-state possible as determined by APM. See 2.5.9 [Application Power Management (APM)]. Hardware sequences the frequency and voltage changes necessary to complete a P-state transition as specified by 2.5.3.1.5 [Core P-state Transition Behavior] with no additional software interaction required. Hardware also coordinates frequency and voltage changes when differing P-state requests are made on cores that share a frequency or voltage plane. See 2.5.2 [Frequency and Voltage Domain Dependencies] for details about hardware coordination.

	Limitation	Contention
		MSRC001_0062 P-state Control Bits | Description 63:3 | MBZ. 2:0 | **PstateCmd: P-state change command**. Read-write; Not-same-for-all. Cold reset value varies by product; after a warm reset, value initializes to the P-state the core was in prior to the reset. Writes to this field cause the core to change to the indicated non-boosted P-state number, specified by MSRC001_00[6B:64]. 0=P0, 1=P1, etc. P-state limits are applied to any P-state requests made through this register. Reads from this field return the last written value, regardless of whether any limits are applied. This field uses software P-state numbering. See 2.5.3 [CPU Power Management] and 2.5.3.1.1.1 [Software P-state Numbering].
1e	wherein said special modes comprise a first special mode in which clock supply to principal constituents of said central processing unit is halted, a second special mode in which clock supply to an entirety of said central processing unit is halted, and a third special mode in which supply of power to the entirety of said central processing unit is halted.	The Accused Products include a first special mode in which clock supply to principal constituents of said central processing unit is halted, for example the core C1 (CC1) state: **2.5.3.2.3.2 Core C1 (CC1) State** When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct].

	Limitation	Contention
		2.5.3.2.3.2 Core C1 (CC1) State When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct]. **2.5.3.2.3.3 Core C6 (CC6) State** A core can gate off power to its internal logic when it enters any non-C0 state. This power gated state is known as CC6. In order to enter CC6, hardware first enters CC1 then checks D18F4x118/D18F4x11C[PwrGateEnCstAct]. Power gating reduces the amount of power consumed by the core. VDD voltage is not reduced when a core is in CC6. The following sequence occurs when a core enters the CC6 state: 1. If MSRC001_0071[CurPstate] < D18F3xA8[PopDownPstate], transition the core P-state to D18F3xA8[PopDownPstate]. 2. Internal core state is saved to L1 cache . 3. L1 cache is flushed to L2 cache. See 2.5.3.2.3.1 [C-state Probes and Cache Flushing]. 4. Power is removed from the core and the core PLL/voltage regulator is powered down as specified by D18F5x128[CC6PwrDwnRegEn].

	Limitation	Contention

D18F4x11[C:8] C-state Control

D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states].

- D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr].
- D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1.
- D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2.

D18F4x118 C-state Control 1

7:5	**ClkDivisorCstAct0: clock divisor**. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or: • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register. Bits Description Bits Description 000b /1 100b /16 001b /2 101b /128 010b /4 110b /512 011b /8 111b Turn off clocks. See CacheFlushTmrSelCstAct0.

	Limitation	Contention
		The Accused Products include a second special mode in which clock supply to an entirety of said central processing unit is halted, for example the package C1 (PC1) state. See e.g., 14h BKDG: **2.5.3.2.3.3 Package C1 (PC1) State** The processor enters the PC1 state with auto-Pmin when all of the following are true: • All cores are in the CC1 state or deeper. If D18F4x1AC[CstPminEn] indicates that auto-Pmin is enabled when the processor enters PC1, the P-state for all cores is transitioned as specified by 2.5.3.2.7.1 [Auto-Pmin]. Regardless of the state of D18F4x1AC[CstPminEn], all core clocks are ramped to the frequency specified by D18F4x1A8[AllHaltCpuDid]. **D18F4x1A8 CPU State Power Management Dynamic Control 0** Reset: 0000_0000h. 9:5 **AllHaltCpuDid**. Read-write. BIOS: 1Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State]. Bits — Divisor 1Ch-00h — Reserved. 1Dh — 128 1Eh — 512 1Fh — Clocks off. See D18F4x1A8[SingleHaltCpuDid]. The Accused Products include a third special mode in which supply of power to the entirety of said central processing unit is halted, for example the package C6 (PC6) state:

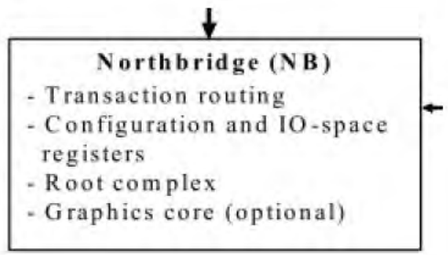
	Limitation	Contention
		2.5.3.2.3.4 Package C6 (PC6) State When all cores enter a non-C0 state, VDD can be reduced to a non-operational voltage that does not retain core state. This state is known as PC6 and reduces the amount of static and dynamic power consumed by all cores. The following actions are taken by hardware prior to PC6 entry: 1. If MSRC001_0071[CurPstate] < D18F3xA8[PopDownPstate], transition the core P-state to D18F3xA8[PopDownPstate]. 2. For all cores not in CC6, internal core state is saved to L1 cache . 3. For all cores not in CC6, L1 cache is flushed to L2 cache. See 2.5.3.2.3.1 [C-state Probes and Cache Flushing]. 4. VDD is transitioned to the VID specified by D18F5x128[PC6Vid]. 5. If the core PLLs are not powered down during CC6 entry (see 2.5.3.2.3.3 [Core C6 (CC6) State]), then they are powered down as specified by D18F5x128[PC6PwrDwnRegEn]. **D18F5x128 Clock Power/Timing Control 3** 6:0 **PC6Vid[6:0]: package C6 vid**. Read-write. Cold reset: Product-specific. PC6Vid[7:0] = {PC6Vid[7], PC6Vid[6:0]}. PC6Vid[7:0] specifies the VID driven in the PC6 state. See 2.5.3.2.3.4 [Package C6 (PC6) State] and 2.5.1.3.2 [Low Power Voltages].

	Limitation	Contention

		2.5.1.3.2 Low Power Voltages
		
		In order to save power, voltages lower than those normally needed for operation may be applied to the VDD power plane while the processor is in a C-state or S-state. The lower voltage is defined as follows:
		
		• PC6Vid: D18F5x128[PC6Vid] specifies a voltage that does not retain the CPU caches or the core microarchitectural state. PC6Vid does not allow execution and is only applied to the cores. See 2.5.3.2.3.4 [Package C6 (PC6) State].
		
		2.5.1.4.1 Hardware-Initiated Voltage Transitions
		
		When software requests any of the following state changes, or hardware determines that any of the following state changes are necessary, hardware coordinates the necessary voltage changes:
		
		• VDD:
		  • Core P-state transition. See 2.5.3.1 [Core P-states].
		  • Package C-state transition. D18F5x128[PC6Vid] specifies a voltage that does not retain the CPU caches or the core microarchitectural state. PC6Vid does not allow execution and is only applied to the cores. See 2.5.3.2.3.4 [Package C6 (PC6) State].
		  • S-state transition. See 2.5.8.1 [S-states].

2p	A system LSI as claimed in claim 1, wherein said clock control library comprises:	
2a	a plurality of libraries that control said system control circuit and said	The clock control libraries of the Accused Products contain a plurality of libraries that control the SMU and clock generator to transition clock frequencies. For example, source code provided by AMD to coreboot indicates that P-state

	Limitation	Contention
	clock generation circuit to transition the clock frequencies supplied to said central processing unit; and	and C-state transitions are controlled by separate libraries: https://github.com/coreboot/coreboot/tree/master/src/vendorcode/amd/agesa/f14/Proc/CPU/Feature
2b	a main library which is called by said application program and selects any one of said libraries in correspondence with the clock frequency supplied to said central processing unit.	As discussed above, P-states and C-states may be controlled by software, which includes a main library that calls upon the plurality of libraries.
3p	A system LSI as claimed in claim 2,	
3a	wherein said main library is described using a same program language as said application program.	The main library in the SMU firmware and the application program instructions stored in the caches are both use the same language such as machine code.
5p	A system LSI as claimed in claim 2,	
5a	wherein each of said libraries is described using a program language capable of directly controlling said clock generation circuit and said system control circuit.	The SMU firmware directly controls the SMU hardware.
6p	A system LSI as claimed in claim 5,	
6a	wherein each of said libraries is described using an assembler	The SMU firmware directly controls the SMU hardware and is described using an assembler language such as machine code.

	Limitation	Contention
	language.	
7p	7. A system LSI as claimed in claim 1, wherein said system control circuit comprises:	
7a	a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit;	The NB of the Accused Products contains a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit. The NB contains the configuration register space for the Accused Products. *See* BKDG: See e.g., BKDG:  BKDG, section 2.12:

	Limitation	Contention
		2.12 System Management Unit (SMU) The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details. **2.12.1 Microcontroller** The SMU contains a microcontroller with a 16k ROM and a 16k RAM. Configuration space register mnemonics are defined in section 3.1 of the BKDG: • **DXFYxZZZ**: PCI-defined configuration space; X specifies the hexadecimal device number (this may be 1or 2 digits), Y specifies the function number, and ZZZ specifies the hexidecimal byte address (this may be 2 or 3 digits; e.g., D18F3x40 specifies the register at device 18h, function 3, and address 40h). See 2.7 [Configuration Space], for details about configuration space. the core C1 (CC1) state: **2.5.3.2.3.2 Core C1 (CC1) State** When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct].

	Limitation	Contention

D18F4x11[C:8] C-state Control

D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states].

- D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr].
- D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1.
- D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2.

D18F4x118 C-state Control 1

7:5	**ClkDivisorCstAct0: clock divisor**. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or: • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.

Bits	Description	Bits	Description
000b	/1	100b	/16
001b	/2	101b	/128
010b	/4	110b	/512
011b	/8	111b	Turn off clocks.

See CacheFlushTmrSelCstAct0.

	Limitation	Contention
7b	a clock halting register that receives the clock from said clock generation circuit and individually sets the clock to be halted or supplied;	the core C1 (CC1) state: **2.5.3.2.3.2 Core C1 (CC1) State** When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct]. **D18F4x11[C:8] C-state Control** D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states]. • D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]. • D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1. • D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2. **D18F4x118 C-state Control 1**

	Limitation	Contention
		7:5 **ClkDivisorCstAct0: clock divisor**. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or: • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register. Bits DescriptionBits Description 000b /1 100b /16 001b /2 101b /128 010b /4 110b /512 011b /8 111b Turn off clocks. See CacheFlushTmrSelCstAct0.
7c	And a status register that judges a state of said central processing unit immediately after being released from said third special mode.	The Accused Products contain a status register that judges a state of the CPU after waking from PC6. See 14h BKDG:

	Limitation	Contention
		2.5.3.2.7.2 Exiting PC6 If the PService timer is enabled when the processor exits PC6, all cores transition to the P-state specified by D18F4x1AC[PstateIdCoreOffExit]. The cores remain in this state until one of the following occurs: • The PService timer expires while the package is in C0: In this case, the cores transition back to the last P-state requested by software. • The package enters PC1 without auto-Pmin: In this case, the PService timer continues counting. If it expires while in PC1, the cores remain in the P-state specified by D18F4x1AC[PstateIdCoreOffExit] until they return to C0, at which time they transition to the last P-state requested by software. • The package enters PC1 with auto-Pmin: In this case, the PService timer stops counting and the cores enter the PService state. • The package enters PC6: In this case the PService timer stops counting and the actions associated the requested package C-state occur. See 2.5.3.2.3.4 [Package C6 (PC6) State]. If the PService timer is disabled when the processor exits PC6, the cores transition back to the last P-state requested by software. See also 14h BKDG pp.320-321: **D18F4x1AC CPU State Power Management Dynamic Control 1** 18:16 **PstateIdCoreOffExit**. Read-write. Reset: 0. BIOS: See 2.5.3.2.9. When exiting the package C6 state, the core transitions to the P-state specified by this register. See 2.5.3.2.7.2 [Exiting PC6]. If PC6 is enabled (see 2.5.3.2.9 [BIOS Requirements for C-state Initialization]), PstateIdCoreOffExit must be programmed to the lowest-performance P-state displayed to the operating system or to any lower-performance P-state. This P-state must have a core clock frequency of at least 400 MHz. Programming this field to 0 causes the core to transition to the last P-state requested by software when exiting package C6. This field uses hardware P-state numbering. See 2.5.3.1.2.2 [Hardware P-state Numbering].

	Limitation	Contention
10p	A system LSI as claimed in claim 1,	
10a	wherein said first memory and said second memory are two independent memories which are separated from each other.	As detailed above, the first memory in the SMU and the second memory in the caches are independent memories that are separated from each other.

Exhibit B.4: Preliminary Infringement Contention Claim Chart for U.S. Patent 6,895,519

Accused Products: AMD Family 17h Products

These preliminary infringement contentions were prepared without the benefit of the Court's claim construction or the parties' exchange of constructions. As of the date of these contentions, AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court's constructions or to account for new information that becomes available.

	Limitation	Contention
1p	A system LSI having a plurality of ordinary operation modes and a plurality of special modes in response to clock frequencies supplied to a central processing unit, comprising:	To the extent that the preamble is limiting, Aquila contends that it is met. For example, each product in the 17h Accused Product Family ("Accused Product") is a system LSI. The Accused Product has a plurality of ordinary operation modes, for example the Core P-states. See e.g., AMD Ryzen Master Overclocking Guide ("OC Guide"), p.11: 1. The frequency of processor core clock is determined by a combination of the software-requested p-state and then adjusted by a combination of numerous power and performance optimizing features to attain any of number of fine grain p-states around that software-requested p-state. See also OC Guide, p.13: 3) CPU low power c-states (CC1, CC6, and PC6) and software visible p-states (P1 and P2) remain operational and may be requested by software so that power savings can be achieved. Documentation from other AMD products provide exemplary guidance on the AMD's implementation of P-states and C-states. *See, e.g.*, BIOS and Kernel Developer's Guide for AMD Family 16h Models 00h-0Fh Processors ("16h BKDG"), §2.5.3.1:

	Limitation	Contention

2.5.3.1 Core P-states

Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states (P0 through P7), specified in MSRC001_00[6B:64]. Out of cold reset, the voltage and frequency of the compute units is specified by MSRC001_0071[StartupPstate].

16h BKDG, Table 9:

Table 9: Software P-state Naming

D18F4x15C[NumBoost-States]=1		D18F4x15C[NumBoost-States]=3	
P-state Name	**Corresponding MSR Address**	**P-state Name**	**Corresponding MSR Address**
Pb0	MSRC001_0064	Pb0	MSRC001_0064
P0	MSRC001_0065	Pb1	MSRC001_0065
P1	MSRC001_0066	Pb2	MSRC001_0066
P2	MSRC001_0067	P0	MSRC001_0067
P3	MSRC001_0068	P1	MSRC001_0068
P4	MSRC001_0069	P2	MSRC001_0069
P5	MSRC001_006A	P3	MSRC001_006A
P6	MSRC001_006B	P4	MSRC001_006B

All sections and register definitions use software P-state numbering unless otherwise specified.

The Accused Product Family has a plurality of special modes, for example, the Core C-states or deep sleep modes such as ACPI S3 or connected standby S0i3. *See* OC Guide, p.13:

	Limitation	Contention
		3) CPU low power c-states (CC1, CC6, and PC6) and software visible p-states (P1 and P2) remain operational and may be requested by software so that power savings can be achieved. See also OC guide, p.11: 4. Software requested p-state or halt states adjust the level of power to which those internal control mechanisms manage. For example, when software executes a HALT instruction on a processor core, that core will enter the C1 reduced-power state. If that core does not receive an interrupt to resume execution, it will progress to increasingly-lower power states until finally saving the state of the core and being powered off. *See* also 16h BKDG, §§ 2.5.3.2, 2.5.3.2.1, 2.5:

	Limitation	Contention
		2.5.3.2 Core C-states C-states are processor power states. C0 is the operational state in which instructions are executed. All other C-states are low-power states in which instructions are not executed. When coming out of warm and cold reset, the processor is transitioned to the C0 state. **2.5.3.2.1 C-state Names and Numbers** C-states are often referred to by an alphanumeric naming convention, C1, C2, C3, etc. The mapping between ACPI defined C-states and AMD specified C-states is not direct. AMD specified C-states are referred to as IO-based C-states. Up to three IO-based C-states are supported, IO-based C-state 0, 1, and 2. The IO-based C-state index corresponds to the offset added to MSRC001_0073[CstateAddr] to initiate a C-state request. See 2.5.3.2.2 [C-state Request Interface]. The actions taken by the processor when entering a low-power C-state are configured by software. See 2.5.3.2.3 [C-state Actions] for information about AMD specific actions.

Limitation	Contention

2.5 Power Management

The processor supports many power management features in a variety of systems. Table 8 provides a summary of ACPI states and power management features and indicates whether they are supported.

Table 8: Power Management Support

ACPI/Power Management State	Supported	Description
G0/S0/C0: Working	Yes	
G0/S0/C0: Core P-state transitions	Yes	2.5.3.1 [Core P-states]
G0/S0/C0: NB P-state transitions	Yes	2.5.4.1 [NB P-states]
G0/S0/C0: Hardware thermal control (HTC)	Yes	2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)]
G0/S0/Per-core IO-based C-states	Yes	2.5.3.2 [Core C-states] and 2.5.1.3.2 [Low Power Voltages]
G0/S0/C1: Halt	Yes	
G0/S0/CC6: Per-core Power gating	Yes	2.5.3.2 [Core C-states]
G0/S0: CPC-L2 power gating	Yes	2.5.3.2 [Core C-states]
G0/S0/PC6: 0V support (VDD power plane).	Yes	2.5.3.2 [Core C-states] and 2.5.1.3.2 [Low Power Voltages]
G0/S0/Cx: Cache flushing support	Yes	2.5.3.2.3.1 [C-state Probes and Cache Flushing]
G0/S0: Northbridge C-states (DRAM self-refresh, NB clock-gating)	Yes	2.5.4.2 [NB C-states]
G1/S1: Stand By (Powered On Suspend)	No	
G1/S3: Stand By (Suspend to RAM)	Yes	2.5.8.1 [S-states]
G1/S4: Hibernate (Suspend to Disk)	Yes	
G1/S5: Shut Down (Soft Off)	Yes	
G3 Mechanical Off	Yes	
Parallel VID Interface	No	2.5.1 [Processor Power Planes And Voltage Control]
Serial VID Interface 1	No	
Serial VID Interface 2	Yes	
Single-plane systems	No	
Number of voltage planes	2	2.5.1 [Processor Power Planes And Voltage Control]
APM: Application Power Management	Yes	2.5.9 [Application Power Management (APM)]

	Limitation	Contention
		Furthermore, the Core P-states and Core C-states are in response to clock frequencies supplied to a central processing unit. For example, the core P-states are "characterized" by "core frequency;" core P-state changes are further requested by software. *See* OC Guide p.13: a. The P1 and P2 p-state tables may also be modified to adjust the voltage and frequency of the CPU when running in software-requested, reduced-performance states. These may also be left at stock values. See also OSRR for AMD Family 17h processors, Models 00h-2Fh, p.130: **MSRC001_006[4...B] [P-state [7:0]] (Core::X86::Msr::PStateDef)** Read-write. Reset: X000_0000_XXXX_XXXXh. Each of these registers specify the frequency and voltage associated with each of the core P-states. The CpuVid field in these registers is required to be programmed to the same value in all cores of a processor, but are allowed to be different between processors in a multi-processor system. All other fields in these registers are required to be programmed to the same value in each core of the coherent fabric. *See e.g.,* 16h BKDG, § 2.5.3.1, 2.5.3.1.2: **2.5.3.1 Core P-states** Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states (P0 through P7), specified in MSRC001_00[6B:64]. Out of cold reset, the voltage and frequency of the compute units is specified by MSRC001_0071[StartupPstate].

	Limitation	Contention
		Support for dynamic core P-state changes is indicated by more than one enabled selection in MSRC001_00[6B:64][PstateEn]. At least one enabled P-state (P0) is specified for all processors. Software requests core P-state changes for each core independently using the hardware P-state control mechanism (a.k.a. fire and forget). Support for hardware P-state control is indicated by CPUID Fn8000_0007_EDX[HwPstate]=1b. Software may not request any P-state transitions using the hardware P-state control mechanism until the P-state initialization requirements defined in 2.5.3.1.6 [BIOS Requirements for Core P-state Initialization and Transitions] are complete. The processor supports independently-controllable frequency planes for each compute unit and the NB; and independently-controllable voltage planes. See 2.5.1 [Processor Power Planes And Voltage Control] for voltage plane definitions. The following terms may be applied to each of these planes: • FID: frequency ID. Specifies the PLL frequency multiplier, relative to the reference clock, for a given domain. • DID: divisor ID. Specifies the post-PLL power-of-two divisor that can be used to reduce the operating frequency. • COF: current operating frequency. Specifies the operating frequency as a function of the FID and DID. Refer to CoreCOF for the CPU COF formula and NBCOF for the NB COF formula. • VID: voltage ID. Specifies the voltage level for a given domain. Refer to 2.5.1.2.1 [MinVid and MaxVid Check] for encodings. All FID and DID parameters for software P-states must be programmed to equivalent values for all cores and NBs in the coherent fabric. See 2.5.3.1.1.1 [Software P-state Numbering]. Refer to MSRC001_00[6B:64] and D18F5x16[C:0] for further details on programming requirements.

	Limitation	Contention
		2.5.3.1.2 Core P-state Control Core P-states are dynamically controlled by software and are exposed through ACPI objects (refer to 2.5.3.1.8.3 [ACPI Processor P-state Objects]). Software requests a core P-state change by writing a 3 bit index corresponding to the desired P-state number to MSRC001_0062[PstateCmd] of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's MSRC001_0062[PstateCmd]. Boosted P-states may not be directly requested by software. Whenever software requests the P0 state on a processor that supports APM (i.e. writes 000b to MSRC001_0062[PstateCmd]), hardware dynamically places the core into the highest-performance P-state possible as determined by APM. See 2.5.9 [Application Power Management (APM)]. Hardware sequences the frequency and voltage changes necessary to complete a P-state transition as specified by 2.5.3.1.5 [Core P-state Transition Behavior] with no additional software interaction required. Hardware also coordinates frequency and voltage changes when differing P-state requests are made on cores that share a frequency or voltage plane. See 2.5.2 [Frequency and Voltage Domain Dependencies] for details about hardware coordination. Similarly, C-states are requested by software, for example when executing a HALT instruction, and also dependent upon clock frequency ("reduced power" or "lower power" state). *See* OC Guide, p.11: 4. Software requested p-state or halt states adjust the level of power to which those internal control mechanisms manage. For example, when software executes a HALT instruction on a processor core, that core will enter the C1 reduced-power state. If that core does not receive an interrupt to resume execution, it will progress to increasingly-lower power states until finally saving the state of the core and being powered off.

	Limitation	Contention
		See also 16h BKDG §§ 2.5.3.2.3.2, 2.5.3.2.3.3, 2.5.3.2.3.2; p.320-321: **2.5.3.2.3.2 Core C1 (CC1) State** When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct]. **2.5.3.2.3.3 Core C6 (CC6) State** A core can gate off power to its internal logic when it enters any non-C0 state. This power gated state is known as CC6. In order to enter CC6, hardware first enters CC1 then checks D18F4x118/D18F4x11C[PwrGateEnCstAct]. Power gating reduces the amount of power consumed by the core. VDD voltage is not reduced when a core is in CC6. The following sequence occurs when a core enters the CC6 state: 1. If MSRC001_0071[CurPstate] < D18F3xA8[PopDownPstate], transition the core P-state to D18F3xA8[PopDownPstate]. 2. Internal core state is saved to L1 cache . 3. L1 cache is flushed to L2 cache. See 2.5.3.2.3.1 [C-state Probes and Cache Flushing]. 4. Power is removed from the core and the core PLL/voltage regulator is powered down as specified by D18F5x128[CC6PwrDwnRegEn].

	Limitation	Contention

D18F4x11[C:8] C-state Control

D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states].

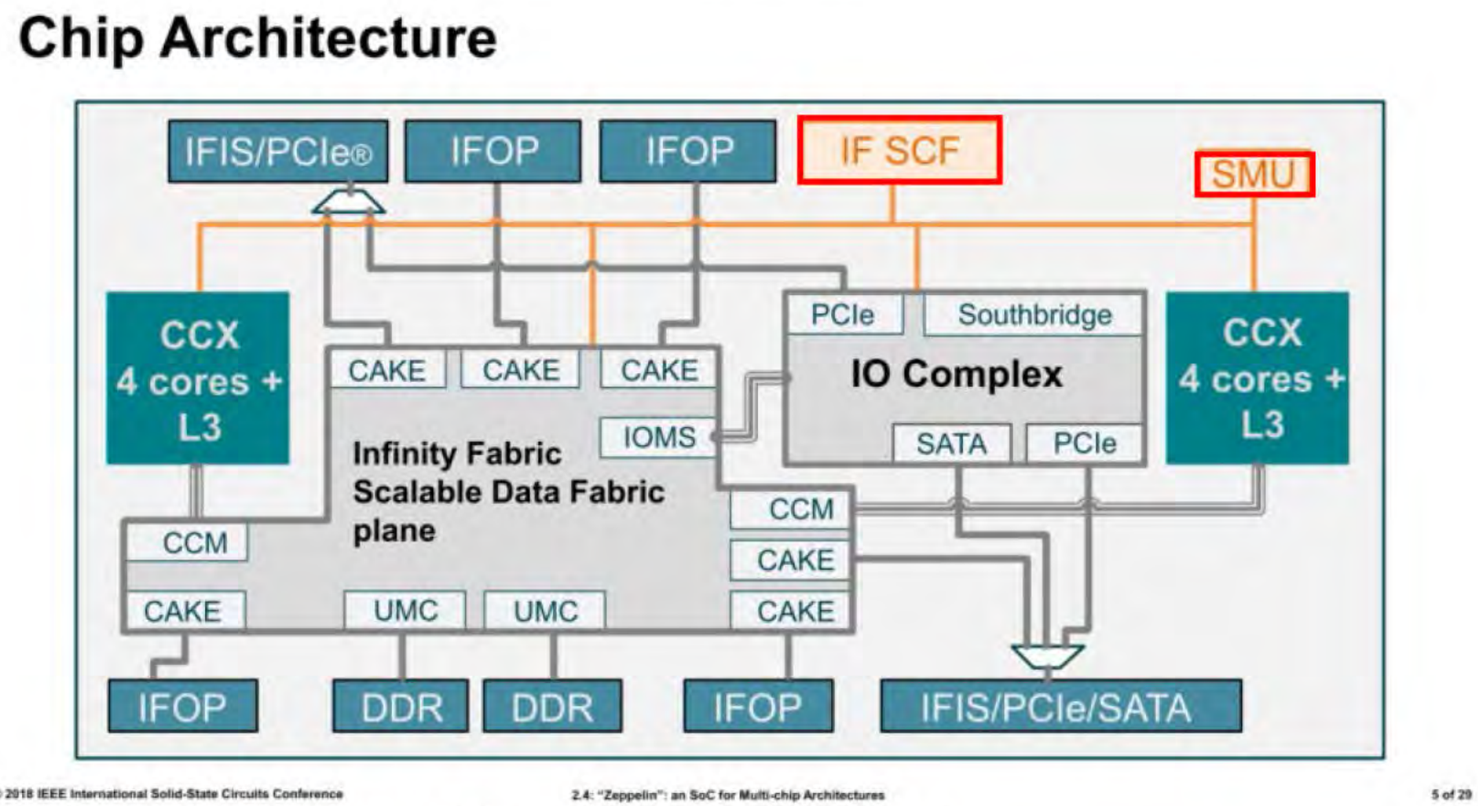
- D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr].
- D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1.
- D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2.

D18F4x118 C-state Control 1

7:5	**ClkDivisorCstAct0: clock divisor**. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or: • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register. Bits Description Bits Description 000b /1 100b /16 001b /2 101b /128 010b /4 110b /512 011b /8 111b Turn off clocks. See CacheFlushTmrSelCstAct0.

	Limitation	Contention
1a	a first memory that stores a clock control library for controlling a clock frequency transition between said ordinary operation modes;	The Accused Products include a first memory that stores a clock control library. For example, the SMU and/or Scalable Control Fabric and Scalable Data Fabric contains memory that stores the firmware and configuration space registers, including a clock control library. The clock control library controls clock frequency transition between the P-states. PPR for AMD Family 17h Models 00h-0Fh, pp. 26-27: • 16MB L3 total • Scalable Data Fabric. This provides the data path that connects the compute complexes, the I/O interfaces, and the memory interfaces to each other. • Handles request, response, and data traffic • Handles probe traffic to facilitate coherency, including a probe filter supporting up to 512GB per DRAM channel • Handles interrupt request routing (APIC) • PSP and SMU • MP0 (PSP) and MP1 (SMU) microcontrollers • This document refers to the AMD Secure Processor technology as Platform Security Processor (PSP). • Thermal monitoring • Fuses • Clock control

	Limitation	Contention

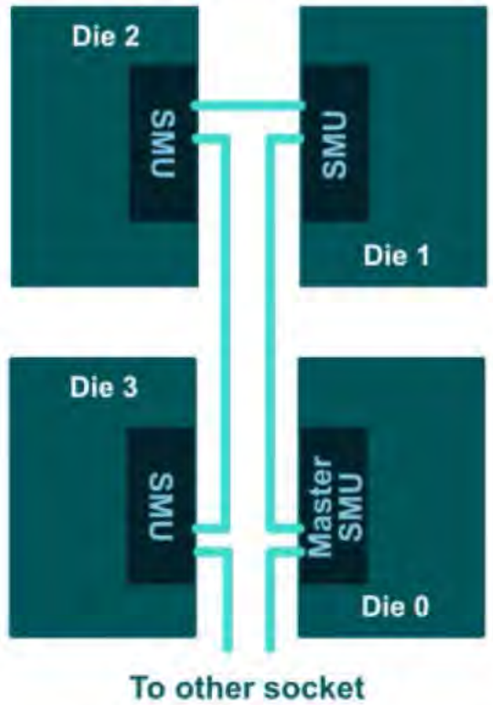


Source: Beck et al., "Zeppelin": an SoC for Multi-chip Architectures, p. 5.

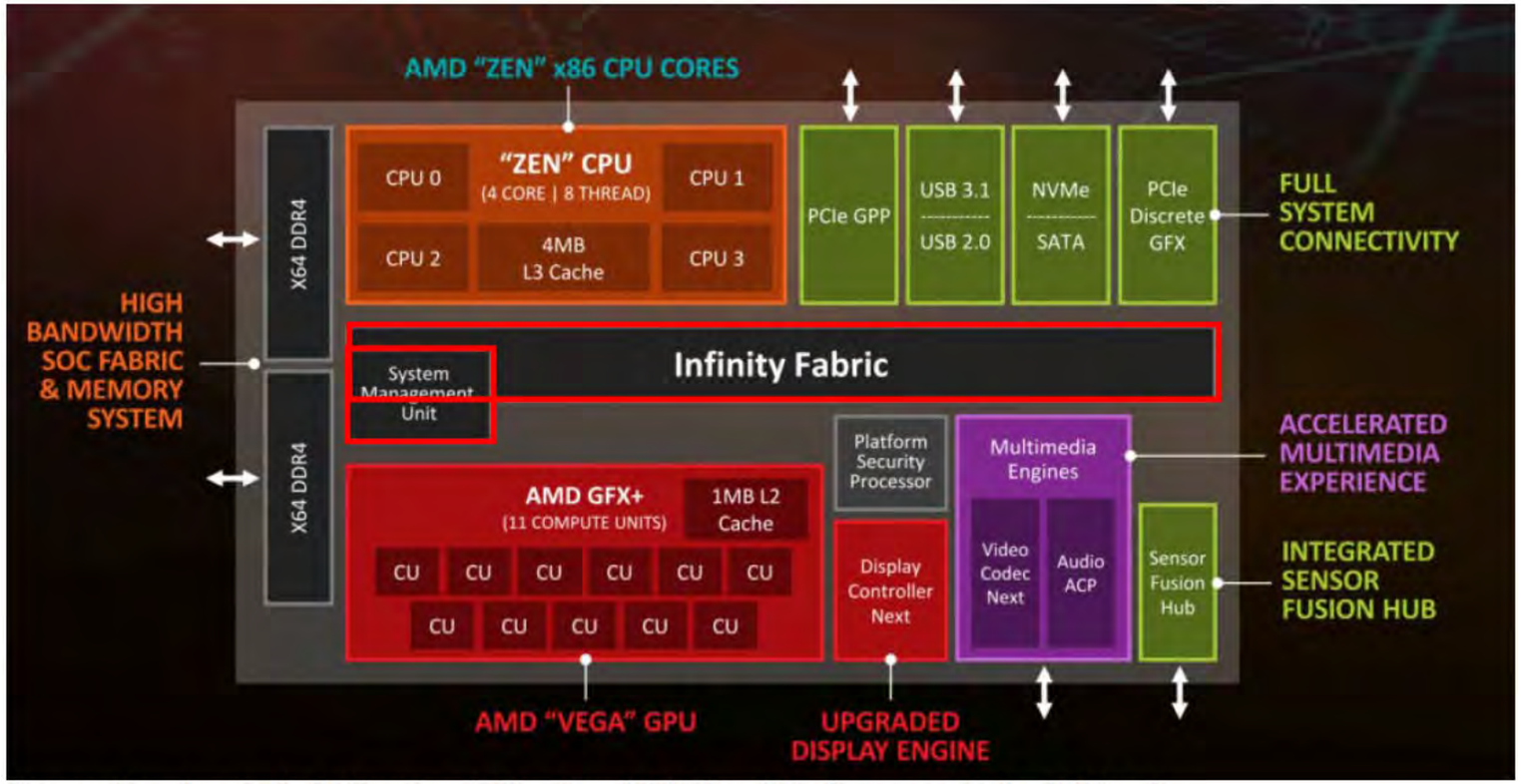
	Limitation	Contention

Hierarchical Power Management

- System Management Unit (SMU) uses IF Scalable Control Fabric (SCF) plane
- SCF: single-lane IFIS SerDes link for chip-to-chip or socket-to-socket
- SMU calculation hierarchy for voltage level control, C-State Boost, thermal management, electrical design current management
  - Local chip SMU fast loop
  - Master chip SMU slower loop



Source: Beck, p.12.

	Limitation	Contention
		 Source: Bouvier et al., Delivering A New Level Of Visual Performance In An SOC, p.3 See e.g., 16h BKDG, 29:

	Limitation	Contention
		• Northbridge: • One communication packet routing block referred to as the northbridge (NB). The NB routes transactions between the cores, the link, and the DRAM interfaces. It includes the configuration register space for the device. 16h BKDG, section 2.12: **2.12 System Management Unit (SMU)** The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. The SMU contains a microcontroller to assist with many of these tasks. See also 16h BKDG, Table 10: **Table 10: Software P-state Control**

D18F4x15C[NumBoostStates]=1			D18F4x15C[NumBoostStates]=3		
P-state Name	**Index Used for Requests/Status**	**Corresponding MSR Address**	**P-state Name**	**Index Used for Requests/Status**	**Corresponding MSR Address**
Pb0	n/a	MSRC001_0064	Pb0	n/a	MSRC001_0064
P0	0	MSRC001_0065	Pb1	n/a	MSRC001_0065
P1	1	MSRC001_0066	Pb2	n/a	MSRC001_0066
P2	2	MSRC001_0067	P0	0	MSRC001_0067
P3	3	MSRC001_0068	P1	1	MSRC001_0068
P4	4	MSRC001_0069	P2	2	MSRC001_0069
P5	5	MSRC001_006A	P3	3	MSRC001_006A
P6	6	MSRC001_006B	P4	4	MSRC001_006B

1b	a system control circuit which has a register, wherein	The Accused Product has a system control circuit, for example, the System Management Unit and/or the System Management Controller, that has a register. *See* PPR, p.27:

	Limitation	Contention

	said system control circuit carries out the clock frequency transition between said ordinary operation modes and said special modes in response to a change of a value in said register, and also carries out the clock frequency transition among said ordinary operation modes in response to said clock control library;	• PSP and SMU
		  • MP0 (PSP) and MP1 (SMU) microcontrollers
		  • This document refers to the AMD Secure Processor technology as Platform Security Processor (PSP).
		  • Thermal monitoring
		  • Fuses
		  • Clock control
		
		See e.g., 16h BKDG:
		
		• Northbridge:
		  • One communication packet routing block referred to as the northbridge (NB). The NB routes transactions between the cores, the link, and the DRAM interfaces. It includes the configuration register space for the device.
		
		16h BKDG, section 2.12:
		2.12 System Management Unit (SMU)
		
		The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. The SMU contains a microcontroller to assist with many of these tasks.
		
		See also BKDG for 14h Family 00h-0Fh Processors, section 2.12:

	Limitation	Contention
		2.12 System Management Unit (SMU) The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details. **2.12.1 Microcontroller** The SMU contains a microcontroller with a 16k ROM and a 16k RAM. The NB/SMU controls the clock frequency transitions between the core P-states. See e.g., SATHE et al.: RESONANT-CLOCK DESIGN FOR A POWER-EFFICIENT, HIGH-VOLUME X86-64 MICROPROCESSOR, p.144 tion of the configuration programming interface. On receiving notification from the NB of a PState transition, the core implements a PState entry sequence which transitions the core into a clock-gated state. A program sequencer then accesses a
1c	a clock generation circuit that receives a plurality of standard clocks, wherein said clock generation circuit generates a clock supplied to said central processing unit according to control by said system control circuit; and	The Accused Products include a digital frequency synthesizer clock generation circuit, including the core PLL, clock multipliers and dividers, and/or the digital frequency synthesizer. The DFS receives a plurality of standard clocks, for example, different phases of the PLL clock or reference clock, and outputs the core clock such as CCLK to the CPU.

	Limitation	Contention

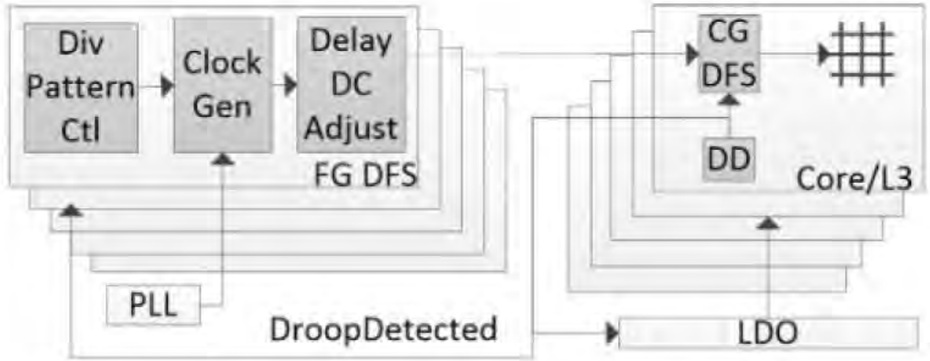


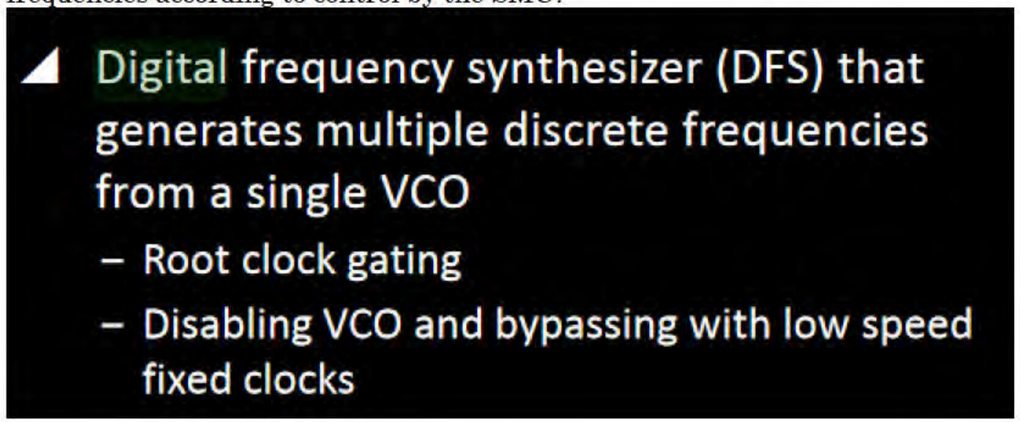
Fig. 15. Coarse grain (CG) and fine grain (FG) clock stretch.

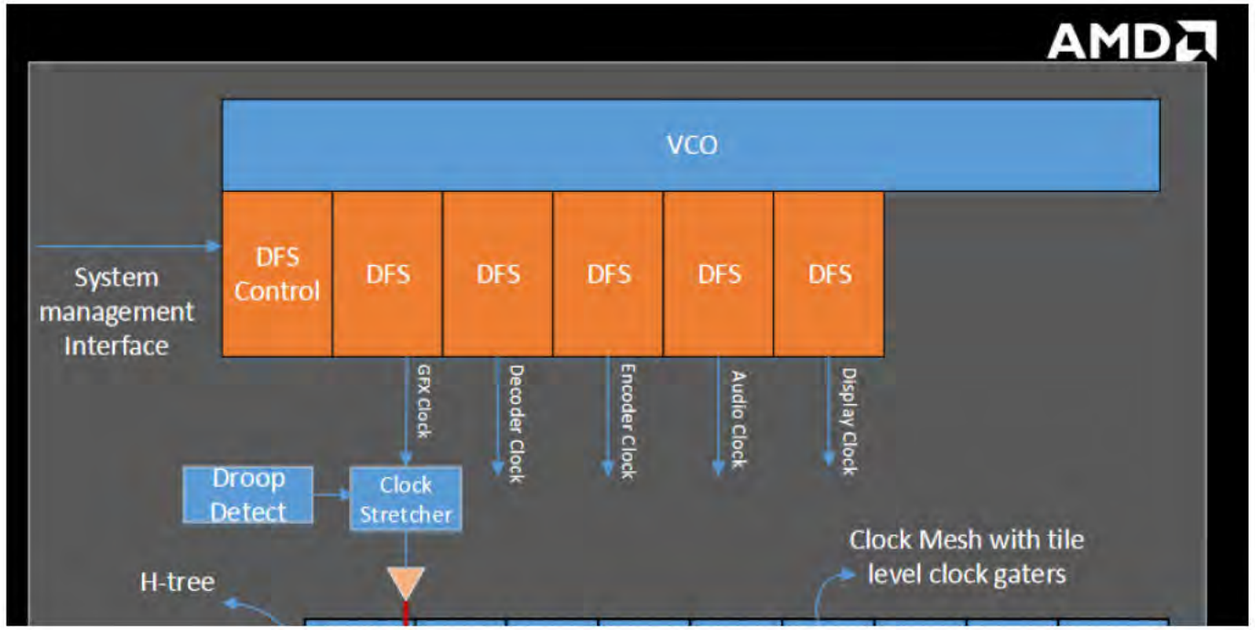
Source: Singh et al.: Energy-Efficient High-Performance x86 Core, Fig. 15:

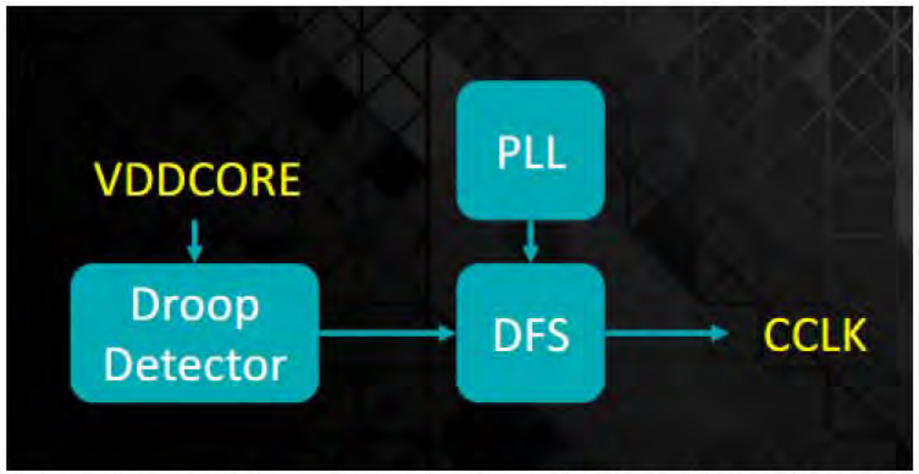
See also PPR at p.138-139:

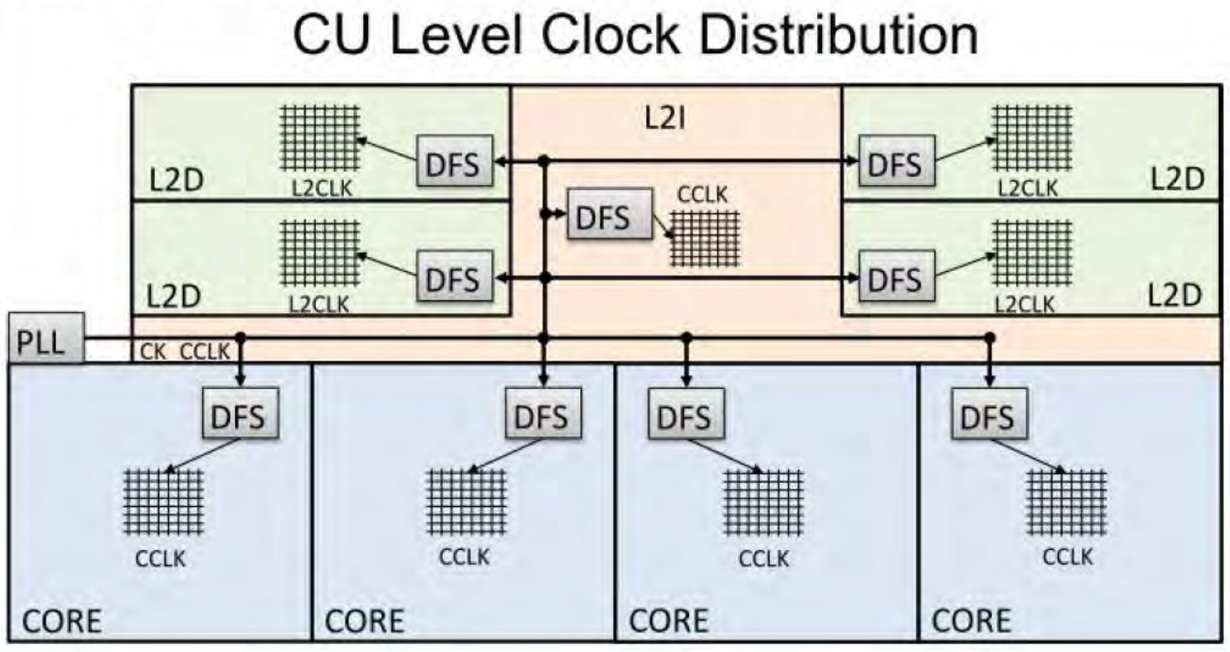
MSRC001_0064 [P-state [7:0]] (PStateDef)

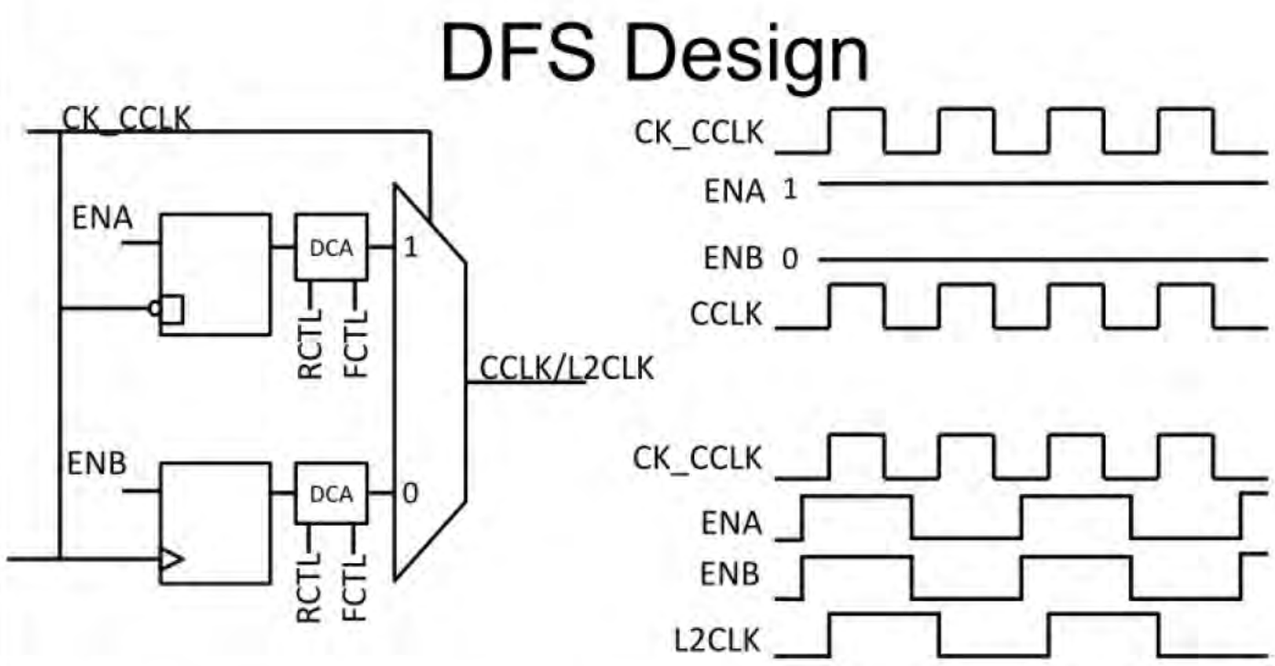
Read-write. Reset: X000_0000_XXXX_XXXXh.
Each of these registers specify the frequency and voltage associated with each of the core P-states. The CpuVid field in these registers is required to be programmed to the same value in all cores of a processor, but are allowed to be different between processors in a multi-processor system. All other fields in these registers are required to be programmed to the same value in each core of the coherent fabric. See 2.1.3 [CPU Power Management].
Core::X86::Msr::PStateDef_lthree[1:0]_core[3:0]_thread[1:0]_n[7:0]; MSRC001_006[B:4]

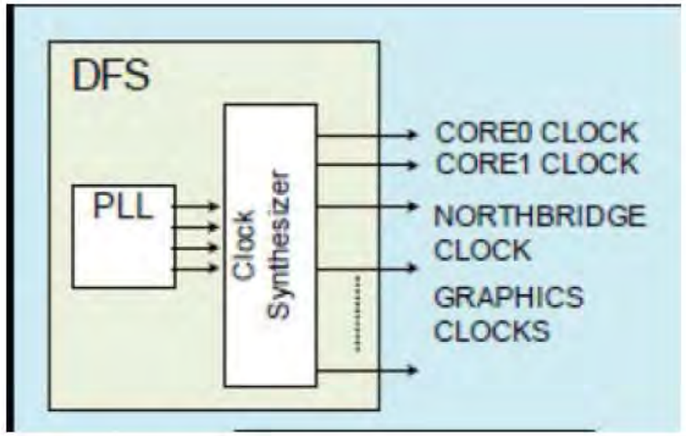
	Limitation	Contention
		13:8 **CpuDfsId**: **core divisor ID**. Read-write. Reset: XXXXXXb. Specifies the core frequency divisor; see CpuFid. For values [1Ah:08h], 1/8th integer divide steps supported down to VCO/3.25 (Note, L3/L2 fifo logic related to 4-cycle data heads-up requires core to be 1/3 of L3 frequency or higher). For values [30h:1Ch], 1/4th integer divide steps supported down to VCO/6 (DID[0] should zero if DID[5:0]>1Ah). (Note, core and L3 frequencies below 400MHz are not supported by the architecture). Core supports DID up to 30h, but L3 must be 2Ch (VCO/5.5) or less. The digital frequency synthesizer receives multiple phases of the PLL clock (see above), and generates multiple discrete frequencies according to control by the SMU. 

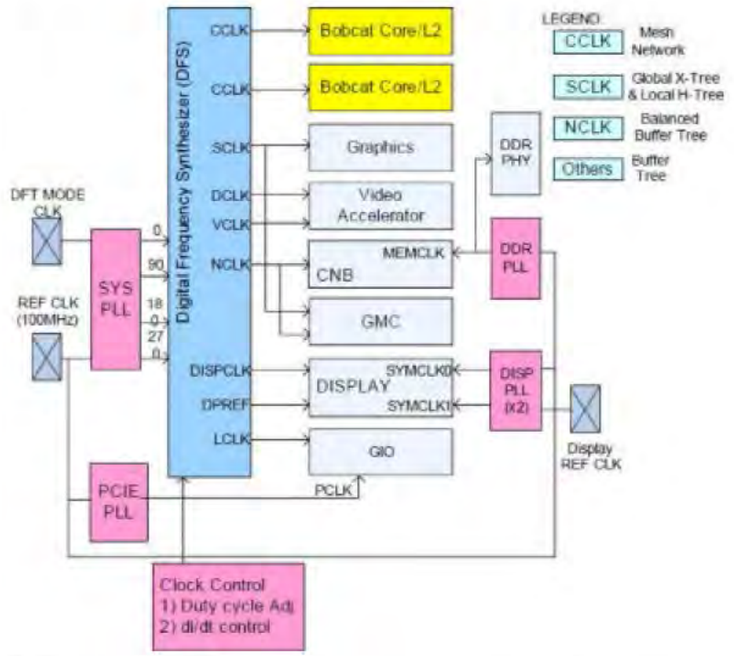
	Limitation	Contention
		 Source: Krishnan et al., "Energy Efficient Graphics and Multimedia in 28nm Carrizo APU," p.14

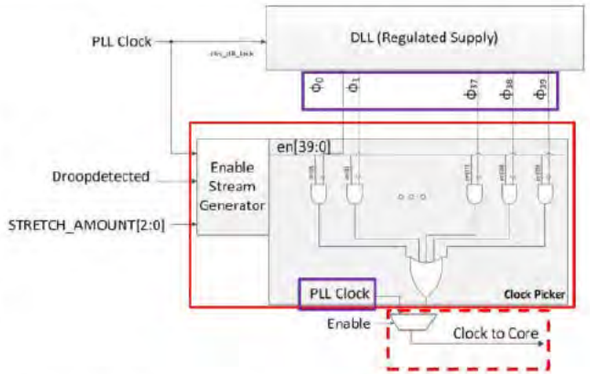
	Limitation	Contention
		 *Source: Integrated Power Conversion Strategies Across Laptop, Server, and Graphics Products, 2016 Power SOC Conference, p.4* See also, e.g., Singh et al., Jaguar: A Next-Generation Low-Power x86-64 Core, pp. 25-26:

	Limitation	Contention
		3.4: Jaguar: A Next-Generation Low-Power x86-64 Core 25 of 33 

	Limitation	Contention
		 • Clock dividing for various operating modes • Duty cycle adjuster for independent control of duty cycle within each block See also:

	Limitation	Contention
		

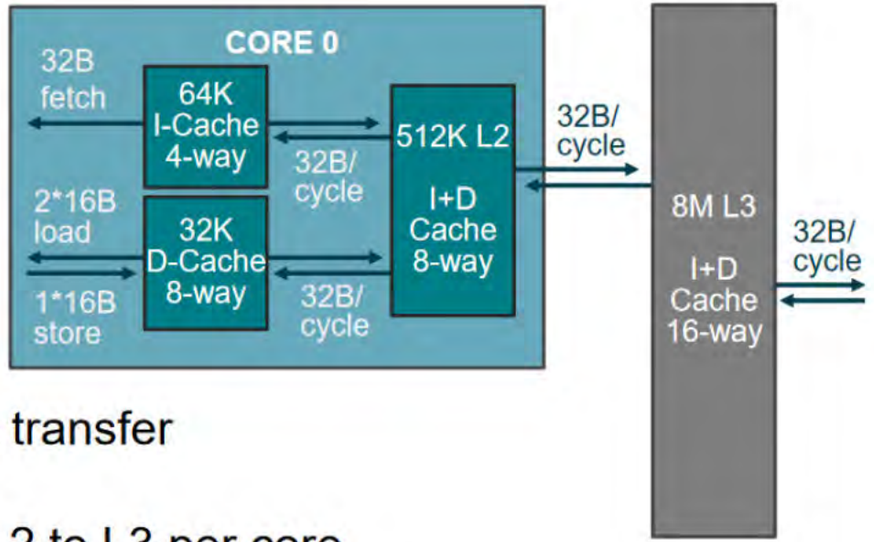
	Limitation	Contention
		 Source: Foley et al., A Low-Power Integrated x86-64 And Graphics Processor For Mobile Computing Devices, Fig. 1., 11; p.224-225. *See also e.g.,*

	Limitation	Contention
		D. Glitch Less Clock Phase Picker The glitch-less clock picker (Fig. 6) takes the 40 phases (40 total phases generated from the 20 DLL delay elements) and generates a stretched clock (configurable stretch amount) by selecting different phases of the clock. The clock picker always performs a complete loop through all the phases before selecting the 0^{th} phase (pll_clk) to avoid any contraction of the clock period. When the clock stretcher block is disabled (STRETCH_ENABLE = 0), the clock picker simply picks the pll_clk without any insertion delay of the clock stretcher logic.  Source: WILCOX et al.: STEAMROLLER MODULE AND ADAPTIVE CLOCKING SYSTEM IN 28 nm CMOS, Fig. 6
1d	a second memory that stores an application program, wherein calling of said clock control library and changing of said register value are programmably controlled by said application program to enable user selectable clock frequency transitions,	The Accused Products include a second memory, such as the hierarchy of L1, L2 caches that stores an application program, including but not limited to ACPI drivers, power management utilities, APIs provided by AMD, or any software that causes the SMU/SMC firmware to perform P-state transitions.

	Limitation	Contention

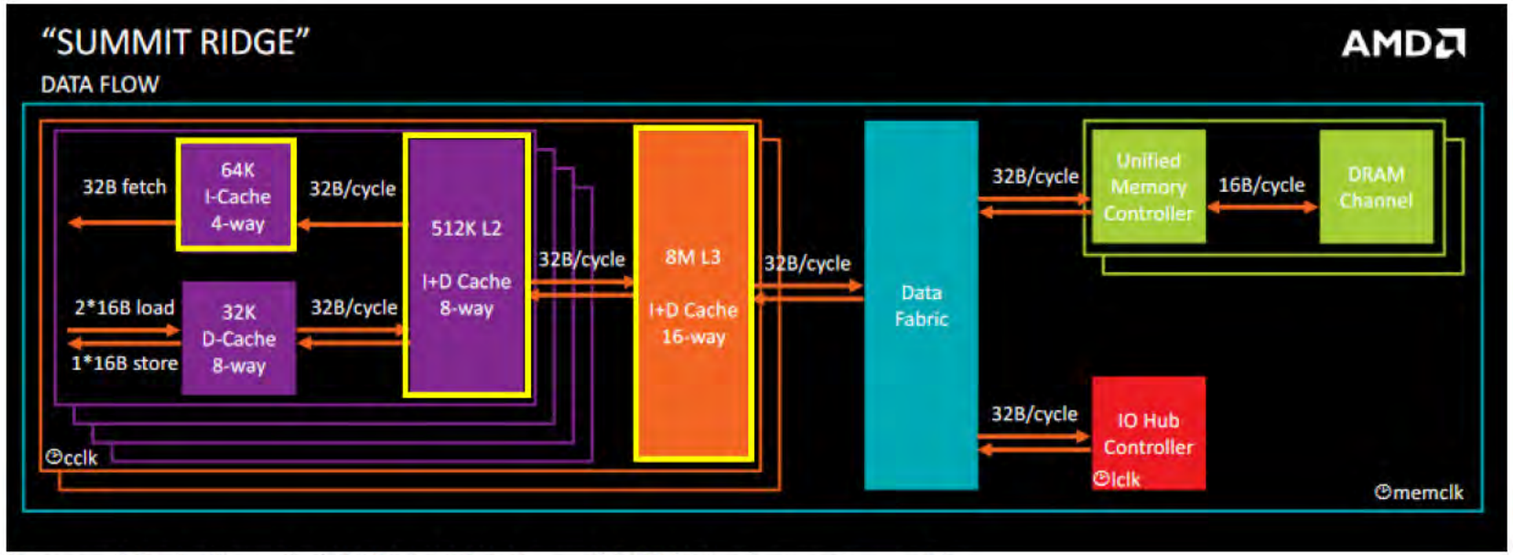
"Zen" Cache hierarchy

- Fast private L2 cache, 12 cycles
- Fast shared L3 cache, 35 cycles
- L3 filled from L2 victims of all four cores
- L2 tags duplicated in L3 for probe filtering and fast cache transfer
- Multiple smart prefetchers
- 50 outstanding misses from L2 to L3 per core
- 96 outstanding misses from L3 to memory



Source: Beck, p.7

	Limitation	Contention



Source: Mitchell et al., GDC18 AMD Ryzen™ CPU Optimization, p.10.

The frequency changes are programmable to enable user-selectable frequency transitions. See e.g., AMD Ryzen Master Overclocking Guide ("OC Guide"), p.11:

> 1. The frequency of processor core clock is determined by a combination of the software-requested p-state and then adjusted by a combination of numerous power and performance optimizing features to attain any of number of fine grain p-states around that software-requested p-state.

See also OC Guide, p.13:

	Limitation	Contention
		3) CPU low power c-states (CC1, CC6, and PC6) and software visible p-states (P1 and P2) remain operational and may be requested by software so that power savings can be achieved. See also OC guide, p.11: 4. Software requested p-state or halt states adjust the level of power to which those internal control mechanisms manage. For example, when software executes a HALT instruction on a processor core, that core will enter the C1 reduced-power state. If that core does not receive an interrupt to resume execution, it will progress to increasingly-lower power states until finally saving the state of the core and being powered off. See also, e.g., 16h BKDG section 2.5.3.1.2; p. 548:

	Limitation	Contention
		2.5.3.1.2 Core P-state Control Core P-states are dynamically controlled by software and are exposed through ACPI objects (refer to 2.5.3.1.8.3 [ACPI Processor P-state Objects]). Software requests a core P-state change by writing a 3 bit index corresponding to the desired P-state number to MSRC001_0062[PstateCmd] of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's MSRC001_0062[PstateCmd]. Boosted P-states may not be directly requested by software. Whenever software requests the P0 state on a processor that supports APM (i.e. writes 000b to MSRC001_0062[PstateCmd]), hardware dynamically places the core into the highest-performance P-state possible as determined by APM. See 2.5.9 [Application Power Management (APM)]. Hardware sequences the frequency and voltage changes necessary to complete a P-state transition as specified by 2.5.3.1.5 [Core P-state Transition Behavior] with no additional software interaction required. Hardware also coordinates frequency and voltage changes when differing P-state requests are made on cores that share a frequency or voltage plane. See 2.5.2 [Frequency and Voltage Domain Dependencies] for details about hardware coordination.

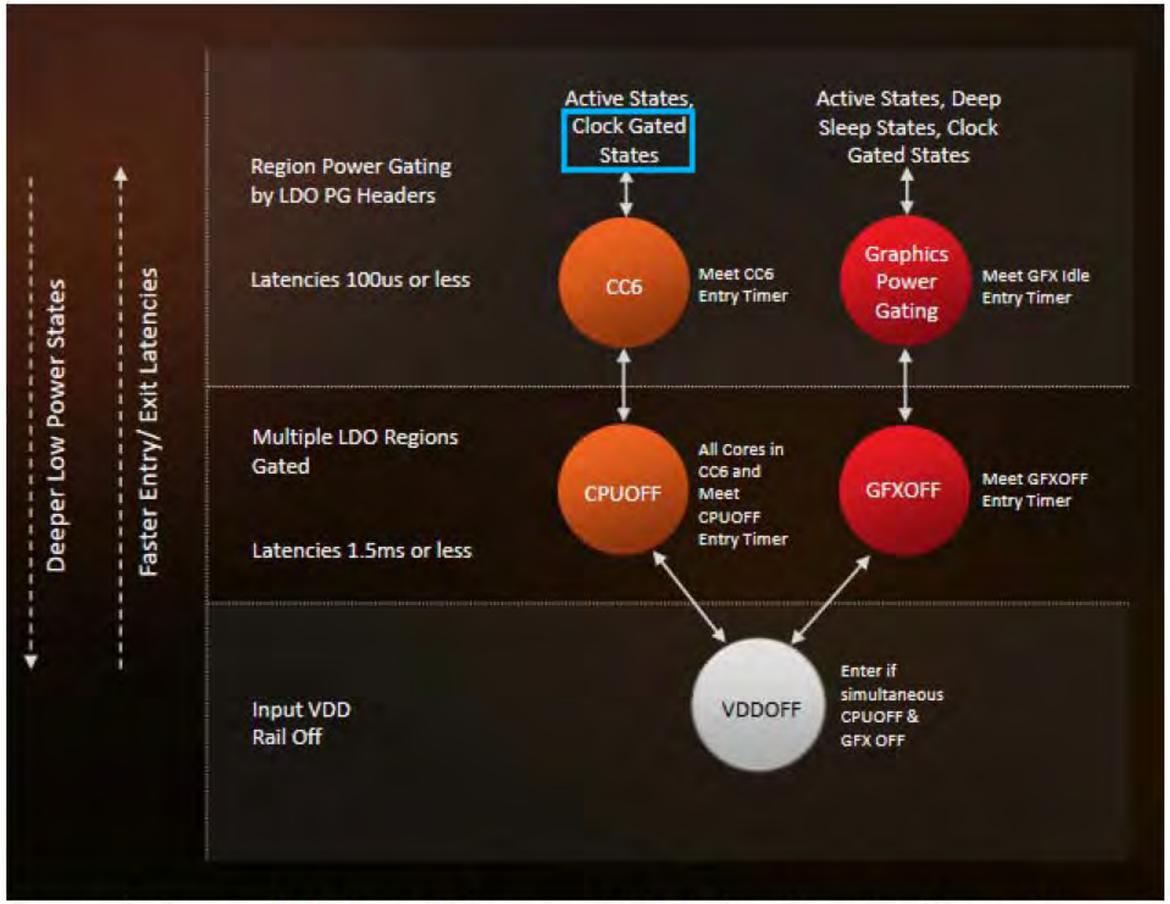
<table>
<tr><th></th><th>Limitation</th><th>Contention</th></tr>
<tr><td></td><td></td><td>MSRC001_0062 P-state Control
<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>63:3</td><td>MBZ.</td></tr>
<tr><td>2:0</td><td>PstateCmd: P-state change command. Read-write; Not-same-for-all. Cold reset value varies by product; after a warm reset, value initializes to the P-state the core was in prior to the reset. Writes to this field cause the core to change to the indicated non-boosted P-state number, specified by MSRC001_00[6B:64]. 0=P0, 1=P1, etc. P-state limits are applied to any P-state requests made through this register. Reads from this field return the last written value, regardless of whether any limits are applied. This field uses software P-state numbering. See 2.5.3 [CPU Power Management] and 2.5.3.1.1.1 [Software P-state Numbering].</td></tr>
</table></td></tr>
<tr><td>1e</td><td>wherein said special modes comprise a first special mode in which clock supply to principal constituents of said central processing unit is halted, a second special mode in which clock supply to an entirety of said central processing unit is halted, and a third special mode in which supply of power to the entirety of said central processing unit is halted.</td><td>The Accused Products include a first special mode in which clock supply to principal constituents of said central processing unit is halted, for example the core C1 (CC1) state:

See OC guide, p.11:

4. Software requested p-state or halt states adjust the level of power to which those internal control mechanisms manage. For example, when software executes a HALT instruction on a processor core, that core will enter the C1 reduced-power state. If that core does not receive an interrupt to resume execution, it will progress to increasingly-lower power states until finally saving the state of the core and being powered off.

See https://www.reddit.com/r/Amd/comments/6w793f/how_to_reduce_idle_clock_speed_on_a_manually/dm6gfkv/</td></tr>
</table>

	Limitation	Contention
		The Ryzen Balanced plan tells Windows to keep a core in p0 for the fastest possible ramp time to max clock. "Keep this core in p0" is **only** true when the core is actively being used. When the core is not being used, our microcode will put the core into core-c1 (cc1) through core-c6 (cc6) sleep states. The cores are so dormant in the CC sleep states that their true clockspeed cannot be probed, though the core's current VID can be. **Zen cores can enter into and out of the CC sleep states up to 1000 times a second, and will spend the majority of their time in a CC sleep state when not under active load**. The effective frequency for a core in this condition is sub-1GHz and sub-1V. Unfortunately there isn't really a tool that can capture this, because the act of probing the core's sleep condition is sufficient load to wake the core and ruin the power savings of the CC state.

	Limitation	Contention
		 Source: Anderson, AMD Ryzen™ Processor With Radeon Vega Graphics, p. 41 See also, e.g., 16h BKDG:

	Limitation	Contention
		2.5.3.2.3.2 Core C1 (CC1) State When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct]. **2.5.3.2.3.2 Core C1 (CC1) State** When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct]. **2.5.3.2.3.3 Core C6 (CC6) State** A core can gate off power to its internal logic when it enters any non-C0 state. This power gated state is known as CC6. In order to enter CC6, hardware first enters CC1 then checks D18F4x118/D18F4x11C[PwrGateEnCstAct]. Power gating reduces the amount of power consumed by the core. VDD voltage is not reduced when a core is in CC6. The following sequence occurs when a core enters the CC6 state: 1. If MSRC001_0071[CurPstate] < D18F3xA8[PopDownPstate], transition the core P-state to D18F3xA8[PopDownPstate]. 2. Internal core state is saved to L1 cache . 3. L1 cache is flushed to L2 cache. See 2.5.3.2.3.1 [C-state Probes and Cache Flushing]. 4. Power is removed from the core and the core PLL/voltage regulator is powered down as specified by D18F5x128[CC6PwrDwnRegEn].

	Limitation	Contention

D18F4x11[C:8] C-state Control

D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states].

- D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr].
- D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1.
- D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2.

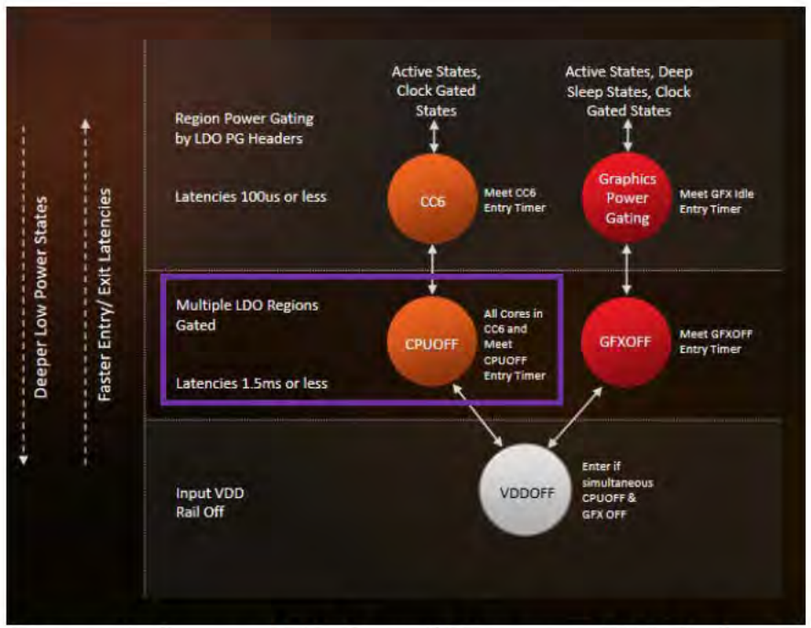
D18F4x118 C-state Control 1

7:5	**ClkDivisorCstAct0: clock divisor**. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or: • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.

Bits	Description	Bits	Description
000b	/1	100b	/16
001b	/2	101b	/128
010b	/4	110b	/512
011b	/8	111b	Turn off clocks.

See CacheFlushTmrSelCstAct0.

	Limitation	Contention
		The Accused Products include a second special mode in which clock supply to an entirety of said central processing unit is halted, for example the package C1 (PC1) state. See e.g., 14h BKDG: **2.5.3.2.3.3 Package C1 (PC1) State** The processor enters the PC1 state with auto-Pmin when all of the following are true: • All cores are in the CC1 state or deeper. If D18F4x1AC[CstPminEn] indicates that auto-Pmin is enabled when the processor enters PC1, the P-state for all cores is transitioned as specified by 2.5.3.2.7.1 [Auto-Pmin]. Regardless of the state of D18F4x1AC[CstPminEn], all core clocks are ramped to the frequency specified by D18F4x1A8[AllHaltCpuDid]. **D18F4x1A8 CPU State Power Management Dynamic Control 0** Reset: 0000_0000h. 9:5 **AllHaltCpuDid**. Read-write. BIOS: 1Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State]. Bits — Divisor 1Ch-00h — Reserved. 1Dh — 128 1Eh — 512 1Fh — Clocks off. See D18F4x1A8[SingleHaltCpuDid].

	Limitation	Contention
		The Accused Products include a third special mode in which supply of power to the entirety of said central processing unit is halted, for example the package C6 (PC6) state: See also OC Guide, p.13: 3) CPU low power c-states (CC1, CC6, and PC6) and software visible p-states (P1 and P2) remain operational and may be requested by software so that power savings can be achieved.  Source: Anderson, AMD Ryzen™ Processor With Radeon Vega Graphics, p. 41

	Limitation	Contention
		See also, e.g., 16h BKDG: **2.5.3.2.3.4 Package C6 (PC6) State** When all cores enter a non-C0 state, VDD can be reduced to a non-operational voltage that does not retain core state. This state is known as PC6 and reduces the amount of static and dynamic power consumed by all cores. The following actions are taken by hardware prior to PC6 entry: 1. If MSRC001_0071[CurPstate] < D18F3xA8[PopDownPstate], transition the core P-state to D18F3xA8[PopDownPstate]. 2. For all cores not in CC6, internal core state is saved to L1 cache . 3. For all cores not in CC6, L1 cache is flushed to L2 cache. See 2.5.3.2.3.1 [C-state Probes and Cache Flushing]. 4. VDD is transitioned to the VID specified by D18F5x128[PC6Vid]. 5. If the core PLLs are not powered down during CC6 entry (see 2.5.3.2.3.3 [Core C6 (CC6) State]), then they are powered down as specified by D18F5x128[PC6PwrDwnRegEn]. **D18F5x128 Clock Power/Timing Control 3** 6:0 **PC6Vid[6:0]: package C6 vid**. Read-write. Cold reset: Product-specific. PC6Vid[7:0] = {PC6Vid[7], PC6Vid[6:0]}. PC6Vid[7:0] specifies the VID driven in the PC6 state. See 2.5.3.2.3.4 [Package C6 (PC6) State] and 2.5.1.3.2 [Low Power Voltages].

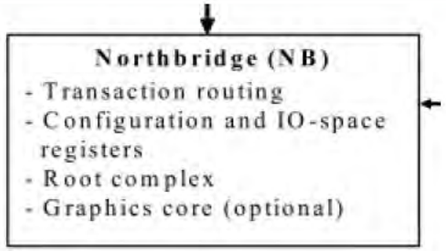
	Limitation	Contention

		2.5.1.3.2 Low Power Voltages
		
		In order to save power, voltages lower than those normally needed for operation may be applied to the VDD power plane while the processor is in a C-state or S-state. The lower voltage is defined as follows:
		
		• PC6Vid: D18F5x128[PC6Vid] specifies a voltage that does not retain the CPU caches or the core microarchitectural state. PC6Vid does not allow execution and is only applied to the cores. See 2.5.3.2.3.4 [Package C6 (PC6) State].
		
		2.5.1.4.1 Hardware-Initiated Voltage Transitions
		
		When software requests any of the following state changes, or hardware determines that any of the following state changes are necessary, hardware coordinates the necessary voltage changes:
		
		• VDD:
		  • Core P-state transition. See 2.5.3.1 [Core P-states].
		  • Package C-state transition. D18F5x128[PC6Vid] specifies a voltage that does not retain the CPU caches or the core microarchitectural state. PC6Vid does not allow execution and is only applied to the cores. See 2.5.3.2.3.4 [Package C6 (PC6) State].
		  • S-state transition. See 2.5.8.1 [S-states].

2p	A system LSI as claimed in claim 1, wherein said clock control library comprises:	
2a	a plurality of libraries that	The clock control libraries of the Accused Products contain a plurality of libraries that control the SMU and clock

	Limitation	Contention
	control said system control circuit and said clock generation circuit to transition the clock frequencies supplied to said central processing unit; and	generator to transition clock frequencies. For example, source code provided by AMD to coreboot indicates that P-state and C-state transitions are controlled by separate libraries: https://github.com/coreboot/coreboot/tree/master/src/vendorcode/amd/agesa/f14/Proc/CPU/Feature
2b	a main library which is called by said application program and selects any one of said libraries in correspondence with the clock frequency supplied to said central processing unit.	As discussed above, P-states and C-states may be controlled by software, which includes a main library that calls upon the plurality of libraries.
3p	A system LSI as claimed in claim 2,	
3a	wherein said main library is described using a same program language as said application program.	The main library in the SMU firmware and the application program instructions stored in the caches are both use the same language such as machine code.
5p	A system LSI as claimed in claim 2,	

	Limitation	Contention
5a	wherein each of said libraries is described using a program language capable of directly controlling said clock generation circuit and said system control circuit.	The SMU firmware directly controls the SMU hardware.
6p	A system LSI as claimed in claim 5,	
6a	wherein each of said libraries is described using an assembler language.	The SMU firmware directly controls the SMU hardware and is described using an assembler language such as machine code.
7p	7. A system LSI as claimed in claim 1, wherein said system control circuit comprises:	
7a	a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit;	The system control circuit of the Accused Products as described above contains a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit. See e.g., 16h BKDG:

	Limitation	Contention
		 BKDG, section 2.12: **2.12 System Management Unit (SMU)** The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details. **2.12.1 Microcontroller** The SMU contains a microcontroller with a 16k ROM and a 16k RAM. Configuration space register mnemonics are defined in section 3.1 of the BKDG: • **DXFYxZZZ**: PCI-defined configuration space; X specifies the hexadecimal device number (this may be 1or 2 digits), Y specifies the function number, and ZZZ specifies the hexidecimal byte address (this may be 2 or 3 digits; e.g., D18F3x40 specifies the register at device 18h, function 3, and address 40h). See 2.7 [Configuration Space], for details about configuration space. the core C1 (CC1) state:

	Limitation	Contention
		2.5.3.2.3.2 Core C1 (CC1) State When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct]. **D18F4x11[C:8] C-state Control** D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states]. • D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]. • D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1. • D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2. **D18F4x118 C-state Control 1**

	Limitation	Contention
		7:5 **ClkDivisorCstAct0: clock divisor**. Read-write. Reset: 0. BIOS: 000b. Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or: • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register. Bits DescriptionBits Description 000b /1 100b /16 001b /2 101b /128 010b /4 110b /512 011b /8 111b Turn off clocks. See CacheFlushTmrSelCstAct0.
7b	a clock halting register that receives the clock from said clock generation circuit and individually sets the clock to be halted or supplied;	the core C1 (CC1) state:

	Limitation	Contention
		2.5.3.2.3.2 Core C1 (CC1) State When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x118/D18F4x11C[ClkDivisorCstAct]. **D18F4x11[C:8] C-state Control** D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states]. • D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]. • D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1. • D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2. **D18F4x118 C-state Control 1**

<table>
<tr><th></th><th>Limitation</th><th>Contention</th></tr>
<tr><td></td><td></td><td>
<table>
<tr><td>7:5</td><td>ClkDivisorCstAct0: clock divisor. Read-write. Reset: 0.
BIOS: 000b.
Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or:
• 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate].
If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.
<table>
<tr><th>Bits</th><th>Description</th><th>Bits</th><th>Description</th></tr>
<tr><td>000b</td><td>/1</td><td>100b</td><td>/16</td></tr>
<tr><td>001b</td><td>/2</td><td>101b</td><td>/128</td></tr>
<tr><td>010b</td><td>/4</td><td>110b</td><td>/512</td></tr>
<tr><td>011b</td><td>/8</td><td>111b</td><td>Turn off clocks.</td></tr>
</table>
See CacheFlushTmrSelCstAct0.</td></tr>
</table>
</td></tr>
<tr><td>7c</td><td>And a status register that judges a state of said central processing unit immediately after being released from said third special mode.</td><td>The Accused Products contain a status register that judges a state of the CPU after waking from PC6. See 14h BKDG:</td></tr>
</table>

	Limitation	Contention
		2.5.3.2.7.2 Exiting PC6 If the PService timer is enabled when the processor exits PC6, all cores transition to the P-state specified by D18F4x1AC[PstateIdCoreOffExit]. The cores remain in this state until one of the following occurs: • The PService timer expires while the package is in C0: In this case, the cores transition back to the last P-state requested by software. • The package enters PC1 without auto-Pmin: In this case, the PService timer continues counting. If it expires while in PC1, the cores remain in the P-state specified by D18F4x1AC[PstateIdCoreOffExit] until they return to C0, at which time they transition to the last P-state requested by software. • The package enters PC1 with auto-Pmin: In this case, the PService timer stops counting and the cores enter the PService state. • The package enters PC6: In this case the PService timer stops counting and the actions associated the requested package C-state occur. See 2.5.3.2.3.4 [Package C6 (PC6) State]. If the PService timer is disabled when the processor exits PC6, the cores transition back to the last P-state requested by software. See also 14h BKDG pp.320-321: **D18F4x1AC CPU State Power Management Dynamic Control 1** 18:16 **PstateIdCoreOffExit**. Read-write. Reset: 0. BIOS: See 2.5.3.2.9. When exiting the package C6 state, the core transitions to the P-state specified by this register. See 2.5.3.2.7.2 [Exiting PC6]. If PC6 is enabled (see 2.5.3.2.9 [BIOS Requirements for C-state Initialization]), PstateIdCoreOffExit must be programmed to the lowest-performance P-state displayed to the operating system or to any lower-performance P-state. This P-state must have a core clock frequency of at least 400 MHz. Programming this field to 0 causes the core to transition to the last P-state requested by software when exiting package C6. This field uses hardware P-state numbering. See 2.5.3.1.2.2 [Hardware P-state Numbering].

	Limitation	Contention
10p	A system LSI as claimed in claim 1,	
10a	wherein said first memory and said second memory are two independent memories which are separated from each other.	As detailed above, the first memory in the SMU and the second memory in the caches are independent memories that are separated from each other.

Exhibit B.5: Preliminary Infringement Claim Chart for U.S. Patent 6,895,519

Accused Products: AMD Family 12h Products

These preliminary infringement contentions were prepared without the benefit of the Court's claim construction or the parties' exchange of constructions. As of the date of these contentions, AMD has not produced any information concerning the Accused Products. Thus, this chart is based on publicly available evidence, and based upon information and reasonable belief in light of such evidence. As such, Aquila reserves the right to amend or supplement its contentions to address any issues arising from the Court's constructions or to account for new information that becomes available.

	Limitation	Contention
1p	A system LSI having a plurality of ordinary operation modes and a plurality of special modes in response to clock frequencies supplied to a central processing unit, comprising:	To the extent that the preamble is limiting, Aquila contends that it is met. For example, each product in the 12h Accused Product Family ("Accused Product") is a system LSI. The Accused Product has a plurality of ordinary operation modes, for example the Core P-states. *See* BIOS and Kernel Developer's Guide for AMD Family 12h Models 00h-0Fh Processors ("BKDG"), §2.5.3.1:

	Limitation	Contention
		2.5.3.1 Core P-states Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states, specified in MSRC001_00[6B:64]. Out of reset, the voltage and frequency of the cores is specified by MSRC001_0071[StartupPstate]. Support for dynamic core P-state changes is indicated by more than one enabled selection in MSRC001_00[6B:64][PstateEn]. All FID and DID parameters for equivalent P-states must be programmed to equivalent values for all cores. For examples, P0 on core0 must have the same FID and DID values as P0 on core1, P1 on core0 must have the same FID and DID values as P1 on core1, and so on. Refer to MSRC001_00[6B:64] for further details on programming requirements. The COF for core P-states is a function of the FID and the DID. See MSRC001_00[6B:64][CpuFid, CpuDid] for more details. Software requests core P-state changes for each core independently using the hardware P-state control mechanism (a.k.a. fire and forget). Support for hardware P-state control is indicated by CPUID Fn8000_0007_EDX[HwPstate]=1b. P-state transitions using the hardware P-state control mechanism are not allowed until the P-state initialization requirements defined in 2.5.3.1.7 [BIOS Requirements for Core P-State Initialization and Transitions] are complete. BKDG at p.47:

	Limitation	Contention

Table 5: Software P-state numbering example

D18F4x15C[NumBoostStates]=1		D18F4x15C[NumBoostStates]=3	
P-state Name	**MSR Address**	**P-state Name**	**MSR Address**
Pb0	MSRC001_0064	Pb0	MSRC001_0064
P0	MSRC001_0065	Pb1	MSRC001_0065
P1	MSRC001_0066	Pb2	MSRC001_0066
P2	MSRC001_0067	P0	MSRC001_0067
P3	MSRC001_0068	P1	MSRC001_0068
P4	MSRC001_0069	P2	MSRC001_0069
P5	MSRC001_006A	P3	MSRC001_006A
P6	MSRC001_006B	P4	MSRC001_006B

All sections and register definitions use software P-state numbering unless otherwise specified.

The Accused Product Family has a plurality of special modes, for example, the Core C-states or deep sleep modes such as ACPI S3 or connected standby S0i3. *See* BKDG, §§ 2.5.3.2, 2.5.3.2.1, 2.5:

	Limitation	Contention
		2.5.3.2 C-states C-states are processor power states. C0 is the operational state in which instructions are executed. All other C-states are low-power states in which instructions are not executed. **2.5.3.2.1 C-state Names and Numbers** C-states are often referred to by an alphanumeric naming convention, C1, C2, C3, etc. The mapping between ACPI defined C-states and AMD specified C-state actions is not direct. The actions taken by the processor when entering a low-power C-state are specified by D18F4x118 and D18F4x11C and are configured by software. See 2.5.3.2.3 [C-state Actions] for information about AMD specific actions.

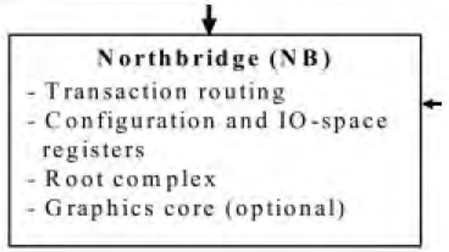
	Limitation	Contention
		2.5 Power Management The processor supports many power management features in a variety of systems. Table 4 provides a summary of ACPI states and power management features and indicates whether they are supported. **Table 4: Power management support**

ACPI/Power Management State	Supported	Description
G0/S0/C0: Working	Yes	
G0/S0/C0: Core P-state transitions	Yes	2.5.3.1 [Core P-states]
G0/S0/C0: NB P-state transitions	Yes	2.5.4.2 [NB Clock Ramping]
G0/S0/C0: Hardware thermal control (HTC)	Yes	2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)]
G0/S0/C0: Software thermal control (STC)	No	
G0/S0/C0: Thermal clock throttling (SMC controlled)	No	
G0/S0: Low power C-states	Yes	2.5.3.2 [C-states] and 2.5.1.4.2 [Alternate Low Power Voltages]
G1/S1: Stand By (Powered On Suspend)	No	

<table>
<tr><th></th><th>Limitation</th><th>Contention</th></tr>
<tr><td></td><td></td><td>
Table 4: Power management support
<table>
<tr><th>ACPI/Power Management State</th><th>Supported</th><th>Description</th></tr>
<tr><td>G1/S3: Stand By (Suspend to RAM)</td><td>Yes</td><td>2.5.7.1.1 [ACPI Suspend to RAM State (S3)]</td></tr>
<tr><td>G1/S4, S5: Hibernate (Suspend to Disk), Shut Down (Soft Off)</td><td>Yes</td><td></td></tr>
<tr><td>G3 Mechanical Off</td><td>Yes</td><td></td></tr>
<tr><td>Parallel VID Interface</td><td>No</td><td rowspan="3">2.5.1 [Processor Power Planes And Voltage Control]</td></tr>
<tr><td>Serial VID Interface</td><td>Yes</td></tr>
<tr><td>Dual-plane systems</td><td>Yes</td></tr>
</table>

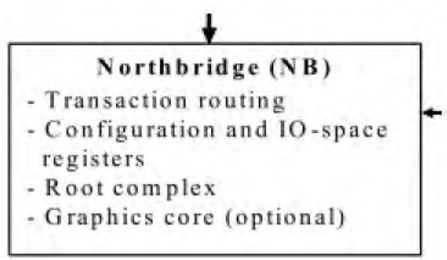
Furthermore, the Core P-states and Core C-states are in response to clock frequencies supplied to a central processing unit. For example, the core P-states are “characterized” by “core frequency;” core P-state changes are further requested by software. See e.g., BKDG, § 2.5.3.1, 2.5.3.1.3.

Similarly, C-states are “dynamically requested by software” and also dependent upon clock frequency. See BKDG §§ 2.5.3.2.2, 2.5.3.2.3.1, 2.5.3.2.3.2, p.343.
</td></tr>
<tr><td>1a</td><td>a first memory that stores a clock control library for controlling a clock frequency transition between said ordinary operation modes;</td><td>The Accused Products include a first memory that stores a clock control library. For example, the SMU contains memory that stores the firmware and configuration space registers, including a clock control library. The clock control library controls clock frequency transition between the P-states. See e.g., BKDG, Fig. 1:</td></tr>
</table>

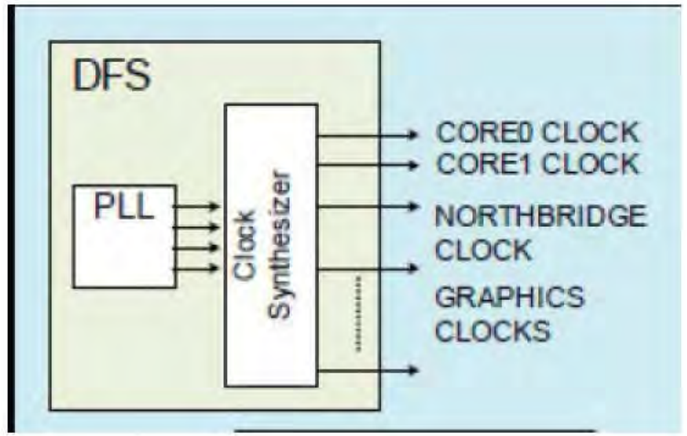
	Limitation	Contention
		 BKDG, section 2.12: **2.12 System Management Unit (SMU)** The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details. **2.12.1 Microcontroller** The SMU contains a microcontroller with a 16k ROM and a 16k RAM. See also BKDG, Table 10:

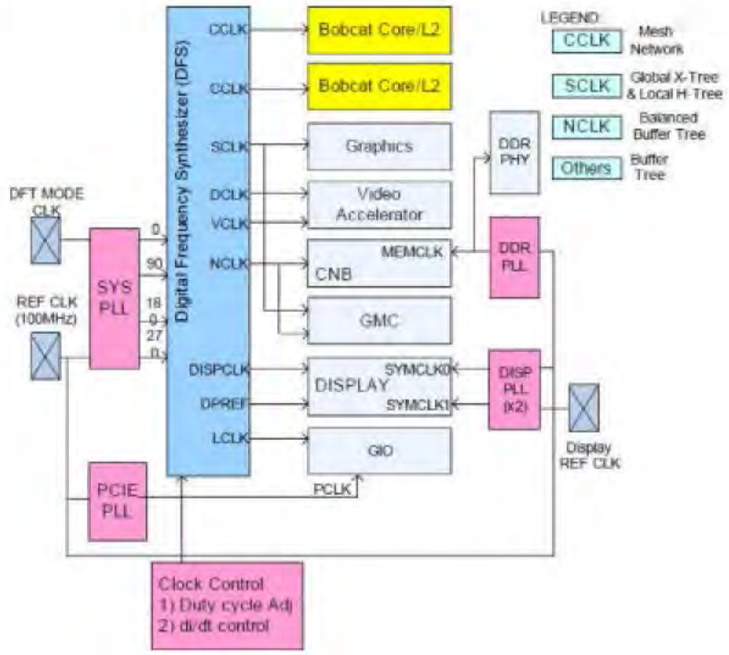
	Limitation	Contention
		Table 6: P-state control example D18F4x15C[NumBoostStates]=1 / D18F4x15C[NumBoostStates]=3

P-state Name	Index Used for Requests/Status	Corresponding MSR Address	P-state Name	Index Used for Requests/Status	Corresponding MSR Address
Pb0	n/a	MSRC001_0064	Pb0	n/a	MSRC001_0064
P0	0	MSRC001_0065	Pb1	n/a	MSRC001_0065
P1	1	MSRC001_0066	Pb2	n/a	MSRC001_0066
P2	2	MSRC001_0067	P0	0	MSRC001_0067
P3	3	MSRC001_0068	P1	1	MSRC001_0068
P4	4	MSRC001_0069	P2	2	MSRC001_0069
P5	5	MSRC001_006A	P3	3	MSRC001_006A
P6	6	MSRC001_006B	P4	4	MSRC001_006B

1b	a system control circuit which has a register, wherein said system control circuit carries out the clock frequency transition between said ordinary operation modes and said special modes in response to a change of a value in said register, and also carries out the clock	The Accused Product has a system control circuit, for example, the System Management Unit and/or the System Management Controller, that has a register. See e.g., BKDG: 

	Limitation	Contention
	frequency transition among said ordinary operation modes in response to said clock control library;	BKDG, section 2.12: **2.12 System Management Unit (SMU)** The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details. **2.12.1 Microcontroller** The SMU contains a microcontroller with a 16k ROM and a 16k RAM. The NB/SMU controls the clock frequency transitions between the core P-states. See e.g., SATHE et al.: RESONANT-CLOCK DESIGN FOR A POWER-EFFICIENT, HIGH-VOLUME X86-64 MICROPROCESSOR, p.144 tion of the configuration programming interface. On receiving notification from the NB of a PState transition, the core implements a PState entry sequence which transitions the core into a clock-gated state. A program sequencer then accesses a
1c	a clock generation circuit that receives a plurality of standard clocks, wherein said clock generation circuit generates a clock supplied to said central processing unit according to control by said system control circuit; and	The Accused Products include a digital frequency synthesizer clock generation circuit, including the core PLL, clock multipliers and dividers, and/or the digital frequency synthesizer. The DFS receives a plurality of standard clocks, for example, different phases of the PLL clock or reference clock, and outputs the core clock such as CCLK to the CPU. The Accused Products operate similarly to other product families with regards to this limitation. The clock generator circuit includes at least the PLL and the digital frequency synthesizer. The DFS receives a plurality of standard clocks (the 4 phases-offset references provided by the PLL), and generates CCLK according to control by the SMU:

	Limitation	Contention
		

	Limitation	Contention
		 Fig. 11. DFS clock generation Source: Foley et al., A Low-Power Integrated x86-64 And Graphics Processor For Mobile Computing Devices, Fig. 1., 11; p.224-225.
1d	a second memory that stores an application program, wherein calling of said clock control library	The Accused Products include a second memory, such as the hierarchy of L1, L2 caches that stores an application program, including but not limited to ACPI drivers, power management utilities, APIs provided by AMD, or any software that causes the SMU/SMC firmware to perform P-state transitions. See BKDG section 2.5.3.1.3; p. 429:

	Limitation	Contention
	and changing of said register value are programmably controlled by said application program to enable user selectable clock frequency transitions,	**2.5.3.1.3 Core P-state Control** Core P-states are dynamically controlled by software and are exposed through ACPI objects (see 2.5.3.1.9 [ACPI Processor P-State Objects]). Software requests a core P-state change by writing a 3 bit index corresponding to the desired non-boosted P-state number to MSRC001_0062 [P-State Control] of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's MSRC001_0062[PstateCmd]. Boosted P-states may not be directly requested by software. Whenever software requests the P0 state (i.e. when software writes 000b to MSRC001_0062[PstateCmd]) on a processor that supports CPB, hardware dynamically places that core into the highest-performance P-state possible as determined by CPB. See 2.5.3.1.1 [Core Performance Boost (CPB)]. Hardware sequences the frequency and voltage changes necessary to complete a P-state transition as specified by 2.5.3.1.6 [Core P-state Transition Behavior] with no additional software interaction required. Hardware also coordinates frequency and voltage changes when differing P-state requests are made on cores that share a frequency or voltage plane. See 2.5.2 [Frequency and Voltage Domain Dependencies] for details about hardware coordination. **MSRC001_0062 P-State Control Register** Bits | Description 63:3 | MBZ. 2:0 | **PstateCmd: P-state change command**. Read-write. Reset: Product-specific. Writes to this field cause the core to change to the indicated non-boosted P-state number, specified by MSRC001_00[6B:64]. 0=SWP0, 1=SWP1, etc. P-state limits are applied to any P-state requests made through this register. See 2.5.3.1 [Core P-states] and 2.5.3.1.2.1 [Software P-state Numbering]. Reads from this field return the last written value, regardless of whether any limits are applied.

	Limitation	Contention
1e	wherein said special modes comprise a first special mode in which clock supply to principal constituents of said central processing unit is halted, a second special mode in which clock supply to an entirety of said central processing unit is halted, and a third special mode in which supply of power to the entirety of said central processing unit is halted.	The Accused Products include a first special mode in which clock supply to principal constituents of said central processing unit is halted, for example the core C6 (CC6) state: **2.5.3.2.3.2 Core C6 (CC6) State** When a core enters the CC6 state, it executes the following sequence: 1. L1 and L2 caches are flushed to DRAM by hardware. 2. Internal core state is saved to DRAM by hardware. 3. The core clock ramps down to the frequency specified by D18F4x1AC[C6Did]. 4. Power is removed from the core if possible as specified by D18F4x1AC[CoreC6Cap] and D18F4x1AC[CoreC6Dis]. The events which cause a core to exit the CC6 state are specified in 2.5.3.2.6 [Exiting C-states]. If a warm reset occurs while a core is in CC6, all MCA registers in the core shown in Table 41 are cleared to 0. See 2.16 [Machine Check Architecture]. **D18F4x1AC CPU State Power Management Dynamic Control 1**

	Limitation	Contention

9:5	**C6Did: CC6 divisor**. Read-write. Reset: 0. BIOS: 0Fh. Specifies the divisor applied to the core when ramping clocks down for CC6. See 2.5.3.2.3.2 [Core C6 (CC6) State].

Bits	Divisor	Bits	Divisor
00h	Reserved	09h	Reserved
01h	Reserved	0Ah	Reserved
02h	Reserved	0Bh	Reserved
03h	Reserved	0Ch	/128
04h	Reserved	0Dh	/512
05h	Reserved	0Eh	Reserved
06h	Reserved	0Fh	Clocks off
07h	Reserved	1Fh-10h	Reserved
08h	Reserved		

See D18F4x1A8[SingleHaltCpuDid].

The Accused Products include a second special mode in which clock supply to an entirety of said central processing unit is halted, for example the package C1 (PC1) state:

2.5.3.2.3.3 Package C1 (PC1) State

The processor enters the PC1 state with auto-Pmin when all of the following are true:

- All cores are in the CC1 state or deeper.

If D18F4x1AC[CstPminEn] indicates that auto-Pmin is enabled when the processor enters PC1, the P-state for all cores is transitioned as specified by 2.5.3.2.7.1 [Auto-Pmin]. Regardless of the state of D18F4x1AC[CstPminEn], all core clocks are ramped to the frequency specified by D18F4x1A8[AllHaltCpuDid].

	Limitation	Contention

D18F4x1A8 CPU State Power Management Dynamic Control 0

Reset: 0000_0000h.

9:5	**AllHaltCpuDid**. Read-write. BIOS: 0Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State]. This field must be set to a divisor deeper than D18F4x1A8[SingleHaltCpuDid] or undefined behavior may result.

Bits	Divisor	Bits	Divisor
00h	Reserved	09h	Reserved
01h	Reserved	0Ah	Reserved
02h	Reserved	0Bh	Reserved
03h	Reserved	0Ch	/128
04h	Reserved	0Dh	/512
05h	Reserved	0Eh	Reserved
06h	Reserved	0Fh	Clocks off
07h	Reserved	1Fh-10h	Reserved
08h	Reserved		

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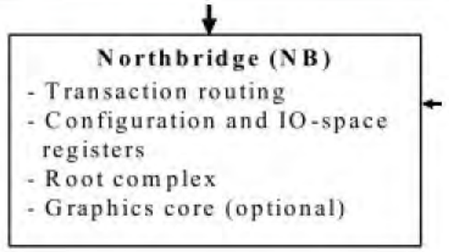
The Accused Products include a third special mode in which supply of power to the entirety of said central processing unit is halted, for example the package C6 (PC6) state:

	Limitation	Contention
		2.5.3.2.3.4 Package C6 (PC6) State The processor enters the PC6 state when all of the following are true: • All cores enter the CC6 state. • The C-state action field targeted by each core's C-state request has the C6Enable bit programmed to indicated entry into PC6 is allowed. See D18F4x118 and D18F4x11C. • PC6 is supported and enabled as specified by D18F4x1AC[PkgC6Cap] and D18F4x1AC[PkgC6Dis]. When the package enters PC6, VDDCR_CPU is transitioned to the VID specified by D18F3x128[C6Vid]. **2.5.1.4.2 Alternate Low Power Voltages** In order to save power, voltages lower than those normally used may be applied to the VDDCR_CPU power plane while the processor is in a C-state. D18F3x128[C6Vid] specifies a VDDCR_CPU voltage that does not retain the CPU caches or the cores' microarchitectural state, nor allows for execution. As a result, hardware flushes caches and saves the cores' microarchitectural state to DRAM before transitioning to C6Vid. See 2.5.3.2.3.4 [Package C6 (PC6) State]. **2.5.1.4.3 Power Gating** The processor can remove power from an individual core. This is referred to as power gating. Gating power to a subcomponent causes its internal microarchitectural state and, if applicable, any data in its caches to be lost. When entering a power gated state, hardware saves any needed data, either internally or to DRAM, and flushes caches. When exiting a power gated state, hardware performs any required resets and restores any needed data. See 2.5.3.2.3.2 [Core C6 (CC6) State].

	Limitation	Contention
2p	A system LSI as claimed in claim 1, wherein said clock control library comprises:	
2a	a plurality of libraries that control said system control circuit and said clock generation circuit to transition the clock frequencies supplied to said central processing unit; and	The clock control libraries of the Accused Products contain a plurality of libraries that control the SMU and clock generator to transition clock frequencies. For example, source code provided by AMD to coreboot indicates that P-state and C-state transitions are controlled by separate libraries: https://github.com/coreboot/coreboot/tree/master/src/vendorcode/amd/agesa/f14/Proc/CPU/Feature
2b	a main library which is called by said application program and selects any one of said libraries in correspondence with the clock frequency supplied to said central processing unit.	As discussed above, P-states and C-states may be controlled by software, which includes a main library that calls upon the plurality of libraries.
3p	A system LSI as claimed in claim 2,	
3a	wherein said main library is described using a same program language as said application program.	The main library in the SMU firmware and the application program instructions stored in the caches are both use the same language such as machine code.

	Limitation	Contention
5p	A system LSI as claimed in claim 2,	
5a	wherein each of said libraries is described using a program language capable of directly controlling said clock generation circuit and said system control circuit.	The SMU firmware directly controls the SMU hardware.
6p	A system LSI as claimed in claim 5,	
6a	wherein each of said libraries is described using an assembler language.	The SMU firmware directly controls the SMU hardware and is described using an assembler language such as machine code.
7p	7. A system LSI as claimed in claim 1, wherein said system control circuit comprises:	
7a	a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit;	The NB of the Accused Products contains a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit. The NB contains the configuration register space for the Accused Products. See e.g., BKDG:

	Limitation	Contention
		 BKDG, section 2.12: **2.12 System Management Unit (SMU)** The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. Several internal registers are used to control various tasks. See 3.17 [GPU Memory Mapped Registers] for registers descriptions and details. **2.12.1 Microcontroller** The SMU contains a microcontroller with a 16k ROM and a 16k RAM. Configuration space register mnemonics are defined in section 3.1 of the BKDG: • **DZFYxXXX**: PCI-defined configuration space; XXX specifies the hexadecimal byte address of the configuration register (this may be 2 or 3 digits); Y specifies the function number; Z defined the device number; e.g., D0F3x40 specifies the register of device 0 at function 3, address 40. See 2.7 [Configuration Space], for details about configuration space. the core C1 (CC1) state:

	Limitation	Contention

2.5.3.2.3.1 Core C1 (CC1) State

When a core enters the CC1 state, its clock ramps down to the frequency specified by D18F4x1A8[Single-HaltCpuDid].

D18F4x1A8 CPU State Power Management Dynamic Control 0

Reset: 0000_0000h.

4:0	**SingleHaltCpuDid**. Read-write. BIOS: 1Eh. On a processor with multiple cores, this specifies the divisor used when ramping core clocks down after a single core has entered the clocks ramped state.

Bits	Divisor
1Ch-00h	Reserved.
1Dh	128
1Eh	512
1Fh	Clocks off.

- If MSRC001_00[6B:64][CpuDidMSD] of the current P-state is greater than or equal to Single-HaltCpuDid, then no frequency change is made when entering the low-power state associated with this register.
- The COF = (the frequency specified by D18F3xD4[MainPllOpFreqId]) / (the divisor specified by this field).

	Limitation	Contention

2.5.3.2.3.3 Package C1 (PC1) State

The processor enters the PC1 state with auto-Pmin when all of the following are true:

- All cores are in the CC1 state or deeper.

If D18F4x1AC[CstPminEn] indicates that auto-Pmin is enabled when the processor enters PC1, the P-state for all cores is transitioned as specified by 2.5.3.2.7.1 [Auto-Pmin]. Regardless of the state of D18F4x1AC[CstPminEn], all core clocks are ramped to the frequency specified by D18F4x1A8[AllHaltCpuDid].

D18F4x1A8 CPU State Power Management Dynamic Control 0

Reset: 0000_0000h.

9:5	**AllHaltCpuDid**. Read-write. BIOS: 1Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State]. Bits — Divisor 1Ch-00h — Reserved. 1Dh — 128 1Eh — 512 1Fh — Clocks off. See D18F4x1A8[SingleHaltCpuDid].

	Limitation	Contention
7b	a clock halting register that receives the clock from said clock generation circuit and individually sets the clock to be halted or supplied;	**2.5.3.2.3.3 Package C1 (PC1) State** The processor enters the PC1 state with auto-Pmin when all of the following are true: • All cores are in the CC1 state or deeper. If D18F4x1AC[CstPminEn] indicates that auto-Pmin is enabled when the processor enters PC1, the P-state for all cores is transitioned as specified by 2.5.3.2.7.1 [Auto-Pmin]. Regardless of the state of D18F4x1AC[CstPminEn], all core clocks are ramped to the frequency specified by D18F4x1A8[AllHaltCpuDid]. **D18F4x1A8 CPU State Power Management Dynamic Control 0** Reset: 0000_0000h. 9:5 **AllHaltCpuDid**. Read-write. BIOS: 0Fh. Specifies the divisor used when entering PC1 with or without auto-Pmin. See 2.5.3.2.3.3 [Package C1 (PC1) State]. This field must be set to a divisor deeper than D18F4x1A8[SingleHaltCpuDid] or undefined behavior may result. Bits Divisor Bits Divisor 00h Reserved 09h Reserved 01h Reserved 0Ah Reserved 02h Reserved 0Bh Reserved 03h Reserved 0Ch /128 04h Reserved 0Dh /512 05h Reserved 0Eh Reserved 06h Reserved 0Fh Clocks off 07h Reserved 1Fh-10h Reserved 08h Reserved 2/13/2019

	Limitation	Contention
7c	And a status register that judges a state of said central processing unit immediately after being released from said third special mode.	**2.5.3.2.7.2 Exiting PC6** If the PService timer is enabled when the processor exits PC6, all cores transition to the P-state specified by D18F4x1AC[PstateIdCoreOffExit]. The cores remain in this state until one of the following occurs: • The PService timer expires while the package is in C0: In this case, the cores transition back to the last P-state requested by software. • The package enters PC1 without auto-Pmin: In this case, the PService timer continues counting. If it expires while in PC1, the cores remain in the P-state specified by D18F4x1AC[PstateIdCoreOffExit] until they return to C0, at which time they transition to the last P-state requested by software. • The package enters PC1 with auto-Pmin: In this case, the PService timer stops counting and the cores enter the PService state. • The package enters PC6: In this case the PService timer stops counting and the actions associated the requested package C-state occur. See 2.5.3.2.3.4 [Package C6 (PC6) State]. If the PService timer is disabled when the processor exits PC6, the cores transition back to the last P-state requested by software. See also BKDG pp.320-321: **D18F4x1AC CPU State Power Management Dynamic Control 1**

	Limitation	Contention
		18:16 **PstateIdCoreOffExit**. Read-write. Reset: 0. BIOS: 2.5.3.2.9. When exiting the package C6 state, the core transitions to the P-state specified by this register. See 2.5.3.2.7.2 [Exiting PC6]. If PC6 is enabled (see 2.5.3.2.9 [BIOS Requirements for C-state Initialization]), PstateIdCoreOffExit must be programmed to lowest-performance P-state displayed to the operating system or to any lower-performance P-state. Programming this field to 0 causes the core to transition to the last P-state requested by software when exiting package C6. This field uses hardware P-state numbering. See 2.5.3.1.2.2 [Hardware P-state Numbering].
10p	A system LSI as claimed in claim 1,	
10a	wherein said first memory and said second memory are two independent memories which are separated from each other.	As detailed above, the first memory in the SMU and the second memory in the caches are independent memories that are separated from each other.

Exhibit C.1 – Preliminary Accused Product Identification for '614 Patent – AMD Family 12h Processors

This identification of products is based on information reasonably available to Polaris, and was prepared without the benefit of discovery from AMD. Accordingly, this chart may not include non-public AMD products such as OEM or custom products. Aquila reserves the right to modify or supplement its identification of Accused Products when AMD provides more information.

Model	Family	Line	uArch
641	AMD Athlon Processors	AMD Athlon II X4	Llano
638	AMD Athlon Processors	AMD Athlon II X4	Llano
631	AMD Athlon Processors	AMD Athlon II X4	Llano
631	AMD Athlon Processors	AMD Athlon II X4	Llano
620e	AMD Athlon Processors	AMD Athlon II X4	Llano
E2-3000M	AMD E-Series Processors		Llano
A4-3300M	AMD A-Series Processors		Llano
A4-3305M	AMD A-Series Processors		Llano
A4-3310MX	AMD A-Series Processors		Llano
A4-3320M	AMD A-Series Processors		Llano
A4-3330MX	AMD A-Series Processors		Llano
A6-3400M	AMD A-Series Processors		Llano
A6-3410MX	AMD A-Series Processors		Llano
A6-3420M	AMD A-Series Processors		Llano
A6-3430MX	AMD A-Series Processors		Llano
A8-3500M	AMD A-Series Processors		Llano
A8-3510MX	AMD A-Series Processors		Llano
A8-3520M	AMD A-Series Processors		Llano
A8-3530MX	AMD A-Series Processors		Llano
A8-3550MX	AMD A-Series Processors		Llano
Sempron X2 198	AMD Sempron Processors		Llano
Athlon II X2 221	AMD Athlon Processors		Llano
Athlon II X4 651	AMD Athlon Processors		Llano
Athlon II X4 651K	AMD Athlon Processors		Llano
E2-3200	AMD E-Series Processors		Llano
A4-3300	AMD A-Series Processors		Llano
A4-3400	AMD A-Series Processors		Llano
A4-3420	AMD A-Series Processors		Llano

Model	Family	Line	uArch
A6-3500	AMD A-Series Processors		Llano
A6-3600	AMD A-Series Processors		Llano
A6-3620	AMD A-Series Processors		Llano
A6-3650	AMD A-Series Processors		Llano
A6-3670K	AMD A-Series Processors		Llano
A8-3800	AMD A-Series Processors		Llano
A8-3820	AMD A-Series Processors		Llano
A8-3850	AMD A-Series Processors		Llano
A8-3870K	AMD A-Series Processors		Llano

Exhibit C.2 – Preliminary Accused Product Identification for '614 Patent – AMD Bulldozer/Piledriver Processors

This identification of products is based on information reasonably available to Polaris, and was prepared without the benefit of discovery from AMD. Accordingly, this chart may not include non-public AMD products such as OEM or custom products. Aquila reserves the right to modify or supplement its identification of Accused Products when AMD provides more information.

Model	Family	Line	uArch
A10-6800B with Radeon HD 8670D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6800K with Radeon HD 8670D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6790K with Radeon HD 8670D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6790B	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6700 with Radeon HD 8670D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6700T with Radeon HD 8650D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-5800K	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-5700	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A8-6600K with Radeon HD 8570D	AMD A-Series Processors	AMD A8-Series APU for Desktops	Piledriver
A8-6500B	AMD A-Series Processors	AMD A8-Series APU for Desktops	Piledriver
A8-6500 with Radeon HD 8570D	AMD A-Series Processors	AMD A8-Series APU for Desktops	Piledriver
A8-6500T with Radeon HD 8550D	AMD A-Series Processors	AMD A8-Series APU for Desktops	Piledriver
A6-6420K with Radeon HD 8470D	AMD A-Series Processors	AMD A6-Series APU for Desktops	Piledriver
A6-6400K with Radeon HD 8470D	AMD A-Series Processors	AMD A6-Series APU for Desktops	Piledriver
A6-5400K	AMD A-Series Processors	AMD A6-Series APU for Desktops	Piledriver
A4-7300 with Radeon HD 8470D	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-6320B	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver

Model	Family	Line	uArch
A4-6320 with Radeon HD 8370D	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-6300	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-6300B	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-6300 with Radeon HD 8370D	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
FX-9590	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-9370	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8370 with Wraith cooler	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8370E	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8370	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8350 with Wraith cooler	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8350	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8320E	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8320	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8310	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8300	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8170	AMD FX-Series Processors		Bulldozer
FX-8150	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Bulldozer
FX-8140	AMD FX-Series Processors		Bulldozer
FX-8120	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Bulldozer
FX-8100	AMD FX-Series Processors		Bulldozer
FX-6350 with Wraith cooler	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Piledriver

Model	Family	Line	uArch
A4-4020	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-4000	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A8-7200P with Radeon R5 Graphics	AMD A-Series Processors	AMD A8-Series APU for Laptops	Piledriver
FX-6350	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Piledriver
FX-6300	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Piledriver
FX-6200	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Bulldozer
FX-6130	AMD FX-Series Processors		Bulldozer
FX-6120	AMD FX-Series Processors		Bulldozer
FX 6100	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Bulldozer
FX-4350	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Piledriver
FX-4320	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Piledriver
FX-4300	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Piledriver
FX-4170	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Bulldozer
FX-4150	AMD FX-Series Processors		Bulldozer
FX-4130	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Bulldozer
FX-4120	AMD FX-Series Processors		Bulldozer
FX-4100	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Bulldozer
A6-5350M with Radeon HD 8450G	AMD A-Series Processors	AMD A6-Series APU for Laptops	Piledriver
A10-6800B with Radeon HD 8670D	AMD A-Series Processors	AMD Business Class - Quad-Core A10-Series APU for Desktops	Piledriver
A10-6790B with Radeon HD 8670D	AMD A-Series Processors	AMD Business Class - Quad-Core A10-Series APU for Desktops	Piledriver

Model	Family	Line	uArch
A8-6500B with Radeon HD 8570D	AMD A-Series Processors	AMD Business Class - Quad-Core A8-Series APU for Desktops	Piledriver
760K	AMD Athlon Processors	AMD Athlon X4	Piledriver
750	AMD Athlon Processors	AMD Athlon X4	Piledriver
A6-6420B with Radeon HD 8470D	AMD A-Series Processors	AMD Business Class - Dual-Core A6-Series APU for Desktops	Piledriver
750K	AMD Athlon Processors	AMD Athlon X4	Piledriver
A6-6400B with Radeon HD 8470D	AMD A-Series Processors	AMD Business Class - Dual-Core A6-Series APU for Desktops	Piledriver
740	AMD Athlon Processors	AMD Athlon X4	Piledriver
6386 SE	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6380	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6378	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6376	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6370P	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6366 HE	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6348	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
A4 PRO-7300B with Radeon HD 8470D	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Desktops	Piledriver
6344	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6338P	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6328	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6320	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6308	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver

Model	Family	Line	uArch
6287 SE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6284 SE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6282 SE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6278	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6276	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6274	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6272	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6262 HE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6230 HE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6238	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6234	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6220	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6212	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6204	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
4386	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
43GK HE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4376 HE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4365	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4340	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4334	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4332 HE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
43CX EE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver

Model	Family	Line	uArch
4310 EE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4284	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4280	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4276 HE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4274 HE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
42MX EE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4256 EE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4240	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4238	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4234	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4230 HE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4228 HE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4226	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
42DX EE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
3380	AMD Opteron	AMD Opteron 3300 Series Processor	Piledriver
3365	AMD Opteron	AMD Opteron 3300 Series Processor	Piledriver
3350 HE	AMD Opteron	AMD Opteron 3300 Series Processor	Piledriver
3320 EE	AMD Opteron	AMD Opteron 3300 Series Processor	Piledriver
3280	AMD Opteron	AMD Opteron 3200 Series Processor	Bulldozer
3260 HE	AMD Opteron	AMD Opteron 3200 Series Processor	Bulldozer
3250 HE	AMD Opteron	AMD Opteron 3200 Series Processor	Bulldozer

Model	Family	Line	uArch
R-252F	AMD Embedded R-Series Processors		Piledriver
R-260H	AMD Embedded R-Series Processors		Piledriver
R-268D	AMD Embedded R-Series Processors		Piledriver
R-272F	AMD Embedded R-Series Processors		Piledriver
R-452L	AMD Embedded R-Series Processors		Piledriver
R-460H	AMD Embedded R-Series Processors		Piledriver
R-460L	AMD Embedded R-Series Processors		Piledriver
R-464L	AMD Embedded R-Series Processors		Piledriver
A10-5750M	AMD A-Series Processors		Piledriver
A10-4600M	AMD A-Series Processors		Piledriver
A8-5550M	AMD A-Series Processors		Piledriver
A8-4500M	AMD A-Series Processors		Piledriver
A6-5350M	AMD A-Series Processors		Piledriver
A6-4400M	AMD A-Series Processors		Piledriver
A4-5150M	AMD A-Series Processors		Piledriver
A4-4300M	AMD A-Series Processors		Piledriver
A10-5757M	AMD A-Series Processors		Piledriver
A10-5745M	AMD A-Series Processors		Piledriver
A10-4655M	AMD A-Series Processors		Piledriver
A8-5557M	AMD A-Series Processors		Piledriver
A8-5545M	AMD A-Series Processors		Piledriver
A8-4555M	AMD A-Series		Piledriver

Model	Family	Line	uArch
	Processors		
A6-5357M	AMD A-Series Processors		Piledriver
A6-5345M	AMD A-Series Processors		Piledriver
A6-4455M	AMD A-Series Processors		Piledriver
A4-5145M	AMD A-Series Processors		Piledriver
A4-4355M	AMD A-Series Processors		Piledriver

Exhibit C.3 – Preliminary Accused Product Identification for '614 Patent – AMD Excavator(+) Processors

This identification of products is based on information reasonably available to Polaris, and was prepared without the benefit of discovery from AMD. Accordingly, this chart may not include non-public AMD products such as OEM or custom products. Aquila reserves the right to modify or supplement its identification of Accused Products when AMD provides more information.

Model	Family	Line	uArch
7th Gen AMD PRO A4-4350B APU	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Laptops	Excavator+
7th Gen AMD PRO A6-7350B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Excavator+
7th Gen A12 9800 APU	AMD A-Series Processors	AMD A12-Series APU for Desktops	Excavator+
7th Gen A12 9800E APU	AMD A-Series Processors	AMD A12-Series APU for Desktops	Excavator+
7th Gen A12 9720P APU	AMD A-Series Processors	AMD A10-Series APU for Desktops	Excavator+
7th Gen A10 9700 APU	AMD A-Series Processors	AMD A10-Series APU for Desktops	Excavator+
7th Gen A10 9700E APU	AMD A-Series Processors	AMD A10-Series APU for Desktops	Excavator+
7th Gen A10-9620P APU	AMD A-Series Processors	AMD A10-Series APU for Laptops	Excavator+
7th Gen A8 9600 APU	AMD A-Series Processors	AMD A8-Series APU for Desktops	Excavator+
7th Gen A6 9550 APU	AMD A-Series Processors	AMD A6-Series APU for Desktops	Excavator+
7th Gen A6 9500 APU	AMD A-Series Processors	AMD A6-Series APU for Desktops	Excavator+
7th Gen A6 9500E APU	AMD A-Series Processors	AMD A6-Series APU for Desktops	Excavator+
7th Gen A12-9730P APU	AMD A-Series Processors	AMD A12-Series APU for Laptops	Excavator+
7th Gen A12-9700P APU	AMD A-Series Processors	AMD A12-Series APU for Laptops	Excavator+
7th Gen A10-9630P APU	AMD A-Series Processors	AMD A10-Series APU for Laptops	Excavator+
7th Gen A10-9600P APU	AMD A-Series Processors	AMD A10-Series APU for Laptops	Excavator+
7th Gen A9-9425 APU	AMD A-Series Processors	AMD A9-Series APU for Laptops	Excavator+
7th Gen A9 9420 APU	AMD A-Series	AMD A9-Series APU	Excavator+

Model	Family	Line	uArch
	Processors	for Laptops	
7th Gen A9 9410 APU	AMD A-Series Processors	AMD A9-Series APU for Laptops	Excavator+
7th Gen A6-9225 APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6 9220 APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6-9220C APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6 9210 APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6-9200 APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6 9200e APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A4-9120 APU	AMD A-Series Processors	AMD A4-Series APU for Laptops	Excavator+
7th Gen A49120C APU	AMD A-Series Processors	AMD A4-Series APU for Laptops	Excavator+
7th Gen AMD PRO A12-9800 APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Desktops	Excavator+
7th Gen AMD PRO A12-9800E APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Desktops	Excavator+
7th Gen AMD PRO A10-9700 APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Excavator+
7th Gen AMD PRO A10-9700E APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Excavator+
7th Gen AMD PRO A8-9600 APU	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Desktops	Excavator+
7th Gen AMD PRO A6-9500 APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator+
7th Gen AMD PRO A6-9500E APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator+
7th Gen AMD PRO A12-9830B APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Laptops	Excavator+
7th Gen AMD PRO A12-9800B APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Laptops	Excavator+
7th Gen AMD PRO A10-9730B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator+

Model	Family	Line	uArch
7th Gen AMD PRO A10-9700B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator+
7th Gen AMD PRO A8-9630B	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Laptops	Excavator+
7th Gen AMD PRO A8-9600B APU	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Laptops	Excavator+
7th Gen AMD PRO A6-9500B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Excavator+
7th Gen FX 9830P APU	AMD FX-Series Processors	AMD FX-Series Processors for Laptops	Excavator+
7th Gen FX 9800P APU	AMD FX-Series Processors	AMD FX-Series Processors for Laptops	Excavator+
7th Gen E2 9010 APU	AMD E-Series Processors	AMD E2-Series APU for Laptops	Excavator+
6th Gen A10-8700P APU	AMD A-Series Processors	AMD A10-Series APU for Laptops	Excavator
6th Gen A8-8600P APU	AMD A-Series Processors	AMD A8-Series APU for Laptops	Excavator
6th Gen AMD PRO A12-8870 APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Desktops	Excavator
6th Gen AMD PRO A12-8870E APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Desktops	Excavator
6th Gen AMD PRO A10-8770 APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Excavator
6th Gen AMD PRO A10-8770E APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Excavator
6th Gen AMD PRO A8-8650B APU	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Desktops	Excavator
6th Gen AMD PRO A6-8570 APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator
6th Gen AMD PRO A6-8570E APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator
6th Gen AMD PRO A6-8550B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator
6th Gen AMD PRO A4-8350B APU	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Desktops	Excavator
6th Gen AMD PRO A12-	AMD PRO A-Series	AMD PRO A-Series	Excavator

Model	Family	Line	uArch
8830B APU	Processors	A12 APU for Laptops	
6th Gen AMD PRO A12-8800B APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Laptops	Excavator
6th Gen AMD PRO A10-8780P APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator
6th Gen AMD PRO A10-8730B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator
6th Gen AMD PRO A10-8700B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator
6th Gen AMD PRO A8-8600B APU	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Laptops	Excavator
6th Gen AMD PRO A6-8530B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Excavator
6th Gen AMD PRO A6-8500B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Excavator
6th Gen FX-8800P APU	AMD FX-Series Processors	AMD FX-Series Processors for Laptops	Excavator
A6-8500P with Radeon R5 Graphics	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator
A10-8700P with Radeon R6 Graphics	AMD A-Series Processors	AMD A10-Series APU for AIOs	Excavator
7th Gen AMD Athlon X4 970	AMD Athlon Processors	AMD Athlon X4	Excavator
A8-8600P with Radeon R6 Graphics	AMD A-Series Processors	AMD A8-Series APU for AIOs	Excavator
7th Gen AMD Athlon X4 950	AMD Athlon Processors	AMD Athlon X4	Excavator
7th Gen AMD Athlon X4 940	AMD Athlon Processors	AMD Athlon X4	Excavator
A6-8500P with Radeon R5 Graphics	AMD A-Series Processors	AMD A6-Series APU for AIOs	Excavator
835	AMD Athlon Processors	AMD Athlon X4	Excavator
845 with Near Silent Thermal Solution	AMD Athlon Processors	AMD Athlon X4	Excavator
FX-8800P with Radeon R7 Graphics	AMD FX-Series Processors	AMD FX-Series Processors for AIOs	Excavator
RX-421ND	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-421BD	AMD Embedded R-Series Processors	R-Series SOC	Excavator

Model	Family	Line	uArch
RX-418GD	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-416GD	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-216TD	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-216GD	AMD Embedded R-Series Processors	R-Series SOC	Excavator
GX-224IJ	AMD Embedded G-Series Processors	3rd Generation G-Series SOC J Family	Excavator
GX-215JJ	AMD Embedded G-Series Processors	3rd Generation G-Series SOC J Family	Excavator
GX-217GI	AMD Embedded G-Series Processors	3rd Generation G-Series SOC I Family	Excavator
GX-420GI	AMD Embedded G-Series Processors		Excavator
GX-212JJ	AMD Embedded G-Series Processors		Excavator
GX-220IJ	AMD Embedded G-Series Processors		Excavator
X3216	AMD Opteron	AMD Operton X3000-series	Excavator
X3418	AMD Opteron	AMD Operton X3000-series	Excavator
X3421	AMD Opteron	AMD Operton X3000-series	Excavator
Athlon X4 835	AMD Athlon Processors		Excavator
Athlon X4 845	AMD Athlon Processors		Excavator

Exhibit D.1 – Preliminary Accused Product Identification for '519 Patent – AMD Family 12h Processors

This identification of products is based on information reasonably available to Polaris, and was prepared without the benefit of discovery from AMD. Accordingly, this chart may not include non-public AMD products such as OEM or custom products. Aquila reserves the right to modify or supplement its identification of Accused Products when AMD provides more information.

Model	Family	Line	uArch
641	AMD Athlon Processors	AMD Athlon II X4	Llano
638	AMD Athlon Processors	AMD Athlon II X4	Llano
631	AMD Athlon Processors	AMD Athlon II X4	Llano
631	AMD Athlon Processors	AMD Athlon II X4	Llano
620e	AMD Athlon Processors	AMD Athlon II X4	Llano
E2-3000M	AMD E-Series Processors		Llano
A4-3300M	AMD A-Series Processors		Llano
A4-3305M	AMD A-Series Processors		Llano
A4-3310MX	AMD A-Series Processors		Llano
A4-3320M	AMD A-Series Processors		Llano
A4-3330MX	AMD A-Series Processors		Llano
A6-3400M	AMD A-Series Processors		Llano
A6-3410MX	AMD A-Series Processors		Llano
A6-3420M	AMD A-Series Processors		Llano
A6-3430MX	AMD A-Series Processors		Llano
A8-3500M	AMD A-Series Processors		Llano
A8-3510MX	AMD A-Series Processors		Llano
A8-3520M	AMD A-Series Processors		Llano
A8-3530MX	AMD A-Series Processors		Llano
A8-3550MX	AMD A-Series Processors		Llano
Sempron X2 198	AMD Sempron Processors		Llano
Athlon II X2 221	AMD Athlon Processors		Llano
Athlon II X4 651	AMD Athlon Processors		Llano
Athlon II X4 651K	AMD Athlon Processors		Llano
E2-3200	AMD E-Series Processors		Llano
A4-3300	AMD A-Series Processors		Llano
A4-3400	AMD A-Series Processors		Llano
A4-3420	AMD A-Series Processors		Llano

Model	Family	Line	uArch
A6-3500	AMD A-Series Processors		Llano
A6-3600	AMD A-Series Processors		Llano
A6-3620	AMD A-Series Processors		Llano
A6-3650	AMD A-Series Processors		Llano
A6-3670K	AMD A-Series Processors		Llano
A8-3800	AMD A-Series Processors		Llano
A8-3820	AMD A-Series Processors		Llano
A8-3850	AMD A-Series Processors		Llano
A8-3870K	AMD A-Series Processors		Llano

Exhibit D.2 – Preliminary Accused Product Identification for '519 Patent – AMD Family 14h Processors

This identification of products is based on information reasonably available to Polaris, and was prepared without the benefit of discovery from AMD. Accordingly, this chart may not include non-public AMD products such as OEM or custom products. Aquila reserves the right to modify or supplement its identification of Accused Products when AMD provides more information.

Model	Family	uArch
G-Series T24L	AMD Embedded G-Series Processors	Bobcat
G-Series T30L	AMD Embedded G-Series Processors	Bobcat
G-Series T48L	AMD Embedded G-Series Processors	Bobcat
G-Series T16R	AMD Embedded G-Series Processors	Bobcat
G-Series T40R	AMD Embedded G-Series Processors	Bobcat
G-Series T40E	AMD Embedded G-Series Processors	Bobcat
G-Series T40N	AMD Embedded G-Series Processors	Bobcat
G-Series T40R	AMD Embedded G-Series Processors	Bobcat
G-Series T44R	AMD Embedded G-Series Processors	Bobcat
G-Series T48E	AMD Embedded G-Series Processors	Bobcat
G-Series T48N	AMD Embedded G-Series Processors	Bobcat
G-Series T52R	AMD Embedded G-Series Processors	Bobcat
G-Series T56E	AMD Embedded G-Series Processors	Bobcat
G-Series T56N	AMD Embedded G-Series Processors	Bobcat
C-50	C-Series	Bobcat
C-60	C-Series	Bobcat
C-70	C-Series	Bobcat
E-240	AMD E-Series Processors	Bobcat
E-300	AMD E-Series Processors	Bobcat

Model	Family	uArch
E-350	AMD E-Series Processors	Bobcat
E-450	AMD E-Series Processors	Bobcat
E1-1200	AMD E-Series Processors	Bobcat
E1-1500[23]	AMD E-Series Processors	Bobcat
E2-1800	AMD E-Series Processors	Bobcat
E2-2000[23]	AMD E-Series Processors	Bobcat
Z-01	Z-Series	Bobcat
Z-60[24]	Z-Series	Bobcat

Exhibit D.3 – Preliminary Accused Product Identification for '519 Patent – AMD Family 15h Processors

This identification of products is based on information reasonably available to Polaris, and was prepared without the benefit of discovery from AMD. Accordingly, this chart may not include non-public AMD products such as OEM or custom products. Aquila reserves the right to modify or supplement its identification of Accused Products when AMD provides more information.

Model	Family	Line	uArch
7th Gen AMD PRO A4-4350B APU	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Laptops	Excavator+
7th Gen AMD PRO A6-7350B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Excavator+
7th Gen A12 9800 APU	AMD A-Series Processors	AMD A12-Series APU for Desktops	Excavator+
7th Gen A12 9800E APU	AMD A-Series Processors	AMD A12-Series APU for Desktops	Excavator+
7th Gen A12 9720P APU	AMD A-Series Processors	AMD A10-Series APU for Desktops	Excavator+
7th Gen A10 9700 APU	AMD A-Series Processors	AMD A10-Series APU for Desktops	Excavator+
7th Gen A10 9700E APU	AMD A-Series Processors	AMD A10-Series APU for Desktops	Excavator+
7th Gen A10-9620P APU	AMD A-Series Processors	AMD A10-Series APU for Laptops	Excavator+
7th Gen A8 9600 APU	AMD A-Series Processors	AMD A8-Series APU for Desktops	Excavator+
7th Gen A6 9550 APU	AMD A-Series Processors	AMD A6-Series APU for Desktops	Excavator+
7th Gen A6 9500 APU	AMD A-Series Processors	AMD A6-Series APU for Desktops	Excavator+
7th Gen A6 9500E APU	AMD A-Series Processors	AMD A6-Series APU for Desktops	Excavator+
7th Gen A12-9730P APU	AMD A-Series Processors	AMD A12-Series APU for Laptops	Excavator+
7th Gen A12-9700P APU	AMD A-Series Processors	AMD A12-Series APU for Laptops	Excavator+
7th Gen A10-9630P APU	AMD A-Series Processors	AMD A10-Series APU for Laptops	Excavator+
7th Gen A10-9600P APU	AMD A-Series Processors	AMD A10-Series APU for Laptops	Excavator+
7th Gen A9-9425	AMD A-Series	AMD A9-Series APU for	Excavator+

Model	Family	Line	uArch
APU	Processors	Laptops	
7th Gen A9 9420 APU	AMD A-Series Processors	AMD A9-Series APU for Laptops	Excavator+
7th Gen A9 9410 APU	AMD A-Series Processors	AMD A9-Series APU for Laptops	Excavator+
7th Gen A6-9225 APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6 9220 APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6-9220C APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6 9210 APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6-9200 APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A6 9200e APU	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator+
7th Gen A4-9120 APU	AMD A-Series Processors	AMD A4-Series APU for Laptops	Excavator+
7th Gen A49120C APU	AMD A-Series Processors	AMD A4-Series APU for Laptops	Excavator+
7th Gen AMD PRO A12-9800 APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Desktops	Excavator+
7th Gen AMD PRO A12-9800E APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Desktops	Excavator+
7th Gen AMD PRO A10-9700 APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Excavator+
7th Gen AMD PRO A10-9700E APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Excavator+
7th Gen AMD PRO A8-9600 APU	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Desktops	Excavator+
7th Gen AMD PRO A6-9500 APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator+
7th Gen AMD PRO A6-9500E APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator+
7th Gen AMD PRO A12-9830B	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Laptops	Excavator+

Model	Family	Line	uArch
APU			
7th Gen AMD PRO A12-9800B APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Laptops	Excavator+
7th Gen AMD PRO A10-9730B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator+
7th Gen AMD PRO A10-9700B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator+
7th Gen AMD PRO A8-9630B	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Laptops	Excavator+
7th Gen AMD PRO A8-9600B APU	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Laptops	Excavator+
7th Gen AMD PRO A6-9500B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Excavator+
7th Gen FX 9830P APU	AMD FX-Series Processors	AMD FX-Series Processors for Laptops	Excavator+
7th Gen FX 9800P APU	AMD FX-Series Processors	AMD FX-Series Processors for Laptops	Excavator+
7th Gen E2 9010 APU	AMD E-Series Processors	AMD E2-Series APU for Laptops	Excavator+
6th Gen A10-8700P APU	AMD A-Series Processors	AMD A10-Series APU for Laptops	Excavator
6th Gen A8-8600P APU	AMD A-Series Processors	AMD A8-Series APU for Laptops	Excavator
6th Gen AMD PRO A12-8870 APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Desktops	Excavator
6th Gen AMD PRO A12-8870E APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Desktops	Excavator
6th Gen AMD PRO A10-8850B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Steamroller
6th Gen AMD PRO A10-8770 APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Excavator
6th Gen AMD PRO A10-8770E APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Excavator

Model	Family	Line	uArch
6th Gen AMD PRO A10-8750B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Steamroller
6th Gen AMD PRO A8-8650B APU	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Desktops	Excavator
6th Gen AMD PRO A6-8570 APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator
6th Gen AMD PRO A6-8570E APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator
6th Gen AMD PRO A6-8550B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Excavator
6th Gen AMD PRO A4-8350B APU	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Desktops	Excavator
6th Gen AMD PRO A12-8830B APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Laptops	Excavator
6th Gen AMD PRO A12-8800B APU	AMD PRO A-Series Processors	AMD PRO A-Series A12 APU for Laptops	Excavator
6th Gen AMD PRO A10-8780P APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator
6th Gen AMD PRO A10-8730B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator
6th Gen AMD PRO A10-8700B APU	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Excavator
6th Gen AMD PRO A8-8600B APU	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Laptops	Excavator
6th Gen AMD PRO A6-8530B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Excavator
6th Gen AMD PRO A6-8500B APU	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Excavator
6th Gen FX-8800P APU	AMD FX-Series Processors	AMD FX-Series Processors for Laptops	Excavator

Model	Family	Line	uArch
A10-7890K with Radeon R7 Graphics and Wraith cooler	AMD A-Series Processors	AMD A10-Series APU for Desktops	Steamroller
A10-7870K with Radeon R7 Series	AMD A-Series Processors	AMD A10-Series APU for Desktops	Steamroller
A10-7870K with Radeon R7 Graphics and Near Silent Thermal Solution	AMD A-Series Processors	AMD A10-Series APU for Desktops	Steamroller
A10-7860K with Radeon R7 Series	AMD A-Series Processors	AMD A10-Series APU for Desktops	Steamroller
A10-7860K with Radeon R7 Graphics and Near Silent Thermal Solution	AMD A-Series Processors	AMD A10-Series APU for Desktops	Steamroller
A10-7850K with Radeon R7 Series	AMD A-Series Processors	AMD A10-Series APU for Desktops	Steamroller
A10-7800 with Radeon R7 Series	AMD A-Series Processors	AMD A10-Series APU for Desktops	Steamroller
A10-7700K with Radeon R7 Series	AMD A-Series Processors	AMD A10-Series APU for Desktops	Steamroller
A10-6800B with Radeon HD 8670D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6800K with Radeon HD 8670D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6790K with Radeon HD 8670D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6790B	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6700 with Radeon HD 8670D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-6700T with Radeon HD 8650D	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A8-7670K with Radeon R7 Graphics and	AMD A-Series Processors	AMD A8-Series APU for Desktops	Steamroller

Model	Family	Line	uArch
Near Silent Thermal Solution			
A8-7650K with Radeon R7 Series	AMD A-Series Processors	AMD A8-Series APU for Desktops	Steamroller
A8-7650K with Radeon R7 Graphics and Near Silent Thermal Solution	AMD A-Series Processors	AMD A8-Series APU for Desktops	Steamroller
A8-7600 with Radeon R7 Series	AMD A-Series Processors	AMD A8-Series APU for Desktops	Steamroller
A10-5800K	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A10-5700	AMD A-Series Processors	AMD A10-Series APU for Desktops	Piledriver
A8-6600K with Radeon HD 8570D	AMD A-Series Processors	AMD A8-Series APU for Desktops	Piledriver
A8-6500B	AMD A-Series Processors	AMD A8-Series APU for Desktops	Piledriver
A8-6500 with Radeon HD 8570D	AMD A-Series Processors	AMD A8-Series APU for Desktops	Piledriver
A8-6500T with Radeon HD 8550D	AMD A-Series Processors	AMD A8-Series APU for Desktops	Piledriver
A6-7470K with Radeon R5 Series	AMD A-Series Processors	AMD A6-Series APU for Desktops	Steamroller
A6-7400K with Radeon R5 Series	AMD A-Series Processors	AMD A6-Series APU for Desktops	Steamroller
A6-6420K with Radeon HD 8470D	AMD A-Series Processors	AMD A6-Series APU for Desktops	Piledriver
A6-6400K with Radeon HD 8470D	AMD A-Series Processors	AMD A6-Series APU for Desktops	Piledriver
A6-5400K	AMD A-Series Processors	AMD A6-Series APU for Desktops	Piledriver
A4-7300 with Radeon HD 8470D	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-6320B	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver

Model	Family	Line	uArch
A4-6320 with Radeon HD 8370D	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-6300	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-6300B	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-6300 with Radeon HD 8370D	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
FX-9590	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-9370	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8370 with Wraith cooler	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8370E	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
A10-7400P with Radeon R6 Graphics	AMD A-Series Processors	AMD A10-Series APU for Laptops	Steamroller
FX-8370	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
A10-7300 with Radeon R6 Graphics	AMD A-Series Processors	AMD A10-Series APU for Laptops	Steamroller
FX-8350 with Wraith cooler	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8350	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8320E	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8320	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8310	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8300	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Piledriver
FX-8170	AMD FX-Series Processors		Bulldozer
FX-8150	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Bulldozer
FX-8140	AMD FX-Series		Bulldozer

Model	Family	Line	uArch
	Processors		
FX-8120	AMD FX-Series Processors	AMD FX 8-Core Black Edition Processors	Bulldozer
FX-8100	AMD FX-Series Processors		Bulldozer
FX-6350 with Wraith cooler	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Piledriver
A4-4020	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A4-4000	AMD A-Series Processors	AMD A4-Series APU for Desktops	Piledriver
A8-7200P with Radeon R5 Graphics	AMD A-Series Processors	AMD A8-Series APU for Laptops	Piledriver
FX-6350	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Piledriver
A8-7100 with Radeon R5 Graphics	AMD A-Series Processors	AMD A8-Series APU for Laptops	Steamroller
FX-6300	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Piledriver
FX-6200	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Bulldozer
FX-6130	AMD FX-Series Processors		Bulldozer
FX-6120	AMD FX-Series Processors		Bulldozer
FX 6100	AMD FX-Series Processors	AMD FX 6-Core Black Edition Processors	Bulldozer
FX-4350	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Piledriver
FX-4320	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Piledriver
FX-4300	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Piledriver
FX-4170	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Bulldozer
FX-4150	AMD FX-Series Processors		Bulldozer
FX-4130	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Bulldozer
FX-4120	AMD FX-Series Processors		Bulldozer

Model	Family	Line	uArch
FX-4100	AMD FX-Series Processors	AMD FX 4-Core Black Edition Processors	Bulldozer
A6-8500P with Radeon R5 Graphics	AMD A-Series Processors	AMD A6-Series APU for Laptops	Excavator
A6-7000 with Radeon R4 Graphics	AMD A-Series Processors	AMD A6-Series APU for Laptops	Steamroller
A6-5350M with Radeon HD 8450G	AMD A-Series Processors	AMD A6-Series APU for Laptops	Piledriver
A10-8700P with Radeon R6 Graphics	AMD A-Series Processors	AMD A10-Series APU for AIOs	Excavator
7th Gen AMD Athlon X4 970	AMD Athlon Processors	AMD Athlon X4	Excavator
A8-8600P with Radeon R6 Graphics	AMD A-Series Processors	AMD A8-Series APU for AIOs	Excavator
7th Gen AMD Athlon X4 950	AMD Athlon Processors	AMD Athlon X4	Excavator
7th Gen AMD Athlon X4 940	AMD Athlon Processors	AMD Athlon X4	Excavator
A6-8500P with Radeon R5 Graphics	AMD A-Series Processors	AMD A6-Series APU for AIOs	Excavator
830	AMD Athlon Processors	AMD Athlon X4	Steamroller
840	AMD Athlon Processors	AMD Athlon X4	Steamroller
880K with Near Silent Thermal Solution	AMD Athlon Processors	AMD Athlon X4	Steamroller
870K with Near Silent Thermal Solution	AMD Athlon Processors	AMD Athlon X4	Steamroller
860K	AMD Athlon Processors	AMD Athlon X4	Steamroller
A10-6800B with Radeon HD 8670D	AMD A-Series Processors	AMD Business Class - Quad-Core A10-Series APU for Desktops	Piledriver
860K with Near Silent Thermal Solution	AMD Athlon Processors	AMD Athlon X4	Steamroller
A10-6790B with Radeon HD	AMD A-Series Processors	AMD Business Class - Quad-Core A10-Series APU for	Piledriver

Model	Family	Line	uArch
8670D		Desktops	
835	AMD Athlon Processors	AMD Athlon X4	Excavator
845 with Near Silent Thermal Solution	AMD Athlon Processors	AMD Athlon X4	Excavator
A8-6500B with Radeon HD 8570D	AMD A-Series Processors	AMD Business Class - Quad-Core A8-Series APU for Desktops	Piledriver
760K	AMD Athlon Processors	AMD Athlon X4	Piledriver
750	AMD Athlon Processors	AMD Athlon X4	Piledriver
A6-6420B with Radeon HD 8470D	AMD A-Series Processors	AMD Business Class - Dual-Core A6-Series APU for Desktops	Piledriver
750K	AMD Athlon Processors	AMD Athlon X4	Piledriver
A6-6400B with Radeon HD 8470D	AMD A-Series Processors	AMD Business Class - Dual-Core A6-Series APU for Desktops	Piledriver
740	AMD Athlon Processors	AMD Athlon X4	Piledriver
6386 SE	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6380	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
A10 PRO-7850B with Radeon R7 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Steamroller
6378	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6376	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
A10 PRO-7800B with Radeon R7 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Desktops	Steamroller
A8 PRO-7600B with Radeon R7 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Desktops	Steamroller
6370P	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
A6 PRO-7400B with Radeon R5 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Desktops	Steamroller
6366 HE	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver

Model	Family	Line	uArch
A4 PRO-7350B with Radeon R5 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Desktops	Steamroller
6348	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
A4 PRO-7300B with Radeon HD 8470D	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Desktops	Piledriver
6344	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
A10 PRO-7350B with Radeon R6 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A10 APU for Laptops	Steamroller
6338P	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6328	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
A8 PRO-7150B with Radeon R5 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A8 APU for Laptops	Steamroller
6320	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
A6 PRO-7050B with Radeon R4 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A6 APU for Laptops	Steamroller
6308	AMD Opteron	AMD Opteron 6300 Series Processor	Piledriver
6287 SE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6284 SE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
FX-7600P with Radeon R7 Graphics	AMD FX-Series Processors	AMD FX-Series Processors for Laptops	Steamroller
6282 SE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
FX-7500 with Radeon R7 Graphics	AMD FX-Series Processors	AMD FX-Series Processors for Laptops	Steamroller
6278	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6276	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer

Model	Family	Line	uArch
FX-8800P with Radeon R7 Graphics	AMD FX-Series Processors	AMD FX-Series Processors for AIOs	Excavator
6274	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6272	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6262 HE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6230 HE	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6238	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6234	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6220	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6212	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
6204	AMD Opteron	AMD Opteron 6200 Series Processor	Bulldozer
4386	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
43GK HE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4376 HE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4365	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4340	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4334	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4332 HE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
43CX EE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4310 EE	AMD Opteron	AMD Opteron 4300 Series Processor	Piledriver
4284	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4280	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4276 HE	AMD Opteron	AMD Opteron 4200 Series	Bulldozer

Model	Family	Line	uArch
		Processor	
4274 HE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
42MX EE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4256 EE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4240	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4238	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4234	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4230 HE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4228 HE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
4226	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
42DX EE	AMD Opteron	AMD Opteron 4200 Series Processor	Bulldozer
3380	AMD Opteron	AMD Opteron 3300 Series Processor	Piledriver
3365	AMD Opteron	AMD Opteron 3300 Series Processor	Piledriver
3350 HE	AMD Opteron	AMD Opteron 3300 Series Processor	Piledriver
3320 EE	AMD Opteron	AMD Opteron 3300 Series Processor	Piledriver
3280	AMD Opteron	AMD Opteron 3200 Series Processor	Bulldozer
3260 HE	AMD Opteron	AMD Opteron 3200 Series Processor	Bulldozer
3250 HE	AMD Opteron	AMD Opteron 3200 Series Processor	Bulldozer
RX-421ND	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-421BD	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-418GD	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-416GD	AMD Embedded R-Series Processors	R-Series SOC	Excavator

Model	Family	Line	uArch
RX-216TD	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-216GD	AMD Embedded R-Series Processors	R-Series SOC	Excavator
RX-427NB	AMD Embedded R-Series Processors	2nd Generation R-Series APU	Steamroller
RX-427BB	AMD Embedded R-Series Processors	2nd Generation R-Series APU	Steamroller
RX-425BB	AMD Embedded R-Series Processors	2nd Generation R-Series APU	Steamroller
RX-225FB	AMD Embedded R-Series Processors	2nd Generation R-Series APU	Steamroller
RX-219NB	AMD Embedded R-Series Processors	2nd Generation R-Series APU	Steamroller
GX-224IJ	AMD Embedded G-Series Processors	3rd Generation G-Series SOC J Family	Excavator
GX-215JJ	AMD Embedded G-Series Processors	3rd Generation G-Series SOC J Family	Excavator
GX-217GI	AMD Embedded G-Series Processors	3rd Generation G-Series SOC I Family	Excavator
GX-420GI	AMD Embedded G-Series Processors		Excavator
GX-212JJ	AMD Embedded G-Series Processors		Excavator
GX-220IJ	AMD Embedded G-Series Processors		Excavator
R-252F	AMD Embedded R-Series Processors		Piledriver
R-260H	AMD Embedded R-Series Processors		Piledriver
R-268D	AMD Embedded R-Series Processors		Piledriver
R-272F	AMD Embedded R-Series Processors		Piledriver
R-452L	AMD Embedded R-Series Processors		Piledriver
R-460H	AMD Embedded R-Series Processors		Piledriver
R-460L	AMD Embedded R-Series Processors		Piledriver

Model	Family	Line	uArch
R-464L	AMD Embedded R-Series Processors		Piledriver
X3216	AMD Opteron	AMD Operton X3000-series	Excavator
X3418	AMD Opteron	AMD Operton X3000-series	Excavator
X3421	AMD Opteron	AMD Operton X3000-series	Excavator
A10-5750M	AMD A-Series Processors		Piledriver
A10-4600M	AMD A-Series Processors		Piledriver
A8-5550M	AMD A-Series Processors		Piledriver
A8-4500M	AMD A-Series Processors		Piledriver
A6-5350M	AMD A-Series Processors		Piledriver
A6-4400M	AMD A-Series Processors		Piledriver
A4-5150M	AMD A-Series Processors		Piledriver
A4-4300M	AMD A-Series Processors		Piledriver
A10-5757M	AMD A-Series Processors		Piledriver
A10-5745M	AMD A-Series Processors		Piledriver
A10-4655M	AMD A-Series Processors		Piledriver
A8-5557M	AMD A-Series Processors		Piledriver
A8-5545M	AMD A-Series Processors		Piledriver
A8-4555M	AMD A-Series Processors		Piledriver
A6-5357M	AMD A-Series Processors		Piledriver
A6-5345M	AMD A-Series Processors		Piledriver
A6-4455M	AMD A-Series Processors		Piledriver
A4-5145M	AMD A-Series		Piledriver

Model	Family	Line	uArch
	Processors		
A4-4355M	AMD A-Series Processors		Piledriver
Athlon X2 450	AMD Athlon Processors		Steamroller
Athlon X4 830	AMD Athlon Processors		Steamroller
Athlon X4 840	AMD Athlon Processors		Steamroller
Athlon X4 860K	AMD Athlon Processors		Steamroller
Athlon X4 870K	AMD Athlon Processors		Steamroller
Athlon X4 880K	AMD Athlon Processors		Steamroller
Athlon X4 835	AMD Athlon Processors		Excavator
Athlon X4 845	AMD Athlon Processors		Excavator

Exhibit D.4 – Preliminary Accused Product Identification for '519 Patent – AMD 16h Product Family

This identification of products is based on information reasonably available to Polaris, and was prepared without the benefit of discovery from AMD. Accordingly, this chart may not include non-public AMD products such as OEM or custom products. Aquila reserves the right to modify or supplement its identification of Accused Products when AMD provides more information.

Model	Family	Line	uArch
A6-6310 with Radeon R4 Graphics	AMD A-Series Processors	AMD A6-Series APU for Desktops	Jaguar+
A6-5200 with Radeon HD 8400	AMD A-Series Processors	AMD A6-Series APU for Desktops	Jaguar
A4-5100 with Radeon HD 8330	AMD A-Series Processors	AMD A4-Series APU for Desktops	Jaguar
A4-5000 with Radeon HD 8330	AMD A-Series Processors	AMD A4-Series APU for Desktops	Jaguar
A10 Micro-6700T with Radeon R6 Graphics	AMD A-Series Processors	AMD A10-Series APU for Laptops	Jaguar+
A6 Micro 6500T	AMD A-Series Processors		Jaguar+
A8-7410 with Radeon R5 Graphics	AMD A-Series Processors	AMD A8-Series APU for Laptops	Jaguar+
A8-6410 with Radeon R5 Graphics	AMD A-Series Processors	AMD A8-Series APU for Laptops	Jaguar+
A6-7310 with Radeon R4 Graphics	AMD A-Series Processors	AMD A6-Series APU for Laptops	Jaguar+
A6-6310 with Radeon R4 Graphics	AMD A-Series Processors	AMD A6-Series APU for Laptops	Jaguar+
A6-5200M with Radeon HD 8400	AMD A-Series Processors	AMD A6-Series APU for Laptops	Jaguar
A4-7210 with Radeon R3 Graphics	AMD A-Series Processors	AMD A4-Series APU for Laptops	Jaguar+
A4 Micro-6400T with Radeon R3 Graphics	AMD A-Series Processors	AMD A4-Series APU for Laptops	Jaguar+
A4-6210 with Radeon R3 Graphics	AMD A-Series Processors	AMD A4-Series APU for Laptops	Jaguar+
A4-5100 with Radeon HD 8330	AMD A-Series Processors	AMD A4-Series APU for Laptops	Jaguar
A4-5000 with Radeon HD 8330	AMD A-Series Processors	AMD A4-Series APU for Laptops	Jaguar
A4-6250J	AMD A-Series Processors		Jaguar+

Model	Family	Line	uArch
A6-6310	AMD A-Series Processors		Jaguar+
A8-6410 with Radeon R5 Graphics	AMD A-Series Processors	AMD A8-Series APU for AIOs	Jaguar+
A6-7310 with Radeon R4 Graphics	AMD A-Series Processors	AMD A6-Series APU for AIOs	Jaguar+
A4-7210 with Radeon R3 Graphics	AMD A-Series Processors	AMD A4-Series APU for AIOs	Jaguar+
X1150	AMD Opteron	AMD Opteron X1100 Series Processors	Jaguar
A4 PRO-3350B with Radeon R4 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Laptops	Jaguar+
A4 PRO-3340B with Radeon HD 8240 Graphics	AMD PRO A-Series Processors	AMD PRO A-Series A4 APU for Laptops	Jaguar
Athlon 5370 APU with Radeon R3 Series	AMD Athlon Processors	AMD Athlon Quad-Core APU	Jaguar
Athlon 5350 APU with Radeon R3 Series	AMD Athlon Processors	AMD Athlon Quad-Core APU	Jaguar
Athlon 5150 APU with Radeon R3 Series	AMD Athlon Processors	AMD Athlon Quad-Core APU	Jaguar
Sempron 3850 APU with Radeon R3 Series	AMD Sempron	AMD Sempron Quad-Core APU	Jaguar
Sempron 2650 APU with Radeon R3 Series	AMD Sempron	AMD Sempron Dual-Core APU	Jaguar
E2-7110 with Radeon R2 Graphics	AMD E-Series Processors	AMD E2-Series APU for Laptops	Jaguar+
E2-7110 with Radeon R2 Graphics	AMD E-Series Processors	AMD E2-Series APU for Laptops	Jaguar+
E2-6110 with Radeon R2 Graphics	AMD E-Series Processors	AMD E2-Series APU for Laptops	Jaguar+
E2-3800 with Radeon HD 8280	AMD E-Series Processors	AMD E2-Series APU for Laptops	Jaguar
E2-3000 with Radeon HD 8280	AMD E-Series Processors	AMD E2-Series APU for Laptops	Jaguar
E2-7110 with Radeon R2 Graphics	AMD E-Series Processors	AMD E2-Series APU for AIOs	Jaguar+
E1-7010 with Radeon R2 Graphics	AMD E-Series Processors	AMD E1-Series APU for Laptops	Jaguar+
E1 Micro-6200T with Radeon R2 Graphics	AMD E-Series Processors	AMD E1-Series APU for Laptops	Jaguar+
E1-6010 with Radeon R2 Graphics	AMD E-Series Processors	AMD E1-Series APU for Laptops	Jaguar+

Model	Family	Line	uArch
E1-6015	AMD E-Series Processors	AMD E1-Series APU for Laptops	Jaguar+
E1-2500 with Radeon HD 8240	AMD E-Series Processors	AMD E1-Series APU for Laptops	Jaguar
E1-2200 with Radeon HD 8210	AMD E-Series Processors	AMD E1-Series APU for Laptops	Jaguar
E1-2100 with Radeon HD 8210	AMD E-Series Processors	AMD E1-Series APU for Laptops	Jaguar
E1-7010 with Radeon R2 Graphics	AMD E-Series Processors	AMD E1-Series APU for AIOs	Jaguar
AMD Opteron X2170	AMD Opteron	AMD Opteron X2100 Series APU	Jaguar
AMD Opteron X2150 APU	AMD Opteron	AMD Opteron X2100 Series APU	Jaguar
GX-424CC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-420MC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-412TC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-412HC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-410VC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-224PC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-222GC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-216HC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-212JC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-210JC	AMD Embedded G-Series Processors	2nd Generation G-Series SOC	Jaguar+
GX-420CA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-416RA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-415GA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-411GA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar

Model	Family	Line	uArch
GX-218TF	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-217GA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-210UA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-210JA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-210HA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-209HA	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-208VF	AMD Embedded G-Series Processors	1st Generation G-Series SOC	Jaguar
GX-218GL	AMD Embedded G-Series Processors	G-Series LX SOC	Jaguar+
GX-215GL	AMD Embedded G-Series Processors	G-Series LX SOC	Jaguar+
GX-210KL	AMD Embedded G-Series Processors	G-Series LX SOC	Jaguar+
GX-210HL	AMD Embedded G-Series Processors	G-Series LX SOC	Jaguar+
GX-216HC	AMD Embedded G-Series Processors		Jaguar+
GX-222GC	AMD Embedded G-Series Processors		Jaguar+
GX-424CC	AMD Embedded G-Series Processors		Jaguar+
GX-208JL	AMD Embedded G-Series Processors		Jaguar+
GX-210HL	AMD Embedded G-Series Processors		Jaguar+
GX-210JL	AMD Embedded G-Series Processors		Jaguar+
A6-1450	AMD A-Series Processors		Jaguar
A4-1350	AMD A-Series Processors		Jaguar
A4-1250	AMD A-Series Processors		Jaguar
A4-1200	AMD A-Series Processors		Jaguar

Model	Family	Line	uArch
Playstation 4 APU			Jaguar
Playstation 4 Slim APU			Jaguar
Playstation 4 Pro APU			Jaguar
Xbox One APU			Jaguar
Xbox One S APU			Jaguar
Xbox one X APU			Jaguar

Exhibit D.5 – Preliminary Accused Product Identification for '519 Patent – Products Containing Zen or Zen+ Cores

This identification of products is based on information reasonably available to Polaris, and was prepared without the benefit of discovery from AMD. Accordingly, this chart may not include non-public AMD products such as OEM or custom products. Aquila reserves the right to modify or supplement its identification of Accused Products when AMD provides more information.

Model	Family	Line	uArch
AMD Athlon 240GE	AMD Athlon Processors	AMD Athlon Desktop Processors with Radeon Vega Graphics	Zen
AMD Athlon 220GE	AMD Athlon Processors	AMD Athlon Desktop Processors with Radeon Vega Graphics	Zen
AMD Athlon 200GE	AMD Athlon Processors	AMD Athlon Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 7 3750H	AMD Ryzen Processors	AMD Ryzen 7 Mobile Processors with Radeon RX Vega Graphics	Zen+
AMD Ryzen 7 3700U	AMD Ryzen Processors	AMD Ryzen 7 Mobile Processors with Radeon RX Vega Graphics	Zen+
AMD Ryzen 5 3550H	AMD Ryzen Processors	AMD Ryzen 5 Mobile Processors with Radeon Vega Graphics	Zen+
AMD Ryzen 5 3500U	AMD Ryzen Processors	AMD Ryzen 5 Mobile Processors with Radeon Vega Graphics	Zen+
AMD Ryzen 3 3300U	AMD Ryzen Processors	AMD Ryzen 3 Mobile Processors with Radeon Vega Graphics	Zen+
AMD Ryzen 3 3200U	AMD Ryzen Processors	AMD Ryzen 3 Mobile Processors with Radeon Vega Graphics	Zen+
AMD Athlon 300U	AMD Athlon Processors	AMD Athlon Mobile Processors with Radeon Vega Graphics	Zen
AMD Ryzen Threadripper 2990WX	AMD Ryzen Processors	AMD Ryzen Threadripper Processors	Zen+
AMD Ryzen Threadripper	AMD Ryzen Processors	AMD Ryzen Threadripper Processors	Zen+

Model	Family	Line	uArch
2970WX			
AMD Ryzen Threadripper 2950X	AMD Ryzen Processors	AMD Ryzen Threadripper Processors	Zen+
AMD Ryzen Threadripper 2920X	AMD Ryzen Processors	AMD Ryzen Threadripper Processors	Zen+
AMD Ryzen 7 2700X	AMD Ryzen Processors	AMD Ryzen 7 Desktop Processors	Zen+
AMD Ryzen 7 2700	AMD Ryzen Processors	AMD Ryzen 7 Desktop Processors	Zen+
AMD Ryzen 7 2700E Processor	AMD Ryzen Processors	AMD Ryzen 7 Desktop Processors	Zen+
AMD Ryzen 5 2600X	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors	Zen+
AMD Ryzen 5 2600	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors	Zen+
AMD Ryzen 5 2600E	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors	Zen+
AMD Ryzen 5 2500X	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors	Zen+
AMD Ryzen 5 2400G with Radeon RX Vega 11 Graphics	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 5 2400GE with Radeon RX Vega 11 Graphics	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 3 2300X	AMD Ryzen Processors	AMD Ryzen 3 Desktop Processors	Zen+
AMD Ryzen 3 2200G with Radeon Vega 8 Graphics	AMD Ryzen Processors	AMD Ryzen 3 Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 3 2200GE with Radeon Vega 8 Graphics	AMD Ryzen Processors	AMD Ryzen 3 Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 7 2800H	AMD Ryzen Processors	AMD Ryzen 7 Mobile Processors with Radeon RX Vega Graphics	Zen
AMD Ryzen 5 2600H	AMD Ryzen Processors	AMD Ryzen 5 Mobile Processors with Radeon Vega	Zen

Model	Family	Line	uArch
		Graphics	
AMD Ryzen 7 2700U	AMD Ryzen Processors	AMD Ryzen 7 Mobile Processors with Radeon RX Vega Graphics	Zen
AMD Ryzen 5 2500U	AMD Ryzen Processors	AMD Ryzen 5 Mobile Processors with Radeon Vega Graphics	Zen
AMD Ryzen 3 2300U	AMD Ryzen Processors	AMD Ryzen 3 Mobile Processors with Radeon Vega Graphics	Zen
AMD Ryzen 3 2200U	AMD Ryzen Processors	AMD Ryzen 3 Mobile Processors with Radeon Vega Graphics	Zen
AMD Ryzen Threadripper 1950X	AMD Ryzen Processors	AMD Ryzen Threadripper Processors	Zen
AMD Ryzen Threadripper 1920X	AMD Ryzen Processors	AMD Ryzen Threadripper Processors	Zen
AMD Ryzen Threadripper 1900X	AMD Ryzen Processors	AMD Ryzen Threadripper Processors	Zen
AMD Ryzen 7 1800X	AMD Ryzen Processors	AMD Ryzen 7 Desktop Processors	Zen
AMD Ryzen 7 1700X	AMD Ryzen Processors	AMD Ryzen 7 Desktop Processors	Zen
AMD Ryzen 7 1700 Processor	AMD Ryzen Processors	AMD Ryzen 7 Desktop Processors	Zen
AMD Ryzen 5 1600X	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors	Zen
AMD Ryzen 5 1600	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors	Zen
AMD Ryzen 5 1500X	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors	Zen
AMD Ryzen 5 1400	AMD Ryzen Processors	AMD Ryzen 5 Desktop Processors	Zen
AMD Ryzen 3 1300X	AMD Ryzen Processors	AMD Ryzen 3 Desktop Processors	Zen
AMD Ryzen 3 1200	AMD Ryzen Processors	AMD Ryzen 3 Desktop Processors	Zen
AMD Ryzen 7 PRO 2700X	AMD Ryzen PRO Processors	AMD Ryzen 7 PRO Desktop Processors	Zen+
AMD Ryzen 7	AMD Ryzen PRO	AMD Ryzen 7 PRO Desktop	Zen+

Model	Family	Line	uArch
PRO 2700	Processors	Processors	
AMD Ryzen 7 PRO 1700X Processor	AMD Ryzen PRO Processors	AMD Ryzen 7 PRO Desktop Processors	Zen
AMD Ryzen 7 PRO 1700	AMD Ryzen PRO Processors	AMD Ryzen 7 PRO Desktop Processors	Zen
AMD Ryzen 5 PRO 2600	AMD Ryzen PRO Processors	AMD Ryzen 5 PRO Desktop Processors	Zen+
AMD Ryzen 5 PRO 1600	AMD Ryzen PRO Processors	AMD Ryzen 5 PRO Desktop Processors	Zen
AMD Ryzen 5 PRO 1500	AMD Ryzen PRO Processors	AMD Ryzen 5 PRO Desktop Processors	Zen
AMD Ryzen 7 PRO 2700U	AMD Ryzen PRO Processors	AMD Ryzen 7 PRO Mobile Processors with Radeon Vega Graphics	Zen
AMD Ryzen 5 PRO 2400G with Radeon Vega 11 Graphics	AMD Ryzen PRO Processors	AMD Ryzen 5 PRO Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 5 PRO 2400GE with Radeon Vega 11 Graphics	AMD Ryzen PRO Processors	AMD Ryzen 5 PRO Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 3 PRO 1300	AMD Ryzen PRO Processors	AMD Ryzen 3 PRO Desktop Processors	Zen
AMD Ryzen 5 PRO 2500U	AMD Ryzen PRO Processors	AMD Ryzen 5 PRO Mobile Processors with Radeon Vega Graphics	Zen
AMD Ryzen 3 PRO 2200G with Radeon Vega 8 Graphics	AMD Ryzen PRO Processors	AMD Ryzen 3 PRO Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 3 PRO 2200GE with Radeon Vega 8 Graphics	AMD Ryzen PRO Processors	AMD Ryzen 3 PRO Desktop Processors with Radeon Vega Graphics	Zen
AMD Ryzen 3 PRO 1200	AMD Ryzen PRO Processors	AMD Ryzen 3 PRO Desktop Processors	Zen
AMD Ryzen 3 PRO 2300U	AMD Ryzen PRO Processors	AMD Ryzen 3 PRO Mobile Processors with Radeon Vega Graphics	Zen
AMD EPYC 7601	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7551P	AMD EPYC	AMD EPYC 7000 Series	Zen

Model	Family	Line	uArch
AMD EPYC 7551	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7501	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7451	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7401P	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7401	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7351P	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7351	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7301	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7281	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7261	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD EPYC 7251	AMD EPYC	AMD EPYC 7000 Series	Zen
AMD Athlon 240GE	AMD Athlon Processors	AMD Athlon Desktop Processors with Radeon Vega Graphics	Zen
AMD Athlon 220GE	AMD Athlon Processors	AMD Athlon Desktop Processors with Radeon Vega Graphics	Zen
AMD Athlon 200GE	AMD Athlon Processors	AMD Athlon Desktop Processors with Radeon Vega Graphics	Zen
AMD Athlon PRO 200GE	AMD Athlon PRO Processors	AMD Athlon PRO Desktop Processors with Radeon Vega Graphics	Zen
AMD EPYC Embedded 3251	AMD EPYC Embedded Processors	EPYC Embedded SOC	Zen
AMD EPYC Embedded 3201	AMD EPYC Embedded Processors	EPYC Embedded SOC	Zen
AMD EPYC Embedded 3151	AMD EPYC Embedded Processors	EPYC Embedded SOC	Zen
AMD EPYC Embedded 3101	AMD EPYC Embedded Processors	EPYC Embedded SOC	Zen
AMD Ryzen Embedded V1807B	AMD Ryzen Embedded V-series Processors	V-Series V1000	Zen
AMD Ryzen Embedded V1756B	AMD Ryzen Embedded V-series Processors	V-Series V1000	Zen
AMD Ryzen Embedded V1605B	AMD Ryzen Embedded V-series Processors	V-Series V1000	Zen

Model	Family	Line	uArch
AMD Ryzen Embedded V1202B	AMD Ryzen Embedded V-series Processors	V-Series V1000	Zen
V1202B	Ryzen Embedded		Zen
V1605B	Ryzen Embedded		Zen
V1756B	Ryzen Embedded		Zen
V1807B	Ryzen Embedded		Zen
3101	Epyc Embedded		Zen
3151	Epyc Embedded		Zen
3201	Epyc Embedded		Zen
3251	Epyc Embedded		Zen
3301	Epyc Embedded		Zen
3351	Epyc Embedded		Zen
3401	Epyc Embedded		Zen
3451	Epyc Embedded		Zen