

UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

AQUILA INNOVATIONS, INC., a	§	No. 1:18-cv-554-LY
Delaware corporation,	§	
	§	
Plaintiff,	§	
	§	
v.	§	
	§	
ADVANCED MICRO DEVICES, INC., a	§	
Delaware corporation	§	
	§	
Defendant.	§	

AQUILA INNOVATIONS, INC.'S OPENING CLAIM CONSTRUCTION BRIEF

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Pursuant to the Court’s Scheduling Order, ECF No. 36, Plaintiff Aquila Innovations Ltd. (“Aquila”) respectfully submits this opening claim construction brief in support of its proposed constructions for the terms identified in the Joint Claim Construction and Prehearing Statement for U.S. Patent 6,895,519 (“’519 patent”) and U.S. Patent 6,239,614 (“’614 patent”).

I. U.S. PATENT 6,895,519

A. Overview

The ’519 patent is entitled “System LSI.” The ’519 patent addresses a System On a Chip (System LSI) that dynamically controls its clocks in order to achieve power reduction.

B. “system LSI”

Aquila Construction	AMD Construction
“system on a chip”	“single integrated chip, which has a central processing unit, first memory, second memory, and I/O capability”

The ’519 patent claims priority to a Japanese patent application filed in February 2002. “System LSI” is a Japanese term of art used to refer to a “system on a chip,” and would be understood by a person having ordinary skill in the art to carry that meaning. Oklobdzija Decl. ¶¶ 27. The remainder of the preamble recites that the system LSI has ordinary and special operation modes, and a central processing unit. These elements do not require construction.

The “system on a chip” recited in the preamble of claim 1 is a single integrated chip, but there is no need to mention that in a construction. Claim construction “is not an obligatory exercise in redundancy.” *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997). There is also no need to mention “a central processing unit” because the preamble recites “a central processing unit.” The Court need not “repeat or restate every claim term.” *Id.* AMD’s construction of “system LSI” includes a CPU (mentioned in the preamble), first memory (not mentioned in the preamble, but mentioned in the body of the claim), and second memory (also

not mentioned in the preamble, but mentioned in the body of the claim). These elements are explicitly identified in the preamble or the body of the claim as elements of the “system on a chip,” and there is no need to mention them in a construction of the preamble.

“It is improper for a court to add ‘extraneous’ limitations to a claim, that is, limitations added ‘wholly apart from any need to interpret what the patentee meant by particular words or phrases in the claim.’” *Hoganas AB v. Dresser Indus.*, 9 F.3d 948, 950 (Fed. Cir. 1993) (citing *E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 1433 (Fed. Cir. 1988)). AMD’s inclusion of “I/O capability” is both unnecessary and extraneous. Neither claim 1 nor the specification requires that the system LSI have input or output capability. The purported I/O capability does not play a role in any other limitation of claim 1 or any of the other claims, and would simply be an extraneous limitation “wholly apart from any need to interpret what the patentee meant” by the term “system LSI.”

C. “plurality of standard clocks (claim 1)

Aquila Construction	AMD Construction
“multiple clock signals”	“multiple clock signals, each at a unique reference frequency”

The parties agree on the use of “multiple clock signals,” but dispute whether each of the multiple clock signals has a unique reference frequency. The “plurality of standard clocks” are the clock signals received by the “clock generation circuit” mentioned in the third element of claim 1. While the disclosed preferred embodiment has three oscillators, each of which generates a clock signal having a different frequency, nothing in the specification requires that each of the clock signals received by the “clock generation circuit” have a unique frequency. A person of skill in the art would understand that the “clock generation circuit” could also accept two clock signals having the same frequency, but different phases, or the clock signals from two crystals

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