David H. Albonesi

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Education

1996 Doctor of Philosophy, Computer Engineering, University of Massachusetts Amherst

1986 Master of Science, Electrical Engineering, Syracuse University

1982 Bachelor of Science, Electrical Engineering, University of Massachusetts Amherst

Professional Experience

2010- Professor, Electrical and Computer Engineering, Cornell University

2013-16 Associate Director, Electrical and Computer Engineering, Cornell University

2004-10 Associate Professor, Electrical and Computer Engineering, Cornell University

2001-04 Associate Professor, Electrical and Computer Engineering, University of Rochester

1996-2001 Assistant Professor, Electrical and Computer Engineering, University of Rochester

1993-96 Research Engineer, Electrical and Computer Engineering, University of Massachusetts
Digital systems consulting, system administration, and evaluation of benchmark performance of supercomputers and workstations.

1992-95 Lecturer, Electrical and Computer Engineering, University of Massachusetts
Revamped undergraduate digital design and microprocessor systems laboratory courses.

1986-92 Section Manager/Principal Engineer, Processor Development, Prime Computer, Inc.
Project manager and computer architect for high performance uniprocessor and multiprocessor designs implemented using CMOS and ECL technologies.

1982-86 Senior Associate Engineer, Memory Development, IBM Corporation
IBM 3090 mainframe main memory subsystem development including chip design and verification, circuit and board-level analysis, and hardware prototype debugging and integration with other subsystems.

Honors and Awards

IEEE Fellow

Three IEEE Micro Top Picks in Computer Architecture Awards

Three IBM Faculty Awards

NSF CAREER Award

MICRO Hall of Fame

Kenneth A. Goldman '71 Excellence in Teaching Award

Michael Tien '72 Excellence in Teaching Award

Ralph S. Watts '72 Excellence in Teaching Award

Ruth and Joel Spira Excellence in Teaching Award (twice)

IEEE Computer Society Golden Core Award

Prime Computer Patent Plateau Award

Two Prime Computer Excellence Awards

IBM Excellence Award

Book Chapters

"Alleviating Thermal Constraints while Maintaining Performance Via Silicon-Based On-Chip Optical Interconnects," N. Nelson, G. Briggs, M. Haurylau, G. Chen, H. Chen, D.H. Albonesi, E.G. Friedman, and P.M. Fauchet, *Unique Chips and Systems*, CRC Press, 2007.

"Power-Efficient Issue Queue Design," A. Buyuktosunoglu, D.H. Albonesi, S. Schuster, D. Brooks, P. Bose, P. Cook, in *Power Aware Computing*, R. Graybill and R. Melhem (Eds), Kluwer Academic Publishers, Chapter 3, pp. 37-60, 2002.

"Low-Voltage 0.25um CMOS Improved Power Adaptive Issue Queue For Embedded Microprocessors," B.W. Curran, M. Gifaldi, J. Martin, A. Buyuktosunoglu, M. Margala, and D.H. Albonesi, in *SOC Design Methodologies*, M. Robert, B. Rouzeyre, C. Piguet, and M.-L. Flottes (Eds), Kluwer Academic Publishers, 2002.

Journal Publications

"A Phase Adaptive Cache Hierarchy for SMT Processors," S. Lopez, O. Garnica, D.H. Albonesi, S. Dropsho, J. Lanchares, and J.I. Hidalgo, *Microprocessors & Microsystems*, Vol. 35, No. 8, pp. 683-694, November 2011.

"A Low Latency, High Throughput On-Chip Optical Router Architecture for Future Chip Multiprocessors," M.J. Cianchetti and D.H. Albonesi, *ACM Journal on Emerging Technologies in Computing Systems*, Special Issue on Nanophotonic Communication Technology Integration, Vol. 7, No. 2, June 2011.

"ReMAP: A Reconfigurable Architecture for Chip Multiprocessors," M.A. Watkins and D.H. Albonesi, *IEEE Micro*, Special Issue on the Top Picks from the Computer Architecture Conferences, pp. 65-77, January/February 2011 (IEEE Micro Top Picks).

"Addressing Thermal Non-Uniformity in SMT Workloads," J.A. Winter and D.H. Albonesi, *ACM Transactions on Architecture and Code Optimization*, Vol. 5, No. 1, May 2008.

"Predictions of CMOS Compatible On-Chip Optical Interconnect," G. Chen, H. Chen, M. Haurylau, N. A. Nelson, D. H. Albonesi, P. M. Fauchet, and E. G. Friedman, Integration, The VLSI Journal, Vol. 40, No. 4, pp. 434-446, July 2007.

"On-chip Optical Technology in Future Bus-based Multicore Designs: Opportunities and Challenges," N. Kırman, M. Kırman,, R.K. Dokania, J. Martínez, A.B. Apsel, M.A. Watkins, and D.H. Albonesi, *IEEE Micro*, Special Issue on the Top Picks from the Computer Architecture Conferences, pp. 56-66, January/February 2007 (IEEE Micro Top Picks).

"On-Chip Optical Interconnect Roadmap: Challenges and Critical Directions," M. Haurylau, G. Chen, H. Chen, J. Zhang, N.A. Nelson, D.H. Albonesi, E.G. Friedman, and P.M. Fauchet, *IEEE Journal of Selected Topics in Quantum Electronics*, Special Issue on Silicon Photonics, Vol. 12, No. 6, pp. 1699-1705, November/December 2006.

"Power Efficient Error Tolerance in Chip Multi-Processors," M.W. Rashid, E.J. Tan, M.C. Huang, and D.H. Albonesi, IEEE Micro, Special Issue on Reliability-Aware Microarchitectures, Vol. 25, No. 6, pp. 60-70, November/December 2005.

"Micro's Top Picks from Microarchitecture Conferences," D.H. Albonesi, *IEEE Micro*, Guest Editor's Introduction for Special Issue on Micro's Top Picks from Microarchitecture Conferences, Vol. 24, No. 6, pp. 8-9, November/December 2004.

"An Evaluation of a Configurable VLIW Microarchitecture for Embedded DSP Applications," W. Liu, D.H. Albonesi, J. Gostomski, L. Palum, D. Hinterberger, R. Wanzenried, and M. Indovina, *Journal of Circuits, Systems, and Computers*, Special Issue on VLSI Architectures for Multimedia Applications, Vol. 13, No. 6, pp. 1321-1345, December 2004.

"Dynamically Tuning Processor Resources with Adaptive Processing," D.H. Albonesi, R. Balasubramonian, S.G. Dropsho, S. Dwarkadas, E.G. Friedman, M.C. Huang, V. Kursun, G. Magklis, M.L. Scott, G. Semeraro, P. Bose, A. Buyuktosunoglu, P.W. Cook, and S.E. Schuster, *IEEE Computer*, Special Issue on Power-Aware Computing, Vol. 36, No. 12, pp. 49-58, December 2003.

"Dynamic Frequency and Voltage Scaling for a Multiple-Clock-Domain Microprocessor," G. Magklis, G. Semeraro, D.H. Albonesi, S.G. Dropsho, S. Dwarkadas, and M.L. Scott, *IEEE Micro*, Special Issue on the Top Picks from the Computer Architecture Conferences, Vol. 23, No. 6, pp. 62-68, November/December 2003 (IEEE Micro Top Picks).

"A Dynamically Tunable Memory Hierarchy," R. Balasubramonian, D.H. Albonesi, A. Buyuktosunoglu, and S. Dwarkadas, *IEEE Transactions on Computers*, Vol. 52, No. 10, pp. 1243-1258, October 2003.

"Power and Complexity Aware Design," P. Bose, D.H. Albonesi, and D. Marculescu, *IEEE Micro*, Guest Editors' Introduction for Special Issue on Power and Complexity Aware Design, Vol. 23, No. 5, pp. 8-11, September/October 2003.

"Selective Cache Ways: On-Demand Cache Resource Allocation," D.H. Albonesi, *Journal of Instruction-Level Parallelism*, Special Issue on the Best Papers from the *32nd International Symposium on Microarchitecture*, Vol. 2, 2000.

"Runtime Reconfiguration Techniques for Efficient General Purpose Computation," B. Xu and D.H. Albonesi, *IEEE Design & Test of Computers*, Special Issue on Configurable Computing, pp. 42-52, January-March, 2000.

"STATS: A Framework for Microprocessor and System-Level Design Space Exploration," D.H. Albonesi and I. Koren, *Journal of Systems Architecture*, Special Issue on Microprocessor Architecture, Vol. 45, No. 12-13, pp. 1097-1110, June 1999.

"A Mean Value Analysis Multiprocessor Model Incorporating Superscalar Processors and Latency Tolerating Techniques," D.H. Albonesi and I. Koren, *International Journal of Parallel Programming*, Special Issue on Parallel Architectures and Compilation Techniques, Vol. 24, No. 3, pp. 235-263, August 1996.

Refereed Conference and Workshop Publications

"Productively Generating High-Performance Spatial Hardware for Dense Tensor Computations," N. Srivastava et al., *27th International Symposium on Field-Programmable Custom Computing Machines*, April 2019.

"DeepRecon: Dynamically Reconfigurable Architecture for Accelerating Deep Neural Networks," T. Rzayev, S. Moradi, D.H. Albonesi, and R. Manohar, *International Joint Conference on Neural Networks*, May 2017.

"Toolbox for Exploration of Energy-Efficient Event Processors for Human-Computer Interaction," T. Rzayev, D.H. Albonesi, R. Manohar, F. Guimbretiere, and J. Kihm, *International Symposium on Performance Analysis of Systems and Software*, April 2017.

"Dynamic GPGPU Power Management using Adaptive Model Predictive Control," A. Majumdar, L. Piga, I. Paul, J.L. Greathouse, W. Huang, and D.H. Albonesi, *23rd International Symposium on High Performance Computer Architecture*, February 2017.

"Fractured Arithmetic Accelerator for Training Deep Neural Networks," T. Rzayev, S. Moradi, D.H. Albonesi, and R. Manohar, *Workshop on Hardware and Algorithms for On-chip Learning*, held at the *International Conference on Computer-Aided Design*, November 2016.

"Characterizing the Benefits and Limitations of Smart Building Meeting Room Scheduling," A. Majumdar, Z. Zhang, and D.H. Albonesi, *7th International Conference on Cyber-Physical Systems*, April 2016.

"Energy-Comfort Optimization using Discomfort History and Probabilistic Occupancy Prediction," A. Majumdar, J.L. Setter, J.R. Dobbs, B.M. Hencey, and D.H. Albonesi, *5th International Green Computing Conference*, November 2014.

"Flicker: A Dynamically Adaptive Architecture for Power Limited Multicore Systems," P. Petrica, A.M. Izraelevitz, D.H. Albonesi, and C.A. Shoemaker, *40th International Symposium on Computer Architecture*, pp. 13-23, June 2013.

"Energy-Aware Meeting Scheduling Algorithms for Smart Buildings," A. Majumdar, D.H. Albonesi, and P. Bose, *4th ACM Workshop On Embedded Systems For Energy-Efficiency In Buildings*, November 2012.

"ReMAP: A Reconfigurable Heterogeneous Multicore Architecture," M.A. Watkins and D.H. Albonesi, *43rd International Symposium on Microarchitecture*, pp. 497-508, December 2010.

"Scalable Thread Scheduling and Global Power Management for Heterogeneous Many-Core Architectures," J.A. Winter, D.H. Albonesi, and C.A. Shoemaker, *19th International Conference on Parallel Architectures and Compilation Techniques*, pp. 29-39, September 2010.

"Dynamically Managed Multithreaded Reconfigurable Architectures for Chip Multiprocessors," M.A. Watkins and D.H. Albonesi, *19th International Conference on Parallel Architectures and Compilation Techniques*, pp. 41-52, September 2010.

"Adaptive Cache Memories for SMT Processors," S. Lopez, O. Garnica, D.H. Albonesi, S. Dropsho, J. Lanchares, and J.I. Hidalgo, *13th Euromicro Conference on Digital System Design*, pp. 331-338, September 2010.

"Dynamic Power Redistribution in Failure Prone CMPs," P. Petrica, J.A. Winter, and D.H. Albonesi, *Workshop on Energy Efficient Design*, June 2010.

"Enabling Parallelization via a Reconfigurable Chip Multiprocessor," M.A. Watkins and D.H. Albonesi, *Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures*, June 2010.

"Phastlane: A Rapid Transit Optical Routing Network," M.J. Cianchetti, J.C. Kerekes, and D.H. Albonesi, *36th International Symposium on Computer Architecture*, pp. 441-450, June 2009.

"Shared Reconfigurable Architectures for CMPs," M.A. Watkins, M.J. Cianchetti, and D.H. Albonesi, *18th IEEE International Conference on Field Programmable Logic and Applications*, September 2008 (Best Paper Award Nomination).

"The Scalability of Scheduling Algorithms for Unpredictably Heterogeneous CMP Architectures," J.A. Winter and D.H. Albonesi, *Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures*, held at the *35th International Symposium on Computer Architecture*, June 2008.

"Scheduling Algorithms for Unpredictably Heterogeneous CMP Architectures," J.A. Winter and D.H. Albonesi, *38th International Conference on Dependable Systems and Networks*, pp. 42-51, June 2008.

"On-Chip Optical Interconnects: Challenges and Critical Directions," G. Chen, H. Chen, M. Haurylau, N.A. Nelson, D.H. Albonesi, P.M. Fauchet, and E.G. Friedman, *Proceedings of the European Optical Society Topical Meeting on Optical Microsystems*, p. 97, October 2007.

"On-Chip Optical Interconnect for Reduced Delay Uncertainty," G. Chen, H. Chen, M. Haurylau, N.A. Nelson, D.H. Albonesi, P.M. Fauchet, and E.G. Friedman, *Proceedings of Nano-Net*, September 2007.

"Dynamic Capacity-Speed Tradeoffs in SMT Processor Caches," S. Lopez, S. Dropsho, D.H. Albonesi, O. Garnica, and J. Lanchares, *International Conference on High Performance Embedded Architectures and Compilers*, pp. 136-150, January 2007.

"Leveraging Optical Technology in Future Bus-based Chip Multiprocessors," N. Kırman, M. Kırman,, R.K. Dokania, J. Martínez, A.B. Apsel, M.A. Watkins, and D.H. Albonesi, *39th International Symposium on Microarchitecture*, December 2006 (Best Paper Award Nomination).

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