Steven A. Przybylski

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Professional Experience

9/91 - Present

President and Principal Consultant, Verdande Group, Inc

I have consulted on product strategy, comparative technical analysis, and system-level design in the areas of DRAMs, Flash, SRAMs and other semiconductor memories, computer systems and CPU architecture, and uni- and multi-processor memory hierarchy design. Technical engagements have included serving as memory system architect for Flash and DRAM memory devices and systems. In addition, I offer: general business planning and analysis services to computer and semiconductor companies; intellectual property management, including portfolio evaluation, development and brokering, patent infringement and litigation support services to IP holders and legal firms; and due-diligence analyses to venture capitalists and securities firms.

I have written on a variety of topics for a broad spectrum of trade magazines and academic journals. As one of the leading independent analysts of the semiconductor memory industry, I wrote (1994) and substantially revised (1996) an 850-page research report entitled *New DRAM Technologies: A Comprehensive Analysis of the New Architectures,* available from the publishers of *The Microprocessor Report*. I have also taught and presented tutorials to both technical and non-technical audiences on subjects including semiconductor memory architecture, memory hierarchy design, and computer systems and CPU architecture. In particular, I have presented over 50 full- and partial-day seminars on these topics to over 2,500 managers, engineers, marketers, and analysts. I have also served on the advisory boards of high-technology start-ups, advising on processor, DRAM and Flash memory trends and general business opportunities.

1/00 - 12/03

Manager, SSM Technologies, LLC.

I managed, developed and ultimately sold a significant patent portfolio relating to DRAMs. I recognized the intrinsic value of a long-neglected portfolio, negotiated control of the portfolio, and developed a new patent prosecution strategy. I oversaw and participated in the implementation of this strategy, culminating in the issue of a new set of broad method and apparatus claims. I then worked to monetarize the portfolio and to maximize return to the inventors and SSM's investors by analyzing the sell/license decision and guiding the stakeholders through the decision-making process. In the end, I gathered relevant documentation and analyses, approached likely purchasers, presented interested parties with the collected materials, actively sold the offensive and defensive utility of the portfolio, and orchestrated an auction-style final sales process.

7/89 - 9/91

Chief Scientist and Systems Architect, MIPS Computer Systems.

I played a variety of roles within MIPS, including assistant to the Senior Vice President of Engineering, technical lead for a group of designers that investigated the technical and economic feasibility of developing a companion chip to the R3000 CPU and R3010 FPU, troubleshooter within the High-End Systems Group responsible for taking on any short or long term task that was in need of additional manpower, chief scientist for the group in charge of planning and investigating options for future high-end systems, systems architect for both a new R4000 based symmetrical multi-processor and a low-cost desk-top machine.

10/90 - 8/91

Consulting Assistant Professor, Dept. of Elect. Eng., Stanford University.

I designed and taught an advanced graduate level course on cache and memory hierarchy design and supervised the students' research activities. Two groups of students continued their research and ultimately published their efforts under my direction.

1/89 - 7/89	**Postdoctoral Scholar,** Department of Electrical Engineering, Stanford University.
	As a postdoctoral scholar, I continued my dissertation research into the analysis of cache behaviour and performance-optimal memory hierarchy design.

10/84 - 10/85	**Computer Architect and Systems Designer,** MIPS Computer Systems.
	My main contribution during MIPS' first year was the specification of the architecture and micro-organization of the R2000 VLSI RISC CPU, including the CPU interface and the cache subsystem. I was integrally involved in the implementation of both the CPU and system-level design. My most important role was that of liaison between the VLSI, board-level hardware, compiler and operating system teams.

10/81 - 9/88	**Research Assistant,** Department of Electrical Engineering, Stanford University.
	During my tenure at Stanford I was a key participant in the MIPS VLSI CPU design team, involved in the design, debugging and testing of the IC design. I also oversaw the development of a prototype CPU board, and I subsequently aided in the architectural specification of the MIPS-X VLSI CPU. My dissertation research used analytical and empirical techniques to examine memory hierarchy design from the perspective of optimizing system level performance.

Education

Haas School of Business, University of California at Berkeley, M.B.A. (2000).
With a combined emphasis on business strategy and financial analysis.

Stanford University, M.S.E.E. (1982), Ph.D. (1988).
Research areas: RISC computer architecture, VLSI integrated circuit design, and high performance single- and multi-level computer memory hierarchies. Course work concentrations: computer design, semiconductor devices, system software. Dissertation title: Performance-Directed Memory Hierarchy Design.

University of Toronto, B.A.Sc. with Honours (1980).
My personal variant of the Computer Science Option of the Engineering Science Programme was a combination of the computer science and electrical engineering degree programmes that specifically focused on computer systems and system software design.

Honours

Most Influential Paper Award, 16th Annual International Symposium on Computer Architecture, Presented jointly by the IEEE and the ACM, May 2004

Special Achievement Award, MIPS Computer Systems, May 1990.

J.W. Billes Entrance Scholarship, University of Toronto, 1976-1980.

1967 Science Scholarship, Natural Sciences and Engineering Research Council of Canada, 1980-1984, declined.

Publications

Awards

Most Influencial Paper Award , ACM/IEEE International Symposium on Computer Architecture, 1989, with Mark Horowitz and John Hennessy.

Micro Test-of-Time Award, for one of the ten most influential papers of the first 25 years of the IEEE Micro Symposium, with John hennessy, Normal Jouppi, Christopher Rowen, THomas Gross, Forest Baskett, and John Gill. 1994.

Books

S. Przybylski, *New DRAM Technologies*, MicroDesign Resources, 1996, 1994.

S. Przybylski. *Cache and Memory Hierarchy Design: A Performance-Directed Approach*, Morgan Kaufmann, 1990.

J. Hennessy, S. Przybylski. VLSI Processor Design Methodology. Chapter I in *VLSI Electronics, Microstructure Science,* Vol. 14, Einspruch, N. ed., Academic Press, 1986.

Journal Articles

T. Wada, et al. An Analytical Access Time Model For On-Chip Cache Memories, *Journal of Solid-State Circuits*, Vol. 27, No. 8, August 1992.

T. Gross, et al. Measurement and Evaluation of the MIPS Architecture and Processor. *ACM Transactions on Computer Systems,* Vol. 6, No. 3, August 1988.

M. Horowitz, et al. MIPS-X: A 20 MIPS Peak, 32-bit Microprocessor with On-Chip Cache. *Journal of Solid-State Circuits,* Vol. 22, No. 5, October 1987.

C. Rowen, et al. RISC VLSI Design for System-Level Performance. *VLSI Systems Design,* Vol. 7, No. 3, March 1986.

S. Przybylski, et al. The Organization and VLSI Implementation of MIPS. *Journal of VLSI and Computer Systems,* Vol. 1, No. 2, December 1984.

Other Articles

T. Gross, N. Jouppi, J. Hennessy, S. Przybylski, C. Rowen. A Retrospective on "MIPS: A Microprocessor Architecture", *IEEE Micro*, Vol. 36, No. 4, July/August, 2016.

R. Schuetz, H.J. Oh, J.-K. Kim, H.-B. Pyeon, S. Przybylski, P. Gillingham. HyperLink NAND Flash Architecture for Mass Storage Applications, 22nd IEEE Nonvolatile Semiconductor Memory Workshop (NVSMW), August 2007.

S. Przybylski, Intel's RDRAM Strategy a Sure Winner, *Microprocessor Report*, Vol. 11, No. 5, April 21, 1997

S. Przybylski, Intel's Gambles on a Sure Thing, *Electronic Engineering Times*, No. 947, March 31, 1997.

S. Przybylski, Will 1997 be the year of the 64-Mbit DRAM?, *Computer Design*, March 1997.

S. Przybylski, Combining DRAM and System Architecture, *OEM Magazine*, Vol. 4, No. 28, June, 1996.

S. Przybylski, SDRAMs Ready to Enter Mainstream, *Microprocessor Report*, Vol. 10, No. 6, May 6, 1996.

S. Przybylski, MoSys Reveals MDRAM Architecture, *Microprocessor Report*, Vol. 9, No. 17, December 25, 1995.

S. Przybylski, New DRAMs Improve Bandwidth, *Microprocessor Report*, Vol. 7, No. 2, February 15, 1993.

S. Przybylski, DRAMs for New Memory Systems *Microprocessor Report*, Vol. 7, No. 3, March 8, 1993.

S. Przybylski, DRAMs for New Memory Systems, *Microprocessor Report*, Vol. 7, No. 4, March 29, 1993.

S. Przybylski. The Performance Impact of Block Sizes and Fetch Strategies. 17th Annual International Symposium on Computer Architecture, May 1990.

S. Przybylski, J. Hennessy, M. Horowitz. Characteristics of Performance-Optimal Multi-Level Cache Hierarchies. 16th Annual International Symposium on Computer Architecture, June 1989.

S. Przybylski, M. Horowitz, J. Hennessy. Performance Tradeoffs in Cache Design. 15th Annual International Symposium on Computer Architecture. June 1988.

M. Horowitz, et al. A 12 MIPS 32b Microprocessor with On-Chip Cache. International Solid State Circuits Conference, February 1987.

J. Moussouris, et al. A RISC Microprocessor with Integral MMU and Cache Interface. International Conference on Computer Design (ICCD), October 1986.

J. Moussouris, et al. A CMOS RISC Processor with Integrated System Functions. Proceedings of

C. Rowen, et al. A Pipelined 32b nMOS Microprocessor. International Solid State Circuits Conference, February 1984.

S. Przybylski. The Design Verification and Testing of MIPS. MIT Conference on Advanced Research in VLSI, January 1984.

J. Hennessy, et al. Performance Issues in VLSI Processor Design. International Conference on Computer Design (ICCD), November 1983.

J. Hennessy, et al. Design of a High Performance VLSI Processor. Third Caltech Conference on VLSI, March 1983.

J. Hennessy, et al. MIPS: A Microprocessor Architecture. MICRO-15, October 1982.

Technical Reports

S. Przybylski. *Performance-Directed Memory Hierarchy Design.* Technical Report No. CSL-TR-88-366, Stanford University, September 1988.

S. Przybylski. *The Implementation of MIPS.* Internal Technical Report, Computer Systems Laboratory, Stanford University, August 1984.

J. Gill, et al. *Summary of MIPS Instruction.* CSL Technical Note No. 237, Computer Systems Laboratory, Stanford University, March 1983.

J. Hennessy, et al. *Hardware/Software Tradeoffs for Increased Performance.* CSL Technical Report No. 228, Computer Systems Laboratory, Stanford University, February 1983.

Tutorials, Seminars, and Session Chairs

PC System Architecture Trends, Panel member, 1999 Microprocessor Forum, San Jose, October 1999.

An Introduction to Semiconductor Memories, A Verdande Group presentation in cooperation with Citibank Inc, Taipei, Taiwan ROC, June 1998.

Embedded DRAMs: Today and Toward System-Level Integration, Half-day seminar. Presented more than 10 times to corporations between September 1997 and October 1999

The New DRAMs For Main Memory and Graphics, Full day Seminar, Verdande Group Seminar Series, Portland, Austin, San Jose, and Boston, September 1997.

Embedded DRAMs: Today and Toward System-Level Integration, Half-day seminar, Verdande Group Seminar Series, Portland, Austin, San Jose, and Boston, September 1997.

Sorting Out the New DRAMs, Half-Day Tutorial, Hot Chips IX, August 1997.

Embedded DRAMs: Today and Toward System-Level Integration, Half-day seminar, Presented at 24th Annual International Symposium on Computer Architecture, May 1997.

The New DRAMs For Main Memory and Graphics, Full day tutorial, 1997 PC Tech Forum, May 1997.

The New DRAM Architectures, DRAM Tutorial, 1996 ISSCC, February 1997.

Selecting the Best Memory Technology for PCs and Graphics, Full day tutorial, 1996 PC Tech Forum, May 1996.

The Changing DRAM and VRAM Marketplace, Full day tutorial, Presented more than 20 times to corporations between September 1995 and October 1999.

The Changing DRAM and VRAM Marketplace, Full day tutorial, Sponsored by Nikkei Microdevices, Tokyo, Japan, March 1996.

The Changing DRAM and VRAM Marketplace, Full day tutorial, 1995 Microprocessor Forum, October 1995.

Cache and Main Memory Options. Lecture. WinHEC, March 1995.

New Graphics Memories. Lecture. WinHEC, March 1995.

Emerging DRAM Architectures. Lecture. WinHEC, February 1994.

New DRAM Organizations. Session chair. Proceedings of COMPCON, Spring 1994.

Computer architecture and organization. Half-day tutorial. OCATE/Oregon State University, August 18, 1993.

DRAM Choices for the 1990s. Half-day tutorial. Hot Chips V, August 1993.

Computer Architecture. Full day tutorial with Normal Jouppi and Mark Horowitz. International Solid State Circuits Conference, February 1993.

Recent Trends in Processor Design, Reclimbing the Complexity Curve. Week-long course with Mark Horowitz and Mike Smith. Western Institute of Computer Science/Stanford University, August 1992 and August 1993.

Tracking the Processor-Memory Bandwidth Problem. Session chair, Microprocessor Forum, October 1992.

Patents

H. Pyeon, H. Oh, J.-K. Kim, S. Przybylski, *ID generation apparatus and method for serially interconnected devices*, Patent No. 8,984,249, March 17, 2015.

S. Przybylski, *Ring-of-clusters network topologies*, Patent No. 8,902,910, December 2, 2014.

S. Przybylski, R. Schuetz, H. Oh, H.B.Pyeon, *System having one or more memory devices*, Patent No. 8,812,768, August 19, 2014.

S. Przybylski, *Error detection and correction codes for channels and memories with incomplete error characteristics,* Patent 8,806,305, August 12, 2014.

J.-K. Kim, H. Oh, H.B. Pyeon, S. Przybylski. *Scalable Memory System.* Patent No. 8,671,252, March 11, 2014.

S. Przybylski, *Ring-of-clusters network topologies*, Patent No. 8,594,110, November 26, 2013.

S. Przybylski, *Error detection and correction codes for channels and memories with incomplete error characteristics*, Patent No. 8,429,495, April 23, 2013.

J.-K. Kim, H. Oh, H. Pyeon, S. Przybylski. *Scalable Memory System.* Patent No. 8,407,395, March 26, 2013.

L. Crudele, J. Moussouris, S. Przybylski. *System Having An Address Generating Unit and a Log Comparator Packaged as an Integrated Circuit Separate From Cache Log Memory and Cache Data Memory.* Patent No. 5,113,506, May 12, 1992.

L. Crudele, J. Moussouris, S. Przybylski. *CPU Chip Having Tag Comparator and Address Translation Unit on Chip and Connected to Off-Chip Cache and Main Memories.* Patent No. 4,953,073, August 28, 1990.

C. Hansen, S. Przybylski, T, Riordan, L. Weber. *Dual Byte Order Computer Architecture.* Patent No. 4,959,779, September 25, 1990.

Foreign counterparts of the above

Additional Information

Registered US Patent Agent, 1997 - present
Professional Societies: IEEE, ACM
Marital Status: Married with two children.
Citizenship: Canadian with resident alien status.