

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.
Petitioner

v.

AQUILA INNOVATIONS, INC.
Patent Owner

Case IPR2019-01525
U.S. Patent No. 6,239,614

**PETITIONER ADVANCED MICRO DEVICES, INC.'S
UPDATED EXHIBIT LIST**

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Petitioner submits this Updated Exhibit List to accompany submission of Exhibit 1051, Petitioner's Demonstratives for Oral Argument, in accordance with the Board's Order Setting Oral Argument (Paper 31).

PETITIONER'S UPDATED EXHIBIT LIST

Exhibit	Description
1001	U.S. Patent No. 6,239,614 to Morikawa ("614 patent")
1002	Prosecution History of U.S. Patent No. 6,239,614 ("614 Prosecution History")
1003	Declaration of Dr. Holberg in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 6,239,614 ("Holberg Decl.")
1004	Dr. Holberg's Curriculum Vitae
1005	Mutoh et al., "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 30, No. 8, 847-854 (1995) ("Mutoh")
1006	U.S. Patent No. 6,653,693 to Makino ("Makino")
1007	Japanese Patent Publication No. H10125878 to Masami Urano ("Urano")
1008	English translation of Urano
1009	Translation Certificate of Urano
1010	U.S. Patent No. 5,486,774 to Douseki <i>et al.</i> ("Douseki")
1011	U.S. Patent No. 5,631,492 to Ramus <i>et al.</i> ("Ramus")
1012	Japanese Patent Publication No. H0818021 to Shin'ichiro Mutoh <i>et al.</i> ("Mutoh021")
1013	English translation of Mutoh021

Exhibit	Description
1014	Translation Certificate of Mutoh021
1015	Declaration of Dr. Holberg in Support of District Court Case No. 1:18-cv-00554-LY (“Holberg Dec. 2”)
1016	Saigo et al., “A 20 K-Gate CMOS Gate Array,” <i>IEEE Journal of Solid State Circuits</i> , Vol. SC-18, No. 5, 578-584 (1983)
1017	Sato et al., “A Subnanosecond 2000 Gate Array with ECL 100K Compatibility,” Vol. ED-31, No. 2, 139-143 (1984)
1018	Masseti et al., “A CMOS-Based Mixed Analog-Logic Standard Cell Product Family,” <i>IEEE 1988 Custom Integrated Circuits Conference</i> , 24.1.1 (1988)
1019	Horowitz et al., “Chapter 2: Transistors,” <i>The Art of Electronics</i> , 2 nd Edition, Cambridge University Press (1989)
1020	U.S. Patent No. 4,001,869 to Brown (“Brown”)
1021	U.S. Patent No. 4,499,387 to Konishi (“Konishi”)
1022	U.S. Patent No. 5,544,102 to Tobita <i>et al.</i> (“Tobita”)
1023	U.S. Patent No. 6,285,052 to Draper (“Draper”)
1024	U.S. Patent No. 6,292,015 to Ooishi <i>et al.</i> (“Ooishi”)
1025	Baker et al., “CMOS Circuit Design, Layout, and Simulation” <i>Institute of Electrical and Electronics Engineers, Inc.</i> (1998)
1026	Sato et al., “A Subnanosecond 2000 Gate Array with ECL 100K Compatibility,” <i>IEEE Journal of Solid-State Circuits</i> , Vol. SC-19, No. 1, 5-9 (1984)
1027	Smith et al., “A CMOS-Based Analog Standard Cell Product Family,” <i>IEEE Journal of Solid-State Circuits</i> , Vol. 24, No. 2, 370-379 (1989)
1028	U.S. Patent No. 6,340,825 to Shibata (“Shibata”)

Exhibit	Description
1029	Scheduling Order, <i>Aquila Innovations, Inc. v. Advanced Micro Devices, Inc.</i> , Case No. 1:18-cv-00554-LY (W.D. Tex.), issued January 18, 2019
1030	Order Granting Unopposed Motion to Extend Claim Construction Deadlines, <i>Aquila Innovations, Inc. v. Advanced Micro Devices, Inc.</i> , Case No. 1:18-cv-00554-LY (W.D. Tex.), issued May 14, 2019
1031	Webster's Third New International Dictionary (2002)
1032	U.S. Patent No. 4,937,649 to Shiba <i>et al.</i> ("Shiba")
1033	U.S. Patent No. 6,459,331 to Takeuchi <i>et al.</i> ("Takeuchi")
1034	Weste, Neil H. E. et al., <i>Principles of CMOS VLSI Design</i> (2d ed. 1993) ("Weste")
1035	Laplante, P.A., <i>Comprehensive Dictionary of Electrical Engineering</i> (CRC Press 1999) ("Laplante")
1036	Graf, R.F., <i>Modern Dictionary of Electronics</i> (7th ed. 1999) ("Graf")
1037	Merriam-Webster's Collegiate Dictionary (10th ed. 2001)
1038	Cabe, Adam and Shamik Das, "Performance Simulation and Analysis of a CMOS/Nano Hybrid Nanoprocessor System," <i>Nanotechnology</i> , Vol. 20, No. 16, 22 (Apr. 2009) ("Cabe and Das")
1039	U.S. Patent No. 5,781,062 to Mashiko <i>et al.</i> ("Mashiko")
1040	U.S. Patent No. 5,933,384 to Terada <i>et al.</i> ("Terada")
1041	U.S. Patent No. 6,034,563 to Mashiko ("Mashiko1996")
1042	U.S. Patent No. 6,046,627 to Itoh <i>et al.</i> ("Itoh")

Exhibit	Description
1043	U.S. Patent No. 6,111,427 to Fujii <i>et al.</i> (“Fujii”)
1044	U.S. Patent No. 6,119,250 to Nishimura <i>et al.</i> (“Nishimura”)
1045	U.S. Patent No. 6,140,836 to Fujii <i>et al.</i> (“Fujii1998”)
1046	U.S. Patent No. 6,211,725 to Kang (“Kang”)
1047	Deposition Transcript of Dr. Przybylski
1048	Declaration of Dr. Holberg in Support of Petitioner’s Reply
1049	Chapter 13 of Microchip Fabrication by Van Zant from the 4 th Edition (2000)
1050	“Sea-of-gates architecture” by Manoel E.de Lima and David J.Kinniment, published on Microelectronics Journal Volume 26, Issue 5, July 1995
1051	Petitioner’s Demonstratives for Oral Argument

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Christopher R. O’Brien/

Date: December 8, 2020

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