Microelectronics Journal, 26 (1995) 431–440

Sea-of-gates architecture

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This paper deals with the development of sea-of-gates technology for the design of VLSI circuits. Sea-of-gates technology, also considered a second generation gate-array system, is discussed in detail. Its internal structure and the main physical aspects that differentiate sea-of-gates from conventional gate-arrays are presented. The advantages over the previous generation of gate-arrays, and for some circuits in comparison with full-custom technology, are discussed, together with its influence in the likely ASIC market.

1. Introduction

Since computers first began to be used to design chips more than 20 years ago, they have become essential for the design of complex circuits. With the rapid development of highly integrated electronic systems, more sophisticated software systems have also had to be produced in order to keep pace with the evolution of the technology. Today, large CAD systems contain millions of lines of code for the specification of state-of-the-art integrated circuits. Despite increasing complexity, the turnaround time for the layout of designs has been reduced from months and weeks to days and hours in recent CAD systems. This reduction in time is in part the result of the development in design styles that has taken place in the last few years, prompted by the need for more integration, higher density and greater flexibility. Among the design styles that have been applied to today's Application Specific Integrated Circuit (ASIC) projects, standard cell and gate-array technologies are good examples of the application of CAD in the ASIC industry. Semicustom technology has recently taken a considerable portion of this market, mainly as a result of its new member, the sea-of-gates, which has had a considerable impact on the architecture of the new generation of ASIC technology.

2. Semicustom technology

Semicustom technology [1] basically consists of wafer pre-processing up to the level of metallization patterning. This means that all transistors in the array matrix are pre-defined with fixed size and positions. Therefore, in general, the efficiency and performance may not be as good as that of full-custom designs, in which all devices are created specifically for a particular design. Full-custom technology [2] can result in higher area efficiency, and consequently a better speed and power consumption. Nevertheless, because of lower development costs and fast prototype turnaround time, semicustom methodology is an attractive option for many electronic systems requiring small or medium volume production.

0026–2692/95/$9.50

Within the semicustom family, a new class of gate-array, the sea-of-gates, has received considerable attention in the last few years because it offers more flexibility and higher density than conventional arrays. As a result, it has become one of the most popular components in this class. The sea-of-gates architecture, which employs a complete carpeting of gates in the core area of the chip, has now become dominant in the implementation of large-scale systems on gate-array architectures. Intense competition and short product lifecycles have created enormous pressure on the time needed for development and manufacture, and sea-of-gates has become a useful technology for companies which require speed, good performance, low cost and high density in their ASIC designs [3–5].

3. Sea-of-gates

Sea-of-gates (SOG) technology was introduced in around 1982 to provide a topology that allowed more flexibility in layout between channels and gates [6–17]. Considered to be the second generation of gates-arrays, sea-of-gates arrays can also be called 'continuous gate arrays', 'channelless arrays' or 'gate forest arrays'. The technique provides an implementation environment with the characteristics of both full custom and semicustom designs, offering the low cost and speed of semicustom gate arrays in fabrication and design time [2, 18, 19], and retaining some of the density and performance of full custom technology.

Since the basic pitch of transistors in silicon is different and denser in sea-of-gates than in conventional arrays, this technology requires more sophisticated methods to cope with its layout. Also, with the possibility of two or more metal layers for routing, and the use of sub-micron CMOS technology, even more dense and integrated systems will be possible, demanding more power from each of the layout tools and better integration between the traditional stages of the layout synthesis, i.e., partitioning, floorplanning, placement and routing.

This new generation of gate-arrays has promoted a substantial advance in semicustom design in the VLSI system integration world, allowing circuits to be built of the order of more than 1,000,000 gates per chip, a number which it is estimated may grow to around 20,000,000 by the year 2000. Sea-of-gates gives a similar density but greater flexibility compared to that achieved in full custom design, mainly because it is possible to use almost 100% of the silicon area in regular structures such as memories or PLAs.

Because of its density and flexibility, the inherent hierarchy of circuits can be more easily exploited. This is a very important feature, since a semicustom environment usually has a reduced layout flexibility when compared to the full custom environment. A designer can now exploit this flexibility at higher levels, to improve the speed of the design and produce more dense and regular circuits [7].

Two basic and important concepts are the heart of the modern sea-of-gates technology: removal of the conventional channels for routing [5, 6, 19–26] and gate isolation (GIC)[21–23, 27, 28]. These two characteristics are the keys for the density and flexibility of this new member of the gate-array family.

3.1 Channelless architecture

Conventional gate-array architecture uses channels, which appear as wide gaps between the rows, to allow enough space for inter- and intracell routing. The interconnections are done by processing the metal layer patterning of the logic gates that comprise the matrix of gates. The channels in the gate-array technology can be positioned either between the rows or columns, as shown in Fig. 1a. In general, two levels of interconnections are used for orthogonal tracking (vertical and horizontal routing). A third

level can also be used in some cases for power and ground. Because of the extra space reserved for these routing channels, some silicon is not used for active devices. Consequently, there may be a low density of circuits on the silicon.

The new concept in gate arrays, called channelless, as depicted in Fig. 1b, shows that the new generation of gates-arrays does not contain pre-defined wiring channels between cells for the custom metallization. The whole area of the die is now filled with potentially active p- and n-channel transistors, and the interconnections are made by metal layers over unused transistors. The routing process and device connections generally employ two-sided metallization in rows and columns that run above the transistors, and are isolated from them by an insulating material. These levels are implemented with the connections spaced on a grid where the centres of the contacts holes (vias) are located on the grid points. The metal layers usually have a preferential direction on each level. Depending on the technology used, sea-of-gates can also provide more than two metal layers for routing. For instance, in a three metal layers technology, the first metal layer could be used for building up the basic logic elements (intra-cell connections), and the second and third layers to perform the vertical and horizontal routing among the logic functions (inter-cell connection) or power distribution. This arrangement has been used to improve the efficiency for the router [7, 19]. The new technology allows highly integrated circuits to be built, offers fast turnaround and good performance.

3.2 Gate isolation

The second important concept, gate isolation, consists of replacing the field oxide usually providing the isolation between basic cells in a conventional gate-array by transistors. Figure 2 shows a typical NAND gate that is implemented on a conventional gate array (Fig. 2a) and on a channelless configuration (Fig. 2b).

In a conventional architecture, common gates are used to control the data flow on both n and p transistors which are grouped in a pre-determined number to create the basic cell in the array. Furthermore, the oxide isolation, which is also used in some sea-of-gates architectures, is employed to separate the basic cells on the array, thus increasing the gate area and giving a low density on the chip. However, with the gate isolation technique, no gap in diffusion layers isolating a cell from the other neighbouring ones

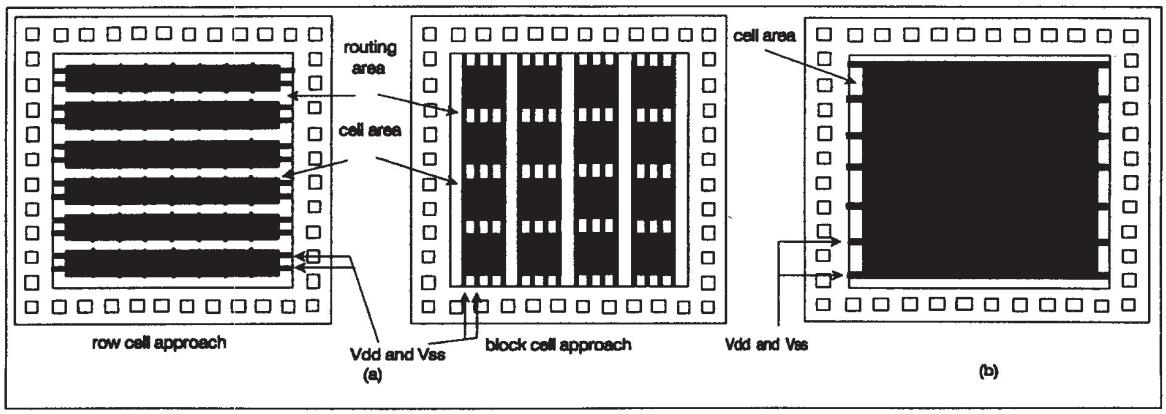

Fig. 1. Gate-array architecture. (a) Conventional gate-array architecture; (b) sea-of-gates architecture.

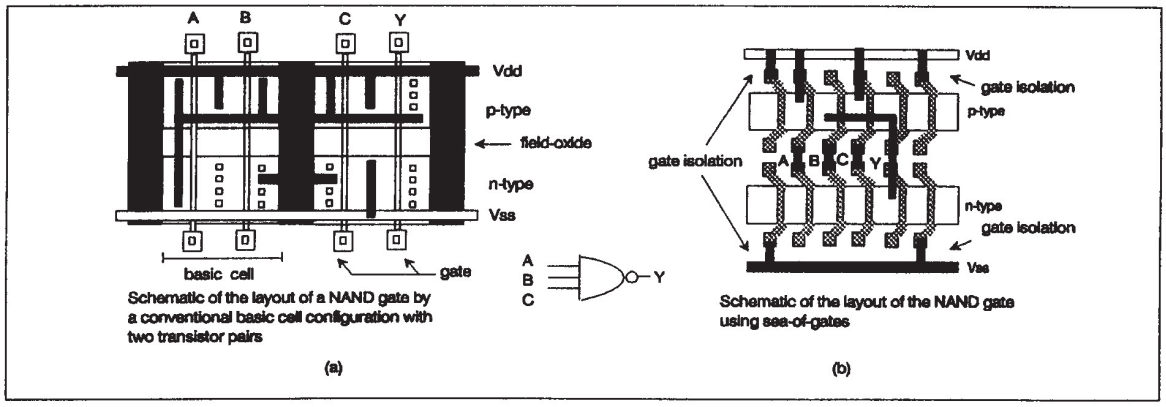

Fig. 2. Conventional and sea-of-gates arrays architecture. (a) Conventional gate-array architecture; (b) sea-of-gates architecture.

exists, and continuous p and n transistor chains can be created in the silicon die without interruptions (Fig. 2b).

Gate isolation is only provided where necessary, and it is done by a transistor gate connected to the appropriated power line (V_{SS} or V_{DD}), setting the respective transistors in a cut-off state. Hence, the transistors are isolated to help create the circuit required. The main advantages of this technology are:

- significant increase in transistor packing density,
- less wiring when creating complex functions, and
- easy control of the data flow.

Moreover, because the transistors have different gates, these gates can be used separately in order to implement different logic, or for facilitating the routing to critical areas of the chip.

In recent sea-of-gates architectures, these two techniques, channelless layout and gate isolation, have been used together, thus improving the flexibility, density and routability of the circuits and achieving a significantly reduced final area [8, 29].

4. Sea-of-gates styles

In a sea-of-gates architecture, the macrocells are composed by repeating basic cell boundaries horizontally or vertically on either a Row Macrocell (RMC) approach (Fig. 3a) or a Column Macrocell (CMC) approach (Fig. 3b) [29, 30] until enough gates are assembled. These two techniques provide different feed-through capabilities and different penalties for the vertical and horizontal routing. The terms 'macrocell' and 'functional cell' are here used to designate large cells with a certain logic function whose shape and area must be considered in the placement of the cells in the array.

4.1 The RMC architecture

With the RMC architecture, the basic cell is usually represented by a single vertical pair or pairs of transistors, as depicted in Fig. 3a. The macrocell in this architecture is implemented by repeating the basic cell along the horizontal direction until enough gates are allocated to the macrocell. In this technique, primitive cells such as gates NAND, XOR, etc., which are placed closely to create macrocells, do not have, in

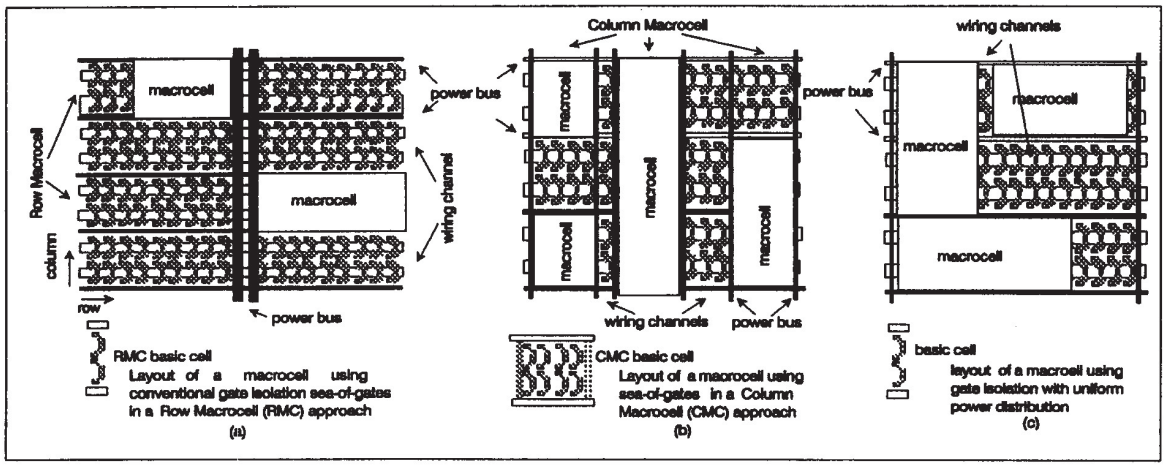

Fig. 3. Sea-of-gates architectures. (a) Layout of a macrocell using conventional gate isolation sea-of-gates in a Row Macrocell (RMC) approach; (b) layout of a macrocell using sea-of-gates in a Column Macrocell (CMC) approach; (c) layout of a macrocell using gate isolation with uniform power distribution.

general, enough feed-through to provide the intra-cell connections and so guarantee the routability of the circuits. As a result of this strategy, horizontal wiring channels are required to supply extra free tracks for routing. The allocation of free tracks in the congested area varies by one basic cell (BC) row pitch in this structure. This number of free tracks per row, which depends upon the technology used, can represent an increment of 13, 15, 20 tracks, etc. In the worst case, one BC row is allocated for each single track shortage, causing a low transistor utilization. This architecture does not have the capacity to distribute mesh power because of its variable-width structure horizontally and an insufficiency of feed-through tracks. Power distribution is therefore needed among the macrocells, which promotes difficulties in the routing, as illustrated in Fig. 3a.

To increase the gate utilization, a low increment in the number of tracks per basic cell is needed. Finally, using the RMC architecture, the arrangement of big cells such as memories and large macrocells is restricted to being located between the power buses.

4.2 The CMC architecture

On the other hand, in the CMC architecture the basic cells can have different sizes and also different sets of p and n transistors involving different numbers of transistors, as shown in Fig. 3b. The number of transistors must be well chosen in order to allow the ready implementation of gates in the system library.

In this approach, the macrocells are in general created by joining basic cells vertically, until enough gates are gathered together to form the macrocells. Because of the regularity of the basic cell distribution in a CMC architecture on the silicon die, it is possible to have a fine mesh power distribution in the array [31]. In this architecture, the wiring channels, created in a congested area, run vertically along the gates, providing the numbers of tracks needed for routing. The width of the channels, in contrast to the RMC, can change smoothly by the width of one column of pn transistors to provide the routing tracks, hence eliminating a big waste of silicon, and consequently providing a high utilization of gates in the circuit.

4.3 An alternative architecture

Although both of the above architectures use gate isolation, the idea of a completely channelless layout seems not to be 100% implemented. Another architecture offers rather more flexibility in the design, as depicted in Fig. 3c. In this structure, the macrocells can grow in both directions without restriction in the routing of the power supply, since it is distributed along the circuit using a second level of metal when needed. In this architecture, the isolation gate approach can be totally exploited, since there is always a continuous sequence of transistors without limits for all macrocells. Despite the advantages and disadvantages in different sea-of-gates architectures, a good result in the final layout also depends critically upon the algorithms used for partitioning, placement and routing [7, 25, 28, 32–34] of the circuits and the number of metal layers availbale for routing.

5. Microarchitectures and macroarchitectures

In terms of the internal structure of basic cells and their distribution on the silicon, sea-of-gates can be classified hierarchically at two levels; namely microarchitectures and macroarchitectures.

5.1 Microarchitecture

This level describes the internal characteristics of the core cells, which are used to build the overall structure of the array. These core cells (often basic cells) which are a combination of a certain number of p and n transistors, can be connected in different configurations, depending on the technology adopted.

A good example of a simple sea-of-gate's structure using gate isolation is that developed at Delft University, called Fishbone [8]. This structure is very similar to most of the sea-of-gates basic cells. This particular architecture uses gate-isolation in a 1.6 μm CMOS process with two layers of metal for routing. As depicted in Fig. 4a, each basic cell is composed of a pair of transistors using a traditional configuration, where the transistors are positioned horizontally creating a continuous row of transistors with the gates positioned vertically. Similar architectures can be found elsewhere [6, 8, 9, 11, 15, 17, 19–23, 26, 29–31, 35].

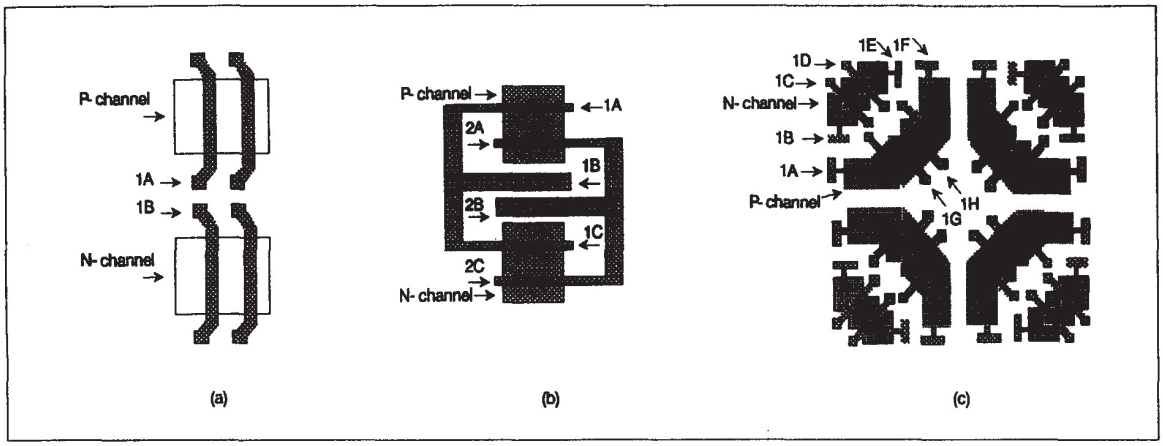

Fig. 4. Sea-of-gates microarchitecture. (a) Fishbone structure, 1A, 1B represent the transistor gates; (b) interleaved structure, 1A, 1B, 1C, 2A, 2B, 2C represent the transistor gates; (c) octagon structure, 1A, 1B, 1C, 1D, 1E, 1F, 1G, 1H represent the transistor gates.

New microarchitectures, however have recently appeared, presenting other advantages and new layout options for the sea-of-gates approach, for instance, the interleaved sea-of-gates image [37]. This new architecture, S-MOS interleaved sea-of-gate's architecture, presents a basic cell configuration composed of four two-layer metal CMOS gate arrays, in which the p- and n-channel source/drain regions and gate are laid out in parallel, as depicted in Fig. 4b. This parallelism facilitates the cell interconnections that can be performed through straight lines over the cells without the need for changing metal direction, hence and so using only a single layer of metal. As compared with a conventional sea-of-gates basic cell architecture, diffusion regions, both p- and n-channels, are slightly wider in the horizontal direction, and polysilicon gates 1A to 1C and 2A to 2C are not vertical in the column direction. The S-MOS interleaved architecture also claims to offer a good answer for dense and large circuits, with a high percentage of gate utilization, leaving at least 70% of the routing resources for global routing.

Another powerful new sea-of-gates architecture is the octagon image [8]. This architecture presents a very regular and symmetrical structure in which the transistors are not arranged entirely in a single vertical or horizontal sequence, but symmetrically distributed as in an octagon. The cells in this structure can also be mirrored regarding the 45° mirror axis. Octagon image uses three levels of metal in a 0.8 μm CMOS process. As depicted in Fig. 4c, each basic cell is composed of four groups of four pairs of transistors, symmetrically positioned. The gates are separated as a fishbone structure (1A to 1H).

5.2 Macroarchitecture

This is the higher level, in which the macrocells will be created as a combination of core cells. It is basically characterized by the number of core cells used to build the macro-architecture (macro-RAM block, multiplier, and so on), and the distribution of functions that deal with the distribution of the core cell on the master image (Fig. 5). The macroarchitecture can be further divided into three sub-groups:

- *Uniform distribution* – in this approach, the distribution function is combined with one or more basic cells, so as to build all possible functional cells into the array (Fig. 5a).
- *Channel distribution function* – this style is similar to the older gate array architecture, in

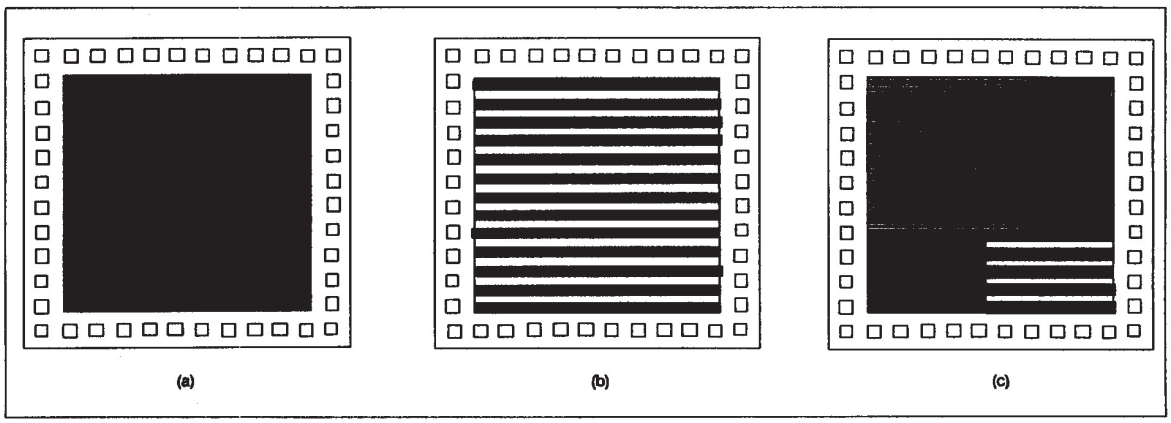

Fig. 5. Sea-of-gates macroarchitectures. (a) Uniform distribution function; (b) channel distribution function; (c) block distribution function.

which channels were defined to support routing. In general, this kind of architecture comprises either one or more cores to support the distribution functions (Fig. 5b).

- *Block distribution function* – still largely used. In this approach, the distribution functions are used almost solely as a combination of two or more core cells (Fig. 5c). The different core cells could be used to implement different functions such as memory, analogue circuits, and so on.

Because of the use of more than one core cell and different distribution function(s), the applicability of micro- and macro-architecture becomes limited, directly influencing the flexibility of the placement of the functional cells on the array. Recent sea-of-gates architectures [29, 31, 36, 37] have used just a single core cell to generate all the macro-architectures without routing channels. This approach allows the implementation of different design styles, supporting, for instance, dynamic and static libraries [35], and analogue circuits [23] in a homogeneous environment. The designer is now able to build up circuits which can share the regular structure, together with the placing of random logic blocks anywhere on the array [8, 22, 37, 38] without suffering substantial disadvantages.

Taken together, these new architectures and the evolution of CAD tools has motivated a massive increase in the use of cell-based design using sea-of-gates. Currently, a designer can choose functional cells of varied complexity, which are predefined and pre-characterized in system libraries. These libraries can support different design styles, as follows:

- *Standard cells (static or dynamic libraries)* – We can compare these to the traditional CMOS families like 74C00. However, rather than selecting packaged devices from a catalogue, they are chosen from software libraries contained in a CAD system, and placed on a silicon slice rather than a PCB. Many other logic combinations can be provided to optimize the integration of the circuits.

- *General cells* – Also called parameterized cells (paracells) these cells, which usually involve a very regular structure, are generated by software in different sizes according to the need of the circuits. Examples of this class of cells are RAMs, ROMs, PLAs, multipliers, adders, and so on.

- *Supracells* – also known as megacells, these are larger unparameterized macrocells, such as microprocessors, A/D converters, and so on.

Because of this wide range of possibilities in the physical layout of sea-of-gates, new tools have to be developed to deal with the extra complexity and high level of integration required. One of the most difficult problems for the layout of sea-of-gates is that there is no easy way to move the cells once placed in the array. This flexibility in placement can be very important, and heuristics should be developed to deal with the need to look ahead to later stages of the layout, such as global and detailed routing, considering free space available for routing, congestion, and so on, thus optimizing the silicon area available to guarantee the routability at every stage of the design.

6. Conclusion

Sea-of-gates is one of the most important microelectronic design styles to appear in recent years. Due to its flexibility and density, it is an ideal solution for highly-integrated systems that require a low and medium volume production. With the industry offering sea-of-gates arrays with over a million transistors, it is possible to implement complete systems or powerful microprocessors in a single array, with a density comparable in some cases to a full-custom style.

Acknowledgments

This work was supported by the Federal Brazilian Agency for Post-Graduate Education, CAPES, Brazil.

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