

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.
Petitioner

v.

AQUILA INNOVATIONS, INC.
Patent Owner

Case IPR2019-01525
Patent 6,239,614 B1

PETITION FOR *INTER PARTES* REVIEW

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TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	MANDATORY NOTICES	4
	A. Real parties-in-interest	4
	B. Notice of related matters	4
	C. Lead and back-up counsel with service information	4
III.	GROUNDS FOR STANDING.....	5
IV.	IDENTIFICATION OF CHALLENGE	5
V.	THE '614 PATENT.....	7
	A. Technical Background.....	7
	B. The Alleged Problem in the Prior Art.....	11
	C. The Alleged Invention of the '614 Patent.....	11
	D. Summary of the Prosecution History	14
VI.	LEVEL OF ORDINARY SKILL IN THE ART.....	14
VII.	CLAIM CONSTRUCTION	15
VIII.	OVERVIEW OF THE APPLIED REFERENCES	25
	1. Overview of Urano.....	25
	2. Overview of Mutoh021.....	26
	3. Overview of Mutoh.....	29
	4. Overview of Douseki	31
	5. Overview of Ramus	33

*Petition for Inter Partes Review of
U.S. Patent No. 6,239,614*

EXHIBIT LIST

Exhibit	DESCRIPTION
1001	U.S. Patent No. 6,239,614 to Morikawa (“614 patent”)
1002	Prosecution History of U.S. Patent No. 6,239,614 (“614 Prosecution History”)
1003	Declaration of Dr. Holberg in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 6,239,614 (“Holberg Decl.”)
1004	Dr. Holberg’s Curriculum Vitae
1005	Mutoh et al., “1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS,” <i>IEEE Journal of Solid-State Circuits</i> , Vol. 30, No. 8, 847-854 (1995) (“Mutoh”)
1006	U.S. Patent No. 6,653,693 to Makino (“Makino”)
1007	Japanese Patent Publication No. H10125878 to Masami Urano (“Urano”)
1008	English translation of Urano
1009	Translation Certificate of Urano
1010	U.S. Patent No. 5,486,774 to Douseki <i>et al.</i> (“Douseki”)
1011	U.S. Patent No. 5,631,492 to Ramus <i>et al.</i> (“Ramus”)
1012	Japanese Patent Publication No. H0818021 to Shin’ichiro Mutoh <i>et al.</i> (“Mutoh021”)
1013	English translation of Mutoh021
1014	Translation Certificate of Mutoh021
1015	Declaration of Dr. Holberg in Support of District Court Case No. 1:18-cv-00554-LY (“Holberg Dec. 2”)
1016	Saigo et al., “A 20 K-Gate CMOS Gate Array,” <i>IEEE Journal of</i>

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Exhibit	DESCRIPTION
	<i>Solid State Circuits</i> , Vol. SC-18, No. 5, 578-584 (1983)
1017	Sato et al., “A Subnanosecond 2000 Gate Array with ECL 100K Compatibility,” Vol. ED-31, No. 2, 139-143 (1984)
1018	Massetti et al., “A CMOS-Based Mixed Analog-Logic Standard Cell Product Family,” <i>IEEE 1988 Custom Integrated Circuits Conference</i> , 24.1.1 (1988)
1019	Horowitz et al., “Chapter 2: Transistors,” <i>The Art of Electronics</i> , 2 nd Edition, Cambridge University Press (1989)
1020	U.S. Patent No. 4,001,869 to Brown (“Brown”)
1021	U.S. Patent No. 4,499,387 to Konishi (“Konishi”)
1022	U.S. Patent No. 5,544,102 to Tobita <i>et al.</i> (“Tobita”)
1023	U.S. Patent No. 6,285,052 to Draper (“Draper”)
1024	U.S. Patent No. 6,292,015 to Ooishi <i>et al.</i> (“Ooishi”)
1025	Baker et al., “CMOS Circuit Design, Layout, and Simulation” <i>Institute of Electrical and Electronics Engineers, Inc.</i> (1998)
1026	Sato et al., “A Subnanosecond 2000 Gate Array with ECL 100K Compatibility,” <i>IEEE Journal of Solid-State Circuits</i> , Vol. SC-19, No. 1, 5-9 (1984)
1027	Smith et al., “A CMOS-Based Analog Standard Cell Product Family,” <i>IEEE Journal of Solid-State Circuits</i> , Vol. 24, No. 2, 370-379 (1989)
1028	U.S. Patent No. 6,340,825 to Shibata (“Shibata”)
1029	Scheduling Order, <i>Aquila Innovations, Inc. v. Advanced Micro Devices, Inc.</i> , Case No. 1:18-cv-00554-LY (W.D. Tex.), issued January 18, 2019
1030	Order Granting Unopposed Motion to Extend Claim Construction

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