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Fujii et al.

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[54] **SELF-TIMED PIPELINED DATAPATH SYSTEM AND ASYNCHRONOUS SIGNAL CONTROL CIRCUIT**

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[21] Appl. No.: **09/033,850**

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[30] **Foreign Application Priority Data**

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[51] **Int. Cl.**[7] **H03K 17/23**

[52] **U.S. Cl.** **326/35**; 326/93; 326/121; 326/112

[58] **Field of Search** 326/46, 35, 36, 326/93, 96, 112, 119, 120, 121

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Assistant Examiner—Don Phu Le
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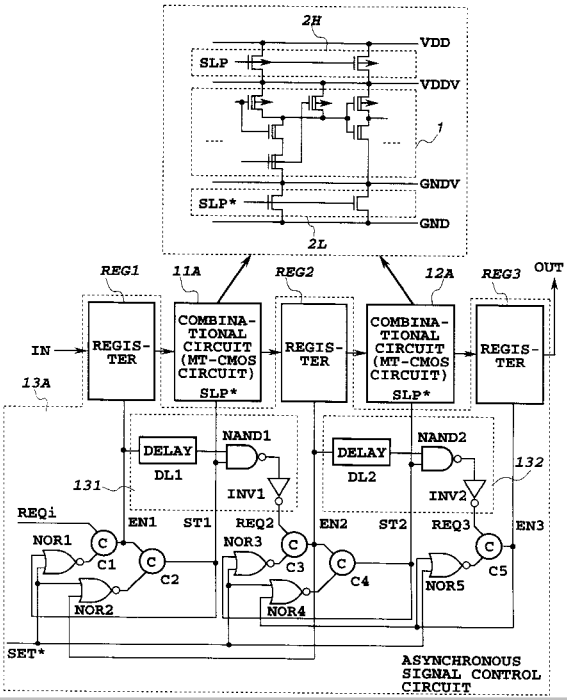
[57] **ABSTRACT**

A self-timed pipelined datapath system reduces its power dissipation by accurately controlling the active and inactive states of the multi-threshold CMOS (MT-CMOS) circuit used as its combinational circuit. The MT-CMOS circuit comprises a logic circuit of low-threshold and a power control circuit formed of high-threshold transistors for controlling the power feeding to the logic circuit. The self-timed pipelined datapath system comprises: a pipelined datapath circuit including a plurality of data processing stages, each having a combinational circuit for processing input data and a register connected to the input side of the combinational circuit; and an asynchronous signal control circuit that controls data transmission to and from each of the registers in the pipelined datapath circuit in response to a request signal. The state change of an active state to an inactive state of the combinational circuit is performed in consideration of the signal propagation time therein, whereby the issue of the request signal with respect to the combinational circuit at the preceding stage is delayed from the time the request signal with respect to the current combinational circuit is issued.

11 Claims, 13 Drawing Sheets



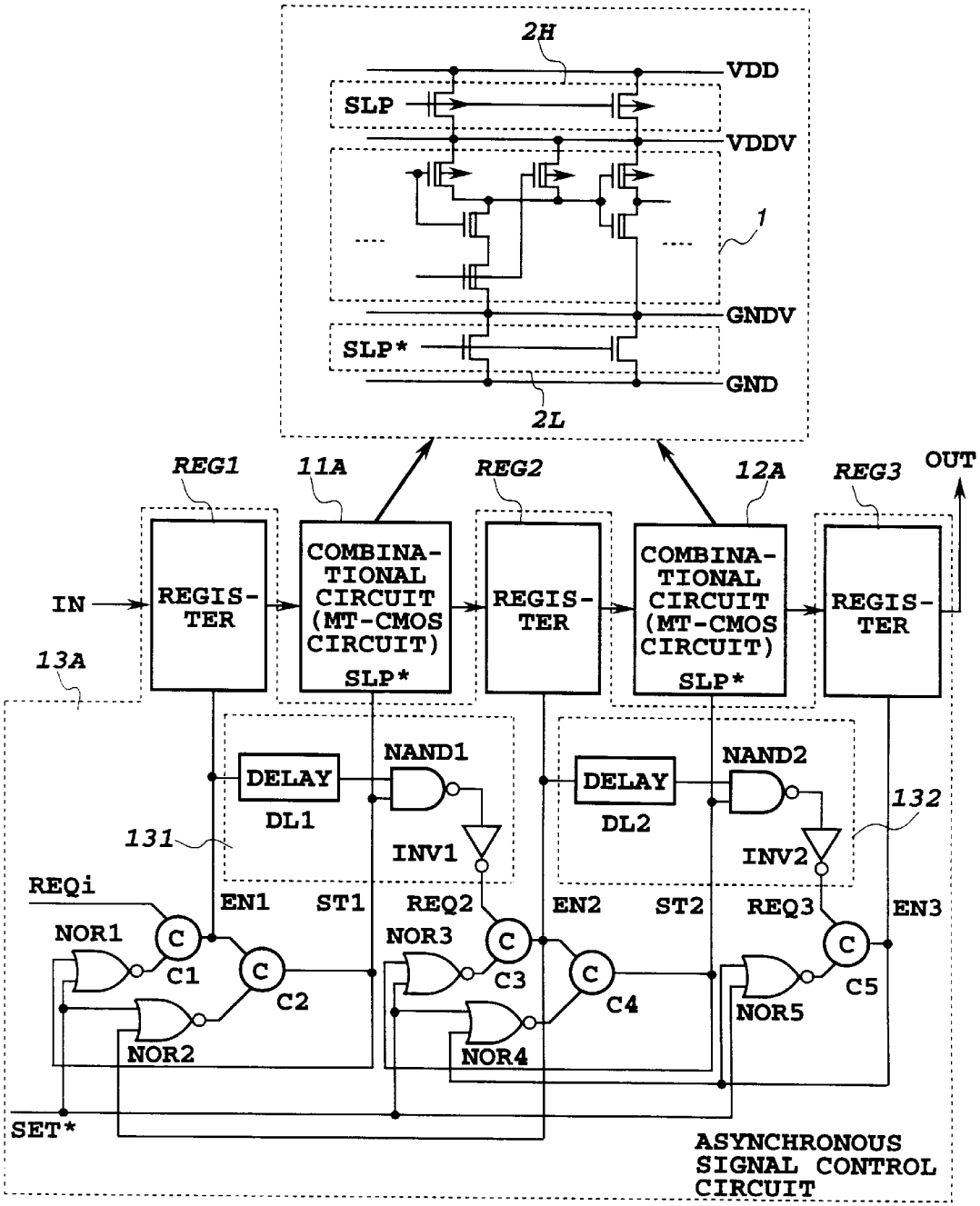


FIG.1

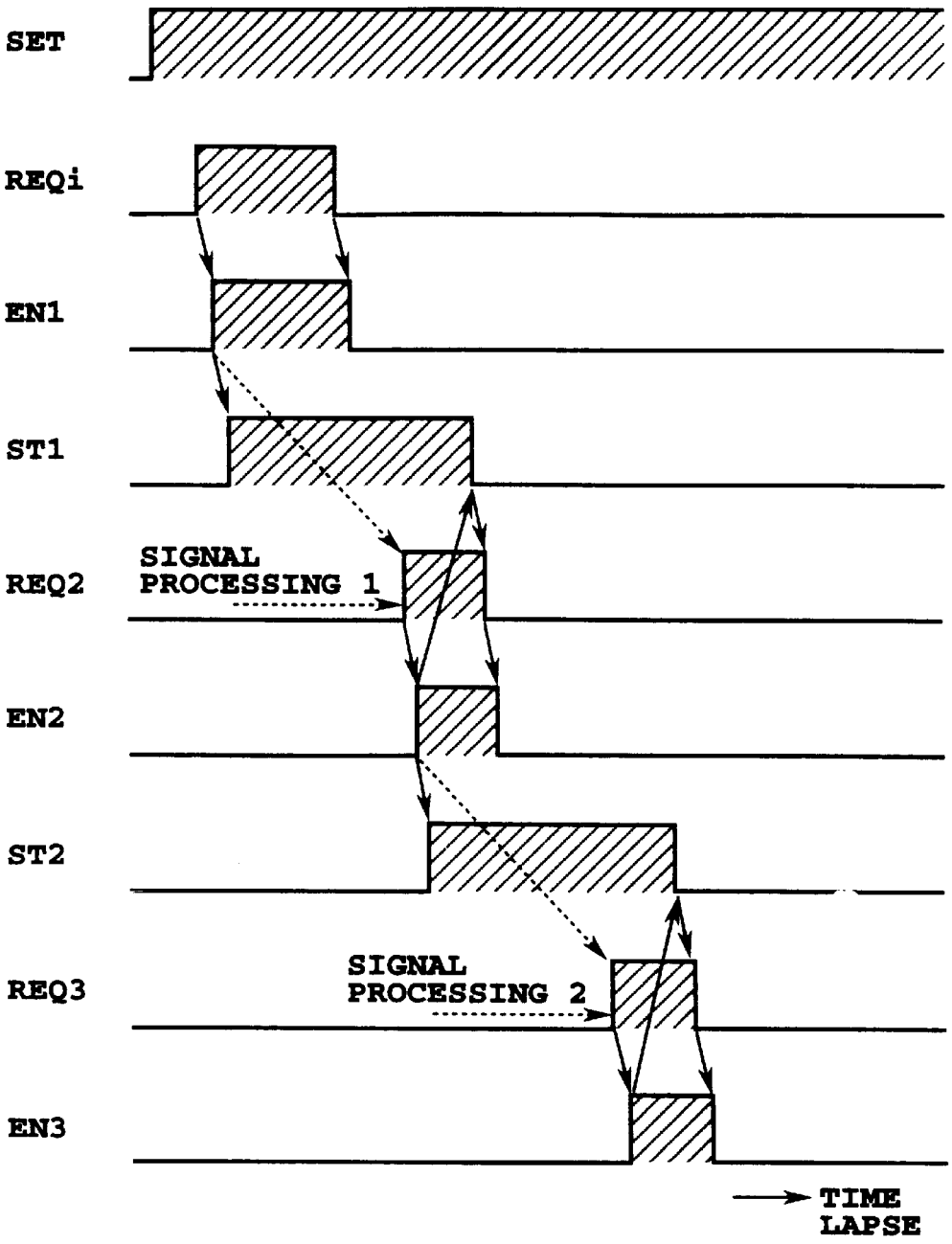


FIG.2

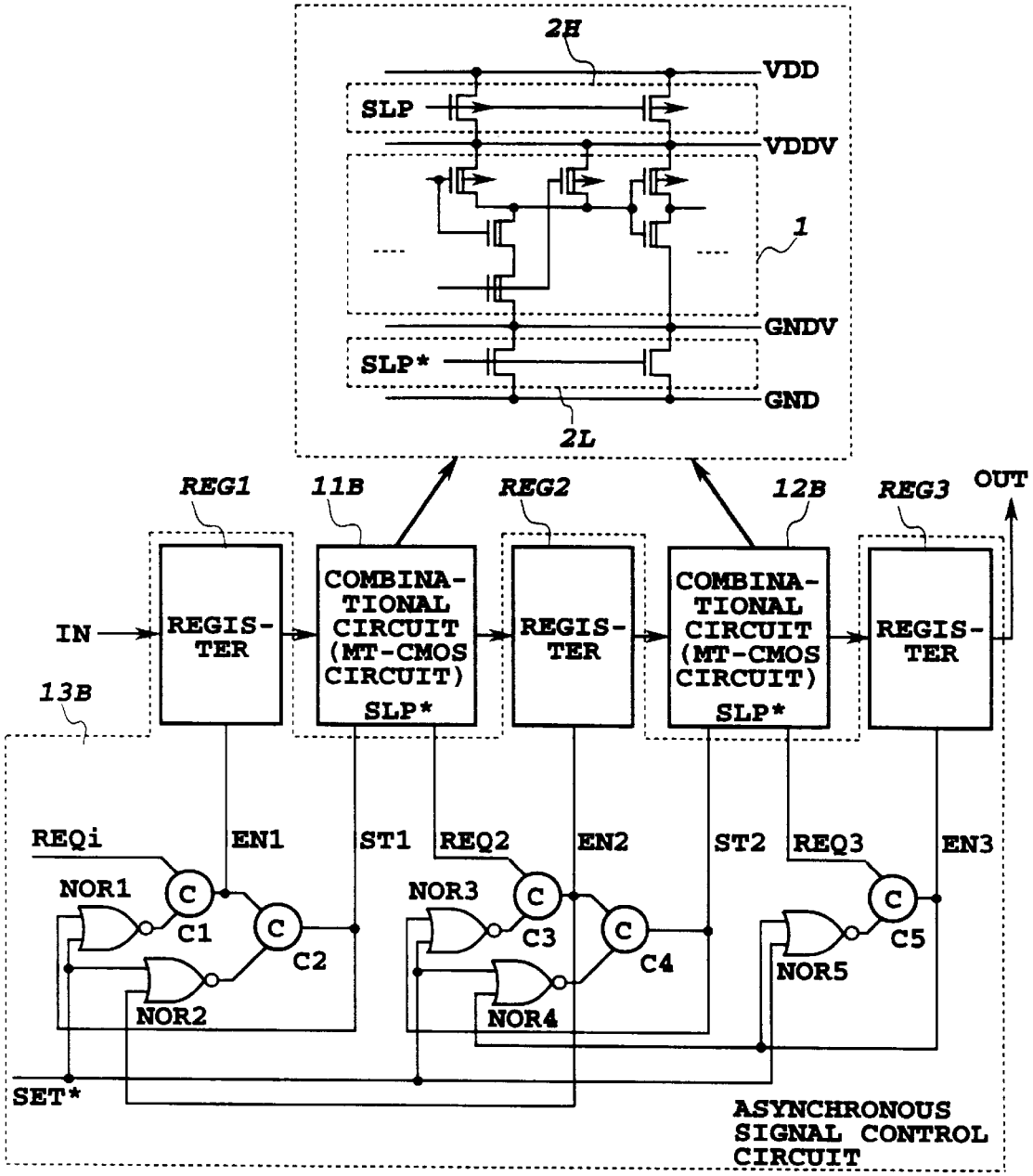


FIG.3

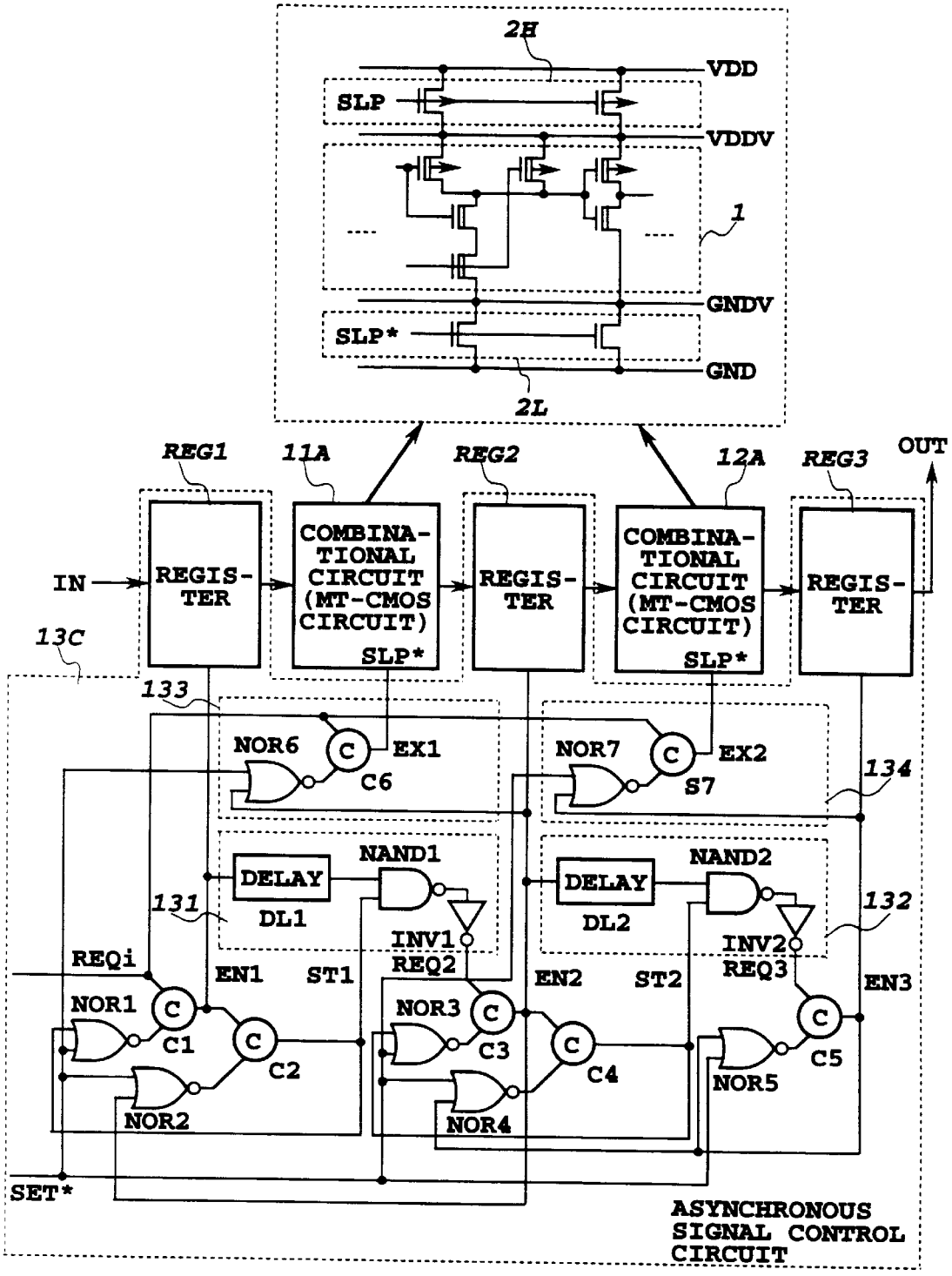


FIG.4

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