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Nishimura et al.

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[57] ABSTRACT

A test-target circuit is constructed of circuit blocks each comprising low-Vth MOS transistors including address buffers and a timing generator. A test enable signal for indication of a test, an operation selection signal for indication of an operation, and a block selection signal used to select a desired circuit block are provided. A high-Vth NMOS and a high-Vth PMOS transistor are provided in order to provide to a test circuit one of detected currents of the circuit blocks that was selected by placing a block selection signal and the test enable signal in the state of HIGH.

11 Claims, 19 Drawing Sheets

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D.1		١	VREF	, I11	TE	Ĵ	VCIR	S11	CP	∘ BS
D11 ← : : : : : : : : : : : : : : : : : :				: : : : : : : : : : : : : : : : : : :		(AB) : : (M1)	 	: S31		
	REGISTER CIRCUIT	·	TEST CIRCUIT	:	:	TEST-TARGET CIRCUIT		:	SCAN REGISTER	
D3n ←				< 13n ⋮		(Mn)	 	< S3n :		
D61 ←		T		: <u>I61</u>	: 	: (TG)	: 	S61		
	250		240	22	0B	230	GND	220A	210	

[54] SEMICONDUCTOR INTEGRATED CIRCUIT [75] Inventors: Kazuko Nishimura, Kyoto; Hironori Akamatsu, Osaka; Akira Matsuzawa, Kyoto; Mitsuyasu Ohta, Osaka, all of [73] Assignee: Matsushita Electric Industrial Co., Ltd., Osaka, Japan [21] Appl. No.: 09/083,389 [22] Filed: May 22, 1998 Related U.S. Application Data Continuation of application No. 08/888,920, Jul. 7, 1997, [63] Pat. No. 5,978,948. [30] Foreign Application Priority Data Japan 8-175304 May 23, 1997 [JP] Japan 9-133369 Int. Cl.⁷ G11C 29/00 [52] **Field of Search** 714/718, 724, 714/736, 733, 735; 365/201 [56] **References Cited** U.S. PATENT DOCUMENTS

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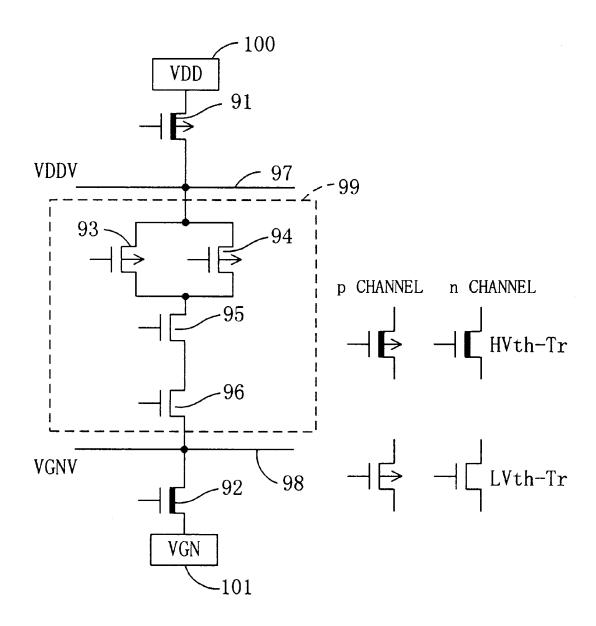
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Fig. 1 PRIOR ART



LOGIC CIRCUIT ∞ 7a (LOGIC BLOCK) \mathcal{O} Fig. VGNV 6a NORMAL CONTROL SIGNAL TEST CONTROL UNIT NORMAL CONTROL UNIT Sdt.



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Fig. 3

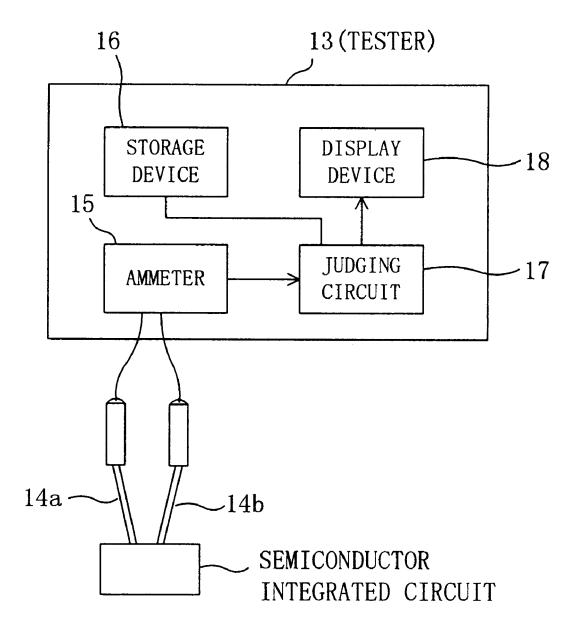
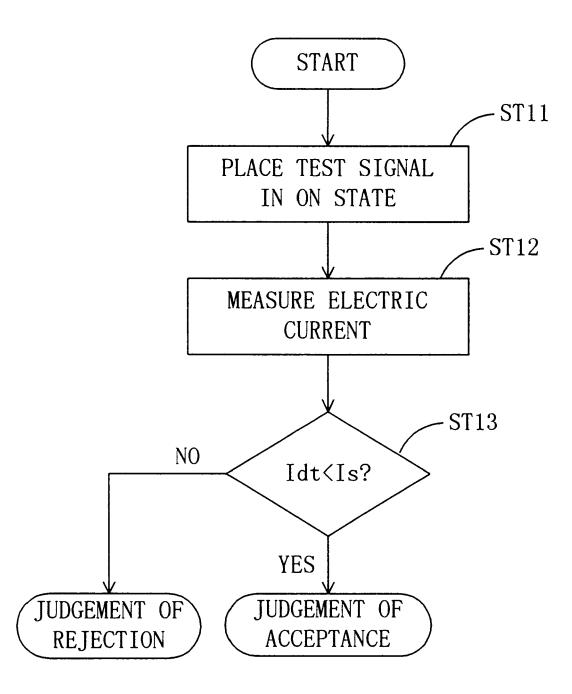




Fig. 4





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