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United States Patent [19]

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Fujii et al.

[45] Date of Patent: **Aug. 29, 2000**

[54] **LOGIC CIRCUIT HAVING DIFFERENT THRESHOLD VOLTAGE TRANSISTORS AND ITS FABRICATION METHOD**

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[75] Inventors: **Koji Fujii, Zama; Takakuni Douseki, Atsugi, both of Japan**

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ISSCC96/Session 5/Technology Directions: High Speed, Low Power/Paper TP 5. TP:5.4 A 0.5V Simox-MTCMOS Circuit with 200ps Logic Gate; Takakuni Douseki, et al., 1996 IEEE International Solid-State Circuits Conference; pp. 84-85, 66-67, and 364-365.

[73] Assignee: **Nippon Telegraph and Telephone Corporation, Toyko, Japan**

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Attorney, Agent, or Firm—Venable; Robert J. Frank; Jeffrey W. Gluck

[21] Appl. No.: **08/861,319**

[22] Filed: **May 21, 1997**

[30] Foreign Application Priority Data

| | | | | |
|---------------|------|-------|-------|----------|
| May 22, 1996 | [JP] | Japan | | 8-150268 |
| Aug. 13, 1996 | [JP] | Japan | | 8-231306 |

[51] **Int. Cl.⁷** **H03K 17/16**

[52] **U.S. Cl.** **326/34; 326/83; 326/121**

[58] **Field of Search** 326/17, 31, 34-36, 326/53, 54, 55, 83, 86, 112, 119, 121

[57] ABSTRACT

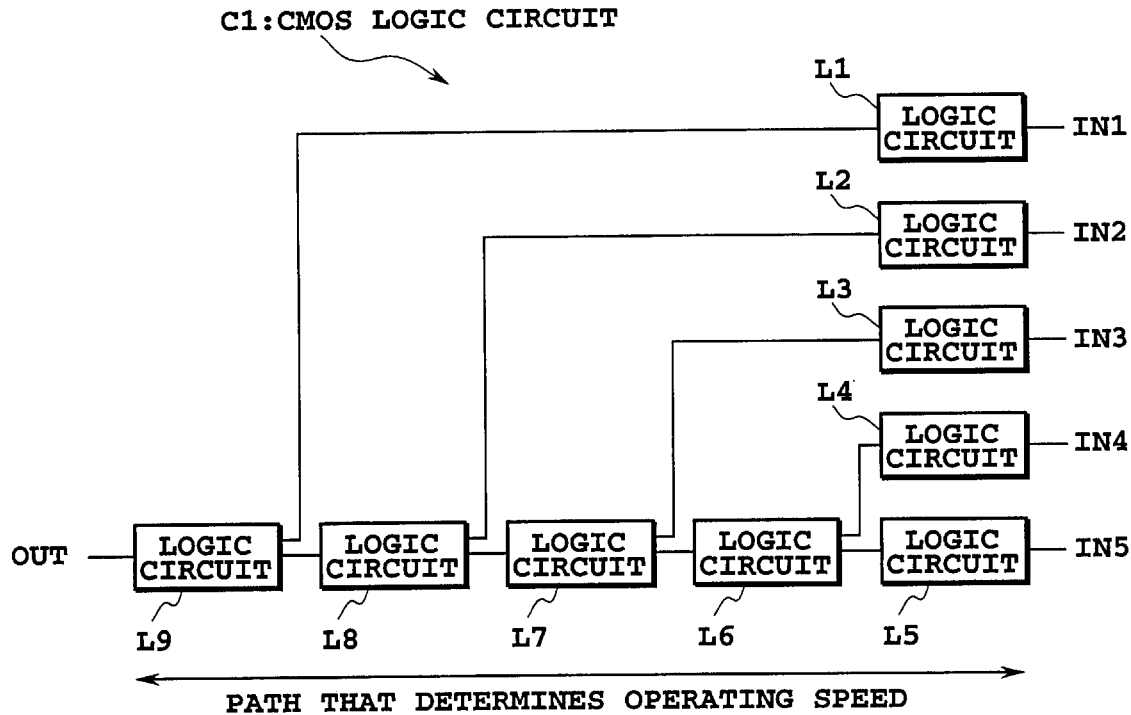
A logic circuit having a first logic gate and the remaining logic gate or gates. The first logic gate is interposed in a signal path determining an operating speed, and includes at least one first MOS transistor which has a threshold voltage lower than a predetermined voltage and operates at a high speed. The remaining logic gate or gates include at least one of a second MOS transistor and a third MOS transistor as a transistor having a margin for operating speed. The second MOS transistor has a middle threshold voltage equal to or greater than the predetermined voltage, and the third MOS transistor has a high threshold voltage equal to or greater than the predetermined voltage. The power consumption of the entire logic circuit at the time of operation is reduced, while maintaining the maximum operating speed.

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17 Claims, 24 Drawing Sheets



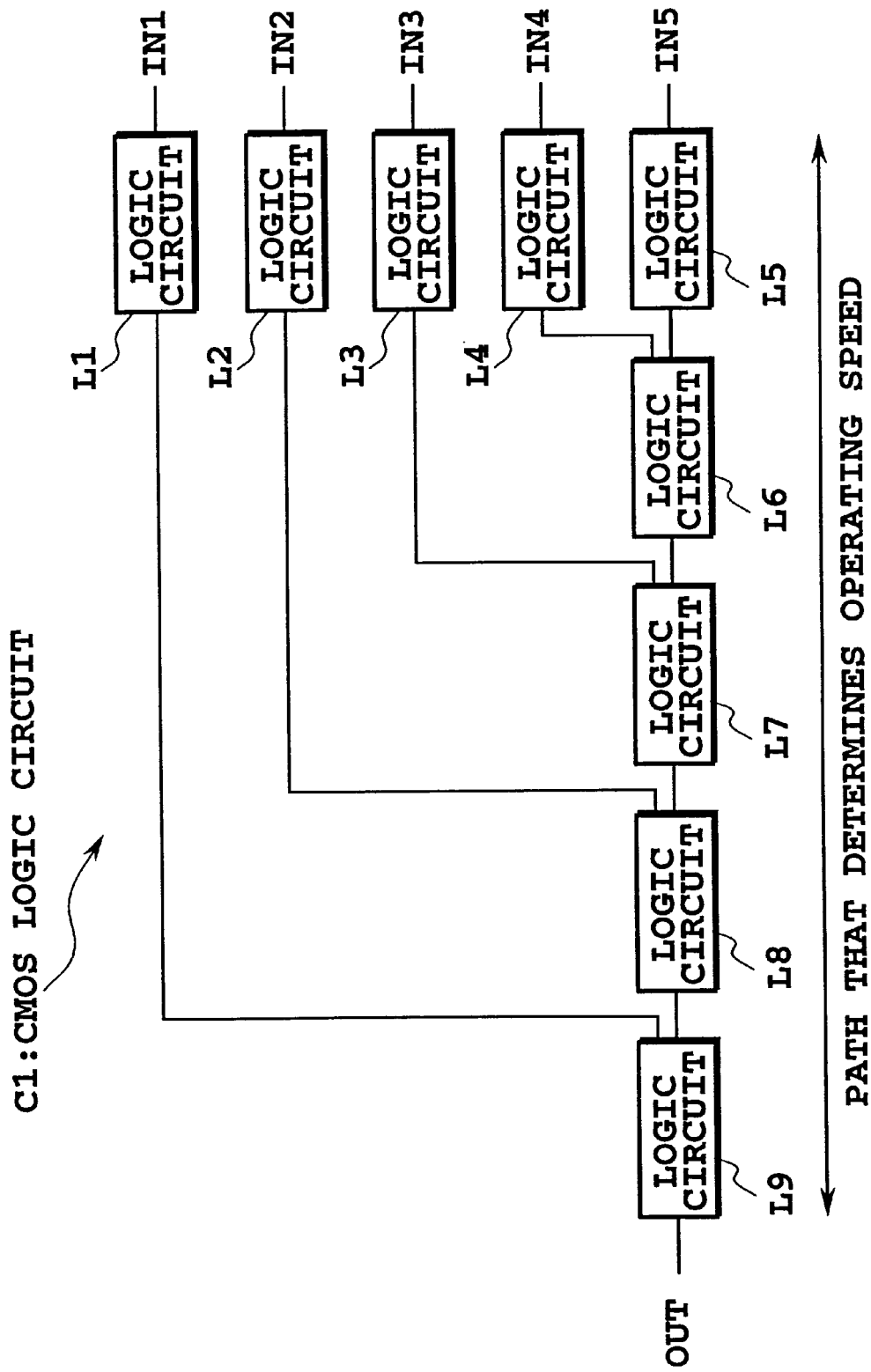


FIG.1

L1: LOGIC CIRCUIT

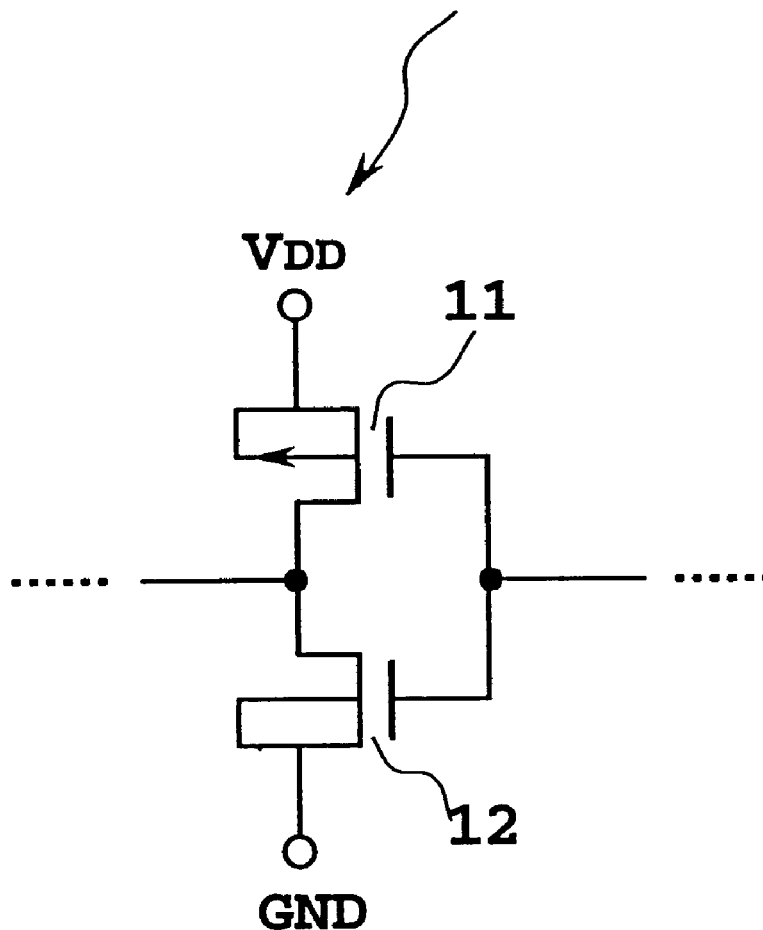


FIG.2

FIG.3

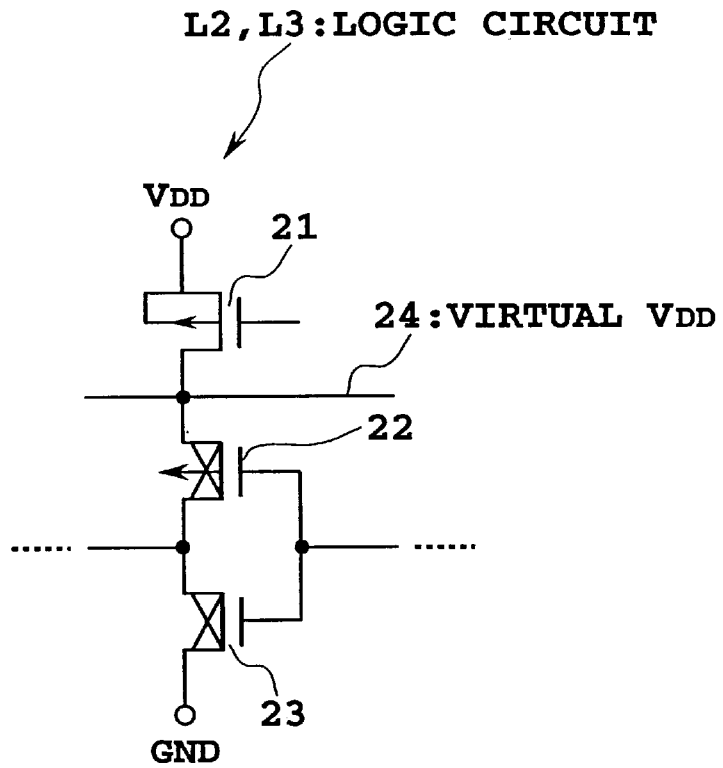
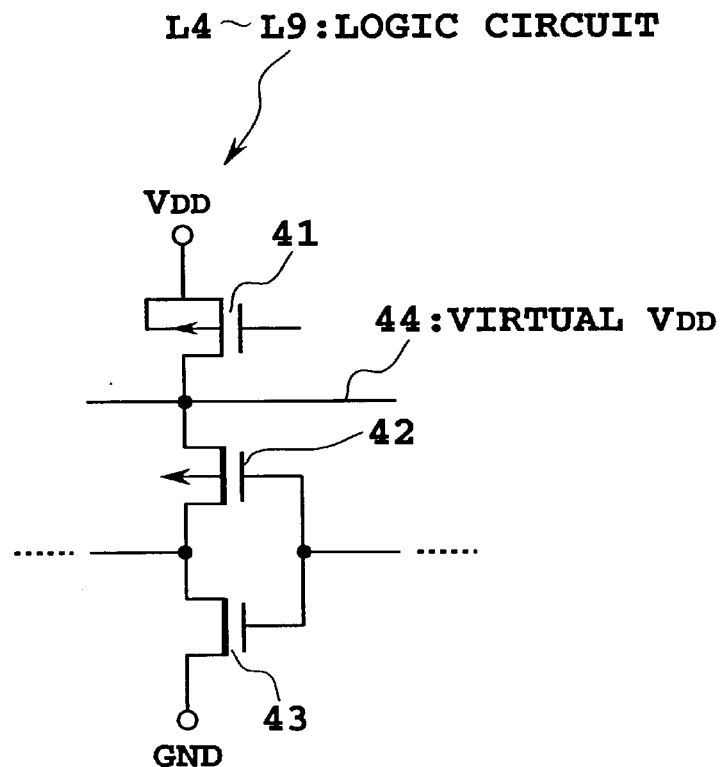


FIG.4



| | LOW THRESHOLD VOLTAGE MOS TRANSISTOR | MIDDLE THRESHOLD VOLTAGE MOS TRANSISTOR | HIGH THRESHOLD VOLTAGE MOS TRANSISTOR |
|------|--|---|---|
| nMOS | | | |
| pMOS | | | |

FIG.5

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