

United States Patent [19]

Itoh et al.

5,394,365

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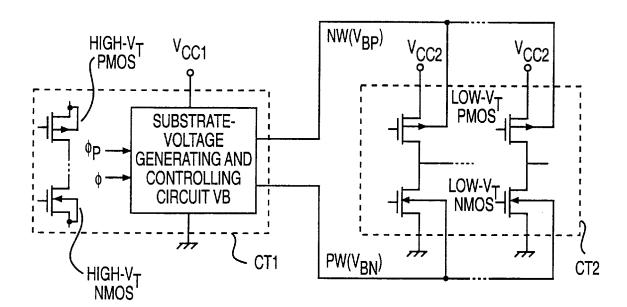
Primary Examiner—Kenneth B. Wells Assistant Examiner—An T. Luu Attorney, Agent, or Firm-Beall Law Offices

ABSTRACT

The well voltage of a CMOS circuit having low-thresholdvoltage MOSFETs is controlled when the power supply is turned on, during normal operation, and when the supply voltage is cut off. The CMOS circuit can thus operate stably with lower power consumption, because latching-up is reduced when the supply voltage is applied to the CMOS circuit or when the supply voltage is cut off, and subthreshold current is decreased during normal operation.

25 Claims, 23 Drawing Sheets

[54]	SEMICONDUCTOR DEVICE CAPABLE OF OPERATING STABLY WITH REDUCED POWER CONSUMPTION						
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[30] Foreign Application Priority Data							
Feb	. 28, 1997	[JP]	Japan		9-045235		
[51]	Int. Cl. ⁷				G05F 1/10		
[52]	U.S. Cl.			327/54	6 ; 327/544; 327/534		
[58]	Field of	Search			327/534, 535,		
			327/54	14, 545, 5	546, 547; 326/35, 36		
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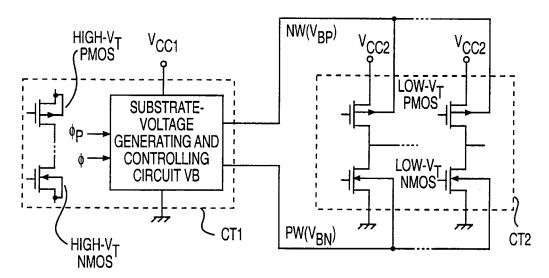
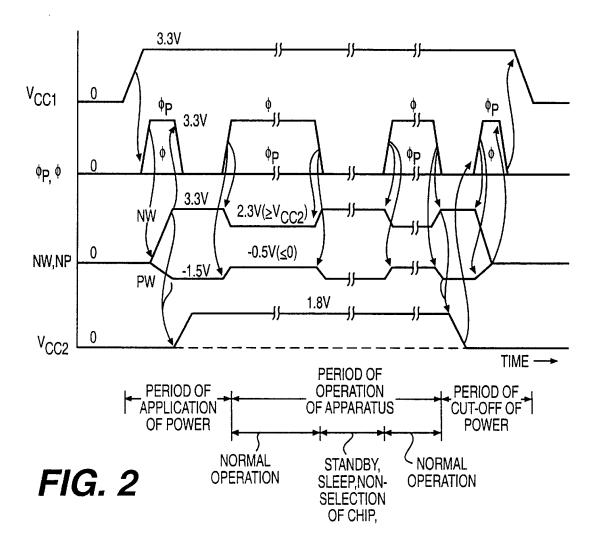


FIG. 1





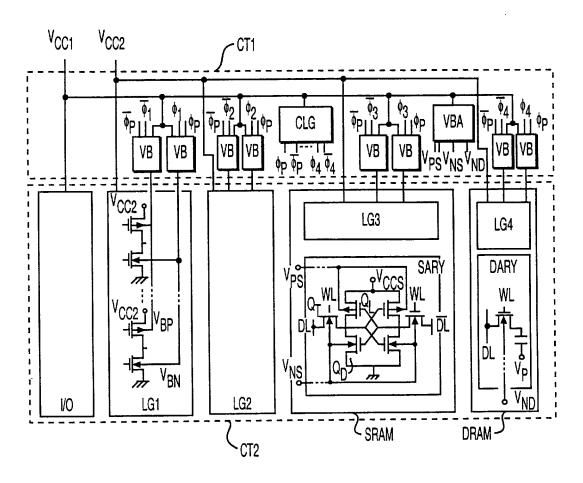


FIG. 3

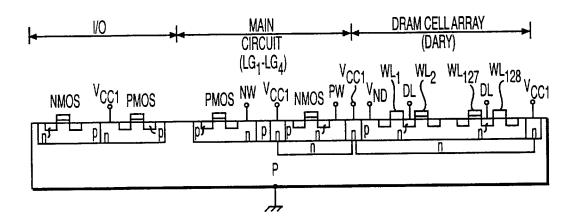


FIG. 4



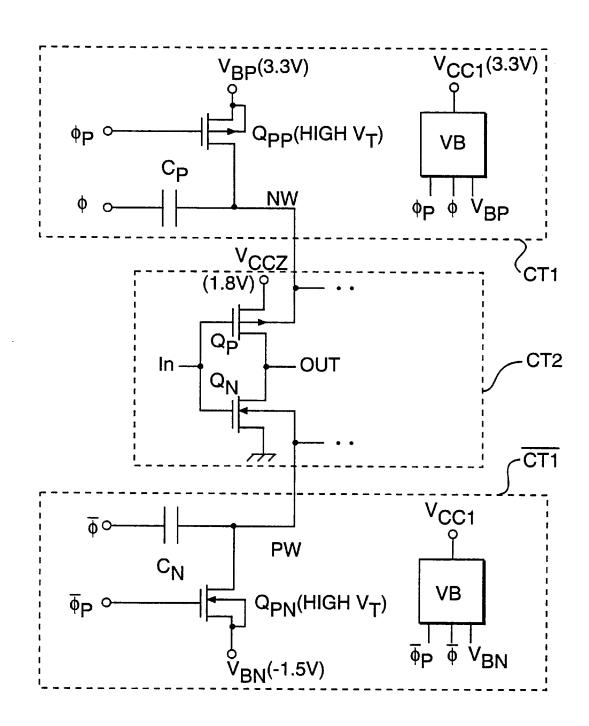


FIG. 5



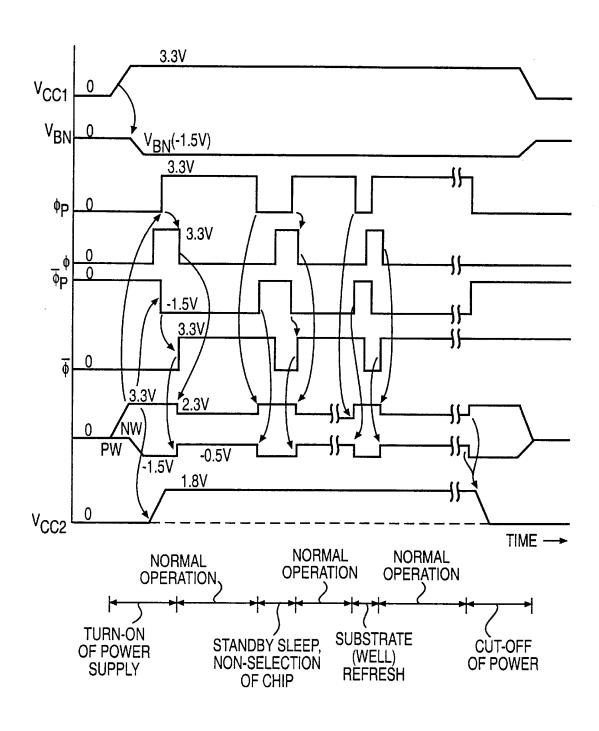


FIG. 6



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