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# United States Patent [19]

**Mashiko**

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 [45] **Date of Patent:** **\*Mar. 7, 2000**

[54] **SEMICONDUCTOR INTEGRATED CIRCUIT HAVING REDUCED CURRENT LEAKAGE AND HIGH SPEED**

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[73] Assignee: **Mitsubishi Denki Kabushiki Kaisha**, Tokyo, Japan

[\*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: **08/651,588**

[22] Filed: **May 22, 1996**

[30] **Foreign Application Priority Data**

Oct. 19, 1995 [JP] Japan ..... 7-271574

[51] **Int. Cl.<sup>7</sup>** ..... **G05F 1/10**

[52] **U.S. Cl.** ..... **327/544; 327/377**

[58] **Field of Search** ..... 327/390, 589, 327/377, 170, 108-112, 544; 326/88, 80, 81

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[57] **ABSTRACT**

A semiconductor integrated circuit including a first MOS transistor supplied with a first power supply voltage and having a high threshold voltage; a second MOS transistor supplied with a second power supply voltage and having the high threshold voltage; a logic circuit connected between the first transistor and the second transistor and including a plurality of MOS transistors having a low threshold voltage; a control circuit for generating a control signal when the logic circuit is in a standby state; and a voltage generating circuit for generating a first voltage which is a higher than the first power supply voltage and a second voltage which is a lower than the second power supply voltage, for supplying the first voltage to a gate of the first MOS transistor and for supplying the second voltage to a gate of the second MOS transistor when the logic circuit is in the standby state, thereby to decrease leakage current through the first and second transistors and through the logic circuit when in the standby state.

**34 Claims, 11 Drawing Sheets**

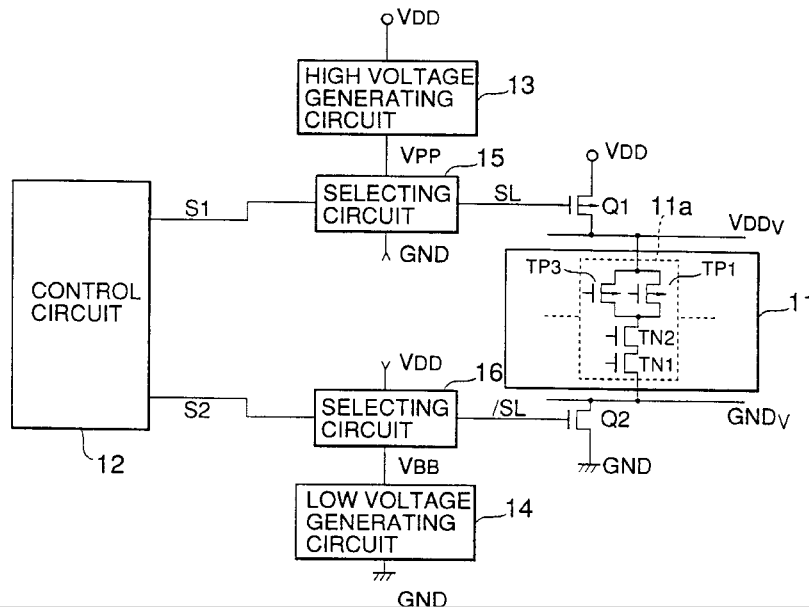


FIG. 1

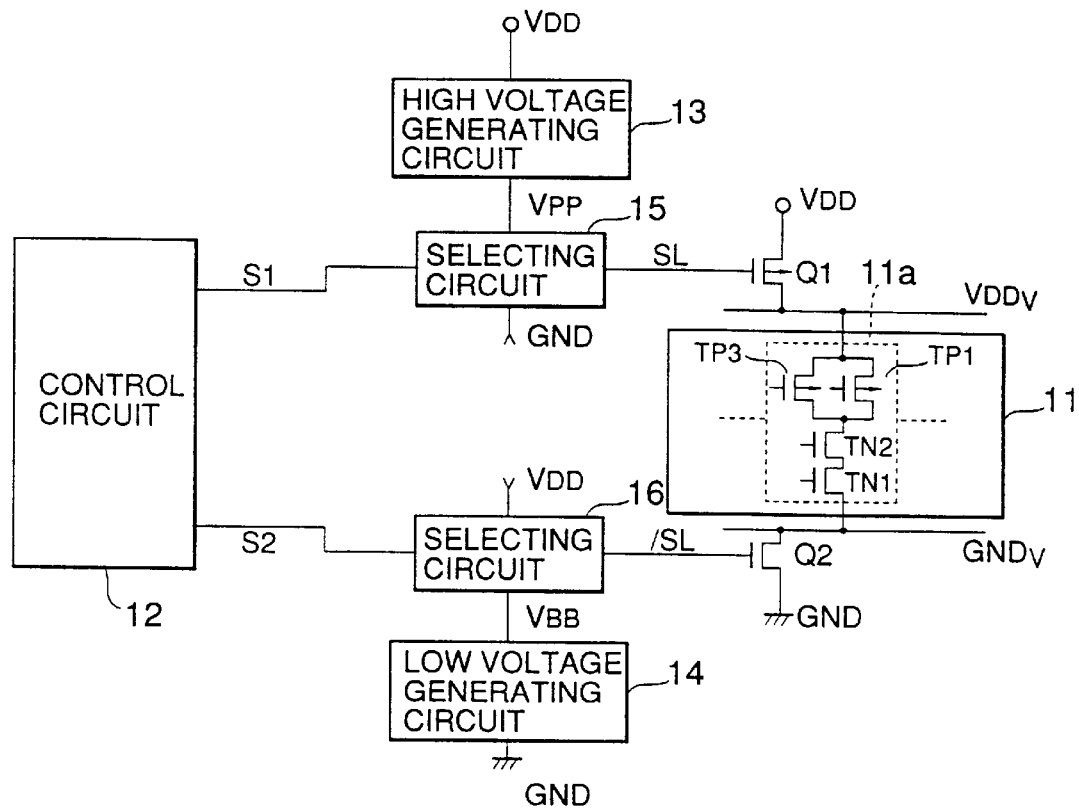


FIG. 2

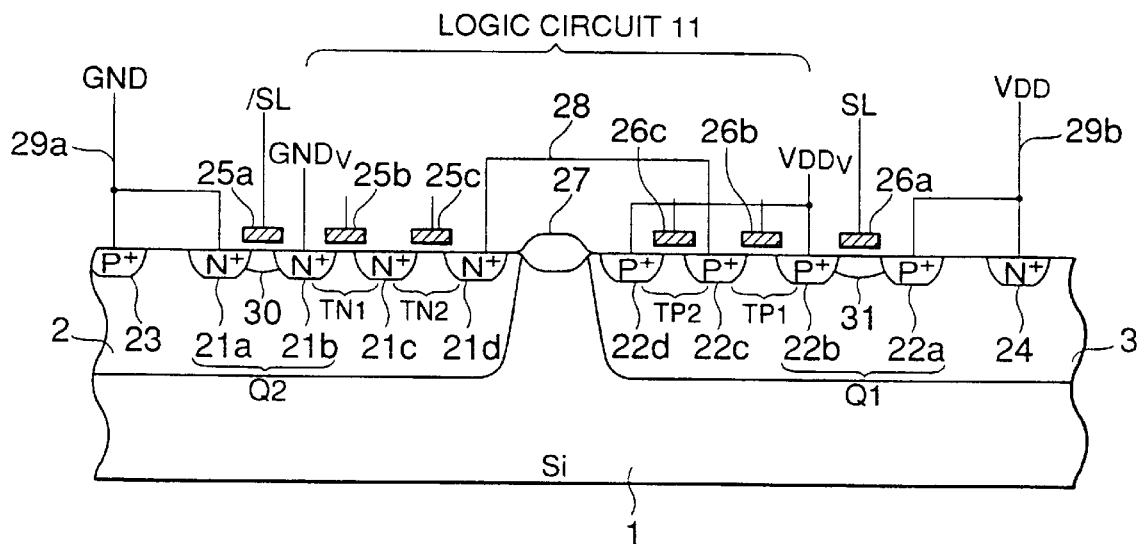


FIG.3

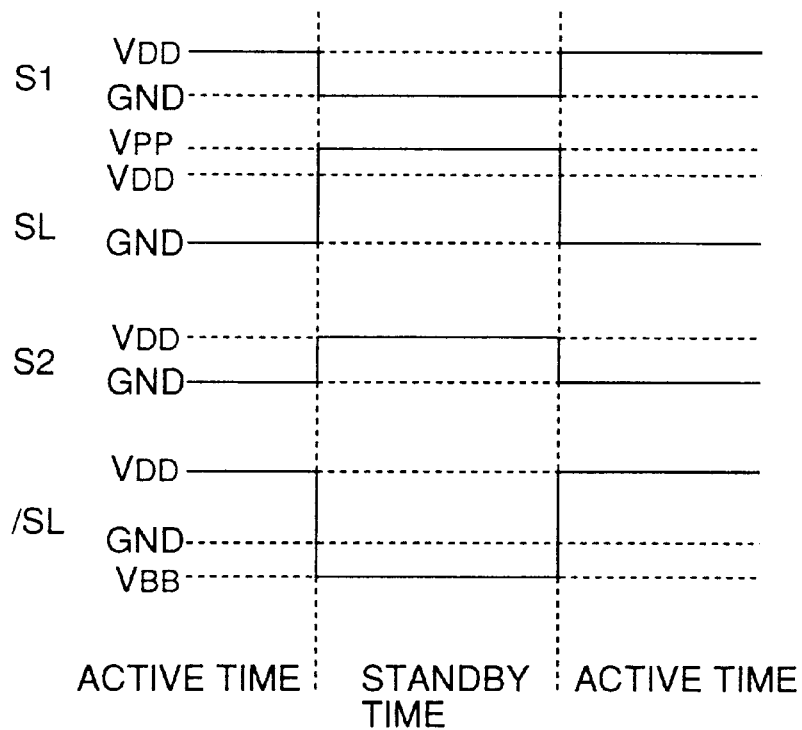


FIG.4

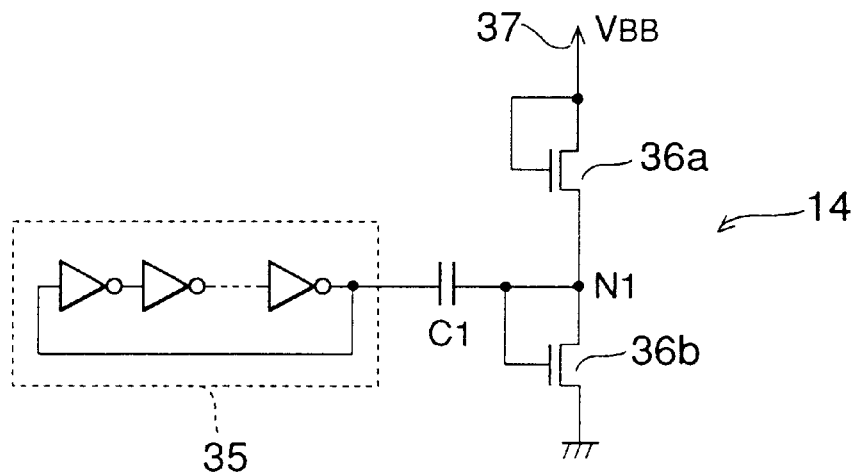


FIG. 5

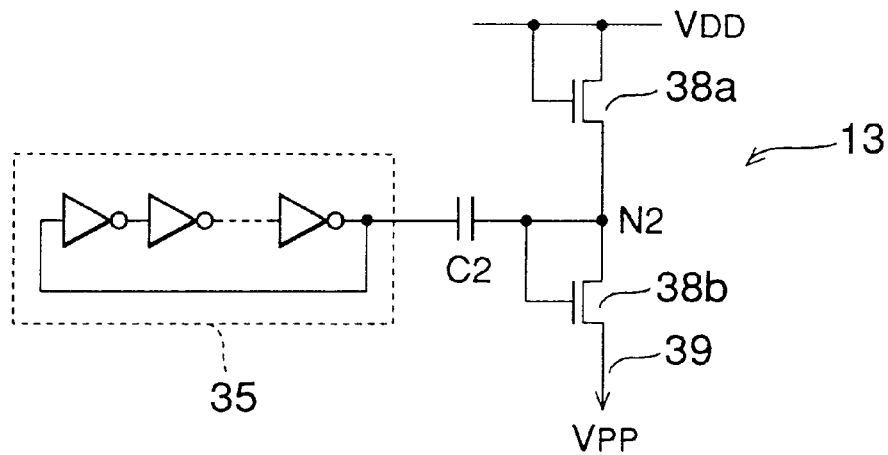
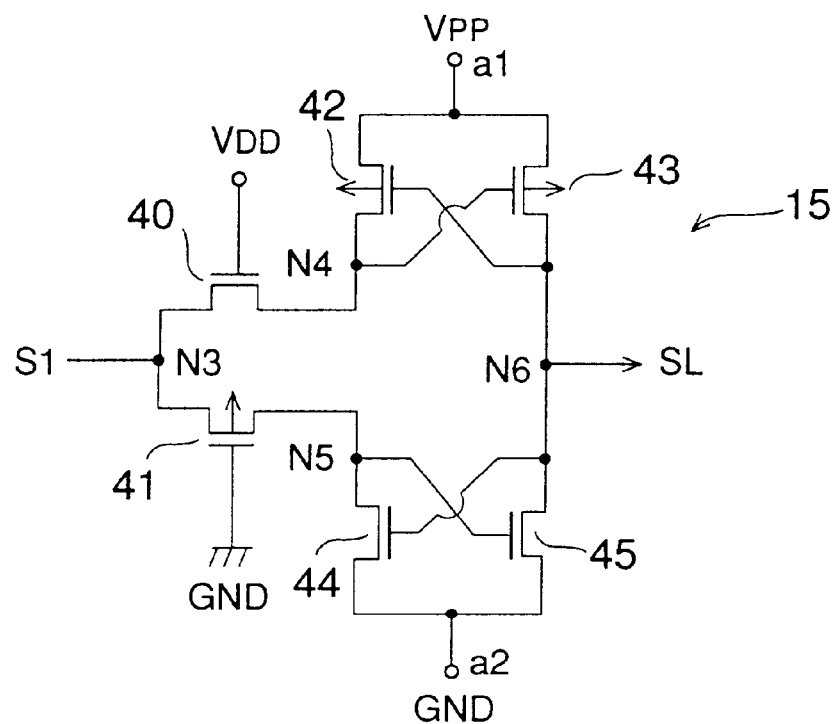


FIG. 6





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