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United States Patent [19]

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Mashiko et al.

[45] Date of Patent: **Jul. 14, 1998**

[54] SEMICONDUCTOR INTEGRATED CIRCUIT

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[57] **ABSTRACT**

[21] Appl. No.: **582,416**

A logic circuit (L_i) is connected between a virtual power supply line (VDDV) connected to an actual power supply (VDD) through a PMOS transistor (Q1) and a virtual grounding line (GNDV) connected to an actual ground (GND) through an NMOS transistor (Q2). During an active period, the transistors (Q1, Q2) are constantly conducting, and the virtual power supply line (VDDV) and virtual grounding line (GNDV) are at the power supply potential (VDD) and ground potential (GND), respectively. During a standby period, the transistors (Q1, Q2) periodically repeat conduction/non-conduction to charge and discharge the virtual power supply line (VDDV) and virtual grounding line (GNDV), suppressing power consumption while preventing loss of information held by the logic circuit (L_i).

[22] Filed: **Jan. 3, 1996**

[30] **Foreign Application Priority Data**

Aug. 21, 1995 [JP] Japan 7-211772

[51] Int. Cl.⁶ **G05F 1/10**

[52] U.S. Cl. **327/544; 329/546; 329/215**

[58] Field of Search 327/77, 87, 198, 327/530, 538, 540, 541, 543, 545, 544, 546, 199, 215, 217; 365/222

[56] **References Cited**

PUBLICATIONS

Denshi Gijutsu, pp. 29–32, Junzo Yamada, et al., “1v Low-Power High-Speed Operation MTCMOS Logical Circuit Technology” Sep. 1994.

22 Claims, 8 Drawing Sheets

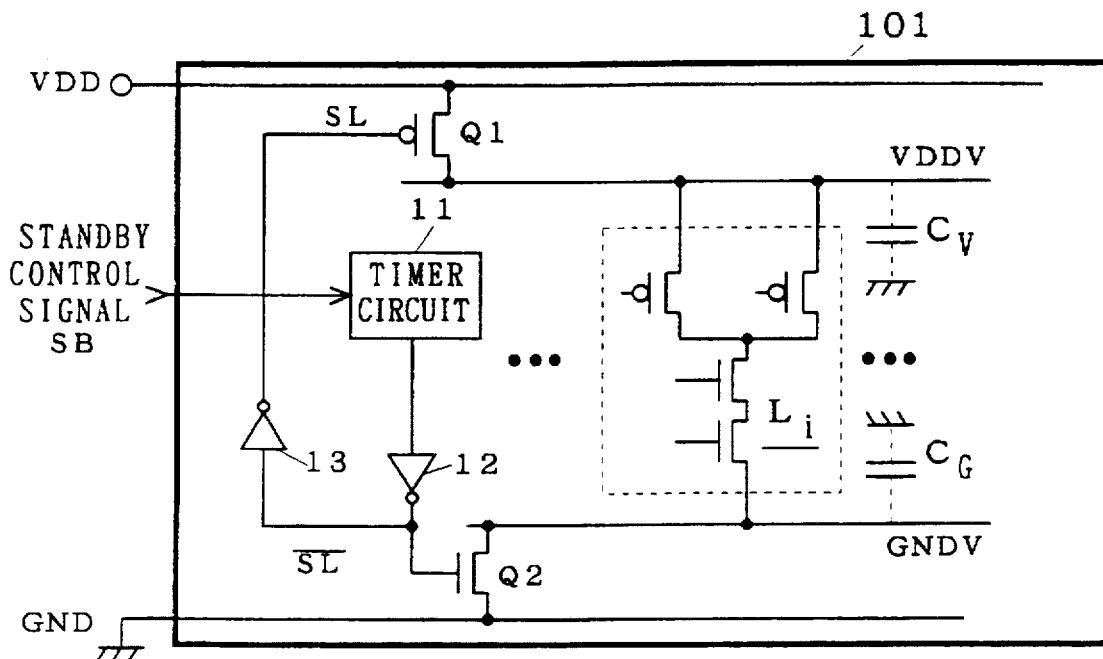


FIG. 1

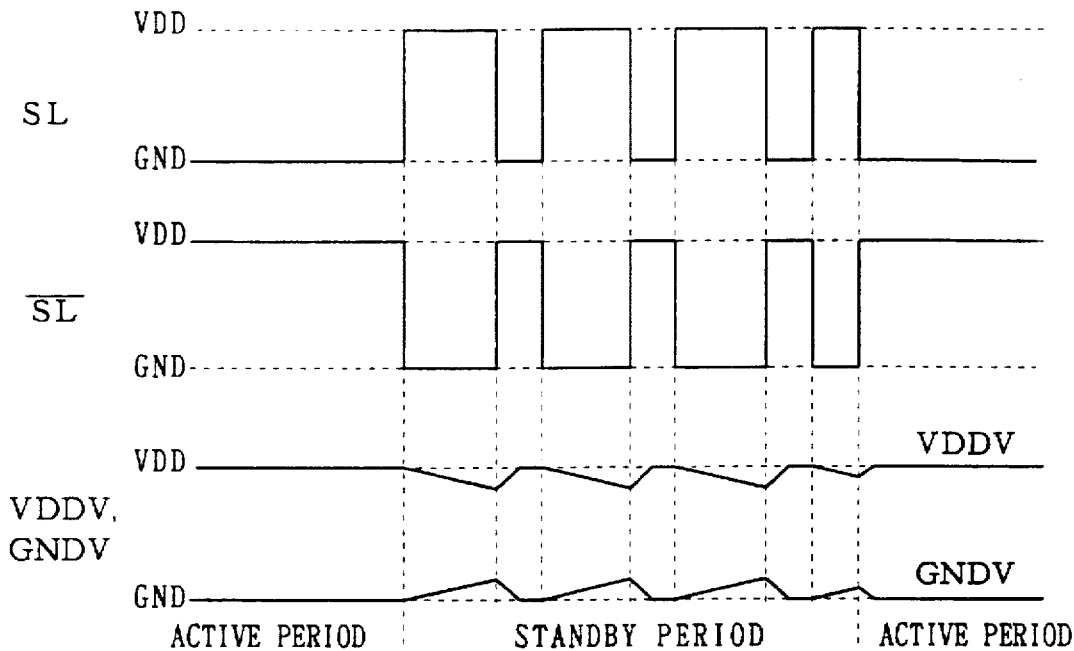


FIG. 2

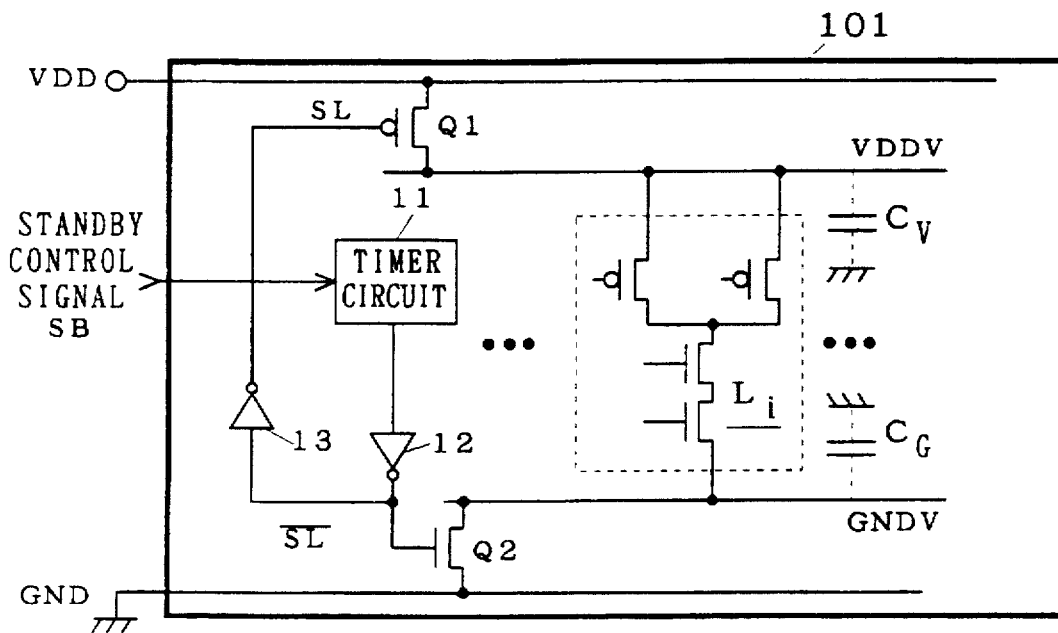


FIG. 3

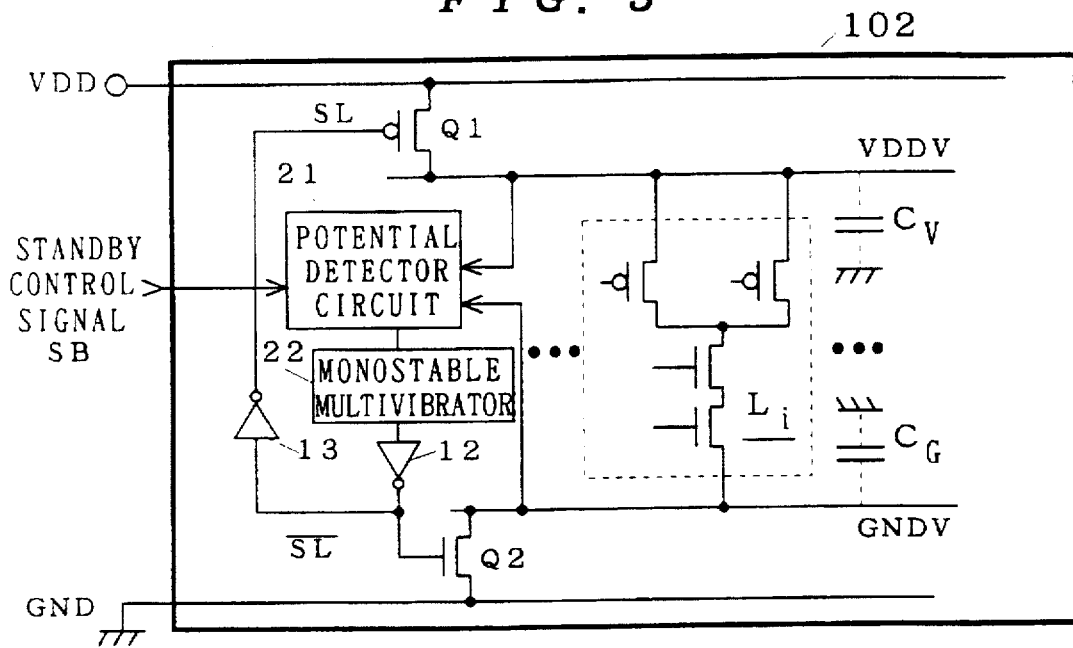


FIG. 4

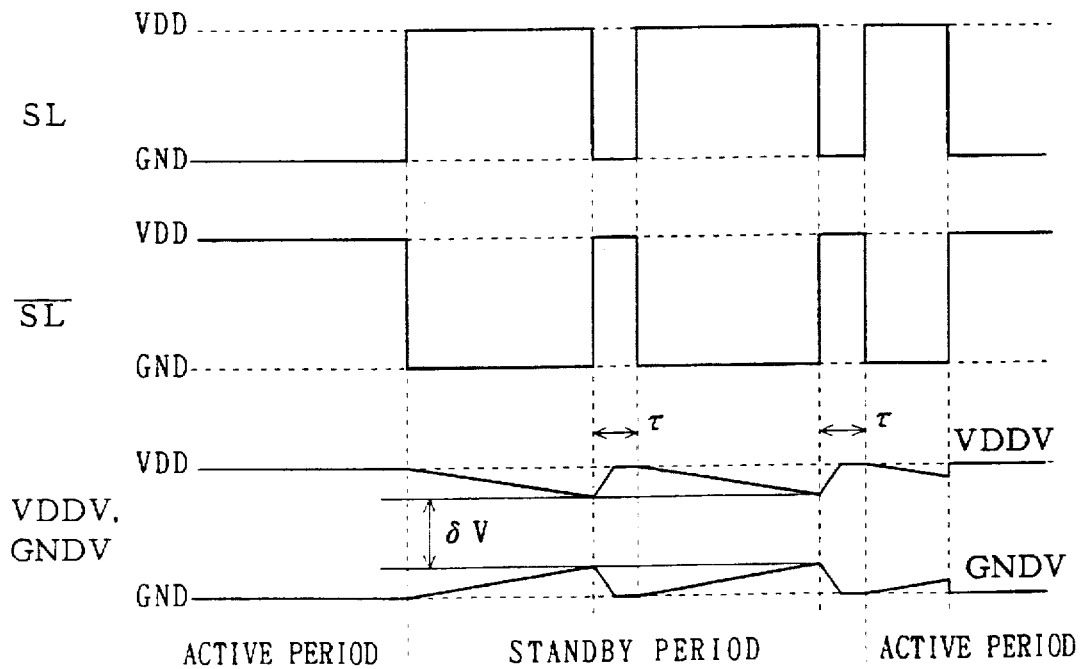


FIG. 5

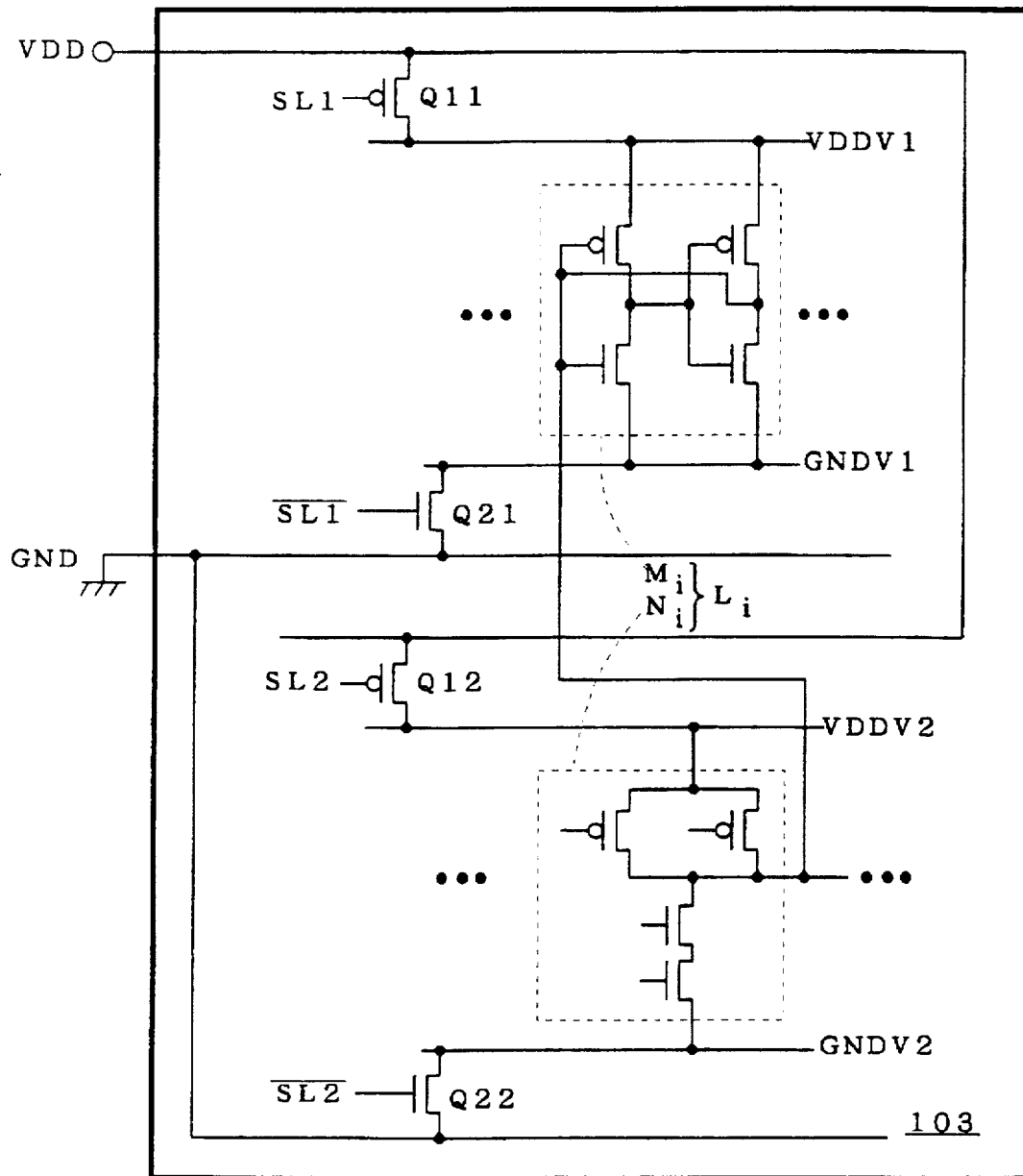
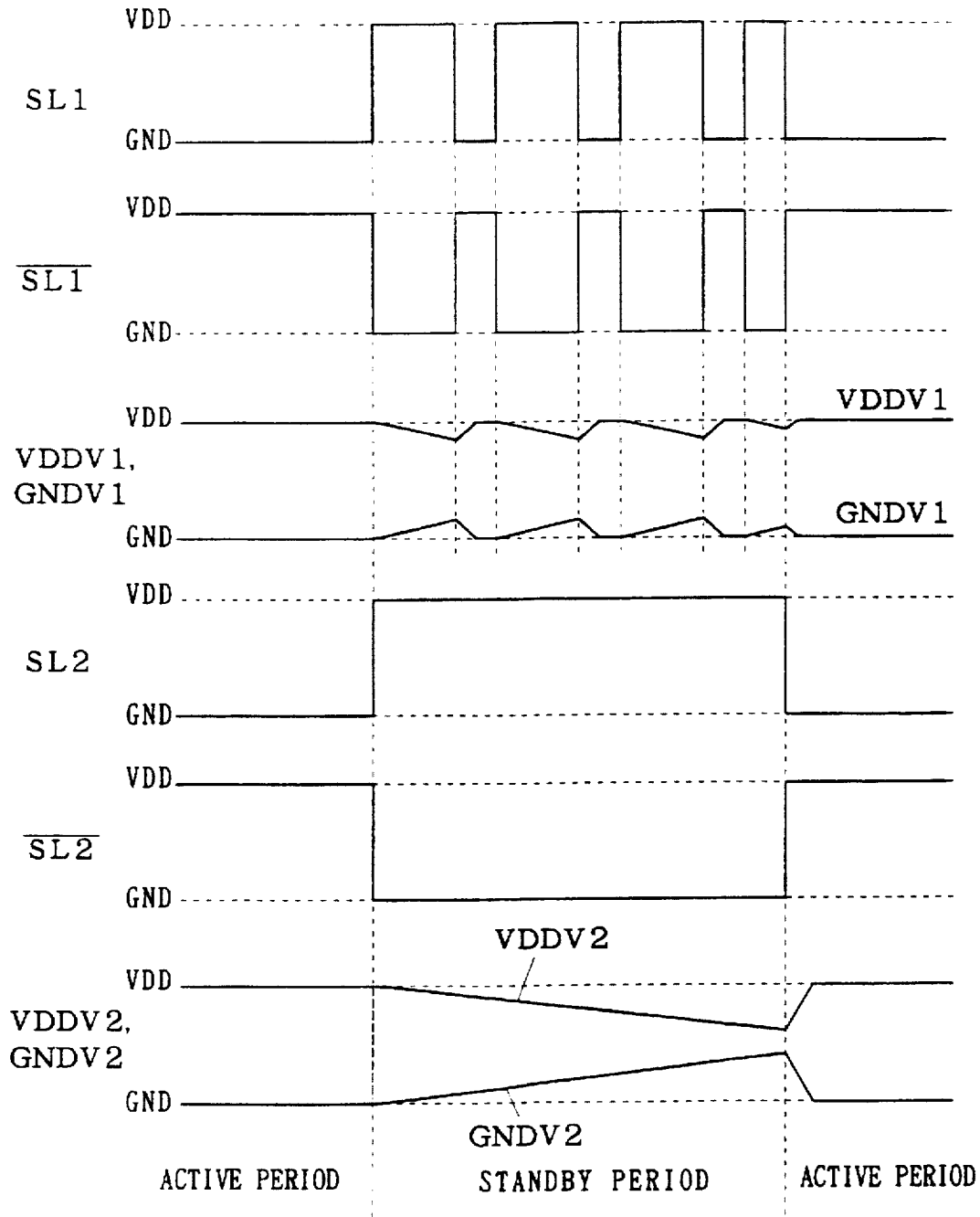


FIG. 6



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