# Special Papers

# A Subnanosecond 2000 Gate Array with ECL 100K Compatibility

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*Abstract*—**This paper describes a subnanosecond gate array with 2000 gate complexity using an advanced bipolar process. The high performance of this process and the optimized circuit design have made it possible to achieve a 700-ps delay time for a basic ECL gate under a general usage condition of a 3 fan-in, 3 fan-out and 3-mm wiring length, in spite of a low power dissipation of 1.9 mW/gate. A 450-MHz typical toggle frequency has been obtained by using a series-gated flip-flop. Utilizing the integrated computer aided design (CAD) system, a quick and error-free design can be achieved. As a result, 100 percent routability has been attained for automatic placement and wiring in spite of 90 percent cell utilization. Low thermal resistance (6°C/W) packages are employed for this LSI chip to enable installation in an air cooled system.**

## I. Introduction

THE DEMANDS of higher system speed are increasing from manufacturers of mainframes, telecommunications equipment, IC testers, and electric measuring instruments. One very effective improvement for a high-performance data processing system is the change to a high-speed and a highly complex gate array from standard IC's. The media delay caused by the interconnect and package capacitance can be reduced by using customized and more highly integrated circuits. In order to meet these requirements, this high-speed and highly complex gate array has been developed. Furthermore, this gate array was designed using the following concepts to extend the application of high-speed LSI.

### A. High-Speed Operation in Systems

This concept includes high-speed operation of the chip itself and reduction of media delay. In order to achieve high-speed operation of the chip itself an advanced bipolar process [1] and optimized circuit configuration are employed. Since sufficient drive capability is required for media delay reduction, an ECL 100K output buffer having a 50-Ω terminated resistor is adopted.

### B. Necessity of Predictable Performance

In order to achieve an optimum system design, performance prediction before production of gate arrays is strongly required by the customer. For this concept, a reproducible simple structured process has been developed, and a stable circuit configuration has been adopted.

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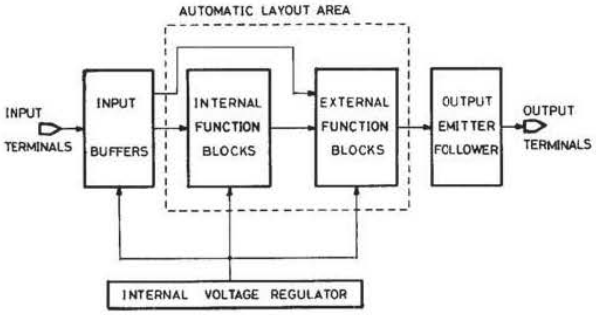


Fig. 1. Logic flow.

### C. Adoption of an Air Cooled Environment

Since the air cooling technique is popular and inexpensive for systems, the operation in an air cooled environment is considered to be important for wide use in many systems. Accordingly, low power internal gates and low thermal resistivity packages are used for this gate array.

### D. Quick and Error-Free Design of Customized Circuits

The quick and error-free design is an essential concept for the custom design of gate arrays. In order to satisfy this concept, the integrated CAD system [2] which is based on a macro cell design method is utilized.

## II. Logic Flow

This gate array was designed to be compatible with ECL 100K logic levels which are used in the fastest standard logic integrated circuits. ECL 100K levels are converted to internal ECL levels to perform logic through the input buffer, and then converted back again to ECL 100K levels through external function blocks and output emitter followers to facilitate system compatibility (Fig. 1). A small logic swing is used for internal ECL levels in order to achieve high-speed operation and a two-level series-gated structure. The internal voltage regulators ($V_{csi}$ and $V_{cs}$) drive all the constant current sources of internal and

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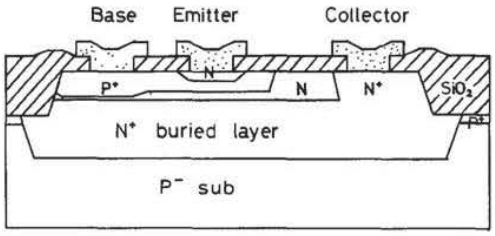


Fig. 2. Cross section of the basic transistor fabricated by an advanced bipolar process.

TABLE I
CHARACTERISTICS OF AN INTERNAL GATE TRANSISTOR

| | | | |
|---|---|---|---|
| C-B Junction Capacitance | Cjc | 0.015 | pF |
| B-E Junction Capacitance | Cje | 0.016 | pF |
| C-Sub Junction Capacitance | Ccs | 0.041 | pF |
| Base Resistance | Rbb | 1080 | Ohm |
| Collector Resistance | Rsc | 79 | Ohm |
| Cut-Off Frequency | $f_T$ | 8 | GHz |
| Current Gain | $h_{fe}$ | 70 | |

external gates respectively to keep the logic swing stable. The stable reference voltages for internal gates ($V_{R1}$) and input buffers ($V_{bb}$) are also generated by the internal voltage regulators.

The function blocks, or predefined logic elements, containing the intracell connections are used for implementation of the custom logic. According to the design database for custom logic implementation, internal and external function blocks are automatically placed in the appropriate cell position within the automatic layout area and are further interconnected using the CAD system.

## III. Process

An advanced bipolar process using oxide isolation [1] has been adopted for this gate array (Fig. 2). In order to predict precise gate array performance before production, the small distribution of characteristics is considered to be important to a gate array process. In contrast with new devices for high-speed operation having complex structure and a complicated fabrication sequence [3], [4], [5], the simple structure is applied to realize reproducible high volume production for a high complexity LSI chip. As a result, a high predictability in production yields and circuit performance has been obtained prior to production.

Generally, the reduction of parasitic capacitances, the decrease of base resistance, and higher cutoff frequency are known to be effective methods for increasing speed in ECL circuits. In order to reduce the parasitic capacitances of a transistor, the oxide isolation and narrow emitter stripe are adopted. In an attempt to decrease base resistance, the spacing between an emitter electrode and a base electrode is reduced to 2 $\mu$m, which is the minimum electrode spacing in this process. A shallow junction structure which has 0.1 $\mu$m base width 0.1 $\mu$m emitter depth have been realized using ion implantation and a polysilicon arsenic emitter. Consequently, a high cutoff frequency of 8 GHz has been obtained. A thin n-type epitaxial layer 1 $\mu$m thick is used for this process.

In order to minimize the propagation delay time, the tradeoffs between the small capacitance of a single base transistor and the small base resistance of a double base transistor are considered using circuit simulation. As a result, the single base transistor proved to be effective for the circuits which have relatively large load resistors and effective for high packing density. Accordingly, the single base transistor is used in the internal cells. On the other hand, the double base transistor is used in the external cells which have relatively small load resistors. The emitter sizes are $1.5 \times 3$ $\mu m^2$ for internal gate transistors and $1.5 \times 5$ $\mu m^2$ for internal emitter follower transistors. Table I shows characteristics of an internal gate transistor.

Three layer aluminum metallization is used for signal and bias routing and for the power buses. The third layer is only used for the power buses to reduce the power line resistance. The first layer metallization for signal is 3 $\mu$m wide with a 5 $\mu$m pitch and the second layer metallization is 4 $\mu$m wide with a 10 $\mu$m pitch.

## IV. Circuits and Function Blocks

A stable small logic swing ECL circuit has been adopted in this gate array to achieve high speed operation. The stable logic swings within the logic array are tightly controlled by the active transistor current sources, whose bias voltage is fully voltage and temperature compensated by internal voltage regulators. Consequently, the internal logic swing has been reduced to 560 mV.

In an attempt to achieve high-speed operation, current levels for internal transistors have been optimized through circuit simulation and trial production. The effect of cutoff frequency falloff at high currents [6] and the current division between gate and emitter followers are considered in the circuit simulation using a Gummel–Poon model [7]. As a result, a current of 0.4 mA has been selected for internal gates and emitter followers.

In order to increase the function capabilities and reduce the gate equivalent delay, series gating, collector dotting, and emitter dotting can effectively be used for function implementation. Fig. 3 shows a basic internal circuit of the OR-AND block using the diode-clamped collector dot. This block uses only one internal cell out of 832 internal cells in this gate array. The internal cell has 8 transistors for the gates, 4 transistors for the emitter followers, 12 resistors for the gates, and 8 resistors for the emitter followers. For internal function block outputs, emitter followers having a low output impedance are used to minimize the delay variation due to an unpredictable wiring length. Unused emitter followers in the multioutput blocks are not connected by the integrated CAD system so that unnecessary power dissipation may be avoided. Emitter dotting between blocks can be enhanced by widening the interconnection between emitter followers to minimize the logic level drops of the emitter dotting. As a result, a maximum

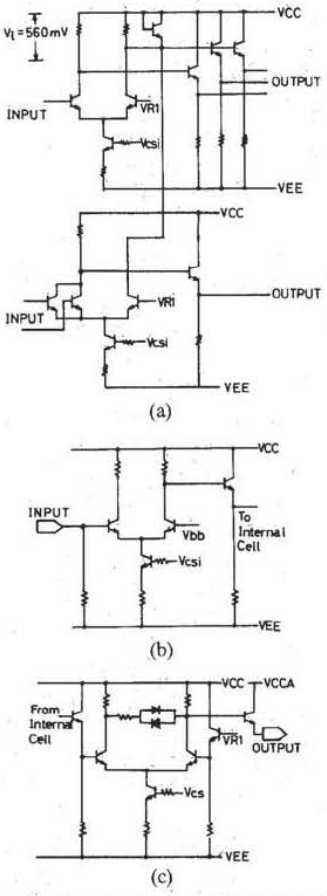


Fig. 3. (a) Schematic diagram of a basic internal circuit of the OR-AND block. (b) Schematic diagram of an input buffer. (c) Schematic diagram of an output buffer.

of 4 multiinput emitter dots between blocks is allowable for this gate array.

The 60 types of internal function blocks ranging from one simple gate to complicated circuits are available for the custom logic implementation. Only a simple gate is applied for external function blocks to minimize the external cell area which is occupied by large external transistors.

A 50 kΩ pull-down resistor is provided for the input buffer to keep a logic "low" state for the open input terminals as shown in Fig. 3(b). Furthermore, the input buffers contain circuitry to protect the inputs against damage due to high static voltages or electric fields.

Fig. 3(c) shows the output buffer which has 100K ECL interface. 100K ECL logic has temperature and voltage compensated high (−955 mV) and low (−1705 mV) voltage levels.

## V. Device Layout

The microphotograph of the gate array chip is shown in Fig. 4. The 832 (26×32) internal cells are placed within the internal logic circuit area. The 48 (24×2) external cells are placed on the left and right sides. Therefore the output signals appear on the left and right side bonding pads. Since the 108 input buffers are provided on all four sides,

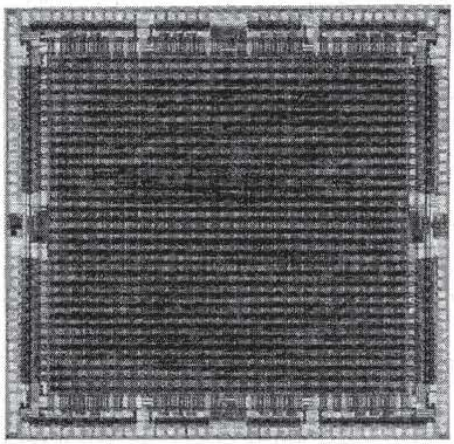

Fig. 4. Microphotograph of the gate array chip.

the left and right side pads can also be used as input terminals. The power supply terminals are located on all four sides of the chip to reduce the voltage drops in power busses caused by the maximum power supply current of 2 A. As a result, the voltage drops in power busses are limited to 60 mV. Power supply terminals are provided separately for internal and external logic cells ($V_{CC}$) and for the output emitter followers ($V_{CCA}$) in order to minimize coupling of the output emitter follower switching noise back into the internal and external logic. The chip size is 7.5 mm by 7.2 mm. The bonding pad with 174 μm pitches are used to increase the signal and power terminals.

## VI. Performance

In order to achieve high-speed operation and low power dissipation, the circuit and process parameters have been optimized through circuit simulation and trial production. The general usage condition of 3 fan-in, 3 fan-out having a 3-mm wiring length is used for optimization for high-speed operation in custom circuits. As a result, the internal gate delay of 700 ps (FI = FO = 3 wiring length = 3 mm) and 400 ps (FI = FO = 1) have been achieved in spite of a low power dissipation of 1.9 mW. The fan-out delay coefficient of the internal gate is 0.022 ns/fan-out (Fig. 5) and the interconnect delay coefficient in the internal cells is 0.06 ns/mm (Fig. 6). A typical toggle frequency for flip-flop blocks using series gating is 450 MHz with 7.3-mW power dissipation. The ECL 100K interface provides voltage and temperature compensated output logic levels having less than a 0.2 mV/°C temperature variation and 20 mV/V source voltage variation. The output emitter followers can be connected to −2 V with 50-Ω loads to obtain large drive capability.

The features of this gate array are shown in Table II.

## VII. Package

In order to maintain high-speed operation of the gate array chips, small capacitance and inductance signal terminals are necessary for the package. Good heat transfer

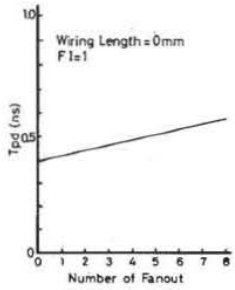


Fig. 5. Propagation delay time of an internal gate versus number of fan-out.

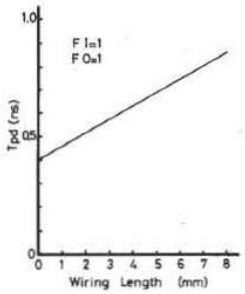


Fig. 6. Propagation delay time of an internal gate versus wiring length.

TABLE II
MAIN FEATURES

| | |
|---|---|
| Interface Level | ECL 100K |
| Equivalent Gates | 2000 |
| Propagation Delay Time | |
| Internal Gate (F I=F O=3 Wiring Length=3mm) | 0.7ns/1.9mW |
| Input Buffer | 0.6ns/1.9mW |
| Output Buffer | 1.0ns/22.5mW |
| Power Dissipation | 6.0W (Typ.) |
| Source Voltage | -4.5V |
| Signal Pins | 108 (Max.) |
| Number of Cells | |
| Internal | 832 |
| External | 48 |
| Packages | 72 or 132 pin pingrid array<br>68 pin leadless chip carrier |

properties and small size are also required for a high packing density implementation. In order to meet these requirements, the ceramic pin-grid array package and 68 pin JEDEC leadless chip carrier have been utilized for this gate array. The 72 pin and 132 pin pin-grid array packages (Fig. 7) have a low thermal resistance of 6°C/W with 4 m/s air flow. Good heat transfer is assued since the LSI chip is mounted on the lid of the package attached to the heat sink.

Due to the low thermal resistance package, this gate array can be used in an air cooled system. Furthermore, the height of the package (from the bottom of the package substrate to the top of the heat sink) was designed to be less than 11 mm. Accordingly, a high packing density of 17 mm pitch between printed circuit boards can be employed.

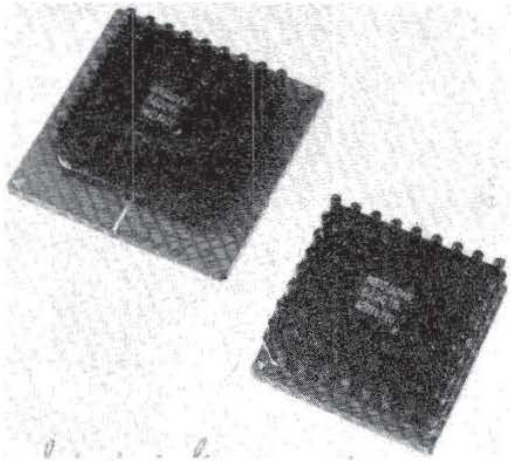

Fig. 7. 72 and 132 pin pin-grid array package.

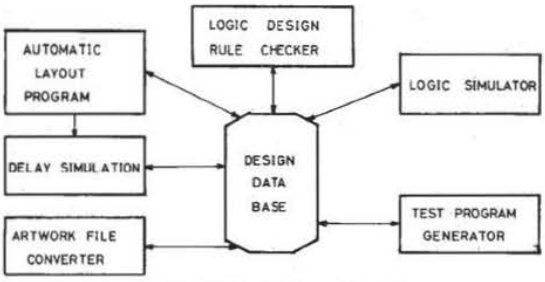


Fig. 8. CAD system configuration.

## VIII. CAD SUPPORT

For quick and error-free design of custom circuit implementation, the integrated CAD system [2] is utilized. The CAD system provides design utilities for all logical and physical design stages (Fig. 8).

This system is based on the design database containing function block connection data, functional test patterns, and pin assignments. In the first design step, the custom circuits are checked by the logic design rule checker to determine if the circuits satisfy the design rules such as number of fan-in and fan-out, and power dissipation. In addition, the function of the circuits are verified by the logic simulator.

An estimation of the propagation delay time is important for the performance verification of a high-speed gate array. In order to assure the customer requirements, the delay simulation assuming typical interconnection length can be performed before layout. After the automatic placement and wiring, precise delay simulation can be accomplished using the actual interconnection length. Using two level interconnection, 100 percent routability has been attained for automatic placement and wiring in spite of 90 percent cell utilization.

In the final steps, a pattern generation tape for a mask maker is created by an artwork file converter, and a test program generator creates the test program for an IC tester.

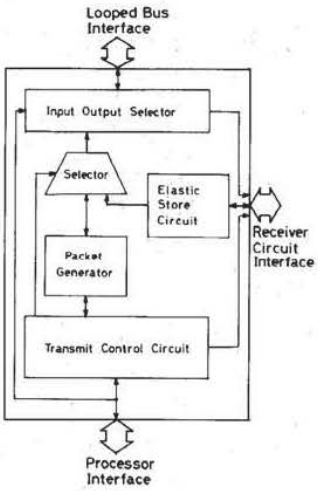


Fig. 9. Block diagram of loop bus controller (LBC).

## IX. Application

Fig. 9 shows a block diagram of the loop bus controller (LBC) using this gate array. Packet data are sent to looped buslines through the loop bus interface under the control of LBC. LBC also has the processor interface and the receiver circuit interface. This LSI has 2039 equivalent gates in spite of 85 percent cell utilization. Due to the high performance of this gate array, an 100-MHz operation has been achieved. In this circuitry, a 4-bit universal counter is implemented using 26 cells, which has 140-mW power dissipation and 1.0-ns propagation delay time from clock to output. In contrast with standard MSI counter chip which has 624-mW and 3.3-ns propagation delay time, a high-performance counter has been realized in this gate array.

This LSI has 5.3-W power dissipation and uses 132 pin pin-grid array package.

## X. Conclusion

A subnanosecond gate array with ECL 100K compatibility has been developed. This gate array has a 700-ps propagation delay time (FI = FO = 3, wiring length = 3 mm), 2000 equivalent gate complexity, and a 132 pin low thermal resistance package. These features have been realized by using an advanced bipolar process, an optimized circuit design, and a good heat transfer package. In addition, a quick and error-free design of customized circuits is realized by the integrated CAD system. This type of gate array will contribute greatly to a high-speed data processing system.

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