

## (12) United States Patent Draper

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(54)	INTEGRATED C	APACITOR	

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(\*) Notice: This patent issued on a continued prosecution application filed under 37 CFR

1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C.

154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35

U.S.C. 154(b) by 0 days.

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(51) **Int. Cl.**<sup>7</sup> ...... **H01L 27/108**; H01L 29/76; H01L 29/94; H01L 31/119

**U.S. Cl.** ...... **257/300**; 257/532

257/532

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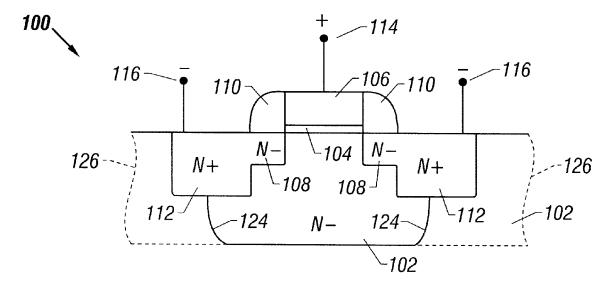
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### **ABSTRACT**

An integrated capacitor includes a device region of first conductivity type in a semiconductor substrate, a source/ drain region of the first conductivity type in the device region with a higher doping concentration than the device region, a gate insulator over the device region, and a gate over the gate insulator. A first terminal is coupled to the source/drain region, and a second terminal is coupled to the gate. Advantageously, the integrated capacitor is operated with the device region beneath the gate driven into accumulation instead of inversion. This allows a lower voltage to be applied to the gate, which allows for a thinner gate insulator to be used resulting in higher capacitance per unit area. Furthermore, since the device region is much thicker and more highly conductive than an inversion layer, the integrated capacitor has greatly improved frequency response.

### 21 Claims, 5 Drawing Sheets







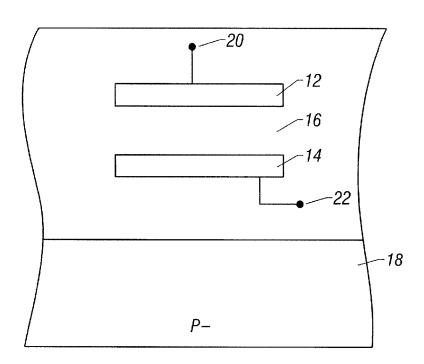


FIG. 1 (Prior Art)

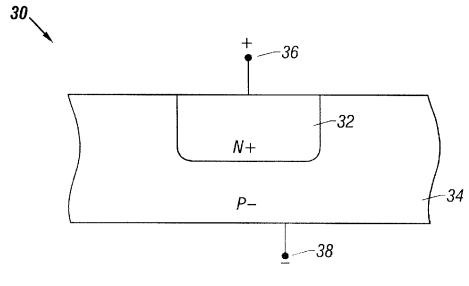


FIG. 2 (Prior Art)

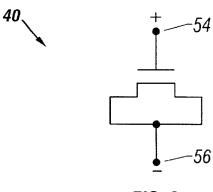


FIG. 3

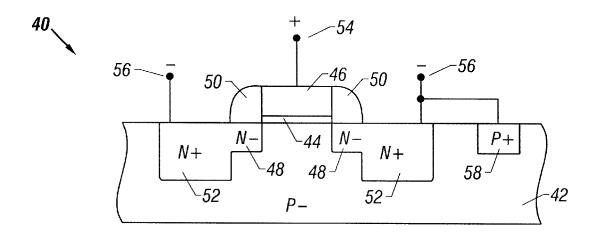
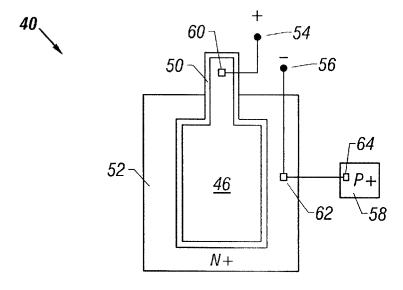
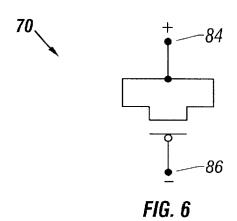


FIG. 4



**FIG.** 5





*70* \ 86 -84 84 -76 -80 80 74 P+ 72-*88 -*/ -72 82 82 N-

FIG. 7

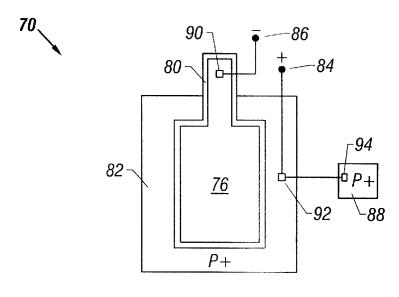
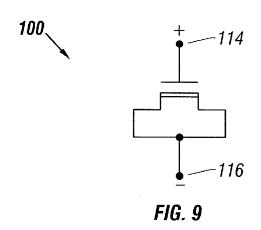


FIG. 8



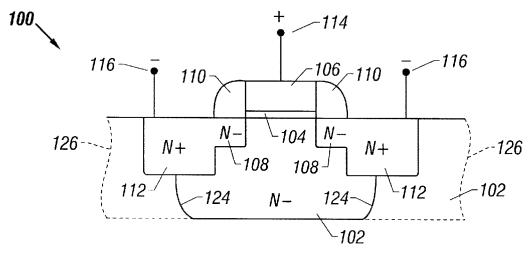
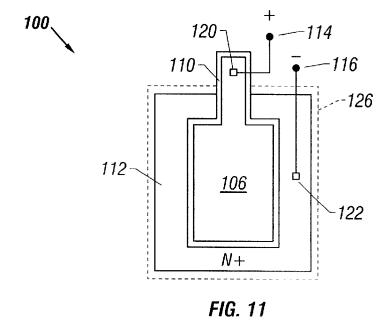


FIG. 10





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