

[54] INTEGRATED CIRCUIT FORMED ON A SEMICONDUCTOR SUBSTRATE WITH A VARIABLE CAPACITOR CIRCUIT

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[75] Inventor: Satoshi Konishi, Tokyo, Japan

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[22] Filed: Dec. 3, 1982

[30] Foreign Application Priority Data

Dec. 15, 1981 [JP] Japan 56-201837
 Jan. 18, 1982 [JP] Japan 57-5680

[51] Int. Cl.³ H03K 4/94; H03K 5/01

[52] U.S. Cl. 307/443; 307/246; 307/451; 307/469; 307/585; 307/268; 307/591

[58] Field of Search 307/443, 448, 451, 468, 307/469, 246, 574-576, 579, 581, 584, 585, 267, 268, 591, 594, 601, 603, 605, 263

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[57] ABSTRACT

A MOS type semiconductor integrated circuit comprising a C-MOS inverter including P- and N-channel MOS transistors connected in series between V_{DD} and V_{SS} power supply terminals, the gates of the MOS transistors being supplied with an input signal; a variable capacitor connected between a node at which the transistors are interconnected and a reference voltage; and a voltage generator for producing an output voltage to the variable capacitor, the voltage generator being capable of irreversibly changing the level of the output voltage, thereby changing a capacitance of the variable capacitor.

23 Claims, 89 Drawing Figures

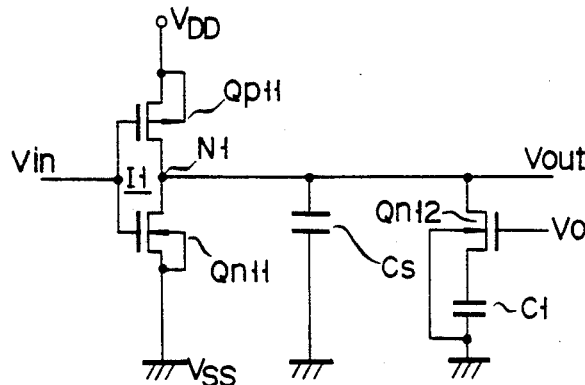
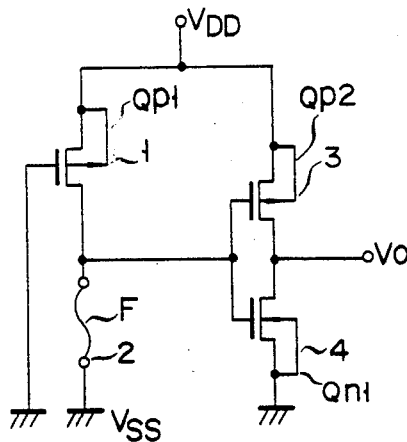


FIG. 1

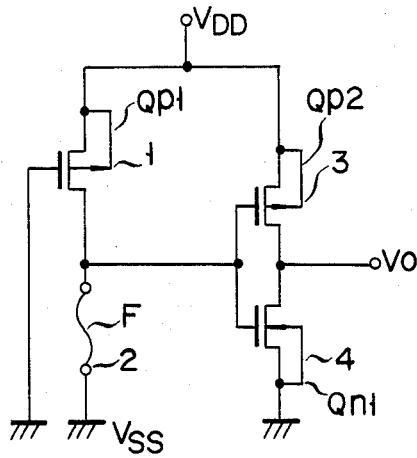


FIG. 2

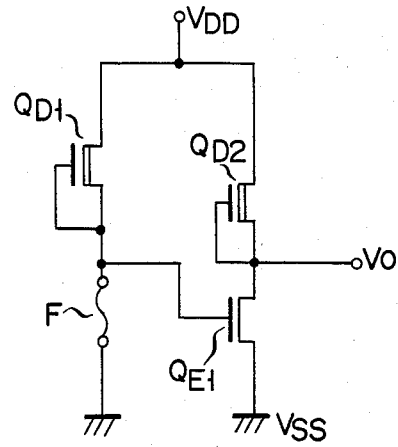


FIG. 3

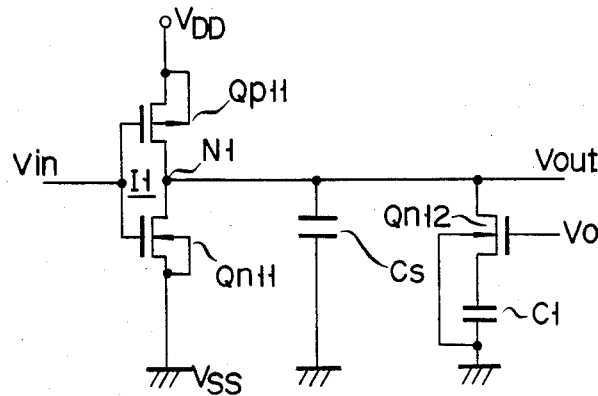


FIG. 4A

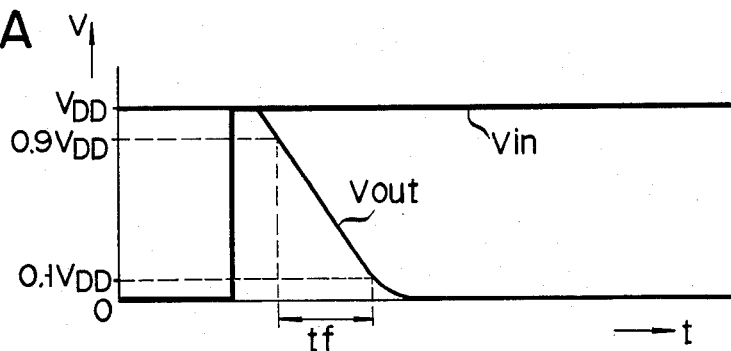


FIG. 4B

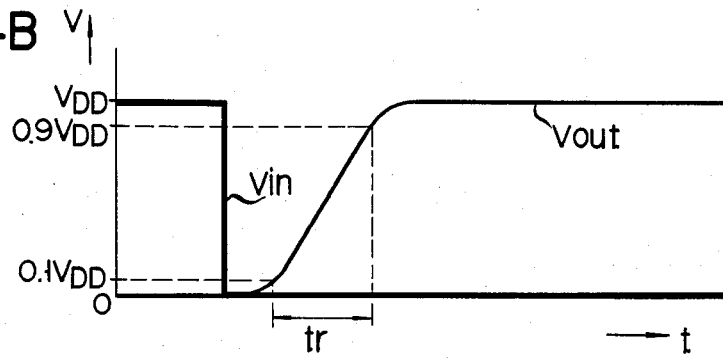


FIG. 4C

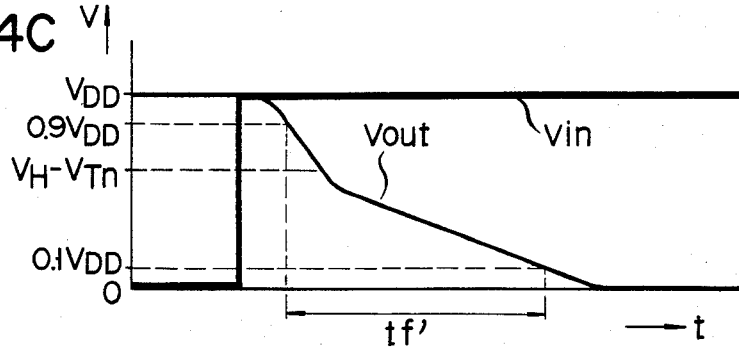


FIG. 4D

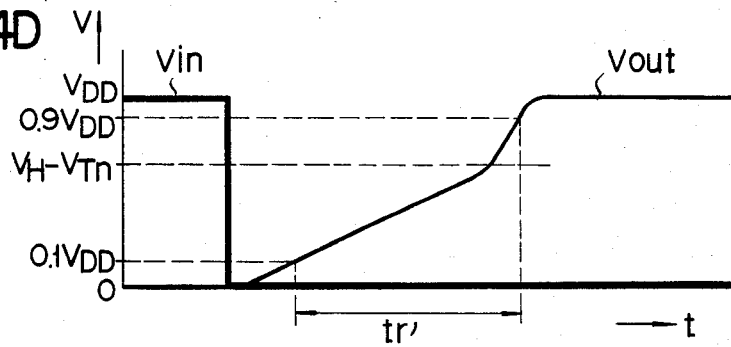


FIG. 5A

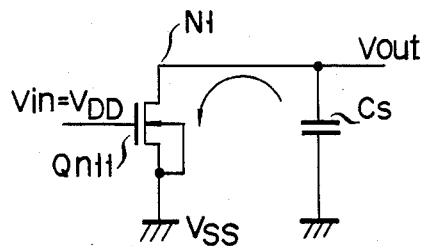


FIG. 5B

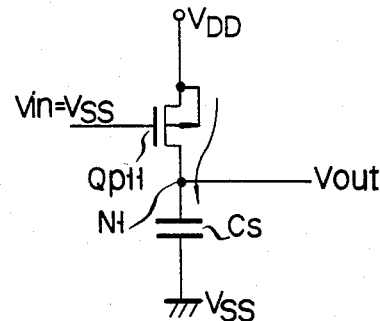


FIG. 5C

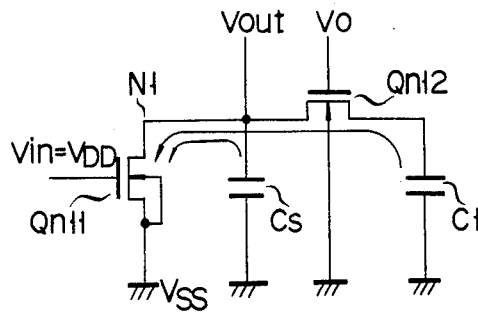


FIG. 5D

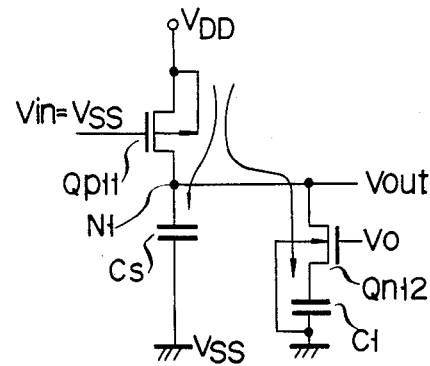


FIG. 6

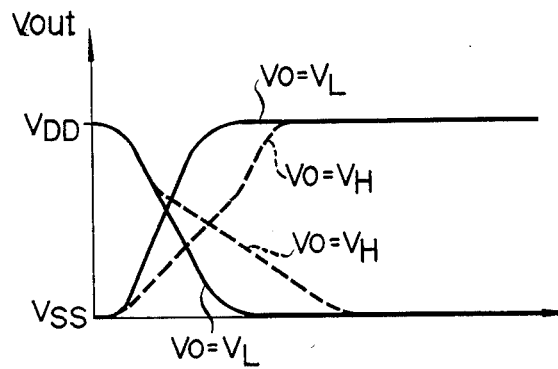


FIG. 7

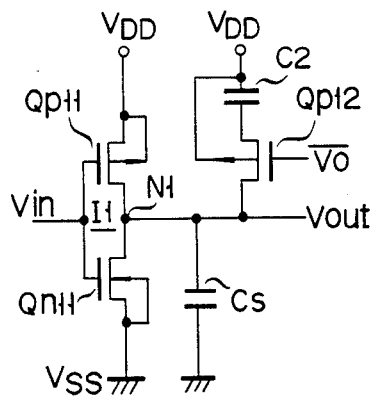


FIG. 8

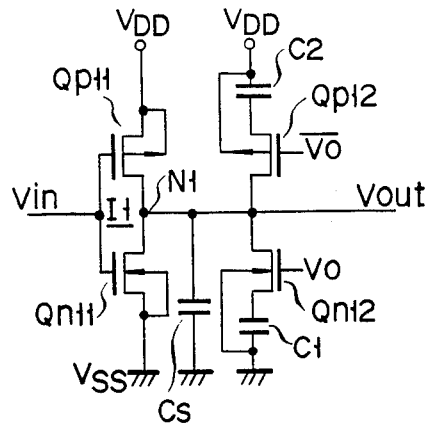


FIG. 9

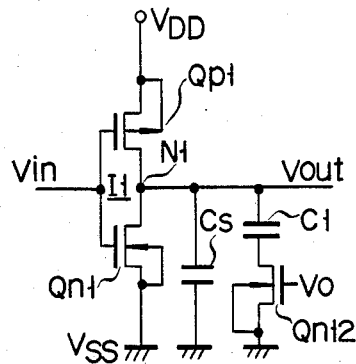


FIG. 10

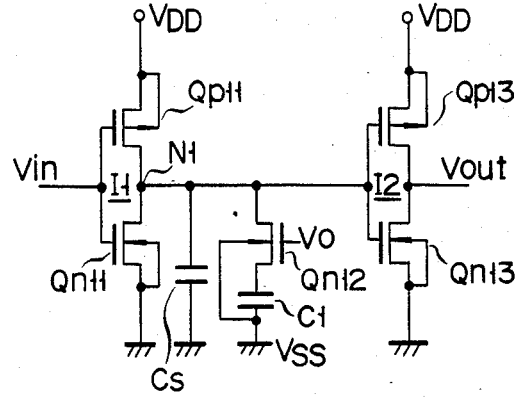


FIG. 11A

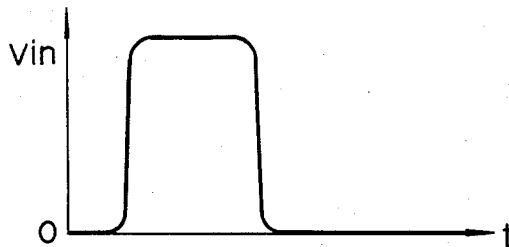


FIG. 11B

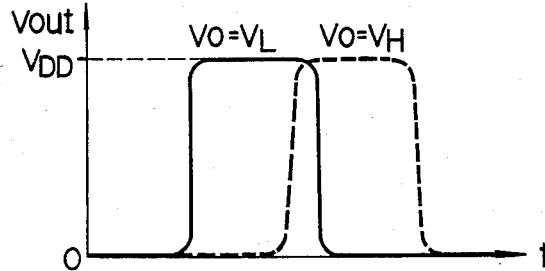
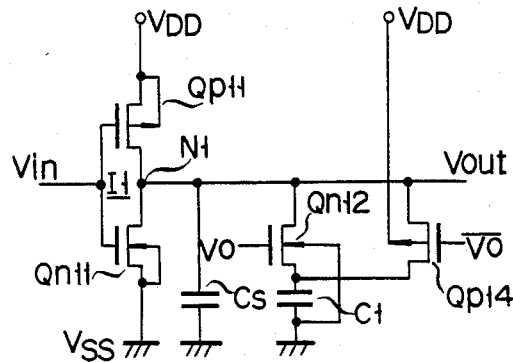


FIG. 12



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