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(54) [Title of the Invention]

Gate Array-Type Integrated Circuit

(57) [Abstract]

[Purpose]

To enable a MT-CMOS circuit to be realized using a gate array integrated circuit.

[Constitution]

A gate array is configured by arranging a second basic cell 3 composed of MOS transistors with a high threshold voltage adjacent to a first basic cell 2 composed of MOS transistors with a low threshold voltage.

[Claims]

[Claim 1]

A gate array-type integrated circuit comprising a first basic cell composed of a field effect transistor and a second basic cell composed of a field effect transistor having an absolute value of the threshold voltage that is greater than that of the field effect transistor constituting the first basic cell, at least one cell array being formed using the first basic cell and another cell array being formed using the second basic cell, and the cell array composed of the second basic cell being arranged adjacent to the cell array composed of the first basic cell, at any end vertically or horizontally, at both ends horizontally, at both ends vertically, at all ends vertically and horizontally, or inside the first basic cell.

[Claim 2]

A gate array-type integrated circuit according to claim 1, wherein a group of logic circuits is formed in the first basic cell, and a power supply control circuit is formed in the second basic cell to control the supply of power to the group of logic circuits.

[Claim 3]

A gate array-type integrated circuit according to claim 1, wherein the integrated circuit comprises a group of logic circuits formed using transistors constituting the first basic cell and having a first and second power supply terminal, a first and/or second power supply control circuit formed using transistors constituting the second basic cell for controlling the supply of power to the group of logic circuits, first and second actual power supply lines constituting the power supply source to the group of logic circuits, and a first and/or second pseudo-power supply line, the first actual pseudo power supply line being connected to the first power supply terminal of the group of logic circuits, the first power supply control circuit being connected between the first pseudo power supply line and the first actual power supply line, and a second power supply line being connected directly to the second power supply terminal of the group of logic circuits, or a second power supply control circuit being connected to the second pseudo power supply line and between the second pseudo power supply line and the second actual power supply line.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to a semiconductor integrated circuit configured in gate array style and, more specifically, to a gate array-type integrated circuit compatible with CMOS circuits for low-voltage/high-speed operation composed of a transistor with a high threshold voltage and a transistor with a low threshold voltage.

[0002]

[Prior Art]

A gate array-type semiconductor integrated circuit realizes the desired circuit function by arranging a plurality of basic cells made of a plurality of transistor elements in matrix

fashion on a semiconductor wafer and wiring the basic cells together. In this way, an integrated circuit can be obtained in a short period of time.

[0003]

FIG. 10 is a schematic diagram of an LSI chip with a gate array in the prior art (Reference Document: "ULSI Design Technology," Takuo OGINO, supervisor, The Institute of Electronics, Information and Communication Engineers). Basic cells 12 are arranged in matrix fashion in the central portion of the LSI chip 11 to form a cell array 12A. Input/output cell arrays 13 are arranged on the outer periphery to form an interface with outside components.

[0004]

FIG. 11 is a diagram used to explain a CMOS gate array-type basic cell 12 used in the prior art. Q11 and Q12 are P channel-type MOS field effect transistors (referred to simply as MOS transistors below), Q13 and Q14 are N channel-type MOS transistors, and both are used as transistors forming logic gates.

[0005]

In order to explain an example in which transistors are formed on a P type substrate, P channel MOS transistors Q11 and Q12 are formed in n well 121. Here, 122 is a p^+ region functioning as a source or drain for a P channel MOS transistor, 123 is an n^+ region functioning as a source or drain for an N channel MOS transistor, and 124 is a gate electrode.

[0006]

Although the transistors Q11 and Q12 may vary in size, the threshold voltages are set to the same value because it has a significant effect on device characteristics. The same applies to transistors Q13 and Q14.

[0007]

FIG. 12 shows a connection example realizing a two-input NAND gate, and FIG. 13 shows the equivalent circuit in this example. The black circles in FIG. 12 indicate the contact positions for a source, drain, or gate electrode in a MOS transistor. Also, A1 and A2 are input terminals, Y is an output terminal, VDD is a high potential actual power supply line, and VSS is a low potential actual power supply line.

[0008]

In order to meet demand for portable electronic devices, progress has been made in recent years on low-voltage operation of semiconductor integrated circuits. An example of this technology is the multi-threshold CMOS (MT-CMOS) circuit described in the Spring 1994 Conference Proceedings of the Institute of Electronics, Information and Communication Engineers, Vol. 5, pp. 5-195 shown in FIG. 14.

[0009]

In FIG. 14, the transistors Q21 to Q24 constituting the logic circuit (two-input NAND gate) 14 are low threshold voltage transistors. The power supply terminal on the high potential

side of the logic circuit 14 is connected to a high potential pseudo power supply line VDDV, and the power supply terminal on the low potential side is connected to a low potential actual power supply line VSS. A MOS transistor for controlling the high threshold voltage power QH11 is connected between the high potential pseudo power supply line VDDV and the high potential actual power supply line VDD. A sleep signal SL for the power control is inputted to the gate of MOS transistor QH11.

[0010]

During operation, the sleep signal SL is set to a low potential. As a result, the PMOS transistor QH11 becomes conductive, and the high potential pseudo power supply line VDDV can be regarded as a high potential actual power supply line VDD. At this time, because the logic circuit 14 connected to the high potential pseudo power supply line VDDV is composed of MOS transistors Q21 to Q24 with low threshold voltage, it operates at high speed even at an extremely low voltage of 1 V or less.

[0011]

In general, a MOS transistor experiences a problem in which leakage current blocking capacity is reduced when the absolute value of the threshold voltage is lowered and the current is increased during standby (during cutoff). In MT-CMOS circuit technology, a power control function known as sleep control is introduced to avoid this problem. In other words, the circuit is put to sleep when the circuit is not in operation. Specifically, the sleep signal SL is set to a high potential, and the P channel MOS transistor QH11 is cut off. Because the cut off high threshold voltage P channel MOS transistor QH11 is interposed between the high potential actual power supply line VDD and the low potential actual power supply line VSS, the standby leakage current that occurs in low threshold voltage MOS transistors Q21 to Q24 can be cut off and ultra-low power characteristics can be realized.

[0012]

As a result, MT-CMOS circuit technology shows promise as a low-voltage/high-speed circuit technology. However, transistors with a high threshold voltage and transistors with a low threshold voltage have to be combined on a single LSI chip in order to realize this circuit in an actual LSI.

[0013]

[Problem to be Solved by the Invention]

However, in the conventional gate array used widely in simple LSI implementation methods, both P channel MOS transistors and N channel MOS transistors are simply arrayed and configured in basic cells consisting of MOS transistors, each having a single threshold voltage.

[0014]

It is an object of the present invention to enable the MT-CMOS circuit technology using field effect transistors with different threshold voltages to be realized using a gate array integrated circuit.

[0015]

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