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Ramus et al.

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[54] **STANDARD CELL HAVING A CAPACITOR AND A POWER SUPPLY CAPACITOR FOR REDUCING NOISE AND METHOD OF FORMATION**

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[73] Assignee: **Motorola**, Schaumburg, Ill.

[21] Appl. No.: **632,690**

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Related U.S. Application Data

[63] Continuation of Ser. No. 184,167, Jan. 21, 1994, abandoned.

[51] **Int. Cl.**^{6} **H01L 29/00**

[52] **U.S. Cl.** **257/532**; 257/401

[58] **Field of Search** 307/576; 257/299, 257/207, 208, 532, 401

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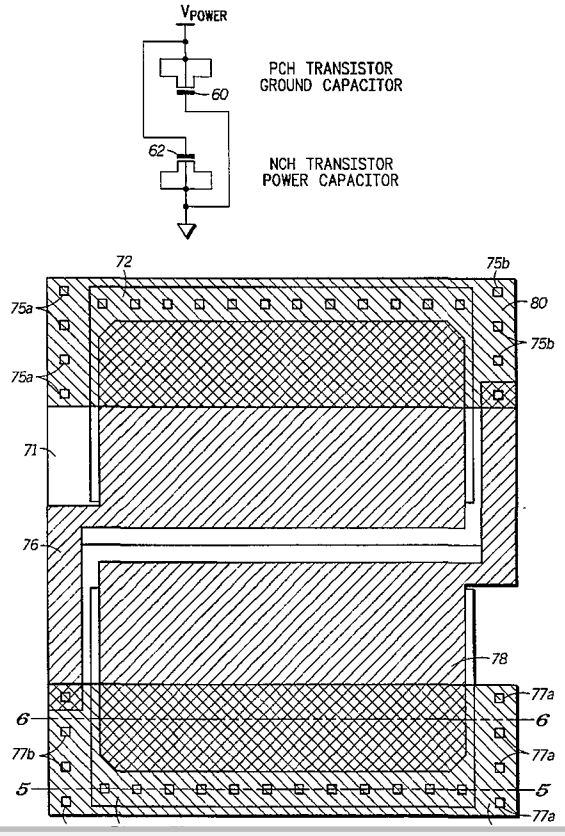
[57] **ABSTRACT**

An integrated circuit (**10**), which is designed using standard cells (**20**, **22**, **24**, **26**, **28**, **30**, **32**, **34**, **35**, **36**, **37**, **28**, **40**, **42**, **44**, **46**, **48**, **50**, **52**), usually has one or more empty spaces (**54**) wherein no circuitry is formed. These empty spaces may be used to form capacitor standard cells which have capacitors (see FIGS. **3** and **4**) to both ground and power supply lines within the integrated circuit. These capacitors are used to reduce noise in the power and supply lines in a manner more useful/efficient than known methods. The capacitor standard cell taught herein is more useful/efficient due to the fact that the capacitance provided by these standard cells is distributed over the entire integrated circuit in small portions (i.e., standard cells are placed all over the integrated circuit (**10**)), and is placed close to the logic which is switching. It is the switching logic which is the root of a large portion of internal integrated circuit noise.

18 Claims, 3 Drawing Sheets



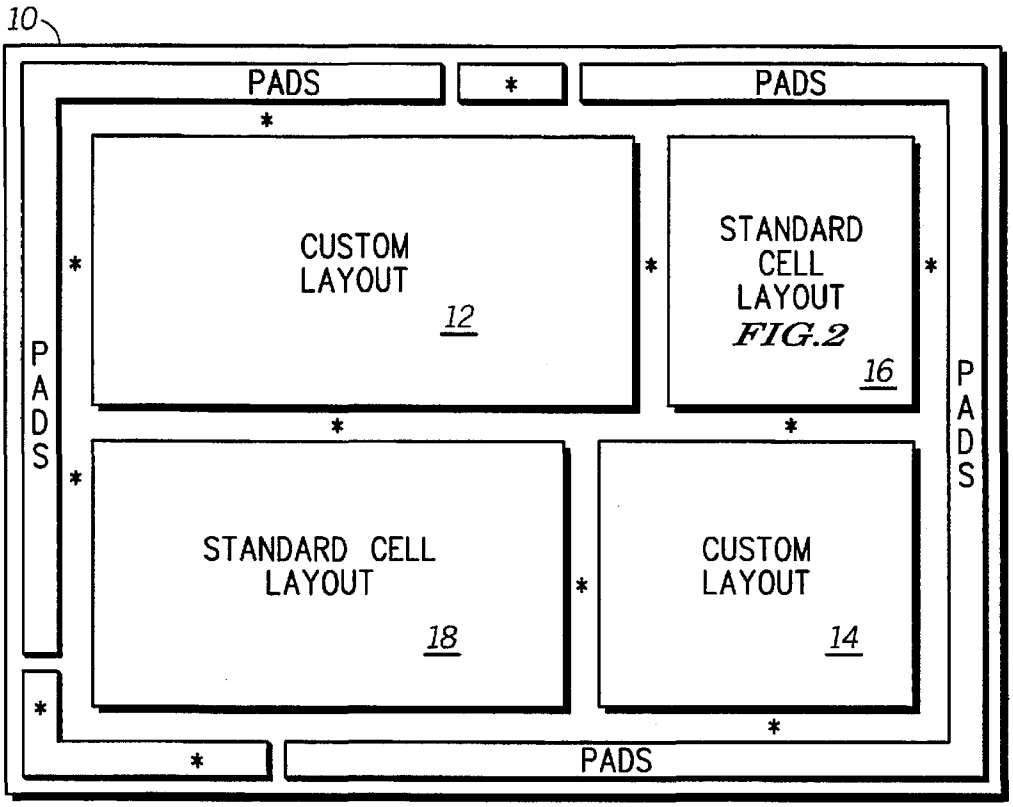


FIG.1

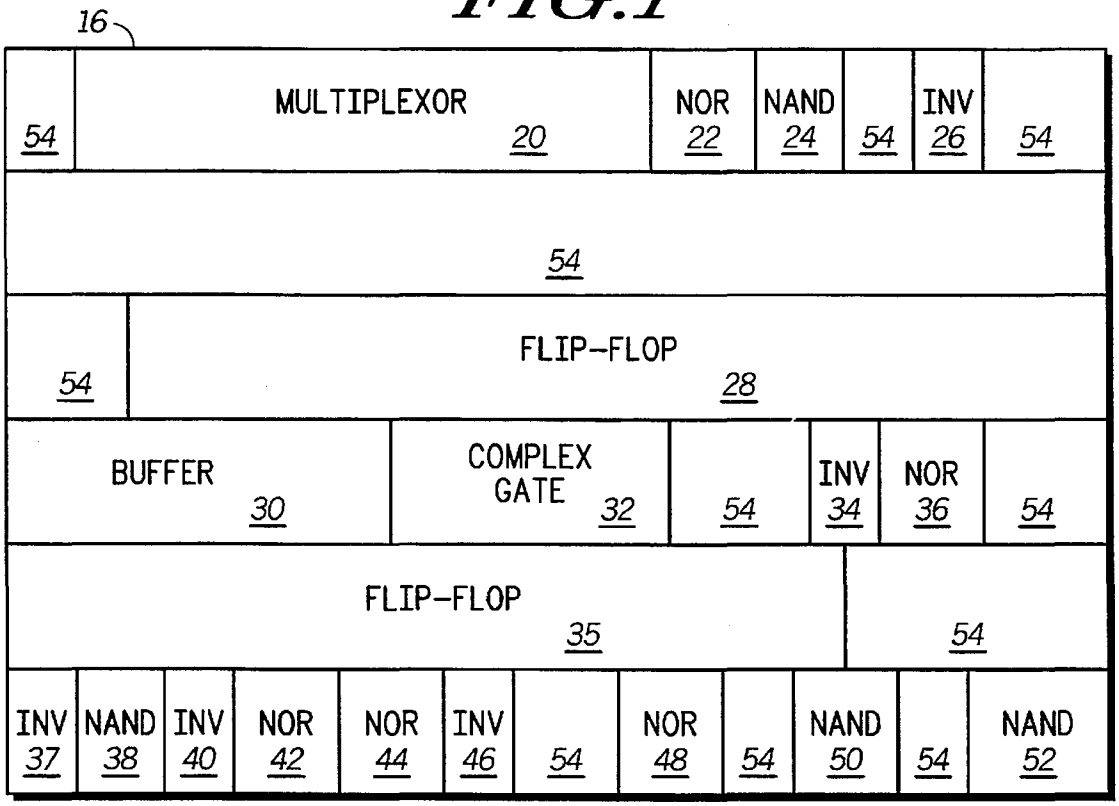


FIG.2

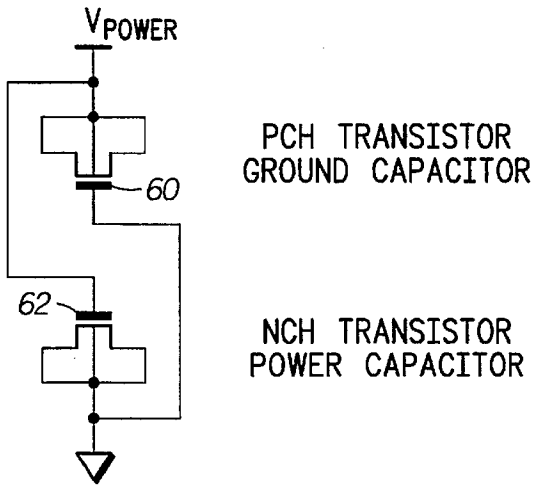


FIG.3

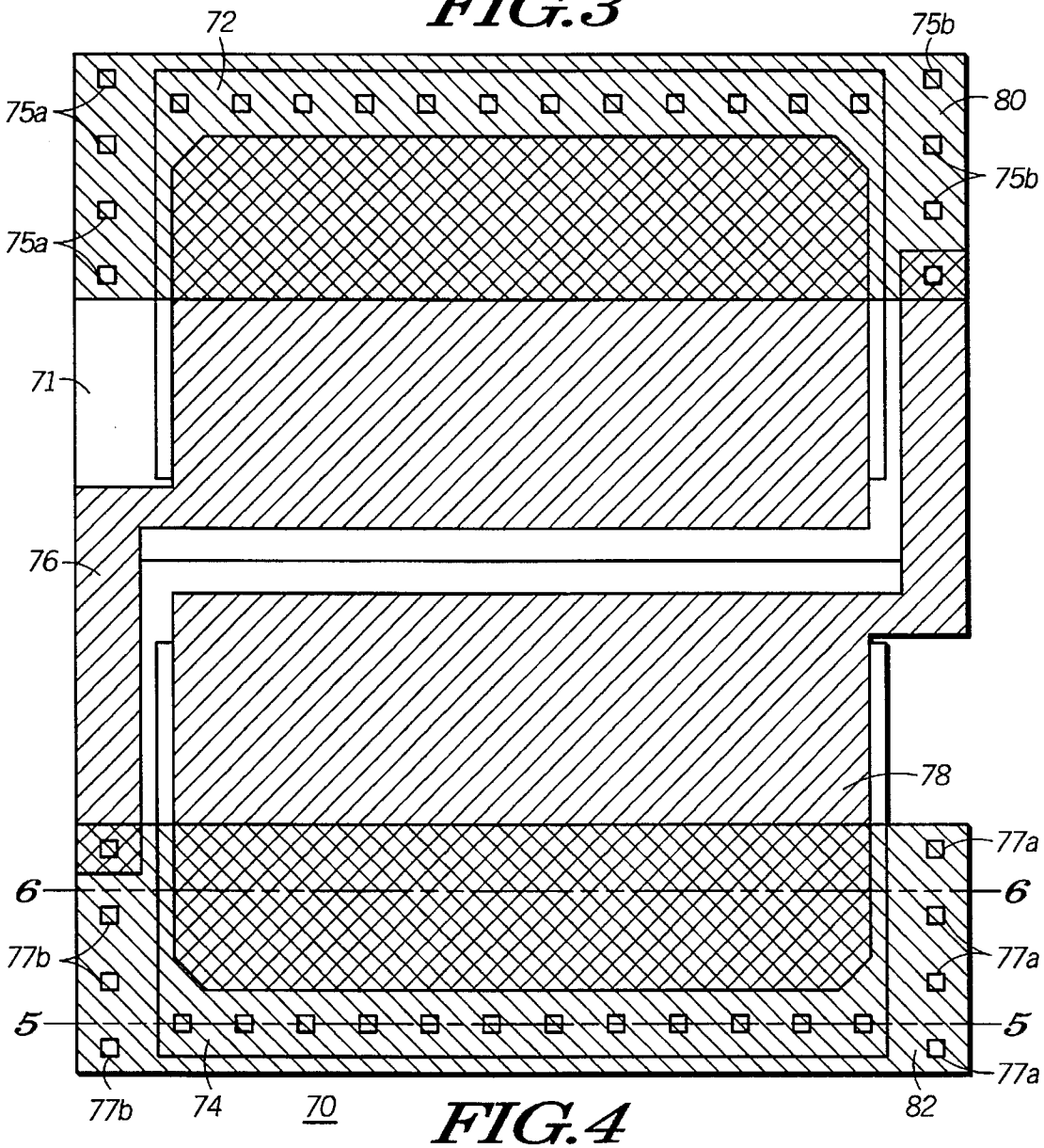


FIG.4

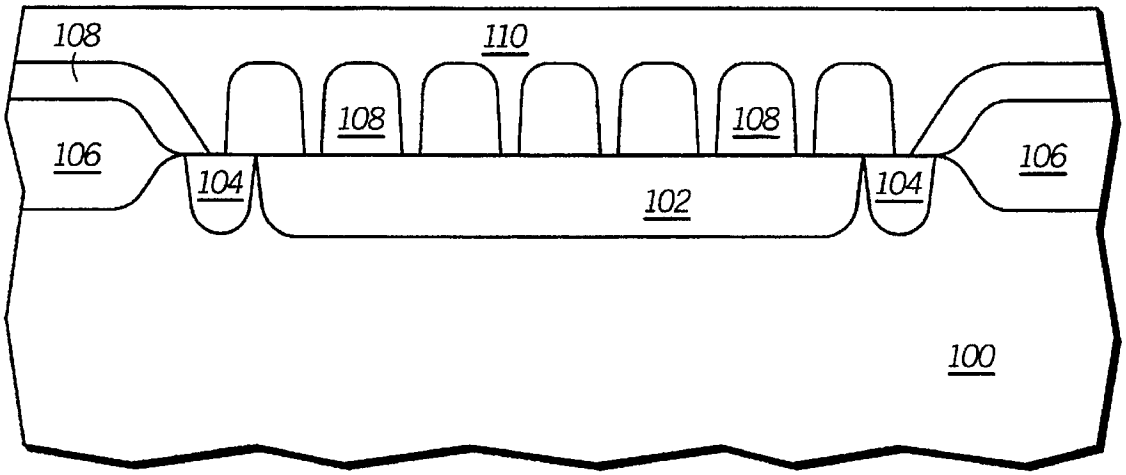


FIG.5

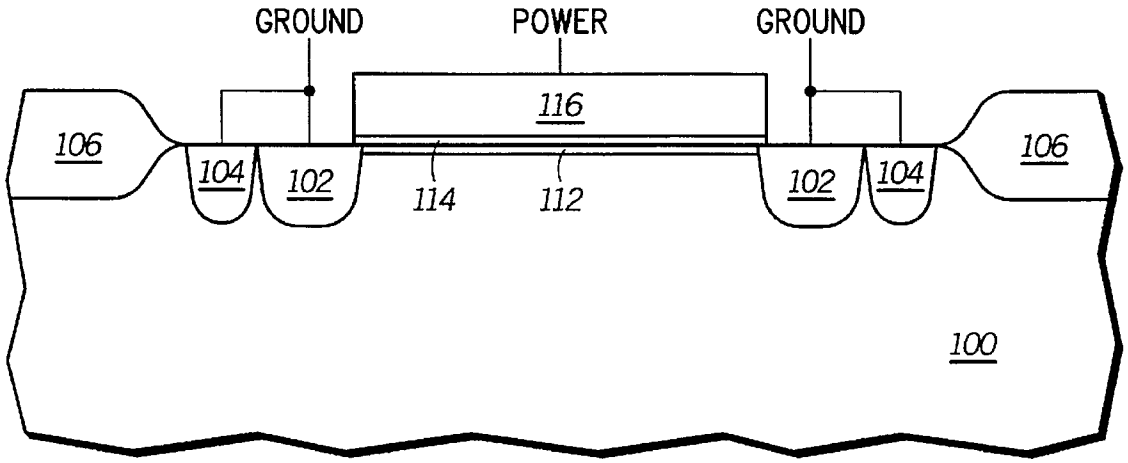


FIG.6

STANDARD CELL HAVING A CAPACITOR AND A POWER SUPPLY CAPACITOR FOR REDUCING NOISE AND METHOD OF FORMATION

This application is a continuation application Ser. No. 08/184,167, filed on Jan. 21, 1994 entitled A STANDARD CELL HAVING A CAPACITOR AND A POWER SUPPLY CAPACITOR FOR REDUCING NOISE AND METHOD OF FORMATION now abandoned.

FIELD OF THE INVENTION

The present invention relates generally to semiconductor circuits, and more particularly, to a standard cell decoupling capacitor circuit.

BACKGROUND OF THE INVENTION

Current capacitive methods and structures for reducing noise on an integrated circuit (IC) are not always adequate. For example, previous implementations of capacitance would include a capacitor residing on the circuit board or package containing the device. Such capacitance is inherently inferior to a capacitance directly resident on the semiconductor device because it is isolated by the board and package inductance, thus severely reducing its effectiveness in providing noise immunity. Another prior art method is to include capacitors on an integrated circuit but place the capacitors far from the switching logic in which it is to reduce noise (usually capacitors are positioned at the periphery of an IC, and not in standard cell layout blocks). Again, other capacitances, line resistance, inductance, timing delays, and physical separation reduce the effectiveness of this technique. In other words, by not being located immediately adjacent to the standard cells, a significant amount of resistance (etc.) exists between the capacitor cells and the actual switching logic. This reduces the amount of transient current the capacitor can provide, which limits its noise suppression capability and will slow down the speed of the switching circuits. Widening the metal conductors connecting the switching logic to the capacitor cells would overcome this, but at the expense of device area consumed by the widened power and ground buses. Another prior art method is to use the inherent capacitance in the well and substrate normally present in the spacer cells of a standard cell block as the capacitor cell. The severe drawback to this is the total amount of capacitance provided is not nearly enough to suppress any noise appearing on the power and/or ground conductors. At least two orders of magnitude greater capacitance must be provided to accomplish a reduction in power and ground noise.

SUMMARY OF THE INVENTION

The previously mentioned disadvantages are overcome and other advantages achieved with the present invention. In one form, the present invention comprises an integrated circuit having a first standard cell, a second standard cell, and a capacitor circuit. The first standard cell performs a predetermined function and has a power conductor and a ground conductor. The second standard cell performs a predetermined function and has the power conductor and the ground conductor. The capacitor circuit has a first conductive region coupled to the power conductor. The first conductive region overlying a first active region which is coupled to the ground conductor. The capacitor circuit has a second conductive region separated from the first conductive

the ground conductor. The first conductive layer overlies a second active region which is coupled to the power conductor.

In another form, the invention comprises an integrated circuit standard cell, a standard cell layout, and a semiconductor device structure.

In yet another form, the invention comprises a method for forming an integrated circuit. The method begins by providing a substrate. A gate oxide dielectric layer is formed overlying the substrate. A conductive layer is formed overlying the gate oxide dielectric layer. The conductive layer is patterned wherein a first portion of the conductive layer forms at least one standard cell capacitor between the substrate and the conductive layer, and a second portion of the conductive layer is used as a gate electrode for a standard cell logic device.

The present invention will be more clearly understood from the detailed description below in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates, in a top perspective view, an integrated circuit having standard cells in accordance with the present invention;

FIG. **2** illustrates, in a top perspective view, a standard cell logic block portion of an integrated circuit in accordance with the present invention;

FIG. **3** illustrates, in a circuit schematic, a capacitor circuit standard cell used for reducing signal noise, the cell being in accordance with the present invention; and

FIG. **4** illustrates, in a top perspective view, a capacitor layout for the circuit of FIG. **3** in accordance with the present invention;

FIG. **5** illustrates, in a cross-sectional diagram, a cross-section of the FIG. **4** along line B–B' in accordance with the present invention; and

FIG. **6** illustrates, in a cross-sectional diagram, a cross-section of the FIG. **4** along line A–A' in accordance with the present invention.

It will be appreciated that for simplicity and clarity of illustration, elements illustrated in the FIGURES have not necessarily been drawn to scale. For example, the dimensions of some of the elements are exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals have been repeated among the FIGURES to indicate corresponding or analogous elements.

DESCRIPTION OF A PREFERRED EMBODIMENT

Generally, the present invention provides a circuit, a layout, and/or a semiconductor device which is implemented as a standard cell for use in a data processor or an integrated circuit. The circuit, layout, and/or semiconductor device which is implemented as a standard cell includes at least one capacitor and is, in a preferred form, placed several times in several locations within an integrated circuit to reduce power supply and ground supply noise internal to the integrated circuit, and to improve switching speed of the circuits in the integrated circuit. Specifically, the present invention provides a standard cell design with high capacitance (around 20 nF) located adjacent to a group of standard cell logic (i.e., NAND, NOR, multiplexor, flip-flop, counter, etc.). The capacitor is formed as a power capacitor and a

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