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United States Patent [19]

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Douseki et al.

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[54] **CMOS LOGIC CIRCUITS HAVING LOW AND HIGH-THRESHOLD VOLTAGE TRANSISTORS**

[75] Inventors: **Takakuni Douseki; Junzo Yamada; Yasuyuki Matsuya; Shinichirou Mutou**, all of Kanagawa, Japan

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[73] Assignee: **Nippon Telegraph and Telephone Corporation**, Tokyo, Japan

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[21] Appl. No.: **333,235**

[22] Filed: **Nov. 2, 1994**

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Related U.S. Application Data

[63] Continuation of Ser. No. 981,183, Nov. 24, 1992, abandoned.

Foreign Application Priority Data

Nov. 26, 1991	[JP]	Japan	3-311007
Dec. 6, 1991	[JP]	Japan	3-323382
Dec. 9, 1991	[JP]	Japan	3-324512
Feb. 3, 1992	[JP]	Japan	4-017537

Primary Examiner—Edward P. Westin
Assistant Examiner—Benjamin D. Driscoll
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[51] Int. Cl.⁶ **H03K 19/0948**

[52] U.S. Cl. **326/33; 326/81; 327/541**

[58] Field of Search 307/443, 451, 307/475, 473, 296.8; 326/33, 81, 58; 327/541

[57] ABSTRACT

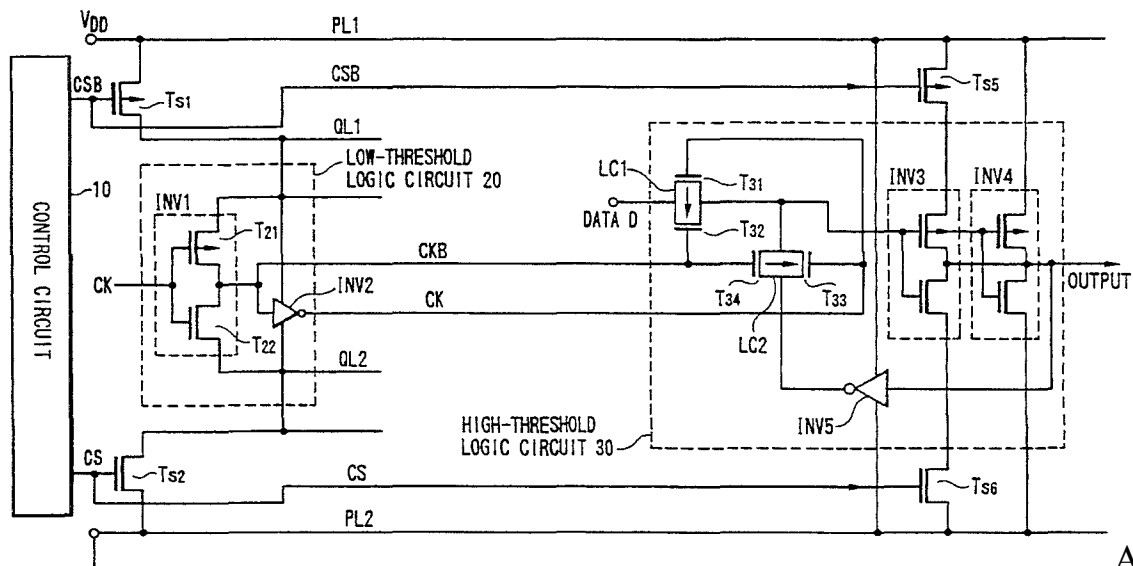
A logic circuit includes a low-threshold logic circuit, a pair of first and second power lines, a first dummy power line, and a first high-frequency logic circuit. The low-threshold logic circuit has a logic circuit element constituted by a plurality of low-threshold field effect transistors. The pair of first and second power lines supply power to the low-threshold logic circuit. The first dummy power line is connected to one of power source terminals of the low-threshold logic circuit. The first high-threshold control transistor is arranged between the first dummy power line and the first power line.

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11 Claims, 9 Drawing Sheets



AMD EX1010

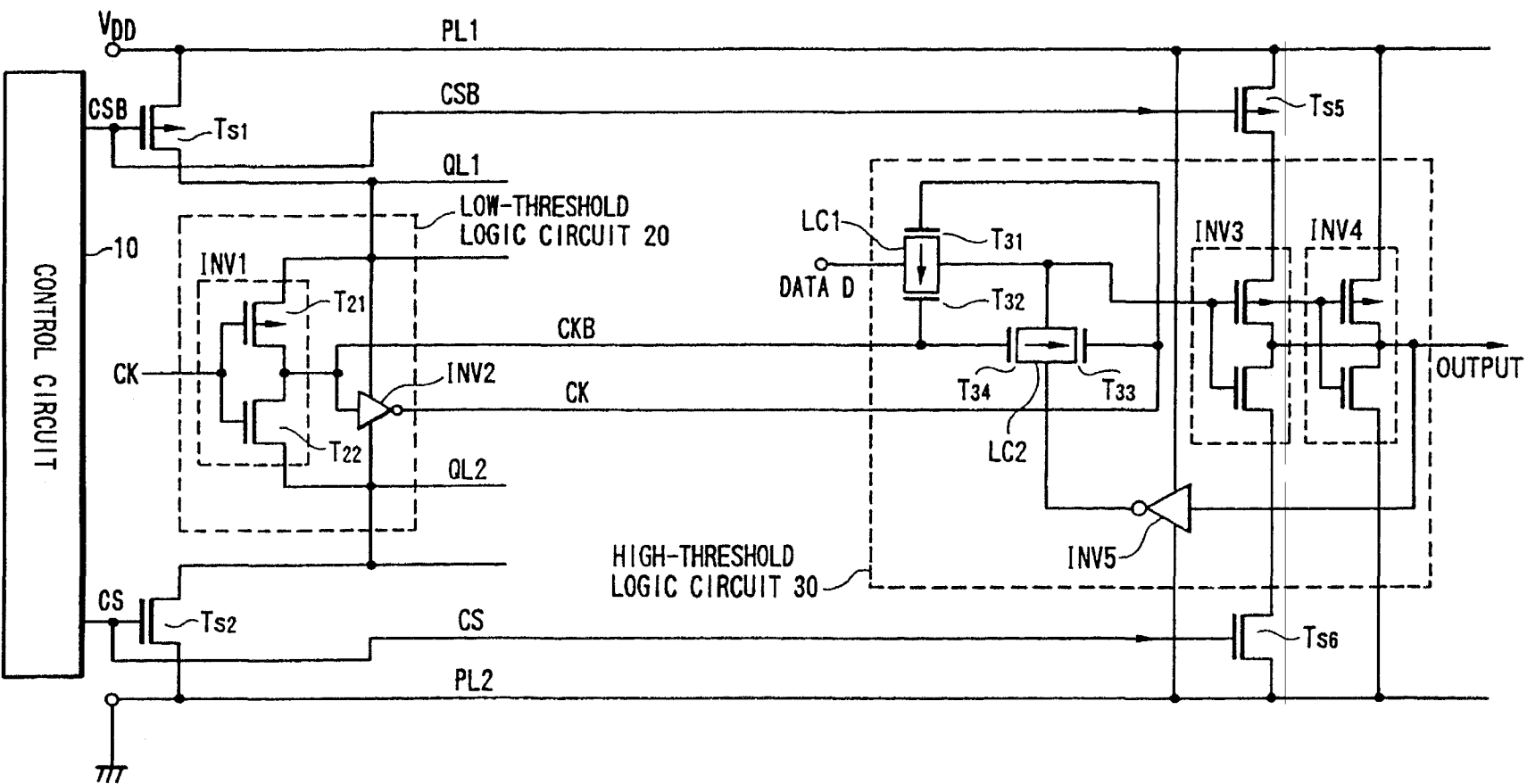


FIG. 1

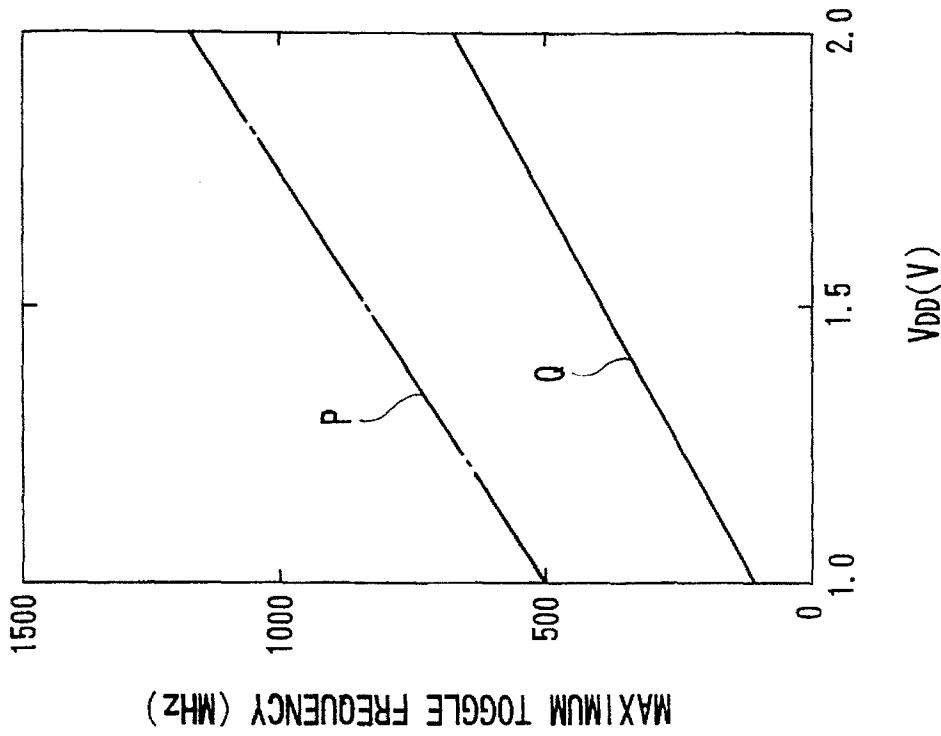


FIG.3

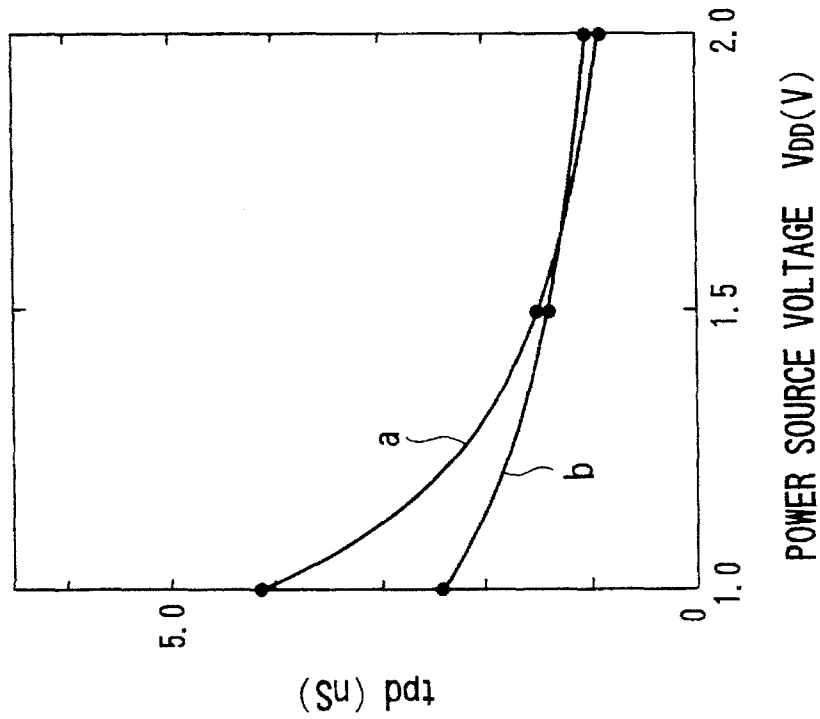


FIG.2

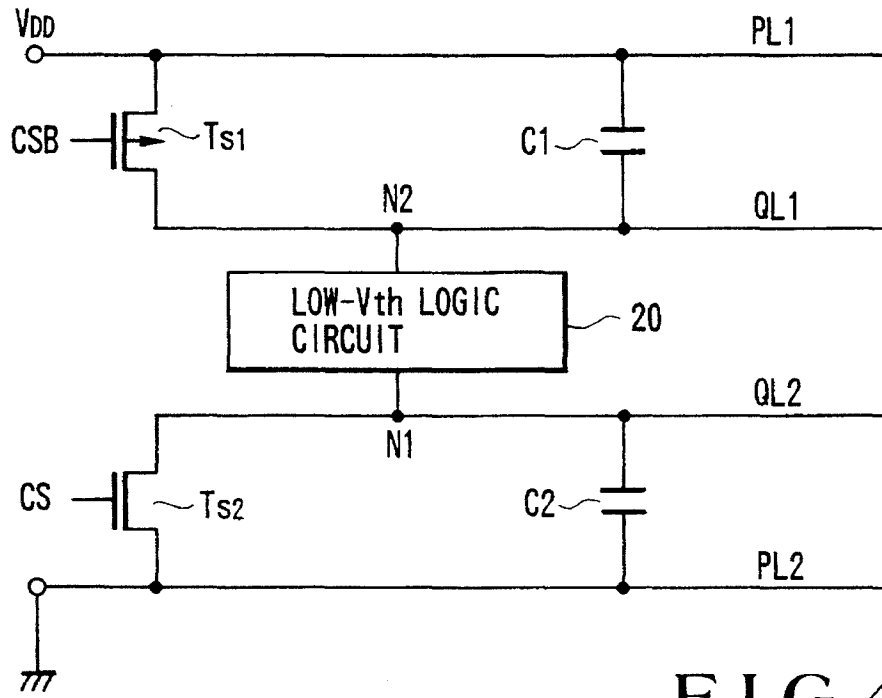


FIG.4

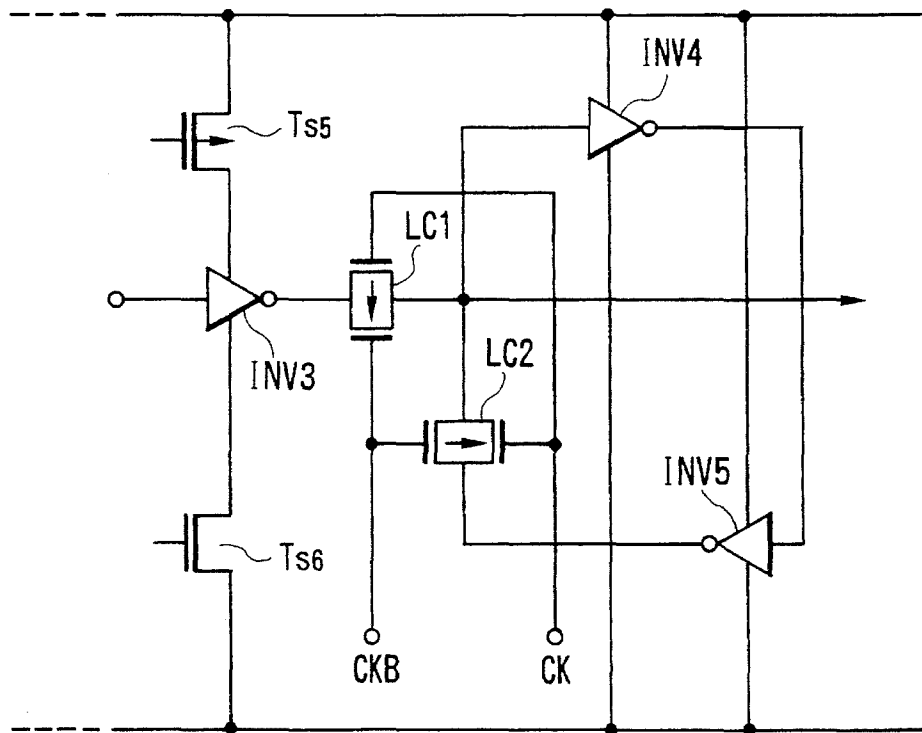


FIG.5

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