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Makino

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(54) **SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE**

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(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(30) **Foreign Application Priority Data**

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(51) Int. Cl.⁷ **H01L 21/8232**

(52) U.S. Cl. **257/391; 257/392; 257/393; 257/401**

(58) Field of Search **257/372, 379, 257/390, 391, 401, 909, 206, 392, 393**

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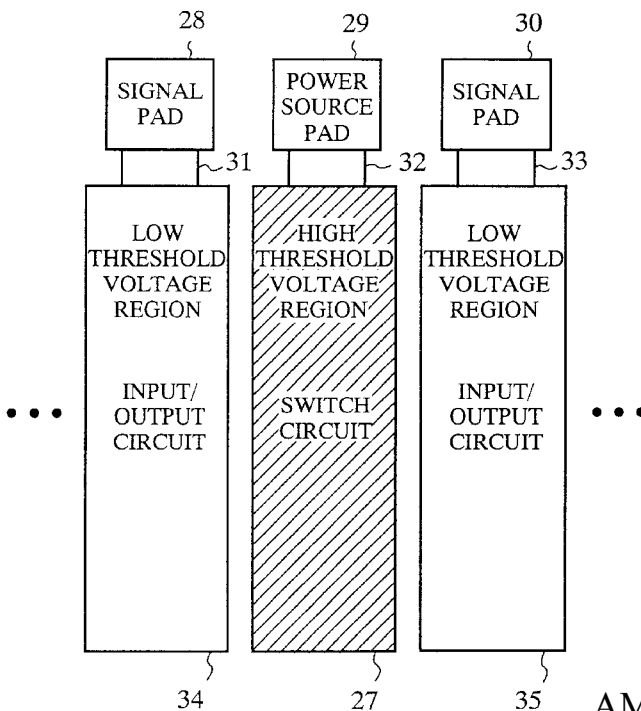
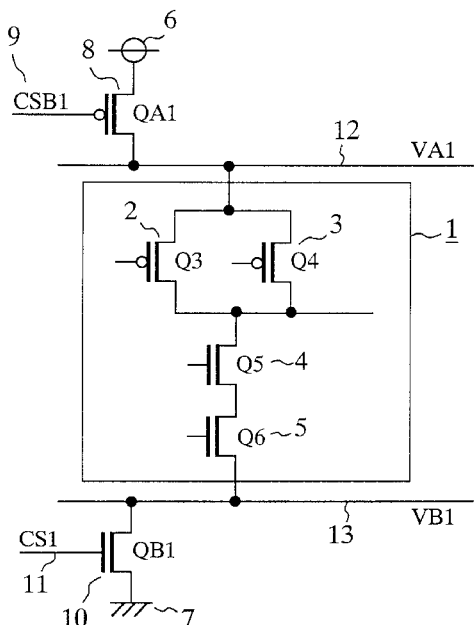
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(57) **ABSTRACT**

A semiconductor integrated circuit device of a low power consumption capable of performing under a low voltage has an array section 21 in which only low threshold voltage MOS FETs are formed, and areas other than the array section 21 in which high threshold voltage MOS FETs whose threshold voltage is higher than that of each low threshold voltage MOS FET formed in the array section are formed.

5 Claims, 8 Drawing Sheets



AMD EX1006

FIG. 1

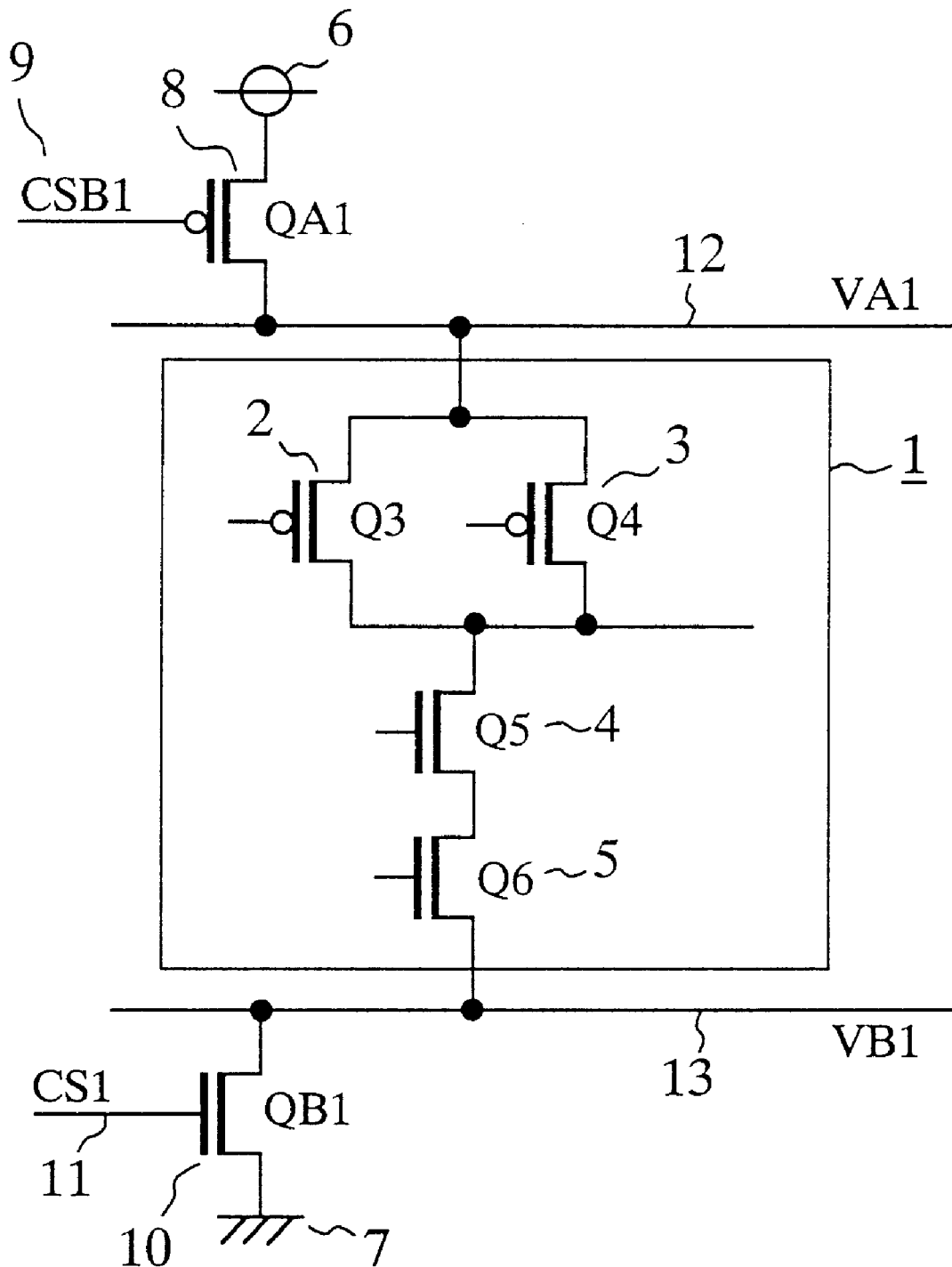


FIG.2(PRIOR ART)

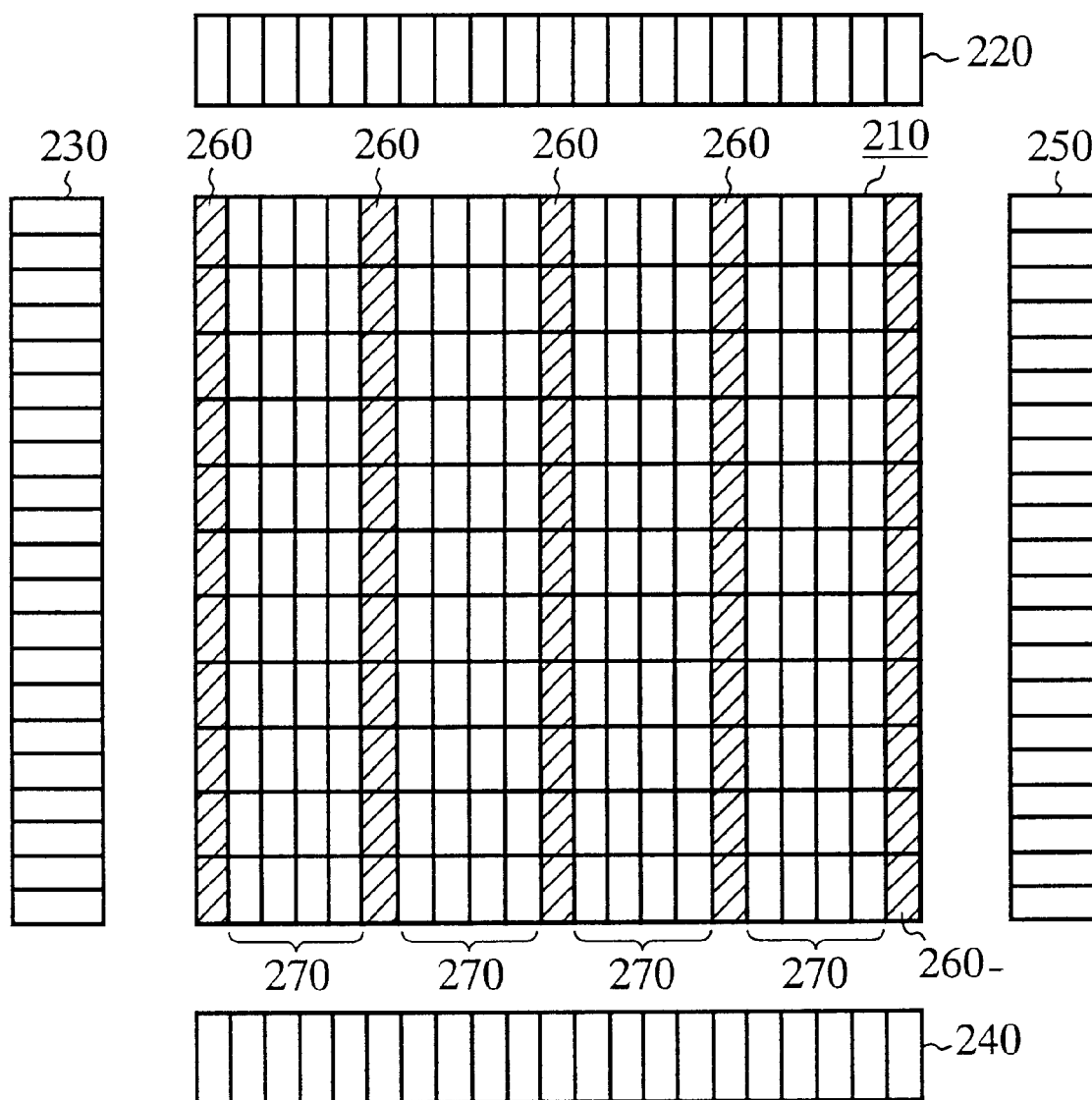


FIG. 3

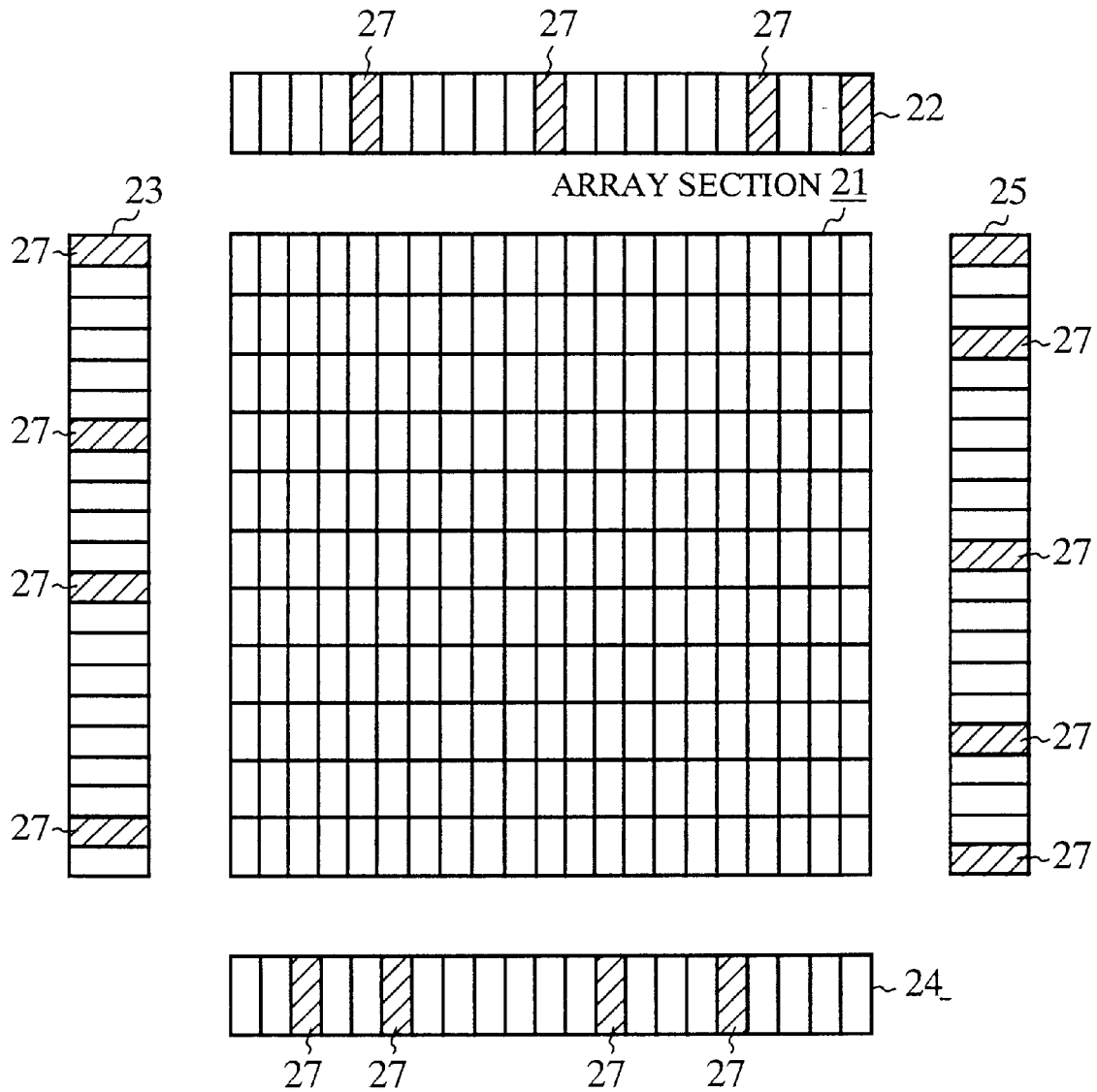


FIG.4

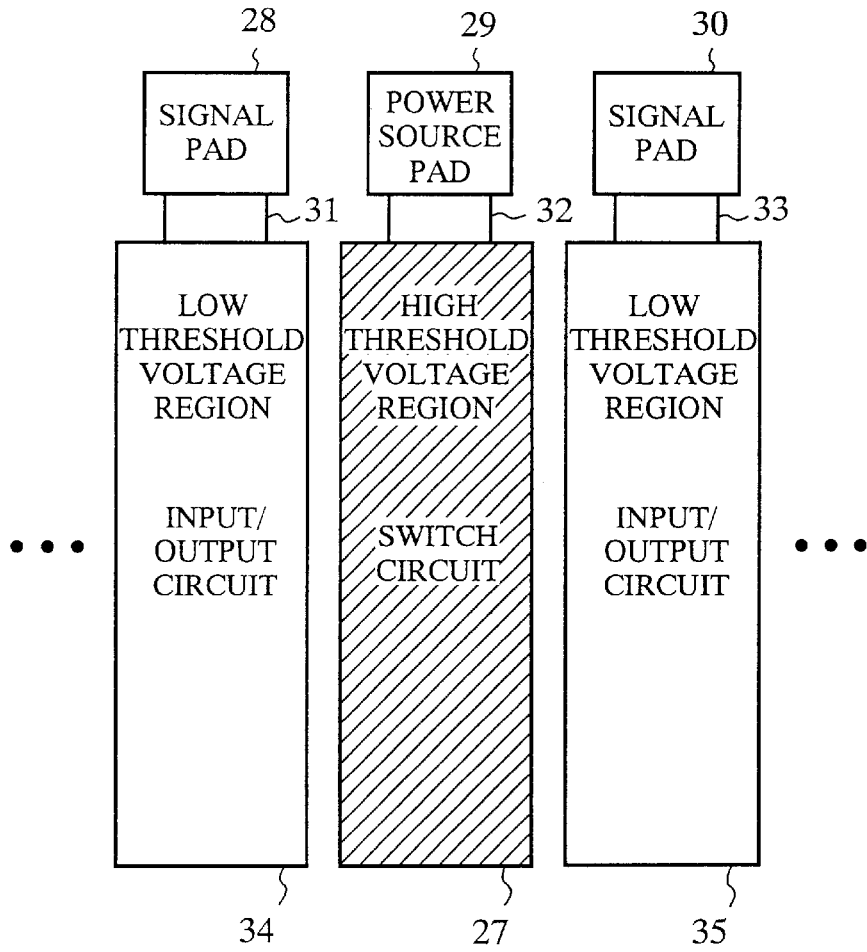
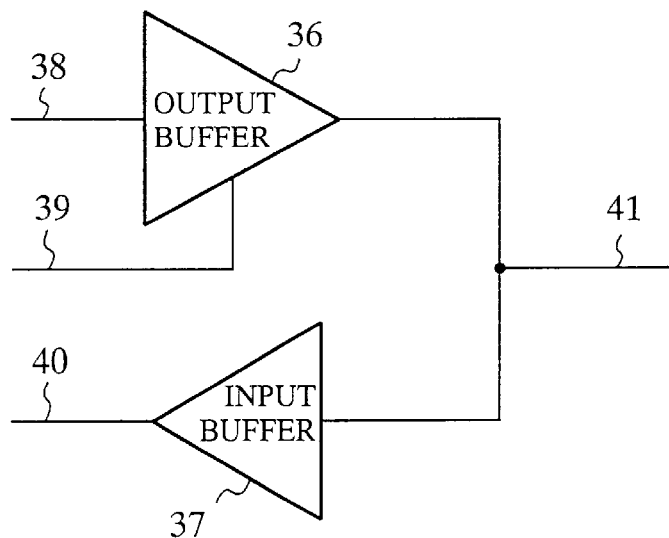


FIG.5



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