

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

AQUILA INNOVATIONS, INC.,
Patent Owner.

IPR2019-01525
Patent 6,239,614 B1

Before SALLY C. MEDLEY, DENISE M. POTHIER, and
AMBER L. HAGY, *Administrative Patent Judges*.

HAGY, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Advanced Micro Devices, Inc. (“Petitioner”)¹ filed a Petition (Paper 2, “Pet.”) to institute an *inter partes* review of claims 1–5 (the “challenged claims”) of U.S. Patent 6,239,614 B1 (Ex. 1001, the “’614 patent”). Aquila Innovations, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 9, “Prelim. Resp.”). With authorization from the Board, Petitioner filed a Reply (Paper 10, “Reply”), and Patent Owner filed a Sur-reply (Paper 11, “Sur-reply”).

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2012). A decision to institute under 35 U.S.C. § 314 may not institute on fewer than all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018).

After considering the evidence and arguments presented in the Petition, Preliminary Response, Reply, and Sur-reply, we determine Petitioner has demonstrated a reasonable likelihood that it would prevail in showing unpatentability of claims 1–5 of the ’614 patent, and we institute review on all challenged claims and on all grounds.

¹ Petitioner identifies itself and ATI Technologies ULC as the real parties-in-interest. Pet. 4.

A. Related Proceedings

Petitioner states the '614 patent has been asserted by Patent Owner against Nichia Corporation and Nichia America Corporation in *Aquila Innovations Inc. v. Advanced Micro Devices, Inc.*, Case No. 1:18-cv-00554-LY, filed July 2, 2018, pending in the Western District of Texas. Pet. 4; *see also* Paper 5, 2.

B. The '614 Patent

The '614 patent was filed on April 1, 1999, and claims priority to a Japanese application filed on January 14, 1999. Ex. 1001, codes (22), (30). The '614 patent relates to a layout for a semiconductor integrated circuit device including multi-threshold voltage metal oxide semiconductor (“MOS”) transistors (“MTCMOS”), which is capable of operating at a lower power supply voltage when active and with reduced leakage current during standby. *Id.* at code (57), 1:7–12. The '614 patent also relates to the use of MOS decoupling capacitors to reduce voltage variations and time delays in MTCMOS devices. *Id.* at code (57), 4:59–5:9.

By way of background, the '614 patent describes the desirability of operating integrated circuit devices with a low threshold voltage to reduce power consumption. *Id.* at 1:14–21. Lowering the threshold voltage, however, increases leakage current of the MOS transistor during standby. *Id.* at 1:21–26. The '614 patent describes a type of transistor—the MTCMOS transistor—that was known to address this problem. *Id.* at 1:26–32. The MTCMOS transistor is comprised of MOS transistors having a low threshold voltage, which allow reduced power consumption while maintaining operating speed, and standby power control MOS transistors

each having a high threshold voltage, which reduce leakage current during standby. *Id.* at 1:33–41.

The '614 patent states that the conventional layout for MTCMOS devices adopted “a standard cell system in which layout design is performed in units of a latch circuit such as a flip-flop circuit comprised of an inverter circuit, a master circuit and a slave circuit, and a logic circuit.” *Id.* at 1:50–55. The '614 patent further notes that “[t]he layout design based on such a standard cell system has a problem in that since it is performed in respective circuit units, the period required to manufacture the MTCMOS becomes long.” *Id.* at 1:55–58. The '614 patent purports to address this problem by “implement[ing] the layout of a semiconductor integrated circuit device by a gate array system, thereby shortening a manufacturing period thereof as compared with the conventional standard cell system.” *Id.* at 2:1–7.

Figure 1 of the '614 patent, reproduced below, illustrates the layout of MTCMOS transistors in a gate array:

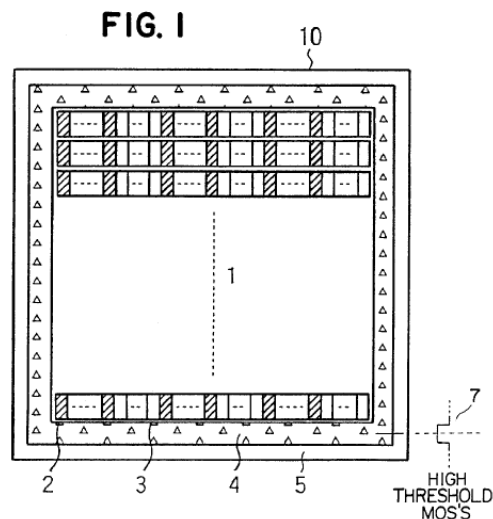


Figure 1 of the '614 patent, reproduced above, is a layout showing an embodiment of the claimed invention. *Id.* at 2:49–50. In particular, Figure 1

illustrates unit cell array 1, in which unit cells 2 with low-threshold MOSFETs are shown in columns alternating with columns of unit cells 3 with high-threshold MOSFETs. *Id.* at 3:7–16. Power switch 4 is placed around the unit cell array 1, and input/output circuits 5 are disposed there around. *Id.* at 3:16–19. Power switch 4 comprises a PMOS transistor and an NMOS transistor, each of which is a MOS transistor 7 that has a high threshold voltage for cutting off leakage current during standby. *Id.* at 3:19–22.

Figure 3 of the '614 patent, shown below, illustrates the unit cells in a MTCMOS integrated circuit device.

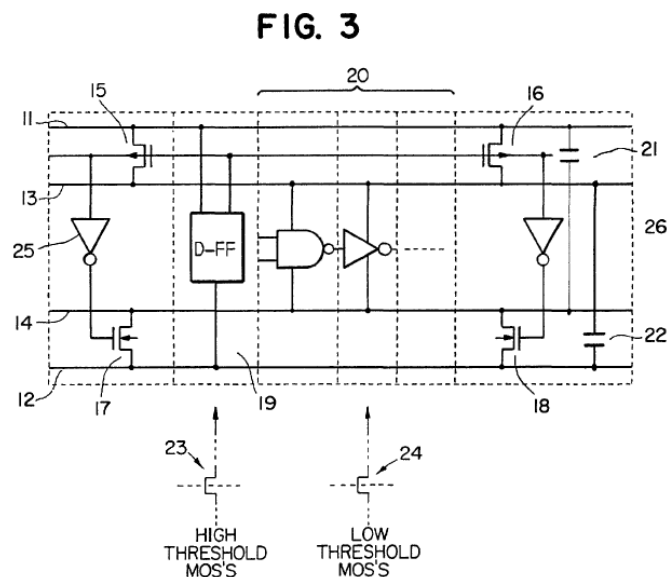


Figure 3 of the '614 patent, reproduced above, is a circuit diagram depicting one example of the unit cells shown in Figure 1 according to the claimed invention. *Id.* at 2:54–56. In particular, the MTCMOS device comprises (1) unit cells having low threshold voltage MOS transistors to form logic cells 20 connecting between two virtual power supply lines 13 and 14, (2) unit cells having high threshold voltage MOS transistors to form the DFF

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