

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

AQUILA INNOVATIONS, INC.,
Patent Owner.

IPR2019-01525
Patent 6,239,614 B1

Before SALLY C. MEDLEY, DENISE M. POTHIER, and
AMBER L. HAGY, *Administrative Patent Judges*.

HAGY, *Administrative Patent Judge*.

DECISION
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Advanced Micro Devices, Inc. (“Petitioner”)¹ filed a Petition (Paper 2, “Pet.”) to institute an *inter partes* review of claims 1–5 (the “challenged claims”) of U.S. Patent 6,239,614 B1 (Ex. 1001, the “’614 patent”). Aquila Innovations, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 9, “Prelim. Resp.”). With authorization from the Board, Petitioner filed a Reply (Paper 10, “Reply”), and Patent Owner filed a Sur-reply (Paper 11, “Sur-reply”). Pursuant to 35 U.S.C. § 314, we instituted an *inter partes* review of all challenged claims on all grounds presented in the Petition. Paper 12 (“Institution Decision” or “Dec.”). Patent Owner filed a Patent Owner Response (Paper 18, “PO Resp.”), Petitioner filed a Reply (Paper 21, “Pet. Reply”), and Patent Owner filed a Sur-reply (Paper 33, “PO Sur-reply”).

On December 11, 2020, we conducted an oral hearing. A copy of the transcript (Paper 38, “Tr.”) is included in the record.

We have jurisdiction under 35 U.S.C. § 6(b). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–5 of the ’614 patent are unpatentable. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a).

¹ Petitioner identifies itself and ATI Technologies ULC as the real parties-in-interest. Pet. 4.

II. BACKGROUND

A. Related Proceedings

Petitioner states the '614 patent has been asserted by Patent Owner in *Aquila Innovations Inc. v. Advanced Micro Devices, Inc.*, No. 1:18-cv-00554-LY, filed July 2, 2018, pending in the Western District of Texas. Pet. 4; *see also* Paper 5, 2.

B. The '614 Patent

The '614 patent was filed on April 1, 1999, and claims priority to a Japanese application filed on January 14, 1999. Ex. 1001, codes (22), (30). The '614 patent relates to a layout for a semiconductor integrated circuit device, including multi-threshold complementary metal oxide semiconductor (“MTCMOS”) transistors, which is capable of operating at a lower power supply voltage when active and with reduced leakage current during standby. *Id.* at code (57), 1:7–12. The '614 patent also relates to the use of MOS decoupling capacitors to reduce voltage variations and time delays in MTCMOS devices. *Id.* at code (57), 4:59–5:9.

The '614 patent describes the desirability of operating integrated circuit devices with a low threshold voltage to reduce power consumption. *Id.* at 1:14–21. Lowering the threshold voltage, however, increases leakage current of the MOS transistor during standby. *Id.* at 1:21–26. The '614 patent describes a type of transistor—the MTCMOS transistor—that was known to address this problem. *Id.* at 1:26–32. The MTCMOS transistor is comprised of MOS transistors having a low threshold voltage, which allow reduced power consumption while maintaining operating speed, and standby power control MOS transistors each having a high threshold voltage, which reduce leakage current during standby. *Id.* at 1:33–41.

The '614 patent states that the conventional layout for MTCMOS devices adopted “a standard cell system in which layout design is performed in units of a latch circuit such as a flip-flop circuit comprised of an inverter circuit, a master circuit and a slave circuit, and a logic circuit.” *Id.* at 1:50–55. The '614 patent further notes that “[t]he layout design based on such a standard cell system has a problem in that since it is performed in respective circuit units, the period required to manufacture the MTCMOS becomes long.” *Id.* at 1:55–58. The '614 patent purports to address this problem by “implement[ing] the layout of a semiconductor integrated circuit device by a gate array system, thereby shortening a manufacturing period thereof as compared with the conventional standard cell system.” *Id.* at 2:1–7.

Figure 1 of the '614 patent, reproduced below, illustrates the layout of MTCMOS transistors in a gate array:

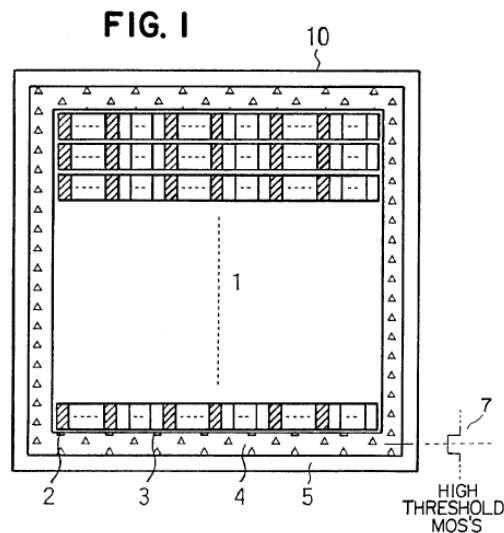


Figure 1 of the '614 patent, reproduced above, is a layout showing an embodiment of the claimed invention. *Id.* at 2:49–50. In particular, Figure 1 illustrates unit cell array 1, in which unit cells 2 with low-threshold MOSFETs are arranged in columns alternating with columns of unit cells 3

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