United States Patent [19]

Hasani et al.

[11] Patent Number: 5,805,808

[45] Date of Patent: Sep. 8, 1998

[54] **REAL TIME PARSER FOR DATA PACKETS IN A COMMUNICATIONS NETWORK**

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[73] Assignee: **Digital Equipment Corporation**, Maynard, Mass.

[21] Appl. No.: **838,678**

[22] Filed: **Apr. 9, 1997**

Related U.S. Application Data

[63] Continuation of Ser. No. 365,993, Dec. 29, 1994, abandoned, which is a continuation of Ser. No. 814,997, Dec. 27, 1991, abandoned.

[51] **Int. Cl.^{6}** **G06F 13/00**
[52] **U.S. Cl.** **395/200.2**; 370/392
[58] **Field of Search** 395/800, 200.15, 395/200.2, 840, 841, 851, 853, 182.13; 370/252, 351, 353, 389, 392, 401, 402; 380/3, 4, 9, 28, 37, 42, 49, 50
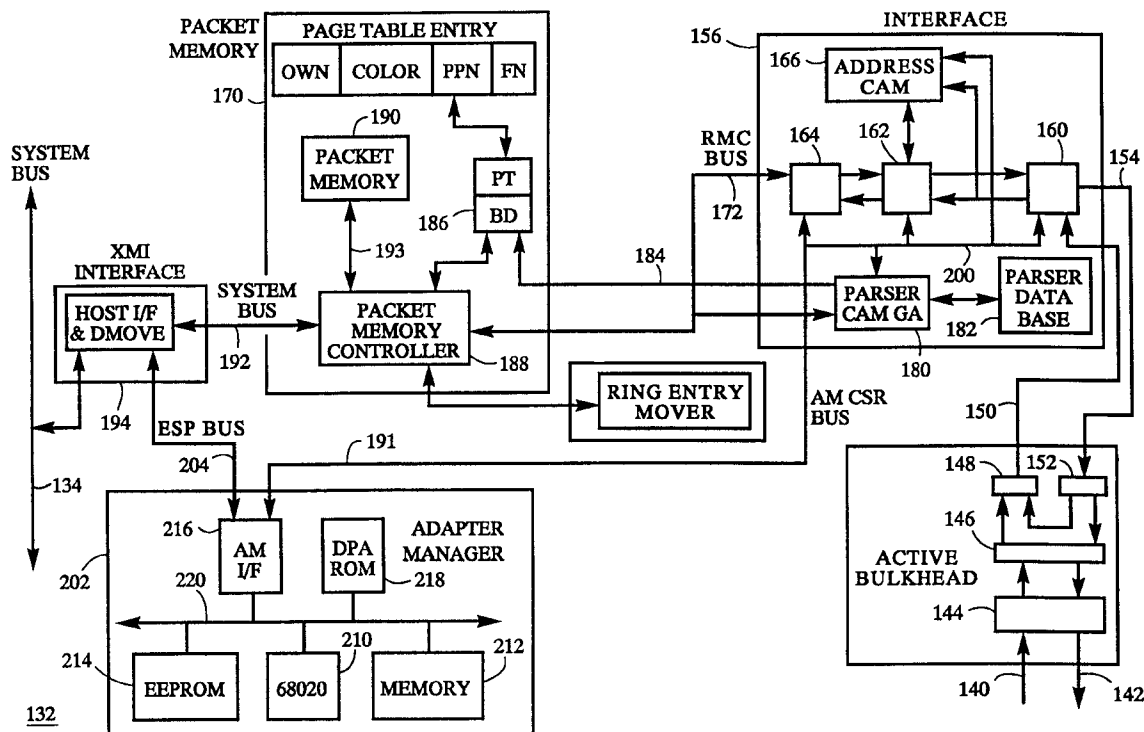
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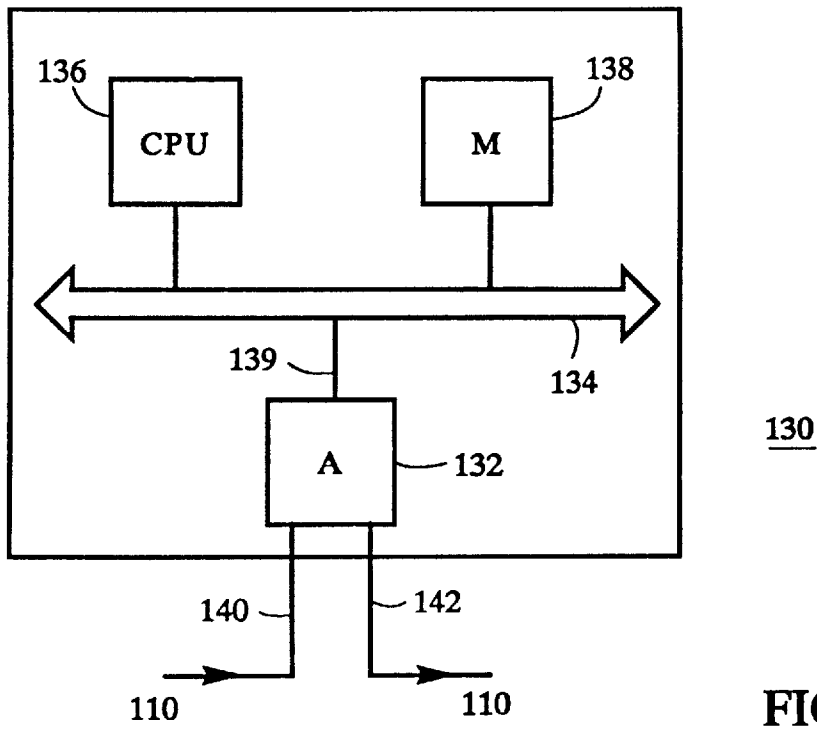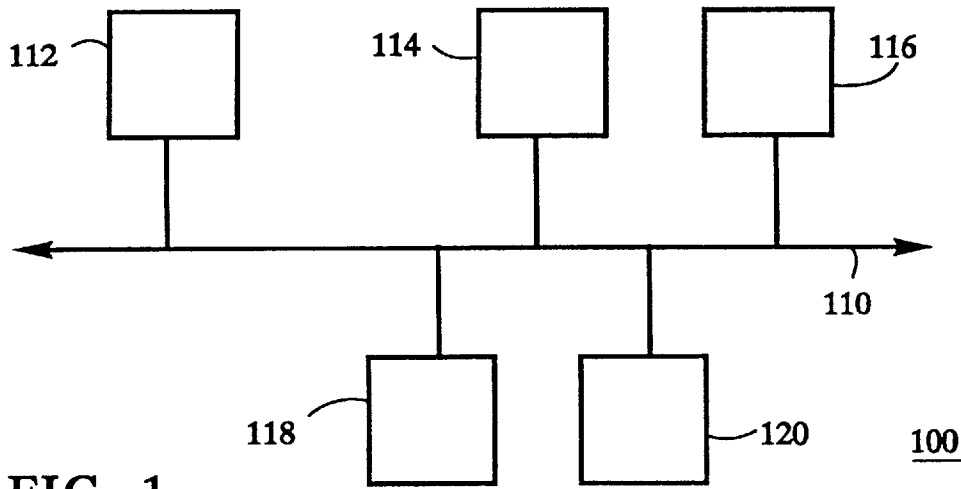|			
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[57] **ABSTRACT**

A parser for reading bits of a packet has a set of logic circuits implemented in a computer chip; a memory interacting with the computer chip, the memory providing first data to the set of logic circuits; means for reading bits from any field of packet into the set of logic circuits, the bits providing second data to the set of logic circuits; means, responsive to the first data and the second data, for the logic circuits to interpret bits of the packet.
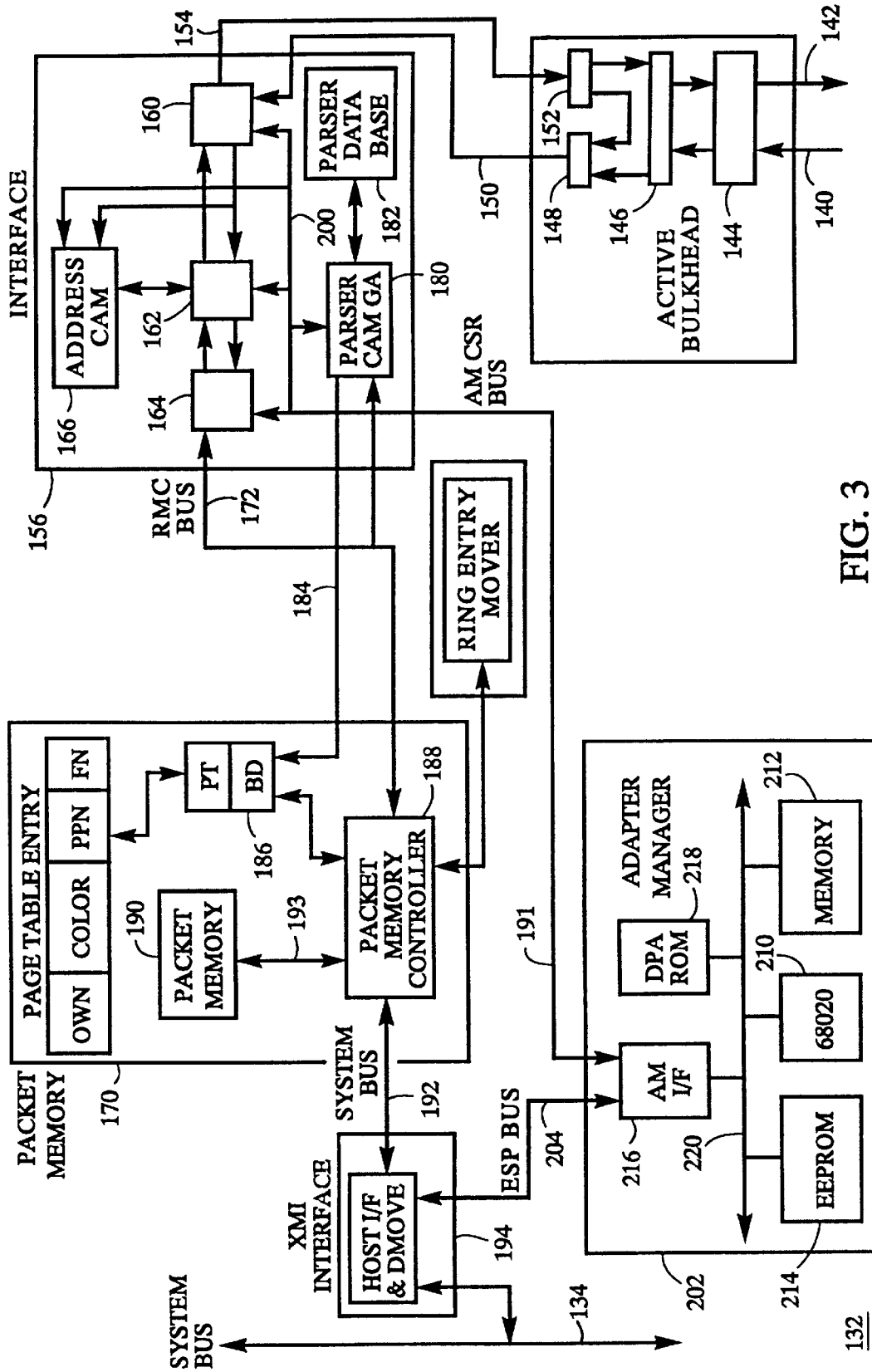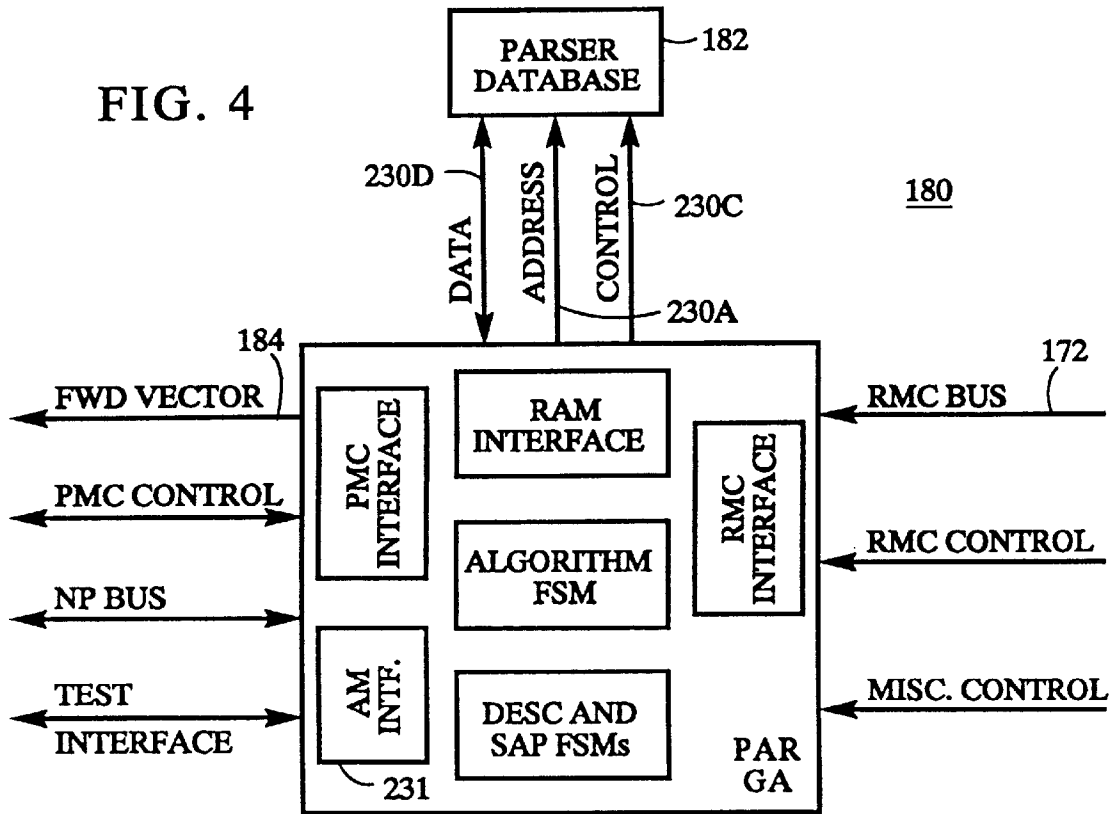
13 Claims, 21 Drawing Sheets

112

114

116

110

118   120   **100**

FIG. 1

136   138

CPU   M

139   134

130

A   132

140   142

110   110   **FIG. 2**

FIG. 3

FIG. 4

PARSER DATABASE — 182

230D — DATA ADDRESS CONTROL — 230C

230A

180

184

PMC INTERFACE

FWD VECTOR

PMC CONTROL

NP BUS

TEST INTERFACE

AM INTR. — 231

RAM INTERFACE

ALGORITHM FSM

DESC AND SAP FSMs

RMC INTERFACE

PAR GA

RMC BUS — 172

RMC CONTROL

MISC. CONTROL

15	14	13	12	11	10	9	8	7	6	5	4	0
PAR	COL	DIS	HOST	TYPE	UNK		MD		SOP	EOP	UINDEX	

FIG. 6

FDDI PACKET FORMAT

PRE (7)	SD (1)	FC (1)	DA (6)	SA (6)	INFO	FCS (4)	ED (.5)	FS (1.5)

MAC LAYER

SD	FC	DA	SA		FCS	ED	FS

LLC LAYER

DSAP (1)	SSAP (1)	CNTL (1-2)	PID (5)	DATA

* SNAP SAP　　* UID
* NON SNAP SAP　　* XID
　　* TEST

FIG. 5A

DOCKET ALARM
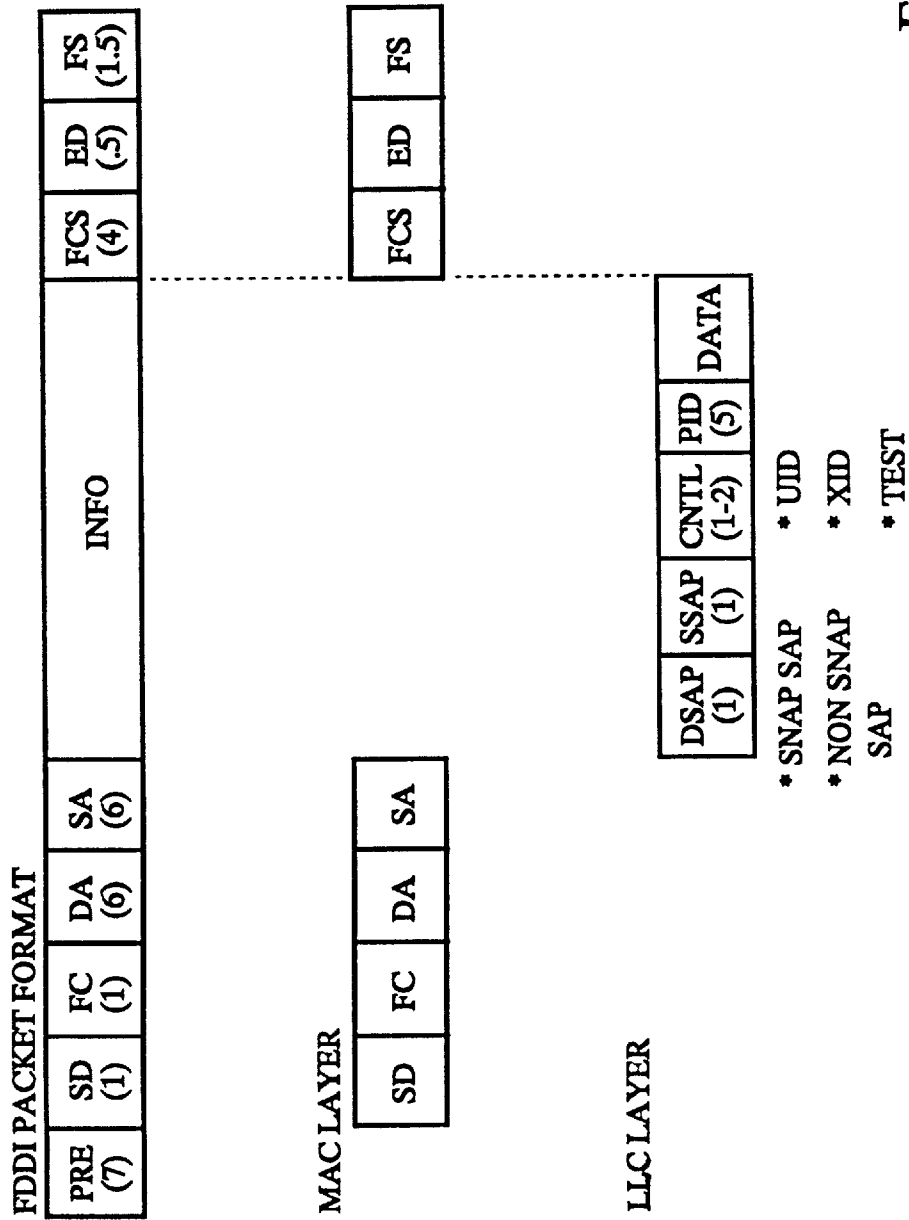
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