



[54] REAL TIME PARSER FOR DATA PACKETS IN A COMMUNICATIONS NETWORK

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Related U.S. Application Data

[63] Continuation of Ser. No. 365,993, Dec. 29, 1994, abandoned, which is a continuation of Ser. No. 814,997, Dec. 27, 1991, abandoned.

[51] Int. Cl.<sup>6</sup> G06F 13/00

[52] U.S. Cl. 395/200.2; 370/392

[58] Field of Search 395/800, 200.15, 395/200.2, 840, 841, 851, 853, 182.13; 370/252, 351, 353, 389, 392, 401, 402; 380/3, 4, 9, 28, 37, 42, 49, 50

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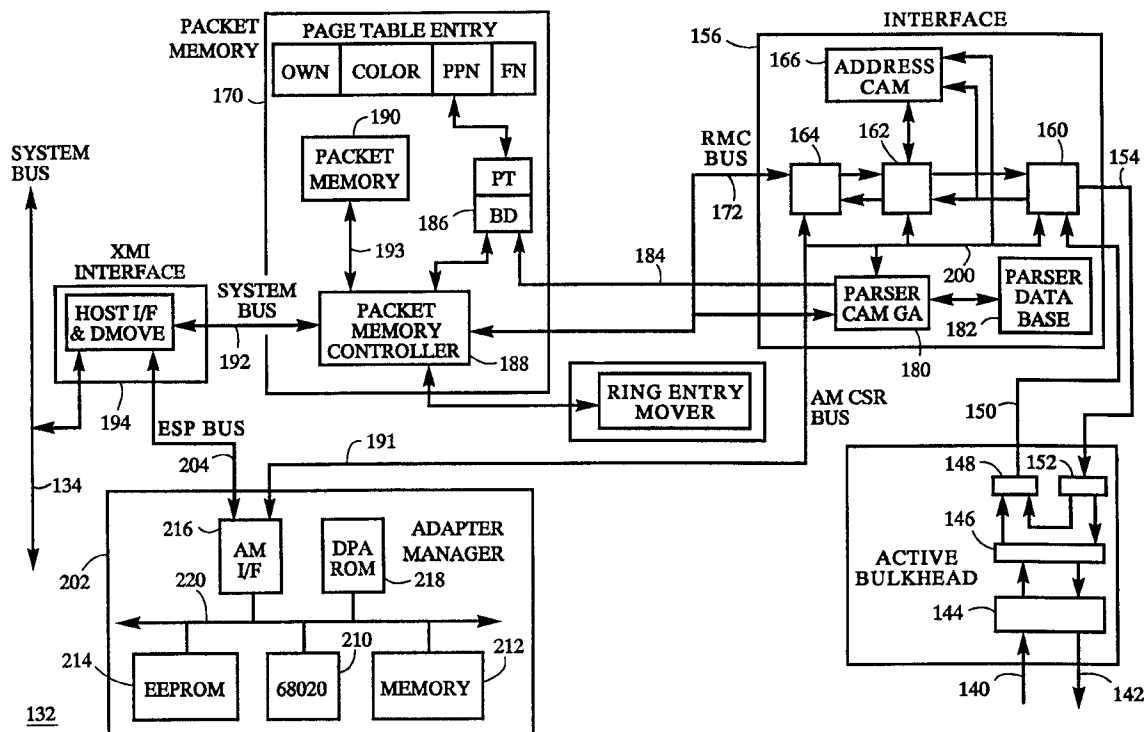
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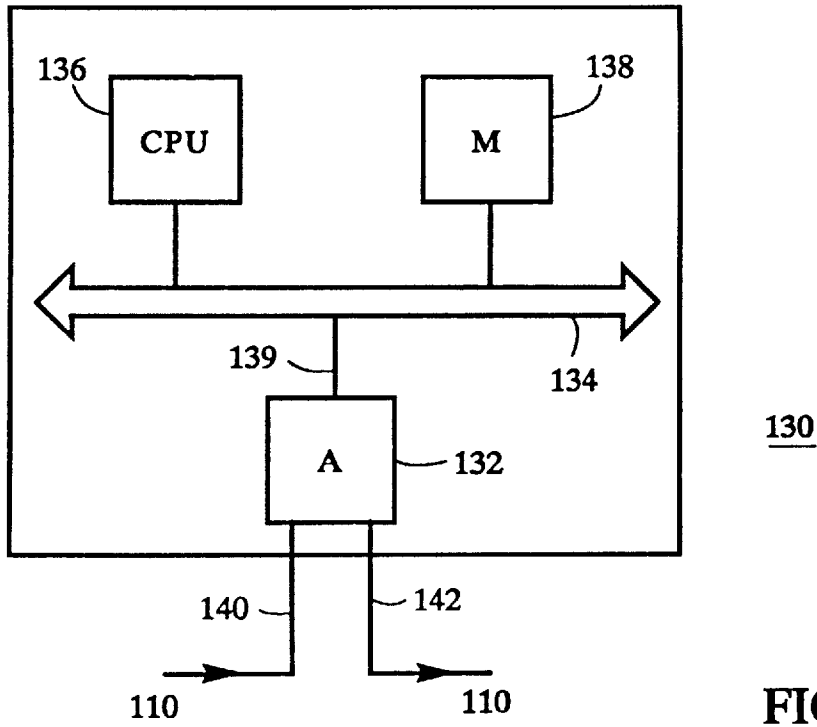
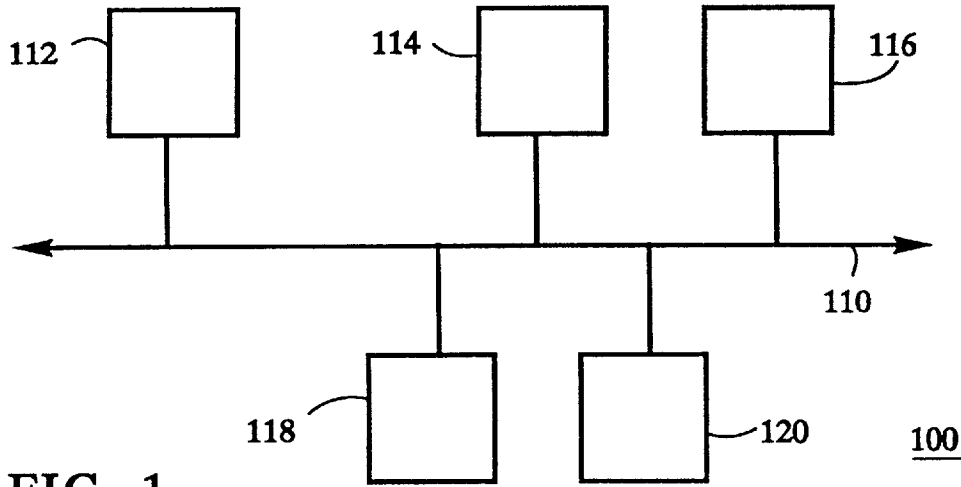
Primary Examiner—Alpesh M. Shah  
Attorney, Agent, or Firm—Christine M. Kuta; A. Sidney Johnston

[57] ABSTRACT

A parser for reading bits of a packet has a set of logic circuits implemented in a computer chip; a memory interacting with the computer chip, the memory providing first data to the set of logic circuits; means for reading bits from any field of packet into the set of logic circuits, the bits providing second data to the set of logic circuits; means, responsive to the first data and the second data, for the logic circuits to interpret bits of the packet.

13 Claims, 21 Drawing Sheets





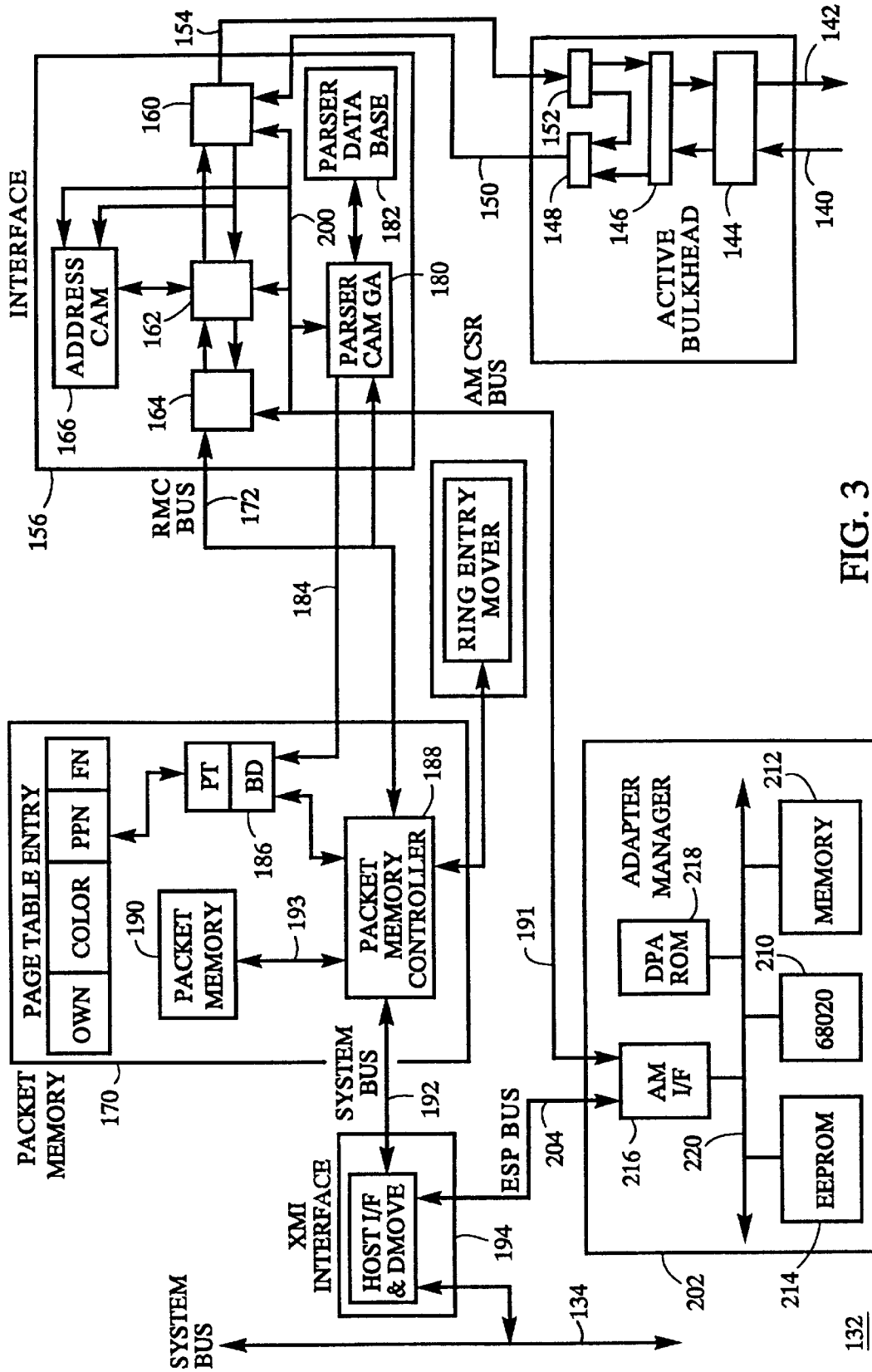
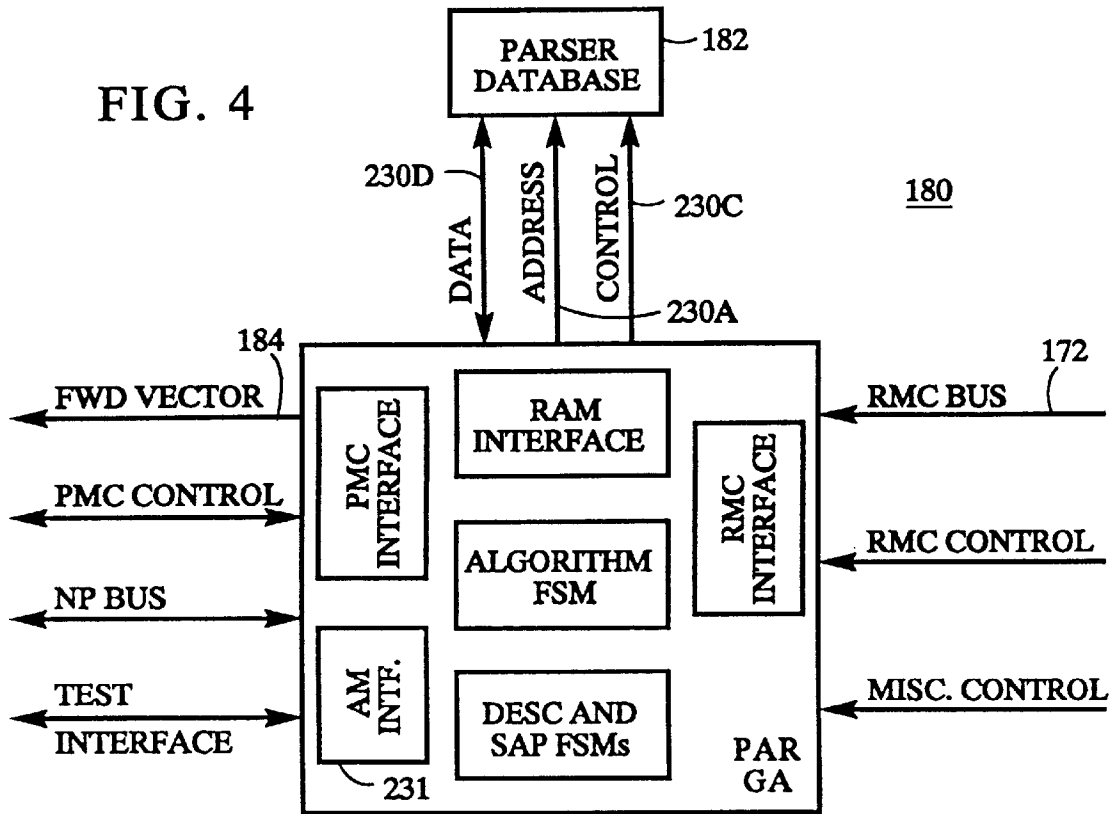


FIG. 3

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FIG. 4



15	14	13	12	11	10	9	8	7	6	5	4	0
PAR	COL	DIS	HOST	TYPE	UNK	MD	SOP	EOP	UINDEX			

FIG. 6

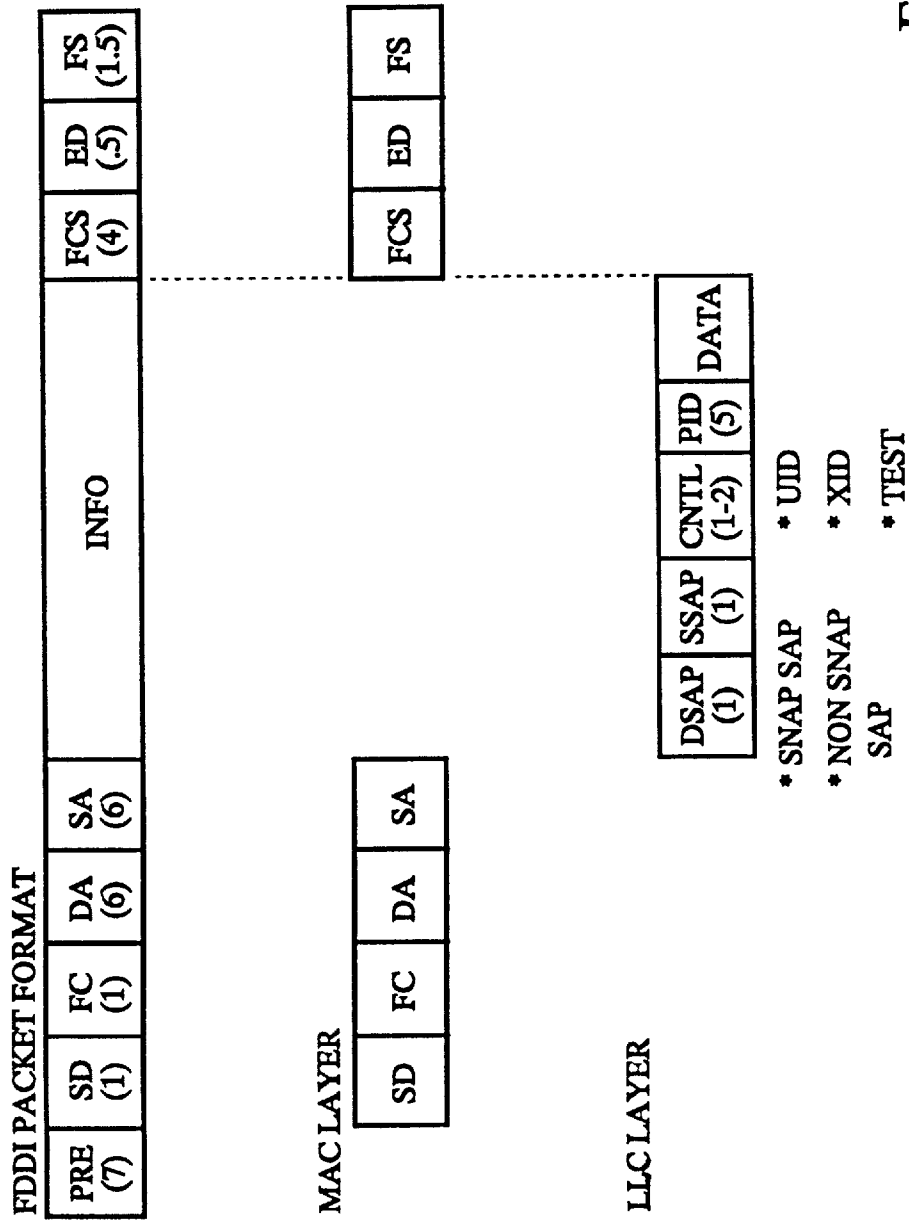


FIG. 5A

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