



- [54] **HIGH SPEED SIGNAL CONVERSION METHOD AND DEVICE**
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- [73] Assignee: **LSI Logic Corporation**, Milpitas, Calif.
- [*] Notice: This patent is subject to a terminal disclaimer.

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Primary Examiner—Dennis-Doon Chow

- [21] Appl. No.: **08/607,433**
- [22] Filed: **Feb. 27, 1996**

Related U.S. Application Data

- [63] Continuation of application No. 08/161,729, Dec. 3, 1993, Pat. No. 5,504,503.
- [51] **Int. Cl.⁷** **B09G 5/00**
- [52] **U.S. Cl.** **345/518; 345/516; 345/507**
- [58] **Field of Search** 365/230.04, 230.05, 365/230.08, 230.09, 189.05; 345/185, 189, 186, 190, 200, 507, 509, 515, 516, 517, 518; 395/507, 509, 515, 516, 517, 518

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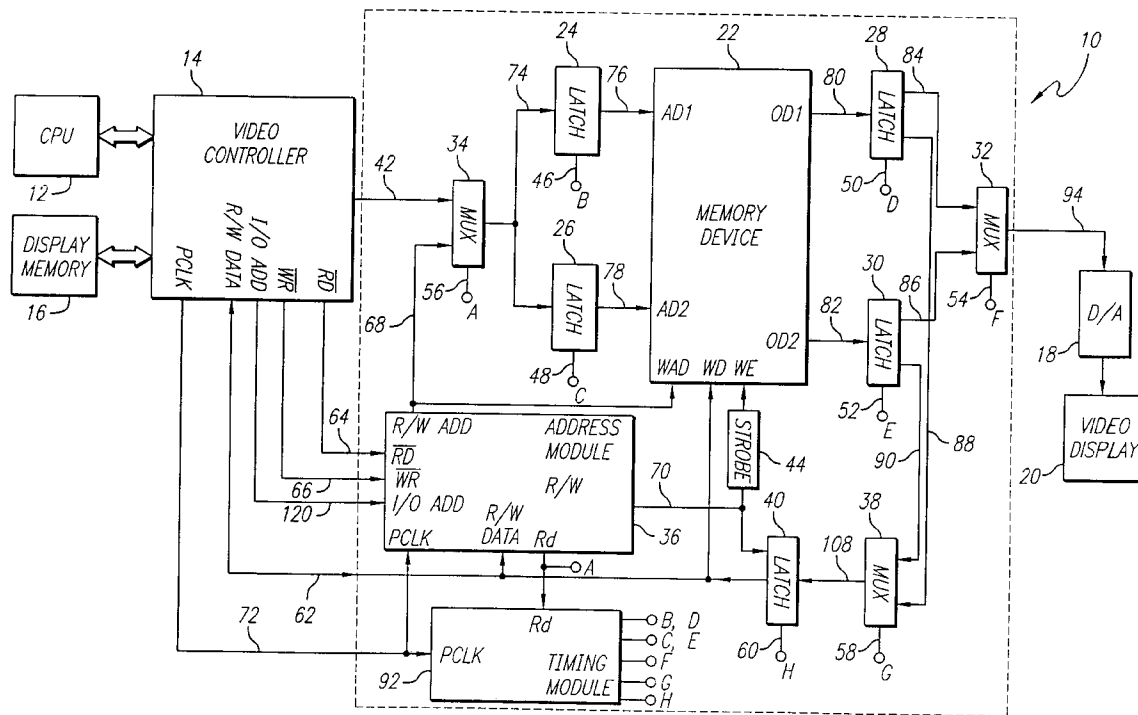
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[57] **ABSTRACT**

A random access memory has an access time which is longer than the period of read input signals, for example digital video data signals, such that it cannot respond directly to the input signals. The memory has two read address inputs and two outputs which are arranged as separate channels, each of which can access any location in the memory. The access time of the memory is shorter than two input signal periods. The input signals are applied alternately to the read address inputs, and output signals constituted by data stored at addresses corresponding to the input signals are produced at the memory outputs by an arrangement of clocked latches such that, although two input signal periods are used for accessing each memory location, the alternating accessing using two channels enables the memory to produce output signals having the same period (at the same frequency) as the input signals. Additional elements are provided to enable writing to the memory using the alternating channel arrangement, and also to enable memory locations to be unconditionally interrogated while responding to a stream of read input signals.

17 Claims, 4 Drawing Sheets



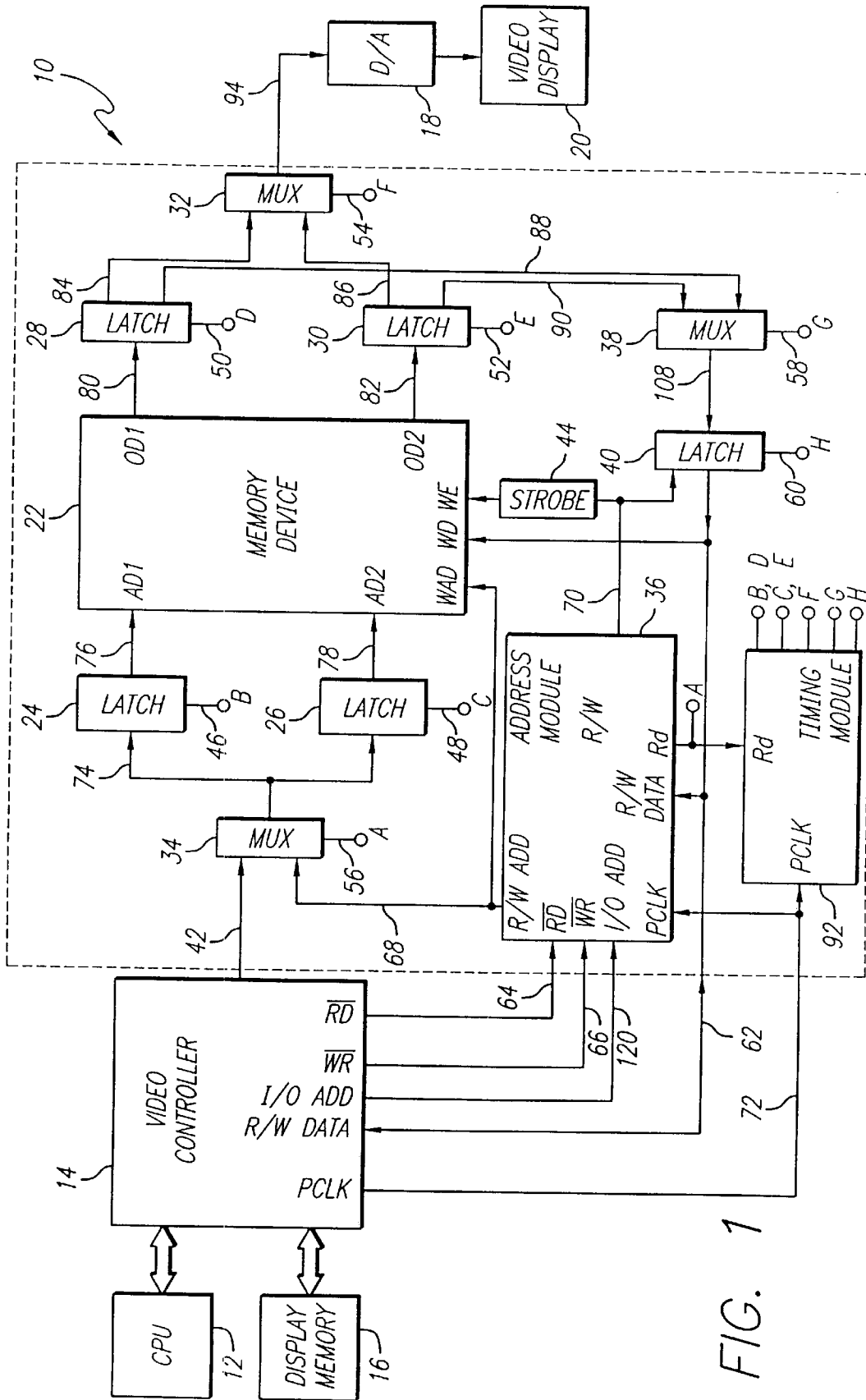


FIG. 1

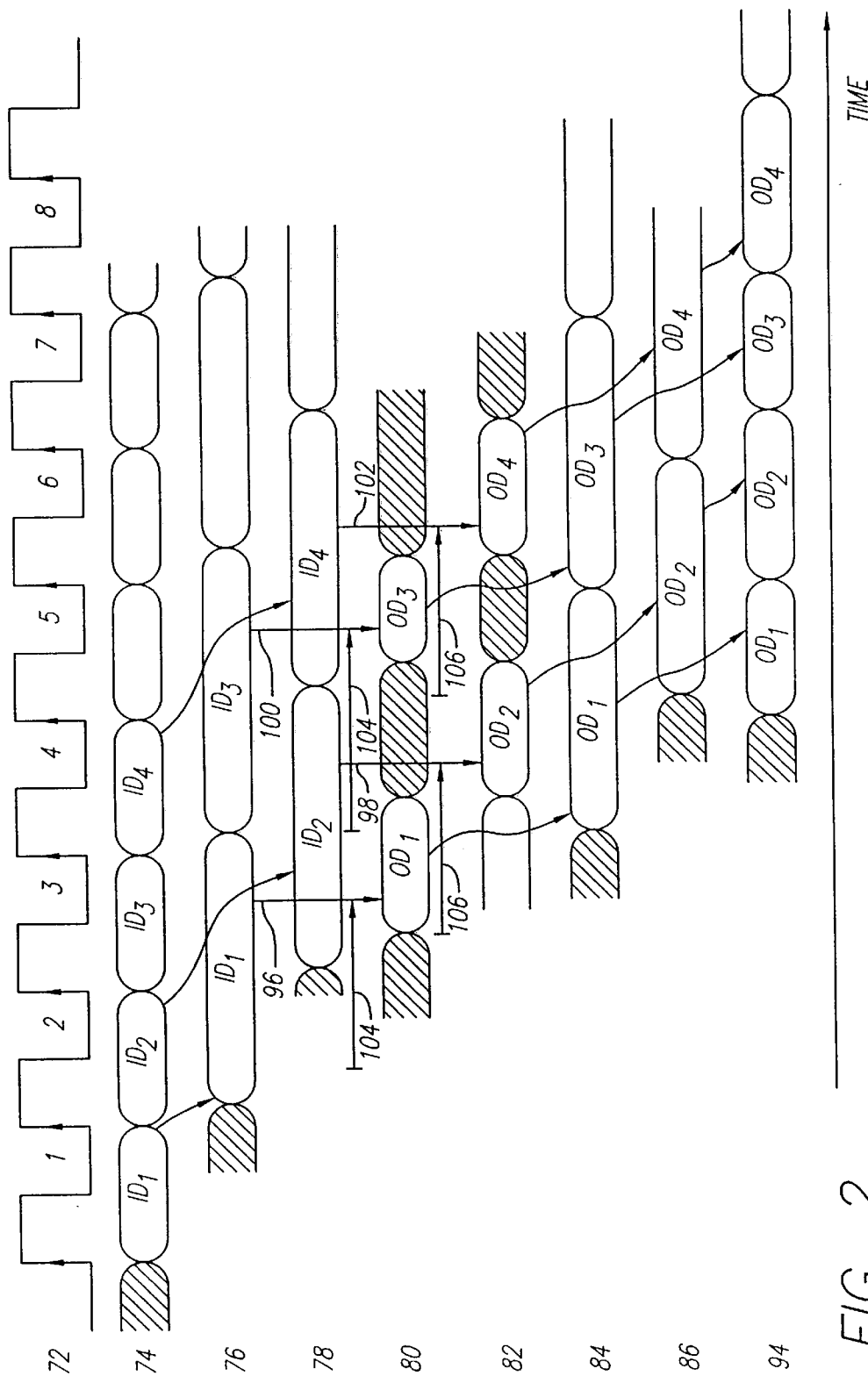


FIG. 2

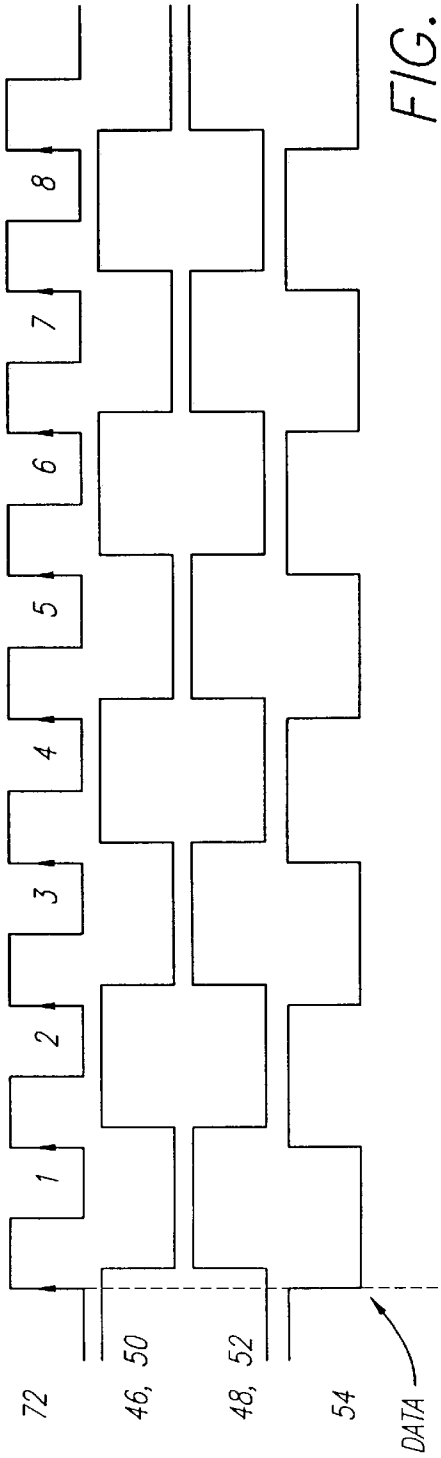


FIG. 3(a)

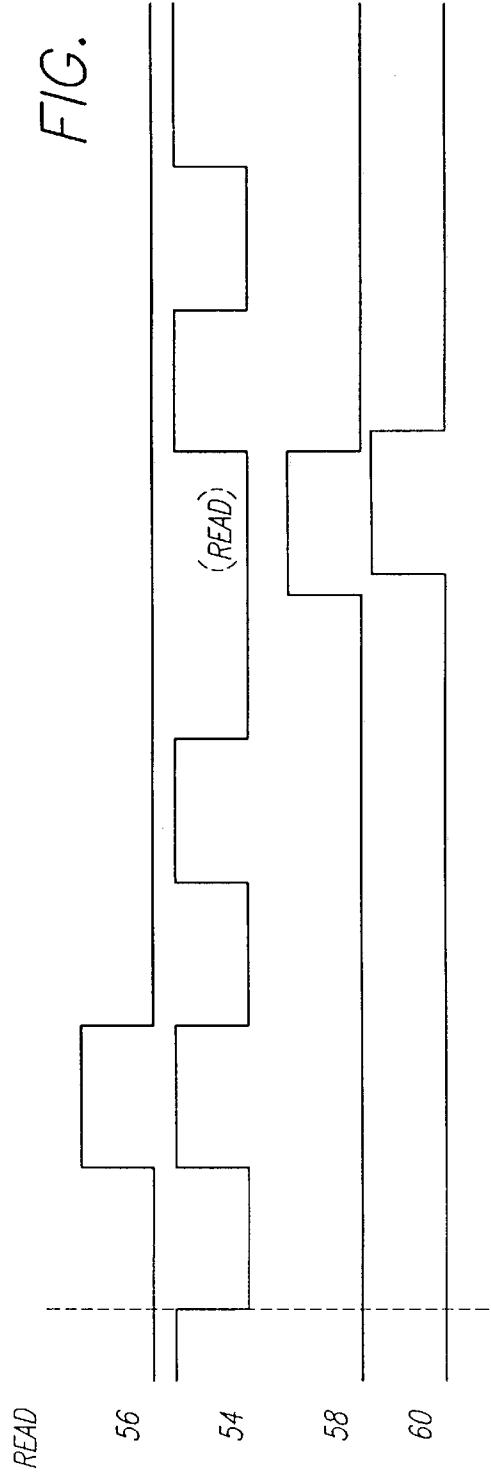


FIG. 3(b)

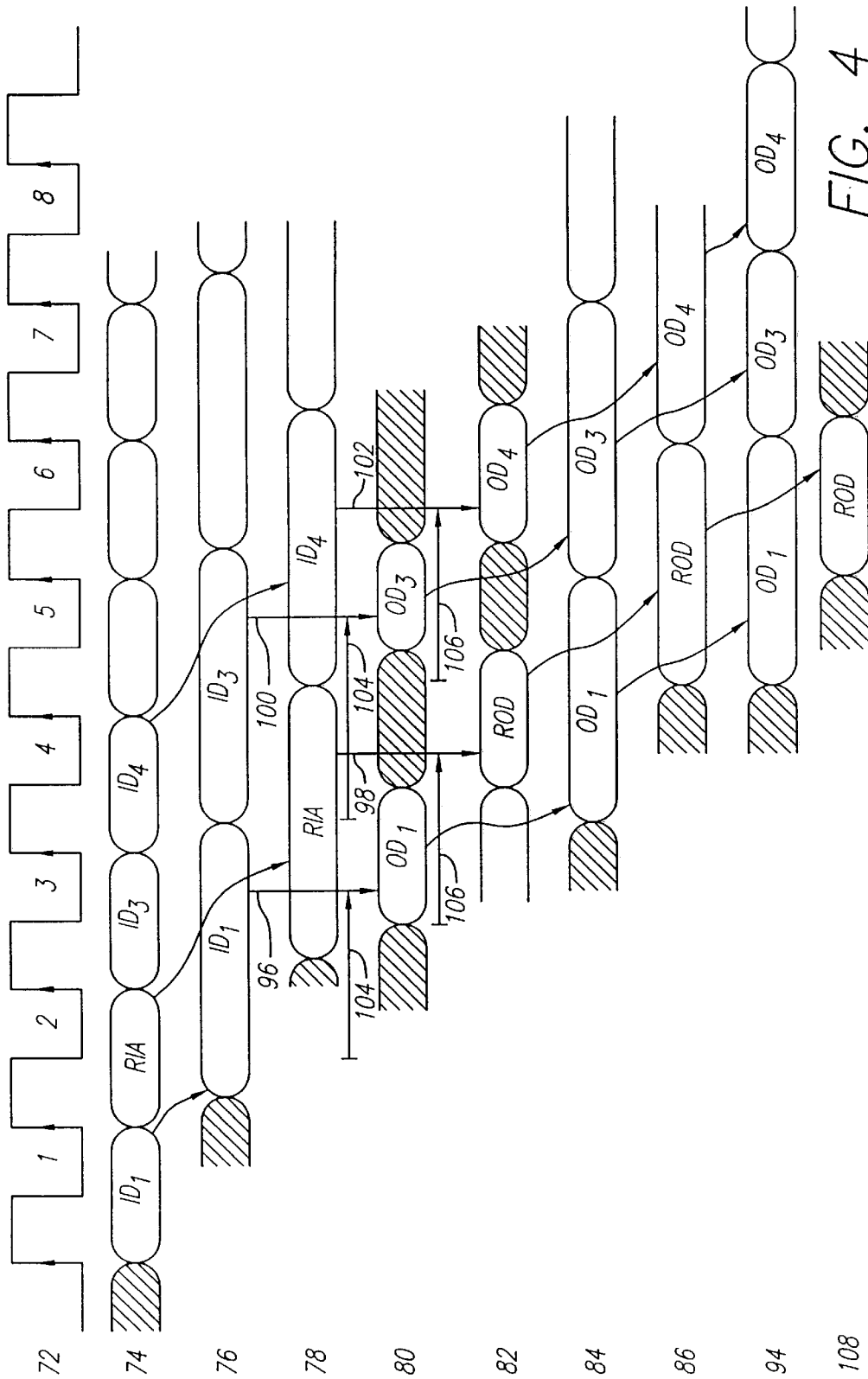


FIG. 4

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