AGILENT TECHNOLOGIES, INC.
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PATENT APPLICATION

ATTORNEY DOCKET NO. 70030259-1

IN THE U.S. PATENT AND TRADEMARK OFFICE
Patent Application Transmittal L tter

COMMISSIONER FOR PATENTS
PO Box 1450
Al xandria, VA 22313-1450

Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is a(n): (X) Utility ( ) Design
(X) original patent application,
( ) continuation-in-part application

INVENTOR(S): **Kong Weng Lee et al.**

TITLE: **PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME**

Enclosed are:

(X) The Declaration and Power of Attorney. (X) signed ( ) unsigned or partially signed

(X) 8 sheets of drawings (one set) ( ) Associate Power of Attorney

( ) Form PTO-1449 ( ) Information Disclosure Statement and Form PTO-1449

( ) Priority document(s) ( )(Other) _____ (fee $_____)

CLAIMS AS FILED BY OTHER THAN A SMALL ENTITY				
(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) TOTALS
TOTAL CLAIMS	20 — 20	0	X $18	$ 0
INDEPENDENT CLAIMS	2 — 3	0	X $84	$ 0
ANY MULTIPLE DEPENDENT CLAIMS	0		$280	$ 0
BASIC FEE: Design ($330.00); Utility ($750.00)				$ 750
TOTAL FILING FEE				$ 750
OTHER FEES				$
TOTAL CHARGES TO DEPOSIT ACCOUNT				$ 750

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By Linda A. Iimura

Typed Name: Linda A. Iimura

Respectfully submitted,

Kong Weng Lee et al.

By

Ian Hardcastle

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR PATENT

Packaging Device for Semiconductor Die, Semiconductor Device Incorporating Same and Method of Making Same

Inventors: Kong Weng Lee
Kee Yean Ng
Yew Cheong Kuan
Cheng Why Tan
Gin Ghee Tan

Related Application

[0001] This application is related to a simultaneously-filed United States patent application serial number 10/xxx,xxx entitled *Method for Fabricating a Packaging Device for Semiconductor Die and Semiconductor Device Incorporating Same* of inventors Kong Weng Lee, Kee Yean Ng, Yew Cheong Kuan, Cheng Why Tan and Gin Ghee Tan, attorney docket number 70030260-1.

Background of the Invention

[0002] Many types of conventional semiconductor device are composed of a semiconductor die mounted in a packaging device. One type of packaging device widely used in the industry includes a metal lead frame. A metallization layer of aluminum located on the bottom surface of the semiconductor die is bonded to a conductive surface that forms part of the lead frame to attach and electrically connect the die to the lead frame. Additionally, electrical connections are made between bonding pads on the top surface of the die and other leads of the lead frame to provide additional electrical connections to the die. The lead frame and semiconductor die are then encapsulated to complete the semiconductor device. The packaging device protects the semiconductor die and provides electrical and mechanical connections to the die that are compatible with conventional printed circuit board assembly

processes.

[0003] In such conventional semiconductor devices, the bottom surface of the die is typically bonded to the conductive surface of the lead frame using a silver epoxy adhesive that cures at a relatively low temperature, typically about 120 °C. The curing temperature of the silver epoxy adhesive is compatible with the other materials of the packaging device.

[0004] The volume of the packaging device used in such conventional semiconductor devices, i.e., the lead frame and the encapsulant, is typically many times that the semiconductor die. This makes such conventional semiconductor devices unsuitable for use in applications in which a high packing density is required. A high packing density allows miniaturization and other benefits. Therefore, what is needed is a semiconductor packaging device that is comparable in volume with the semiconductor die and that is compatible with conventional printed circuit board assembly processes.

[0005] Recently, semiconductor die having a substrate surface metallization layer of a gold-tin alloy (80 % Au:20 % Sn approximately) have been introduced in light-emitting devices. Such semiconductor die typically have a substrate of sapphire, silicon carbide or a Group III-V semiconductor material, such as gallium arsenide. Semiconductor devices having substrates of the first two substrate materials have layers of Group III-V semiconductor materials, such as gallium nitride, deposited on their substrates. The die attach process for such semiconductor die uses a gold-tin eutectic, which has a melting point of about 280 °C. Temperatures as high as about 350 °C can be encountered in the die attach process for such die. Such high temperatures are incompatible with the materials of many conventional packaging devices. Thus, what is also needed is a packaging device for semiconductor die that use a high-temperature die attach process.

[0006] Many printed circuit assembly processes and assembly equipment require the use of standard semiconductor device packages. Modifying such processes to use a new semiconductor device package can be expensive and can interrupt production. Therefore, what is additionally needed is a way to mount a semiconductor die that requires a high-temperature die attach process in a conventional packaging device.

Summary of the Invention

[0007] The invention provides a packaging device for a semiconductor die. The packaging device includes a substrate, a mounting pad, a connecting pad and an interconnecting element. The substrate is substantially planar and has opposed major surfaces. The mounting pad is conductive and is located on one of the major surfaces. The connecting pad is conductive and is located on the other of the major surfaces. The conductive interconnecting element extends through the substrate and electrically interconnects the mounting pad and the connecting pad.

[0008] The packaging device has a volume that is only a few times that of the semiconductor die and can be fabricated from materials that can withstand a high-temperature die attach process. The packaging device can be configured as the only packaging device of the semiconductor device. The packaging device can alternatively be configured as a submount for a semiconductor die that requires a high-temperature die attach process. The submount with attached semiconductor die can be handled as a conventional, albeit slightly larger, semiconductor die that is then mounted in a conventional packaging device, such as a lead frame based packaging device, using a conventional semiconductor device assembly process, including conventional temperatures.

[0009] The invention also provides a semiconductor device that includes a substrate, a mounting pad, a connecting pad, an interconnecting element and a semiconductor die. The substrate is substantially planar and has opposed major surfaces. The mounting pad is conductive and is located on one of the major surfaces. The connecting pad is conductive and is located on the other of the major surfaces. The conductive interconnecting element extends through the substrate and electrically interconnects the mounting pad and the connecting pad. The semiconductor die is affixed to the mounting pad.

[0010] The semiconductor device as just described can be mounted in a conventional packaging device as described above. Alternatively, the semiconductor device may additionally include a bonding pad, an additional connecting pad, an additional interconnecting element and a bonding wire. The bonding pad is conductive and is located on the one of the major surfaces. The additional connecting pad is conductive and is located on the other of the major surfaces. The additional interconnecting

element is conductive and extends through the substrate and electrically interconnects the bonding pad and the additional connecting pad. The bonding wire extends between the semiconductor die and the bonding pad. Such a semiconductor device constitutes a stand-alone semiconductor device that has a low profile and that can be used in high packing density applications. The semiconductor device may additionally include an encapsulant that encapsulates the semiconductor die and at least a portion of the major surface of the substrate on which the mounting pad is located.

Brief Description of the Drawings

[0011] Figures 1A, 1B, 1C, 1D, 1E and 1F are respectively an isometric view, a side view, a front view, a top view, a bottom view and a cross-sectional view of a first embodiment of a packaging device in accordance with the invention. The cross-sectional view of Figure 1F is along the section line 1F-1F in Figure 1D.

Figures 2A, 2B, 2C, 2D, 2E and 2F are respectively an isometric view, a side view, a front view, a top view, a bottom view and a cross-sectional view of a first embodiment of a semiconductor device in accordance with the invention. The cross-sectional view of Figure 2F is along the section line 2F-2F in Figure 2D.

Figures 3A, 3B, 3C, 3D, 3E and 3F are respectively an isometric view, a side view, a front view, a top view, a bottom view and a cross-sectional view of a second embodiment of a packaging device in accordance with the invention. The cross-sectional view of Figure 3F is along the section line 3F-3F in Figure 3D.

Figures 4A, 4B, 4C, 4D, 4E and 4F are respectively an isometric view, a side view, a front view, a top view, a bottom view and a cross-sectional view of a second embodiment of a semiconductor device in accordance with the invention. The cross-sectional view of Figure 4F is along the section line 4F-4F in Figure 4D.

Figures 5A-5C are side views illustrating a method in accordance with the invention for fabricating a packaging device for a semiconductor die.

Figure 5D is a side view illustrating an optional additional process that may be included in the method illustrated in Figures 5A-5C.

Figures 6A-6D are side views illustrating a method in accordance with the invention for fabricating a semiconductor device.

Detailed Description of the Invention

[0012] Figures 1A-1F are schematic diagrams illustrating a first exemplary embodiment 100 of a packaging device for a semiconductor die in accordance with the invention. Packaging device 100 is composed of a substrate 110, interconnecting elements 120 and 122, a mounting pad 130, a bonding pad 132 and connecting pads 140 and 142 (Figure 1E).

[0013] Substrate 110 is substantially planar, has opposed major surfaces 112 and 114 and defines through holes 116 and 118 that extend through the substrate between major surfaces 112 and 114. Interconnecting element 120 is electrically conductive and is located in through hole 116. Interconnecting element 122 is electrically conductive and is located in through hole 118. Mounting pad 130 and bonding pad 132 are electrically conductive, are separate from one another and are located on the portions of the major surface 112 of substrate 110 in which through holes 116 and 118 are respectively located. Connecting pads 140 and 142 are electrically conductive, are separate from one another and are located on the portions of the major surface 114 of substrate 110 in which through holes 116 and 118 are respectively located.

[0014] Mounting pad 130 and connecting pad 140 are electrically connected to opposite ends of interconnecting element 120. Thus, interconnecting element 120 extending through substrate 110 in through hole 116 electrically connects mounting pad 130 to connecting pad 140. Bonding pad 132 and connecting pad 142 are electrically connected to opposite ends of interconnecting element 122. Thus, interconnecting element 122 extending through substrate 110 in through hole 118 electrically connects bonding pad 132 to connecting pad 142.

[0015] The material of substrate 110 is a thermally-conductive ceramic such as alumina or beryllia. In an embodiment, the material of the substrate was Kyocera® Type A440 ceramic sold by Kyocera Corp., of Kyoto, Japan. Typical dimensions of the substrate are in the range from about 0.5 mm square to about 2 mm square. Rectangular configurations are also possible. Alternative substrate materials include semiconductors, such as silicon, and epoxy laminates, such as those used in printed-circuit boards. Other materials that have a high thermal conductivity and a low electrical conductivity can be used instead of those exemplified above. The coefficient of thermal expansion of the substrate material relative to that of the semiconductor die

to be mounted on packaging device 100 should also be considered in choosing the substrate material.

[0016] As will be described in more detail below, substrate 110 is part of a wafer (not shown) from which typically several hundred packaging devices 100 are fabricated by batch processing. After fabrication of the packaging devices, the wafer is singulated into individual packaging devices. Alternatively, the packaging devices may be left in wafer form after fabrication. In this case, singulation is not performed until after at least a die attach process has been performed to attach a semiconductor die to each mounting pad 130 on the wafer. In some embodiments, wafer-scale wire bonding, encapsulation and testing are also performed prior to singulation. Full electrical testing, including light output testing, may be performed on the wafer.

[0017] The material of interconnecting elements 120, 122 is metal or another electrically-conductive material. In an embodiment, the material of the interconnecting elements is tungsten, but any electrically-conductive material capable of forming a low-resistance electrical connection with the pads, i.e., mounting pad 130, bonding pad 132 and connecting pads 140, 142, and capable of withstanding the temperature of the die-attach process may be used. As noted above, packaging device 100 may be subject to a temperature as high as about 350 °C when a gold-tin eutectic is used to attach a semiconductor die to the mounting pad 130 of the packaging device. Interconnecting elements 120, 122 may be located relative to mounting pad 130 and bonding pad 132, respectively, elsewhere than the centers shown. Moreover, more than one interconnecting element may be located within either or both of the mounting pad and the bonding pad.

[0018] The material of pads 130, 132, 140, 142 is metal or another electrically-conductive material. Important considerations in selecting the material of the pads are adhesion to substrate 110, an ability to form a durable, low-resistance electrical connection with interconnecting elements 120 and 122 and an ability to withstand the temperature of the die attach process. In an embodiment, the structure of the pads is a seed layer of tungsten covered with layer of nickel about 1.2 μm to about 8.9 μm thick that is in turn covered with a layer of gold about 0.75 μm thick. Other metals, alloys, conductive materials and multi-layer structures of such materials can be used.

[0019] Packaging device 100 is used to package a semiconductor die. A

semiconductor device in which a semiconductor die is packaged using packaging device 100 described above will be described next.

[0020] Figures 2A-2F are schematic diagrams illustrating an exemplary embodiment 200 of a semiconductor device in accordance with the invention. Semiconductor device 200 incorporates packaging device 100 in accordance with the invention. Elements of semiconductor device 200 that correspond to elements of packaging device 100 described above with reference to Figures 1A-1F are indicated using the same reference numerals and will not be described again in detail.

[0021] Semiconductor device 200 is composed of packaging device 100 described above with reference to Figures 1A-1F, a semiconductor die 250, encapsulant 252 and a bonding wire 254. In the example shown, semiconductor die 250 embodies a light-emitting diode and has anode and cathode electrodes (not shown) covering at least parts of its opposed major surfaces. Semiconductor die 250 is mounted on packaging device 100 with the metallization on its bottom major surface attached to mounting pad 130. Encapsulant 252 covers the semiconductor die and the part of the major surface 112 of substrate 100 where mounting pad 130 and bonding pad 132 are located. Bonding wire 254 extends between a bonding pad located on the top major surface of semiconductor die 250 and bonding pad 132.

[0022] The bonding pad on the top major surface of semiconductor die 250 is typically part of or connected to the anode electrode of the light-emitting diode. The metallization on the bottom major surface of semiconductor die 250 typically constitutes the cathode electrode of the light-emitting diode. Thus, the anode electrode of semiconductor die 250 is electrically connected to connecting pad 142 by bonding wire 254, bonding pad 132 and interconnecting element 122, and the cathode electrode of semiconductor die 250 is electrically connected to connecting pad 140 by mounting pad 130 and interconnecting element 120.

[0023] Encapsulant 252 has a thickness greater than the maximum height of bonding wire 254 above major surface 112. In the example shown, the encapsulant is transparent to enable semiconductor device 200 to emit the light generated by semiconductor die 250.

[0024] Semiconductor die 250 is composed of one or more layers (not shown) of any semiconductor material composed of elements from Groups II, III, IV, V and VI of

the periodic table in binary, ternary, quaternary or other form. Semiconductor die 250 may additionally include a non-semiconductor substrate material, such as sapphire, metal electrode materials and dielectric insulating materials, as is known in the art.

[0025] In an embodiment of the above-described example in which semiconductor die 250 embodies a light-emitting diode, semiconductor die 250 is composed of a substrate of silicon carbide that supports one or more layers of (indium) gallium nitride. Such a light-emitting diode generates light in a wavelength range extending from ultra-violet to green. The bottom major surface (not shown) of the substrate remote from the layers of (indium) gallium nitride is coated with a metallization layer of a gold-tin alloy. A gold-tin eutectic attaches the semiconductor die to mounting pad 130, as described above, to provide a mechanical and electrical connection between the semiconductor die and the mounting pad.

[0026] The material of bonding wire 254 is gold. A process known in the art as low-loop wire bonding is used to connect the bonding wire between the anode electrode of semiconductor die 250 and bonding pad 132. Using low-loop wire bonding minimizes the maximum height of the bonding wire above substrate 110, and, therefore, reduces the overall height of semiconductor device 200. Other processes for providing an electrical connection between a bonding pad on a semiconductor die and a bonding pad on a packaging device are known in the art and may be used instead, especially in applications in which device height is a less important consideration.

[0027] The material of encapsulant 252 is clear epoxy. Alternative encapsulant materials include silicone. Embodiments of semiconductor device 200 that neither emit nor detect light can use an opaque encapsulant.

[0028] In the example of semiconductor device 200 described above, semiconductor die 250 is embodied as a light-emitting diode. Semiconductor die 250 may alternatively embody another type of diode without modification to packaging device 100. Versions of packaging device 100 may be used to package semiconductor die other than those that embody such electrical components as diodes that have only two electrodes. Versions of packaging device 100 may be used to package semiconductor die that embody such electronic circuit elements as transistors and integrated circuits that have more than two electrodes. Such versions of packaging device 100 have a number of bonding pads, interconnecting elements and connecting pads

corresponding to the number of bonding pads located on the top major surface of the semiconductor die. For example, a version of packaging device 100 for packaging a semiconductor die that embodies a transistor having collector, base and emitter electrodes, and in which the substrate metallization provides the collector electrode, has two bonding pads, two interconnecting elements and two connecting pads. Wire bonds connect the emitter bonding pad on the semiconductor die to one of the bonding pads on the packaging device and the base bonding pad on the semiconductor die to the other of the bonding pads on the packaging device.

[0029] The connecting pads, e.g., connecting pads 140 and 142, of embodiments of packaging device 100 having multiple connecting pads may be arranged to conform with an industry standard pad layout to facilitate printed circuit layout. In such embodiments, the interconnecting elements may be offset from the centers of the respective mounting pads, bonding pads and connecting pads to allow the connecting pad layout to conform with such a standard pad layout. In some embodiments, one or more of the mounting pad, bonding pads and connecting pads may have a shape that differs from the regular shapes illustrated. Some irregular shapes include two main regions electrically connected by a narrow track. For example, an irregularly-shaped bonding pad includes a region to which the bonding wire is attached, a region connected to the interconnecting element and a narrow track interconnecting the two regions.

[0030] Some versions of packaging device may accommodate two or more semiconductor die. In such versions, mounting pad 130 is sized large enough to accommodate the two or more semiconductor die. Additionally, such versions include sufficient bonding pads, interconnecting elements and connecting pads to make the required number of electrical connections to the semiconductor die. Alternatively, the packaging device may include two or more mounting pads. The mounting pads may be electrically connected to one another and thence to a common interconnecting element and connecting pad. Alternatively, each mounting pad may be electrically connected to a corresponding connecting pad by a respective interconnecting element.

[0031] Semiconductor device 200 is used by mounting it on a printed circuit board or other substrate using conventional surface-mount techniques or other techniques known in the art. Semiconductor device 200 is placed on a surface of the printed

circuit board with connecting pads 140 and 142 aligned with respective pads on the printed circuit board. The printed circuit board is then passed across a solder wave to form a solder joint between connecting pads 140 and 142 and the respective pads on the printed circuit board. Alternatively, semiconductor device 200 may be affixed to a printed circuit board by a process known as infra-red reflow soldering in which a pattern of solder is applied to the printed circuit board using a stencil, semiconductor device 200 and, optionally, other components are loaded onto the printed circuit board and the printed circuit board assembly is irradiated with infra-red light to heat and reflow the solder. Other processes for attaching electronic components to printed circuit boards are known in the art and may alternatively be used. Packaging device 100 and semiconductor device 200 may additionally include adhesive regions on the major surface 114 of substrate 110 external to connecting pads 140 and 142 to hold the semiconductor device in place on the printed circuit board during soldering.

[0032] In semiconductor device 200, packaging device 100 and encapsulant 252 collectively have a volume that is only about 15 times the volume of semiconductor die 250. Thus, packaging device 100 is well suited for use in high packing density applications. Moreover, packaging device 100 is fabricated from materials capable of withstanding the high temperatures involved in a die attach process that uses a gold-tin eutectic. Accordingly, packaging device 100 is well suited for packaging semiconductor die, such as the die of certain light-emitting devices, that require a die attach process that uses a gold-tin eutectic.

[0033] As noted above, many printed circuit board assembly processes are designed to use standard device packages, but many standard device packages are incapable of withstanding the high temperatures involved in a die attach process that uses a gold-tin eutectic. Figures 3A-3F are schematic drawings showing a second embodiment 300 of a packaging device in accordance with the invention. Packaging device 300 takes the form of a submount that enables semiconductor die that are mounted using a gold-tin eutectic or other high-temperature die attach process to be mounted in conventional semiconductor device packages that are incapable of withstanding such high temperatures. Moreover, packaging device 300 with a semiconductor die mounted thereon can be mounted in a conventional semiconductor device package as if it were a conventional semiconductor die. This allows conventional die attach, wire

bond and encapsulation processes to be used to assemble the final semiconductor device that incorporates the submount.

[0034] Figures 3A-3F are schematic diagrams illustrating a second exemplary embodiment 300 of a packaging device for a semiconductor die in accordance with the invention. Packaging device 300 takes the form of a submount for a semiconductor die. Packaging device 300 is composed of a substrate 310, an interconnecting element 320, a mounting pad 330 and a connecting pad 340 (Figure 3E).

[0035] Substrate 310 is substantially planar, has opposed major surfaces 312 and 314 and defines a through hole 316 that extends through the substrate between major surfaces 312 and 314. Interconnecting element 320 is electrically conductive and is located in through hole 316. Mounting pad 330 is electrically conductive and is located on a portion of the major surface 312 of substrate 310 in which through hole 316 is located. Alternatively, mounting pad 330 may cover major surface 312. Connecting pad 340 is electrically conductive and is located on a portion of the major surface 314 of the substrate in which through hole 316 is located. Alternatively, connecting pad 340 may cover major surface 314.

[0036] Mounting pad 330 and connecting pad 340 are electrically connected to opposite ends of interconnecting element 320. Thus, interconnecting element 320 extending through the substrate in through hole 316 electrically connects mounting pad 330 to connecting pad 340.

[0037] Materials and other details of substrate 310, interconnecting element 320, mounting pad 330 and connecting pad 340 are the same as those of substrate 110, interconnecting element 120, mounting pad 130 and connecting pad 140, respectively, of packaging device 100 described above with reference to Figures 1A-1F and will therefore not be described again here.

[0038] A semiconductor device in which a semiconductor die is packaged using packaging device 300 described above will be described next.

[0039] Figures 4A-4F are schematic diagrams illustrating an exemplary embodiment 400 of a semiconductor device in accordance with the invention. Semiconductor device 400 incorporates packaging device 300 in accordance with the invention. Elements of semiconductor device 400 that correspond to elements of semiconductor

device 200 described above with reference to Figures 2A-2F and of packaging device 300 described above with reference to Figures 3A-3F are indicated using the same reference numerals and will not be described again in detail.

[0040] Semiconductor device 400 is composed of a semiconductor die 250 mounted on packaging device 300 described above with reference to Figures 3A-3F. In the example shown, semiconductor die 250 embodies a light-emitting diode and has anode and cathode electrodes (not shown) covering at least parts of its opposed major surfaces. Specifically, semiconductor die 250 is mounted on packaging device 300 with the metallization on its bottom major surface attached to mounting pad 330. The metallization on the bottom major surface of semiconductor die 250 typically constitutes the cathode electrode of the light-emitting diode. Thus, the cathode electrode of semiconductor die 250 is electrically connected to connecting pad 340 by mounting pad 330 and interconnecting element 320. The top major surface of semiconductor die 250 typically includes a bonding pad that is typically part of or connected to the anode electrode of the light-emitting diode. This bonding pad remains exposed for later connection to the conventional semiconductor packaging device in which semiconductor device 400 will later be mounted.

[0041] Semiconductor device 400 is used by mounting it on a conventional semiconductor packaging device (not shown), such as the lead frame of a plastic package. Specifically, semiconductor device 400 is mounted on the lead frame with connecting pad 340 attached to a conductive mounting surface of the lead frame. Connecting pad 340 is attached to the mounting surface of the lead frame using a low-temperature die attach process, such as one that uses silver epoxy. Thus, semiconductor device 400 is compatible with conventional semiconductor device assembly processes. One or more bonding wires (not shown) are connected between bonding pads on the exposed major surface of semiconductor die 250 and the bonding pads of the lead frame. The lead frame with semiconductor device 400 mounted thereon is then encapsulated to complete the fabrication of the semiconductor device. Semiconductor device 400 may be mounted on or in conventional semiconductor packaging devices other that the lead frame based packaging device just exemplified.

[0042] Semiconductor device 400 is also suitable for attaching directly to a printed circuit board. A conventional die attach process can be used to attach connecting pad

340 directly to a suitably-sized pad on the printed circuit board. Such a die attach process does not subject the printed circuit board to the high temperatures that were used to attach semiconductor die 250 to the mounting pad 330 of packaging device 300.

[0043] A fabrication method in accordance with the invention will now be described. The fabrication method can be used to fabricate the packaging devices described above with reference to Figures 1A-1F and 3A-3F. In the method, a substrate is provided. The substrate is substantially planar, has opposed major surfaces, and includes a through hole extending between the major surfaces. The through hole is filled with a conductive interconnecting element. A conductive mounting pad and a conductive connecting pad are formed on different ones of the major surfaces in electrical contact with the conductive interconnecting element.

[0044] The fabrication method will now be described in further detail with reference to Figures 5A-5C, which show a highly simplified example of the method in which two packaging devices similar to packaging device 100 described above with reference to Figures 1A-1F are fabricated in a wafer. As noted above, hundreds of packaging devices are typically fabricated simultaneously in a single wafer of substrate material.

[0045] Figure 5A shows a wafer 510 of substrate material. A portion of the wafer constitutes the substrate of each of the packaging devices that will be fabricated in the wafer. Wafer 510 has opposed major surfaces 512 and 514. Portions of major surfaces 512 and 514 constitute the major surfaces of each of the packaging devices that will be fabricated in the wafer. The material of wafer 510 is one of the substrate materials described above.

[0046] Defined in wafer 510 is at least one through hole for each of the packaging devices that will be fabricated in the wafer. A packaging device similar to packaging device 300 described above with reference to Figures 3A-3F has one through hole per packaging device. In the example shown in Figure 5A, each packaging device is similar to packaging device 100 described above with reference to Figures 1A-1F and has two through holes per packaging device. Through holes 516 and 518 of one of the packaging devices and through holes 517 and 519 of the other of the packaging devices are shown.

[0047] In an embodiment, through holes 516-519 are formed by punching. The through holes may alternatively be formed by drilling or laser ablation. Many other ways suitable for forming holes having a diameter in a range from about 100 μm to about 2mm are known in the art and may be used instead.

[0048] Figure 5B shows interconnecting elements 520-523 being introduced into through holes 516-519, respectively, to fill the through holes. Interconnecting elements 520-523 are slugs of conductive material having a diameter smaller than the diameter of the through holes and a length larger than the thickness of wafer 510. In an embodiment, the material of the interconnecting elements is tungsten. A squeezing process is used to fill the through holes with the interconnecting elements. The squeezing process introduces the interconnecting elements into the through holes and then reduces the length and increases the diameter of the interconnecting elements. The squeezing process leaves the ends of the interconnecting elements approximately flush with respective major surfaces 512 and 514, and the interconnecting elements retained in the through holes by friction. An adhesive may additionally or alternatively be used to retain the interconnecting elements in the through holes.

[0049] The through hole may be filled with the interconnecting element in other ways. For example, through-hole plating may be used. In other alternatives, screen printing or metal deposition are used. A through hole will be regarded as having been filled with an interconnecting element even when the interconnecting element occupies only part of the volume of the through hole.

[0050] Figure 5C shows mounting pad 530 and connecting pad 540 formed on major surfaces 512 and 514, respectively, of wafer 510 in electrical contact with the opposite ends of interconnecting element 520. Figure 5C additionally shows mounting pad 531 and connecting pad 541 formed on major surfaces 512 and 514, respectively, in electrical contact with interconnecting element 521, bonding pad 532 and connecting pad 542 formed on major surfaces 512 and 514, respectively, in electrical contact with interconnecting element 522, and bonding pad 533 and connecting pad 543 formed on major surfaces 512 and 514, respectively, in electrical contact with interconnecting element 523.

[0051] Conductive pads 530-533 and 540-543 are formed on wafer 510 by electro less plating using a screen printed mask. A photo mask may alternatively be used.

Examples of other selective processes that may be used to form pads 530-533 and 540-543 are electroplating, screen printing and metal deposition. In another embodiment, major surfaces 512 and 514 are each initially covered with a layer of metal using a cladding process. The layer of metal may take the form a metal foil pressed into contact with the respective major surface to cause the foil to adhere to the wafer. An adhesive may be used to increase adhesion. Portions of the layer of metal are then selectively removed to define pads 530-533 and 540-543. A mask and etch process may be used to perform the selective removal.

[0052] Packaging devices in accordance with the invention are typically supplied to users in the wafer state shown in Figure 5C so that they can be used in wafer-scale assembly processes. However, the packaging devices can alternatively be supplied singly. Figure 5D shows an optional additional element of the above-described fabrication method in which wafer 510 is singulated into individual packaging devices 100 and 101. Singulation may be performed by sawing, scribing and breaking or by another singulation process.

[0053] In a practical embodiment of the above-described method, through holes 516-519 are formed in wafer 510 (Figure 5A), the through holes are filled with interconnecting elements 520-523 (Figure 5B) and regions of tungsten, each of which constitutes a seed layer for one of the conductive pads 530-533 and 540-543, are screen printed on the wafer with the wafer in its "green", i.e., unfired state. The wafer is then fired. After the wafer has been fired, an electroless plating process is performed to deposit one or more additional layers of metal to complete the formation of conductive pads 530-533 and 540-543 (Figure 5C).

[0054] A method in accordance with the invention for fabricating a semiconductor device using the wafer-scale device packages shown in Figure 5C will now be described. The method can be used to fabricate the semiconductor devices described above with reference to Figures 2A-2F. Portions of the method can be used to fabricate the semiconductor devices illustrated in Figures 4A-4F. In the method, a semiconductor die is mounted on the mounting pad of the packaging device, a bonding wire is connected between the semiconductor die and the bonding pad of the packaging device, and the semiconductor die and at least a portion of the major surface of the packaging device on which the mounting pad is located are

encapsulated.

[0055] The fabrication method will now be described in further detail with reference Figures 6A-6D, which show a highly simplified example in which two semiconductor devices similar to semiconductor device 200 described above with reference to Figures 2A-2F are fabricated. As noted above, hundreds of semiconductor devices are typically fabricated simultaneously on a single wafer.

[0056] Figure 6A shows a wafer-scale array 600 of packaging devices supplied in wafer-scale form on wafer 510. Semiconductor device 250 is mounted on mounting pad 530 and a semiconductor device 251 is mounted on mounting pad 531. In an embodiment, a semiconductor die having a gold-tin metallization on its bottom major surface is placed on each mounting pad 530, 531 on wafer 510. The wafer is then heated to a temperature in the range from about 280 °C to about 350 °C for a time in the range from about one second to about 60 seconds. The gold-tin eutectic that forms attaches the semiconductor die to the respective mounting pad when the wafer is allowed to cool.

[0057] Other die attach processes, including die attach processes that require substantially lower peak temperatures, are known in the art and may be used instead of the die attach process just described. Not all die attach processes are suitable for use with all die metallizations, however.

[0058] Figure 6B shows a bonding wire 254 connected between a bonding pad (not shown) on the exposed major surface of semiconductor die 250 and bonding pad 532 and a bonding wire 255 connected between a bonding pad (not shown) on the exposed major surface of semiconductor die 251 and bonding pad 533.

[0059] In an embodiment, low loop wire bonding is used to connect bonding wires 254, 255 between semiconductor die 250, 251 and bonding pads 532, 533. Other ways to electrically connect a bonding pad located on the exposed surface of a semiconductor die to a bonding pad similar to bonding pads 532, 533 are known the art and can alternatively be used.

[0060] Figure 6C shows semiconductor die 250 and a portion of major surface 512 on which mounting pad 530 is located encapsulated by encapsulation 252, and semiconductor die 251 and a portion of major surface 512 on which mounting pad 531 is located encapsulated by encapsulation 253.

[0061] In an embodiment, the encapsulant is clear epoxy. Silicone is another suitable encapsulant. Other encapsulants are known in the art and may be used where appropriate. In an embodiment, the encapsulant was applied by transfer molding. Other application processes are known in the art and may be used where appropriate. Examples of other suitable application processes include injection molding, casting and dam and fill.

[0062] Figure 6D shows wafer 510 after it has been singulated into individual semiconductor devices 200 and 201. Singulation may be performed by sawing, scribing and breaking or by another suitable singulation process. The semiconductor devices fabricated on wafer 510 may be electrically tested before the wafer is singulated. The ability to test the semiconductor devices at the wafer scale level substantially reduces the cost of testing.

[0063] The processes illustrated in Figures 6B and 6C are omitted when the method illustrated in Figures 6A-6D is used to fabricate a submount semiconductor device similar to that described above with reference to Figures 4A-4F.

[0064] This disclosure describes the invention in detail using illustrative embodiments. However, it is to be understood that the invention defined by the appended claims is not limited to the precise embodiments described.

Claims

We claim:

1. A packaging device for semiconductor die, the packaging device comprising:

a substantially planar substrate having opposed major surfaces;

a conductive mounting pad located on one of the major surfaces;

a conductive connecting pad located on the other of the major surfaces; and

a conductive interconnecting element extending through the substrate and electrically interconnecting the mounting pad and the connecting pad.

2. The packaging device of claim 1, in which the substrate comprises ceramic.

3. The packaging device of claim 1, in which the substrate comprises a material selected from epoxy laminate and silicon.

4. The packaging device of claim 1, in which the mounting pad and the connecting pad each comprise at least one of copper, silver, gold, nickel and tungsten.

5. The packaging device of claim 1, in which the conductive interconnecting element comprises tungsten.

6. The packaging device of claim 1, additionally comprising:

a bonding pad located on the one of the major surfaces,

an additional conductive connecting pad located on the other of the major surfaces, and

an additional conductive interconnecting element extending through the substrate and electrically interconnecting the bonding pad and the additional connecting pad.

7. The packaging device of claim 6, in which the substrate comprises ceramic.

8. The packaging device of claim 6, in which the substrate comprises a material selected from epoxy laminate and silicon.

9. The packaging device of claim 6, in which the mounting pad, the bonding pad and the connecting pads each comprise at least one of copper, silver, gold, nickel and tungsten.

10. The packaging device of claim 6, in which the interconnecting element comprises tungsten.

11. A semiconductor device, comprising:

a substantially planar substrate having opposed major surfaces;

a conductive mounting pad located on one of the major surfaces;

a conductive connecting pad located on the other of the major surfaces;

a conductive interconnecting element extending through the substrate and electrically interconnecting the mounting pad and the connecting pad; and

a semiconductor die attached to the mounting pad.

12. The semiconductor device of claim 11, in which the substrate comprises ceramic.

13. The semiconductor device of claim 11, in which the substrate comprises a material selected from epoxy laminate and silicon.

14. The semiconductor device of claim 11, in which the mounting pad and the connecting pad each comprise at least one of copper, silver, gold, nickel and tungsten.

15. The semiconductor device of claim 11, in which the conductive interconnecting element comprises tungsten.

16. The semiconductor device of claim 11, additionally comprising:

a conductive bonding pad located on the one of the major surfaces;

an additional conductive connecting pad located on the other of the major surfaces;

an additional conductive interconnecting element extending through the substrate and electrically interconnecting the bonding pad and the additional connecting pad, and

a bonding wire extending between the semiconductor die and the bonding pad.

17. The semiconductor device of claim 16, additionally comprising an encapsulant encapsulating the semiconductor die and at least a portion of the major surface of the substrate on which the mounting pad is located.

18. The semiconductor device of claim 16, in which the substrate comprises a material selected from ceramic, epoxy laminate and silicon.

19. The semiconductor device of claim 16, in which the mounting pad, the bonding pad and the connecting pads each comprise at least one of copper, silver, gold, nickel and tungsten.

20. The semiconductor device of claim 16, in which the conductive interconnecting element comprises tungsten

Abstract

[0065] The packaging device includes a substrate, a mounting pad, a connecting pad and an interconnecting element. The substrate is substantially planar and has opposed major surfaces. The mounting pad is conductive and is located on one of the major surfaces. The connecting pad is conductive and is located on the other of the major surfaces. The conductive interconnecting element extends through the substrate and electrically interconnects the mounting pad and the connecting pad. The packaging device has a volume that is only a few times that of the semiconductor die and can be fabricated from materials that can withstand high-temperature die attach processes. The packaging device can be configured as the only packaging device used in the semiconductor device or as a submount for a semiconductor die that requires a high-temperature die attach process.

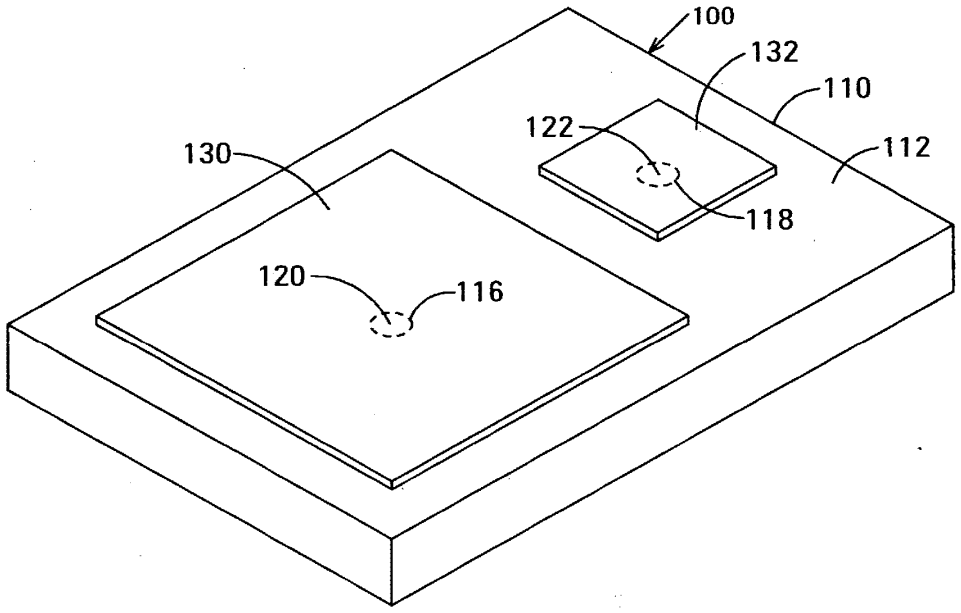

FIG.1A

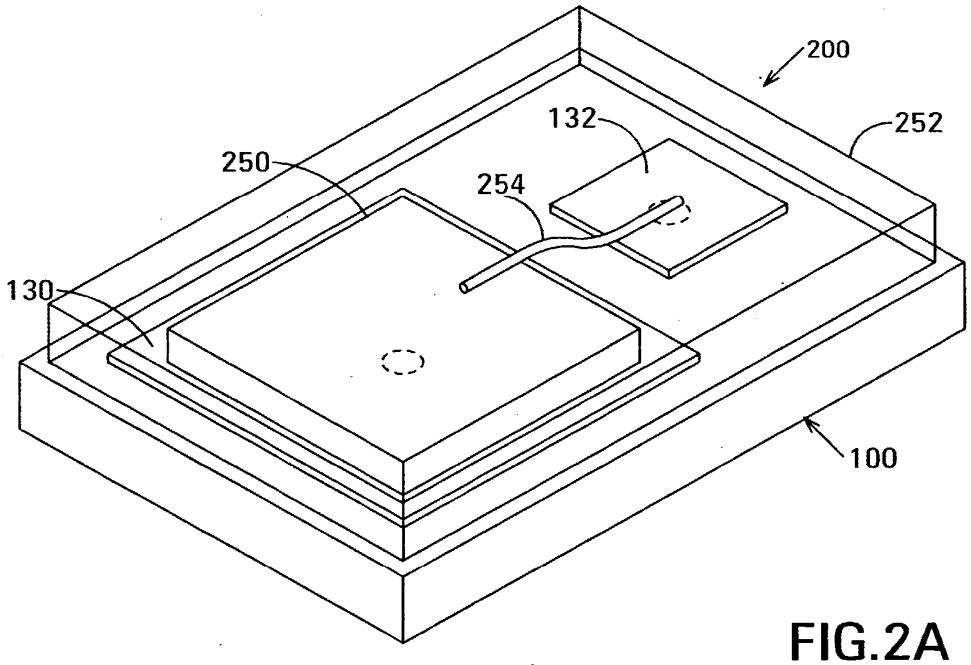

FIG.2A

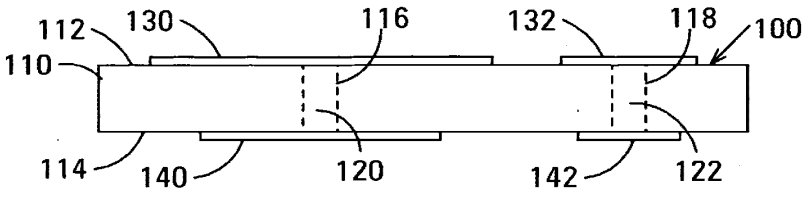

FIG.1B

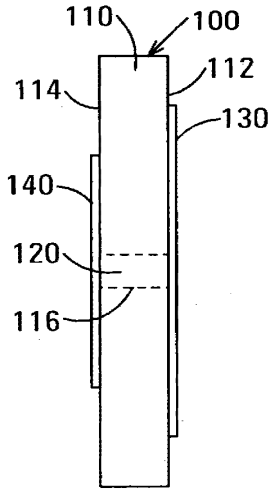

FIG.1C

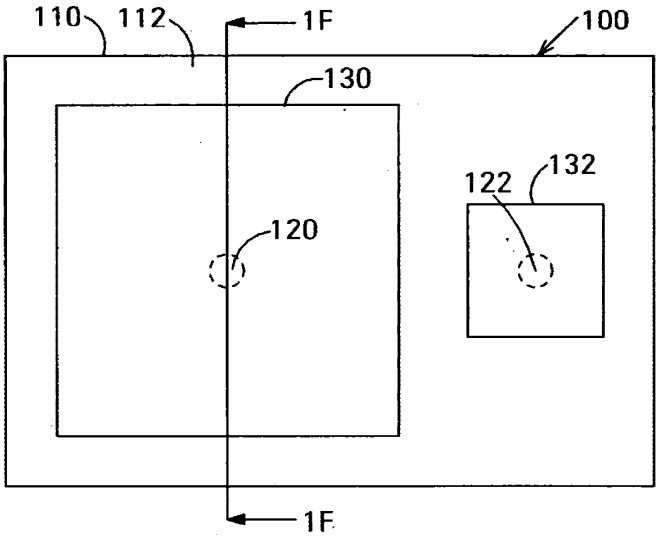

FIG.1D

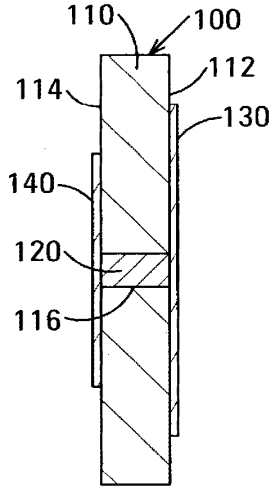

FIG.1F

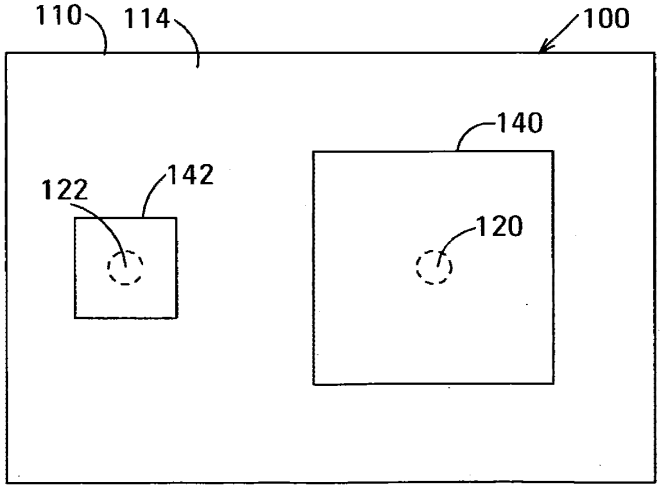

FIG.1E

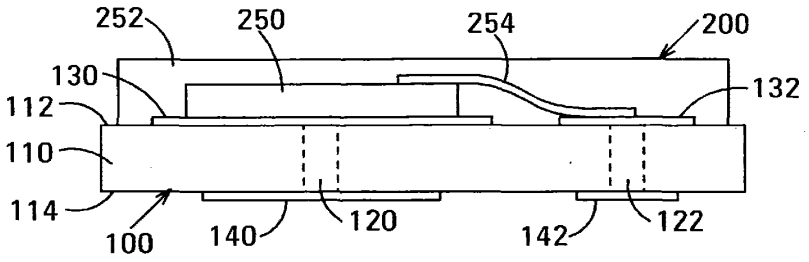

FIG.2B

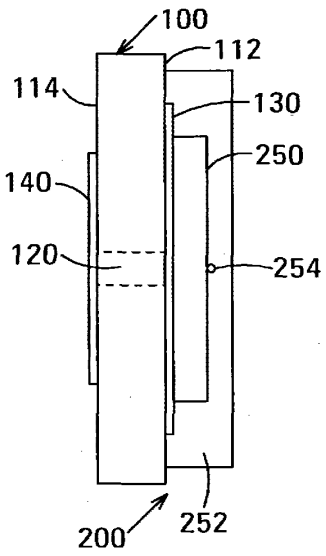

FIG.2C

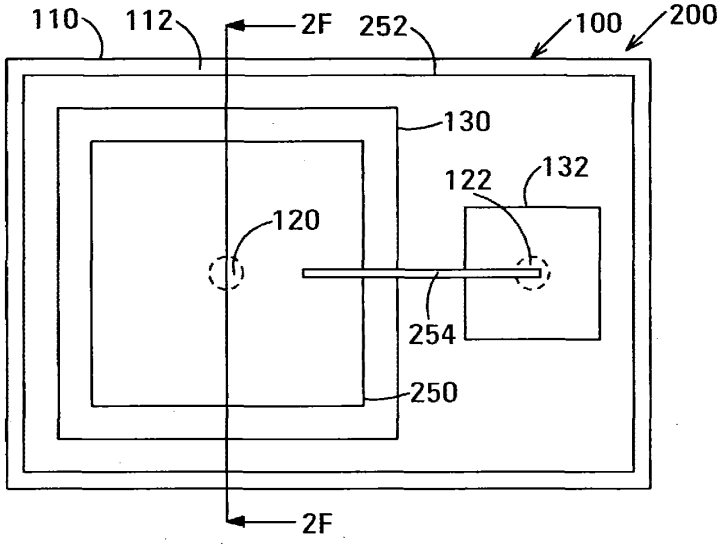

FIG.2D

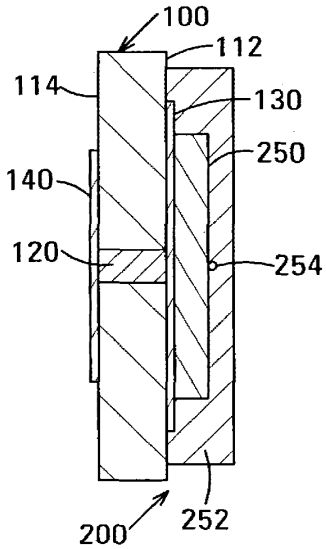

FIG.2F

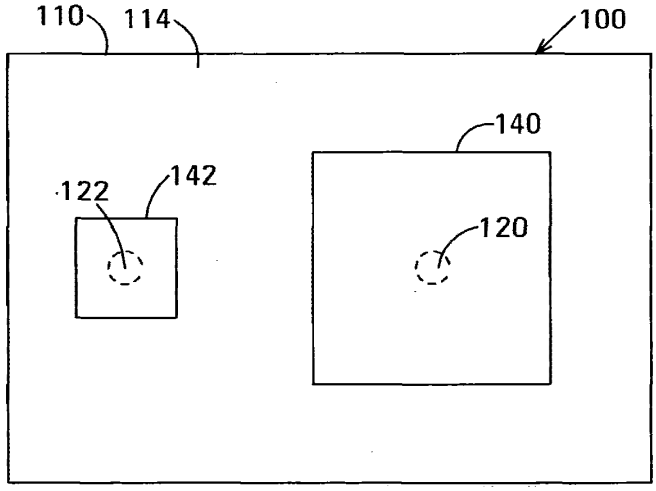

FIG.2E

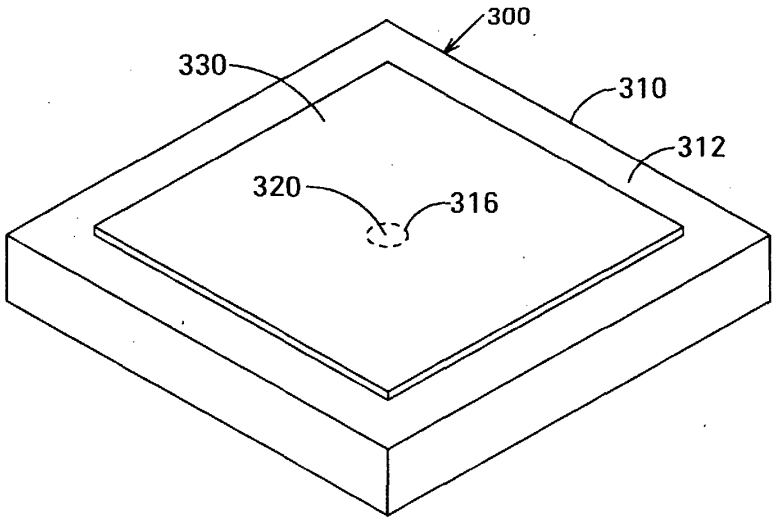

FIG.3A

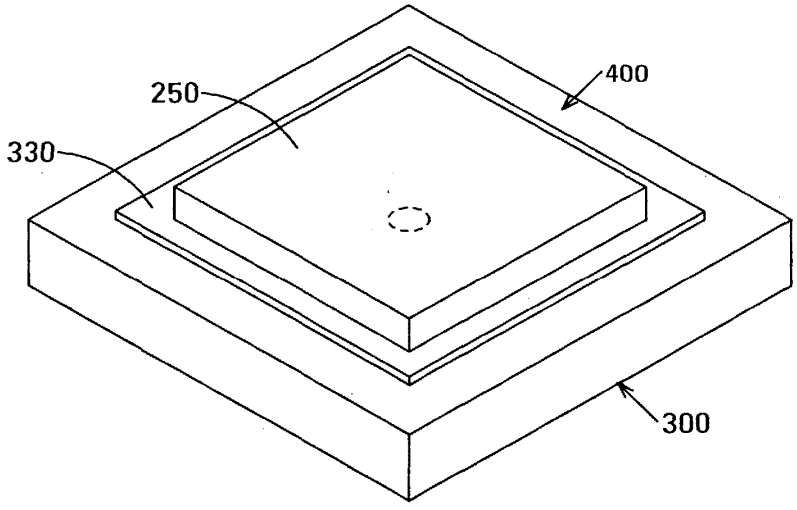

FIG.4A

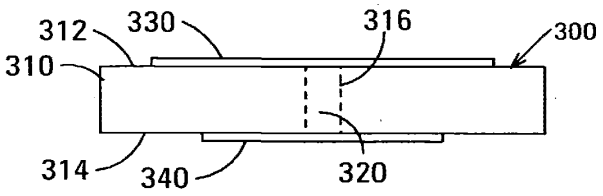

FIG.3B

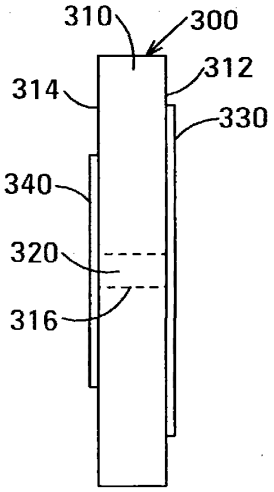

FIG.3C

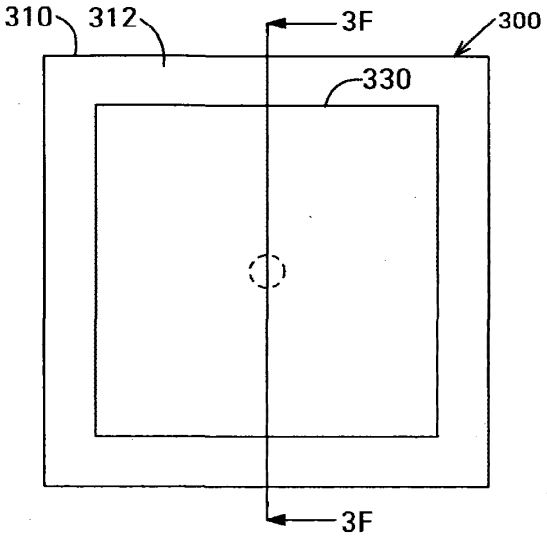

FIG.3D

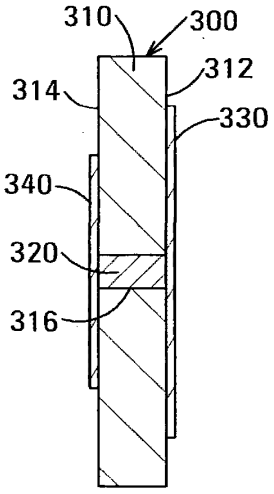

FIG.3F

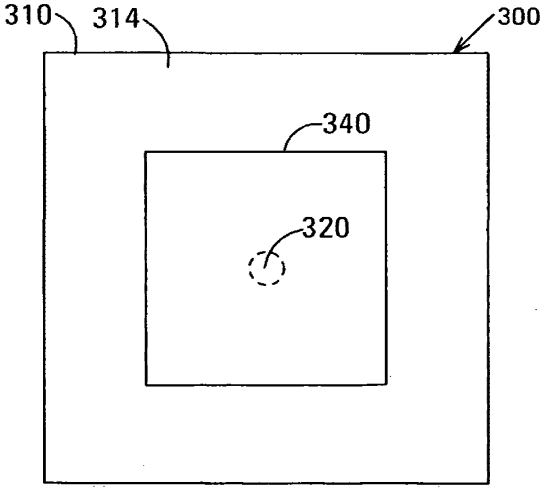

FIG.3E

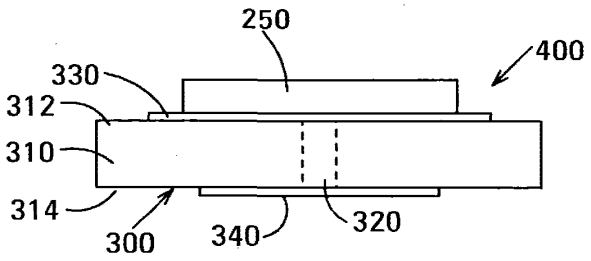

FIG.4B

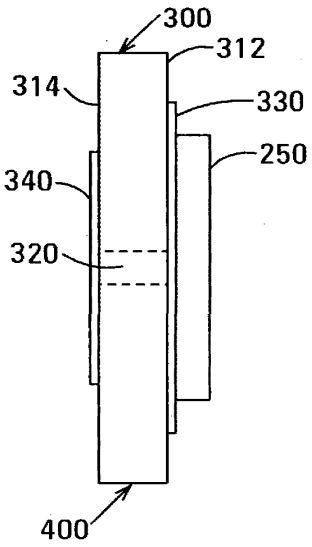

FIG.4C

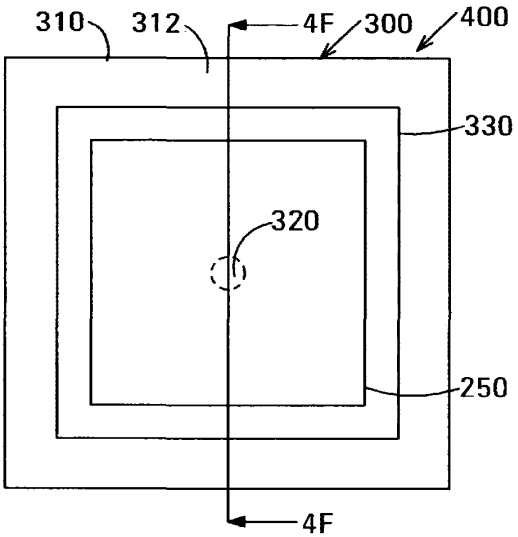

FIG.4D

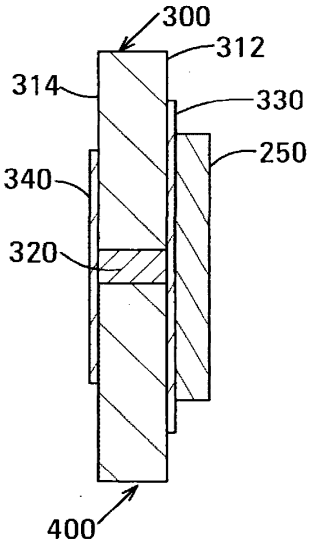

FIG.4F

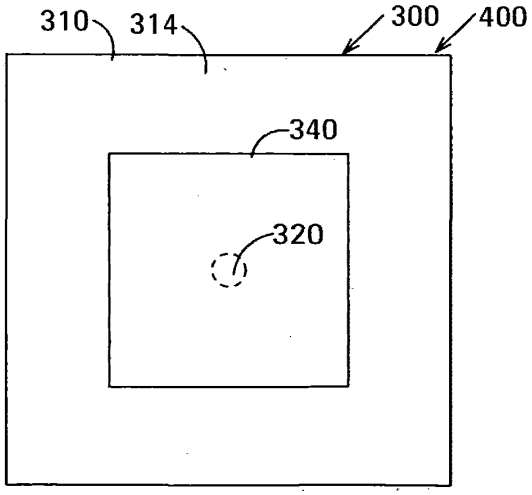

FIG.4E

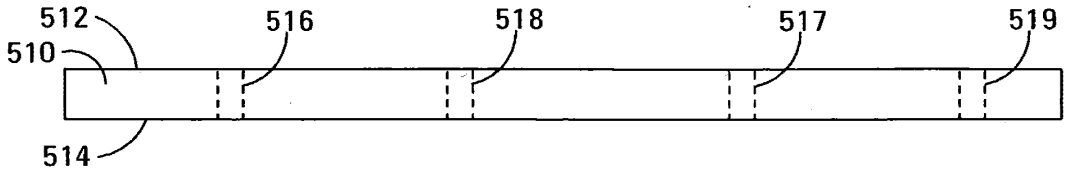

FIG.5A

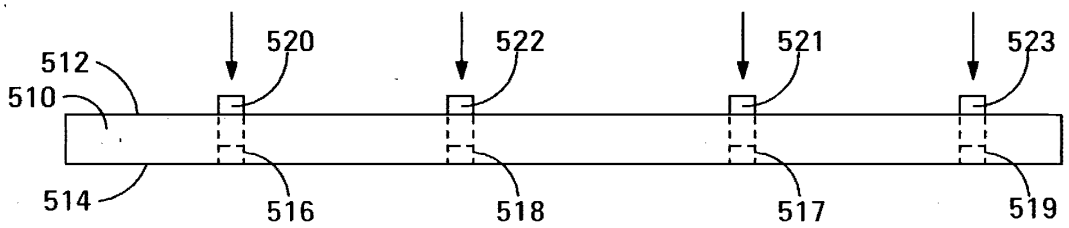

FIG.5B

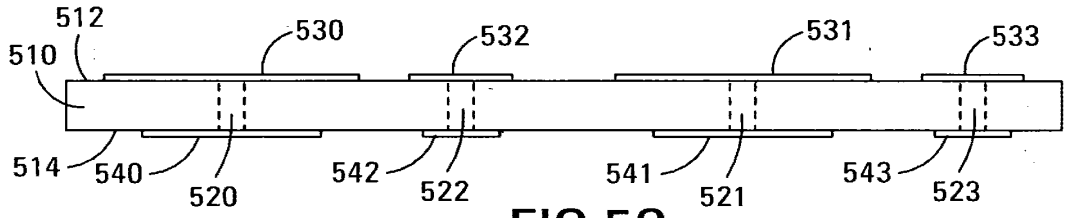

FIG.5C

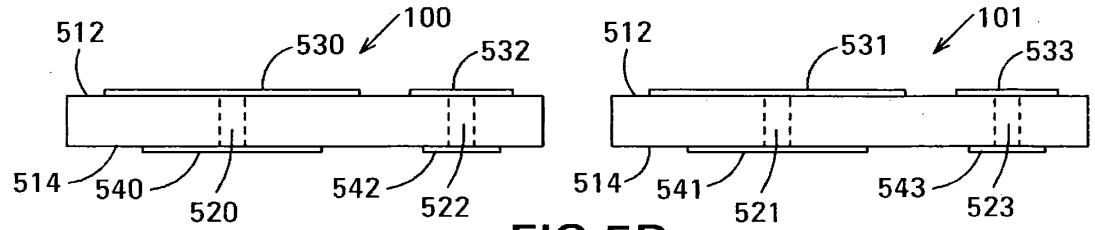

FIG.5D

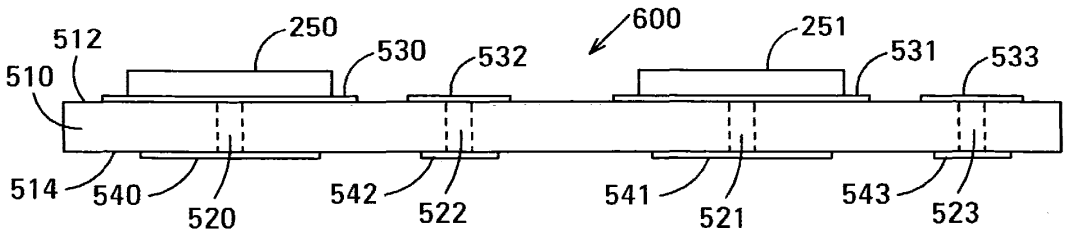

FIG.6A

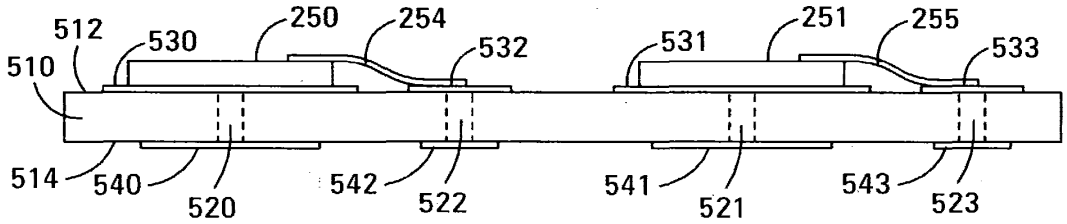

FIG.6B

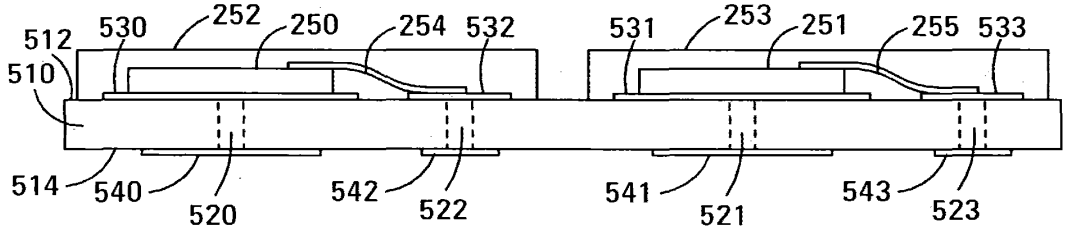

FIG.6C

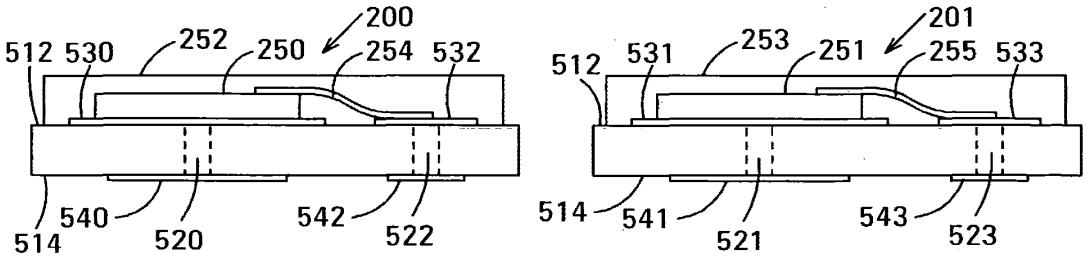

FIG.6D

PATENT APPLICATION

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO. 70030289

As a bel w named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the riginal, first and sole inv ntor (if only ne name is listed bel w) r an riginal, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and f r which a patent is sought on the inventi n entitled:

PACKAGING DEVICE FOR SEMICONDUCTOR DIE, AND SEMICONDUCTOR DEVICE INCORPORATING SAME

th specification of which is attached hereto unless the following box is checked:

( ) was filed on _____ as US Application Serial No. or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES: ___ NO: ___
			YES: ___ NO: ___

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION SERIAL NUMBER	FILING DATE

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Customer Number 022879

Place Customer Number Bar Code Label here

Send Correspondence to:	Direct Telephone Calls To:
AGILENT TECHNOLOGIES, INC. Legal Department, DL429 Intellectual Property Administration P. . Box 7599 Loveland, Colorado 80537-0599	Ian Hardcastle (650) 485-3015

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Inventor: Kong Weng Lee Citizenship: Malaysian

Residence: Lahat Court 48-2-1 Jalan Sekolah La Sall , 10450 Penang, Malaysia

Post Office Address: Same as Residence

Inventor's Signature: _____ Date: 26. June 2003

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATI N (continued)

ATTORNEY DOCKET NO. 70030259

Full Name of # 2 joint inventor: Kee Yean Ng Citizenship: Malaysian

Residence: 6, Halaman Kikik, Taman Inderawasih, 13600 Prai, Penang, Malaysia

Post Office Address: Same as Residence

Inventor's Signature June 26, 2003 Date

Full Name of # 3 joint inventor: Yew Cheong Kuan Citizenship: Malaysian

Residence: 8-4-5 Desa University, Jalan Sungao Dua, 11700 Penang, Malaysia

Post Office Address: Same as Residence

Inventor's Signature June 26, 2003 Date

Full Name of # 4 joint inventor: Gin Ghee Tan Citizenship: Malaysian

Residence: 18-11-03, Taman Seri Sari, Hilir Payar Terubong 1, Relau, 11900 Bayan Lepas, Penang, Malaysia

Post Office Address: Same as Residence

Inventor's Signature June 26, 2003 Date

Full Name of # 5 joint inventor: Cheng Why Tan Citizenship: Malaysian

Residence: 3843, Chip Joo Estate, Bukit Tengah, 14000, Bukit Mertajam, Penang, Malaysia

Post Office Address: Same as Residence

Inventor's Signature June 26, 2003 Date

Full Name of # 6 joint inventor: Citizenship:

Residence:

Post Office Address:

Inventor's Signature Date

Full Name of # 7 joint inventor: Citizenship:

Residence:

Post Office Address:

Inventor's Signature Date

Full Name of # 8 joint inventor: Citizenship:

Residence:

Post Office Address:

Inventor's Signature Date

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

07/02/2003 MGEBREM1 00000032 501078 10608605
01 FC:1001 750.00 DA

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: 10608605

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	20	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	40 minus 20=	* 20
INDEPENDENT CLAIMS	2 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	750

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	06/27/2003	Kong Weng Lee	70030259-1	2253

7590 08/23/2004

AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, CO 80537-0599

EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,605	LEE ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 102

1.The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 6, 7, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Wyland (US 5,986,885).

3. Regarding Claim 1, Wyland discloses a packaging device for semiconductor die, comprising:

a substantially planar substrate having opposed major surfaces (60) (Figure 6),

a conductive "mounting pad" (61) located on one of the major surfaces,

a conductive "connecting pad" (63) located on the other of the major surfaces, and

a conductive interconnecting element (62) extending through the substrate (60) and electrically interconnecting the mounting pad (61) and connecting pad (63).

4. Regarding Claims 2 and 7, Wyland discloses (Col. 7, lines 22 – 25) that the substrate comprises ceramic.

5. Regarding Claims 4 and 9, Wyland discloses (Col. 7, lines 31 – 39) that the mounting pad (61), and the connecting pad (63) are composed of copper.

6. Regarding Claim 6, Wyland discloses the packaging device of Claim 1, additionally comprising:

a bonding pad (right side, Figure 6) (31) (Col. 7, lines 19 – 21) located "on" one of the major surfaces,

an additional conductive connecting pad (63, right side) located on the other of the major surfaces, and

an additional conductive interconnecting element (62, right side) extending through the substrate and electrically interconnecting the bonding pad and the additional connecting pad.

7. Claims 11, 12, 16, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiuchi et al. (US 6,084,295).

8. Regarding Claim 11, Horuichi et al. disclose a semiconductor device, comprising:

a substantially planar substrate having opposed major surfaces (5) Figure 1),

a conductive "mounting pad" (upper surface) (Figures 1, 7(a) and 7(c)) (Col. 6, line 64 – Col. 7, line 2) located on one of the major surfaces,

a conductive connecting pad located on the other of the major surfaces Figures 1, 7(a) and 7(c)) (Col. 6, line 64 – Col. 7, line 2),

a conductive interconnecting element (42) extending through the substrate and electrically connecting the mounting pad and the connecting pad (Col. 6, line 64 – Col. 7, line 2), and

a semiconductor die (10) (Figure 1) attached to the mounting pad.

9. Regarding Claims 12 and 18, Horiuchi et al. discloses (Col. 6, lines 1 – 3) that the substrate is ceramic.

10. Regarding Claim 16, the three claim elements are discussed in Claim 11. Further, Horiuchi et al. disclose a bonding wire (20) (Figure 1) extending between the semiconductor die (10) and the bonding pad.

11. Regarding Claim 17, Horiuchi et al. disclose that an encapsulant (34) (Figure 1) encapsulates the semiconductor die and at least a portion of the major surface of the substrate on which the mounting pad is located (Col. 5, lines 34 – 37).

Claim Rejections – 35 U.S.C. 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 3 and 8 are rejected under 35 103(a) as being unpatentable over Wyland, as applied to Claims 1, 2, 4, 6, 7, and 10, and further in view of Electronic Packaging and Production ("Innovative PCB Reinforcement," (February, 1997), p. 1).

14. Regarding Claims 3 and 8, Wyland does not disclose a substrate material composed of epoxy laminate. However, epoxy laminate substrates are well known and widely used in the art. Electronic Packaging and Production discloses (p. 1, middle column, bottom para.) that epoxy laminate substrates have been in use for almost a decade. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the disclosures of Electronic Packaging and Technology with Wyland to obtain a device with increased reliability and reduced fatigue at joints (p. 1, left column, 5th para.).

15. Claims 5 and 10 are rejected under 35 103(a) as being unpatentable over Wyland, as applied to Claims 1, 2, 4, 6, 7, and 10, and further in view of Wilson et al. ("Handbook of Multilevel Metallization for Integrated Circuits," Noyes Publ., Westwood, New Jersey, (1993), p. 868 – 872).

16. Regarding Claims 5 and 10, Wyland does not disclose a conductive interconnecting element (via) comprising tungsten. Wilson et al. disclose that conductive interconnect elements (vias) composed of tungsten are well established in the art (p.868, lines 7 – 12). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Wyland to reduce costs (p. 868, lines 11 – 12) and reduce signal delays (p. 872, Figure 10).

17. Claim 9 is rejected under 35 103(a) as being unpatentable over Wyland, as applied to Claims 1, 2, 4, 6, 7, and 10, and further in view of Moyer et al. (US 6,620,720 B1).

18.Regarding Claim 9, Wyland discloses (Col. 7, lines 31 – 39) that the mounting pad (61), and the connecting pad (63) are composed of copper, but does not disclose that the bond pad is composed of copper. Moyer et al. disclose (Col. 2, lines 48 – 49) that a copper contact (bond) pad (13) (Figure 1) is formed on the silicon substrate for either wire bonding or solder bump bonding. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moyer et al. with Wyland to provide a contact (bond) pad of low cost and high conductivity (Moyer et al., Col. 1, lines 41 – 43).

18. Claims 13 and 18 are rejected under 35 103(a) as being unpatentable over Horiuchi et al., as applied to Claims11, 12, 16, and 17, and further in view of Electronic Packaging and Production.

19. Regarding Claims 13 and 18, Horuichi et al. do not disclose a substrate material composed of epoxy laminate. However, epoxy laminate substrates are well known and widely used in the art. Electronic Packaging and Production discloses (p. 1, middle column, bottom para.) that epoxy laminate substrates have been in use for almost a decade. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the disclosures of Electronic Packaging and Technology with Horuichi et al. to obtain a device with increased reliability and reduced fatigue at joints (p. 1, left column, 5th para.).

20. Claims 15 and 20 are rejected under 35 103(a) as being unpatentable over Horiuchi et al., as applied to Claims 11, 12, 16, and 17, and further in view of Wilson et al.

21. Regarding Claims 15 and 20, Horuichi et al. do not disclose a conductive interconnecting element (via) comprising tungsten. Wilson et al. disclose that conductive interconnect elements (vias) composed of tungsten are well established in the art (p.868, lines 7 – 12). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Horuichi et al. to reduce costs (p. 868, lines 11 – 12) and reduce signal delays (p. 872, Figure 10).

22. Claim 19 is rejected under 35 103(a) as being unpatentable over Horuichi et al., as applied to Claims 11, 12, 16, and 17, and further in view of Moyer et al. and Wyland.

23. Regarding Claim 19, Horuichi et al. do not disclose that the mounting pad, bond pad, and connecting pad are composed of copper. However, Wyland discloses (Col. 7, lines 31 – 39) that the mounting pad (61), and the connecting pad (63) are composed of copper. Moyer et al. disclose (Col. 2, lines 48 – 49) that a copper contact (bond) pad (13) (Figure 1) is formed on the silicon substrate for either wire bonding or solder bump bonding. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moyer et al. and Wyland with Horuichi et al. to provide a metallic contact structures of low cost and high conductivity (Moyer et al., Col. 1, lines 41 – 43).

Conclusions

24. Any inquiry concerning this communication or earlier communications from the

Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
August 15, 2004

Notice of References Cited	Application/Control No. 10/608,605	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner Thomas J. Magee	Art Unit 2811	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,986,885	11-1999	Wyland, Christopher Paul	361/704
	B	US-6,084,295	07-2000	Horiuchi et al.	257/690
	C	US-6,620,720 B1	09-2003	Moyer et al.	438/612
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Syd R. Wilson, Clarence J. Tracy, and John L. Freeman, Jr., "Handbook of Multilevel Metallization for Integrated Circuits," N oyes Publ., Westwood, New Jersey (1993), pp. 868 - 872.
	V	Electronic Packaging and Production, "Innovative PCB Reinforcement," (February, 1997), p.1
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application No.	Applicant(s)	
10/608,605	LEE ET AL.	
Examiner	**Art Unit**	
Thomas J. Magee	2811	

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	+	Restricted	I	Interference	O	Objected

Claim		Date								
Final	Original									
	1	08/19/10								
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Search Notes

Application No.	Applicant(s)	
10/608,605	LEE ET AL.	
Examiner	**Art Unit**	
Thomas J. Magee	2811	

SEARCHED			
Class	Subclass	Date	Examiner
257	696	08/15/04	
	784		
	700		
	689		
	774		
	783		
361	707		
	718		
	719		
	706		
	717		
	720		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR

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Alexandria, Virginia 22313-1450
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BIBDATASHEET

Bib Data Sheet

CONFIRMATION NO. 2253

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/608,605	06/27/2003 RULE	257	2811	70030259-1

APPLICANTS

Kong Weng Lee, Penang, MALAYSIA;

Kee Yean Ng, Penang, MALAYSIA;
Yew Cheong Kuan, Penang, MALAYSIA;Gin Ghee Tan, Penang, MALAYSIA;
Cheng Why Tan, Penang, MALAYSIA;

** CONTINUING DATA **********

** FOREIGN APPLICATIONS **********

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 09/17/2003

Foreign Priority claimed 35 USC 119 (a-d) conditions met Verified and Acknowledged Examiner's Signature Initials	☐ yes ☒ no ☐ yes ☐ no ☐ Met after Allowance	STATE OR COUNTRY MALAYSIA	SHEETS DRAWING 8	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 2

ADDRESS
AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland , CO
80537-0599

TITLE
Packaging device for semiconductor die, semiconductor device incorporating same and method of making same

FILING FEE RECEIVED 750	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____

Agilent Technologies
Innovating the HP Way

Agilent Technologies Inc.
Legal Dept. DL429
P.O. Box 7599
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650 485-3015 telephone
650 485-5487 facsimile
ian_hardcastle@agilent .com

Facsimile

Date: November 23, 2004 **Fax number:** 703-872-9306

To: Examiner Thomas J. Magee **Total pages:** 19

From: Ian Hardcastle

Subject: US Patent Application 10/608,605
Attorney Docket: 70030259-1
Filed: June 27, 2003

Enclosed is the an Amendment in response to the Office Action dated August 23, 2004.

Respectfully submitted,

Ian Hardcastle
Reg. No. 34,075

AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P. O. Box 7599
Loveland, Colorado 80537-0599

PATENT APPLICATION

ATTORNEY DOCKET NO. 70030259-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Kong Weng Lee et al.

Serial No.: 10/608,605 **Examiner:** Thomas J. Magee

Filing Date: June 27, 2003 **Group Art Unit:** 2811

Title: PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME

COMMISSIONER FOR PATENTS
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

(X) Response/Amendment ( ) Petition to extend time to respond
( ) New fee as calculated below ( ) Supplemental Declaration
(X) No additional fee (Address envelope to "Mail stop Non-Fee Amendments")
( ) Other: _____ (fee $_____)

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	20	MINUS	20	= 0	X $18	$ 0
INDEP. CLAIMS	2	MINUS	3	= 0	X $88	$ 0
[ ] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ $300	$ 0
EXTENSION FEE	1ST MONTH $110.00 [ ]	2ND MONTH $430.00 [ ]	3RD MONTH $980.00 [ ]	4TH MONTH $1530.00 [ ]		$ 0
					OTHER FEES	$
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	$ 0

Charge $ 0 to Deposit Account 50-1078. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 50-1078 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 50-1078 under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this sheet is enclosed.

I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Date of Facsimile: Nov. 23, 2004

Typed Name: Linda A. Iimura

Signature: Linda A. Iimura

Respectfully submitted,

Kong Weng Lee et al.

By _____

Ian Hardcastle

Attorney/Agent for Applicant(s)
Reg. No. 34,075

Date: Nov. 23, 2004

Telephone No.: (650) 485-3015

I hereby certify that this correspondence is being transmitted via facsimile to the Commissioner for Patents at (703) 872 9306 on 23 November 2004.

By Linda A. Iimura Date Nov. 23, 2004

Linda A. Iimura

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Inventor(s): Kong Weng Lee et al. Group Art Unit: 2811

Serial No.: 10/608,605 Examiner: Thomas J. Magee

Filed: 27 June 2003

Title: *Packaging Device for Semiconductor Die, Semiconductor Device Incorporating Same and Method of Making Same*

Atty Docket: 70030259

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria
VA 22313-1450

Sir:

In response to the Official Action dated 23 August 2004, please amend the application as follows:

In the Claims

The claims currently pending in the application are as follows:

1. (currently amended) A packaging device for semiconductor die, the packaging device comprising:

a substantially planar substrate having opposed major surfaces;

located on one of the major surfaces, a conductive mounting pad for attachment of the die with a major surface of the die in contact therewith; ~~located on one of the major surfaces;~~

a conductive connecting pad located on the other of the major surfaces; and

a conductive interconnecting element extending through the substrate and electrically interconnecting the mounting pad and the connecting pad.

2. (originally presented) The packaging device of claim 1, in which the substrate comprises ceramic.

3. (originally presented) The packaging device of claim 1, in which the substrate comprises a material selected from epoxy laminate and silicon.

4. (originally presented) The packaging device of claim 1, in which the mounting pad and the connecting pad each comprise at least one of copper, silver, gold, nickel and tungsten.

5. (originally presented) The packaging device of claim 1, in which the conductive interconnecting element comprises tungsten.

6. (originally presented) The packaging device of claim 1, additionally comprising:

a bonding pad located on the one of the major surfaces,

an additional conductive connecting pad located on the other of the major surfaces, and

an additional conductive interconnecting element extending through the substrate and electrically interconnecting the bonding pad and the additional connecting pad.

7. (originally presented) The packaging device of claim 6, in which the substrate comprises ceramic.

8. (originally presented) The packaging device of claim 6, in which the substrate comprises a material selected from epoxy laminate and silicon.

9. (originally presented) The packaging device of claim 6, in which the mounting pad, the bonding pad and the connecting pads each comprise at least one of copper, silver, gold, nickel and tungsten.

10. (originally presented) The packaging device of claim 6, in which the interconnecting element comprises tungsten.

11. (originally presented) A semiconductor device, comprising:

a substantially planar substrate having opposed major surfaces;

a conductive mounting pad located on one of the major surfaces;

a conductive connecting pad located on the other of the major surfaces;

a conductive interconnecting element extending through the substrate and electrically interconnecting the mounting pad and the connecting pad; and

a semiconductor die attached to the mounting pad.

12. (originally presented) The semiconductor device of claim 11, in which the substrate comprises ceramic.

13. (originally presented) The semiconductor device of claim 11, in which the substrate comprises a material selected from epoxy laminate and silicon.

14. (originally presented) The semiconductor device of claim 11, in which the mounting pad and the connecting pad each comprise at least one of copper, silver, gold, nickel and tungsten.

15. (originally presented) The semiconductor device of claim 11, in which the conductive interconnecting element comprises tungsten.

16. (originally presented) The semiconductor device of claim 11, additionally comprising:

a conductive bonding pad located on the one of the major surfaces;

an additional conductive connecting pad located on the other of the major surfaces;

an additional conductive interconnecting element extending through the substrate and electrically interconnecting the bonding pad and the additional connecting pad, and

a bonding wire extending between the semiconductor die and the bonding pad.

17. (originally presented) The semiconductor device of claim 16, additionally comprising an encapsulant encapsulating the semiconductor die and at least a portion of the major surface of the substrate on which the mounting pad is located.

18. (originally presented) The semiconductor device of claim 16, in which the substrate comprises a material selected from ceramic, epoxy laminate and silicon.

19. (originally presented) The semiconductor device of claim 16, in which the mounting pad, the bonding pad and the connecting pads each comprise at least one of copper, silver, gold, nickel and tungsten.

20. (originally presented) The semiconductor device of claim 16, in which the conductive interconnecting element comprises tungsten.

Remarks

Claims 1-20 are active in the application.

I. CLAIM REJECTIONS UNDER 35 USC § 102(b)

Claims 1, 2, 4, 6, 7 and 10 are rejected under 35 USC § 102(b) as being anticipated by United States patent no. 5,986,885 of Wyland. The applicants respectfully traverse the rejection on the grounds that Wyland does not disclose every element of claims 1, 2, 4, 6, 7 and 10 as now amended.

Wyland's Figure 6 shows die 30 attached to first circuitry metallizations 61 by flip-chip bonding. The applicants respectfully submit that Wyland's first circuitry metallizations do not constitute a mounting pad in the sense in which the term is used in the application, i.e., a pad to which a semiconductor die is attached with the major surface of the die in contact with the mounting pad. The applicants have amended claim 1 accordingly. The applicants respectfully submit that Wyland neither teaches nor suggests "a conductive mounting pad for attachment of the die with a major surface of the die in contact therewith", as recited in claim 1 as now amended. Accordingly, the applicants respectfully submit that claim 1 is allowable.

The applicants further submit that claims 2-10, which depend on claim 1, are allowable because of their dependence on claim 1.

With regard to claim 6, the official action alleges that Wyland discloses a bonding pad, citing "(right side, Figure 6) (31) (Col. 7, lines 19 - 21)." The applicants respectfully disagree. Wyland's bonding pads 31 are described at col. 6, lines 48-49, as being "on the surface of die 30" and are clearly shown that way in Figure 6. The passage of Wyland's disclosure cited in the official action additionally describes the bonding pads 31 as being attached to first circuitry metallizations 61 by conventional means such as solder 59. Wyland's bonding pads 31 are shown in Figure 6 as being separated from the major surface of substrate 60 by solder 59. Thus, the applicants respectfully submit that Wyland's bonding pads 31 are not part of the semiconductor package. The applicants further submit that Wyland's bonding pads 31 cannot accurately be described as being

"on the one of the major surfaces [of the planar substrate]". Therefore, the applicants respectfully submit that Wyland does not disclose "a bonding pad located on the one of the major surfaces" as recited in claim 6 and that claim 6 is allowable for this additional reason.

Claims 11, 12, 16 and 17 are rejected under 35 USC § 102(b) as being anticipated by United States patent no. 6,084,295 of Horiuchi et al. (*Horiuchi*). The applicants respectfully traverse the rejection on the grounds that Horiuchi does not disclose every element of claims 11, 12, 16 and 17.

The official action alleges that Horiuchi discloses "a conductive "mounting pad" (upper surface) (Figures 1, 7(a) and 7(c)) (Col. 6, line 64 Col. 7, line 2) located on one of the major surfaces ... a conductive interconnecting element (42) extending through the substrate and electrically connecting the mounting pad and the connecting pad (Col. 6, line 64 - Col. 7, line 2); and a semiconductor die (10) (Figure 1) attached to the mounting pad."

In the embodiment shown in Horiuchi's Figure 1, a die 10 is attached to the major surface of a substrate 5. The applicants have been unable to find anything in Horiuchi's description of Figure 1 that teaches or suggests that the portion of the major surface of the substrate underlying the die is conducting. In Horiuchi's Figure 1, the vias underlying the die are given a reference numeral (16) different from that (18) assigned to the vias to which bonding wires are attached. Thus, there is nothing in Horiuchi's disclosure that teaches or suggests that vias 16 underlying the die are structured similarly to the vias 18 to which bonding wires are attached and that are shown in detail in Figure 2. Moreover, the applicants have been unable to find anything in Horiuchi's disclosure that teaches or suggests that any conductive structure exists located on the major surface of substrate 5 to which die 10 is attached. Since none of the vias 16 extends over the major surface of substrate 5 underneath die 10, the applicants respectfully submit that the embodiment of Horiuchi's semiconductor device does not comprise "a conductive mounting pad *located on* one of the major surfaces;" as recited in claim 11.

Horiuchi's Figures 7(a) and 7(b) show variations on the circuit board structure

shown in Figure 1. In particular, these Figures show different structures of the vias 18 to which the bonding wires are attached (see Figures 7(a) and 7(b) and col. 6, line 67-col. 7, line 1). The applicants have been unable to find anything in Horiuchi's disclosure that teaches or suggests that the vias 16 underlying die 10 could be structured similarly to the vias 42 shown in Figures 7(a) and 7(b). Moreover, even if the vias 16 underlying die 10 were structured similarly to the vias 42 shown in Figures 7(a) and 7(b), the resulting structure would not comprise "a conductive mounting pad *located on* one of the major surfaces [of a substantially planar substrate]." No part of the vias 42 extends over the major surface of substrate 5 on which the die 10 is mounted. Additionally, in the variations shown in Figures 7(a) and 7(b), the solder bumps 12 are located on the end surfaces of the vias 42 that extend through the substrate 5. No part of the vias 42 extends over the major surface of substrate 5 opposite that on which the die 10 is mounted. The variations shown in Figures 7(a) and 7(b) therefore additionally lack "a conductive connecting pad located on the other of the major surfaces," as recited in claim 11.

Accordingly, the applicants respectfully submit that Horiuchi cannot accurately be said to disclose at least "a conductive mounting pad located on one of the major surfaces [of a substantially planar substrate]", as recited in claim 11. The applicants therefore submit that Horiuchi does not disclose every element of claim 11, and that claim 11 is therefore allowable.

The applicants further submit that claims 12-20, which depend on claim 11, are also allowable because of their dependence on claim 11.

II. CLAIM REJECTIONS UNDER 35 USC § 103(a)

1. Claims 3 and 8

Claims 3 and 8 are rejected under 35 USC §103(a) as being unpatentable over Wyland as applied to claims 1, 2, 4, 6, 7 and 10 in view of *Innovative PCB Reinforcement*, ELECTRONIC PACKAGING AND PRODUCTION, 1 (February 1997) (the *Article*). The applicants traverse the rejection on the grounds that the official action does not set forth a prima facie case of obviousness that complies with the requirements of

MPEP § 2143.

First, the applicants respectfully submit that Wyland's semiconductor package, modified as proposed in the official action, would still lack a mounting pad, for the reason set forth above with reference to claim 1. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claims 3 and 8.

Second, the official action states:

> [I]t would have been obvious to one of ordinary skill in the art at the time of the invention to combine the disclosures of Electronic Packaging and Technology with Wyland to obtain a device with increased reliability and reduced fatigue at joints (p. 1, left column, 5th para.).

The Article discloses mounting thin, small outline integrated circuit packages (TSOPs) on a multilayer reinforced epoxy laminate printed circuit board. The TSOPs are composed of a semiconductor die attached to a metal lead frame. The die and part of the lead frame are encapsulated. Portions of the lead frame remote from the die are attached to the printed circuit board by solder. The use of an epoxy laminate as the material of the printed circuit board was apparently motivated by the need for the printed circuit board to match the coefficient of thermal expansion of the TSOPs to increase the reliability of solder connections between the TSOPs and the printed circuit board.

The structure of Wyland's device is different: a semiconductor die 30 is flip-chip mounted on first circuitry metallizations 61 located on the surface of a substrate 60.

The applicants respectfully submit that the person of ordinary skill in the art would appreciate that the thermal expansion considerations of Wyland's semiconductor device are so different from those of a TSOP attached to a printed circuit board that such person consider any teaching set forth in the Article with respect to the printed circuit board material as inapplicable to choosing the substrate material of Wyland's semiconductor package. Accordingly, the applicants respectfully submit that such person would lack a motivation to make the combination of references proposed in the official action.

The applicants therefore respectfully submit that the rejection of claims 3 and 8 is

improper because the rationale set forth in the official action for combining the cited references does not meet the requirements set forth in MPEP § 2143. The applicants therefore respectfully request that the rejection be withdrawn.

2. Claims 5 and 10

Claims 5 and 10 are rejected under 35 USC § 103(a) as being unpatentable over Wyland, as applied to Claims 1, 2, 4, 6, 7 and 10, in view of Wilson et al., HANDBOOK OF MULTILEVEL METALLIZATION FOR INTEGRATED CIRCUITS, 868 – 872, Noyes Publ., Westwood, New Jersey, (1993) (the *Handbook*). The applicants traverse the rejection on the grounds that the official action does not set forth a prima facie case of obviousness that complies with the requirements of MPEP § 2143.

First, the applicants respectfully submit that Wyland's device, modified as proposed in the official action, would still lack a mounting pad for the reason set forth above with reference to claim 1. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claims 5 and 10.

Second, the official action states:

> It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Wyland to reduce costs (p. 868, lines 11 - 12) and reduce signal delays (p. 872, Figure 10).

The cited passage of the *Handbook* describes the advantages of CVD tungsten in integrated circuits with three or more levels of metallization (p.868, line 8). The substrate 60 of Wyland's semiconductor device, on the other hand, has no more than two levels of metallization. Moreover, the portion of Wyland's semiconductor device to which the official action proposes to apply the teachings of the Handbook is the substrate of a semiconductor package. The applicants respectfully submit that the substrate of a semiconductor package cannot accurately be referred to as an integrated circuit. Accordingly, the applicants respectfully submit that the person of ordinary skill in the art would regard the teaching set forth in the Handbook with respect to the material of the interlayer plugs of an integrated circuit with three or more levels of metallization

inapplicable to the choice of material of the through holes 61 of Wyland's semiconductor package. Accordingly, the applicants respectfully submit that such person would lack a motivation to make the combination of references proposed in the official action.

Referring to the motivations proposed in the official action, the applicants have been unable to find any teaching in the Handbook with regard to tungsten having a cost advantage in an application other than an integrated circuit with three or more levels of metallization. Additionally, it is not clear from Figure 10 whether the data disclosed therein relates to interlayer plugs or to on-layer traces. The distance scales suggest the latter. Finally, it is not clear from Figure 10 that tungsten actually provides the advantage of reduced signal delays, as asserted in the official action.

Accordingly, the applicants respectfully submit that the motivation set forth in the official action for combining the cited references does not meet the requirements set forth in MPEP § 2143.

Therefore, the applicants respectfully submit that the rejection of claims 5 and 10 is improper because the prima facie case of obviousness set forth in the official action does not meet the requirements set forth in MPEP § 2143. The applicants therefore respectfully request that the rejection be withdrawn.

3. Claim 9

Claim 9 is rejected under 35 USC § 103(a) as being unpatentable over Wyland as applied to Claims 1, 2, 4, 6, 7 and 10 in view of United States patent no. 6,620,720 of Moyer et al. (*Moyer*). The applicants traverse the rejection on the grounds that the official action does not set forth a prima facie case of obviousness that complies with the requirements of MPEP § 2143.

First, the applicants respectfully submit that Wyland's device, modified as proposed in the official action, would still lack a mounting pad for the reason set forth above with reference to claim 1. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claim 9.

Second, the official action states:

> Wyland discloses (Col. 7, lines 31 - 39) that the mounting pad (61), and the connecting pad (63) are composed of copper, but does not disclose that the bond pad is composed of copper. Moyer et al. disclose (Col. 2, lines 48 - 49) that a copper contact (bond) pad (13) (Figure 1) is formed on the silicon substrate for either wire bonding or solder bump bonding.

The applicants respectfully submit that Wyland's semiconductor package, modified as proposed in the official action, additionally lacks a copper bonding pad located on the one of the major surfaces [of the substantially planar substrate] as claimed in claim 9. As noted above in the discussion of claim 6 on which claim 9 depends, Wyland's bonding pad 31 is located on the die 30 and cannot therefore be accurately be described as being "located on the one of the major surfaces [of the substantially planar substrate]". Accordingly, the applicants respectfully submit that the facie case of obviousness set forth in the official action does not comply with the requirements of MPEP § 2143 because the proposed combination of references does not teach or suggest all the claim limitations.

Third, the official action additionally states:

> It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moyer et al. with Wyland to provide a contact (bond) pad of low cost and high conductivity (Moyer et al., Col. 1, lines 41 - 43).

In the lines following the passage of Moyer's disclosure cited in the official action, Moyer discloses some of the many difficulties of using copper in integrated circuits. Moyer discloses a solution to the problems of using copper to form the bonding pads of an integrated circuit. Moyer's solution involves the deposition of several additional layers over the copper bonding pad. The applicants respectfully submit that the person of ordinary skill in the art would appreciate that the main motivation for adopting copper interconnects in integrated circuits, namely, maintaining low-resistance connections despite ever-decreasing feature sizes, does not apply to selecting the material of the bonding pads of Wyland's semiconductor package. The applicants respectfully submit that this absence of a motivation to use copper, together with Moyer's disclosure of the additional complexity of using copper, means that such person would have no motivation to adopt the teaching set forth in Moyer's disclosure with respect to the

material of the bonding pads of the packaging device.

Accordingly, the applicants respectfully submit that the rejection of claim 9 is improper because the prima facie case of obviousness set forth in the official action does not comply with the requirements of MPEP § 2143. The applicants therefore respectfully request that the rejection be withdrawn.

4. Claims 13 and 18

Claims 13 and 18 are rejected under 35 USC § 103(a) as being unpatentable over Horiuchi as applied to Claims 11, 12, 16, and 17, in view of the Article. The applicants traverse this rejection on the grounds that the prima facie case of obviousness set forth in the official action does not comply with the requirements of MPEP § 2143.

First, the applicants respectfully submit that Horiuchi's device, modified as proposed in the official action, would still lack a mounting pad for the reasons set forth above with reference to claim 11. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claims 13 and 18.

Second, the official action states:

> [I]t would have been obvious to one of ordinary skill in the art at the time of the invention to combine the disclosures of Electronic Packaging and Technology with Horiuchi et al. to obtain a device with increased reliability and reduced fatigue at joints (p. 1, left column, 5th para.).

Second, the disclosure of the Article is described above with reference to claims 3 and 8. The structure of Horiuchi's device package is different that of the TSOPs discussed in the Article: semiconductor die 10 is attached directly to the surface of substrate 5.

The applicants respectfully submit that the person of ordinary skill in the art would appreciate that the thermal expansion considerations of Horiuchi's device package are so different from those of a TSOP attached to a printed circuit board that such person would consider any teaching set forth in the Article with respect to printed circuit board material as inapplicable to choosing the substrate material of Horiuchi's device package.

Accordingly, the applicants respectfully submit that the rationale set forth in the official action for combining the cited references does not meet the requirements set forth in MPEP § 2143.

Therefore, the applicants respectfully submit that the rejection of claims 13 and 18 set forth in the official action does not comply with the requirements of MPEP § 2143 and respectfully request that the rejection be withdrawn.

5. Claims 15 and 20

Claims 15 and 20 are rejected under 35 USC § 103(a) as being unpatentable over Horiuchi as applied to Claims 11, 12, 16, and 17 in view of the Handbook The applicants traverse the rejection on the grounds that the official action does not set forth a prima facie case of obviousness that complies with the requirements of MPEP § 2143.

First, the applicants respectfully submit that Horiuchi's device, modified as proposed in the official action, would still lack a mounting pad for the reasons set forth above with reference to claim 11. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claims 15 and 20.

Second, the official action states:

> It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Horiuchi et al. to reduce costs (p. 868, lines 11 - 12) and reduce signal delays (p. 872, Figure 10).

As noted above, the cited passage of the Handbook describes the advantages of CVD tungsten in integrated circuits with three or more levels of metallization (p.868, line 8). The substrate of Horiuchi's device package, on the other hand, has no more than two levels of metallization. Moreover, the portion of Horiuchi's device to which the official action proposes to apply the teachings of the Handbook is the substrate of a device package. The applicants respectfully submit that the substrate of a device package cannot accurately be described as an integrated circuit. Accordingly, the applicants respectfully submit that the person of ordinary skill in the art would regard the teaching set forth in the Handbook with respect to the material of the interlayer plugs of an integrated circuit

with three or more levels of metallization as inapplicable to the choice of material of the vias of Horiuchi's device package. The applicants respectfully submit that such person would lack a motivation to make the combination of references proposed in the official action.

Referring to the motivations proposed in the official action, the applicants have been unable to find any teaching in the Handbook with regard to tungsten having a cost advantage in applications other than an integrated circuit with three or more levels of metallization. Finally, it is not clear from Figure 10 whether the data disclosed therein relates to interlayer plugs or to on-layer traces. The distance scales suggest the latter. Finally, it is not clear from Figure 10 that tungsten actually provides the advantage stated in the official action.

Accordingly, the applicants respectfully submit that the motivation set forth in the official action for combining the cited references does not meet the requirements set forth in MPEP § 2143.

Therefore, the applicants respectfully submit that the rejection of claims 15 and 20 is improper because the prima facie case of obviousness set forth in the official action does not meet the requirements set forth in MPEP § 2143. The applicants therefore respectfully request that the rejection be withdrawn.

6. Claim 19

Claim 19 is rejected under 35 USC § 103(a) as being unpatentable over Horiuchi as applied to Claims 11, 12, 16, and 17 in view of Moyer and Wyland. The applicants traverse the rejection on the grounds that the official action does not set forth a prima facie case of obviousness that complies with the requirements of MPEP § 2143.

First, the applicants respectfully submit that Horiuchi's device, modified as proposed in the official action, would still lack a mounting pad for the reasons set forth above with reference to claim 11. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claims 15 and 20.

Second, the official action states:

> It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moyer et al. and Wyland with Horiuchi et al. to provide a metallic contact structures of low cost and high conductivity (Moyer et al., Col. 1, lines 41 -43).

The applicants respectfully submit that the prima facie case of obviousness set forth in the official action does not comply with the requirements of MPEP § 2143 because it does not propose a motivation for modifying Horiuchi's device package in accordance with the teaching of Wyland.

Moreover, as noted above, in the lines following the passage of Moyer's disclosure cited in the official action, Moyer discloses some of the many difficulties of using copper in integrated circuits. Moyer discloses a solution to the problems of using copper to form the bonding pads of an integrated circuit. Moyer's solution involves the deposition of several additional layers over the copper bonding pad. The applicants respectfully submit that the person of ordinary skill in the art would appreciate that the main motivation for adopting copper interconnects in integrated circuits, namely, maintaining low-resistance connections despite ever-decreasing feature sizes, does not apply to selecting the material of the pads of Horiuchi's device package. The applicants respectfully submit that this absence of a motivation to use copper, together with Moyer's teaching of the additional complexity of using copper, means that such person would have no motivation to adopt the teaching set forth in Moyer's disclosure with respect to the material of the pads of Horiuchi's device package.

Accordingly, the applicants respectfully submit that the rejection of claim 19 is improper because the prima facie case of obviousness set forth in the official action does not comply with the requirements of MPEP § 2143. The applicants therefore respectfully request that the rejection be withdrawn.

The applicants respectfully request reconsideration of the rejected claims. The applicants believe that the application as now amended is in condition for allowance, and respectfully request such favorable action. If any matters remain outstanding in the application, the Examiner is respectfully invited to telephone the applicants' attorney at (650) 485-3015 so that these matters may be resolved.

Respectfully submitted,

Kong Weng Lee et al.

By: _____

Ian Hardcastle
Reg. No. 34,075

Dated: 04123

Tel.: (650) 485-3015

Agilent Technologies, Inc.
Legal Department, MS DL429
P.O. Box 7599
Loveland, CO 80537-0599

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: 10608605

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	20	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	20 minus 20=	* 0
INDEPENDENT CLAIMS	2 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	750

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 20	Minus	**	=
Independent	* 1	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Index of Claims

Application No.	Applicant(s)	
10/608,605	LEE ET AL.	
Examiner	**Art Unit**	
Thomas J. Magee	2811	

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	+	Restricted	I	Interference	O	Objected

Claim		Date	Claim		Date	Claim		Date
Final	Original	08/18/04	Final	Original		Final	Original	
	1			51			101	
	2			52			102	
	3			53			103	
	4			54			104	
	5			55			105	
	6			56			106	
	7			57			107	
	8			58			108	
	9			59			109	
	10			60			110	
	11			61			111	
	12			62			112	
	13			63			113	
	14			64			114	
	15			65			115	
	16			66			116	
	17			67			117	
	18			68			118	
	19			69			119	
	20			70			120	
	21			71			121	
	22			72			122	
	23			73			123	
	24			74			124	
	25			75			125	
	26			76			126	
	27			77			127	
	28			78			128	
	29			79			129	
	30			80			130	
	31			81			131	
	32			82			132	
	33			83			133	
	34			84			134	
	35			85			135	
	36			86			136	
	37			87			137	
	38			88			138	
	39			89			139	
	40			90			140	
	41			91			141	
	42			92			142	
	43			93			143	
	44			94			144	
	45			95			145	
	46			96			146	
	47			97			147	
	48			98			148	
	49			99			149	
	50			100			150	

19
1
20

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: 10608605

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	20	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	20 minus 20=	* 0
INDEPENDENT CLAIMS	2 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	750

11-23-04

CLAIMS AS AMENDED - PART II

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 20	Minus	**	=
Independent	* 2	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Index of Claims

Application No.	Applicant(s)
10/608,605	LEE ET AL.
Examiner	**Art Unit**
Thomas J. Magee	2811

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date									Claim		Date									Claim		Date								
Final	Original	8/19/05									Final	Original										Final	Original									
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	06/27/2003	Kong Weng Lee	70030259-1	2253

7590 02/09/2005

AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, CO 80537-0599

EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/608,605	LEE ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 102

1.The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 6, 7, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Wyland (US 5,986,885).

3. Regarding Claim 1, Wyland discloses a packaging device for semiconductor die, comprising:

a substantially planar substrate having opposed major surfaces (60) (Figure 6),

a conductive "mounting pad" (61) located on one of the major surfaces,

a conductive "connecting pad" (63) located on the other of the major surfaces, and

a conductive interconnecting element (62) extending through the substrate (60) and electrically interconnecting the mounting pad (61) and connecting pad (63).

The limitation, *"for attachment of the die with a major surface of the die in contact therewith,"* represents an intended use. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 370 F.2d

576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963).

4. Regarding Claims 2 and 7, Wyland discloses (Col. 7, lines 22 – 25) that the substrate comprises ceramic.

5. Regarding Claims 4 and 9, Wyland discloses (Col. 7, lines 31 – 39) that the mounting pad (61), and the connecting pad (63) are composed of copper.

6. Regarding Claim 6, Wyland discloses the packaging device of Claim 1, additionally comprising:

a bonding pad (right side, Figure 6) (61) located "on" one of the major surfaces,

an additional conductive connecting pad (63, right side) located on the other of the major surfaces, and

an additional conductive interconnecting element (62, right side) extending through the substrate and electrically interconnecting the bonding pad and the additional connecting pad.

7. Claims 11, 12, 16, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiuchi et al. (US 6,084,295).

8. Regarding Claim 11, Horuichi et al. disclose a semiconductor device, comprising:

a substantially planar substrate having opposed major surfaces (5) Figure 1),

a conductive "mounting pad" (upper surface) (22) located on one of the major surfaces,

a conductive connecting pad located on the other of the major surfaces (24) (Figure 1)

a conductive interconnecting element (at18) extending through the substrate and electrically connecting the mounting pad and the connecting pad (Col. 3, lines 59 – 63), and

a semiconductor die (10) (Figure 1) attached to the mounting pad.

9. Regarding Claims 12 and 18, Horiuchi et al. discloses (Col. 6, lines 1 – 3) that the substrate is ceramic.

10. Regarding Claim 16, the three claim elements are discussed in Claim 11. Further, Horiuchi et al. disclose a bonding wire (20) (Figure 1) extending between the semiconductor die (10) and the bonding pad.

11. Regarding Claim 17, Horiuchi et al. disclose that an encapsulant (34) (Figure 1) encapsulates the semiconductor die and at least a portion of the major surface of the substrate on which the mounting pad is located (Col. 5, lines 34 – 37).

Claim Rejections – 35 U.S.C. 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art

are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 3 and 8 are rejected under 35 103(a) as being unpatentable over Wyland, as applied to Claims 1, 2, 4, 6, 7, and 10, and further in view of Electronic Packaging and Production ("Innovative PCB Reinforcement," (February, 1997), p. 1).

14. Regarding Claims 3 and 8, Wyland does not disclose a substrate material composed of epoxy laminate. However, epoxy laminate substrates are well known and widely used in the art. Electronic Packaging and Production discloses (p. 1, middle column, bottom para.) that epoxy laminate substrates have been in use for almost a decade. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the disclosures of Electronic Packaging and Technology with Wyland to obtain a device with increased reliability and reduced fatigue at joints (p. 1, left column, 5th para.).

15. Claims 5 and 10 are rejected under 35 103(a) as being unpatentable over Wyland, as applied to Claims 1, 2, 4, 6, 7, and 10, and further in view of Wilson et al. ("Handbook of Multilevel Metallization for Integrated Circuits," Noyes Publ., Westwood, New Jersey, (1993), p. 868 – 872).

16. Regarding Claims 5 and 10, Wyland does not disclose a conductive interconnecting element (via) comprising tungsten. Wilson et al. disclose that conductive interconnect elements (vias) composed of tungsten are well established in the art (p.868, lines 7 – 12). It would have

been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Wyland to reduce costs (p. 868, lines 11 – 12) and reduce signal delays (p. 872, Figure 10).

17. Claim 9 is rejected under 35 103(a) as being unpatentable over Wyland, as applied to Claims 1, 2, 4, 6, 7, and 10, and further in view of Moyer et al. (US 6,620,720 B1).

18.Regarding Claim 9, Wyland discloses (Col. 7, lines 31 – 39) that the mounting pad (61), and the connecting pad (63) are composed of copper, but does not disclose that the bond pad is composed of copper. Moyer et al. disclose (Col. 2, lines 48 – 49) that a copper contact (bond) pad (31) (Figure 1) is formed on the silicon substrate for either wire bonding or solder bump bonding. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moyer et al. with Wyland to provide a contact (bond) pad of low cost and high conductivity (Moyer et al., Col. 1, lines 41 – 43).

18. Claims 13 and 18 are rejected under 35 103(a) as being unpatentable over Horiuchi et al., as applied to Claims11, 12, 16, and 17, and further in view of Electronic Packaging and Production.

19. Regarding Claims 13 and 18, Horuichi et al. do not disclose a substrate material composed of epoxy laminate. However, epoxy laminate substrates are well known and widely used in the art. Electronic Packaging and Production discloses (p. 1, middle column, bottom para.) that epoxy laminate substrates have been in use for almost a decade. Hence, it would have been

obvious to one of ordinary skill in the art at the time of the invention to combine the disclosures of Electronic Packaging and Technology with Horuichi et al. to obtain a device with increased reliability and reduced fatigue at joints (p. 1, left column, 5th para.).

20. Claims 15 and 20 are rejected under 35 103(a) as being unpatentable over Horiuchi et al., as applied to Claims 11, 12, 16, and 17, and further in view of Wilson et al.

21. Regarding Claims 15 and 20, Horuichi et al. do not disclose a conductive interconnecting element (via) comprising tungsten. Wilson et al. disclose that conductive interconnect elements (vias) composed of tungsten are well established in the art (p.868, lines 7 – 12). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Horuichi et al. to reduce costs (p. 868, lines 11 – 12) and reduce signal delays (p. 872, Figure 10).

22. Claim 19 is rejected under 35 103(a) as being unpatentable over Horuichi et al., as applied to Claims 11, 12, 16, and 17, and further in view of Moyer et al. and Wyland.

23. Regarding Claim 19, Horuichi et al. do not disclose that the mounting pad, bond pad, and connecting pad are composed of copper. However, Wyland discloses (Col. 7, lines 31 – 39) that the mounting pad (61), and the connecting pad (63) are composed of copper. Moyer et al. disclose (Col. 2, lines 48 – 49) that a copper contact (bond) pad (13) (Figure 1) is formed on the silicon substrate for either wire bonding or solder bump bonding. It would have been obvious to

one of ordinary skill in the art at the time of the invention to combine Moyer et al. and Wyland with Horuichi et al. to provide a metallic contact structures of low cost and high conductivity (Moyer et al., Col. 1, lines 41 – 43).

Response to Arguments

24. Arguments of Applicant with respect to claim rejections have been carefully considered, but these have been found to be unpersuasive. With regard to Claim 1, the limitation recited in the amended claim represents an intended use and does not result in a structural distinction relevant to the prior art, as discussed in the Office Action.

With regard to Claim 6, Applicant is incorrect in the contention (pp. 6 – 7, Response) that the bonding pad (61) on the right side is not on one of the major surfaces. Figure 6 clearly discloses this location.

The contention that the pad 22 of Horiuchi et al. is not conducting (pp. 7 – 8, Response) is not correct. In order for the pad to be used as an electrical connection, it is essential that the pad be conducting. Further,the contention that there is no conductive pad on the "other" side is not germane, since a pad is shown (Figure 1) (24). Additionally, metal is plated inside via 18 to form an interconnecting element (Col. 3, lines 59 – 63).

In regard to the ELECTRONIC PACKAGING AND PRODUCTION reference (pp. 8 – 9, Response), contrary to allegations of Applicant, there is more than adequate rationale for combining references, as stated in the Office Action. Additionally, as stated in the Office Action, the

use of multilayer laminate boards are extremely well known in the art and widely utilized.

With regard to Claims 5 and 10, Applicant is incorrect in the allegation that the Wilson et al. textbook reference refers to a multilayer structure and does not teach the use of vias (pp. 10 – 11, Response). The reference states that tungsten vias have been used since 1983. Wilson states that *multilevel metallizations use a blanket deposition and etchback for formation.* There is no statement or implication that multilevels are required for via formation. Cost savings (p.868, lines 11 – 12) are indeed recited as a part of a selective deposition process. Reduction in signal delays are also present, as shown clearly in Figure 10, page 872 in a comparative analysis.

Allegations by Applicant that the combination of Moyer et al. and Wyland is not warranted (pp. 11 – 12, Response) are incorrect. There is more than sufficient motivation (Moyer et al., Col. 1, lines 41 – 43) to use the copper contact pad of Moyer et al. in Wyland. No probative data has been presented to suggest otherwise.

Commentary on Arguments presented for Claims 13 and 18 and Claims 15 and 20 (pp. 13 – 15) has been discussed above.

Allegations by Applicant regarding the applicability of Moyer as a secondary reference are not germane. There is adequate motivation for combining references (Moyer et al., Col. 1, lines 41 - 43). Applicant is reminded that the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference, nor Is it that the claimed invention must be expressly suggested in any one or all of the references.

Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller,* 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

For the reasons stated above, the rejection is maintained.

Conclusions

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax

number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
February 2, 2005

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/608,605	LEE ET AL.
Examiner	**Art Unit**
Thomas J. Magee	2811

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
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Agilent Technologies
Innovating the HP Way

Facsimile

Date:	**April 6, 2005**	**Fax number:**	**703-872-9306**
To:	**Examiner Thomas J. Magee**	**Total pages:**	**20**
From:	**Ian Hardcastle**		

Subject: US Patent Application 10/608,605
Attorney Docket: 70030259-1
Filed: June 27, 2003

Enclosed is the an Amendment in response to the Office Action dated February 9, 2005.

Respectfully submitted,

Ian Hardcastle
Reg. No. 34,075

AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P. O. Box 7599
Loveland, Colorado 80537-0599

ATTORNEY DOCKET NO. 70030259-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Kong Weng Lee, et al.

Serial No.: 10/608605 **Examiner:** Thomas J. Magee

Filing Date: June 27, 2003 **Group Art Unit:** 2811

Title: Packaging Device For Semiconductor Die, Semiconductor Device Incorporating Same And Method of Making Same

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

- [x] Response/Amendment
- [ ] Petition to extend time to respond
- [ ] New fee as calculated below
- [ ] Supplemental Declaration
- [x] No additional fee (Address envelope to "Mail Stop Amendments")
- [ ] Other: (Fee $____)

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	20	MINUS	20	= 0	X 50	$ 0
INDEP. CLAIMS	2	MINUS	3	= 0	X 200	$ 0
☐ FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ 360	$ 0
EXTENSION FEE	1ST MONTH 120.00 ☐	2ND MONTH 450.00 ☐	3RD MONTH 1020.00 ☐	4TH MONTH 1590.00 ☐		$ 0
					OTHER FEES	$ 0
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	$ 0

Charge $ 0 to Deposit Account **50-1078**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-1078** pursuant to 37 CFR 1.2 5. Additionally please charge any fees to Deposit Account **50-1078** under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this transmittal letter is enclosed.

Respectfully submitted,
Kong Weng Lee, et al.
By
Ian Hardcastle
Attorney/Agent for Applicant(s)
Reg. No. 34,075
Date: April 6, 2005
Telephone No. 650 485 3015

I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below:

Date of facsimile: April 6, 2005

Typed Name: Linda A. Iimura

Signature: Linda A. Iimura

Rev 10/04 (TransAmd)

I hereby certify that this correspondence is being transmitted via facsimile to the Commissioner for Patents at (703) 872 9306 on 6 April 2005

By Linda Ce Ilimura Date April 6, 2005
Linda A. Ilimura

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Inventor(s): Kong Weng Lee et al. Group Art Unit: 2811

Serial No.: 10/608,605 Examiner: Thomas J. Magee

Filed: 27 June 2003

Title: *Packaging Device for Semiconductor Die, Semiconductor Device Incorporating Same and Method of Making Same*

Atty Docket: 70030259

AMENDMENT UNDER 37 CFR § 1.116

Commissioner for Patents
P.O. Box 1450
Alexandria
VA 22313-1450

Sir:

In response to the Official Action dated 9 February 2005, the applicants respectfully request entry of the following amendments:

In the Claims

The claims currently pending in the application are as follows:

1. (currently amended) A packaging device for a semiconductor die, the packaging device comprising:

a substantially planar substrate having opposed major surfaces;

located on one of the major surfaces; a conductive die mounting pad ~~for attachment of~~ dimensioned to accommodate the die with a major surface of the die in contact therewith;

a conductive connecting pad located on the other of the major surfaces; and

a conductive interconnecting element extending through the substrate and electrically interconnecting the mounting pad and the connecting pad.

2. (original) The packaging device of claim 1, in which the substrate comprises ceramic.

3. (original) The packaging device of claim 1, in which the substrate comprises a material selected from epoxy laminate and silicon.

4. (original) The packaging device of claim 1, in which the mounting pad and the connecting pad each comprise at least one of copper, silver, gold, nickel and tungsten.

5. (original) The packaging device of claim 1, in which the conductive interconnecting element comprises tungsten.

6. (currently amended) The packaging device of claim 1, additionally comprising:

a bonding pad smaller in area than the die mounting pad, the bonding pad located on the one of the major surfaces,

an additional conductive connecting pad located on the other of the major surfaces, and

an additional conductive interconnecting element extending through the substrate and electrically interconnecting the bonding pad and the additional connecting pad.

7. (original) The packaging device of claim 6, in which the substrate comprises ceramic.

8. (original) The packaging device of claim 6, in which the substrate comprises a material selected from epoxy laminate and silicon.

9. (original) The packaging device of claim 6, in which the mounting pad, the bonding pad and the connecting pads each comprise at least one of copper, silver, gold, nickel and tungsten.

10. (original) The packaging device of claim 6, in which the interconnecting element comprises tungsten.

11. (currently amended) A semiconductor device, comprising:

a semiconductor die;

a substantially planar substrate having opposed major surfaces;

~~a conductive mounting pad~~ located on one of the major surfaces, a conductive die mounting pad dimensioned to accommodate the semiconductor die;

a conductive connecting pad located on the other of the major surfaces; and

a conductive interconnecting element extending through the substrate and electrically interconnecting the mounting pad and the connecting pad; ~~and~~

in which the ~~a~~ semiconductor die is mounted on ~~attached to~~ the die mounting pad with a major surface thereof in contact with the mounting pad.

12. (original) The semiconductor device of claim 11, in which the substrate comprises ceramic.

13. (original) The semiconductor device of claim 11, in which the substrate comprises a material selected from epoxy laminate and silicon.

14. (original) The semiconductor device of claim 11, in which the mounting pad and the connecting pad each comprise at least one of copper, silver, gold, nickel and tungsten.

15. (original) The semiconductor device of claim 11, in which the conductive interconnecting element comprises tungsten.

16. (currently amended) The semiconductor device of claim 11, additionally comprising:

a conductive bonding pad smaller in area than the die mounting pad, the bonding pad located on the one of the major surfaces;

an additional conductive connecting pad located on the other of the major surfaces;

an additional conductive interconnecting element extending through the substrate and electrically interconnecting the bonding pad and the additional connecting pad, and

a bonding wire extending between the semiconductor die and the bonding pad.

17. (original) The semiconductor device of claim 16, additionally comprising an encapsulant encapsulating the semiconductor die and at least a portion of the major surface of the substrate on which the mounting pad is located.

18. (original) The semiconductor device of claim 16, in which the substrate comprises a material selected from ceramic, epoxy laminate and silicon.

19. (original) The semiconductor device of claim 16, in which the mounting pad, the bonding pad and the connecting pads each comprise at least one of copper, silver, gold, nickel and tungsten.

20. (original) The semiconductor device of claim 16, in which the conductive interconnecting element comprises tungsten.

Remarks

This is an amendment under 37 CFR § 1.116. The purpose of this amendment is to put the claims in better form for appeal. The amendments and specific arguments in this amendment, to the extent they were not presented earlier, are now presented because they are necessitated by the new arguments of anticipation and obviousness set forth by the Examiner in the official action dated 9 February 2005. The applicants respectfully submit that these amendments do not raise new issues and do not require any further searching.

Following this amendment, claims 1-20 are active in the application.

I. CLAIM REJECTIONS UNDER 35 USC § 102(b)

A. Claims 1, 2, 4, 6, 7, and 10

Claims 1, 2, 4, 6, 7, and 10 are rejected under 35 USC § 102(b) as being anticipated by United States patent no. 5,986,885 of Wyland. The official action alleges that the limitation, "for attachment of the die with a major surface of the die in contact therewith," represents an intended use. The applicants respectfully disagree, but to advance prosecution of the application have amended Claim 1 to recite a more explicit structural limitation.

The applicants respectfully submit that Wyland's metallization 61, alleged in the official action to correspond to the die mounting pad recited in Claim 1, cannot accurately be described as "dimensioned to accommodate the die with a major surface of the die in contact therewith" as recited in Claim 1 as now amended.

Accordingly, the applicants respectfully submit that Claim 1 as now amended, and claims 2-9 that depend on Claim 1, are all patentable.

B. Claim 6

With reference to claim 6, the official action alleges that Wyland discloses a bonding pad, citing "(right side, Figure 6) (61) located "on" one of the major surfaces." This differs from the rejection set forth in the previous official action mailed on 23 August 2004 in which Wyland's *die bonding pad 31* was alleged to correspond to the bonding pad recited in Claim 6. In its Response to Arguments, the official action states that the applicants were incorrect and refers to

"bonding pad (61)." However, the applicants respectfully submit that the previous official action referred to element 31, i.e., to die bonding pad 31, and not to element 61, i.e., metallization 61, as now alleged.

The applicants have amended Claim 6 to recite: "a bonding pad smaller in area than the die mounting pad, the bonding pad located on the one of the major surfaces." The applicants respectfully submit that Wyland's metalizations 61 to which die 30 is attached are substantially similar in area, as would be expected given that the die is attached to each metallization by means of a flip-chip connection. The applicants therefore respectfully submit that, in Wyland's semiconductor package, the metallization 61 alleged to correspond to the bonding pad recited in claim 6 cannot accurately be said to be smaller in area than the metallization 61 alleged in the rejection of Claim 1 to correspond to the die mounting pad recited in Claim 1.

Accordingly, the applicants respectfully submit that Claim 6 as now amended is patentable for this additional reason, and Claims 7-10 that depend on Claim 6 are also patentable.

C. Claims 11, 12, 16, and 17

Claims 11, 12, 16, and 17 are rejected under 35 USC § 102(b) as being anticipated by United States patent no. 6,084,295 of Horiuchi et al. (*Horiuchi*).

The official action alleges that bonding pad 22 corresponds to the mounting pad recited in claim 11. The applicants respectfully thank the Examiner for clearly identifying the element allgeged to correspond to the mounting pad. The prior official action did not indicate that Horiuchi's bonding pad 22 corresponded to the mounting pad. In responding to the prior official action, the applicants took the reference to "upper surface" to refer to the upper surface of substrate 5 rather than to the upper surface of bonding pad 22. It appears that this is not what the Examiner intended.

The applicants respectfully submit that bonding pad 22 cannot accurately be said to correspond to "a conductive mounting pad located on one of the major surfaces" as recited in the original version of Claim 11. Horiuchi shows bonding pad 22 located in a region of substrate 5 outside that occupied by semiconductor chip 10. The original version of Claim 11 recites in part: "a semiconductor die attached to the mounting pad." The applicants respectfully submit that chip

10 cannot accurately be described as attached to bonding pad 22.

Moreover, Horiuchi shows vias 16 underlying chip 10. Figure 1 shows the ends of vias 16 adjacent chip 10 lying flush with the surface of substrate 5. The applicants therefore respectfully submit that the ends of vias 16 therefore cannot accurately be said to be "on" the major surface of the substrate. The official action provides no indication of where may be found in Horiuchi's disclosure a teaching that bonding pads similar to bonding pads 22 exist under chip 10. The applicants have been unable to find such teaching. Figures 7(a) and 7(c) referred to the prior official action show structures of pads to which bonding wires 20 are attached, and not of the vias underlying chip 10.

Nevertheless, to advance prosecution of the application and to conform Claim 11 with Claim 1, the applicants have amended Claim 11 to recite: "located on one of the major surfaces, a conductive die mounting pad dimensioned to accommodate the semiconductor die" and "in which the semiconductor die is mounted on the die mounting pad with a major surface thereof in contact with the mounting pad." The applicants respectfully submit that Horiuchi's device lacks any element described by the quoted elements of Claim 11 as now amended.

Accordingly, the applicants respectfully submit that Claim 11 as now amended is patentable. The applicants further submit that Claims 12-19 that depend on Claim 11 are patentable due to the patentability of Claim 11.

II. CLAIM REJECTIONS UNDER 35 USC § 103(a)

A. Claims 3 and 8

Claims 3 and 8 are rejected under 35 USC § 103(a) as being unpatentable over Wyland as applied to Claims 1, 2, 4, 6, 7 and 10 in view of *Innovative PCB Reinforcement*, ELECTRONIC PACKAGING AND PRODUCTION, 1 (1997) (the *Article*).

The official action states that Wyland does not disclose a substrate material composed of epoxy laminate and looks to ELECTRONIC PACKAGING AND PRODUCTION for a disclosure of this material. The official action states:

> Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the disclosures of Electronic Packaging and Technology with Wyland to obtain a device with increased reliability and reduced fatigue at joints (p. 1, left column, 5 th para.).

The Article discloses mounting thin, small outline integrated circuit packages (TSOPs) on a multilayer reinforced epoxy laminate printed circuit board. The TSOPs are composed of a semiconductor die attached to a metal lead frame. The die and part of the lead frame are encapsulated. Portions of the lead frame remote from the die are attached to the printed circuit board by solder. The use of an epoxy laminate as the material of the printed circuit board was apparently motivated by the need for the printed circuit board to match the coefficient of thermal expansion of the TSOPs to increase the reliability of solder connections between the TSOPs and the printed circuit board.

The structure of Wyland's device is different: a semiconductor die 30 is flip-chip mounted on first circuitry metallizations 61 located on the surface of a substrate 60.

The applicants respectfully submit that the person of ordinary skill in the art would appreciate that the thermal expansion considerations of the semiconductor die 30 of Wyland's semiconductor device are so different from those of a TSOP attached to a printed circuit board that such person would consider any teaching set forth in the Article with respect to the printed circuit board material as inapplicable to choosing the substrate material of Wyland's semiconductor package. Accordingly, the applicants respectfully submit that the cited references lack any teaching or suggestion that could properly be regarded as providing a motivation for a person of ordinary skill in the art to combine the references in the manner proposed in the official action.

The official action states that multilayer laminate boards are extremely well known in the art and widely utilized. The applicants do not dispute this. However, the applicants respectfully remind the Examiner that the fact that multi-layer boards are known does not make it obvious to modify Wyland's semiconductor device to incorporate a multilayer board absent a teaching or suggestion in the cited references that can properly regarded as a motivation for a person of ordinary skill in the art to make such modification. The applicants respectfully submit that the passage of the Article cited in the official action does not rise to this level. It simply describes an advantage that arises in the specific circumstance in which TSOPs are mounted on a PC11 printed circuit board. The applicants have been unable to find anything in the Article that teaches or suggests that this advantage would be obtained in the context of Wyland's semiconductor

package in which a semiconductor die is flip-chip mounted on a substrate. The applicants have been unable to find anything in Wyland's disclosure that teaches or suggests that his semiconductor package has problems with solder joint reliability.

Moreover, the official action does not indicate where in the cited references may be found a teaching or suggestion that would provide a person of ordinary skill in the art with a reasonable expectation of success in the event such person were to attempt to modify Wyland's semiconductor package in the manner suggested in the official action.

Additionally, the applicants respectfully submit that Wyland's semiconductor package, modified as proposed in the official action, would still lack a die mounting pad, for the reason set forth above with reference to Claim 1. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claims 3 and 8.

The applicants therefore respectfully submit that the rejection of claims 3 and 8 is improper because the prima facie case of obviousness set forth in the official action does not meet the requirements set forth in MPEP § 2143. The applicants therefore respectfully request that the rejection be withdrawn.

B. Claims 5 and 10

Claims 5 and 10 are rejected under 35 USC § 103(a) as being unpatentable over Wyland as applied to Claims 1, 2, 4, 6, 7 and 10 in view of Wilson et al. (HANDBOOK OF MULTILEVEL METALLIZATION FOR INTEGRATED CIRCUITS, 868-872 (*Wilson*).

The official action indicates that Wyland does not disclose a conductive interconnecting element (via) comprising tungsten and looks to Wilson for a teaching of conductive interconnect elements (vias) composed of tungsten. The official action states:

> It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Wyland to reduce costs (p. 868, lines 11 - 12) and reduce signal delays (p. 872, Figure 10).

The cited passage of Wilson's disclosure describes the advantages of CVD tungsten contacts and via plugs in integrated circuits. The official action proposes to apply Wilson's teachings to the choice of the material to fill through holes 62 extending through the substrate 60 of Wyland's semiconductor package. The applicants respectfully submit that the substrate of a

semiconductor package cannot accurately be referred to as an integrated circuit. Accordingly, the applicants respectfully submit that the person of ordinary skill in the art would regard Wilson's teaching with respect to the material of the interlayer plugs of an integrated circuit inapplicable to the choice of material to fill the through holes 62 of Wyland's semiconductor package. Accordingly, the applicants respectfully submit that the cited passage of Wilson's disclosure does not provide a sufficient motivation for a person of ordinary skill in the art to make the combination of references proposed in the official action.

Moreover, the applicants respectfully submit that Wilson is non-analogous art and hence, is not a valid reference with respect to the invention claimed in Claims 5 and 10. The invention claimed in Claims 5 and 10 relates to a packaging device for a semiconductor die. Wilson's disclosure relates to the structure of the semiconductor die itself. The *Manual of Patent Classification* classifies Horiuchi's semiconductor device, which is analogous prior art, in class 257, subclass 690, whereas integrated circuit vias appear to fall into class 438.

The sentence that includes the passage of Wilson's disclosure cited in the official action as constituting a motivation reads: "There are also attempts to use a selective CVD tungsten because of the potential process simplification and cost savings." The applicants respectfully submit that this passage of Wilson's disclosure does not indicate whether the attempts have been successful or that the potential cost savings have been achieved. Moreover, the applicants have been unable to find any teaching in the cited passage or elsewhere in Wilson's disclosure that teaches or suggests that tungsten provides a cost advantage in an application other than in an integrated circuit. The applicants respectfully remind the Examiner that obviousness is not established if a person of ordinary skill might find it *obvious to try* to modify the teaching of one reference in accordance with the teachings of another. "[T]his is not the standard of 35 USC § 103." *In re Geiger*, 815 F2d 686, 688, 2 USPQ2d 1276, 1278 (Fed. Cir. 1987).

The official action additionally cites Wilson's Figure 10 as demonstrating that tungsten interconnects and inter-layer plugs reduce signal delays, and thus provide a motivation. The applicants respectfully submit that Figure 10 demonstrates that, with respect to signal delay in an integrated circuit, tungsten performs marginally better than aluminum but performs significantly worse than copper. The applicants therefore respectfully submit that, if anything, Wilson's

Figure 10 teaches away from using tungsten.

Moreover, the applicants have been unable to find anything in Wyland's disclosure that teaches or suggests that his semiconductor package is costly to manufacture and/or suffers from problems with signal delay that would provide a person of ordinary skill in the art with a motivation to look outside Wyland's disclosure for a solution to such problems.

The official action does not indicate where in the cited references may be found a teaching or suggestion that would provide a person of ordinary skill in the art with a reasonable expectation of success in the event such person were to undertake the modification of Wyland's semiconductor package proposed in the official action.

Finally, the applicants respectfully submit that Wyland's semiconductor package, modified as proposed in the official action, lacks the die mounting pad recited in Claim 1 on which Claims 5 and 10 depend for the reasons set forth above with reference to Claim 1. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest all the claim limitations recited in Claims 5 and 10.

The applicants therefore respectfully submit that the rejection of claims 5 and 10 is improper because the prima facie case of obviousness set forth in the official action does not meet the requirements set forth in MPEP § 2143. The applicants therefore respectfully request that the rejection be withdrawn.

C. Claim 9

Claim 9 is rejected under 35 USC § 103(a) as being unpatentable over Wyland as applied to Claims 1, 2, 4, 6, 7 and 10 in view of United States patent no. 6,620,720 of Moyer et al. (*Moyer*).

The official action indicates that Wyland does not disclose that the bond pad is composed of copper and looks to Moyer at (col. 2, lines 48 - 49) for a disclosure of a copper contact (bond) pad (31) (Figure 1) formed on the silicon substrate for either wire bonding or solder bump bonding. The official action states:

> It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moyer with Wyland to provide a contact (bond) pad of low cost and high conductivity (Moyer, col. 1, lines 41 - 43).

The applicants acknowledge that the cited passage of Moyer's disclosure describes the advantages of using copper as the material of the interconnects of an integrated circuit. However, in the lines following the cited passage of Moyer's disclosure, Moyer discloses some of the many difficulties of using copper as the material of the interconnects of an integrated circuit. Moyer discloses a solution to the problems of using copper to form the bonding pads of an integrated circuit. Moyer's solution involves the deposition of several additional layers over the copper bonding pad. The applicants respectfully submit that the person of ordinary skill in the art would appreciate that the main motivation for adopting copper interconnects in integrated circuits, namely, maintaining low-resistance connections despite ever-decreasing feature sizes, does not apply to selecting the material of the bonding pads of Wyland's semiconductor package. The applicants respectfully submit that this absence of a motivation to use copper, together with Moyer's disclosure of the additional difficulties of using copper, means that such person would have no motivation to adopt the teaching set forth in Moyer's disclosure with respect to the material of the bonding pads of Wyland's semiconductor package.

The applicants additionally submit that Moyer is non-analogous art and, hence, is not a valid reference with respect to the invention claimed in Claim 9. The invention claimed in Claim 9 relates to the structure of a packaging device for a semiconductor die. Moyer's disclosure relates to structures for the bonding pads of an integrated circuit having copper interconnects. The *Manual of Patent Classification* classifies Horiuchi's semiconductor device, which is analogous prior art, in class 257, subclass 690, whereas it classified Moyer's disclosure in class 438, subclass 612.

The official action asserts that col. 1, lines 41-43, of Moyer's disclosure provides more than sufficient motivation to use Moyer's copper contact pad in Wyland's semiconductor package. The applicants do not dispute that the cited passage of Moyer's disclosure teaches the desirability of using copper as an interconnect material in an integrated circuit. However, the portion of Wyland's semiconductor package the Examiner is proposing to modify is metallization 61 that forms part of the semiconductor package and is not part of semiconductor die 30. The applicants have been unable to find anything in Moyer's disclosure that teaches or suggests the desirability of making an element of a semiconductor package corresponding to

Wyland's metallization 61 of copper.

Moreover, the applicants respectfully submit that the portion of Moyer's disclosure cited in the official action quotes is taken out of the context of the discussion of the problems of using copper as an interconnect material in integrated circuits that immediately follows the cited passage. The applicants respectfully submit that this portion of Moyer's disclosure would discourage a person of ordinary skill in the art from using copper as the interconnect material of an integrated circuit absent the compelling reason of high-frequency performance. The applicants further submit that Moyer is silent with respect to the suitability of copper in applications such as Wyland's metallization 61, and that this would further discourage the person of ordinary skill in the art from making the modification proposed in the official action. Moreover, in view of the caveats uttered by Moyer about the problems of using copper, Moyer's disclosure as a whole cannot reasonably be regarded as providing the person of ordinary skill in the art with a reasonable expectation of success in the event such person were to attempt to perform the proposed modification of Wyland's semiconductor package. Finally, the applicants note that they have been unable to find anything in Wyland's disclosure that teaches or suggests that the performance of his semiconductor package is unsatisfactory at high frequencies. Such teaching might motivate the person of ordinary skill in the art to ignore Moyer's teaching with regard to the difficulties of using copper, but no such teaching or suggestion can be found.

The official action does not indicate where in the cited references may be found a teaching or suggestion that would provide a person of ordinary skill in the art with a reasonable expectation of success in the event such person were to undertake the modification of Wyland's semiconductor package proposed in the official action.

Additionally, the applicants submit that Wyland's semiconductor package, modified as proposed in the official action, would still lack a die mounting pad for the reason set forth above with reference to Claim 1. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claim 9.

The applicants therefore respectfully submit that the rejection of claim 9 is improper because the prima facie case of obviousness set forth in the official action does not meet the requirements set forth in MPEP § 2143. The applicants therefore respectfully request that the

rejection be withdrawn.

D. Claims 13 and 18

Claims 13 and 18 are rejected under 35 USC § 103(a) as being unpatentable over Horiuchi as applied to Claims 11, 12, 16, and 17 in view of *Electronic Packaging and Production* (the *Article*).

The official action indicates that Horuichi does not disclose a substrate material composed of epoxy laminate and looks to *Electronic Packaging and Production* for a disclosure of this material. The official action states:

> Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the disclosures of Electronic Packaging and Technology with Horuichi et al. to obtain a device with increased reliability and reduced fatigue at joints (p. 1, left column, 5th para.).

The disclosure of the Article is described above with reference to claims 3 and 8.

The applicants respectfully submit that structure of Horiuchi's device package is different that of the TSOPs discussed in the Article: in Horiuchi's device package, semiconductor die 10 is attached directly to the surface of substrate 5. The applicants respectfully submit that the person of ordinary skill in the art would appreciate that the thermal expansion considerations of Horiuchi's semiconductor device are so different from those of a TSOP attached to a printed circuit board that such person would consider any teaching set forth in the Article with respect to printed circuit board material as inapplicable to choosing the substrate material of Horiuchi's semiconductor device. Accordingly, the applicants respectfully submit that the rationale set forth in the official action for combining the cited references does not meet the requirements set forth in MPEP § 2143.

Additionally, the applicants respectfully submit that Horiuchi's semiconductor device, modified as proposed in the official action, would still lack "located on one of the major surfaces, a conductive die mounting pad dimensioned to accommodate the semiconductor die" and "in which the semiconductor die is mounted on the die mounting pad with a major surface thereof in contact with the mounting pad." for the reasons set forth above with reference to claim 11. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claims 13 and 18.

The official action does not indicate where in the cited references may be found a teaching or suggestion that would provide a person of ordinary skill in the art with a reasonable expectation of success in the event such person were to undertake the modification of Horiguchi's semiconductor device proposed in the official action.

Accordingly the applicants respectfully submit that the rejection of claims 13 and 18 is improper because the official action does not set forth a prima facie case of obviousness that complies with the requirements set forth in MPEP § 2143.

E. Claims 15 and 20

Claims 15 and 20 are rejected under 35 USC § 103(a) as being unpatentable over Horiuchi as applied to Claims 11, 12, 16, and 17 in view of Wilson.

The official action indicates that Horuichi does not disclose a conductive interconnecting element (via) comprising tungsten and looks to Wilson for a disclosure of this material. The official action states:

> It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Horuichi et al. to reduce costs (p. 868, lines 11-12) and reduce signal delays (p. 872, Figure 10).

For reasons corresponding to those described above with reference to Claims 5 and 10, the applicants respectfully submit that the rejection of claims 15 and 20 is improper because the prima facie case of obviousness set forth in the official action does not comply with the requirements set forth in MPEP § 2143. Specifically, the official action does not set forth a motivation that complies with the requirements set forth in MPEP § 2143, the official action does not indicate where in the cited references may be found a teaching or suggestion that would provide a person of ordinary skill in the art with a reasonable expectation of success in the event such person were to undertake the modification of Horiuchi's semiconductor device proposed in the official action and the proposed combination of references does not teach or suggest all the claim limitations.

F. Claim 19

Claim 19 is rejected under 35 USC § 103(a) as being unpatentable over Horuichi as

applied to Claims 11, 12, 16, and 17 in view of Moyer and Wyland.

The official action states that Horuichi does not disclose that the mounting pad, bond pad, and connecting pad are composed of copper and looks to Wyland for a teaching of a mounting pad and a connecting pad (63) composed of copper and looks to Moyer for a teaching of a copper contact (bond) pad (13) (Figure 1) formed on the silicon substrate for either wire bonding or solder bump bonding. The official action states:

> It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moyer et al. and Wyland with Horuichi et al. to provide a metallic contact structures of low cost and high conductivity (Moyer et al., col. 1, lines 41-43).

For reasons corresponding to those described above with reference to Claim 9, the applicants respectfully submit that the rejection of claim 19 is improper because the prima facie case of obviousness set forth in the official action does not comply with the requirements set forth in MPEP § 2143. Specifically, the official action does not set forth a motivation that complies with the requirements set forth in MPEP § 2143, the official action does not indicate where in the cited references may be found a teaching or suggestion that would provide a person of ordinary skill in the art with a reasonable expectation of success in the event such person were to undertake the modification of Horiuchi's semiconductor device proposed in the official action and the proposed combination of references does not teach or suggest all the claim limitations.

The applicants respectfully request that the amendments set forth above be entered and that Examiner reconsider the rejection of the rejected claims. The applicants believe that the application as now amended is in condition for allowance, and respectfully request such favorable action. If any matters remain outstanding in the application, the Examiner is respectfully invited to telephone the applicant attorney at (650) 485-3015 so that these matters may be resolved.

Respectfully submitted,

Kong Weng Lee et al.

By: _____

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Application or Docket Number: 10/608605

CLAIMS AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY FEE
BASIC FEE (37 CFR 1.16(a))				$____	OR		$____
TOTAL CLAIMS (37 CFR 1.16(c))	minus 20 =	*	X $____ =		OR	X $____ =	
INDEPENDENT CLAIMS (37 CFR 1.16(b))	minus 3 =	*	X $____ =		OR	X $____ =	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(d))			+ $____ =		OR	+ $____ =	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL		OR	TOTAL	

CLAIMS AS AMENDED – PART II

4/6/05

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
	Total (37 CFR 1.16(c))	* 20	Minus	** 20	= —	X $____ =		OR	X $____ =	
	Independent (37 CFR 1.16(b))	* 2	Minus	*** 3	= —	X $____ =		OR	X $____ =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $____ =		OR	+ $____ =	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
	Total (37 CFR 1.16(c))	*	Minus	**	=	X $____ =		OR	X $____ =	
	Independent (37 CFR 1.16(b))	*	Minus	***	=	X $____ =		OR	X $____ =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $____ =		OR	+ $____ =	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
	Total (37 CFR 1.16(c))	*	Minus	**	=	X $____ =		OR	X $____ =	
	Independent (37 CFR 1.16(b))	*	Minus	***	=	X $____ =		OR	X $____ =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $____ =		OR	+ $____ =	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
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Intellectual Property Administration
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Loveland, CO 80537-0599

EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/608,605	Applicant(s) LEE ET AL.	
	Examiner Thomas J. Magee	Art Unit 2811	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 08April 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-20*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: (See attached sheet).
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Item 3a) :

The proposed amendments to Claims 1, 6, 11, and 16 will not be entered because they raise new issues that would require further consideration and/or search.

Item 11 :

The request for reconsideration has been carefully considered, in terms of Arguments presented by Applicant relevant to Claim rejections, but these have not been found to be persuasive.

With regard to Claim 6, (pp. 6 – 7, Response) Applicant is correct in the contention that (31) is the bond pad element and (61) is an interconnecting structure. There was a mistype of numbers and (31) is correct, as stated in the earlier Non-Final action. Remaining remarks are addressed to an amendment, and as stated above, further consideration and/or search will be required.

With regard to Claim 11, (pp. 7 – 8, Response) the (unamended) claim recites, *"a bonding pad located on one of the major surfaces,"* and Figure 1 discloses (22) a bonding pad on one of the major surfaces (Col. 3, lines 41 – 47), such that the reference reads on the recited claim.

With regard to Claims 3 and 8 (pp.8 – 10, Response), it should be noted that the Office Action recites the referenced article as evidence that multilayer laminate boards are well known and widely used in the art, a fact to which Applicant concedes (p. 9). The contention by Applicant that it would not be obvious to use the multilayer laminate boards with Wyland is not correct.

Wyland discloses (Abstract) that the invention includes a thermally conductive foam to conduct heat away from the device. As such. It is both an intent and an objecttive in the invention of Wyland to reduce heating of the device (Col. 1, lines 16 – 29). The design and use of multilayer boards with interlayer (metal) layers has been routinely used and provides an avenue for additional dissipation (See, for example, Adam, Proc. IEEE Semi-Therm Symp., 1994) Hence, the use of multilayer boards in Wyland has more than adequate motivation for combining.

With regard to Claims 5, 10, 15, and 20, (pp.10 – 12, and 16, Response), attempts to place Wilson et al. into class 438 are not germane, since Wilson et al. is a textbook and a non-patent literature source. Further, the actual cost analysis of process steps is also not germane and beyond the purview of this Office Action. In regard to signal delay, Applicant has misread the Wilson et al. reference (p. 870). For "long" lines of increased width, as present in Wyland, the advantage is to tungsten. Hence, there is both advantage and motivation for modifying Wyland and including tungsten as the interconnect.

With regard to Claim 9 (pp. 12 – 14, Response), the advantages of using copper for contact bond pads (13) (Figure 1) in Moyer et al. is conceded by Applicant (p. 13). Since a solder layer (Col. 7, lines 19 – 21) is present on bond pad 31 in Wyland, the motivation for combining Wyland and Moyer et al.is clear, i.e., to improve solder bonding to the bond pad layer (Moyer et al., Col. 2, lines 19 – 21).Prima facie obviousness is indeed established. Contentions that

Moyer et al. is non-analagous art (p. 13) are not germane, since Moyer et al. is clearly disclosing within the semiconductor device/packaging area and is dislosing a "layered structure" (Col. 2, line 54).

With regard to Claims 13 and 18 (pp. 15 – 16, Response), Horiuchi et al. disclose that the substrate 5 is a "resinous substrate" (epoxy) (Col. 3, lines 50 – 51), but do not disclose that it Is a multilayer laminate structure. Since the Electronic Packaging and Production article is used to identify such structures as routine in the art, it is apparent that a multilayer board could be used in Horiuchi et al to improve reliability and heat flow, as discussed for Claims 3 and 8. Further, as mentioned for Item 3 above, the amended claims will require further search and consideration.

With regard to Claim 19 (pp. 16 – 17, Response), as discussed for Claim 9, the advantages of using copper for contact bond pads (13) (Figure 1) in Moyer et al. is conceded by Applicant (p. 13). Since a solder layer s present on bond pad in Horuichi et al., the motivation for combining Wyland and Moyer et al. is clear, i.e., to improve solder bonding to the bond pad layer (Moyer et al., Col. 2, lines 19 – 21). Prima facie obviousness is indeed established.

The article by J. Adams, "New Correlations Between Electrical Current and Temperature Rise in PCB Traces," is included herein only as a reference to support the response above.

Notice of References Cited	Application/Control No. 10/608,605	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner Thomas J. Magee	Art Unit 2811	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Johannes Adam, "New Correlations Between Electrical Current and Temperature Rise in PCB Traces," Proc. 20th IEEE Semi-Therm Symp., (March,2004), pp. 1-8.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P. O. Box 7599
Loveland, Colorado 80537-0599

ATTORNEY DOCKET NO. 70030259-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Kong Weng Lee, et al.

Serial No.: 10/608605 **Examiner:** Thomas J. Magee

Filing Date: June 27, 2003 **Group Art Unit:** 2811

Title: Packaging Device For Semiconductor Die, Semiconductor Device Incorporating Same And Method Of Making Same

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

REQUEST FOR CONTINUED EXAMINATION (RCE) 37 CFR 1.114

Subsection (b) of 35 U.S.C. 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995.
See The American Inventors Protection Act of 1999 (AIPA).

Sir:

This is a Request for Continued Examination (RCE) under CFR 1.114 of the above-identified application.

NOTE: 37 CFR 1.114 is effective on May 29, 2000. If the above application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under CFR 1.53(d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice, Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1233 off. Gaz. Pat. Office 47 (Apr.11, 2000), which Established RCE practice.

Submission under 37 CFR 1.114

☒ Previously submitted:
- ☒ Consider the amendment(s)/reply under 37 CFR 1.116 previously filed on April 6, 2005 (Any unentered amendment(s) referred to above will be entered).
- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on
- ☐ Other:

☐ Enclosed:
- ☐ Amendment/Reply
- ☐ Affidavit(s)/Declarations(s)
- ☐ Information Disclosure Statement (IDS)
- ☐ Other:

Miscellaneous

- ☐ Suspension of action is requested under 37 CFR 1.103(c) for a period of months. The fee for this Suspension is (37 CFR 1.17(i)) $130.00.
- ☐ Other:

06/22/2005 RFEKADU1 00000025 501078 10608605

01 FC:1251 120.00 DA
02 FC:1801 790.00 DA

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OIPE/IAP
JUN 2 2 2005

Rev 06/05 (RCE)

CONTINUED EXAMINATION TRANSMITTAL (RCE) (37 CFR 1.114) (continued)

ATTORNEY DOCKET NO. 70030259-01

RCE filing fee **$790.00**

☒ A Petition for Extension of Time

☒	One month	$120.00
☐	Two months	$450.00
☐	Three months	$1020.00
☐	Four months	$1590.00

Please charge to Deposit Account **50-1078** the sum of $910.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **50-1078** pursuant to 37 CFR 1.25.

A duplicate copy of this transmittal letter is enclosed.

☐ I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.

Date of Deposit:

OR

☒ I hereby certify that this paper is being facsimile transmitted to the Commissioner for Patents on the date shown below.

Date of Facsimile: June 21, 2005

Typed Name: Linda A. Iimura

Signature: Linda A Iimura

Respectfully submitted,
Kong Weng Lee, et al.

By

Ian Hardcastle
Attorney/Agent for Applicant(s)

Reg. No. 34,075

Date: June 21, 2005

Telephone No. 650 485 3015

Agilent Technologies Inc.
Legal Dept. DL429
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Loveland, Colorado 80537-0599

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Agilent Technologies
Innovating the HP Way

Facsimile

Date: June 21, 2005 **Fax number:** 703-872-9306

To: Examiner Thomas J. Magee **Total pages:** 3

From: Ian Hardcastle

Subject: US Patent Application 10/608,605
Attorney Docket: 70030259-1
Filed: June 27, 2003

Enclosed is the a Request for Continued Examination in response to the Advisory Action dated May 31, 2005.

Respectfully submitted,

Ian Hardcastle
Reg. No. 34,075

I hereby certify that this correspondence is being transmitted via facsimile to the Commissioner for Patents at (703) 872 9306 on 6 April 2005

By Linda A. Ilmura Date April 6, 2005
Linda A. Ilmura

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Enter Per RCE 6/21/05

In re Application of:

Inventor(s): Kong Weng Lee et al. Group Art Unit: 2811

Serial No.: 10/608,605 Examiner: Thomas J. Magee

Filed: 27 June 2003

Title: *Packaging Device for Semiconductor Die, Semiconductor Device Incorporating Same and Method of Making Same*

Atty Docket: 70030259

AMENDMENT UNDER 37 CFR § 1.116

Commissioner for Patents
P.O. Box 1450
Alexandria
VA 22313-1450

Sir:

In response to the Official Action dated 9 February 2005, the applicants respectfully request entry of the following amendments:

PTO/SB/06 (08-03)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number: 10/608605

CLAIMS AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY FEE
BASIC FEE (37 CFR 1.16(a))				$____	OR		$____
TOTAL CLAIMS (37 CFR 1.16(c))	minus 20 =	*	X $____ =		OR	X $____ =	
INDEPENDENT CLAIMS (37 CFR 1.16(b))	minus 3 =	*	X $____ =		OR	X $____ =	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(d))			+ $____ =		OR	+ $____ =	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL		OR	TOTAL	

CLAIMS AS AMENDED – PART II

4/6/05

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
	Total (37 CFR 1.16(c))	* 20	Minus	** 20	= —	X $____ =		OR	X $____ =	
	Independent (37 CFR 1.16(b))	* 2	Minus	*** 3	= —	X $____ =		OR	X $____ =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $____ =		OR	+ $____ =	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

6/21/05

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
	Total (37 CFR 1.16(c))	* 20	Minus	** 20	=	X $____ =		OR	X $____ =	
	Independent (37 CFR 1.16(b))	* 2	Minus	*** 3	=	X $____ =		OR	X $____ =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $____ =		OR	+ $____ =	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
	Total (37 CFR 1.16(c))	*	Minus	**	=	X $____ =		OR	X $____ =	
	Independent (37 CFR 1.16(b))	*	Minus	***	=	X $____ =		OR	X $____ =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $____ =		OR	+ $____ =	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P. O. Box 7599
Loveland, Colorado 80537-0599

ATTORNEY DOCKET NO. 70030259-01

Fee Only

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Kong Weng Lee, et al.

Serial No.: 10/608605 **Examiner:** Thomas J. Magee

Filing Date: June 27, 2003 **Group Art Unit:** 2811

Title: Packaging Device For Semiconductor Die, Semiconductor Device Incorporating Same And Method Of Making Same

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

REQUEST FOR CONTINUED EXAMINATION (RCE) 37 CFR 1.114

Subsection (b) of 35 U.S.C. 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995.
See The American Inventors Protection Act of 1999 (AIPA).

Sir:

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NOTE: 37 CFR 1.114 is effective on May 29, 2000. If the above application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under CFR 1.53(d) (FITCH/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice, Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1223 off. Gaz. Pat. Office 47 (Apr. 11, 2000), which Established RCE practice.

Submission under 37 CFR 1.114

☒ Previously submitted:
- ☒ Consider the amendment(s)/reply under 37 CFR 1.116 previously filed on April 6, 2005 (Any unentered amendment(s) referred to above will be entered).
- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on
- ☐ Other:

☐ Enclosed:
- ☐ Amendment/Reply
- ☐ Affidavit(s)/Declarations(s)
- ☐ Information Disclosure Statement (IDS)
- ☐ Other:

Miscellaneous

- ☐ Suspension of action is requested under 37 CFR 1.103(c) for a period of months. The fee for this Suspension is (37 CFR 1.17(i)) $130.00.
- ☐ Other:

06/22/2005 RFEKADU1 00000025 501078 10608605
01 FC:1251 120.00 DA
02 FC:1801 790.00 DA

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JUN 22 2005

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	("5986885").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 10:22
S2	2	("6084295").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 10:25
S3	312	die same (mounting adj pad)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/08 10:26
S4	985	(die chip) same (mounting adj pad)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/08 10:26
S5	372	(die chip) same (mounting adj pad) same substrate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/08 10:27
S6	6	(("5986885") or ("6084295") or ("6620720")).PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/22 12:01
S7	2226	(die chip IC) same (mount$3 with pad) same interconnect$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/22 14:02
S8	7479	(die chip IC) same (bond$3 with pad) same interconnect$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/22 14:02
S9	2123	(die chip IC) same (bond$3 with pad) same interconnect$3 same (hole via)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/22 14:38
S10	2	("6191477").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/22 14:38

S11	7	("5506755" | "5640048" | "5646826" | "5721454" | "5808873" | "5923084" | "6097089").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/22 14:57
S12	13	("3568000" | "3582865" | "3739469" | "4535385" | "4739448" | "4866841" | "5010641" | "5102829" | "5264729" | "5291062" | "5355283" | "5397917" | "5468999").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/22 15:00
S13	2	("4739448" | "4855537").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/22 15:02

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	06/27/2003	Kong Weng Lee	70030259-1	2253

7590 09/27/2005

AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, CO 80537-0599

EXAMINER	
OWENS, DOUGLAS W	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/608,605	LEE ET AL.	
	Examiner	Art Unit	
	Douglas W. Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 6/21/05.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 21, 2005 has been entered.

Claim Objections

2. Claims 1 – 10 are objected to because of the following informalities: in line 7 of claim 1, --of the substrate-- should be inserted after "surfaces", since a major surface of the die is also referenced in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 6, 7, 11, 12, 16 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,268,654 to Glenn et al.

Regarding claims 1 and 11, Glenn et al. teach a packaging device for a semiconductor die, (Fig. 5) comprising:

a substantially planar substrate (200) having opposed major surfaces;

a conductive die mounting pad (222) dimensioned to accommodate the die (100), the pad being located on one of the major surfaces, and in contact with a major surface of the die;

a conductive connecting pad (221) located on the other of the major surfaces of the substrate; and

a conductive interconnecting element (220) extending through the substrate and electrically interconnecting the mounting pad and the connecting pad.

Regarding claims 2, 7, 12 and 18, Glenn et al. teach a device, in which the substrate comprises ceramic (Col. 5, lines 19 – 27).

Regarding claims 6 and 16, Glenn et al. teach a device, further comprising:

a bonding pad (204) smaller in area than the die mounting pad, the bonding pad located on the one of the major surfaces;

an additional conductive connecting pad (209) located on the other of the major surfaces; and

an additional conductive interconnecting element (203) extending through the substrate and electrically interconnecting the bonding pad and the additional connecting pad.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4, 5, 9, 14, 15, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al.

Regarding claims 4, 9, 14 and 19, Glenn et al. teach a device, wherein the mounting pad comprises one of copper and gold (Col. 12, lines 40 – 44). Glenn et al. do not teach forming the connecting pad and the bonding pad to comprise copper, silver, gold, nickel or tungsten. Copper, silver, gold, nickel and tungsten are well known materials that are well suited for the intended use. It would have been obvious to one of ordinary skill in the art to use the cited materials, since it is desirable to use materials that are known and suited for the intended use. The selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945).

Regarding claims 5, 10, 15 and 20, Glenn et al. do not teach that the conductive interconnecting element comprises tungsten. Tungsten is a known material that is well suited for use in an interconnecting element. It would have been obvious to one of ordinary skill in the art to use tungsten for the interconnect since it is a known material that is well suited for the intended use.

7. Claims 3, 8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al. as applied to claims 1, 6 and 11 above, and further in view of US Patent No. 6,191,477 to Hashemi.

Glenn et al. do not teach a device, wherein the substrate is an epoxy laminate or silicon. Hashemi teaches a device, wherein the substrate is an epoxy laminate (Col. 3,

lines 1 – 7). It would have been obvious to one of ordinary skill in the art at the time the invention was made, to incorporate the teaching of Hashemi into the device taught by Glenn et al., since it is desirable to use materials that known and well suited for the intended use.

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al. as applied to claim 16 above, and further in view of US Patent No. 6,084,295 to Horiuchi et al.

Glenn et al. do not teach a device further comprising an encapsulant encapsulating the semiconductor die and at least a portion of the major surface of the substrate on which the mounting pad is located. Horiuchi et al. teach an encapsulant encapsulating the semiconductor die and at least a portion of the major surface of the substrate on which the mounting pad is located. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Horiuchi et al. into the device taught by Glenn et al. since it desirable to protect the device from the elements.

Response to Arguments

9. Applicant's arguments with respect to claims 1 – 20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven H. Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Douglas W Owens
Examiner
Art Unit 2811

DWO

Notice of References Cited	Application/Control No. 10/608,605	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner Douglas W. Owens	Art Unit 2811	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,191,477	02-2001	Hashemi, Hassan S.	257/706
	B	US-6,268,654	07-2001	Glenn et al.	257/704
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/608,605	LEE ET AL.
Examiner	**Art Unit**
Douglas W. Owens	2811

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date								
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Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/608,605	LEE ET AL.	
	Examiner	Art Unit	
	Douglas W. Owens	2811	

SEARCHED			
Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST text search	9/22/2005	DWO

AVAGO TECHNOLOGIES, INC.
P.O. Box 1920
Denver, Colorado 80201-1920

ATTORNEY DOCKET NO. 70030259-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Kong Weng Lee et al.

Serial No.: 10/608,605 **Examiner:** Owens, Douglas W

Filing Date: June 27, 2003 **Group Art Unit:** 2811

Title: Packaging Device for Semiconductor Die, Semiconductor Device Incorporating Same and Method of Making Same

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

☒ Response/Amendment ☐ Petition to extend time to respond

☒ New fee as calculated below ☐ Supplemental Declaration

☐ No additional fee (Address envelope to "Mail Stop Amendments")

☐ Other: (Fee $_____)

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	21	MINUS	20	= 1	X 50	$ 50
INDEP. CLAIMS	3	MINUS	3	= 0	X 200	$ 0
☐ FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ 360	$ 0
EXTENSION FEE	1ST MONTH 120.00 ☐	2ND MONTH 450.00 ☐	3RD MONTH 1020.00 ☐	4TH MONTH 1590.00 ☐		$ 0
					OTHER FEES	$ 0
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	$ 50

Charge $ 50 to Deposit Account **50-3718**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3718** pursuant to 37 CFR 1.2 5. Additionally please charge any fees to Deposit Account **50-3718** under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this transmittal letter is enclosed.

Respectfully submitted,
Kong Weng Lee et al.

By _____
P. S. Dara
Attorney/Agent for Applicant(s)

Reg. No. 52,793

Date: 12/23/2005

Telephone No. (404) 610-5689

I hereby certify that this correspondence is being Deposited with the United States Postal Service as First class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: 12/23/2005

Typed Name: P. S. Dara

Signature: _____

Rev 10/04 (TransAmd)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Kong Weng Lee

Serial No.: 10/608,605

Filed: 6/27/2003

Confirmation No.: 2253

Group Art Unit: 2811

Examiner: Owens, Douglas W

Docket No. 70030259-1

For: **Packaging Device for Semiconductor Die, Semiconductor Device Incorporating Same and Method of Making Same**

AMENDMENT AND RESPONSE

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

The outstanding non-final Office Action mailed September 27, 2005 has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

AUTHORIZATION TO DEBIT ACCOUNT

It is not believed that extensions of time or fees for net addition of claims are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to Avago deposit account no. 50-3718.

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AMENDMENTS TO THE CLAIMS

Please amend the present application as follows:

Claims

1. (Currently amended) A packaging device for a semiconductor die, the packaging device comprising:

a substantially planar substrate having opposed major surfaces;

~~located on one of the major surfaces; a~~ an electrically conductive die mounting pad located on one of the major surfaces of the substrate, the conductive die mounting pad dimensioned to accommodate the die with a major surface of the die in contact therewith;

a first electrically conductive connecting pad located on the other of the major surfaces of the substrate, the first electrically conductive connecting pad dimensioned to conform to an industry standard pad layout of a printed circuit board; ~~and~~

a first electrically conductive interconnecting element extending through the substrate and electrically interconnecting the mounting pad and the first electrically conductive connecting pad;

an electrically conductive bonding pad located on the one of the major surfaces of the susbtrate;

a second electrically conductive connecting pad located on the other of the major surfaces of the susbtrate; and

a second electrically conductive interconnecting element extending through the substrate and electrically interconnecting the bonding pad and the second electrically conducting connecting pad.

2. (Currently amended) The packaging device of claim 1, in which the substrate comprises one of a ceramic material and a material selected from epoxy laminate and silicon.

3. (Canceled)

4. (Currently amended) The packaging device of claim 1, in which the mounting pad and the first electrically conductive connecting pad each comprise at least one of copper, silver, gold, nickel and tungsten.

5. (Currently amended) The packaging device of claim 1, in which the first electrically conductive interconnecting element comprises tungsten.

6- 10. (Canceled)

11. (Currently amended) A semiconductor device, comprising:

a semiconductor die comprising metallization on at least a portion of a bottom surface of the die;

a substantially planar substrate having opposed major surfaces;

located on one of the major surfaces, a conductive die mounting pad dimensioned to accommodate the semiconductor die;

a conductive connecting pad located on the other of the major surfaces; and

a conductive interconnecting element extending through the substrate and electrically interconnecting the mounting pad and the connecting pad;

in which the semiconductor die is mounted on the die mounting pad whereby an electrical connection is formed between the metallization on the at least a portion of the bottom surface of the die and ~~with a major surface thereof in contact with~~ the mounting pad.

12. (Original) The semiconductor device of claim 11, in which the substrate comprises ceramic.

13. (Original) The semiconductor device of claim 11, in which the substrate comprises a material selected from epoxy laminate and silicon.

14. (Original) The semiconductor device of claim 11, in which the mounting pad and the connecting pad each comprise at least one of copper, silver, gold, nickel and tungsten.

15. (Original) The semiconductor device of claim 11, in which the conductive interconnecting element comprises tungsten.

16. (Currently amended) The semiconductor device of claim 11, additionally comprising:

a conductive bonding pad smaller in area than the die mounting pad, the bonding pad

located on the one of the major surfaces;

an additional conductive connecting pad located on the other of the major surfaces;

an additional conductive interconnecting element extending through the substrate and electrically interconnecting the bonding pad and the additional connecting pad~~, and~~;

the semiconductor die additonally comprising metallization on at least a portion of a top surface of the die; and

a bonding wire extending between the metallization on the at least a portion of the top surface of the semiconductor die and the bonding pad.

17. (Original) The semiconductor device of claim 16, additionally comprising an encapsulant encapsulating the semiconductor die and at least a portion of the major surface of the substrate on which the mounting pad is located.

18. (Original) The semiconductor device of claim 16, in which the substrate comprises a material selected from ceramic, epoxy laminate and silicon.

19. (Original) The semiconductor device of claim 16, in which the mounting pad, the bonding pad and the connecting pads each comprise at least one of copper, silver, gold, nickel and tungsten.

20. (Original) The semiconductor device of claim 16, in which the conductive interconnecting element comprises tungsten.

21. (New) A semiconductor device, comprising:

a substantially planar substrate having opposed major surfaces;

an electrically conductive mounting pad located on one of the major surfaces of the substrate;

a semiconductor die having a metallized bottom major surface that is mounted on the electrically conductive mounting pad;

a first electrically conductive connecting pad located on the other of the major surfaces of the substrate; and

a first electrically conductive interconnecting element extending through the substrate and electrically interconnecting the mounting pad and the first electrically conductive connecting pad.

22. (New) The semiconductor device of claim 21 wherein the semiconductor die comprises a light emitting diode (LED) and the metallized bottom major surface comprises one of an anode and a cathode of the LED.

23. (New) The semiconductor device of claim 21, further comprising:

an electrically conductive bonding pad located on the one of the major surfaces of the substrate;

a bonding wire extending between a metallized top major surface of the semiconductor die and the electrically conductive bonding pad;

a second electrically conductive connecting pad located on the other of the major surfaces of the substrate; and

a second electrically conductive interconnecting element extending through the substrate and electrically interconnecting the bonding pad and the second connecting pad.

24. (New) The semiconductor device of claim 23 wherein the semiconductor die comprises a light emitting diode (LED), the metallized top major surface comprises a first electrode of the LED and the metallized bottom major surface comprises a second electrode of the LED.

25. (New) The semiconductor device of claim 21 wherein the first electrically conductive interconnecting element is selected to withstand an operating temperature when the semiconductor die is mounted on the electrically conductive mounting pad and to provide a low-resistance electrical connection between the mounting pad and the first electrically conductive connecting pad.

26. (New) The semiconductor device of claim 25, wherein the first electrically conductive interconnecting element comprises tungsten.

27. (New) The semiconductor device of claim 25, wherein the first electrically conductive interconnecting element comprises a slug of electrically conductive material, the slug having a diameter selected to press-fit the slug into a through hole located in the substrate between the mounting pad and the first electrically conductive connecting pad.

REMARKS

This is a full and timely response to the non-final Office Action mailed September 27, 2005. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Present Status of Patent Application

Upon entry of the amendments in this response, claims 1-2, 4-5, and 11-27 remain pending in the present application. More specifically, claims 21-27 have been newly submitted with no new material being added; claims 1, 2, 4, 5, 11, and 16 have been currently amended with no introduction of new matter; and claims 3 and 6-10 have been canceled. Applicants have canceled these claims merely to reduce the number of disputed issues and to facilitate early allowance and issuance of other claims in the present application. Applicants reserve the right to pursue the subject matter of these claims in a continuing application, if Applicants so choose, and do not intend to dedicate the canceled subject matter to the public. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

A. Claim Objections

Statement of the Objection

Claims 1-10 are objected to because of the following informalities: in line 7 of claim 1, -- of the substrate -- should be inserted after "surfaces", since a major surface of the die is also referenced in the claim. Appropriate correction is required.

Response to the Objection

Claim 1 has been appropriately amended as per the Office Action recommendation. Since the objection has been overcome, Applicants respectfully request allowance of claim 1 as well as the corresponding dependent Claims 2, 4, and 5 that are currently pending. Claims 3 and 6-10 have been canceled.

B. Claim Rejections under 35 U.S.C. §102(b)

Statement of the Rejection

Claims 1, 2, 6, 7, 11, 12, 16 and 18 are rejected under 35 U.S.C. §102(b) as being anticipated by US Patent No. 6,268,654 to Glenn et al.

Response to the Rejection

A proper rejection under 35 U.S.C. §102(b) requires that a single prior art reference

disclose each element of the claim. Furthermore, anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference.

Applicants respectfully assert that claims 1, 2, 6, 7, 11, 12, 16 and 18 are now in condition for allowance. Further remarks elaborating on Applicant's assertion have been provided below for each of the rejected claims.

Claim 1

The Office Action asserts that Glenn et al. anticipates Applicant's Claim 1. However, in doing so, the Office Action has improperly asserted that certain elements of Glenn et al. anticipate allegedly equivalent elements of Applicants' Claim 1. Specifically, attention is drawn to page 3, lines 6-7 of the Office Action ("a conductive interconnecting element (220) extending through the substrate and electrically interconnecting the mounting pad and the connecting pad"), which alleges that Glenn's *thermal* via 220 anticipates Applicants' conductive interconnecting element 120 that *electrically* interconnects Applicants' mounting pad 130 and connecting pad 140 (FIG. 1B to be used for Applicants' reference designators).

To the contrary, Applicants respectfully assert that Glenn's mounting pad and connecting pad are *not* electrically interconnected by thermal via 220. Applicants' assertion is based on Glenns' col. 12 lines 63-67, reproduced below for easy reference:

> Substrate 200 includes *thermal vias 220*, which extend through substrate 200 and *conduct heat* from upper surface 201 to lower surface 202 of substrate 200. *By contrast, conductive vias 203* of substrate 200 *conduct electrical* signals to and from die 100. (Emphasis added)

This aspect is described further in Glenns' col. 13, lines 7-27 reproduced below for easy reference:

> Heat sink metallization 221 is formed on lower surface 202 of substrate 200. Thermal vias 220 connect metal die pad 222 to heat sink metalization 221. Accordingly, *heat generated by die 100 is conducted from lower surface 102 of die 100 to die pad 222 to thermal vias 220 and thereby to heat sink metalization 221*. Heat sink metalization 221 may be formed on lower surface 202 of substrate 200 by the same conventional masking and etching process used to form metalizations 204 and 209, as described above. The size and shape of heat sink metallization 221 may vary, depending on the application. For example, heat sink metalization 221 may be square or rectangular in shape and may be the same area as die 100. As is conventionally known, metal solder may be used to thermally connect heat sink metalization 221 to a printed circuit board to dissipate heat from package 12.
>
> Package 12 includes electrical conductors formed on upper surface 201 and lower surface 202 of substrate 200. These electrical conductors include metalizations 204 formed on upper surface 201 and metalizations 209 formed on lower surface 202 of substrate 200. *Metalizations 204 and 209 are electrically connected to vias 203*. Although not shown in FIG. 5, conductive contacts similar to contacts 207 and 209 of

FIG. 1 are formed on the ends of metalization 204 and 209, respectively. (Emphasis added)

As described above and illustrated in his FIG. 5, Glenn has made a clear distinction between a *thermal via 220* and an *electrically conductive via 203* and does not provide any indication or suggestion that the thermal via 220 may be used for electrical conduction.

However, in the interests of further clarifying the scope of the invention, Applicants have currently amended Claim 1 to include language that explicitly describes certain aspects related to connecting pad 140. This language includes the "electrically conductive connecting pad dimensioned to conform to an industry standard pad layout of a printed circuit board." Glenn does not disclose such an industry standard pad layout for his heat sink metallization 221 (the alleged equivalent to Applicants' connecting pad 140) because the primary purpose of his heat sink metallization 221 is to dissipate heat rather than to provide electrical conduction.

Applicants have further amended Claim 1 to include certain other elements, such as bonding pad 132, second connecting pad 142 and second interconnecting element 122, in addition to die mounting pad 130.

For at least the reasons described above, Applicants respectfully assert that the rejection of Claim 1 under 35 U.S.C. 102(b) is improper and hereby request withdrawal of the rejection followed by allowance of Claim 1.

Claim 2

Because Claim 1 is allowable, Claim 2 that depends directly or indirectly on Claim 1 is also allowable as a matter of law. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Applicants respectfully request withdrawal of the rejection, followed by allowance of Claim 2.

Claims 6-7

Claims 6 and 7 have been canceled thereby rendering moot the rejection of these claims.

Claim 11

Applicants' currently amended Claim 11 includes a semiconductor device "in which the semiconductor die is mounted on the die mounting pad whereby *an electrical connection* is formed between the metallization on the at least a portion of the bottom surface of the die and the mounting pad." The die mounting pad uses an interconnecting element that "electrically" interconnects the die mounting pad to a connecting pad located on the underside of the substrate.

The cited prior art of Glenn discloses "*thermal vias 220* that extend through substrate 200 and *conduct heat* from upper surface 201 to lower surface 202 of substrate 200," but fails to

disclose an electrical connection as described in Applicants' currently amended Claim 11. Consequently, Applicants respectfully assert that Claim 11 is allowable and hereby request withdrawal of the rejection followed by allowance of Claim 11.

Claims 12, 16 and 18

Because Claim 11 is allowable, Claims 12, 16 and 18 that depend directly or indirectly on Claim 11 is also allowable as a matter of law. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Applicants respectfully request withdrawal of the rejection, followed by allowance of Claim 12, 16 and 18.

C. Claim Rejections under 35 U.S.C. §103(a)

Statement of the Rejection

Claims 4, 5, 9, 14, 15, 19 and 20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al.

Response to the Rejection

Applicants respectfully request withdrawal of the rejection of claims 4, 5, 9, 14, 15, 19 and 20 for at least the reason that the rejection does not satisfy the requirements of MPEP § 2143.03, which states in pertinent part: "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)."

Specifically, claims 4, 5, 9, 14, 15, 19 and 20 are nonobvious as each of them is a dependent claim. Each of the corresponding independent claims have not been rejected under 35 U.S.C. 103(a). Hence, Applicants respectfully assert that claims 4, 5, 9, 14, 15, 19 and 20 cannot be properly rejected under 35 U.S.C. 103(a), and hereby request withdrawal of the rejection followed by allowance of claims 4, 5, 9, 14, 15, 19 and 20.

Additionally, the MPEP provides several guidelines for rejecting a claim under 35 U.S.C. 103(a). Specifically, reference is made to MPEP 706.2(j) *Contents of a 35 U.S.C. 103 Rejection*, which states in pertinent part:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947

F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP § 2143 - § 2143.03 for decisions pertinent to each of these criteria.
(Emphasis added)

Comments related to MPEP 706.2(j) are presented below.

Claims 4 and 5

Claims 4 and 5 are each directly dependent on Claim 1 and therefore all the elements of Claim 1 are included in Claims 4 and 5 via the dependency. The cited prior art reference, Glenn et al, does not teach or suggest all the claim limitations of each of Applicants' Claims 4 and 5 at least because of the dependency of these claims to independent Claim 1. Glenn et al does not at least teach or suggest "a first *electrically conductive interconnecting element* extending through the substrate and *electrically interconnecting the mounting pad and the first electrically conductive connecting pad*," which is a part of Applicants' Claim 1.

Consequently, Applicants respectfully assert that a rejection under 35 U.S.C 103(a) would be improper because a *prima facie* case of obviousness cannot be established for at least the reason mentioned above.

Applicants respectfully request withdrawal of the rejection followed by allowance of Claims 4 and 5.

Claim 9

Claim 9 has been canceled thereby rendering moot the rejection of Claim 9.

Claims 14, 15, 19 and 20

Claims 14, 15, 19 and 20 are each dependent, directly or indirectly, on Claim 11 and therefore all the elements of Claim 11 are included in Claims 14, 15, 19 and 20 via the dependency. The cited prior art reference, Glenn et al, does not teach or suggest all the claim limitations of each of Applicants' Claims 14, 15, 19 and 20. Glenn et al does not at least teach or suggest a semiconductor device "in which the semiconductor die is mounted on the die mounting pad whereby *an electrical connection* is formed between the metallization on the at least a portion of the bottom surface of the die and the mounting pad," which is a part of Applicants' Claim 11.

Consequently, Applicants respectfully assert that a rejection under 35 U.S.C 103(a) would be improper because a *prima facie* case of obviousness cannot be established for at least the reason mentioned above.

Applicants respectfully request withdrawal of the rejection followed by allowance of Claims 14, 15, 19 and 20.

D. Claim Rejections under 35 U.S.C. §103(a)

Statement of the Rejection

Claims 3, 8 and 13 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al. as applied to claims 1, 6 and 11 above, and further in view of US Patent No. 6,191,477 to Hashemi.

Response to the Rejection

In light of MPEP § 2143.03 described above, Applicants respectfully assert that dependent claims 3, 8 and 13 cannot be properly rejected under 35 U.S.C. 103(a), and hereby request withdrawal of the rejection followed by allowance of claims 3, 8 and 13. Additional arguments with reference to MPEP 706.2(j) *Contents of a 35 U.S.C. 103 Rejection* are presented below.

Claims 3 and 8

Claims 3 and 8 have been canceled thereby rendering moot the rejection of these claims.

Claim 13

Claim 13 depends directly on Claim 11 and therefore all the elements of Claim 11 are included in Claim 13 via the dependency. The cited prior art combination of Glenn et al. and Hashemi, does not teach or suggest all the claim limitations of Applicants' Claim 13. The combination does not at least teach or suggest "a first *electrically conductive interconnecting element* extending through the substrate and *electrically interconnecting the mounting pad and the first electrically conductive connecting pad*," which is a part of Applicants' Claim 11.

Consequently, for at least this reason, Applicants respectfully assert that a rejection of Claim 13 under 35 U.S.C. 103(a) would be improper and hereby request withdrawal of the rejection followed by allowance of Claim 13.

E. Claim Rejections under 35 U.S.C. §103(a)

Statement of the Rejection

Claim 17 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al. as applied to claim 16 above, and further in view of US Patent No. 6,084,295 to Horiuchi et al.

Response to the Rejection

In light of MPEP § 2143.03 described above, Applicants respectfully assert that dependent claim 17 cannot be properly rejected under 35 U.S.C. 103(a) and hereby request withdrawal of the rejection followed by allowance of claim 17. Additional arguments with reference to MPEP 706.2(j) *Contents of a 35 U.S.C. 103 Rejection* are presented below.

Claim 17

Claim 17 depends indirectly on Claim 11 and therefore all the elements of Claim 11 are included in Claim 17 via the dependency. The cited prior art combination of Glenn et al. and Horiuchi et al, does not teach or suggest all the claim limitations of Applicants' Claim 17. The combination does not at least teach or suggest "a first *electrically conductive interconnecting element* extending through the substrate and *electrically interconnecting the mounting pad and the first electrically conductive connecting pad*," which is a part of Applicants' Claim 11.

Consequently, for at least this reason, Applicants respectfully assert that a rejection of Claim 17 under 35 U.S.C. 103(a) would be improper and hereby request withdrawal of the rejection followed by allowance of Claim 17.

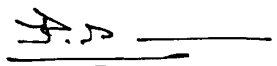
Prior Art Made of Record

The prior art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that claims 1-2, 4-5, and 11-27 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned representative at (404) 610-5689.

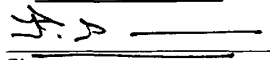
Respectfully submitted,



P. S. Dara
Reg. No. 52,793

P. S. Dara
7115 Threadstone Overlook
Duluth, GA 30097
(404)-610-5689

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA, 22313-1450, on **December 23, 2005**



Signature
Name: P. S. Dara

...persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number 10/608,605

CLAIMS AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY FEE
BASIC FEE (37 CFR 1.16(a))				$	OR		$
TOTAL CLAIMS (37 CFR 1.16(c))	minus 20 =	*	x $ =		OR	x $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(b))	minus 3 =	*	x $ =		OR	x $ =	
[illegible]						x $ =	
* If the difference in column 1 is less than zero, enter "0" in column 2			TOTAL		OR	TOTAL	

CLAIMS AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
AMENDMENT A	Total (37 CFR 1.16(i))	21	Minus	20	1	x $ =		OR	50	50
	Independent (37 CFR 1.16(h))	3	Minus	3	—	x $ =		OR	x $ =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+ $ =		OR	+ $ =	
						TOTAL ADDIT FEE		OR	TOTAL ADDIT FEE	50
AMENDMENT B	Total (37 CFR 1.16(i))		Minus			x $ =		OR	x $ =	
	Independent (37 CFR 1.16(h))		Minus			x $ =		OR	x $ =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+ $ =		OR	+ $ =	
						TOTAL ADDIT FEE		OR	TOTAL ADDIT FEE	
AMENDMENT C	Total (37 CFR 1.16(i))		Minus			x $ =		OR	x $ =	
	Independent (37 CFR 1.16(h))		Minus			x $ =		OR	x $ =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+ $ =		OR	+ $ =	
						TOTAL ADDIT FEE		OR	TOTAL ADDIT FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found either in this space or in any prior amendment.

[illegible]

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	06/27/2003	Kong Weng Lee	70030259-1	2253

57299 7590 04/06/2006

AVAGO TECHNOLOGIES, LTD.
P.O. BOX 1920
DENVER, CO 80201-1920

EXAMINER	
OWENS, DOUGLAS W	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,605	LEE ET AL.	
	Examiner	Art Unit	
	Douglas W. Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5 and 11-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,11-21,23 and 25-27* is/are rejected.

7)☒ Claim(s) *22,24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: in line 16 of the claim "susbtrate" should be replaced with --substrate--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,640,048 to Selna.

Regarding claim 1, Selna teaches a packaging device for a semiconductor die (Fig. 1), the packaging device comprising:

a substantially planar substrate (4) with opposed major surfaces;

an electrically conductive die mounting pad (8C) located on one of the major surfaces of the substrate, the conductive die mounting pad dimensioned to accommodate the die (12) with a major surface of the die in contact therewith;

a first electrically conductive connecting pad (10C) on the other of the major surfaces of the substrate, the first electrically conductive connecting pad dimensioned to conform to an industry standard pad layout of a printed circuit board;

a first electrically conductive interconnecting element (6C) extending through the substrate and electrically interconnecting the mounting pad and the first electrically conductive connecting pad;

an electrically conductive bonding pad (8A) located on the one of the major surfaces of the substrate;

a second electrically conductive pad (10A) located on the other of the major surfaces of the substrate; and

a second electrically conductive interconnecting element (6A) extending through the substrate and electrically interconnecting the bonding pad and the second electrically conducting connecting pad.

Regarding claim 2, Selna teaches a packaging device, wherein the substrate comprises an epoxy laminate (Col 2, lines 38 – 42).

Regarding claim 4, Selna teaches a packaging device, wherein the mounting pad and the first electrically conductive connecting pad comprise copper (Col. 1, lines 37 – 42).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5 and 11 – 21, 23, 25 – 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Selna.

Regarding claim 5, Selna does not teach using tungsten for the first conductive interconnecting element. Tungsten is a known material that is well suited for use in interconnecting elements. It would have been obvious to one having ordinary skill in the art to select tungsten, since it is a known metal that is well suited for the intended use.

Regarding claims 11 and 21, Selna teaches a semiconductor device, comprising:

semiconductor die including pinouts (Col. 1, lines 17 – 20) on a portion of a bottom surface of the die;

a substantially planar substrate (4) having opposed major surfaces;

a conductive die mounting pad (8C) located on one of the major surfaces, wherein the conductive die mounting pad is dimensioned to accommodate the semiconductor die;

a conductive connecting pad (10C) located on the other of the major surfaces;

a conductive interconnecting element (6C) extending through the substrate and electrically interconnecting the mounting pad and the connecting pad; and

wherein the semiconductor die is mounted on the die mounting pad and an electrical connection is formed between the die pads and the mounting pad.

Selna does not teach that the pinouts on the die comprise a metal. Selna is silent with respect to the pinout material. It would have been obvious to one of ordinary skill in the art to select metal for the pinout material (metallization on a bottom portion), since metal is a known material that is well suited for the intended use. The selection of a known material based on its suitability for its intended use supported a *prima facie*

obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945).

Regarding claims 13 and 18, Selna teaches a packaging device, wherein the substrate comprises an epoxy laminate (Col 2, lines 38 – 42).

Regarding claim 14, Selna teaches a packaging device, wherein the mounting pad and the first electrically conductive connecting pad comprise copper (Col. 1, lines 37 – 42).

Regarding claims 15, 20 and 26, Selna does not teach using tungsten for the conductive interconnecting element. Tungsten is a known material that is well suited for use in interconnecting elements. It would have been obvious to one having ordinary skill in the art to select tungsten, since it is a known metal that is well suited for the intended use.

Regarding claims 16 and 23, Selna teaches a semiconductor device, further comprising:

a conductive bonding pad (8A) smaller in area than the die mounting pad, the bonding pad located on the one of the major surfaces;

an additional conductive connecting pad (10A) located on the other of the major surfaces;

an additional conductive interconnecting element (6A) extending through the substrate and electrically interconnecting the bonding pad and the additional connecting pad;

the semiconductor die additionally comprising pads on the die (Col. 2, lines 3 – 6); and

a bonding wire (22) extending between the die pad and the bonding pad.

Selna does not teach that the die pads on the die comprise a metal. Selna is silent with respect to the die pad material. It would have been obvious to one of ordinary skill in the art to select metal for the die pad material (metallization on a bottom portion), since metal is a known material that is well suited for the intended use. The selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945).

Regarding claim 17, Selna teaches a semiconductor device, further comprising an encapsulant (16) encapsulating the semiconductor die and a portion of the major surface of the substrate on which the mounting pad is located.

Regarding claim 19, Selna teaches a semiconductor device, wherein the mounting pad, the bonding pad and the connecting pads each comprise copper.

Regarding claim 25, Selna teaches a semiconductor device, wherein the first electrically conductive interconnecting element is selected to withstand an operating temperature when the semiconductor die is mounted on the electrically conductive mounting pad and to provide a low-resistance electrical connection between the mounting pad and the first electrically conductive connecting pad.

Regarding claim 27, Selna teaches a semiconductor device, wherein the first electrically conductive interconnecting element comprises a slug of electrically

conductive material, the slug having a diameter selected to fit into a through hole in the substrate between the mounting pad and the first electrically conductive connecting pad. Selna does not teach that the slug is selected to press-fit into the through hole. This is considered a product-by-process limitation. "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Selna as applied to claim 11 above, and further in view of US Patent No. 6,268,654 to Glenn et al.

Selna does not teach a semiconductor device, wherein the substrate comprises ceramic. Glenn et al. teaches a semiconductor device, wherein the substrate comprises ceramic (Col. 5, lines 19 – 27). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Glenn et al. into the device taught by Selna, since it is desirable to use materials that are known and well suited for the intended use.

Allowable Subject Matter

7. Claims 22 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments with respect to claims 1, 2, 4, 5 and 11 – 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

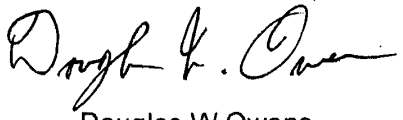
9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Douglas W Owens
Examiner
Art Unit 2811

Notice of References Cited	Application/Control No. 10/608,605	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner Douglas W. Owens	Art Unit 2811	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,640,048	06-1997	Selna, Erich	257/738
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/608,605	LEE ET AL.
Examiner	**Art Unit**
Douglas W. Owens	2811

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date									
Final	Original	9/22/05	3/31/06								
	1	√	√								
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UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/608,605		2811	28M1

Correspondence Address / Fee Address Change

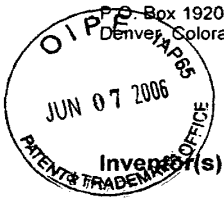
The following fields have been set to Customer Number 57299 on 01/05/2006

- Correspondence Address

The address of record for Customer Number 57299 is:
AVAGO TECHNOLOGIES, LTD.
P.O. BOX 1920
DENVER,CO 80201-1920

AVAGO TECHNOLOGIES, INC.
P.O. Box 1920
Denver, Colorado 80201-1920

ATTORNEY DOCKET NO. 70030259-1



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Kong Weng Lee et al.

Serial No.: 10/608,605 **Examiner:** Owens, Douglas W

Filing Date: June 27, 2003 **Group Art Unit:** 2811

Title: Packaging Device for Semiconductor Die, Semiconductor Device Incorporating Same and Method of Making Same

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

- [x] Response/Amendment
- [ ] Petition to extend time to respond
- [ ] New fee as calculated below
- [ ] Supplemental Declaration
- [x] No additional fee (Address envelope to "Mail Stop Amendments")
- [ ] Other: (Fee $_____)

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	7	MINUS	20	= 0	X 50	$ 0
INDEP. CLAIMS	2	MINUS	3	= 0	X 200	$ 0
☐ FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ 360	$ 0
EXTENSION FEE	1ST MONTH 120.00 ☐	2ND MONTH 450.00 ☐	3RD MONTH 1020.00 ☐	4TH MONTH 1590.00 ☐		$ 0
					OTHER FEES	$ 0
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	$ 0

Charge $0 to Deposit Account **50-3718**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3718** pursuant to 37 CFR 1.2 5. Additionally please charge any fees to Deposit Account **50-3718** under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this transmittal letter is enclosed.

Respectfully submitted,
Kong Weng Lee et al.

By _____
P. S. Dara
Attorney/Agent for Applicant(s)

Reg. No. 52,793

Date: 6/5/2006

Telephone No. (404) 610-5689

I hereby certify that this correspondence is being Deposited with the United States Postal Service as First class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: 6/5/2006

Typed Name: P. S. Dara

Signature: _____

Rev 10/04 (TransAmd)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Kong Weng Lee

Serial No.: 10/608,605

Filed: 6/27/2003

Confirmation No.: 2253

Group Art Unit: 2811

Examiner: Owens, Douglas W

Docket No. 70030259-1

For: **Packaging Device for Semiconductor Die, Semiconductor Device Incorporating Same and Method of Making Same**

AMENDMENT AND RESPONSE

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

The outstanding final Office Action mailed April 6, 2006 has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

AUTHORIZATION TO DEBIT ACCOUNT

It is not believed that extensions of time or fees for net addition of claims are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to Avago deposit account no. 50-3718.

AMENDMENTS TO THE CLAIMS

Please amend the present application as follows:

Claims

1- 4. (Canceled)

5. (Currently amended) A packaging device for a semiconductor die, the packaging device comprising:

a substantially planar substrate having opposed major surfaces;

an electrically conductive die mounting pad located on one of the major surfaces of the substrate, the conductive die mounting pad dimensioned to accommodate the die with a major surface of the die in contact therewith;

a first electrically conductive connecting pad located on the other of the major surfaces of the substrate, the first electrically conductive connecting pad dimensioned to conform to an industry standard pad layout of a printed circuit board;

a ~~The packaging device of claim 1, in which the first electrically conductive interconnecting element comprises~~ tungsten interconnecting element extending through the substrate and electrically interconnecting the mounting pad and the connecting pad.

6- 21. (Canceled)

22. (Currently amended) A semiconductor device, comprising:

a substantially planar substrate having opposed major surfaces;

an electrically conductive mounting pad located on one of the major surfaces of the substrate;

~~The semiconductor device of claim 21 wherein the semiconductor die comprises~~ a light emitting diode (LED) having a metallized bottom major surface that is mounted on the electrically conductive mounting pad, ~~and~~ the metallized bottom major surface ~~comprises~~ comprising one of an anode and a cathode of the LED;

a first electrically conductive connecting pad located on the other of the major surfaces of the substrate; and

a first electrically conductive interconnecting element extending through the substrate and electrically interconnecting the mounting pad and the first electrically

conductive connecting pad.

23. (Currently amended) The semiconductor device of claim ~~21~~ 22, further comprising:

an electrically conductive bonding pad located on the one of the major surfaces of the substrate;

a bonding wire extending between a metallized top major surface of the ~~semiconductor die~~ LED and the electrically conductive bonding pad;

a second electrically conductive connecting pad located on the other of the major surfaces of the substrate; and

a second electrically conductive interconnecting element extending through the substrate and electrically interconnecting the bonding pad and the second connecting pad.

24. (Currently amended) The semiconductor device of claim 23 wherein ~~the semiconductor die comprises a light emitting diode (LED),~~ the metallized top major surface comprises a first electrode of the LED and the metallized bottom major surface comprises a second electrode of the LED.

25. (Currently amended) The semiconductor device of claim ~~21~~ 22 wherein the first electrically conductive interconnecting element is selected to withstand an operating temperature when the ~~semiconductor die~~ LED is mounted on the electrically conductive mounting pad and to provide a low-resistance electrical connection between the mounting pad and the first electrically conductive connecting pad.

26. (Previously presented) The semiconductor device of claim 25, wherein the first electrically conductive interconnecting element comprises tungsten.

27. (Previously presented) The semiconductor device of claim 25, wherein the first electrically conductive interconnecting element comprises a slug of electrically conductive material, the slug having a diameter selected to press-fit the slug into a through hole located in the substrate between the mounting pad and the first electrically conductive connecting pad.

REMARKS

This is a full and timely response to the final Office Action mailed April6, 2006. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Present Status of Patent Application

Upon entry of the amendments in this response, claims 5 and 22-27 remain pending in the present application. More specifically, claims 5 and 22-25 have been currently amended with no introduction of new matter; and claims 1-4 and 6-21 have been canceled. Applicants have canceled these claims merely to reduce the number of disputed issues and to facilitate early allowance and issuance of other claims in the present application. Applicants reserve the right to pursue the subject matter of these claims in a continuing application, if Applicants so choose, and do not intend to dedicate the canceled subject matter to the public. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

A. Allowable Subject Matter

Examiner's Statement

Claims 22 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Examiner's Statement

Applicants wish to place on record their gratitude for Examiner's indication that claims 22 and 24 would be allowable if rewritten in independent form. Applicants have currently rewritten claim 22 in independent form including all of the limitations of base claim 21 from which it depended directly. Consequently, Applicants respectfully request allowance of rewritten claim 22.

Claim 24 has been rewritten to depend indirectly on claim 22. Because claim 22 is currently allowable, dependent claim 24 is also allowable as a matter of law. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Consequently, Applicants respectfully request allowance of rewritten claim 24.

B. Claim Objections

Statement of the Objection

Claim 1 is objected to because of the following informalities: in line 16 of the claim "susbtrate" should be replaced with --substrate--. Appropriate correction is required.

Response to the Objection

Claim 1 has been currently canceled. Hence, Applicants respectfully assert that the objection has been rendered moot.

C. Claim Rejections under 35 U.S.C. §102(b)

Statement of the Rejection

Claims 1, 2 and 4 are rejected under 35 U.S.C. §102(b) as being anticipated by US Patent No. 5,640,048 to Selna.

Response to the Rejection

Claims 1, 2 and 4 have been canceled without prejudice, waiver or disclaimer. Consequently, Applicants respectfully assert that the rejection of these claims has been rendered moot.

D. Claim Rejections under 35 U.S.C. §103(a)

Statement of the Rejection

Claims 5 and 11-21, 23, 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Selna.

Response to the Rejection

Claim 5

In rejecting Applicants' claim 5, the Office Action states: "*Regarding claim 5, Selna does not teach using tungsten for the first conductive interconnecting element. Tungsten is a known material that is well suited for use in interconnecting elements. It would have been obvious to one having ordinary skill in the art to select tungsten, since it is a known metal that is well suited for the intended uses.*"

The third of the three criteria cited in MPEP 706.2(j) "Contents of a 35 U.S.C. 103 Rejection", for establishing a *prima facie* case of obviousness, states that the prior art reference must teach or suggest all the claim limitations. In light of the above-mentioned

admission on the part of the Office Action, Applicants respectfully assert that the rejection fails to satisfy the requirements for a proper rejection under 35 U.S.C. 103(a).

Furthermore, it may be pertinent to point out that MPEP 2144.08 "Obviousness of Species When Prior Art Teaches Genus – 2100 Patentability" is not applicable in this case, because the "genus-species" relationship does not apply.

Referring back to the Office Action admission that Selna does not teach using tungsten, Applicants respectfully traverse the assertion that "*Tungsten is a known material that is well suited for use in interconnecting elements. It would have been obvious to one having ordinary skill in the art to select tungsten, since it is a known metal that is well suited for the intended uses.*" Because reference documents have not been provided to substantiate the assertion that tungsten is well suited for use in interconnecting elements, Applicants conclude that this statement is based on facts within the personal knowledge of the Examiner.

Consequently, Applicants cite *37 CFR 1.104 Nature of examination, paragraph (d) (2)*, reproduced below for easy reference:

> (2) When a rejection in an application is based on facts within the personal knowledge of an employee of the Office, the data shall be as specific as possible, and the reference must be supported, when called for by the applicant, by the affidavit of such employee, and such affidavit shall be subject to contradiction or explanation by the affidavits of the applicant and other persons.

Applicants hereby request an affidavit from Examiner supporting the assertion that tungsten is "well suited for interconnecting elements."

If such an affidavit is not provideable, Applicants respectfully assert that the rejection of claim 5 under 35 U.S.C. 103(a) is improper and request withdrawal of the rejection followed by allowance of claim 5.

Claims 11-21

Claims 11-21 have been currently canceled with no prejudice, waiver or disclaimer. Consequently, Applicants respectfully assert that the rejection of claims 11-21 has been rendered moot.

Claims 23, 25-27

Because claim 22 is allowable, claims 23 and 25-27 that depend directly or indirectly on claim 22 are also allowable as a matter of law. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Applicants respectfully request withdrawal of the rejection, followed by allowance of Claim 23 and 25-27.

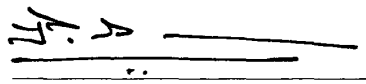
Prior Art Made of Record

The prior art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that claims 5 and 22-27 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned representative at (404) 610-5689.

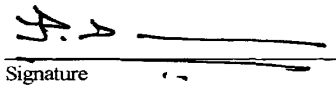
Respectfully submitted,



P. S. Dara
Reg. No. 52,793

P. S. Dara
7115 Threadstone Overlook
Duluth, GA 30097
(404)-610-5689

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA, 22313-1450, on **June 6, 2006**



Signature
Name: P. S. Dara

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 10/603,005

APPLICATION AS FILED - PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))							
SEARCH FEE (37 CFR 1.16(k), (i), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*	x 25 =		OR	x 50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*	x 100 =			x 200 =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
			TOTAL			TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

AMENDMENT A	10/7/06	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	7	Minus	21	=	x 25 =		OR	x 50 =	
	Independent (37 CFR 1.16(h))	2	Minus	3	=	x 100 =		OR	x 200 =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))		Minus		=	x =		OR	x =	
	Independent (37 CFR 1.16(h))		Minus		=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

[illegible]
The "Highest Number Previously Paid For" ... [illegible] ... found in the appropriate box in column 1.

[illegible] ... to retain a benefit by the public which is to file (and by the USPTO to process) an application ... This collection is estimated to take 12 minutes to complete ... [illegible] ... depending upon the individual case ... [illegible] ... should be sent to the Chief Information Officer, U.S. Patent ... [illegible] ... DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

10/608,605

APPLICATION NUMBER	

?	Rejected	—	(Through Numeral) Cancelled	N	Non-Elected	A	Appeal
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	06/27/2003	Kong Weng Lee	70030259-1	2253

57299 7590 06/23/2006

AVAGO TECHNOLOGIES, LTD.
P.O. BOX 1920
DENVER, CO 80201-1920

EXAMINER	
OWENS, DOUGLAS W	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

HA

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/608,605	Applicant(s) LEE ET AL.	
	Examiner Douglas W. Owens	Art Unit 2811	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 07 June 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☐ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *See Continuation Sheet*. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☒ Newly proposed or amended claim(s) 22-27 would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: 22,24.
   Claim(s) rejected: 1,2,4,5,11-21,23 and 25-27.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

Douglas W. Owens

Douglas W Owens
Primary Examiner
Art Unit: 2811

Continuation of 3. NOTE: The proposed amendment to claim 5 is a change of scope that will require additional search and consideration.

Continuation of 11. does NOT place the application in condition for allowance because: Applicant's arguments with respect to claim 5 are not convincing. Applicant argues that the assertion that "tungsten is a known material that is well-suited for use in interconnecting elements" is based on the personal knowledge of the Examiner. In fact, using tungsten in interconnecting elements is notoriously well-known in the art and capable of instant and unquestionable demonstration as being well-known. Examiner has constructively taken official notice of that fact, which has been asserted merely to "fill in the-gaps". To adequately traverse such a finding, an applicant must specifically point out the supposed errors in the examiner's action, which would include stating why the noticed fact is not considered to be common knowledge or well-known in the art. See 37 CFR1.111(b). See also Chevenard, 139 F.2d at 713, 60 USPQ at 241 ("[I]n the absence of any demand by appellant for the examiner to produce authority for his statement, we will not consider this contention."). A general allegation that the claims define a patentable invention without any reference to the examiner's assertion of official notice would be inadequate. If applicant adequately traverses the examiner's assertion of official notice, the examiner must provide documentary evidence in the next Office action if the rejection is to be maintained. See 37 CFR 1.104(c)(2). Applicant has failed to properly traverse the official notice taken in the final rejection, since

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Kong Weng Lee

Serial No.: 10/608,605

Filed: 6/27/2003

Confirmation No.: 2253

Group Art Unit: 2811

Examiner: Owens, Douglas W

Docket No. 70030259-1

For: **Packaging Device for Semiconductor Die, Semiconductor Device Incorporating Same and Method of Making Same**

AMENDMENT AND RESPONSE TO ADVISORY ACTION

Mail Stop – RCE
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants respectfully request entry of the following amendments and remarks contained herein in response to the outstanding Advisory Action mailed June 23, 2006. Applicants respectfully submit that the amendment and remarks contained herein place the instant application in condition for allowance. A Request for Continued Examination under 37 U.S.C. §1.114, together with a one-month extension of time, is being filed concurrently with this response to the Advisory Action. Consequently, Applicants respectfully submit that the final Office Action mailed April 6, 2006 is effectively made non-final.

AUTHORIZATION TO DEBIT ACCOUNT

It is not believed that extensions of time or fees for net addition of claims are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to Avago deposit account no. 50-3718.

AMENDMENTS TO THE CLAIMS

Please amend the present application as follows:

Claims

1- 21. (Canceled)

22. (Currently amended) A semiconductor device, comprising:

a substantially planar substrate having opposed major surfaces;

an electrically conductive mounting pad located on one of the major surfaces of the substrate;

~~The semiconductor device of claim 21 wherein the semiconductor die comprises~~ a light emitting diode (LED) having a metallized bottom major surface that is mounted on the electrically conductive mounting pad, ~~and~~ the metallized bottom major surface ~~comprises~~ comprising one of an anode and a cathode of the LED;

a first electrically conductive connecting pad located on the other of the major surfaces of the substrate; and

a first electrically conductive interconnecting element extending through the substrate and electrically interconnecting the mounting pad and the first electrically conductive connecting pad.

23. (Currently amended) The semiconductor device of claim ~~21~~ 22, further comprising:

an electrically conductive bonding pad located on the one of the major surfaces of the substrate;

a bonding wire extending between a metallized top major surface of the ~~semiconductor die~~ LED and the electrically conductive bonding pad;

a second electrically conductive connecting pad located on the other of the major surfaces of the substrate; and

a second electrically conductive interconnecting element extending through the substrate and electrically interconnecting the bonding pad and the second connecting pad.

24. (Currently amended) The semiconductor device of claim 23 wherein ~~the semiconductor die comprises a light emitting diode (LED),~~ the metallized top major surface comprises a first electrode of the LED and the metallized bottom major surface comprises a second electrode of the LED.

25. (Currently amended) The semiconductor device of claim ~~21~~ 22 wherein the first electrically conductive interconnecting element is selected to withstand an operating temperature when the ~~semiconductor die~~ LED is mounted on the electrically conductive mounting pad and to provide a low-resistance electrical connection between the mounting pad and the first electrically conductive connecting pad.

26. (Previously presented) The semiconductor device of claim 25, wherein the first electrically conductive interconnecting element comprises tungsten.

27. (Previously presented) The semiconductor device of claim 25, wherein the first electrically conductive interconnecting element comprises a slug of electrically conductive material, the slug having a diameter selected to press-fit the slug into a through hole located in the substrate between the mounting pad and the first electrically conductive connecting pad.

REMARKS

This is a response to the Advisory action mailed June 23, 2006. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Present Status of Patent Application

The Advisory action mailed June 23, 2006 indicates that the claim amendments submitted earlier by Applicants have not been entered. Consequently, Applicants are hereby re-submitting the amended claims and additionally canceling previously submitted amended claim 5.

Upon entry of the amendments in this response, claims 22-27 remain pending in the present application. More specifically, claims 22-25 have been currently amended with no introduction of new matter; and claims 1-21 have been canceled. Applicants have canceled these claims merely to reduce the number of disputed issues and to facilitate early allowance and issuance of other claims in the present application. Applicants reserve the right to pursue the subject matter of these claims in a continuing application, if Applicants so choose, and do not intend to dedicate the canceled subject matter to the public. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

A. Allowable Subject Matter

Examiner's Statement

Examiner has indicated in the final Office action dated April 6, 2006 that claims 22 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Examiner's Statement

Applicants wish to place on record their gratitude for Examiner's indication that claims 22 and 24 would be allowable if rewritten in independent form. Applicants have currently rewritten claim 22 in independent form including all of the limitations of base claim 21 from which it depended directly. Consequently, Applicants respectfully request allowance of rewritten claim 22.

Claim 24 has been rewritten to depend indirectly on claim 22. Because claim 22 is currently allowable, dependent claim 24 is also allowable as a matter of law. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Consequently, Applicants respectfully request allowance of rewritten claim 24.

B. Claim Objections

Statement of the Objection

Claim 1 is objected to because of the following informalities: in line 16 of the claim "susbtrate" should be replaced with --substrate--. Appropriate correction is required.

Response to the Objection

Claim 1 has been currently canceled. Hence, Applicants respectfully assert that the objection has been rendered moot.

C. Claim Rejections under 35 U.S.C. §102(b)

Statement of the Rejection

Claims 1, 2 and 4 are rejected under 35 U.S.C. §102(b) as being anticipated by US Patent No. 5,640,048 to Selna.

Response to the Rejection

Claims 1, 2 and 4 have been canceled without prejudice, waiver or disclaimer. Consequently, Applicants respectfully assert that the rejection of these claims has been rendered moot.

D. Claim Rejections under 35 U.S.C. §103(a)

Statement of the Rejection

Claims 5 and 11-21, 23, 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Selna.

Response to the Rejection

Claims 5 and 11-21

Claims 5 and 11-21 have been currently canceled with no prejudice, waiver or disclaimer. Consequently, Applicants respectfully assert that the rejection of claims 5 and 11-21 has been rendered moot.

Claims 23, 25-27

Because claim 22 is allowable, claims 23 and 25-27 that depend directly or indirectly on claim 22 are also allowable as a matter of law. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Applicants respectfully request withdrawal of the rejection, followed by allowance of Claim 23 and 25-27.

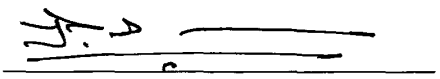
Prior Art Made of Record

The prior art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that claims 22-27 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned representative at (404) 610-5689.

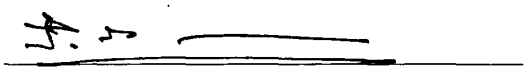
Respectfully submitted,



P. S. Dara
Reg. No. 52,793

P. S. Dara
7115 Threadstone Overlook
Duluth, GA 30097
(404)-610-5689

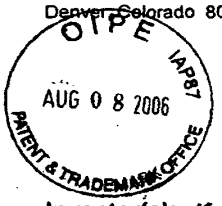
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA, 22313-1450, on **August 4, 2006**



Signature
Name: P. S. Dara

AVAGO TECHNOLOGIES, LTD.
P.O. Box 1920
Denver, Colorado 80201-1920

ATTORNEY DOCKET NO. 70030259-1



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Kong Weng Lee et al.

Serial No.: 10/608,605 **Examiner:** Owens, Douglas W

Filing Date: June 27, 2003 **Group Art Unit:** 2811

Title: Packaging Device for Semiconductor Die, Semiconductor Device Incorporating Same and Method of Making Same

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

REQUEST FOR CONTINUED EXAMINATION (RCE) 37 CFR 1.114

Subsection (b) of 35 U.S.C. 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995.
See The American Inventors Protection Act of 1999 (AIPA).

Sir:

This is a Request for Continued Examination (RCE) under CFR 1.114 of the above-identified application.

NOTE: 37 CFR 1.114 is effective on May 20, 2000. If the above application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under CFR 1.53(d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice, Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1233 off. Gaz. Pat. Office 47 (Apr.11, 2000), which Established RCE practice.

Submission under 37 CFR 1.114

☐ Previously submitted:
- ☐ Consider the amendment(s)/reply under 37 CFR 1.116 previously filed on (Any unentered amendment(s) referred to above will be entered).
- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on
- ☐ Other:

☒ Enclosed:
- ☒ Amendment/Reply
- ☐ Affidavit(s)/Declarations(s)
- ☐ Information Disclosure Statement (IDS)
- ☐ Other:

Miscellaneous

☐ Suspension of action is requested under 37 CFR 1.103(c) for a period of months. The fee for this Suspension is (37 CFR 1.17(i)) **$130.00**.
☐ Other:

08/09/2006 RFEKADU1 00000004 503718 10608605
02 FC:1801 790.00 DA

RCE filing fee **$790.00**

☐ A Petition for Extension of Time

☐	One month	$120.00
☐	Two months	$450.00
☐	Three months	$1020.00
☐	Four months	$1590.00

Please charge to Deposit Account **50-3718** the sum of $790.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **50-3718** pursuant to 37 CFR 1.25.

A duplicate copy of this transmittal letter is enclosed.

☒ I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.

Date of Deposit: 8/4/2006

OR

☐ I hereby certify that this paper is being facsimile transmitted to the Commissioner for Patents on the date shown below.

Date of Facsimile:

Typed Name: P. S. Dara

Signature: _____

Respectfully submitted,

Kong Weng Lee et al.

By _____

P. S. Dara
Attorney/Agent for Applicant(s)

Reg. No. 52,793

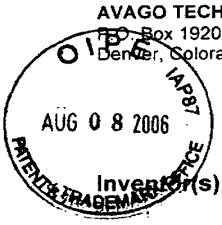
Date: 8/4/2006

Telephone No. (404) 610-5689

AVAGO TECHNOLOGIES, INC.
P.O. Box 1920
Denver, Colorado 80201-1920

ATTORNEY DOCKET NO. 70030259-1

RCE



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Kong Weng Lee et al.

Serial No.: 10/608,605 **Examiner:** Owens, Douglas W

Filing Date: June 27, 2003 **Group Art Unit:** 2811

Title: Packaging Device for Semiconductor Die, Semiconductor Device Incorporating Same and Method of Making Same

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

- [x] Response/Amendment
- [x] Petition to extend time to respond
- [ ] New fee as calculated below
- [ ] Supplemental Declaration
- [ ] No additional fee (Address envelope to "Mail Stop Amendments")
- [ ] Other: (Fee $_____)

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	6	MINUS	20	= 0	X 50	$ 0
INDEP. CLAIMS	2	MINUS	3	= 0	X 200	$ 0
☐ FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ 360	$ 0
EXTENSION FEE	1ST MONTH 120.00 ☒	2ND MONTH 450.00 ☐	3RD MONTH 1020.00 ☐	4TH MONTH 1590.00 ☐		$ 120
					OTHER FEES	$ 0
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	$ 120

Charge $120 to Deposit Account **50-3718**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3718** pursuant to 37 CFR 1.2 5. Additionally please charge any fees to Deposit Account **50-3718** under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this transmittal letter is enclosed.

Respectfully submitted,
Kong Weng Lee et al.

By _____
P. S. Dara
Attorney/Agent for Applicant(s)

Reg. No. 52,793

Date: 8/4/2006

Telephone No. (404) 610-5689

I hereby certify that this correspondence is being Deposited with the United States Postal Service as First class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: 8/4/2006

Typed Name: P. S. Dara

Signature: _____

08/09/2006 RFEKADU1 00000004 503718 10608605
01 FC:1251 120.00 DA

Rev 10/04 (TransAmd)

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number: 10608605

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))							
SEARCH FEE (37 CFR 1.16(k), (l), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	x =		OR	x =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	x =			x =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
			TOTAL			TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

8/08/06

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 6	Minus	** 21	= 0	x25.00 =		OR	x50.00 =	
Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0	x100.00 =		OR	x200.00 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3146	257/690,784,700,689,774,783,707, 718,719,706,717,720.ccls. and @pd>"20040415"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/21 12:41
L2	3087	257/690,784,700,689,774,783,707, 718,719,706,717.ccls. and @pd>"20040415"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/21 12:42
L3	3031	257/690,784,700,689,774,783,707, 718,719,706.ccls. and @pd>"20040415"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/21 12:42
L4	2730	257/690,784,700,689,774,783,707, 718,719.ccls. and @pd>"20040415"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/21 13:12
L5	651	257/706,717,720.ccls. and @pd>"20040415"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/21 13:12
L6	6	((die chip) same (mounting adj pad) and LED).clm.	US-PGPUB	OR	ON	2006/08/21 13:17
S1	2	("5986885").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/21 12:40
S2	2	("6084295").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 10:25
S3	312	die same (mounting adj pad)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/08 10:26
S4	985	(die chip) same (mounting adj pad)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/31 12:59

EAST Search History

S5	372	(die chip) same (mounting adj pad) same substrate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/08 10:27
S6	6	(("5986885") or ("6084295") or ("6620720")).PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/22 12:01
S7	2226	(die chip IC) same (mount$3 with pad) same interconnect$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/22 14:02
S8	7479	(die chip IC) same (bond$3 with pad) same interconnect$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/22 14:02
S9	2123	(die chip IC) same (bond$3 with pad) same interconnect$3 same (hole via)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/22 14:38
S10	2	("6191477").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/22 14:38
S11	7	("5506755" | "5640048" | "5646826" | "5721454" | "5808873" | "5923084" | "6097089").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/22 14:57
S12	13	("3568000" | "3582865" | "3739469" | "4535385" | "4739448" | "4866841" | "5010641" | "5102829" | "5264729" | "5291062" | "5355283" | "5397917" | "5468999").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/22 15:00
S13	2	("4739448" | "4855537").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/22 15:02
S14	3226	(die chip) near3 pad near3 (metal copper cu)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/30 16:38

EAST Search History

S15	1720	(die chip) near2 pad near2 (metal copper cu)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/30 16:39
S16	2	("5640048").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/31 12:55
S17	85	(die chip) same (mounting adj pad) and LED	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/21 13:16

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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NOTICE OF ALLOWANCE AND FEE(S) DUE

57299 7590 08/25/2006

AVAGO TECHNOLOGIES, LTD.
P.O. BOX 1920
DENVER, CO 80201-1920

EXAMINER	
OWENS, DOUGLAS W	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/25/2006

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	06/27/2003	Kong Weng Lee	70030259-1	2253

TITLE OF INVENTION: PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	11/27/2006

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

57299 7590 08/25/2006

AVAGO TECHNOLOGIES, LTD.
P.O. BOX 1920
DENVER, CO 80201-1920

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	06/27/2003	Kong Weng Lee	70030259-1	2253

TITLE OF INVENTION: PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	11/27/2006

EXAMINER	ART UNIT	CLASS-SUBCLASS
OWENS, DOUGLAS W	2811	257-690000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	06/27/2003	Kong Weng Lee	70030259-1	2253

57299 7590 08/25/2006

AVAGO TECHNOLOGIES, LTD.
P.O. BOX 1920
DENVER, CO 80201-1920

EXAMINER	
OWENS, DOUGLAS W	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/25/2006

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

Notice of Allowability	Application No.	Applicant(s)	
	10/608,605	LEE ET AL.	
	Examiner	Art Unit	
	Douglas W. Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on August 8, 2006*.

2. ☒ The allowed claim(s) is/are 22-27.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Douglas W Owens
Primary Examiner
Art Unit: 2811

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In paragraph [0001] of the specification, delete "10/xxx,xxx" and insert -- 10/608,606--.

Allowable Subject Matter

2. Claims 22 – 27 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Douglas W Owens
Primary Examiner
Art Unit 2811

DWO
21 August 2006

Issue Classification

Application/Control No.	Applicant(s)/Patent under Reexamination
10608605	LEE ET AL.
Examiner	**Art Unit**
Owens, Douglas W	2811

ORIGINAL

CLASS	SUBCLASS
257	690

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	784	689			

INTERNATIONAL CLASSIFICATION

CLAIMED	NON-CLAIMED
H 0 1 L 23 / 48	

NONE (Assistant Examiner) (Date)	Douglas K. Owens	**Total Claims Allowed:** 6
Yolanda Robinson 8/23/06 (Legal Instruments Examiner) (Date)	Douglas W. Owens 8/21/06 (Primary Examiner) (Date)	O.G. Print Claim(s): 22 O.G. Print Figure: 4E,4F

U.S. Patent and Trademark Office

Part of Paper No. 20060821

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10608605	LEE ET AL.
	Examiner Owens, Douglas W	Art Unit 2811

Notes	Date	Examiner
Update Search	8/21/06	DWO

Interference Searched	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10608605	LEE ET AL.
	Examiner	Art Unit
	Owens, Douglas W	2811

Class	SubClass	Date	Examiner
257	690,784,689	8/21/06	DWO
Interference text search		8/21/06	DWO

U.S. Patent and Trademark Office	Part of Paper No.:	20060821

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10608605	LEE ET AL.
Examiner	**Art Unit**
Owens, Douglas W	2811

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	8/21/06								
	1	-								
	2	-								
	3	-								
	4	-								
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	27	=								

UNITED STATES PATENT AND TRADEMARK OFFICE

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BIBDATASHEET

Bib Data Sheet

CONFIRMATION NO. 2253

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/608,605	06/27/2003 RULE	257	2811	70030259-1

APPLICANTS

Kong Weng Lee, Penang, MALAYSIA;

Kee Yean Ng, Penang, MALAYSIA;
Yew Cheong Kuan, Penang, MALAYSIA;Gin Ghee Tan, Penang, MALAYSIA;
Cheng Why Tan, Penang, MALAYSIA;

** CONTINUING DATA **********

** FOREIGN APPLICATIONS **********

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 09/17/2003

Foreign Priority claimed	STATE OR	SHEETS	TOTAL	INDEPENDENT
35 USC 119 (a-d) conditions met: ☐ yes ☒ no; ☐ yes ☒ no ☐ Met after Allowance	COUNTRY	DRAWING	CLAIMS	CLAIMS
Verified and Acknowledged: Examiner's Signature / Initials	MALAYSIA	8	20	2

ADDRESS
AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland , CO
80537-0599

TITLE
Packaging device for semiconductor die, semiconductor device incorporating same and method of making same

FILING FEE	FEES: Authority has been given in Paper	☐ All Fees
RECEIVED	No. _____ to charge/credit DEPOSIT ACCOUNT	☐ 1.16 Fees (Filing)
750	No. _____ for following:	☐ 1.17 Fees (Processing Ext. of time)
		☐ 1.18 Fees (Issue)
		☐ Other _____

P.O. Box 1920
Denver, Colorado 80201-1920

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NOV 07 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Lee et al.

Serial No.: 10/608,605 **Examiner:** Owens, Douglas W

Filing Date: June 27, 2003 **Group Art Unit:** 2253

Title: PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

REQUEST FOR CONTINUED EXAMINATION (RCE) 37 CFR 1.114

Subsection (b) of 35 U.S.C. 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995.
See The American Inventors Protection Act of 1999 (AIPA).

Sir:

This is a Request for Continued Examination (RCE) under CFR 1.114 of the above-identified application.

NOTE: 37 CFR 1.114 is effective on May 20, 2000. If the above application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under CFR 1.53(d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice, Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1233 off. Gaz. Pat. Office 47 (Apr.11, 2000), which Established RCE practice.

Submission under 37 CFR 1.114

☐ Previously submitted:
- ☐ Consider the amendment(s)/reply under 37 CFR 1.116 previously filed on (Any unentered amendment(s) referred to above will be entered).
- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on
- ☐ Other: Information Disclosure Statement

☐ Enclosed:
- ☐ Amendment/Reply
- ☐ Affidavit(s)/Declarations(s)
- ☒ Information Disclosure Statement (IDS)
- ☒ Other: PTO Form 1449

Miscellaneous

- ☐ Suspension of action is requested under 37 CFR 1.103(c) for a period of months. The fee for this Suspension is (37 CFR 1.17(i)) **$130.00.**
- ☐ Other:

(RCE) (37 CFR 1.114) (continued)

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NOV 07 2006

RCE filing fee **$790.00**

☐ A Petition for Extension of Time

☐	One month	$120.00
☐	Two months	$450.00
☐	Three months	$1020.00
☐	Four months	$1590.00

Please charge to Deposit Account **50-3718** the sum of $790.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **50-3718** pursuant to 37 CFR 1.25.

A duplicate copy of this transmittal letter is enclosed.

☐ I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.

Date of Deposit:

OR

☒ I hereby certify that this paper is being facsimile transmitted to the Commissioner for Patents on the date shown below.

Date of Facsimile: 11/7/06

Typed Name: Joy Reinhart

Signature: _____

Respectfully submitted,

Lee et al.

By _____

Jay K. Malkin
Attorney/Agent for Applicant(s)

Reg. No. 31,393

Date: 11/7/06

Telephone No. (303) 298-9888

Denver, Colorado 80201-1920

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NOV 07 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Lee et al.

Serial No.: 10/608,605 **Examiner:** Owens, Douglas W

Filing Date: June 27, 2003 **Group Art Unit:** 2253

Title: PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

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☐ Enclosed:
- ☐ Amendment/Reply
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- ☐ Other:

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NOV 07 2006

RCE filing fee **$790.00**

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☐	Two months	$450.00
☐	Three months	$1020.00
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A duplicate copy of this transmittal letter is enclosed.

☐ I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.

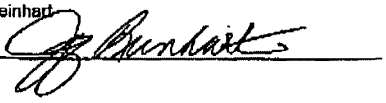
Date of Deposit:

OR

☒ I hereby certify that this paper is being facsimile transmitted to the Commissioner for Patents on the date shown below.

Date of Facsimile: 11/7/06

Typed Name: Joy Reinhart

Signature: 

Respectfully submitted,

Lee et al.

By 

Jay K. Malkin
Attorney/Agent for Applicant(s)

Reg. No. 31,393

Date: 11/7/06

Telephone No. (303) 298-9888

P.O. Box 1920
Denver, Colorado 80201-1920

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NOV 0 7 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Lee et al.

Serial No.: 10/608,605 **Examiner:** Owens, Douglas W

Filing Date: June 27, 2003 **Group Art Unit:** 2253

Title: PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

(a) ☒ Under 37 CFR 1.97(b).
(Within three months of filing national application; or date of entry of national application; or before mailing date of first Office action on the merits; whichever occurs last).

(b) ☐ Under 37 CFR 1.97(c) together with ***either*** a:
☐ Statement under CFR 1.97(e), or
☐ $180.00 fee under 37 CFR 1.17(p).
(After the CFR 1.97(b) time period, but before a final action or notice of allowance, whichever occurs first).

(c) ☐ Under 37 CFR 1.97(d) together with: a
Statement under 37 CFR 1.97(e), ***and***
$180.00 fee as set forth in 37 CFR 1.17(p).
(After a final action or notice of allowance, whichever occurs first, but before payment of the issue fee).

☐ STATEMENT UNDER 37 CFR 1.97(e)
The undersigned certifies that:

☐ Each item of information contained in the Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the statement, **or**

☐ No item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in 37 CFR § 1.56(c) more than three months prior to the filing of the Information Disclosure Statement.

☐ PRIOR APPLICATIONS
References identified with an asterisk (*) in the enclosed PTO Form 1449, were disclosed in prior Patent Application No. , filed , now U.S. Patent No. , and, as such, copies thereof are not included pursuant to the provisions of 37 CFR 1.98(d).

☐ FOREIGN LANGUAGE DOCUMENTS
A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO form 1449, as presently understood by the individual(s) designated in 37 CFR 1.56(c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

☒ FEE AUTHORIZATION

Please charge to Deposit Account **50-3718** the sum of $0.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **50-3718** pursuant to 37 CFR 1.25.

Respectfully submitted,

Lee et al.

By _____

Jay K. Malkin
Attorney/Agent for Applicant(s)

Reg. No. 31,393

Date: 11/7/06

Telephone No. (303) 298-9888

I hereby certify that this correspondence is being deposited with the United States Postal Service as:

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In an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.

OR

☒ I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Date of Facsimile: 11/7/06

Typed Name: Joy Reinhart

Signature: _____

Form PTO-1449	ATTORNEY DOCKET NO. 70030259-1	SERIAL NO. 11/608,605
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	APPLICANT Lee et al.	
(Use several sheets if necessary)	FILING DATE June 27, 2003	GROUP 2253

REFERENCE DESIGNATION — U.S. PATENT DOCUMENTS

EXAMINER INITIAL	*	DOCUMENT NUMBER	DATE	NAME
		5,006,673	April 9, 1991	Freyman et al.
		5,298,687	March 29, 1994	Rapoport et al.
		5,670,797	September 23, 1997	Okazaki
		6,362,525	March 26, 2002	Rahim
		6,383,835	May 7, 2002	Hata et al.
		6,707,247	March 16, 2004	Murano
		6,828,510	December 7, 2004	Asai et al.

FOREIGN PATENT DOCUMENT

		DOCUMENT NUMBER	DATE	NAME	TRANSLATION YES	TRANSLATION NO

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

* Copies of these references are not enclosed Pursuant to 37 CFR 1.98(d). (See accompanying IDS)

Form PTO-1449	ATTORNEY DOCKET NO. 70030259-1	SERIAL NO. 10/608,605
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	APPLICANT Lee et al.	
(Use several sheets if necessary)	FILING DATE June 27, 2003	GROUP 2253

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL	*	DOCUMENT NUMBER	DATE	NAME
		2003/0017645 A1	January 23, 2003	Kabayashi et al.
		2003/0020126 A1	January 30, 2003	Sakamoto et al.
		2003/0040138 A1	Feburary 27, 2003	Kobayashi et al.

FOREIGN PATENT DOCUMENT

		DOCUMENT NUMBER	DATE	NAME	TRANSLATION YES	TRANSLATION NO

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

* Copies of these references are not enclosed Pursuant to 37 CFR 1.98(d). (See accompanying IDS)

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 11/15/2006

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01 FC : 1801 790.00 DA

PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 8, 2004

10/608605

CLAIMS AS FILED - PART I

11/7/06

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	minus 20=	*
INDEPENDENT CLAIMS	minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐			OTHER THAN OR SMALL ENTITY		
RATE	FEE		RATE	FEE	
BASIC FEE	150.00	OR	BASIC FEE	~~300.00~~	
X$ 25=		OR	X$50=	790.	
X100=		OR	X200=		
+180=		OR	+360=		
TOTAL		OR	TOTAL	790.	PAID

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY			OTHER THAN SMALL ENTITY		
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE	
X$ 25=		OR	X$50=		
X100=		OR	X200=		
+180=		OR	+360=		
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE		

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	20	("20030017645"|"20030020126"|"20030040138"|"5006673"|"5298687"|"5670797"|"6362525"|"6383835"|"6707247"|"6828510").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/24 14:54
L2	336	257/690,784,700,689,774,783,707,718,719,706,717.ccls. and @pd>"20060821"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/24 15:05
L3	0	((die chip) same (mounting adj pad) and LED).clm. and @pd>"20060821"	US-PGPUB	OR	ON	2006/11/24 15:11
L4	67	257/706,717,720.ccls. and @pd>"20060821"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/24 15:11
L5	2	(die chip) same (mounting adj pad) and LED and @pd>"20060821"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/24 15:14
L6	0	H01l adj 31/0224	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/24 15:15
S1	2	("5986885").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/24 14:54
S2	2	("6084295").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 10:25
S3	312	die same (mounting adj pad)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/08 10:26
S4	985	(die chip) same (mounting adj pad)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/31 12:59

EAST Search History

S5	372	(die chip) same (mounting adj pad) same substrate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/08 10:27
S6	6	(("5986885") or ("6084295") or ("6620720")).PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/22 12:01
S7	2226	(die chip IC) same (mount$3 with pad) same interconnect$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/22 14:02
S8	7479	(die chip IC) same (bond$3 with pad) same interconnect$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/22 14:02
S9	2123	(die chip IC) same (bond$3 with pad) same interconnect$3 same (hole via)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/22 14:38
S10	2	("6191477").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/22 14:38
S11	7	("5506755" | "5640048" | "5646826" | "5721454" | "5808873" | "5923084" | "6097089").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/22 14:57
S12	13	("3568000" | "3582865" | "3739469" | "4535385" | "4739448" | "4866841" | "5010641" | "5102829" | "5264729" | "5291062" | "5355283" | "5397917" | "5468999").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/22 15:00
S13	2	("4739448" | "4855537").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/22 15:02
S14	3226	(die chip) near3 pad near3 (metal copper cu)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/30 16:38

EAST Search History

S15	1720	(die chip) near2 pad near2 (metal copper cu)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/30 16:39
S16	2	("5640048").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/31 12:55
S17	85	(die chip) same (mounting adj pad) and LED	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/24 15:12
S18	3146	257/690,784,700,689,774,783,707,718,719,706,717,720.ccls. and @pd>"20040415"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/21 12:41
S19	3087	257/690,784,700,689,774,783,707,718,719,706,717.ccls. and @pd>"20040415"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/24 15:05
S20	3031	257/690,784,700,689,774,783,707,718,719,706.ccls. and @pd>"20040415"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/21 12:42
S21	2730	257/690,784,700,689,774,783,707,718,719.ccls. and @pd>"20040415"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/21 13:12
S22	651	257/706,717,720.ccls. and @pd>"20040415"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/24 15:11
S23	6	((die chip) same (mounting adj pad) and LED).clm.	US-PGPUB	OR	ON	2006/11/24 15:11

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

57299 7590 12/04/2006

AVAGO TECHNOLOGIES, LTD.
P.O. BOX 1920
DENVER, CO 80201-1920

EXAMINER	
OWENS, DOUGLAS W.	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/04/2006

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	06/27/2003	Kong Weng Lee	70030259-1	2253

TITLE OF INVENTION: PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	03/05/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

57299 7590 12/04/2006

AVAGO TECHNOLOGIES, LTD.
P.O. BOX 1920
DENVER, CO 80201-1920

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	06/27/2003	Kong Weng Lee	70030259-1	2253

TITLE OF INVENTION: PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	03/05/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
OWENS, DOUGLAS W	2811	257-690000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	06/27/2003	Kong Weng Lee	70030259-1	2253

57299 7590 12/04/2006

AVAGO TECHNOLOGIES, LTD.
P.O. BOX 1920
DENVER, CO 80201-1920

EXAMINER	
OWENS, DOUGLAS W	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/04/2006

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

Notice of Allowability	Application No.	Applicant(s)	
	10/608,605	LEE ET AL.	
	Examiner	Art Unit	
	Douglas W. Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on August 8, 2006*.

2. ☒ The allowed claim(s) is/are 22-27.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 11/07/06
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Douglas W. Owens

DOUGLAS W. OWENS
PRIMARY EXAMINER

Form PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTORNEY DOCKET NO.	SERIAL NO.
70030259-1	11/608,605
APPLICANT	
Lee et al.	
FILING DATE	GROUP
June 27, 2003	2253

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	*	DOCUMENT NUMBER	DATE	NAME
DWO		5,006,673	April 9, 1991	Freyman et al.
DWO		5,298,687	March 29, 1994	Rapoport et al.
DWO		5,670,797	September 23, 1997	Okazaki
DWO		6,362,525	March 26, 2002	Rahim
DWO		6,383,835	May 7, 2002	Hata et al.
DWO		6,707,247	March 16, 2004	Murano
DWO		6,828,510	December 7, 2004	Asai et al.

FOREIGN PATENT DOCUMENT

		DOCUMENT NUMBER	DATE	NAME	TRANSLATION YES	TRANSLATION NO

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	/Douglas W Owens/	DATE CONSIDERED	11/24/2006

* Copies of these references are not enclosed Pursuant to 37 CFR 1.98(d). (See accompanying IDS)

BEST AVAILABLE COPY

Form PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTORNEY DOCKET NO.	SERIAL NO.
70030259-1	10/608,605
APPLICANT	
Lee et al.	
FILING DATE	GROUP
June 27, 2003	2253

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL	*	DOCUMENT NUMBER	DATE	NAME
DWO		2003/0017645 A1	January 23, 2003	Kabayashi et al.
DWO		2003/0020126 A1	January 30, 2003	Sakamoto et al.
DWO		2003/0040138 A1	Feburary 27, 2003	Kobayashi et al.

FOREIGN PATENT DOCUMENT

		DOCUMENT NUMBER	DATE	NAME	TRANSLATION YES	TRANSLATION NO

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER /Douglas W Owens/ DATE CONSIDERED 11/24/2006

* Copies of these references are not enclosed Pursuant to 37 CFR 1.98(d). (See accompanying IDS)

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10608605	LEE ET AL.
Examiner	**Art Unit**
Owens, Douglas W	2811

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	8/21/06	11/24/06							
	1	-	-							
	2	-	-							
	3	-	-							
	4	-	-							
	5	-	-							
	6	-	-							
	7	-	-							
	8	-	-							
	9	-	-							
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	14	-	-							
	15	-	-							
	16	-	-							
	17	-	-							
	18	-	-							
	19	-	-							
	20	-	-							
	21	-	-							
	22	=	=							
	23	=	=							
	24	=	=							
	25	=	=							
	26	=	=							
	27	=	=							

Issue Classification

Application/Control No.	Applicant(s)/Patent under Reexamination
10608605	LEE ET AL.
Examiner	**Art Unit**
Owens, Douglas W	2811

ORIGINAL

CLASS	SUBCLASS
257	690

INTERNATIONAL CLASSIFICATION

CLAIMED	NON-CLAIMED
H 0 1 L 23 / 48	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	784	689			

NONE

(Assistant Examiner) (Date)

Douglas K. Owens

Total Claims Allowed: 6

12/1/06

(Legal Instruments Examiner) (Date)

Douglas W. Owens 11/24/2006

(Primary Examiner) (Date)

O.G. Print Claim(s)	O.G. Print Figure
22	4E,4F

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10608605	LEE ET AL.
	Examiner Owens, Douglas W	Art Unit 2811

Notes	Date	Examiner
Update Search	08/21/2006	DWO
Update Search	11/24/2006	DWO

Interference Searched	Application/Control No. 10608605	Applicant(s)/Patent Under Reexamination LEE ET AL.
	Examiner Owens, Douglas W	Art Unit 2811

Class	SubClass	Date	Examiner
257	690,784,689	08/21/2006	DWO
Interference text search	Pg-Pub	08/21/2006	DWO
Update Interferecne Search		11/24/2006	DWO

AVAGO TECHNOLOGIES, LTD.
P.O. Box 1920
Denver, Colorado 80201-1920

ATTORNEY DOCKET NO. 70030259-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Lee et al.

Serial No.: 10/608,605 **Examiner:** Owens, Douglas W.

Filing Date: June 27, 2003 **Group Art Unit:** 2811

Title: PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

REQUEST FOR CONTINUED EXAMINATION (RCE) 37 CFR 1.114

Subsection (b) of 35 U.S.C. 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995.
See The American Inventors Protection Act of 1999 (AIPA).

Sir:

This is a Request for Continued Examination (RCE) under CFR 1.114 of the above-identified application.

NOTE: *37 CFR 1.114 is effective on May 20, 2000. If the above application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under CFR 1.53(d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice, Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1233 off. Gaz. Pat. Office 47 (Apr.11, 2000), which Established RCE practice.*

Submission under 37 CFR 1.114

☐ Previously submitted:
- ☐ Consider the amendment(s)/reply under 37 CFR 1.116 previously filed on
  (Any unentered amendment(s) referred to above will be entered).
- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on
- ☐ Other: Information Disclosure Statement

☒ Enclosed:
- ☐ Amendment/Reply
- ☐ Affidavit(s)/Declarations(s)
- ☒ Information Disclosure Statement (IDS)
- ☐ Other:

Miscellaneous

- ☐ Suspension of action is requested under 37 CFR 1.103(c) for a period of months.
  The fee for this Suspension is (37 CFR 1.17(i)) **$130.00**.
- ☐ Other:

☐ A Petition for Extension of Time

☐	One month	$120.00
☐	Two months	$450.00
☐	Three months	$1020.00
☐	Four months	$1590.00

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
The Director is hereby autorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No. 50-3718.

Respectfully submitted,
Lee et al.

By /Jay K. Malkin/

Attorney/Agent for Applicant(s)

Reg. No. 31,393

Date: January 29, 2007

Telephone No. (303) 298-9888

I hereby certify that this paper is being electronically transmitted to the Commissioner for Patents on the date shown below.

Date of Transmission: January 29, 2007

Typed Name: Joy Reinhart

Signature: /Joy Reinhart/

Form PTO-1449	ATTORNEY DOCKET NO.	SERIAL NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	70030259-1	11/608,605
	APPLICANT: Lee et al.	
(Use several sheets if necessary)	FILING DATE: June 27, 2003	GROUP: 2811

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL	*	DOCUMENT NUMBER	DATE	NAME
		2,907,925	October 6, 1959	Parsons
		5,440,075	August 8, 1995	Kawakita et al.
		2002/0179335	December 5, 2002	Curcio et al.
		2003/0168256	September 11, 2003	Chien

FOREIGN PATENT DOCUMENT

		DOCUMENT NUMBER	DATE	NAME	TRANSLATION YES	TRANSLATION NO

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

*** Copies of these references are not enclosed Pursuant to 37 CFR 1.98(d). (See accompanying IDS)**

[redacted]

Rev 10/03 (PTO 1449)

Electronic Patent Application Fee Transmittal

Application Number:	10608605
Filing Date:	27-Jun-2003
Title of Invention:	PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME
First Named Inventor/Applicant Name:	Kong Weng Lee
Filer:	Jay Kevin Malkin/Joy Reinhart
Attorney Docket Number:	70030259-1
Filed as Large Entity	

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	790	790
		Total in USD ($)		**790**

Electronic Acknowledgement Receipt

EFS ID:	1473907
Application Number:	10608605
International Application Number:	
Confirmation Number:	2253
Title of Invention:	PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME
First Named Inventor/Applicant Name:	Kong Weng Lee
Customer Number:	57299
Filer:	Jay Kevin Malkin/Joy Reinhart
Filer Authorized By:	Jay Kevin Malkin
Attorney Docket Number:	70030259-1
Receipt Date:	29-JAN-2007
Filing Date:	27-JUN-2003
Time Stamp:	17:41:55
Application Type:	Utility

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$790
RAM confirmation Number	830
Deposit Account	503718
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	RCEelectronicfiling.pdf	433589	no	2
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
2	Information Disclosure Statement (IDS) Filed	PTO1449.pdf	4676414	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8229	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	5118232		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 10/608,605

RCE Filed 4/20/10

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))						400	790
SEARCH FEE (37 CFR 1.16(k), (l), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	4 minus 20 = *		X =		OR	X =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 = *		X =			X =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	$1190.00

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

	Type	L #	Hits	Search Text	DBs
1	BRS	L1	116321	light adj emitting	USPAT
2	BRS	L2	180	1 and (mounting adj pad)	USPAT
3	BRS	L3	0	1 and (mounting adj pad)	US-PGPUB; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
4	BRS	L4	264237	light adj emitting	US-PGPUB; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
5	BRS	L5	120	4 and (mounting adj pad)	US-PGPUB; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
6	BRS	L6	0	("2004/0262738").URPN.	USPAT
7	BRS	L7	571	1 and (metalized near3 surface)	USPAT
8	BRS	L8	360	4 and (metalized near3 surface)	US-PGPUB; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

57299 7590 04/04/2007

AVAGO TECHNOLOGIES, LTD.
P.O. BOX 1920
DENVER, CO 80201-1920

EXAMINER	
CRANE, SARA W	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/04/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	06/27/2003	Kong Weng Lee	70030259-1	2253

TITLE OF INVENTION: PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	07/05/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

57299 7590 04/04/2007

AVAGO TECHNOLOGIES, LTD.
P.O. BOX 1920
DENVER, CO 80201-1920

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	06/27/2003	Kong Weng Lee	70030259-1	2253

TITLE OF INVENTION: PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	07/05/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
CRANE, SARA W	2811	257-690000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	06/27/2003	Kong Weng Lee	70030259-1	2253

57299 7590 04/04/2007

AVAGO TECHNOLOGIES, LTD.
P.O. BOX 1920
DENVER, CO 80201-1920

EXAMINER	
CRANE, SARA W	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/04/2007

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

Notice of Allowability	Application No. 10/608,605	Applicant(s) LEE ET AL.	
	Examiner Sara W. Crane	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *papers of 29 January 2007 (RCE filing)*.

2. ☒ The allowed claim(s) is/are 22-27.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 29 January 2007
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

The device structure as set forth in the claims is not taught or suggested in the prior art, including more specifically the light emitting diode having metallized bottom surface, mounted on a mounting pad, and having the relationship to the interconnecting element and conductive connecting pad as set forth in claim 1.

The references cited on form PTO 892 are similar in some ways to references already of record, showing LEDs having interconnecting elements extending through the underlying substrate to contact back surface electrodes.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to S. Crane, whose telephone number is (571) 272-1652.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sara W. Crane
Primary Examiner
Art Unit 2811

Form PTO-1449	ATTORNEY DOCKET NO.	SERIAL NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	70030259-1	11/608,605
	APPLICANT Lee et al.	
(Use several sheets if necessary)	FILING DATE June 27, 2003	GROUP 2811

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL	*	DOCUMENT NUMBER	DATE	NAME
/SC/		2,907,925	October 6, 1959	Parsons
/SC/		5,440,075	August 8, 1995	Kawakita et al.
/SC/		2002/0179335	December 5, 2002	Curcio et al.
/SC/		2003/0168256	September 11, 2003	Chien

FOREIGN PATENT DOCUMENT

		DOCUMENT NUMBER	DATE	NAME	TRANSLATION YES	TRANSLATION NO

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	/Sara Crane/	DATE CONSIDERED	03/29/2007

* Copies of these references are not enclosed Pursuant to 37 CFR 1.98(d). (See accompanying IDS)

[redacted]

Rev 10/03 (PTO 1449)

Notice of References Cited	Application/Control No. 10/608,605	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner Sara W. Crane	Art Unit 2811	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2002/0139990	10-2002	Suehiro et al.	257/99
*	B	US-5,177,593	01-1993	Abe, Munezo	257/98
*	C	US-7,098,593	08-2006	Teng, Ming-Ching	313/581
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Issue Classification	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/608,605	LEE ET AL.	
	Examiner	Art Unit	
	Sara W. Crane	2811	

ISSUE CLASSIFICATION

ORIGINAL CLASS	ORIGINAL SUBCLASS	CLASS	CROSS REFERENCE(S) SUBCLASS (ONE SUBCLASS PER BLOCK)						
257	99	257	690	784					
INTERNATIONAL CLASSIFICATION									
H01L	29/22								
	/								
	/								
	/								
	/								

(Assistant Examiner) (Date)

(Legal Instruments Examiner) (Date)

Sara Crane
Primary Examiner
(Primary Examiner) (Date) 3/29/07

Total Claims Allowed: 6

O.G. Print Claim(s)	O.G. Print Fig.
1	4E,4F

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		91		121		151		181
	2		32		62		92		122		152		182
	3		33		63		93		123		153		183
	4		34		64		94		124		154		184
	5		35		65		95		125		155		185
	6		36		66		96		126		156		186
	7		37		67		97		127		157		187
	8		38		68		98		128		158		188
	9		39		69		99		129		159		189
	10		40		70		100		130		160		190
	11		41		71		101		131		161		191
	12		42		72		102		132		162		192
	13		43		73		103		133		163		193
	14		44		74		104		134		164		194
	15		45		75		105		135		165		195
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	19		49		79		109		139		169		199
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	21		51		81		111		141		171		201
1	22		52		82		112		142		172		202
2	23		53		83		113		143		173		203
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4	25		55		85		115		145		175		205
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	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/608,605	LEE ET AL.	
	Examiner	Art Unit	
	Sara W. Crane	2811	

SEARCHED			
Class	Subclass	Date	Examiner
update: 257	690	3/07	SWC
	689		
	784		
257	99	3/07	SWC
	100		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
all above - included in search		PGPUBs text 3/27	SWC

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST see printout	3/07	SWC

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/608,605	LEE ET AL.
Examiner	**Art Unit**
Sara W. Crane	2811

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

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Claim		Date
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Claim		Date
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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

57299 7590 04/04/2007

AVAGO TECHNOLOGIES, LTD.
P.O. BOX 1920
DENVER, CO 80201-1920

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	06/27/2003	Kong Weng Lee	70030259-1	2253

TITLE OF INVENTION: PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	07/05/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
CRANE, SARA W	2811	257-690000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47, Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 .....
2 .....
3 .....

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Avago Technologies ECBU IP (Singapore) Pte. Ltd.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Singapore

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies .....

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-3712 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature Scott Weitzel
Date 07/05/2007
Typed or printed name Scott Weitzel
Registration No. 54534

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	10608605
Filing Date:	27-Jun-2003
Title of Invention:	PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME
First Named Inventor/Applicant Name:	Kong Weng Lee
Filer:	Scott Weitzel/Adrienne Barclay
Attorney Docket Number:	70030259-1

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1400	1400
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1700**

Electronic Acknowledgement Receipt

EFS ID:	1940428
Application Number:	10608605
International Application Number:	
Confirmation Number:	2253
Title of Invention:	PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME
First Named Inventor/Applicant Name:	Kong Weng Lee
Customer Number:	57299
Filer:	Scott Weitzel/Adrienne Barclay
Filer Authorized By:	Scott Weitzel
Attorney Docket Number:	70030259-1
Receipt Date:	05-JUL-2007
Filing Date:	27-JUN-2003
Time Stamp:	11:54:34
Application Type:	Utility

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$1700
RAM confirmation Number	4850
Deposit Account	503718
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	IssueFee.pdf	383904	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	8339	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	392243		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	08/14/2007	7256486	70030259-1	2253

57299 7590 07/25/2007

Kathy Manke
Avago Technologies Limited
4380 Ziegler Road
Fort Collins, CO 80525

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Kong Weng Lee, Penang, MALAYSIA;
Kee Yean Ng, Penang, MALAYSIA;
Yew Cheong Kuan, Penang, MALAYSIA;
Gin Ghee Tan, Penang, MALAYSIA;
Cheng Why Tan, Penang, MALAYSIA;

Small Entity Declaration

PATENT
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Current Date March 20, 2013

Patent Nos. Please see the attached.

CHANGE OF ENTITY STATUS PURSUANT TO 37 C.F.R. §1.27 (g)(2)

Commissioner for Patents
Mail Stop M Correspondence
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This communication hereby asserts that the attached Schedule A patents is entitled to small entity status.

Respectfully submitted,

COMPANY or FIRM NAME AND ADDRESS:

INTELLECTUAL DISCOVERY
135-090
Golden Tower 10F
#511 Samscong-ro, Gangnam-gu,
Seoul, Korea

Signature

Printed Name
CHO MIYOUNG

Title
Manager

OR

Reg. # if US Attorney_____

Schedule A – Patents assigned to *Assignee*

NO	APPLICATION NUMBER	FILING DATE	PATENT NUMBER	ISSUE DATE
20	10/071987	2002-02-08	6940102	2005-09-06
21	09/783101	2001-02-15	6943666	2005-09-13
22	10/128446	2002-04-23	6949771	2005-09-27
23	10/370435	2003-02-20	6967123	2005-11-22
24	10/374268	2003-02-25	7021807	2006-04-04
25	10/820342	2004-04-07	7066633	2006-06-27
26	10/609160	2003-06-27	7075225	2006-07-11
27	10/617626	2003-07-10	7075233	2006-07-11
28	10/649094	2003-08-26	7102177	2006-09-05
29	11/145140	2005-06-03	7105863	2006-09-12
30	10/798130	2004-03-11	7108413	2006-09-19
31	10/267759	2002-10-09	7112916	2006-09-26
32	11/075242	2005-03-07	7115428	2006-10-03
33	09/924653	2001-08-08	7129638	2006-10-31
34	10/661054	2003-09-12	7145182	2006-12-05
35	10/755047	2004-01-08	7183588	2007-02-27
36	10/833905	2004-04-27	7210817	2007-05-01
37	11/205580	2005-08-15	7230222	2007-06-12
38	10/798477	2004-03-11	7239080	2007-07-03
39	10/608605	2003-06-27	7256486	2007-08-14
40	10/789136	2004-02-27	7261441	2007-08-28

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	
Inventor: Kong Weng Lee	Confirmation No.: 2253
Serial No.: 10/608,605	Examiner: Crane, Sara W.
Filing Date: June 27, 2003	Group Art Unit: 2811
Patent No.: 7,256,486	
Issue Date: August 14, 2007	
Title: Packaging Device for Semiconductor Die, Semiconductor Device Incorporating Same and Method of Making Same	

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

NOTICE OF CHANGE OF STATUS TO SMALL ENTITY

Notice is hereby given under 37 C.F.R. § 1.27(g)(1) that effective at least as early as November 10, 2016, large entity status is no longer claimed by the assignee of the above-identified patent. The assignee asserts small entity status, and is entitled to claim small entity status for the purpose of calculating maintenance fees. To the extent any undiscounted fees were paid after the above-listed date, the assignee or a representative of the assignee will retroactively seek to pay the next maintenance fee at the small entity rate by requesting a refund of overpayment.

The practitioner signing below is authorized by the assignee to act in representative capacity under 37 C.F.R. 1.34 for purposes of filing this request only. Should the Office have any questions, the Office is invited to call the undersigned at (312) 913-3341.

McDonnell Boehnen Hulbert & Berghoff LLP
300 South Wacker Drive
Chicago, IL 60606
(312)913-0001

Respectfully submitted,

McDONNELL BOEHNEN
HULBERT & BERGHOFF LLP

Date: February 17, 2017

By: /Michael D. Clifford/
Michael D. Clifford
Reg. No. 60,550

McDonnell Boehnen Hulbert & Berghoff, Ltd.
300 South Wacker Drive, 7th Floor
Chicago, IL 60606
(312)913-0001

Electronic Acknowledgement Receipt	
EFS ID:	28396281
Application Number:	10608605
International Application Number:	
Confirmation Number:	2253
Title of Invention:	PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME
First Named Inventor/Applicant Name:	Kong Weng Lee
Customer Number:	57299
Filer:	Michael David Clifford
Filer Authorized By:	
Attorney Docket Number:	70030259-1
Receipt Date:	22-FEB-2017
Filing Date:	27-JUN-2003
Time Stamp:	19:09:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Assertion of entitlement to small entity status	7256486_SmallEntityStatus.pdf	75914 6ab265b9b045c7fe8986ac9d69117298c9d4ee5b	no	2

Warnings:

Information:	
Total Files Size (in bytes):	75914

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	
Inventor: Kong Weng Lee	Confirmation No.: 2253
Serial No.: 10/608,605	Examiner: Crane, Sara W.
Filing Date: June 27, 2003	Group Art Unit: 2811
Patent No.: 7,256,486	
Issue Date: August 14, 2007	
Title: Packaging Device for Semiconductor Die, Semiconductor Device Incorporating Same and Method of Making Same	

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

NOTIFICATION OF LOSS OF ENTITLEMENT TO SMALL ENTITY STATUS

Notice is hereby given under 37 C.F.R. § 1.27(g)(2) that small entity status is no longer claimed by the applicant for the above-identified patent. Applicant believed Applicant was entitled to small entity status when the previous change to small entity status was made. However, Applicant has now become aware of facts that make Applicant unsure as to whether Applicant is eligible for small entity status. Accordingly, large entity status is now claimed by the Applicant for the above-identified patent.

The practitioner signing below is authorized by the assignee to act in representative capacity under 37 C.F.R. 1.34 for purposes of filing this request only. Should the Office have any questions related to this request, the Office is invited to call the undersigned at (312) 913-3341.

McDonnell Boehnen Hulbert & Berghoff LLP
300 South Wacker Drive
Chicago, IL 60606
(312)913-0001

Respectfully submitted,

McDONNELL BOEHNEN
HULBERT & BERGHOFF LLP

Date: May 17, 2017

By: /Michael D. Clifford/
Michael D. Clifford
Reg. No. 60,550

McDonnell Boehnen Hulbert & Berghoff, Ltd.
300 South Wacker Drive, 7th Floor
Chicago, IL 60606
(312)913-0001

Electronic Acknowledgement Receipt

EFS ID:	29240822
Application Number:	10608605
International Application Number:	
Confirmation Number:	2253
Title of Invention:	PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME
First Named Inventor/Applicant Name:	Kong Weng Lee
Customer Number:	57299
Filer:	Michael David Clifford
Filer Authorized By:	
Attorney Docket Number:	70030259-1
Receipt Date:	22-MAY-2017
Filing Date:	27-JUN-2003
Time Stamp:	19:21:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Notification of loss of entitlement to small entity status	7256486_LargeEntityStatus.pdf	75649 14ee2a99856782c79bbe939ea744473268a25393	no	2

Warnings:

Information:	
Total Files Size (in bytes):	75649

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
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AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas, Marshall Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:17-cv-310	4/13/2017	Eastern District of Texas, Marshall Division

PLAINTIFF	DEFENDANT
Document Security Systems, Inc.	Everlight Electronics Co., Ltd. and Everlight Americas, Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,949,771 B2	9/27/2005	Document Security Systems, Inc.
2	7,524,087 B1	4/28/2009	Document Security Systems, Inc.
3	7,919,787 B2	4/5/2011	Document Security Systems, Inc.
4	7,256,486 B2	8/14/2007	Document Security Systems, Inc.
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:17-cv-309	4/13/2017	Eastern District of Texas, Marshall Division

PLAINTIFF	DEFENDANT
Document Security Systems, Inc.	Cree, Inc.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,949,771 B2	9/27/2005	Document Security Systems, Inc.
2 7,256,486 B2	8/14/2007	Document Security Systems, Inc.
3 7,279,355 B2	10/9/2007	Document Security Systems, Inc.
4 7,524,087 B1	4/28/2009	Document Security Systems, Inc.
5 7,919,787 B2	4/5/2011	Document Security Systems, Inc.

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

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AO 120 (Rev. 08/10)

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:17-cv-310	4/13/2017	Eastern District of Texas, Marshall Division

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Document Security Systems, Inc.	Everlight Electronics Co., Ltd. and Everlight Americas, Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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4	7,256,486 B2	8/14/2007	Document Security Systems, Inc.
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

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2:17-cv-309	4/13/2017	Eastern District of Texas, Marshall Division

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Document Security Systems, Inc.	Cree, Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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2	7,256,486 B2	8/14/2007	Document Security Systems, Inc.
3	7,279,355 B2	10/9/2007	Document Security Systems, Inc.
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AO 120 (Rev. 08/10)

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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court California District Court - So Div on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
17cv00981	6/7/2017	California District Court - So Div

PLAINTIFF	DEFENDANT
Document Security Systems	Seoul Semiconductor Co.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,256,486		
2	6,949,771		
3	7,524,087		
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court California Central District Court on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
17cv04263	6/8/2017	California Central District Court

PLAINTIFF	DEFENDANT
Docuemtn Security Systems	Cree, Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,949,771		
2	7,256,486		
3	7,279,355		
4	7,524,087		
5	7,919,787		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

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DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
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AO 120 (Rev. 08/10)

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Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court California Central District Court on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
17cv04273	6/8/2017	California Central District Court

PLAINTIFF	DEFENDANT
Document Security Systems	Everlight Electronics

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,949,771		
2	7,524,087		
3	7,919,787		
4	7,256,486		
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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AO 120 (Rev. 08/10)

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Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas, Marshall Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:17-cv-309	4/13/2017	Eastern District of Texas, Marshall Division

PLAINTIFF	DEFENDANT
Document Security Systems, Inc.	Cree, Inc.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
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PLAINTIFF	DEFENDANT
Document Security Systems, Inc.	Everlight Electronics Co., Ltd. and Everlight Americas, Inc.

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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Central District of California on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:17-cv-05184	7/13/2017	Central District of California

PLAINTIFF	DEFENDANT
Document Security Systems, Inc.	OSRAM GmbH; OSRAM Opto Semiconductors GmbH & Co.; and OSRAM Sylvania Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,949,771	9/27/2005	Document Security Systems, Inc.
2	7,524,087	10/28/2009	Document Security Systems, Inc.
3	7,256,486	8/14/2007	Document Security Systems, Inc.
4	7,652,297	1/26/2010	Document Security Systems, Inc.
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**