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Chu et al.

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[54] **MULTI-VOLTAGE CIRCUIT ARRANGEMENT AND METHOD FOR ACCOMMODATING HYBRID ELECTRONIC SYSTEM REQUIREMENTS**

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[21] Appl. No.: **320,438**

[22] Filed: **Oct. 7, 1994**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 129,990, Sep. 29, 1993.

[51] **Int. Cl.**[6] **H03K 19/0175**; G05F 1/00

[52] **U.S. Cl.** **327/519**; 326/80; 326/63

[58] **Field of Search** 326/80, 81, 63; 327/519, 547

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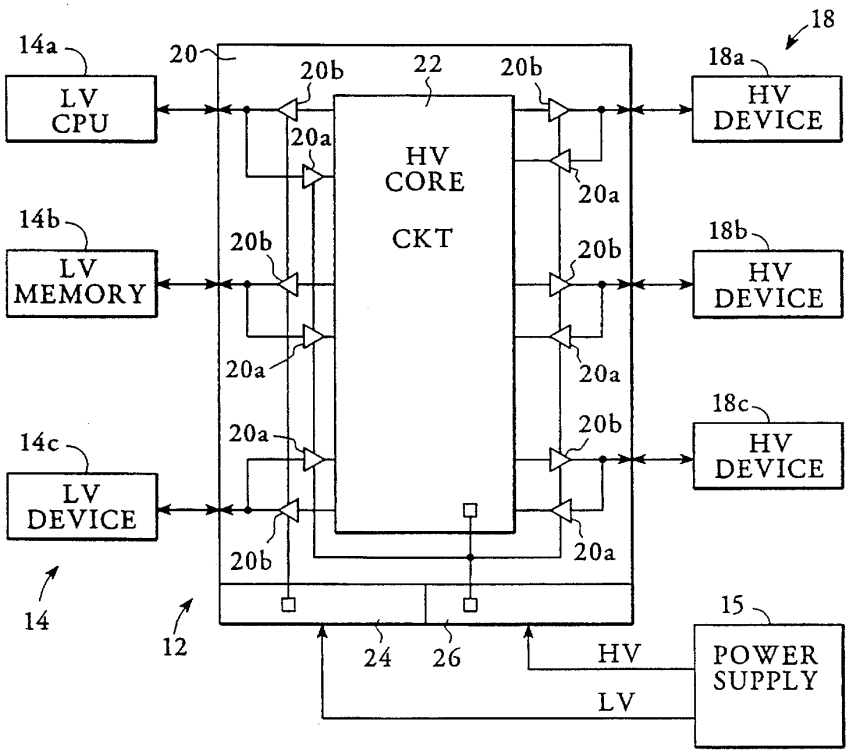
[57] **ABSTRACT**

A multi-voltage circuit on a semiconductor chip including core circuitry driven by a power supply voltage equal to the voltage of a selected external device operating in connection with the semiconductor chip, and having input/output circuitry in selected regions for operating in connection with external devices having the same operating voltage and other external devices having a selected substantially lower operating voltage. Peripheral input/output circuit regions of at least first and second kinds are established for interfacing with the respective high and low voltage external devices. According to one version of the invention, the input/output circuitry directed toward interfacing with external devices operating at a particular voltage level is concentrated at a particular peripheral region in the periphery of the semiconductor chip. According to another version of the invention, multiple regions of input/output circuitry are established for external devices at the same voltage level. These multiple regions may be configured by the system designer to operate with any combination of high voltage and low voltage external devices.

14 Claims, 3 Drawing Sheets



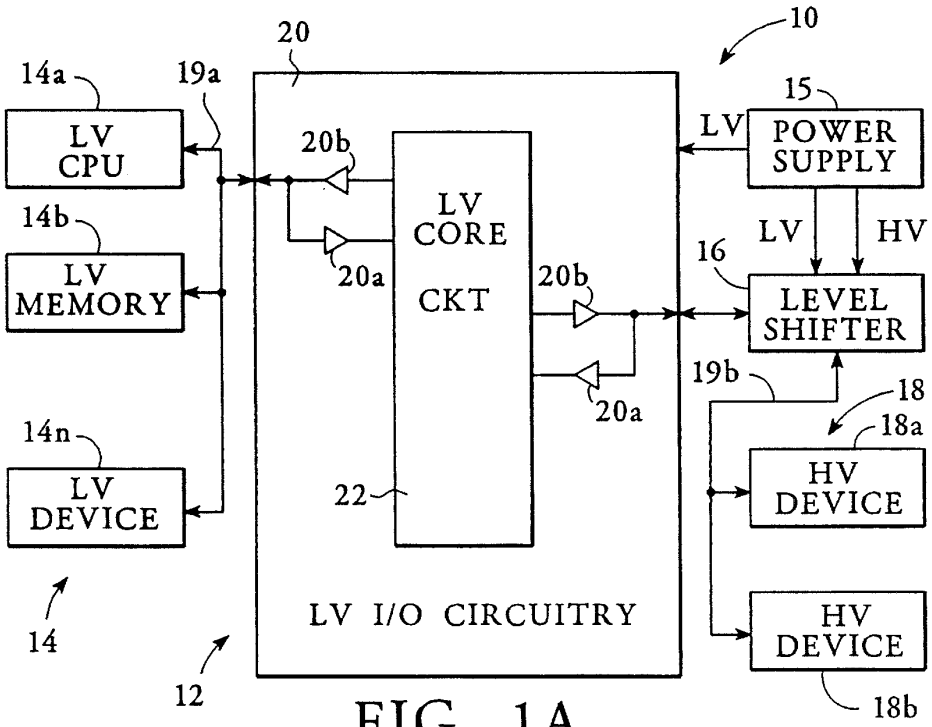


FIG. 1A
(PRIOR ART)

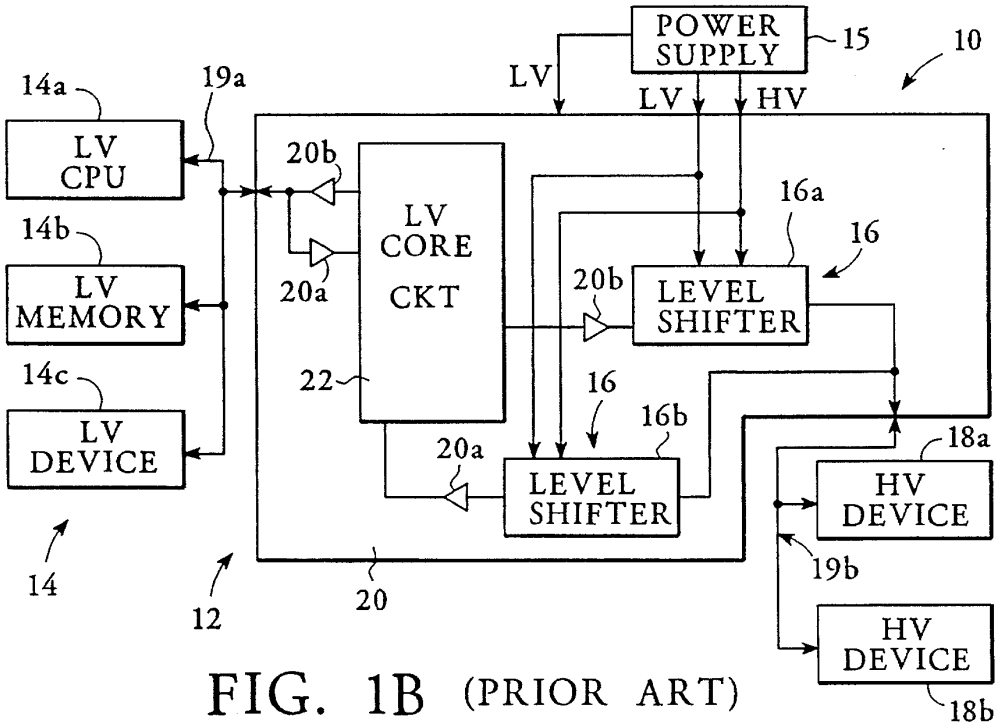


FIG. 1B (PRIOR ART)

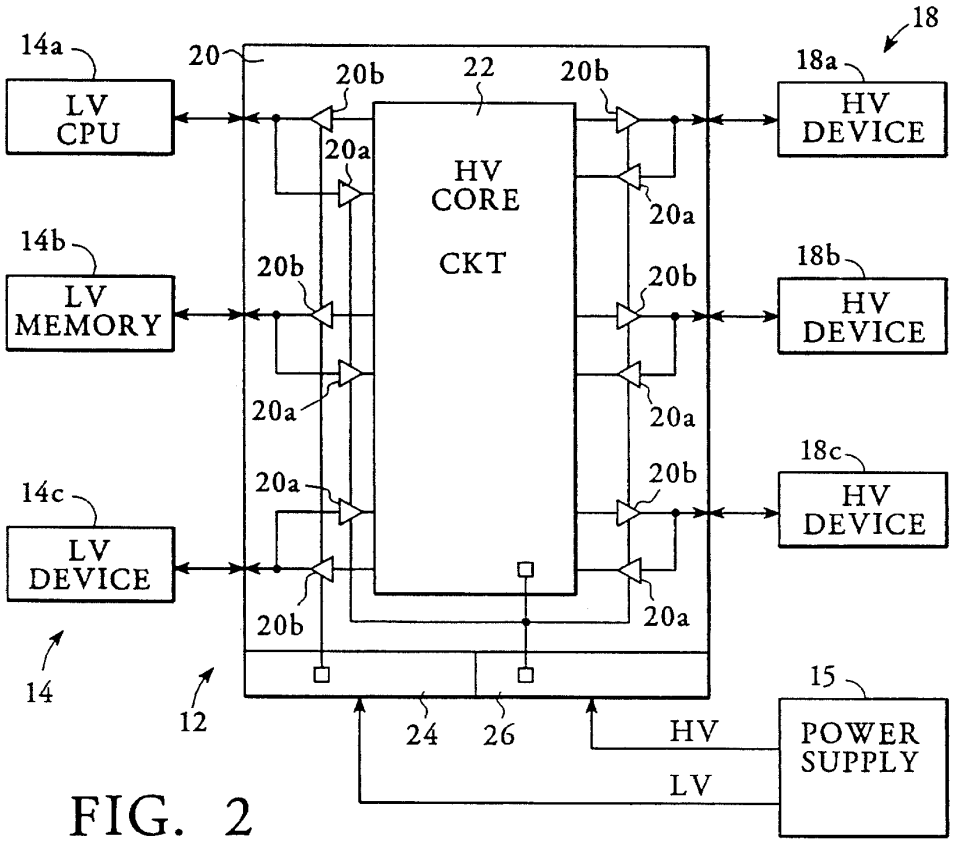


FIG. 2

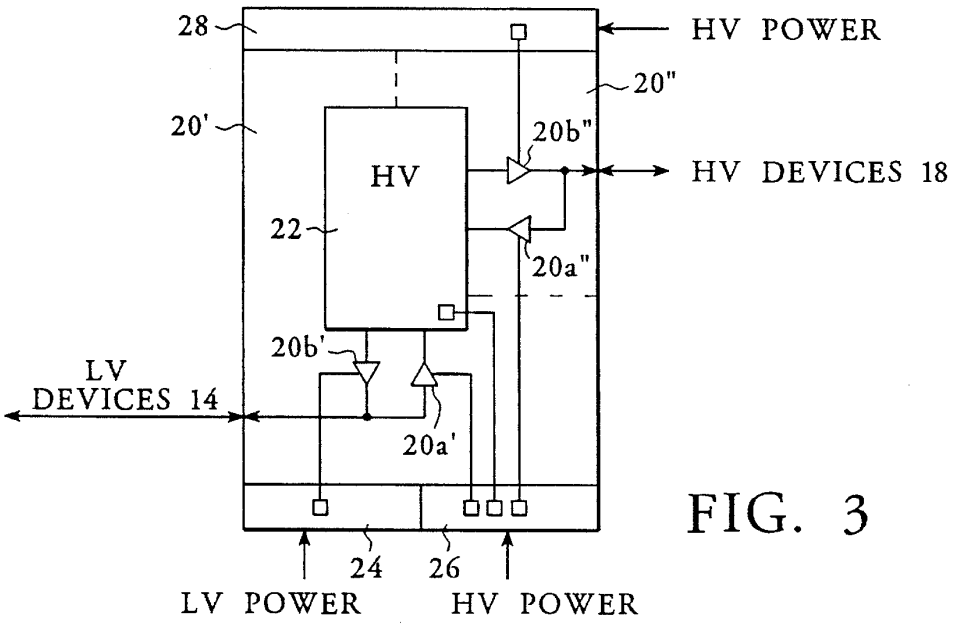


FIG. 3

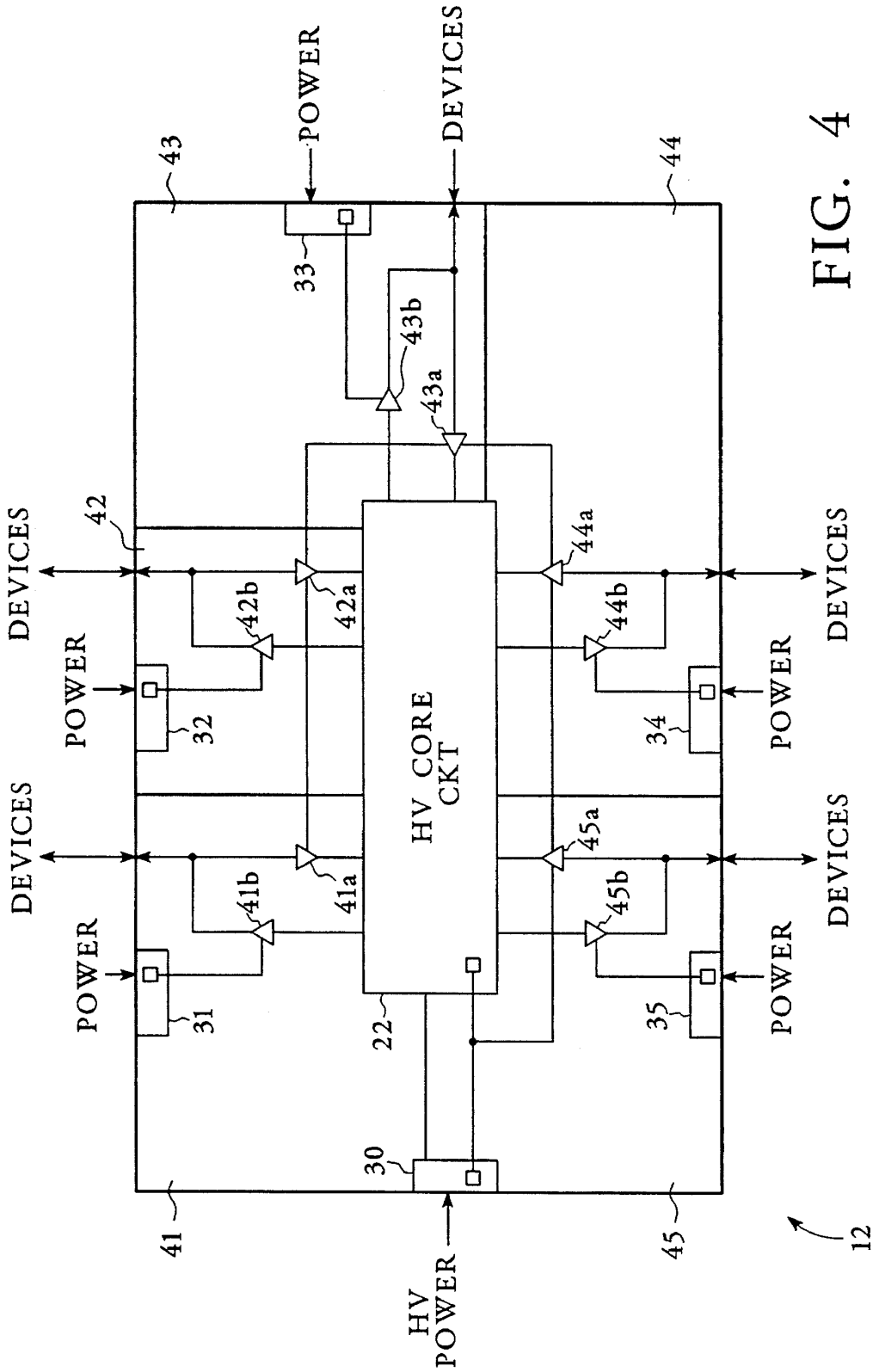


FIG. 4

MULTI-VOLTAGE CIRCUIT ARRANGEMENT AND METHOD FOR ACCOMMODATING HYBRID ELECTRONIC SYSTEM REQUIREMENTS

CROSS REFERENCE TO RELATED APPLICATION

This application is a continuation in part of application Ser. No. 08/129,990, filed Sep. 29, 1993.

TECHNICAL FIELD

The field of this invention is that of multi-voltage circuit arrangements and methods, and more particularly multi-voltage circuit arrangements and methods for accommodating hybrid system requirements.

BACKGROUND OF THE INVENTION

Semiconductor technology is increasingly being driven by market demand for low-power, portable computer systems. Such computer systems include a range of new products directed toward laptop, palmtop and pen-based computers. The effects of this market influence include a strong tendency to increasingly rely upon lower voltage integrated circuits (IC's) and application specific integrated circuits (ASIC's). These low voltage devices help to extend the battery life of the particular systems in which they are used. However, this extended battery life is obtained at the cost of system performance. For example, the delay through a semiconductor device is dependent upon a number of parameters, including the supply voltage. As the supply voltage decreases, the overall speed of the device diminishes. Another concern when using low voltage devices is the reality that existing components such as expansion cards, disk drives and other external devices are built using components that operate at the higher voltage levels. Thus, low voltage devices must include additional circuitry known as level shifters to accommodate pre-existing high voltage devices.

FIG. **1**A shows a multi-voltage circuit arrangement according to the prior art. In particular, FIG. **1**A schematically illustrates a hybrid multi-chip circuit system **10**, including a semiconductor chip **12** and peripheral devices such as external low voltage devices **14**, a power supply **15**, a level shifter **16** and external high voltage devices **18**. The semiconductor chip **12** is a low voltage device in the sense that it is powered by a semiconductor chip power supply having a voltage level lower than the power supply voltage level of some of the peripheral devices to which the semiconductor chip **12** is connected. Currently, many peripheral devices are preferably powered at either 5 volts or 3.3 volts DC. An example of a high voltage device **18** would accordingly be a device which relies upon a 5 volt power supply, while a low voltage device would be a device which is powered by a 3.3 volt power supply. A range of low voltage devices **14***a*–**14***c* are shown in FIG. **1**A. These devices include a low voltage central processing unit (CPU) **14***a*, a low voltage memory **14***b* and a generic low voltage device **14***c*. Similarly, FIG. **1**A shows a plurality of different kinds of high voltage input/output devices **18**, respectively **18***a* and **18***b*. A power supply **15** provides high voltage (HV) power and low voltage (LV) power to a level shifter **16**, and low voltage power to the semiconductor chip **12**.

In the case of the prior art multi-chip circuit system **10** shown in FIG. **1**A, the low voltage devices **14** are directly connected to a semiconductor chip **12** through a suitable bus

19*a*, and the high voltage devices **18** are directly connected to the level shifter **16**, which in turn is connected to the semiconductor chip **12**. The level shifter **16** is a well-known interface device which is effective for receiving output signals from the semiconductor chip **12** and conveying these signals to the high voltage devices **18**. The level shifter **16** is further effective for receiving input signals from high voltage devices **18** to be conveyed to the semiconductor chip **12**. The level shifter **16** is connected to the high voltage devices **18** along a bus **19***b*. Busses **19***a* and **19***b* can connect one or more devices to the semiconductor chip **12**. A bus can further be a serial or parallel electrical connection having a plurality of electric lines.

The semiconductor chip **12** in the prior art of FIG. **1**A includes a region of low voltage input/output circuitry **20** and a region of low voltage core circuitry **22** connected to the low voltage input/output circuitry **20**. The low voltage core circuitry **22** includes, for example, logic circuitry and memory circuitry for performing a variety of selected operations with respect to a range of external devices and systems. The low voltage input/output circuitry **20** includes input buffers **20***a* and output buffers **20***b*. The semiconductor chip **12** is completely unitary in that all of its regions are powered by the same voltage supply level, which is low compared to a high voltage level being employed to power a selected one or more of high voltage devices **18**.

FIG. **1**B shows another version of the prior art, according to which the level shifters **16** are integrated into the semiconductor chip **12**, as opposed to being off chip as shown in FIG. **1**A. According to this version of the prior art, a level shifter **16***b* serves to convert the low voltage output of the low voltage core circuitry **22** to a sufficiently high voltage to drive the high voltage devices **18***a* and **18***b*. Conversely, the level shifter **16***a* converts the high voltage output of the high voltage devices **18***a* and **18***b* to the low voltage level required by the low voltage core circuitry **22**. With the exception of the level shifters **16***a* and **16***b*, the semiconductor chip **12** is supplied with low voltage power (LV) from the power supply **15**. The level shifters **16***a* and **16***b* are provided with both low voltage power (LV) and high voltage power (HV).

Unfortunately, the use of the level shifters **16***a* and **16***b*, whether integrated into the semiconductor chip **12** or used as a separate, discrete element external to the semiconductor chip **12**, tends to increase costs significantly. In the case of the external level shifter **16** of FIG. **1**A, the increased cost includes the cost of the additional component, a reduction in reliability as a result of an additional connection which may fail and added expense in terms of an opportunity cost since available space is consumed which might effectively have been employed in a more worthwhile fashion. In the case of the on-chip level shifters **16***a* and **16***b* of FIG. **1**B, the same loss of space detriment is suffered, except that the space relates to available chip topography, rather than real estate consumed on a chip carrier or circuit board. An additional cost is the design cost in customizing the semiconductor chip **12** to include the level shifters **16***a* and **16***b* as part of the internal circuitry of the semiconductor chip **12**.

It is therefore desirable to have a high voltage semiconductor device which is comparable to the low voltage devices, such as the semiconductor chip **12** of the prior art of FIGS. **1**A and **1**B, in terms of power conservation, while at the same time obviating the need for the level shifters **16**. Such high voltage semiconductor devices would also have speed advantages over the low voltage devices, being operable at a higher voltage. The present invention takes advantage of the fact that the most power hungry logic is the

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