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[54] **CIRCUIT THAT AUTOMATICALLY SWITCHES BETWEEN SUPPLYING A MICROPROCESSOR WITH A FIRST VOLTAGE AND A SECOND VOLTAGE**

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[52] **U.S. Cl.** **395/750**; 326/68

[58] **Field of Search** 395/750; 364/492, 364/707; 323/304, 313, 314, 909; 326/68

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[57] **ABSTRACT**

A circuit that automatically switches the power supply voltage PVDD provided to a CPU between 3.3 volts and 5 volts. The circuit detects whether the CPU installed in a socket is a 3.3-volt part or a 5-volt part by determining the state of a voltage detect sense pin provided by the socket. If the voltage detect sense pin is driven low, that indicates a 3.3-volt CPU is being used. If a 5-volt CPU is installed, the voltage detect sense pin is left floating by the CPU, which allows a pullup resistor to pull the voltage detect sense pin high. The power supply voltage provided to the CPU is regulated through a power field effect transistor (FET). The gate of the power FET is connected to the output of a voltage reference source and is coupled to a 12-volt supply signal. If the voltage detect sense pin is pulled high, the voltage reference source is turned off, allowing the 12-volt supply signal to drive the gate of the power FET. This in turn allows the power FET to pass a 5-volt supply signal to the CPU supply signal PVDD. If the voltage detect sense pin is pulled low, the voltage reference source is turned on to drive the gate of the power FET to approximately one threshold voltage above 3.3 volts. In response, the power FET passes only 3.3 volts to the CPU supply signal PVDD.

18 Claims, 2 Drawing Sheets

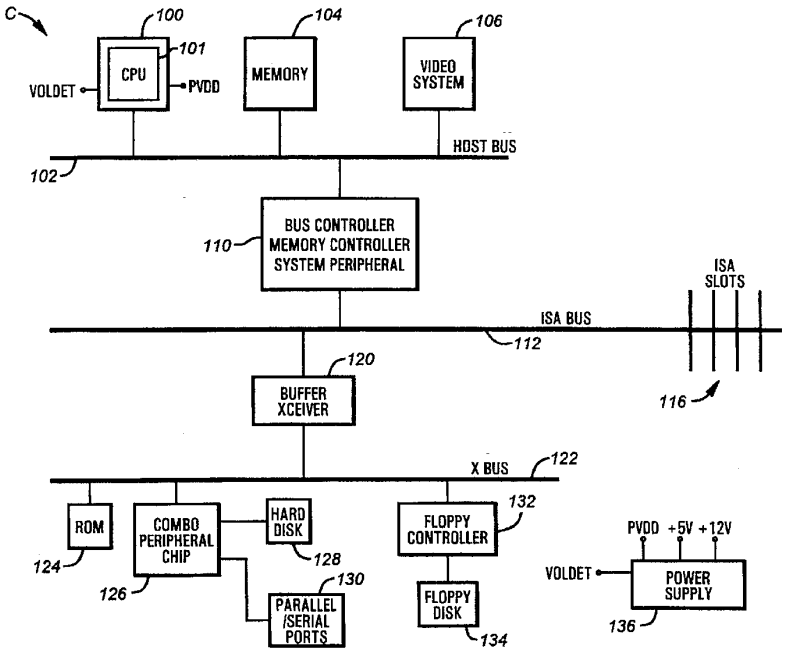
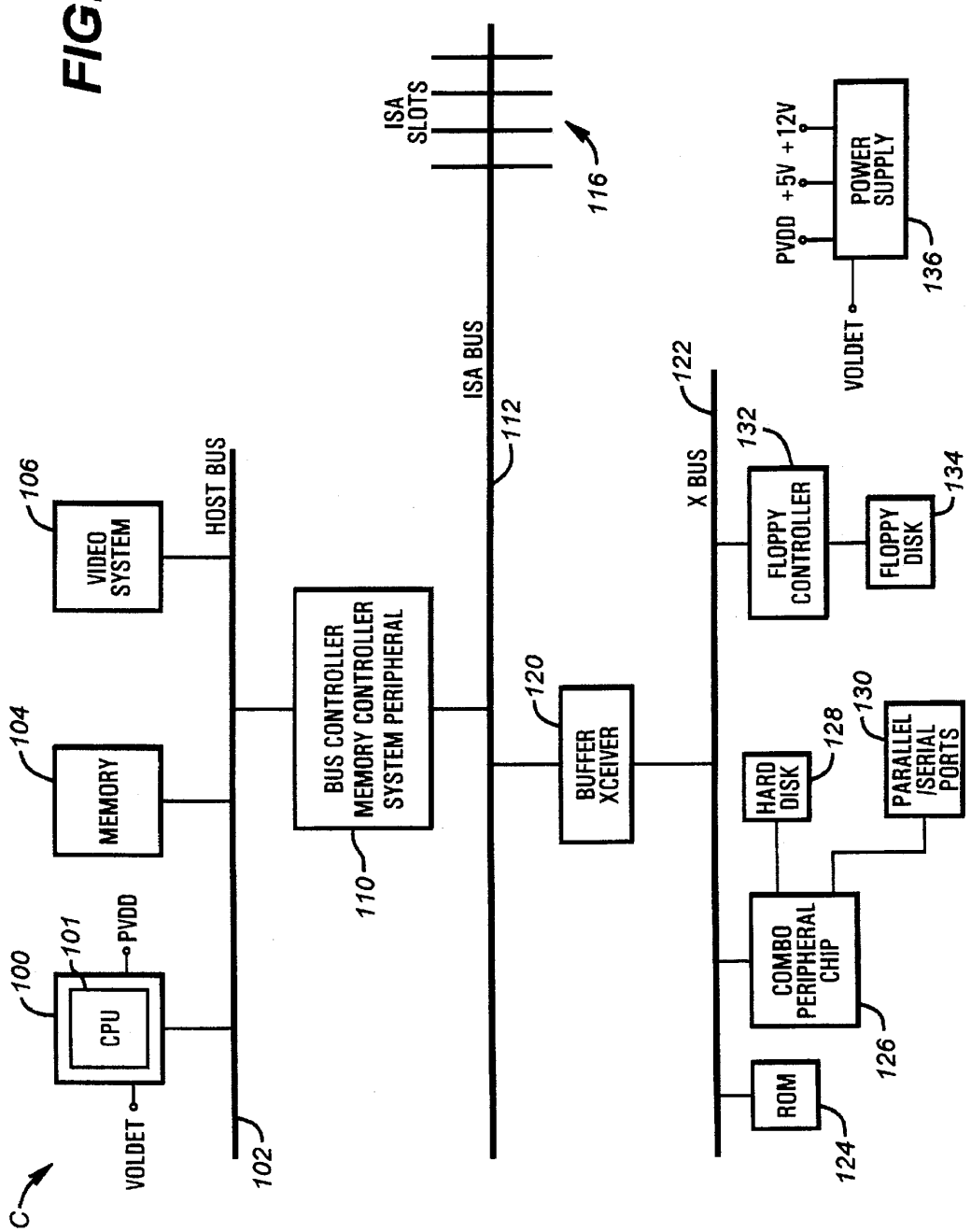


FIG. 1



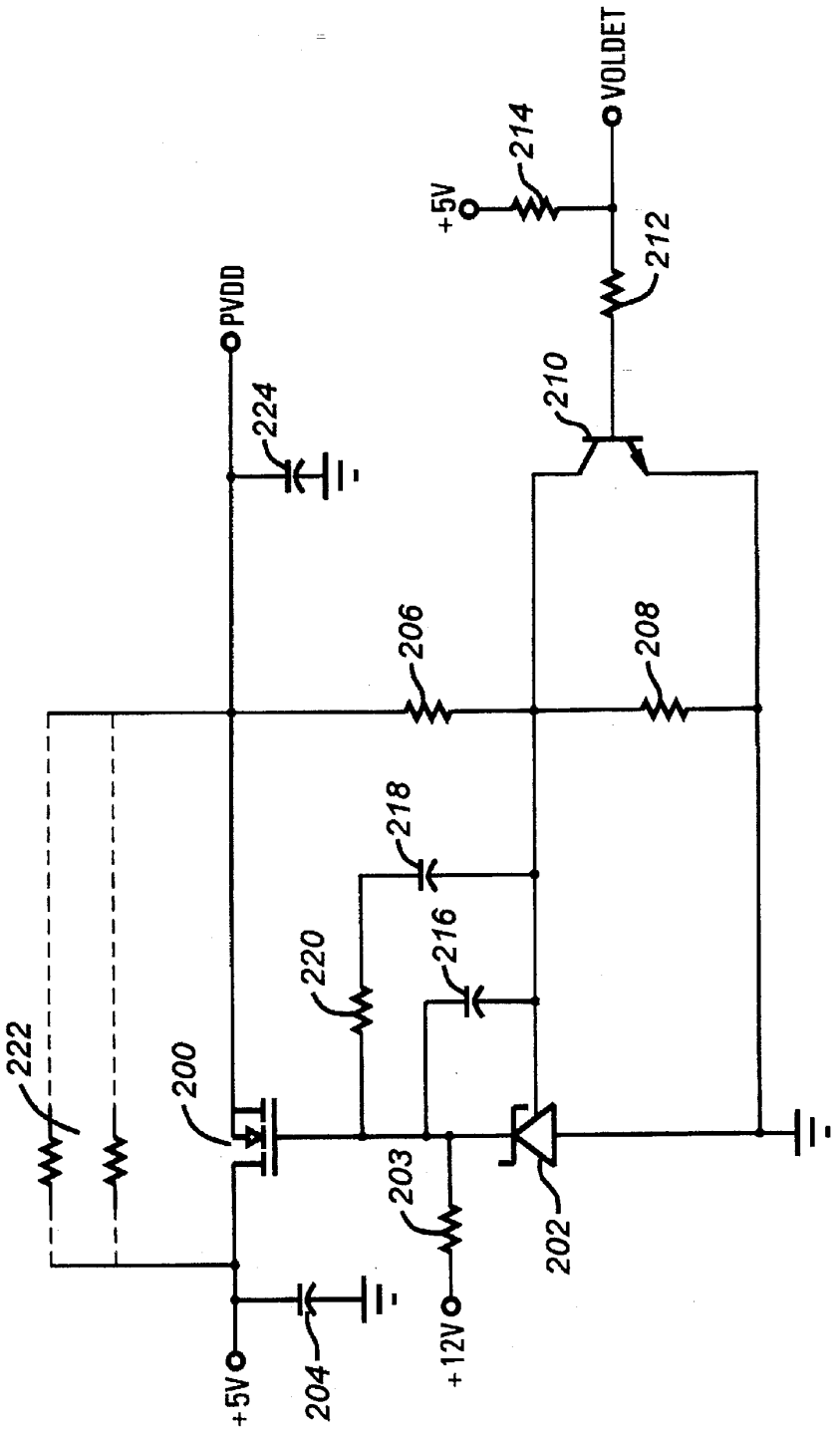


FIG. 2

CIRCUIT THAT AUTOMATICALLY SWITCHES BETWEEN SUPPLYING A MICROPROCESSOR WITH A FIRST VOLTAGE AND A SECOND VOLTAGE

BACKGROUND OF THE INVENTION

1. Field of the invention

The invention relates to controlling a power supply voltage provided to a microprocessor, and more particularly, to a circuit that automatically switches between supplying the microprocessor with a first voltage or a second voltage.

2. Description of the Related Art

Over the past decade, the performance and speed of microprocessors have improved dramatically. The number of transistors that can be fitted onto a microprocessor chip number is in the millions. Such densities are allowed primarily with the use of complementary metal oxide silicon (CMOS) technology, which allows for significantly lower power consumption over prior bipolar and NMOS technologies. However, even with the use of CMOS technology, power dissipation by today's high performance microprocessors is a significant problem. To reduce power consumption, microprocessors such as the **486**SL and Pentium® CPUs from Intel Corporation include built-in power management functions. The energy efficient CPUs include a stop clock and auto halt mode. In stop clock mode, the clock speed of the microprocessor can be reduced or even stopped altogether, which reduces the power dissipation of the microprocessor when it is idle. The CPU enters into the auto halt mode after execution of a halt instruction. This allows the microprocessor to be placed into low power mode via software.

Neither of the above features, however, address how the power consumption of a microprocessor can be reduced while it is active. One popular method of reducing power consumption while the microprocessor is running is to reduce its power supply voltage from the industry standard 5 volts down to 3.3 volts. Lower voltages have also proved to be necessary as die sizes continue to shrink. The small dimensions that exist on a chip require a lower operating voltage to avoid problems associated with high current densities. With the trend towards 3.3 volt microprocessors chip manufacturers have had to provide both microprocessors that operate at 5 volts and 3.3 volts.

This presents the computer manufacturers with a problem, however, as the computer system must be capable of providing two different power supply voltages to the microprocessor. One solution is to include a 5-volt power supply voltage on all computer systems, adding a conventional regulator for providing a 3.3 volt power supply voltage in the 3.3-volt computer systems. However, this requires that the manufacturing process be different for 3.3-volt and 5-volt computer systems. Single-part solutions exist where the same part can be used with both 3.3-volt and 5-volt microprocessors. However, these parts include linear regulators, which are relatively expensive components. Thus the use of the separate, conventional linear regulator is undesirable, as it adds cost to the manufacture of the computer systems for several reasons.

SUMMARY OF THE PRESENT INVENTION

It is an object of the present invention to provide a low-cost power supply control circuit that can be used with microprocessors that operate at either a first or second supply voltage. The power supply control circuit according to the present invention includes regulator circuitry that selectively provides a microprocessor supply voltage at a first voltage or a second voltage, those voltages preferably being 3.3 volts and 5 volts, respectively. The computer system preferably includes a socket for receiving a microprocessor, and the socket includes a pin referred to as the voltage detect sense pin. Microprocessors operating at 3.3 volts drive the voltage detect sense pin low, whereas 5-volt microprocessors leave the voltage detect sense pin floating, allowing a pullup resistor to pull the pin high. The voltage detect sense pin from the microprocessor socket is connected to the regulator circuitry in the power supply control circuit. The regulator circuitry includes a power field effect transistor (FET), whose drain is preferably connected to a 5-volt source, and whose source provides the power supply voltage to the microprocessor. The gate of the power FET **200** in the preferred embodiment is connected to a voltage reference source, which drives the gate of the power FET to approximately 12 volts if the voltage detect sense pin is pulled high by the pullup resistor, and which drives the gate to one threshold voltage of the power FET above 3.3 volts if the sense pin is driven low. Thus, if the voltage detect sense pin is pulled low, the power FET drives the microprocessor supply voltage to 3.3 volts. Otherwise, if the voltage detect sense pin is pulled high, the power FET is completely turned on and allows the 5-volt voltage to pass to the microprocessor supply voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the present invention can be obtained when the following detailed description of **5** the preferred embodiment is considered in conjunction with the following drawings, in which:

FIG. **1** is an exemplary computer system incorporating the power supply control circuit according to the present invention; and

FIG. **2** is a schematic diagram of portions of the power supply control circuit of Figure I that regulates the voltage provided to a microprocessor in the computer system.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIG. **1**, an exemplary computer system C incorporating a power supply control circuit according to the present invention is shown. The computer system C includes a socket **100** for receiving a host CPU or processor **101**, which is conventionally a microprocessor such as a 486 or Pentium® processor from Intel Corporation. It is contemplated that instead of using the socket **100**, the CPU **101** can be directly soldered to the motherboard. The type of microprocessors that can be used with the computer system C include the 486SX, 486DX, 486DX2, 487SX, 486DX4, and Pentium® P24T processors. In addition, microprocessors from other manufacturers compatible with the **486** processor can also be used. The 486SX, 486DX, 486DX2, and P24T processors operate at 5 volts, while the 486DX4 operates at 3.3 volts. Certain of the microprocessors from the other manufacturers also operate at 3.3 volts. The socket **100** receives a pin or plurality of pins PVDD, which is the microprocessor power supply pin or pins driven to 5 volts or 3.3 volts, depending on which microprocessor is used. The socket **100** also includes a voltage detect sense pin VOLDET. When a 3.3-volt microprocessor is inserted into the socket **100**, the microprocessor drives the pin VOLDET low. If a 5-volt microprocessor is inserted, the pin VOLDET is left floating.

A host bus **102** is connected to the CPU **101** to act as a first bus in the computer system C. A main memory system **104** is also connected to the host bus **102** to act as the main memory of the computer system C. A video system **106** is further connected to the host bus **102** to allow for a high performance video system.

A controller **110** is connected between the host bus **102** and an ISA or Industry Standard Architecture bus **112**. The controller **110** includes a bus controller portion, a memory controller portion and a system peripheral control portion. The system peripheral control portion includes certain common peripheral devices used in the computer system C such as timers, an interrupt controller, and a DMA controller. The bus controller portion of the controller **110** controls bus cycles on the host bus **102** and the ISA bus **112**. The memory controller portion provides appropriate signals to the memory **104**, which preferably is made up of dynamic random access memories (DRAMs). A number of ISA slots **116** for receiving interchangeable circuit cards are present on the ISA bus **112**.

Appropriate buffer and transceiver logic **120** is connected between the ISA bus **112** and an X bus **122**, which forms an additional input/output (I/O) bus in the computer system C. A read-only memory or ROM **124**, which contains the instructions forming the BIOS and other fundamental operations, is connected to the X bus **122**. A combo peripheral chip **126** is also connected to the X bus **122**. The combo peripheral chip **126** includes a keyboard controller to receive keyboard and pointing device inputs from a user, an interface for connection to parallel and serial ports **130** to provide for certain I/O capabilities, and a hard disk controller for interfacing to a hard disk drive **128**. The combo peripheral chip **136** also includes a real-time clock (RTC) and basic and extended CMOS memory. The RTC provides various real-time clock functions, and the CMOS memory provides storage for various system configuration information. Additionally, a floppy disk controller **132** is connected to the X bus **122**. The floppy disk controller **132** acts as an interface between the X bus **122** and a floppy disk drive **134**.

A power supply circuit **136** is also located in the computer system C. The outputs provided by the power supply circuit **136** include a 12-volt supply signal +12 V, a 5-volt supply signal +5 V, and the supply signal PVDD, which varies between 3.3 volts and 5 volts depending on the type of the CPU **101** used. The voltage detect sense pin VOLDET is provided to the power supply circuit **136**. The power supply signal PVDD is provided to the CPU **101**, and in accordance with the present invention, is automatically set at 3.3 volts or 5 volts depending on the state of the pin VOLDET.

Referring now to FIG. **2**, regulator circuitry in the power supply circuit **136** for generating the supply signal PVDD is shown. The regulator circuitry includes a power n-channel enhancement field effect transistor (FET) **200**, whose drain is connected to the supply signal +5 V and whose source is connected to the supply signal PVDD. A decoupling capacitor **204** is connected between the drain of the power FET **200** and ground to remove high frequency noise. Decoupling and bulk capacitors **224** are connected to the supply signal PVDD to maintain the voltage level at PVDD stable. The gate of the power FET **200** is connected to the output pin of a voltage reference source **202**. Any one of the standard voltage reference source chips generally available can be used, provided that the reference voltage is as described below, though the TL**431** is preferred. The gate of the power FET **200** is also coupled to the supply signal +12 V through a resistor **203**. The reference input of the voltage reference source **202** is connected to the collector of a bipolar junction transistor (BJT) **210**, and the ground pin of the voltage reference source **202** is connected to ground. The emitter of the BJT **210** is connected to ground and its base is coupled to the voltage detect sense pin VOLDET through a resistor **212**. A pullup resistor **214** is connected between the voltage detect sense pin VOLDET and the supply signal +5 V. When a 5-volt CPU **101** is placed into the socket **100**, the sense pin VOLDET is left floating. As a result, the pullup resistor **214** is able to pull the sense pin VOLDET to 5 volts. If a 3.3-volt CPU **101** is inserted into the socket **100**, then the sense pin VOLDET is driven low by the CPU **101**.

A resistor **206** is connected between the source of the power FET **200** and the collector of the BJT **210**. Another resistor **208** is connected between the collector of the BJT **210** and ground. The resistors **206** and **208** form a voltage divider circuit to provide a voltage at their common node based on the voltage of the supply signal PVDD. In addition, a capacitor **216** is connected between the output pin and the reference pin of the reference voltage source **202**. One side of a resistor **220** is also connected to the output pin of the voltage reference source **202**, and the other side of the resistor **220** is connected to one side of a capacitor **218**. The other side of the capacitor **218** is connected to the reference pin of the voltage reference source **202**. The capacitors **216** and **218** and the resistor **220** function to stabilize the voltage generated on the output pin of the voltage reference source **202**. Any noise glitch occurring on the reference pin of the voltage reference source **202** is filtered by the combination of the resistor **220** and the capacitors **216** and **218**.

If the sense pin VOLDET is pulled high by the resistor **214**, the BJT **210** is turned on, thereby pulling the reference pin of the voltage reference source **202** to approximately the collector-to-emitter saturation voltage of the BJT **210**, which is approximately 0.2 to 0.3 volts. This turns the voltage reference source **202** off, which allows the supply signal +12 V to drive the gate of the power FET **200** to approximately 12 volts. As a result, the voltage of the supply signal +5 V completely passes through the power FET **200** to drive the supply signal PVDD to 5 volts.

If a 3.3-volt CPU **101** is installed and the sense pin VOLDET is driven low, the BJT **210** is turned off. As a result, the voltage provided to the reference pin of the voltage reference source **202** is developed by the voltage divider formed from the resistors **206** and **208**. The voltage at the reference pin of the voltage reference source **202** is thus dependent upon the power supply voltage PVDD. At steady state, the voltage at the reference pin of the voltage reference source **202** is driven to about 2.5 volts. In response to this voltage, the voltage reference source **202** drives the gate of the power FET **200** to approximately one threshold voltage (V_T) above 3.3 volts. The threshold voltage V_T of the power FET **200** ranges from 3 to 10 volts. Consequently, due to the gate-to-source threshold voltage Vof the power FET **200**, the voltage at the source of the power FET **200** is limited to approximately 3.3 volts. A feedback path exists from the regulated supply signal PVDD through the resistor **206** to the reference pin of the voltage reference source **202**, which allows the supply signal PVDD to be maintained at a relatively stable 3.3 volts.

Optional zero ohm resistors **222** are inserted between the supply signal +5 V and the supply signal PVDD when the power FET **200** and all its associated circuitry are not installed. When optional resistors **222** are used instead of the power FET **200**, the computer system C can be used only with 5-volt microprocessors.

Thus, a circuit has been described that automatically switches the power supply voltage provided to a CPU,

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