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Albertsen

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[54] **METHOD OF TESTING A READ-ONLY MEMORY AND DEVICE FOR PERFORMING THE METHOD**

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[51] **Int. Cl.**[5] **G06F 11/00**; G11C 29/00

[52] **U.S. Cl.** **371/21.1**; 371/16.1; 371/16.2

[58] **Field of Search** ..... 371/16.1, 16.2, 21.1; 364/200 MS File, 900 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,334,307	6/1982	Bourgois et al.	371/16.1
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4,777,586	10/1988	Matsubara et al.	369/200
4,868,822	9/1989	Scott et al.	371/16.2
4,933,941	6/1990	Eckard et al.	371/16.2

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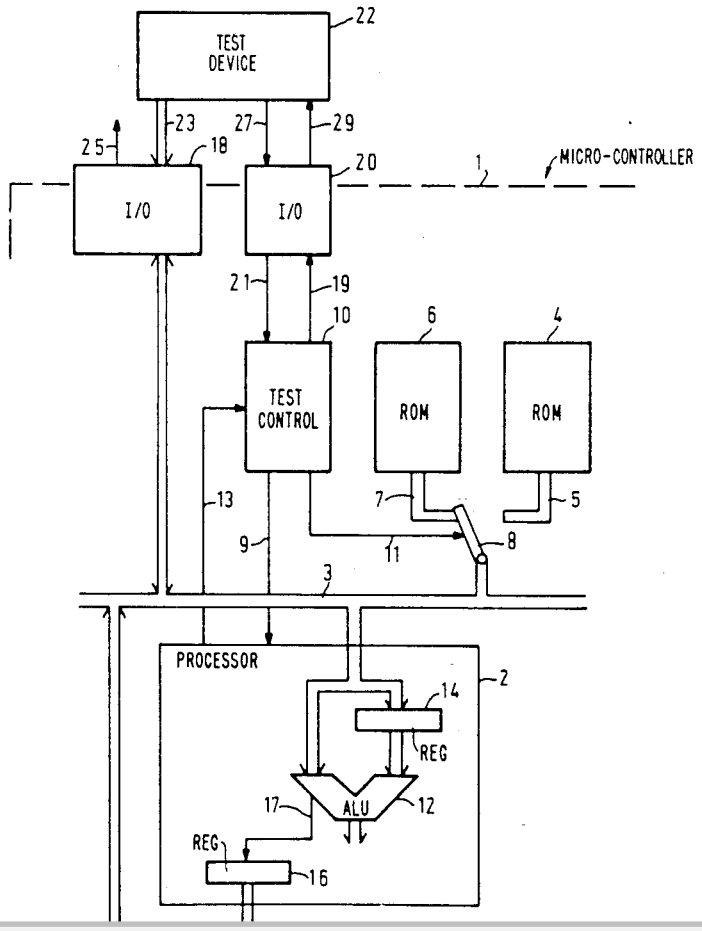
[57] **ABSTRACT**

Microcontrollers generally comprise, in addition to the actual processor, a program memory which is constructed as a read-only memory. In order to enable testing of the contents of the program memory without making these contents also available to the environment of the microcontroller, the reference data of the program are externally supplied and the comparison is performed inside the microcontroller. In accordance with the invention this test is preferably performed as a small test program which is preferably stored in an additional read-only memory in the microcontroller which operates in the test mode and which performs this test. Consequently, except for the memory for the test program, this test program requires hardly any additional hardware.

14 Claims, 2 Drawing Sheets



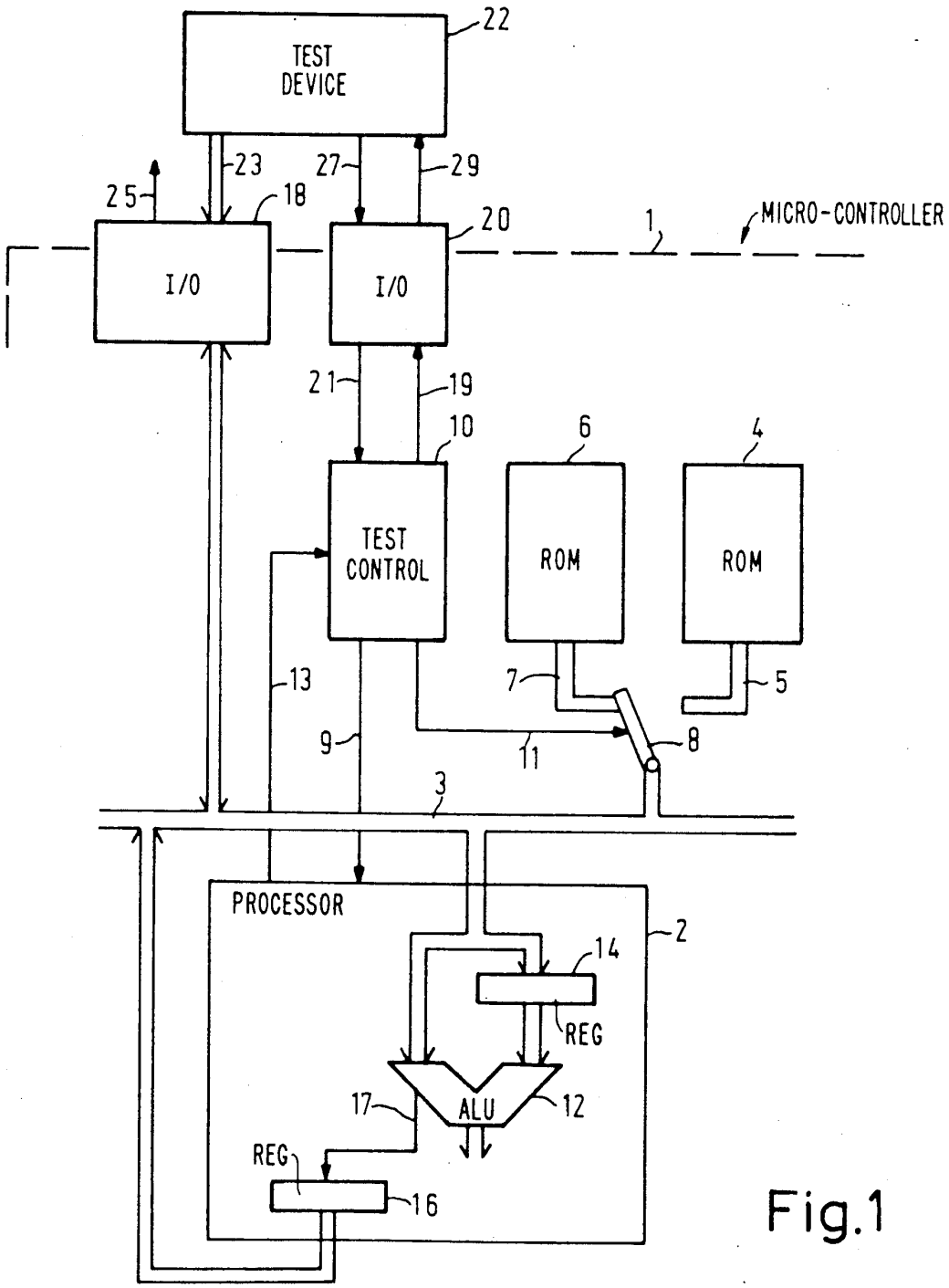


Fig.1

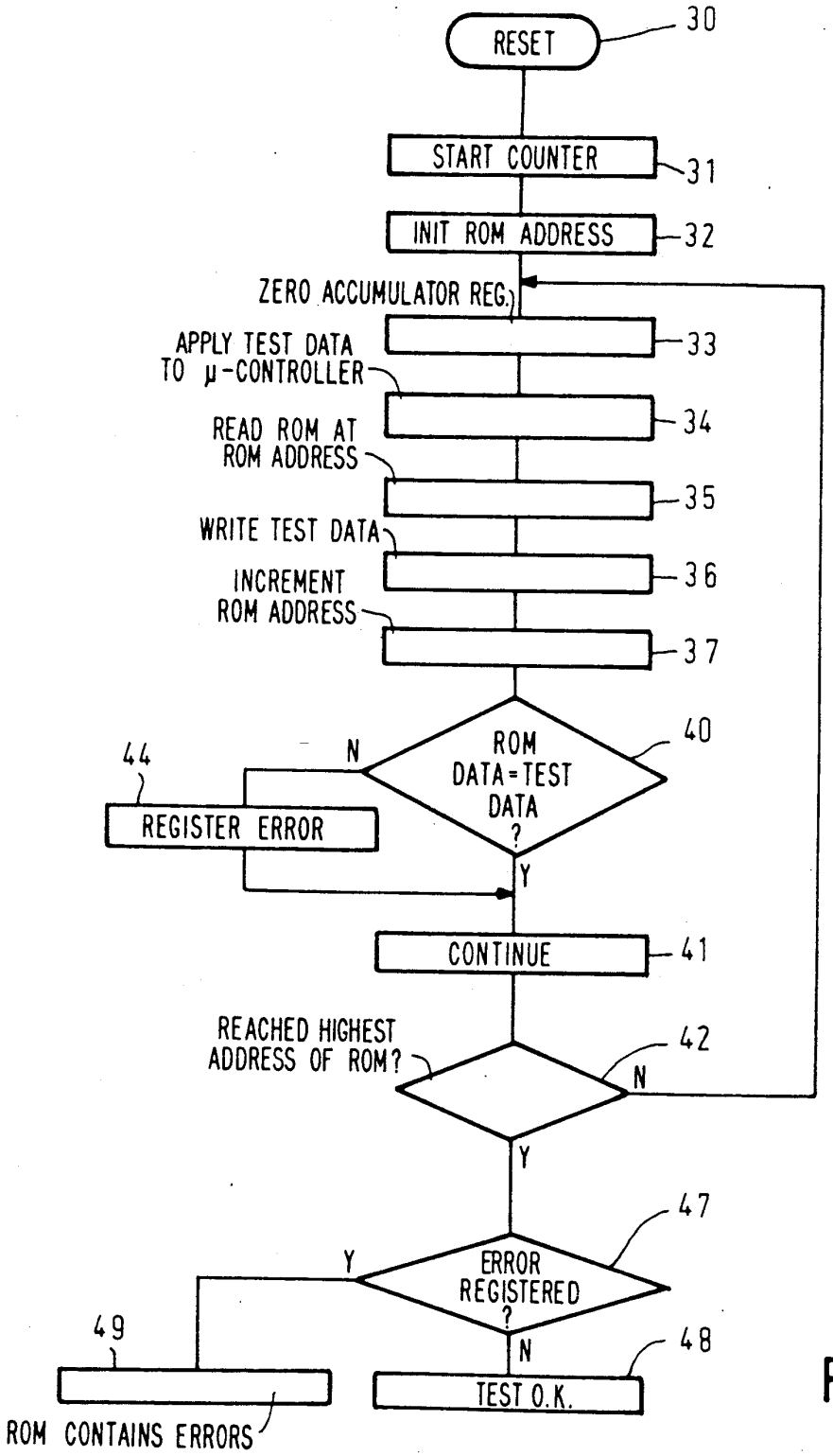


Fig.2

METHOD OF TESTING A READ-ONLY MEMORY AND DEVICE FOR PERFORMING THE METHOD

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a method of testing the contents of a read-only memory in an integrated circuit which also comprises a processor which is controlled by the contents of the read-only memory and also comprises an arithmetic unit and a storage register. The processor is connected to external connections of the integrated circuit and is switchable to a test mode in which the contents of the read-only memory in the integrated circuit are compared with externally supplied test data, an error message is generated in the case of non-correspondence. The invention also relates to a device for performing the method.

2. Prior Art

A method of this kind and an appropriate device are known from U.S. Pat. No. 4,777,586. The program stored in the read-only memory is often developed by the customer at substantial expense, possibly with the assistance of the manufacturer of the microcontroller, so that this program represents a substantial value. In order to ensure that a third party cannot acquire such a microcontroller and read the contents of the read-only memory in order to build or program microcontrollers so that said third party would save the expenditure for the development of the program, testing of the contents of the read-only memory must be possible without these contents being directly detectable from the outside.

In accordance with said U.S. Pat. No. 4,777,586 this is realized in that the contents of the read-only memory are read by means of a separately generated clock signal in order to be applied to a separate comparator which receives externally applied test data upon inversion of said clock signal. The occurrence of errors is stored and output to the environment, via a separate output, after a predetermined number of test steps. A separate counter is required for counting-this number of test steps. The comparator is provided with registers for the intermediate storage of the data read from the read-only memory and the test data. Thus, a number of additional elements are required for testing the contents of the read-only memory, which elements require an additional surface area on the integrated circuit.

SUMMARY OF THE INVENTION

Therefore, it is an object of the invention to provide a method of the kind set forth which enables the testing of the contents of the read-only memory in the integrated circuit to be performed with a minimum number of modifications, i.e. with a minimum amount of hardware.

To achieve this, in accordance with the invention there is provided a test program which is stored in the processor and which is activated in the test mode of the processor. Upon execution of said test program by the processor the contents of the read-only memory are successively read and applied, together with the corresponding, externally supplied test data, to the arithmetic unit for comparison. Any error message which occurs is stored in the storage register and is output only at the end of the test program via a connection which acts as a data connection during normal operation of the processor.

Thus, only a small additional memory will be required for the test program which need comprise only few instructions, and for the remainder of the execution of the test use is made exclusively of elements of the processor or the integrated circuit which have already been provided for normal operation. As a result, with the exception of the additional test program memory, substantially no modifications are required for performing the test in the integrated circuit; additional connections, notably for the error message, are not required either.

In principle it is sufficient to obtain information concerning the correctness of the contents of the read-only memory or whether an error has occurred. For many purposes, for example for correction, if any, of the manufacturing process, however, it is also advantageous to know whether many errors are present in the contents of the read-only memory. In a version of the method in accordance with the invention, therefore, each error message occurring is temporarily stored and at the end of the test program a message concerning the number of error messages is output to the environment. This number of error messages can again be determined, stored and output merely by way of program steps of the processor, without additional hardware being required.

A device for performing the method in accordance with the invention, comprising an integrated circuit which comprises a processor having an arithmetic unit and at least one storage register and one read-only memory as well as a number of external connections, at least one of which is connected to a test device supplying test data, is characterized in that the integrated circuit comprises a test program memory for storing control instructions of a test program in that, after having been switched to the test mode, the processor reads control instructions from the test program memory and successively reads, under the control of these control instructions, the data from the read-only memory and applies these data, together with the test data supplied, to the arithmetic unit for comparison, and in that in the case of a control signal indicating non-correspondence of the supplied data the arithmetic unit modifies the contents of the storage register with respect to a predetermined initial state and applies, at the end of the test program, the contents of the storage register to a connection which acts as a data output during normal operation of the integrated circuit.

In an embodiment of the device in accordance with the invention the processor increments the contents of the storage register, the contents being a binary number, by one unit in response to each control signal from the arithmetic unit. This can be realized by way of appropriate instructions in the test program.

In order to minimize the modification of customary microcontrollers required for performing the test of the ROM contents in accordance with the invention, in a further embodiment of the invention the read-only memory and the test program memory are connected to the processor via a switch which is switched in dependence on the test mode and on the progress of the test program. Thus, the processor can be controlled successively by the test program memory and the read-only memory as the actual program memory. The switch consists of, for example the bus switches already present at the output of the memory.

The test program memory may be realized in various ways. Preferably, the test program memory is a read-only memory. The contents thereof are then defined,

like the contents of the read-only memory for the program, during the manufacture of the integrated circuit and cannot be abusively modified.

It may also be that the contents of the test program memory include errors, so that an error in the contents of the read-only memory can become apparent for the program, even though it is actually correct and the microcontroller is, therefore operational, because the test program is not used during normal operation. Therefore, the contents of the test program memory are preferably accessible from outside the integrated circuit. Thus, first the contents of the test program memory are then tested, which can be customarily done by way of a comparison outside the integrated circuit because the contents of the test program memory are of no significance to third parties. It is only when the test program is correct that the actual testing of the read-only memory for the program can be performed, so that an error message then occurring can in any case be attributed to an error in the contents of the program memory.

BRIEF DESCRIPTION OF THE DRAWING

Embodiments in accordance with the invention will be described in detail hereinafter with reference to the drawing. Therein:

FIG. **1** shows a diagrammatic block diagram of the essential parts of a device in accordance with the invention,

FIG. **2** shows a flowchart illustrating a possible execution of the method in accordance with the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. **1** shows a microcontroller **1** which is constructed as a monolithic integrated circuit and which is connected to a test device **22**. Only the elements of the microcontroller **1** which are important for the following description are shown; other elements having been omitted for the sake of clarity.

An essential part of the microcontroller **1** is formed by the processor **2**, also referred to as CPU, which comprises a number of circuits, only the circuits which are important for the following description being shown. First of all there is the arithmetic and logic unit **12** which is generally referred to as ALU. There is also shown a register **14** whose output is connected to a data input of the ALU, the other input of the ALU **12** and the input of the register being connected to an internal bus **3** (diagrammatically shown). A control output **17** of the ALU **12**, carrying a signal when the result of the logic operation performed in the ALU **12** is unequal to zero, is connected to a further register **16** via program-controlled switches (not shown).

There is also provided a program memory **4** which contains the program to be executed by the microcontroller during normal operation and which is constructed as a read-only memory (ROM), as well as a further read-only memory **6** which contains the test program. The output **5** of the ROM **4** and the output **7** of the test program memory **6** can be connected as desired to the internal bus **3** via a switch **8**. The addressing of the memories **4** and **6** is not separately shown and customarily takes place by the processor **2** via address leads in the bus **3**. When the test program operates without loops and branches, the test program memory **6** could also be controlled by a separate address generator, for example a counter.

The switch **8** may be constructed as a multiplexer or be formed by bus data switches customarily connected behind the outputs of the two memories **4** and **6** and is controlled, via the lead **11**, by a test control circuit **10** which controls the test mode in the microcontroller **1** and which itself is influenced by the CPU **2** via the lead **13**. Such a test control circuit **10** is in any case provided for testing the integrated circuit **1**, independent of the described testing of the contents of the ROM **4**.

For test purposes the microcontroller **1** is connected to a test device **22** via the already present input/output circuits **18** and **20**. The input/output circuits **18** and **20** comprise driver circuits for outgoing leads and receiver circuits for incoming leads, which circuits are at least partly controllable or switchable. This holds good notably for the input/output circuits **18** via which data words can be exchanged with externally connected devices, i.e. in this case also with the test device **22**. In the device **18** the outgoing data leads are often associated with a register so that these data need be only briefly generated by the processor **2** and remain externally available for a prolonged period of time.

In order to perform the test, the test device **22** transmits, via the lead **27** which may actually comprise a plurality of leads, a signal for adjusting the test mode, which signal is applied to the test control circuit **10** via the input/output circuit **20** and the lead **21**. Before that, the test device **22** as well as the microcontroller **1** have been set to an initial state by a reset signal (not shown). The test control circuit **10** then sets, via the lead **11**, the switch **8** to the position shown, thus transferring the first test construction from the test program memory **6**, via the bus **3**, to the processor **2** in which it is stored, for example in an instruction register (not shown). Subsequently, further instructions may be given, if any, which set the processor **2** to a desired state. Instead, or in addition thereto, the processor **2** may also be set to the test mode via a connection **9**.

Subsequently, the test control circuit **10** briefly switches over the switch **8** and applies the first data word from the ROM **4**, via the bus **3**, to the processor **2** in which it is temporarily stored in the register **14** and is present on an input of the ALU **12**. Subsequently, the switch **8** is switched back to the position shown and a data word generated on the output lead **23** by the test device **22** and corresponding to the first correct data word in the ROM **4** is applied to the other input of the ALU **12** via the input/output circuit **18** and the bus **3**, after which the two data words are compared, for example by adjusting the ALU for a subtraction or a logic comparison function, if present. On the lead **17** it is merely indicated whether correspondence or non-correspondence has been detected. In the latter case, i.e. the case where the first word in the ROM **4** does not correspond to the predetermined contents, the corresponding signal on the line **17** is written into the register **16**.

After the comparison, or simultaneously therewith, the address for the ROM **4** is incremented by 1 and, moreover, via the lead **13** the test control circuit **10** receives a signal for the end of a test step; in response thereto, the test control circuit **10** issues, via the lead **19**, a synchronization signal which is applied, via the input/output circuit **20** and the lead **29**, to the test device **22** in which it enables the next comparison value on the lead **23**. Furthermore, via the lead **11** the switch **8** is again switched over to the position shown and the next test step is performed in the same manner. Thus, the

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