Comparison of Device and Method Claims in U.S. Patent No. 7,383,453

Device Claims	Method Claims
1. An instruction-processing system with minimized static power leakage, the instruction-processing system comprising:	8. A method for minimizing static power leakage in an instruction-processing system, wherein the instruction-processing system comprises[:]
a core with instruction-processing circuitry;	a core with instruction-processing circuitry,
an area coupled to the core;	an area coupled to the core,
a core voltage provided to the core; and	a core voltage provided to the core, and
an area voltage provided to the area;	an area voltage provided to the area,
wherein in a normal operation mode:	the method comprising: entering a normal operation mode by:
a clock signal to the core is active;	providing a clock signal to the core;
the core voltage is a first value that is sufficient to maintain the state information of the instruction-processing circuitry;	providing the core with a core voltage that is equal to a first value that is sufficient to maintain the state information of the instruction-processing circuitry;
the core is active;	
the area voltage is a second value that is sufficient to maintain the data stored in the area; and	providing the area with an area voltage equal to a second value that is sufficient to maintain the data stored in the area;
the area is active;	
wherein in a first power-saving mode that can be exited upon receipt of an interrupt signal:	entering a first power-saving mode by:

the clock signal to the core is inactive;	disabling the clock signal to the core;
the core voltage is sufficient to maintain the state information of the instruction-processing circuitry; and	providing the core with a core voltage that is sufficient to maintain the state information of the instruction-processing circuitry; and
the area voltage is sufficient to maintain the data stored in the area;	providing the area with an area voltage that is sufficient to maintain the data stored in the area;
	exiting the first power-saving mode upon receipt of an interrupt signal;
wherein in a second power-saving mode that can be exited upon receipt of a signal that is not an interrupt signal:	entering a second power-saving mode by:
the clock signal to the core is inactive;	disabling the clock signal to the core;
the core voltage is less than the first value; and	setting the core voltage to a value less than the first value; and
the area voltage is sufficient to maintain the data stored in the area.	providing the area with an area voltage that is equal to or greater than the second value; and
	exiting the second power-saving mode upon receipt of a signal that is not an interrupt signal.
2. The instruction-processing system of claim 1, wherein the first power-saving mode can be exited upon receipt of a signal that is not an interrupt signal.	9. The method of claim 8, further comprising exiting the first power-saving mode upon receipt of a signal that is not an interrupt signal.
3. The instruction-processing system of claim 1, wherein the area comprises a cache.	10. The method of claim 8, wherein the area comprises a cache.

4. The instruction-processing system of claim 3, wherein the area further comprises cache tags.	11. The method of claim 10, wherein the area further comprises cache tags.