<u>Comparison of Device and Method Claims</u> <u>in U.S. Patent No. 7,383,453</u>

Device Claims	Method Claims
1. An instruction-processing system	8. A method for minimizing static
with minimized static power leakage,	power leakage in an instruction-
the instruction-processing system	processing system, wherein the
comprising:	instruction-processing system
	comprises[:]
a core with instruction-processing	a core with instruction-
circuitry;	processing circuitry,
an area coupled to the core;	an area coupled to the core,
a core voltage provided to the	a core voltage provided to the
core; and	core, and
an area voltage provided to the	an area voltage provided to the
area;	area,
wherein in a normal operation	the method comprising: entering a
mode:	normal operation mode by:
a clock signal to the core is	providing a clock signal to
active;	the core;
the core voltage is a first	providing the core with a
value that is sufficient to	core voltage that is equal
maintain the state	to a first value that is
information of the	sufficient to maintain the
instruction-processing	state information of the
circuitry;	instruction-processing
	circuitry;
the core is active;	
the area voltage is a second	providing the area with an
value that is sufficient to	area voltage equal to a
maintain the data stored in	second value that is
the area; and	sufficient to maintain the
	data stored in the area;
the area is active;	
wherein in a first power-saving	entering a first power-saving
mode that can be exited upon	mode by:
receipt of an interrupt signal:	

the clock signal to the core	disabling the clock signal
is inactive;	to the core;
the core voltage is	providing the core with a
sufficient to maintain the	core voltage that is
state information of the	sufficient to maintain the
instruction-processing	state information of the
circuitry; and	instruction-processing
	circuitry; and
the area voltage is	providing the area with an
sufficient to maintain the	area voltage that is
data stored in the area;	sufficient to maintain the
	data stored in the area;
	exiting the first power-saving
	mode upon receipt of an
	interrupt signal;
wherein in a second power-	entering a second power-saving
saving mode that can be exited	mode by:
upon receipt of a signal that is not	
an interrupt signal:	
the clock signal to the core	disabling the clock signal
is inactive;	to the core;
the core voltage is less	setting the core voltage to
than the first value; and	a value less than the first
	a value less mail the first
	value; and
the area voltage is	value; and providing the area with an
the area voltage is sufficient to maintain the	value; and providing the area with an area voltage that is equal
the area voltage is sufficient to maintain the data stored in the area.	value; and providing the area with an area voltage that is equal to or greater than the
the area voltage is sufficient to maintain the data stored in the area.	value; and providing the area with an area voltage that is equal to or greater than the second value; and
the area voltage is sufficient to maintain the data stored in the area.	value; and providing the area with an area voltage that is equal to or greater than the second value; and exiting the second power-saving
the area voltage is sufficient to maintain the data stored in the area.	value; and providing the area with an area voltage that is equal to or greater than the second value; and exiting the second power-saving mode upon receipt of a signal
the area voltage is sufficient to maintain the data stored in the area.	value; and providing the area with an area voltage that is equal to or greater than the second value; and exiting the second power-saving mode upon receipt of a signal that is not an interrupt signal.
the area voltage is sufficient to maintain the data stored in the area. 2. The instruction-processing system of	 value; and providing the area with an area voltage that is equal to or greater than the second value; and exiting the second power-saving mode upon receipt of a signal that is not an interrupt signal. 9. The method of claim 8, further
the area voltage is sufficient to maintain the data stored in the area. 2. The instruction-processing system of claim 1, wherein the first power-saving	 value; and providing the area with an area voltage that is equal to or greater than the second value; and exiting the second power-saving mode upon receipt of a signal that is not an interrupt signal. 9. The method of claim 8, further comprising exiting the first power-
the area voltage is sufficient to maintain the data stored in the area. 2. The instruction-processing system of claim 1, wherein the first power-saving mode can be exited upon receipt of a	 value; and providing the area with an area voltage that is equal to or greater than the second value; and exiting the second power-saving mode upon receipt of a signal that is not an interrupt signal. 9. The method of claim 8, further comprising exiting the first power-saving mode upon receipt of a signal
 the area voltage is sufficient to maintain the data stored in the area. 2. The instruction-processing system of claim 1, wherein the first power-saving mode can be exited upon receipt of a signal that is not an interrupt signal. 	 value; and providing the area with an area voltage that is equal to or greater than the second value; and exiting the second power-saving mode upon receipt of a signal that is not an interrupt signal. 9. The method of claim 8, further comprising exiting the first power-saving mode upon receipt of a signal that is not an interrupt signal.
 the area voltage is sufficient to maintain the data stored in the area. 2. The instruction-processing system of claim 1, wherein the first power-saving mode can be exited upon receipt of a signal that is not an interrupt signal. 3. The instruction-processing system of 	 value; and providing the area with an area voltage that is equal to or greater than the second value; and exiting the second power-saving mode upon receipt of a signal that is not an interrupt signal. 9. The method of claim 8, further comprising exiting the first power-saving mode upon receipt of a signal that is not an interrupt signal. 10. The method of claim 8, wherein the
 the area voltage is sufficient to maintain the data stored in the area. 2. The instruction-processing system of claim 1, wherein the first power-saving mode can be exited upon receipt of a signal that is not an interrupt signal. 3. The instruction-processing system of claim 1, wherein the area comprises a 	 value; and providing the area with an area voltage that is equal to or greater than the second value; and exiting the second power-saving mode upon receipt of a signal that is not an interrupt signal. 9. The method of claim 8, further comprising exiting the first power-saving mode upon receipt of a signal that is not an interrupt signal. 10. The method of claim 8, wherein the area comprises a cache.

4. The instruction-processing system of	11. The method of claim 10, wherein
claim 3, wherein the area further	the area further comprises cache tags.
comprises cache tags.	